**********Default**********

01/26/24

jpeg lifting lo & hi pass filters

**********Default**********

```
cd virtual-python-xstools/

python3 -m venv env ; source env/bin/activate

cd SDRAM_Controller/wkg/

python3 jpeg.py

// File: jpeg.v
// Generated by MyHDL 0.11.43
// Date: Fri Jan 26 17:36:41 2024


`timescale 1ns/10ps

module jpeg (
    clk,
    l_s,
    r_s,
    s_s,
    res_s,
    lohipass,
    fwd_inv,
    ex
);


input clk;
input signed [15:0] l_s;
input signed [15:0] r_s;
input signed [15:0] s_s;
output signed [15:0] res_s;
reg signed [15:0] res_s;
input lohipass;
input fwd_inv;
input ex;



// lohipass 1 lo 0 hi pass filter
// fwd_inv 1 fwd 0 inv
always @(posedge clk) begin: JPEG_JPEG_HDL
    if (ex) begin
        if (lohipass) begin
            if (fwd_inv) begin
                res_s <= (s_s - ($signed(l_s >>> 1) + $signed(r_s >>> 1)));
```

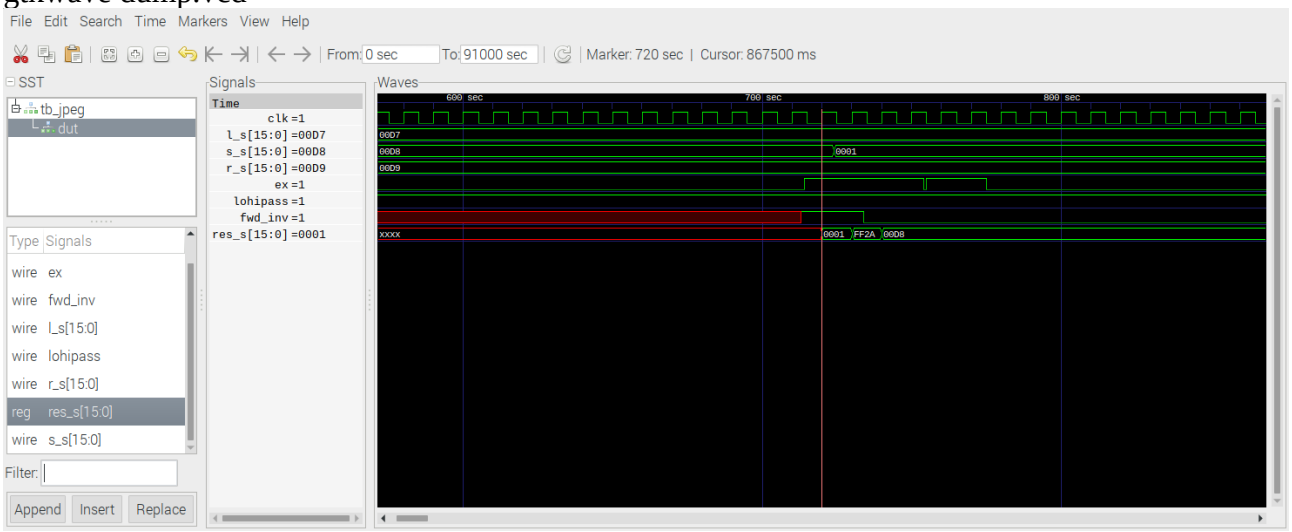
```
            end
            else begin
                res_s <= (s_s + ($signed(l_s >>> 1) + $signed(r_s >>> 1)));
            end
        end
        else begin
            if (fwd_inv) begin
                res_s <= (s_s + $signed(((l_s + r_s) + 2) >>> 2));
            end
            else begin
                res_s <= (s_s - $signed(((l_s + r_s) + 2) >>> 2));
            end
        end
    end
end

endmodule


module tb_jpeg;

reg clk;
reg [15:0] l_s;
reg [15:0] r_s;
reg [15:0] s_s;
wire [15:0] res_s;
reg lohipass;
reg fwd_inv;
reg ex;


always #5 clk = (clk === 1'b0);

jpeg dut(
    clk,
    l_s,
    r_s,
    s_s,
    res_s,
    lohipass,
    fwd_inv,
            ex
);

initial
            begin
            # 100 ex = 0;
            # 200 lohipass = 1;

            # 200 l_s = 215;
            # 1 s_s = 216;
            # 1 r_s = 217;
```

```
        # 210 lohipass = 1;
        # 1 fwd_inv = 1;
        # 1 ex = 1;
        # 10 s_s = res_s;
        # 10 fwd_inv = 0;
        //# 10 lohipass = 0;
        # 20 ex = 0;
        //# 320 s_s = res_s;

        # 1 ex = 1;
        # 20 ex = 0;
        # 400 s_s = 216;
        # 410 lohipass = 0;
        # 1 fwd_inv = 1;
        # 1 ex = 1;
        # 450 s_s = res_s;
        # 10 fwd_inv = 0;
        end
 initial

   begin
     // Required for EDA Playground
     $dumpfile("dump.vcd");
     $dumpvars(0);
   end
 initial
                begin
     #91000;
     $finish();
 end
endmodule
```

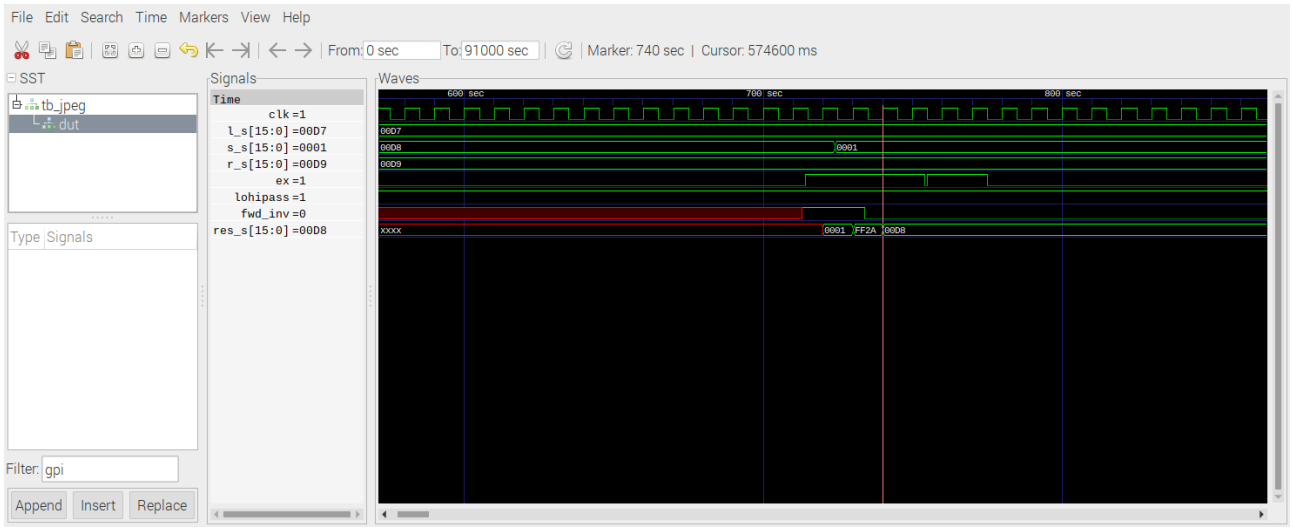
iverilog -o dsn -f filelist

vvp dsn

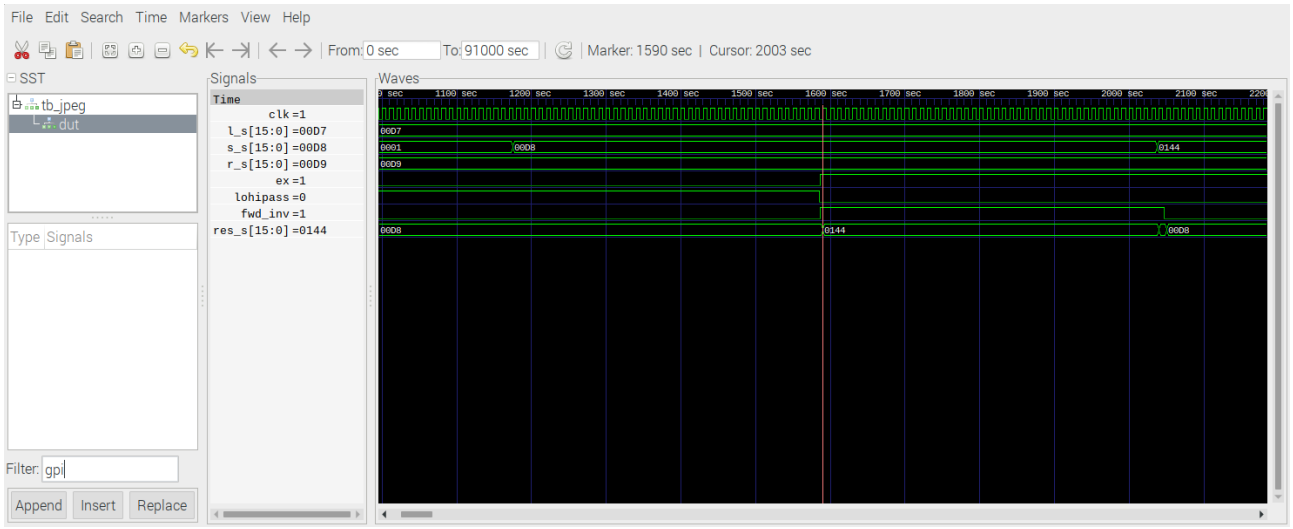
gtkwave dump.vcd



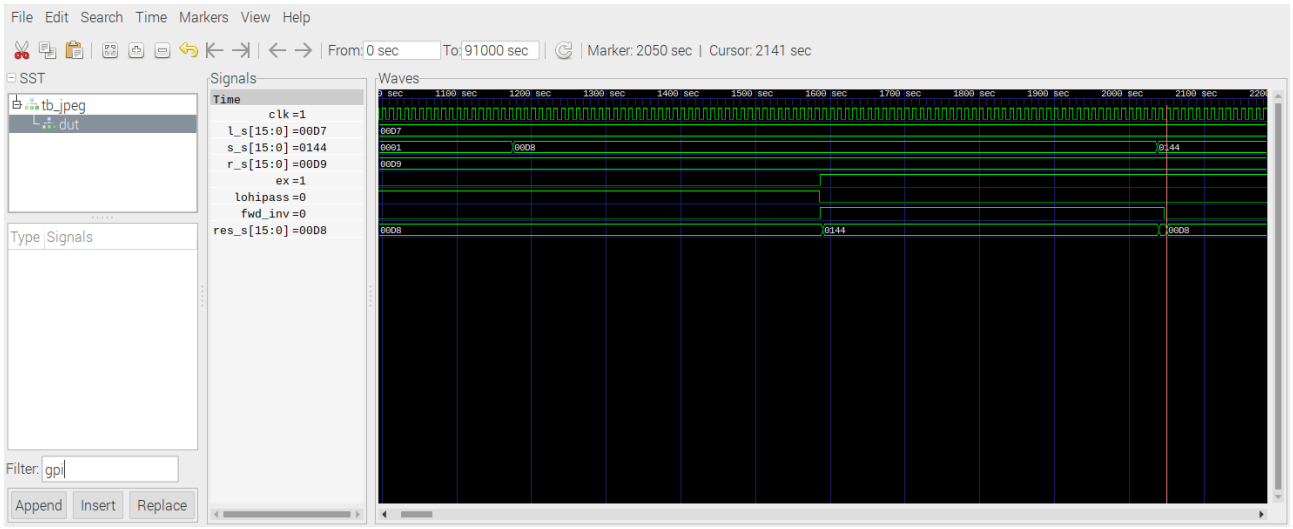
Given 0x00d7, 0xx00d8, & 0x00d9 results 0x0001 lo pass fwd lifting step.



Given 0x00d7, 0x0001, & 0x00d9 results 0x00d8 lo pass inv lifting step.

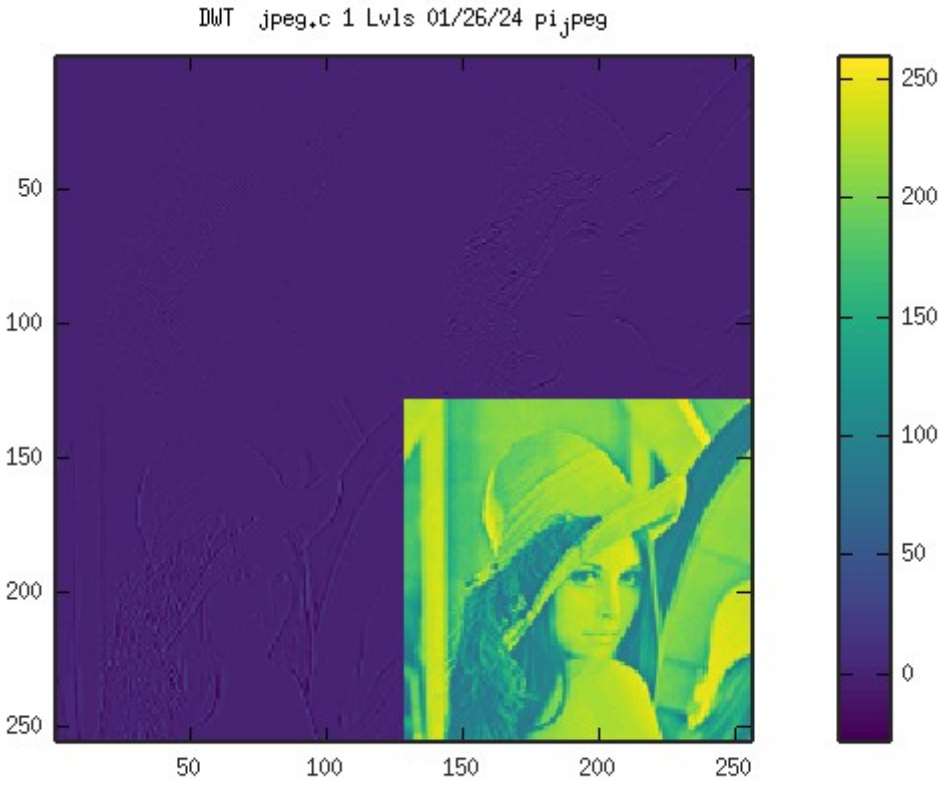


Given 0x00d7, 0x00d8, & 0x00d9 results 0x0144 hi pass fwd lifting step.

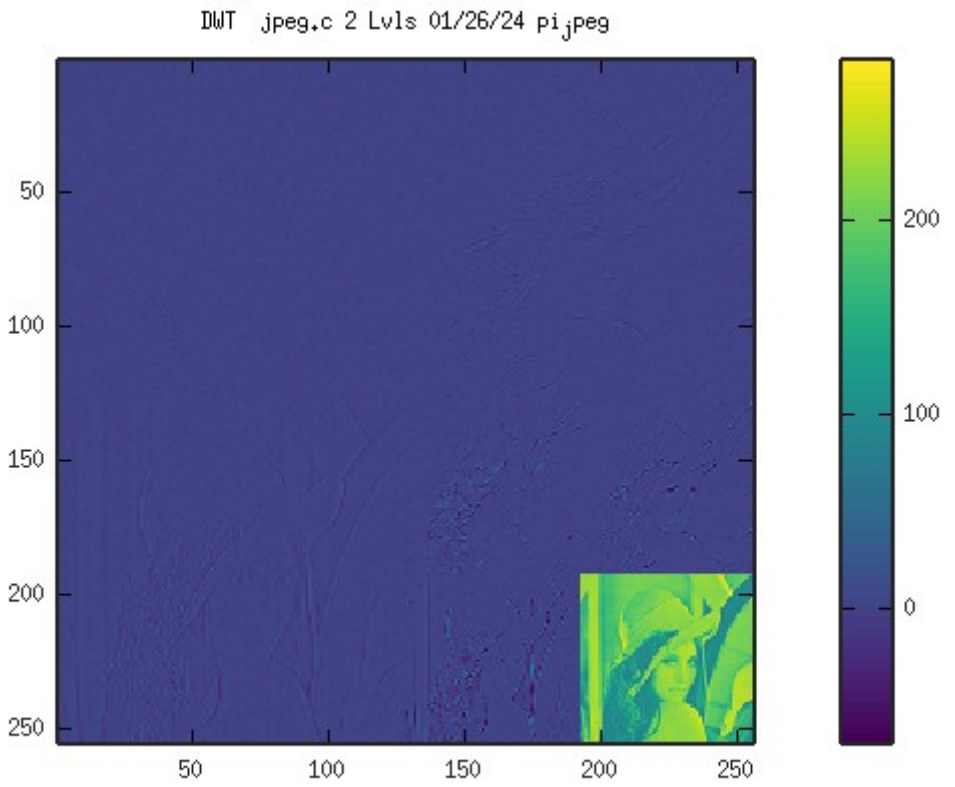


Given 0x00d7, 0x0144, & 0x00d9 results 0x00d8 hi pass inv lifting step.
./buildpi_lift.sh
./pi_jpeg 0 1

buf_red = 0x9eff5010
fwd_inv = 0xbad552a0
spliting red sub band
fwd lifting step only
w = 0x100 buf_red wptr = 0x9eff5010 alt = 0x9f035010 fwd_inverse = 0xbad552a0 fwd_inverse = 0x1
starting red dwt
finished ted dwt



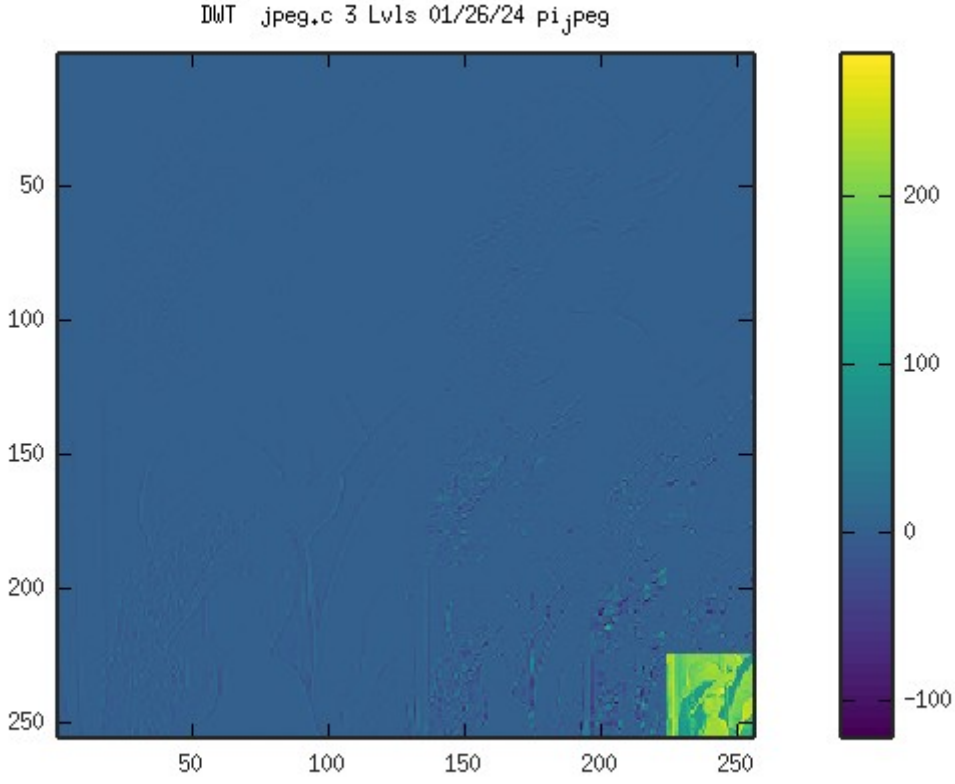
y2=-67.8909
octave
rgb



y2=-118.803

octave

rgb



y2= 318.416