

*****Draft*****

Write Read Simulation

04/07/21

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Goal

```
. testbuilds/catzip-newautofpga/catzip/myenv-a.sh
```

```
devel@mypi3-16:~ $ cd testbuilds/catzip-newautofpga/catzip/sim/verilated/
```

```
devel@mypi3-16:~/testbuilds/catzip-newautofpga/catzip/sim/verilated $ ./arm-main_tb -trace wr-  
rd.vcd
```

```
Listening on port 8363
```

```
Listening on port 8364
```

```
> T
```

```
CMD: Only sent 0 bytes of 3!
```

```
Accepted CMD connection
```

```
POLL = 1
```

```
RCVD: 13 bytes
```

```
< A01000001W55
```

```
> A01000001K00000000
```

```
POLL = 1
```

```
RCVD: 0 bytes
```

```
< [CLOSED]
```

```
Accepted CMD connection
```

```
POLL = 1
```

```
RCVD: 13 bytes
```

```
< A01000005Waa
```

```
> A01000005K00000000
```

```
POLL = 1
```

```
RCVD: 0 bytes
```

```
< [CLOSED]
```

```
Accepted CMD connection
```

```
POLL = 1
```

```
RCVD: 12 bytes
```

```
< A01000009W1
```

```
> A01000009K00000000
```

```
POLL = 1
```

```
RCVD: 0 bytes
```

```
< [CLOSED]
```

```
Accepted CMD connection
```

```
POLL = 1
```

```
RCVD: 12 bytes
```

```
< A0100000dW2
```

```
> A0100000dK00000000
```

```
POLL = 1
```

```
RCVD: 0 bytes
```

< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 16 bytes
< A01000011W10000
> A01000011K00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 16 bytes
< A01000015W20000
> A01000015K00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 11 bytes
< A01000001R
> A01000001R00000055
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 11 bytes
< A01000005R
> A01000005R000000aa
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 11 bytes
< A01000009R
> A01000009R00000001
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 11 bytes
< A0100000dR
> A0100000dR00000002
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 11 bytes

```
< A01000011R
> A01000011R00010000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 11 bytes
< A01000015R
> A01000015R00020000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
^C
```

```
devel@mypi3-16:~/testbuilds/catzip-newautofpga/catzip/sim/verilated $ gtkwave wr-rd.vcd
```

```
devel@mypi3-16:~ $ cd testbuilds/catzip-newautofpga/catzip/sw/host
```

```
devel@mypi3-16:~/testbuilds/catzip-newautofpga/catzip/sw/host $ ./wr.sh
01000000 ( SDRAM)-> 00000055
01000004 ( )-> 000000aa
01000008 ( )-> 00000001
0100000c ( )-> 00000002
01000010 ( )-> 00010000
01000014 ( )-> 00020000
01000000 ( SDRAM) : [...U] 00000055
01000004 ( ) : [...] 000000aa
01000008 ( ) : [...] 00000001
0100000c ( ) : [...] 00000002
01000010 ( ) : [...] 00010000
01000014 ( ) : [...] 00020000
```


Image 0

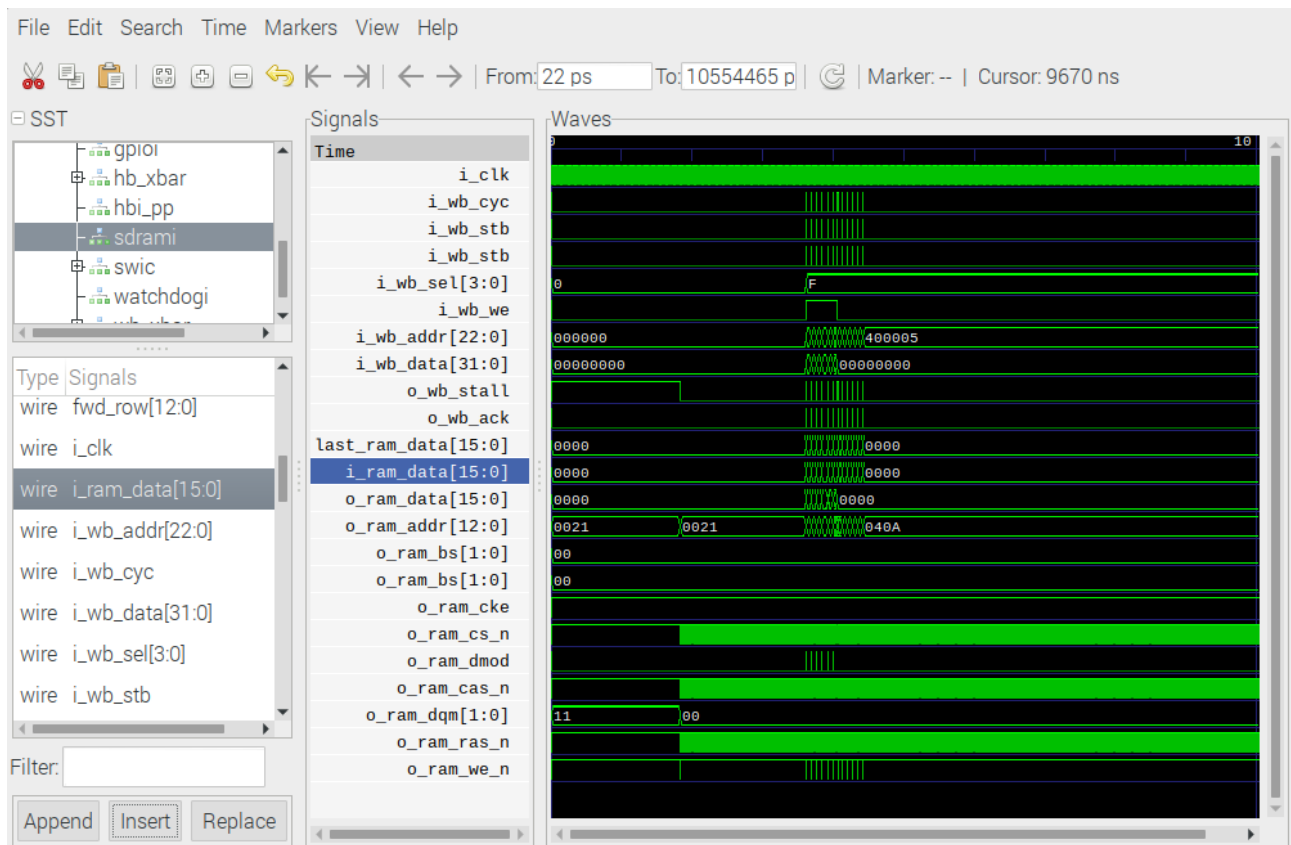


image 1

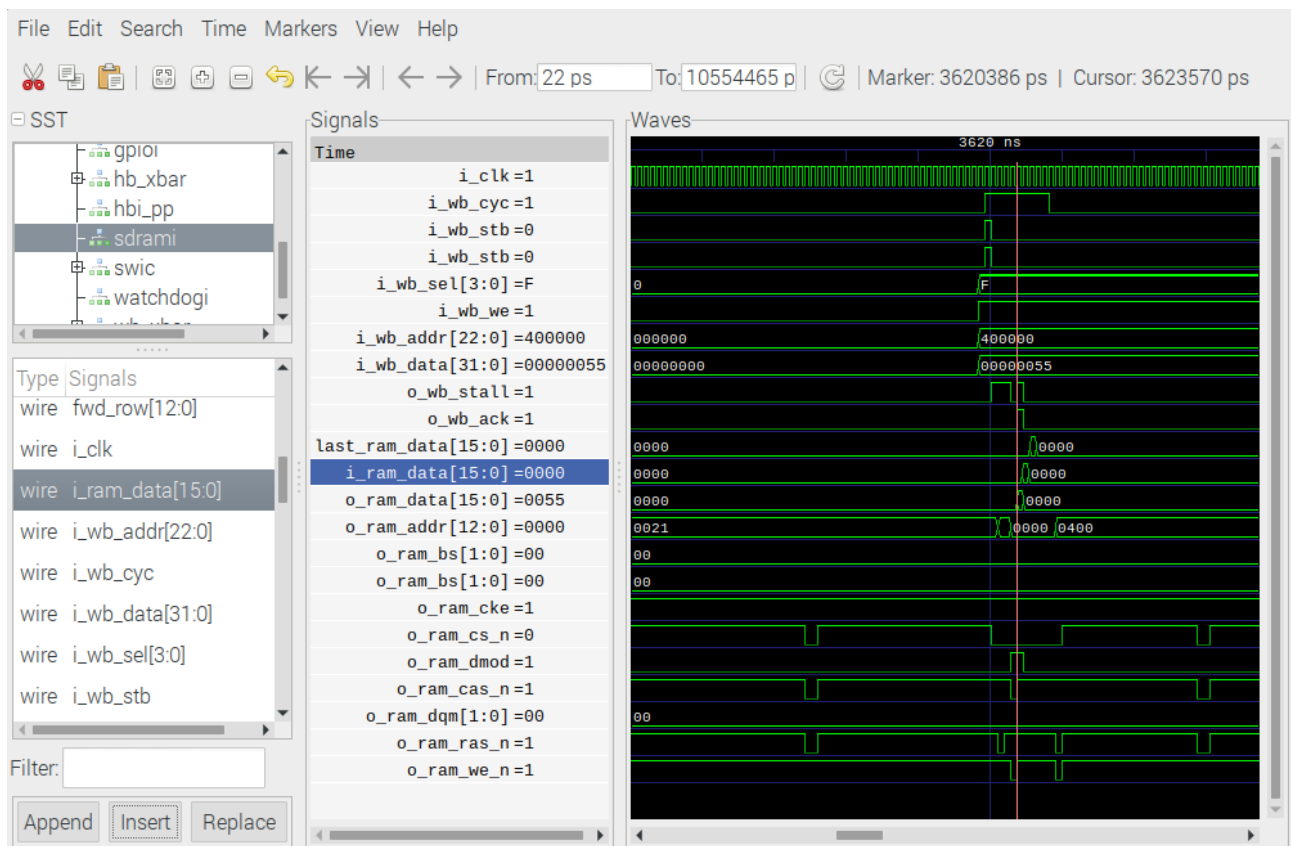


image 2

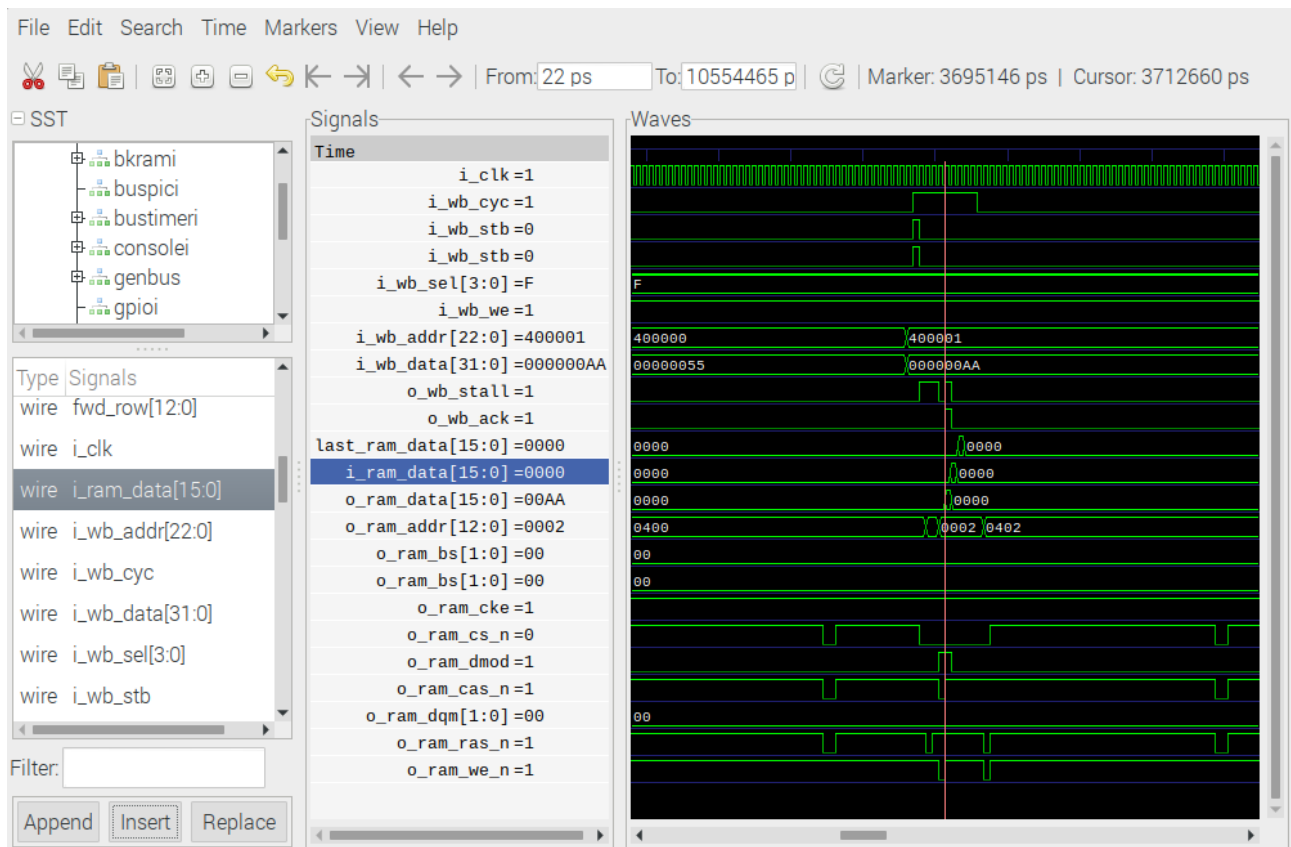


image 3

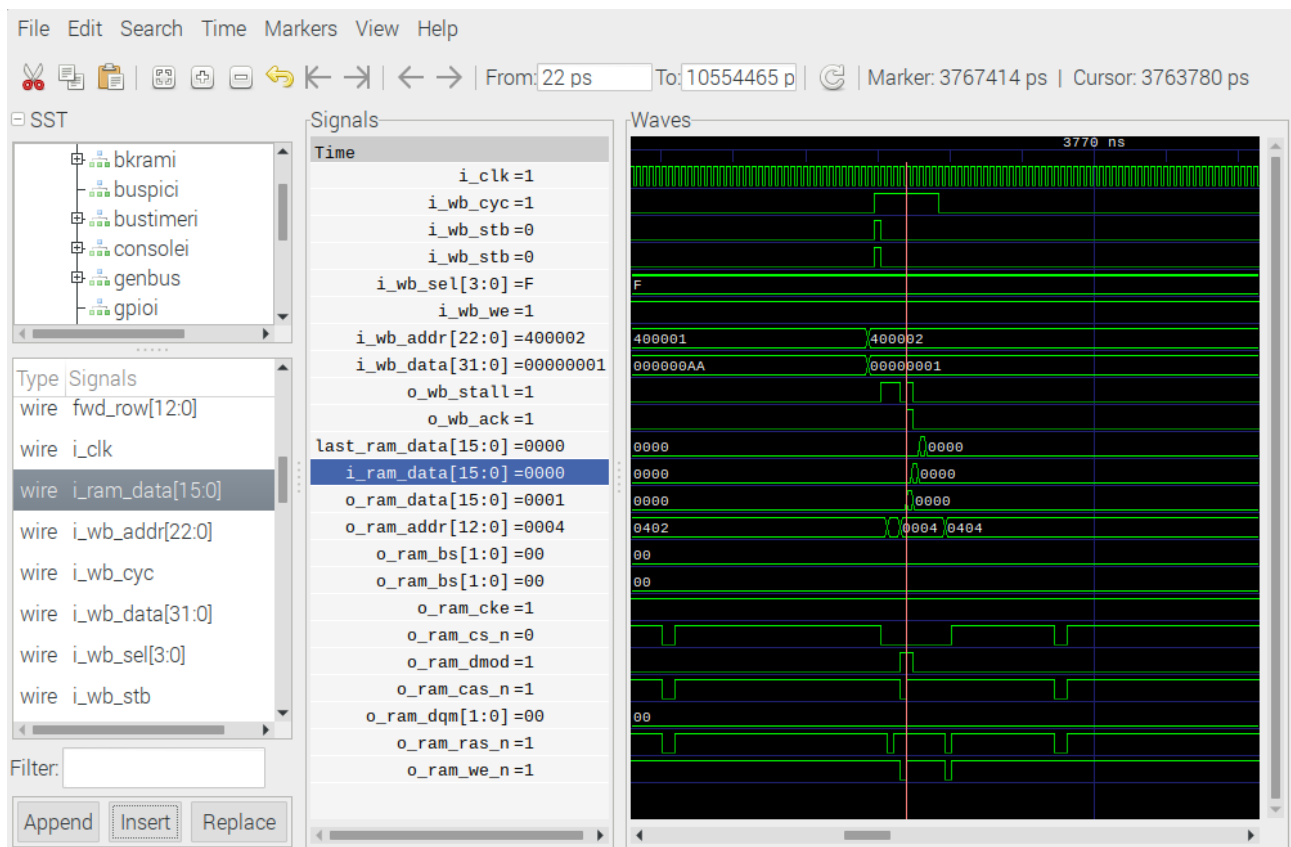


image 4

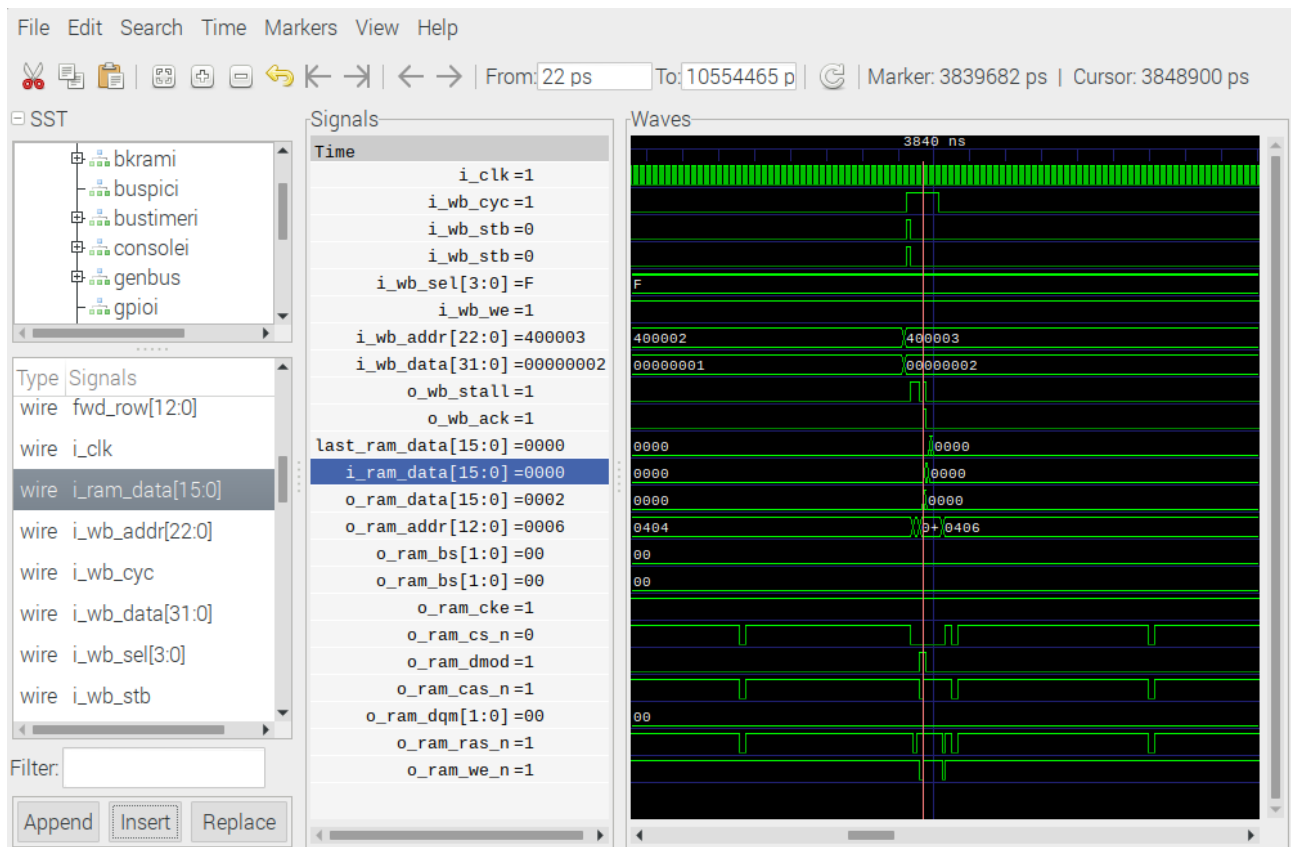


image 5

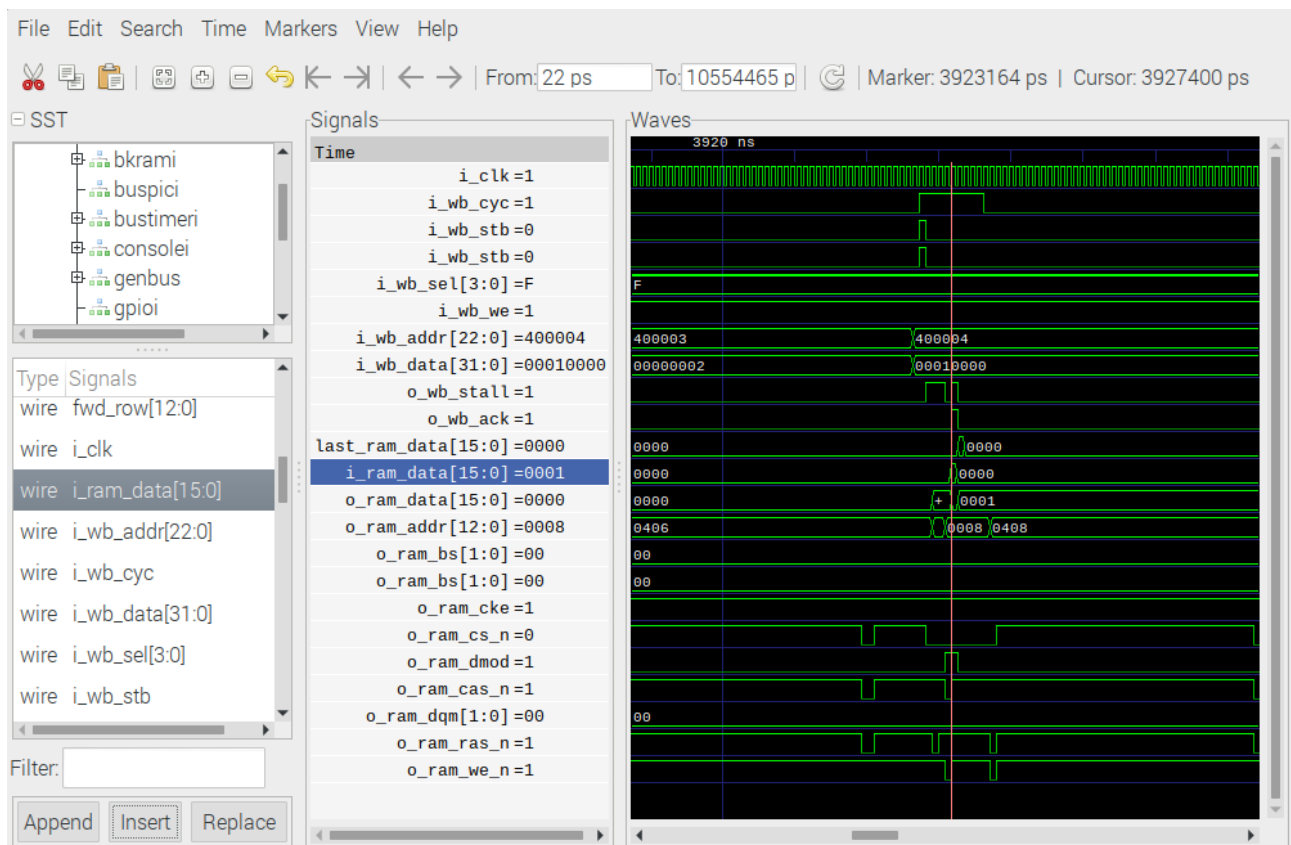


image 6

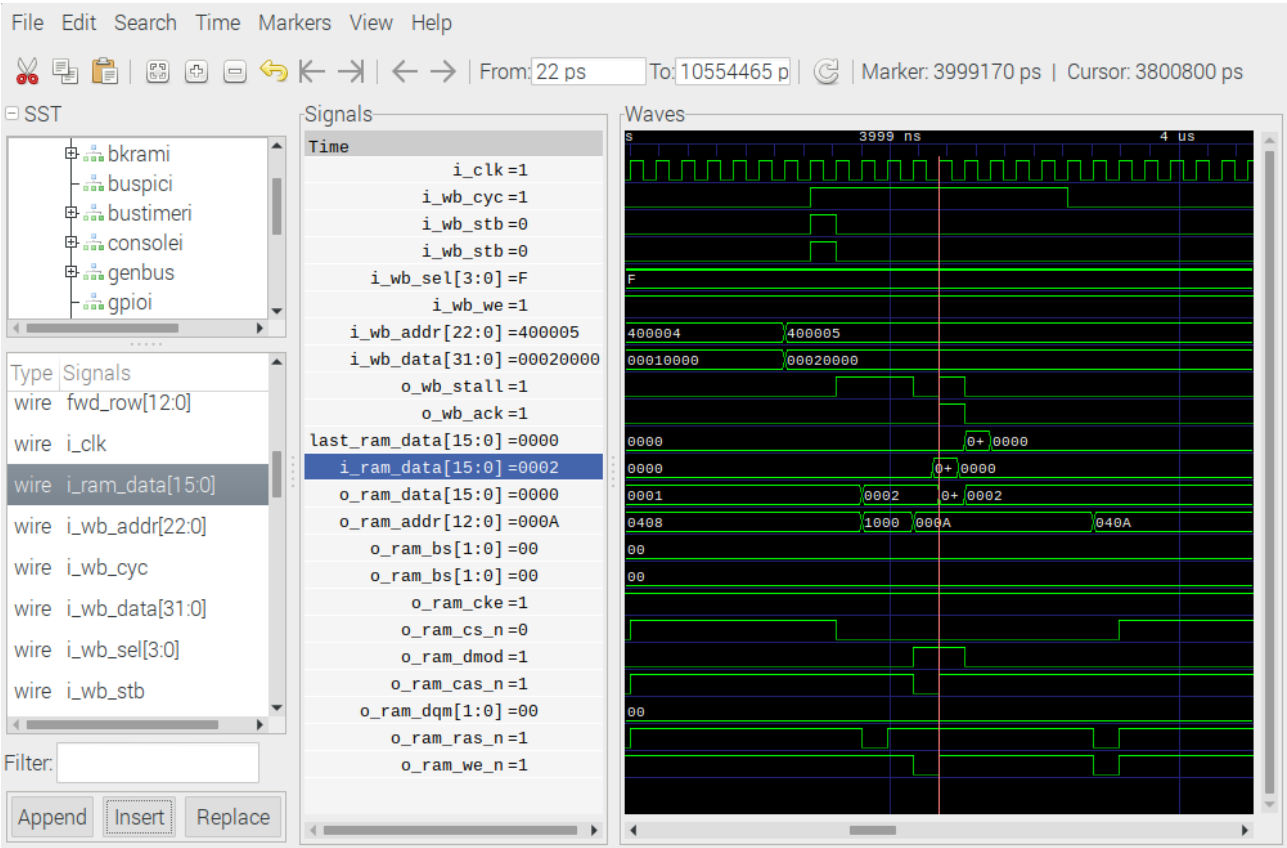


image 7

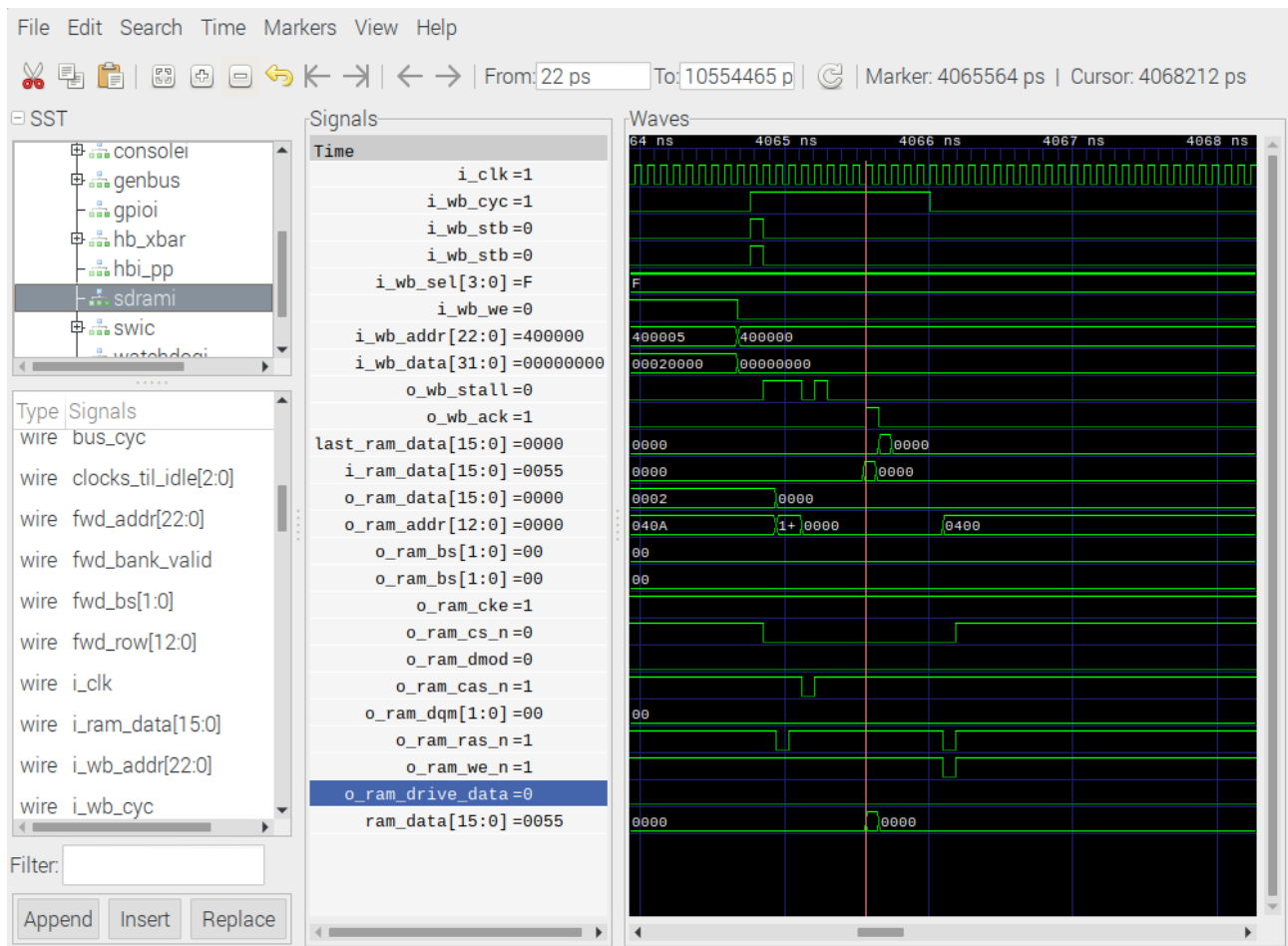


image 8

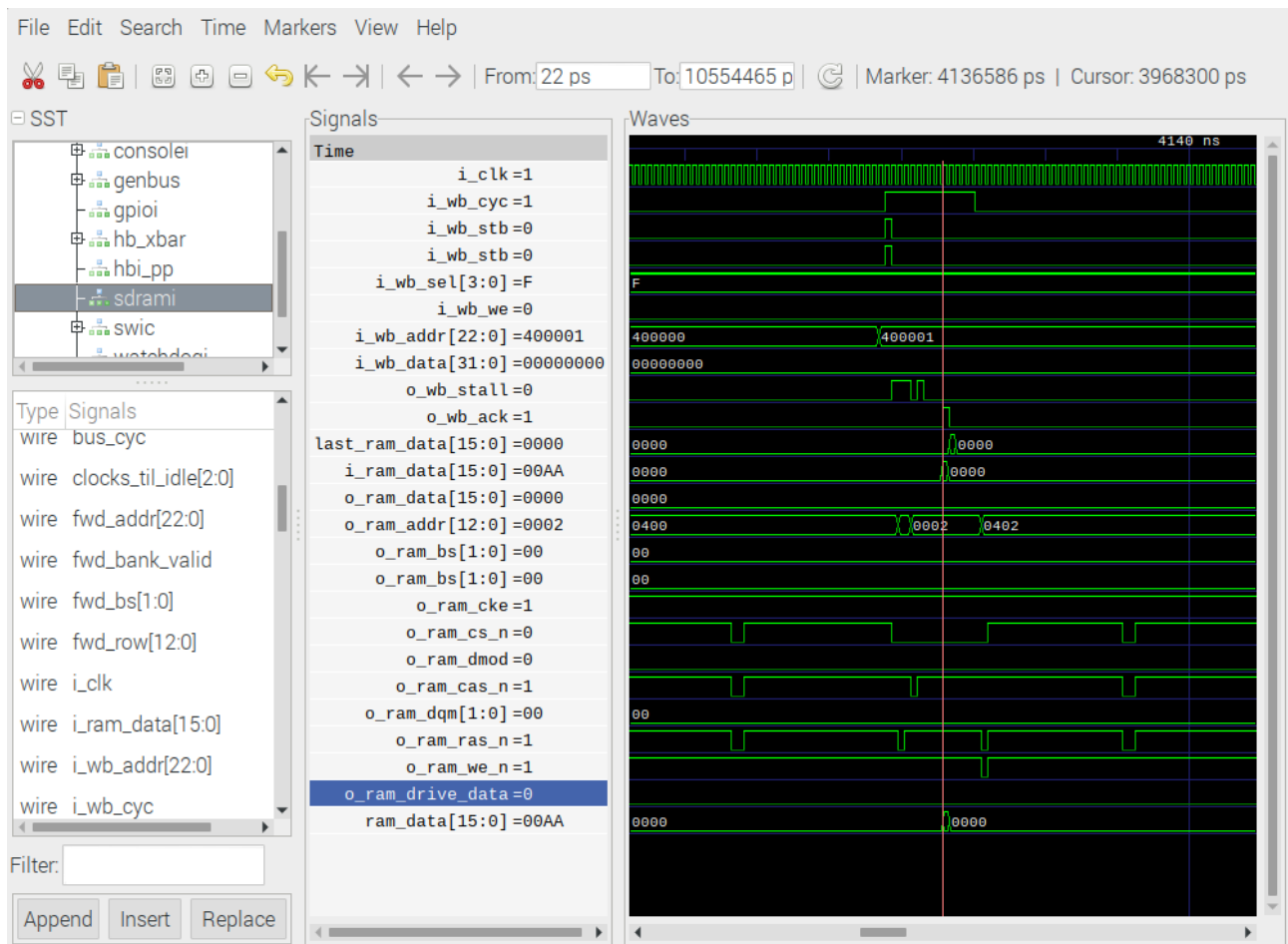


image 9

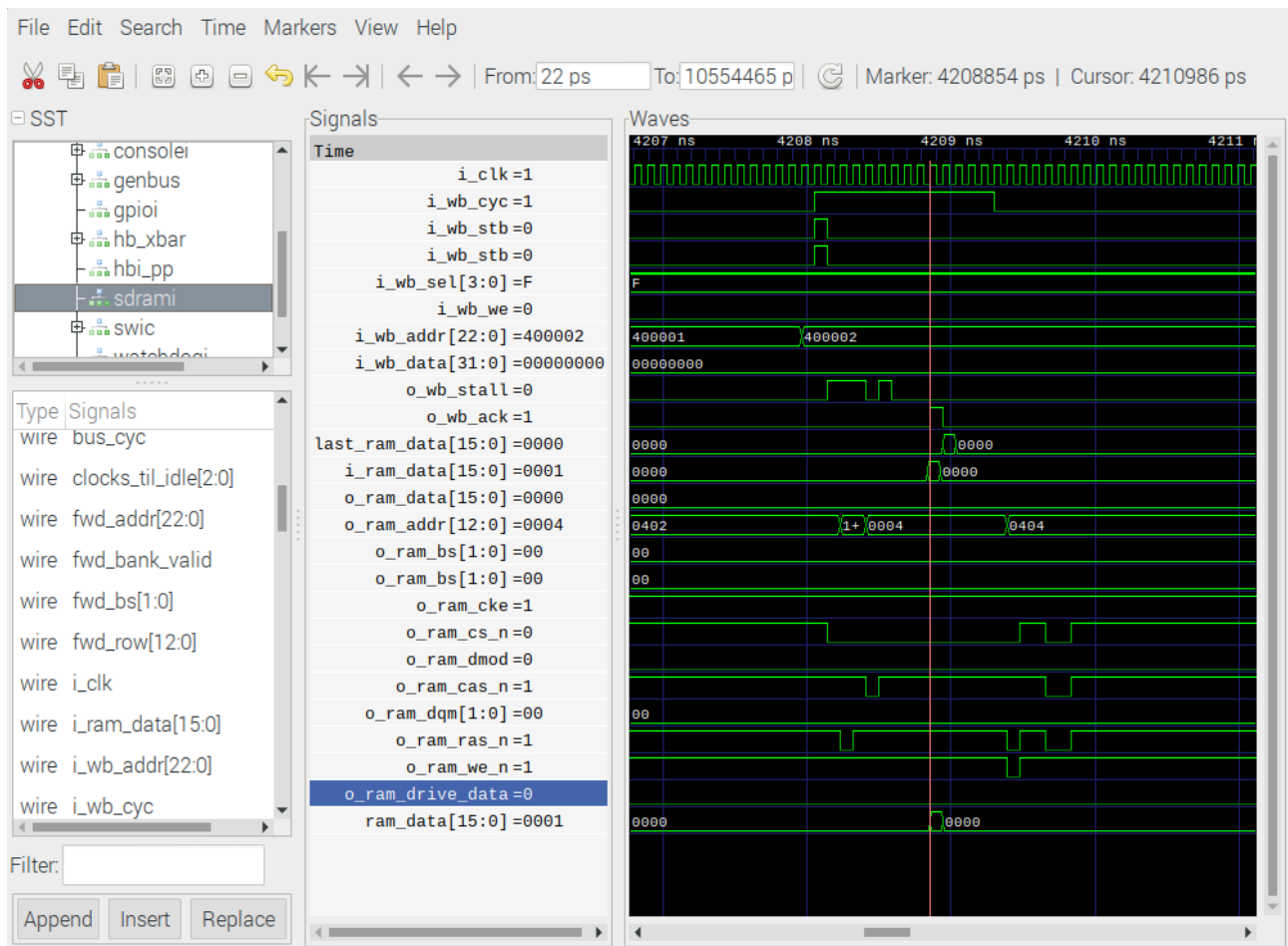


image 10

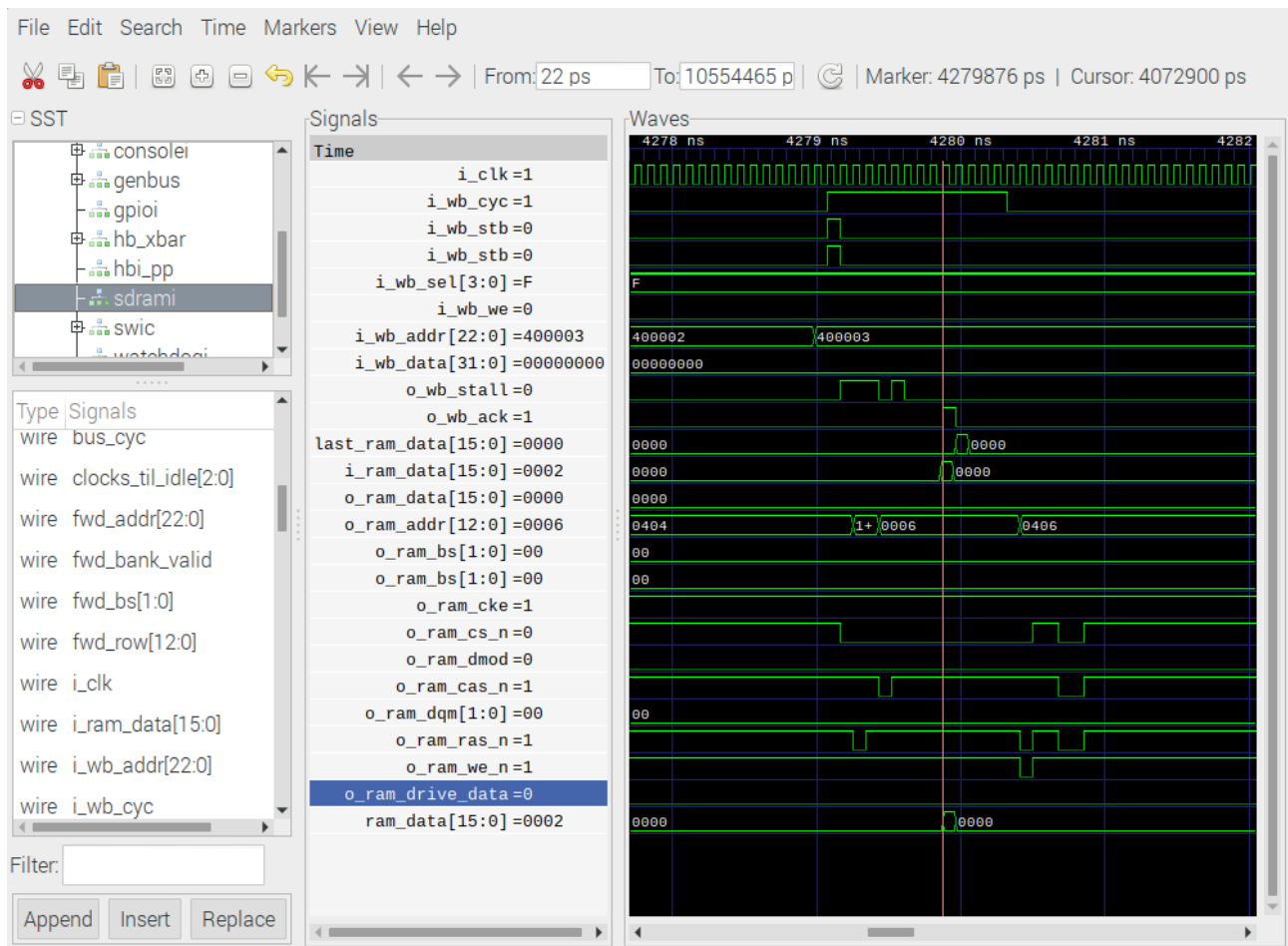


image 11

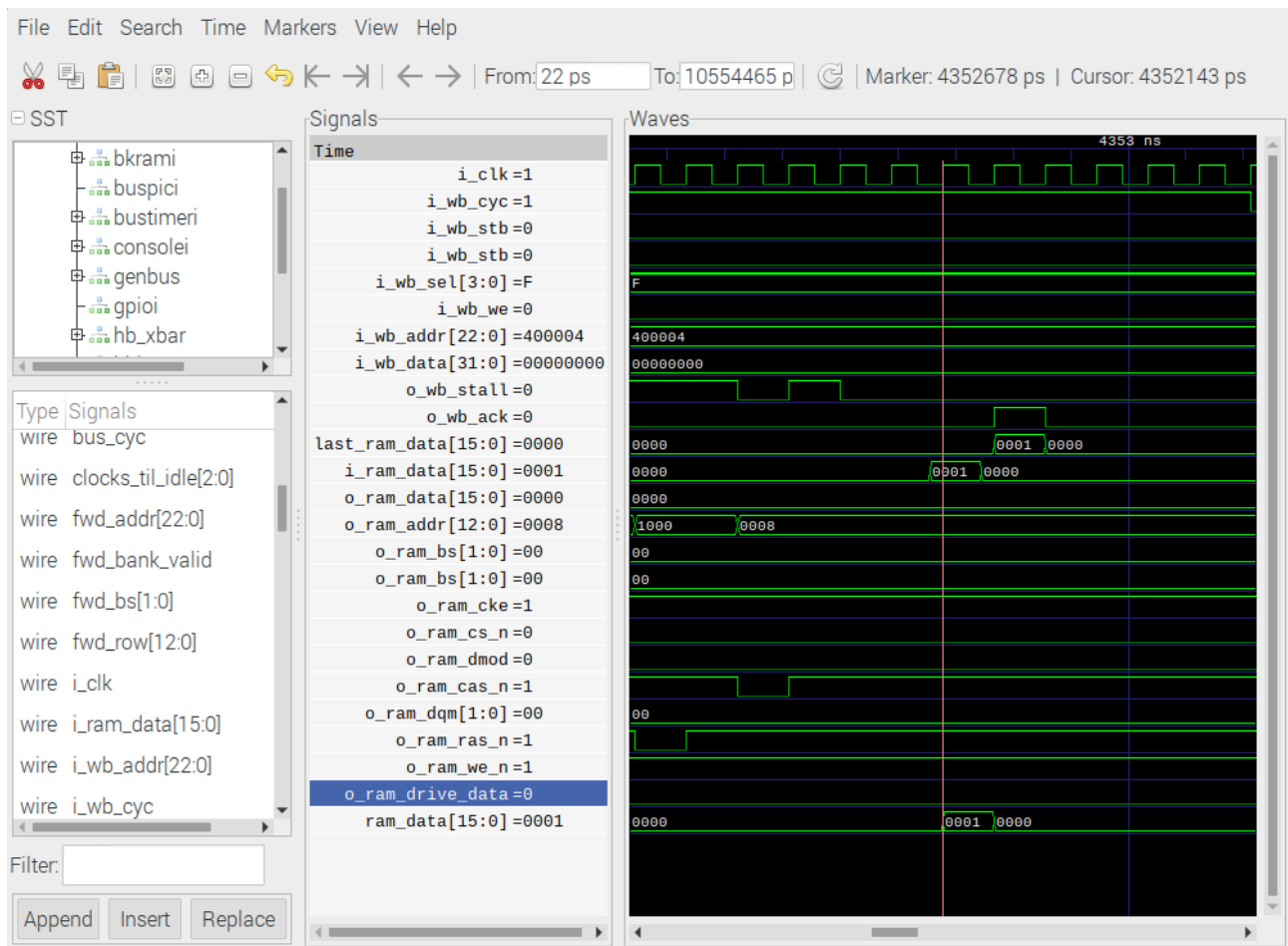
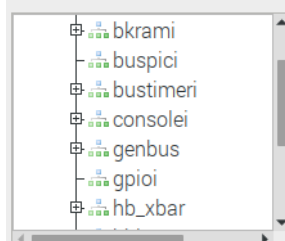


image 12

File Edit Search Time Markers View Help

From: 22 ps To: 10554465 p | Marker: 4421831 ps | Cursor: 4421608 ps

SST



Type	Signals
wire	bus_cyc
wire	clocks_til_idle[2:0]
wire	fwd_addr[22:0]
wire	fwd_bank_valid
wire	fwd_bs[1:0]
wire	fwd_row[12:0]
wire	i_clk
wire	i_ram_data[15:0]
wire	i_wb_addr[22:0]
wire	i_wb_cyc

Filter:

Append Insert Replace

Signals

```
Time
i_clk=1
i_wb_cyc=1
i_wb_stb=0
i_wb_stb=0
i_wb_sel[3:0]=F
i_wb_we=0
i_wb_addr[22:0]=400005
i_wb_data[31:0]=00000000
o_wb_stall=0
o_wb_ack=0
last_ram_data[15:0]=0000
i_ram_data[15:0]=0002
o_ram_data[15:0]=0000
o_ram_addr[12:0]=000A
o_ram_bs[1:0]=00
o_ram_bs[1:0]=00
o_ram_cke=1
o_ram_cs_n=0
o_ram_dmod=0
o_ram_cas_n=1
o_ram_dqm[1:0]=00
o_ram_ras_n=1
o_ram_we_n=1
o_ram_drive_data=0
ram_data[15:0]=0002
```

Waves

