

\*\*\*\*\***DRAFT**\*\*\*\*\*

**Adapting the ICOBOARD icozip  
to the CATBOARD catzip**

**11/27/18**

\*\*\*\*\***DRAFT**\*\*\*\*\*

*Catboard & Icoboard*

## ICOBOARD vs CATBOARD

- |   |   |
|---|---|
| <ul style="list-style-type: none"><li>• Modified Wishbone</li><li>• Autofpga project provides<ul style="list-style-type: none"><li>- toplevel.v &amp; main.v</li><li>- cpudef.h &amp; design.h</li><li>- board.ld</li></ul></li><li>• ZipCPU ab82a88 04/20/18</li><li>• 128K SRAM</li><li>• SB_IO toplevel interface to SRAM</li><li>• 4 PMOD connector, flat ribbon connectors, leds</li><li>• 50 Mhz no PLL</li><li>• SPIEXPRESS flash</li><li>• HX8K FPGA</li><li>• Interface to RPI 8 bit parallel</li><li>• Yosys Tool Chain</li></ul> | <ul style="list-style-type: none"><li>• Modified Wishbone</li><li>• Autofpga project provides<ul style="list-style-type: none"><li>- toplevel.v &amp; main.v</li><li>- cpudef.h &amp; design.h</li><li>- board.ld</li></ul></li><li>• ZipCPU ab82a88 04/20/18</li><li>• 32M SDRAM</li><li>• Tristate toplevel interface to SDRAM</li><li>• 2 PMOD, 4 LEDs, 4 dip switch 2 push button switches, 20 pin header</li><li>• 40 MHz using PLL</li><li>• Ver 0.1 has issues with SPI</li><li>• HX8K FPGA</li><li>• Interface to RPI 8 bit parallel</li><li>• Yosys Tool Chain</li></ul> |
|---|---|

*In shell Used to communicate with FPGA and Rpi3 C programs*

*pi@mypi3-1:~/testbuilds/catzip/sw/host \$ ./arm-netpport*  
*Listening on port 8363*  
*Listening on port 8364*

*In shell arm- commands are executed.*

*arm-wbregs Peek & Poke into FPGA*

*Displays the date the bin file created*

*./arm-wbregs version*

*01000010 ( VERSION) : [...] 20181122*

*Reads Sdram data at address 0x20091e8*

*./arm-wbregs 0x20091e8*

```

020091e8 (    ) : [."$] 0e22247c
arm-zipload
./arm-zipload -v ../board/jpeg
./arm-wbregs cpu 0x0f
Reads data from Sdram writing to a file
arm-rdsdram sdram..
Writes data from a file to Sdram
arm-wrsdram rgb_pack.bin

```

rgb.bin was used to create rgb\_pack.bin  
 const int bb = 0x1ff; lsb 9 bits of 32 bit word  
 const int gg = 0x7fc00; bits 10-19 of 32 bit word  
 const int rr = 0x1ff00000; msb 9 bits 32 bit word

```

r g b
0 e2 89 7c e22247c
1 de 88 83 de22083
2 e2 85 75 e221475
3 e3 88 7b e32207b
4 e1 8a 7a e12287a
5 e2 86 7c e22187c
6 e0 86 70 e021870
7 dd 83 75 dd20c75
8 dc 84 6d dc2106d
9 de 8b 76 de22c76
10 df 80 6a df2006a
11 de 83 69 de20c69
12 db 84 6f db2106f
13 e0 7f 65 e01fc65
14 dc 81 74 dc20474
15 dd 81 74 dd20474
16 df 82 69 df20869
17 e0 83 72 e020c72
18 e2 8a 76 e222876
19 e6 89 70 e622470
.
.
.
48003 d9 66 6a d91986a
48004 db 65 6a db1946a
48005 da 69 6e da1a46e
48006 dc 6f 72 dc1bc72
48007 d8 6c 75 d81b075
48008 dc 6d 6e dc1b46e
48009 de 73 78 de1cc78
48010 e0 77 78 e01dc78
48011 e3 7e 7e e31f87e
48012 e3 85 84 e321484
48013 e0 80 82 e020082
48014 e2 7f 83 e21fc83
48015 e6 82 84 e620884
48016 e4 8f 89 e423c89
48017 e7 95 8c e72548c

```

48018 e8 91 89 e824489  
48019 e6 8d 84 e623484  
48020 e7 90 8d e72408d  
48021 e5 85 84 e521484  
48022 e3 8b 88 e322c88  
48023 de 88 86 de22086  
48024 de 7d 7d de1f47d  
48025 dc 75 7d dc1d47d  
48026 da 7c 7d da1f07d

.  
.  
.

65514 a5 50 5f a51405f  
65515 ac 63 6e ac18c6e  
65516 b2 64 6f b21906f  
65517 ae 6d 75 ae1b475  
65518 a9 69 78 a91a478  
65519 a5 64 71 a519071  
65520 96 55 66 9615466  
65521 85 43 5b 8510c5b  
65522 75 29 44 750a444  
65523 67 22 3f 670883f  
65524 66 21 45 6608445  
65525 5e 1a 3c 5e0683c  
65526 5a f 30 5a03c30  
65527 5f 13 37 5f04c37  
65528 5e 16 39 5e05839  
65529 6b 1d 3d 6b0743d  
65530 77 2d 50 770b450  
65531 7d 37 50 7d0dc50  
65532 96 42 57 9610857  
65533 a8 48 55 a812055  
65534 b2 43 4c b210c4c  
65535 b7 49 51 b712451

00000000 7C 24 22 0E 83 20 E2 0D 75 14 22 0E 7B 20 32 0E |\$".. ..u.".{ 2.  
00000010 7A 28 12 0E 7C 18 22 0E 70 18 02 0E 75 0C D2 0D z(..|. ".p...u...  
00000020 6D 10 C2 0D 76 2C E2 0D 6A 00 F2 0D 69 0C E2 0D m...v,..j...i...  
00000030 6F 10 B2 0D 65 FC 01 0E 74 04 C2 0D 74 04 D2 0D o...e...t...t...  
00000040 69 08 F2 0D 72 0C 02 0E 76 28 22 0E 70 24 62 0E i...r...v(" .p\$b.  
Below is output of the jpeg.c compiled for zipcpu

. img\_ptr = 0x20091e8  
. Start of JPEG DWT!  
. free img\_ptr !  
. img\_ptr = 0x20091e8 \*img\_ptr = 0xe22247c  
. img\_ptr = 0x20091ec \*img\_ptr = 0xde22083  
. img\_ptr = 0x20091f0 \*img\_ptr = 0xe221475  
. img\_ptr = 0x20091f4 \*img\_ptr = 0xe32207b  
. img\_ptr = 0x20091f8 \*img\_ptr = 0xe12287a  
. img\_ptr = 0x20091fc \*img\_ptr = 0xe22187c  
. img\_ptr = 0x2009200 \*img\_ptr = 0xe021870  
. img\_ptr = 0x2009204 \*img\_ptr = 0xdd20c75

```

. img_ptr = 0x2009208 *img_ptr = 0xdc2106d
. img_ptr = 0x200920c *img_ptr = 0xde22c76
. img_ptr = 0x2009210 *img_ptr = 0xdf2006a
. img_ptr = 0x2009214 *img_ptr = 0xde20c69
. img_ptr = 0x2009218 *img_ptr = 0xdb2106f
. img_ptr = 0x200921c *img_ptr = 0xe01fc65
. img_ptr = 0x2009220 *img_ptr = 0xdc20474
. img_ptr = 0x2009224 *img_ptr = 0xdd20474
. img_ptr = 0x2009228 *img_ptr = 0xdf20869
. img_ptr = 0x200922c *img_ptr = 0xe020c72
. img_ptr = 0x2009230 *img_ptr = 0xe222876
. img_ptr = 0x2009234 *img_ptr = 0xe622470

```

## **jpeg.c**

```

#include <stdio.h>
#include <stdlib.h>
#include "board.h"
#include "lifting.h"
#define SDRAM 0x2000000
#define imgsize 256

void zip_clear_sdram(int *imbuf) {
    int val,i;

    val = 0;

    for(i=0; i<256*256*12; i++) {
        *imbuf++ = val;
    }
}

int main(int argc, char **argv) {

    int *m_ptr,*img_ptr;

    img_ptr = (int *)malloc(196608);
    int val,i;
    /*_gpio = GPIO_LEDR_SET;
    printf("gpio 0x%x\n",_gpio);

```

```
printf("img_ptr = 0x%x\n",img_ptr);
```

```
printf("Start of JPEG DWT!\n");
```

```
//this was done by clr_sdram
```

```
//printf("clearing buf_ptr + 786432 buf_ptr = 0x%x\n",img_ptr);
```

```
//zip_clear_sdram(img_ptr);
```

```
//printf("done clearing buf_ptr + 786432 \n");
```

```
printf("free img_ptr !\n");
```

```
for(i=0;i<100;i++) {
```

```
    printf("img_ptr = 0x%x *img_ptr = 0x  
%x\n",img_ptr,*img_ptr);
```

```
    img_ptr ++;
```

```
}
```

```
free(img_ptr);
```

```
/*_gpio = 0x010000;
```

```
}
```

**This is an example of loading the jpeg program into to FPGA**

**pi@mypi3-1:~/testbuilds/catzip/sw/host \$ ./arm-zipload -v ../board/jpeg**

**Halting the CPU**

**Memory regions:**

**Block RAM: 01400000 - 01402000**

**SDRAM : 02000000 - 04000000**

**Loading: ../board/jpeg**

**Section 0: 02000000 - 020091dc**

**Writing to MEM: 02000000-020091dc**

**Clearing the CPUs registers**

**Setting PC to 02000000**

**The CPU should be fully loaded, you may now**

**start it (from reset/reboot) with:**

**> wbreps cpu 0x0f**

**CPU Status is: 0000060f**

**Testing Remote Access & building on Ubuntu 16.04**

**modified the script to perform remote control access of the FPGA interfaced to the RPi3B+**

**testing build on ubuntu 16.04**

Linux ws010 4.4.0-137-generic #163-Ubuntu SMP Mon Sep 24 13:14:43 UTC 2018 x86\_64  
x86\_64 x86\_64 GNU/Linux  
cd testbuilds/

git clone https://github.com/develone/catzip.git

The build proces on Ubuntu take a relative short time.

-rw-rw-r-- 1 Vidal Vidal 6373 Oct 30 10:55 Makefile

-rw-rw-r-- 1 Vidal Vidal 135100 Oct 30 11:03 rtl/catzip/catzip.bin

./rtl/ppptest/linepp.bin

./rtl/ppptest/hellopp.bin

./rtl/ppptest/speechpp.bin

./rtl/switch\_leds/switch\_leds.bin

./rtl/uart/speechfifo.bin

./rtl/uart/helloworld.bin

./rtl/catzip/catzip.bin

./rtl/leddigits/leddigits.bin

./rtl/basic/pmodtest.bin

./rtl/basic/dimmer.bin

./rtl/basic/blinky.bin

./rtl/basic/clktest.bin

pi@mypi3-1:~/testbuilds/ws010/catzip/sw/host \$ diff rem\_test\_sim102218.sh test\_sim102218.sh  
2,18c2,18

< ./pc-wbregs -n mypi3-1 version

< ./pc-wbregs -n mypi3-1 0x2000004 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x2000004

< ./pc-wbregs -n mypi3-1 0x20ffff8 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x20ffff8

< ./pc-wbregs -n mypi3-1 0x2800004 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x2800004

< ./pc-wbregs -n mypi3-1 0x28ffff8 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x28ffff8

< ./pc-wbregs -n mypi3-1 0x2c00004 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x2c00004

< ./pc-wbregs -n mypi3-1 0x2cffff8 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x2cffff8

< ./pc-wbregs -n mypi3-1 0x2f00004 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x2f00004

< ./pc-wbregs -n mypi3-1 0x2fffff8 0x55aaaa55

< ./pc-wbregs -n mypi3-1 0x2fffff8

---

> ./arm-wbregs version

> ./arm-wbregs 0x2000004 0x55aaaa55

> ./arm-wbregs 0x2000004

> ./arm-wbregs 0x20ffff8 0x55aaaa55

> ./arm-wbregs 0x20ffff8

> ./arm-wbregs 0x2800004 0x55aaaa55

> ./arm-wbregs 0x2800004

> ./arm-wbregs 0x28ffff8 0x55aaaa55

> ./arm-wbregs 0x28ffff8

> ./arm-wbregs 0x2c00004 0x55aaaa55

> ./arm-wbregs 0x2c00004

```

> ./arm-wbregs 0x2cffff8 0x55aaaa55
> ./arm-wbregs 0x2cffff8
> ./arm-wbregs 0x2f00004 0x55aaaa55
> ./arm-wbregs 0x2f00004
> ./arm-wbregs 0x2ffffff8 0x55aaaa55
> ./arm-wbregs 0x2ffffff8
pi@mypi3-1:~/testbuilds/ws010/catzip/sw/host $ diff sim_hw_test.sh rem_sim_hw_test.sh
5c5
< ./arm-wbregs version
---
> ./pc-wbregs -n mypi3-1 version
7c7
< ./arm-wbregs 0x1000000 0x10000001
---
> ./pc-wbregs -n mypi3-1 0x1000000 0x10000001
9c9
< ./arm-wbregs 0x1000004 0x10000002
---
> ./pc-wbregs -n mypi3-1 0x1000004 0x10000002
11c11
< ./arm-wbregs 0x1000008 0x10000003
---
> ./pc-wbregs -n mypi3-1 0x1000008 0x10000003
13c13
< ./arm-wbregs 0x100000c 0x10000004
---
> ./pc-wbregs -n mypi3-1 0x100000c 0x10000004
15c15
< ./arm-wbregs 0x1000000 0x10000001
---
> ./pc-wbregs -n mypi3-1 0x1000000 0x10000001
17c17
< ./arm-wbregs 0x1000004 0x10000002
---
> ./pc-wbregs -n mypi3-1 0x1000004 0x10000002
19c19
< ./arm-wbregs 0x1000008 0x10000003
---
> ./pc-wbregs -n mypi3-1 0x1000008 0x10000003
21c21
< ./arm-wbregs 0x100000c 0x10000004
---
> ./pc-wbregs -n mypi3-1 0x100000c 0x10000004
23c23
< ./arm-wbregs 0x1000000
---
> ./pc-wbregs -n mypi3-1 0x1000000
25c25
< ./arm-wbregs 0x1000004
---
> ./pc-wbregs -n mypi3-1 0x1000004
27c27

```

```

< ./arm-wbregs 0x1000008
---
> ./pc-wbregs -n mypi3-1 0x1000008
29c29
< ./arm-wbregs 0x100000c
---
> ./pc-wbregs -n mypi3-1 0x100000c
31c31
< ./arm-wbregs 0x1000000
---
> ./pc-wbregs -n mypi3-1 0x1000000
33c33
< ./arm-wbregs 0x1000004
---
> ./pc-wbregs -n mypi3-1 0x1000004
35c35
< ./arm-wbregs 0x1000008
---
> ./pc-wbregs -n mypi3-1 0x1000008
37c37
< ./arm-wbregs 0x100000c
---
> ./pc-wbregs -n mypi3-1 0x100000c
40c40
< ./arm-wbregs gpio 0x00010001
---
> ./pc-wbregs -n mypi3-1 gpio 0x00010001
43c43
< ./arm-wbregs gpio 0x00020002
---
> ./pc-wbregs -n mypi3-1 gpio 0x00020002
46c46
< ./arm-wbregs gpio 0x00040004
---
> ./pc-wbregs -n mypi3-1 gpio 0x00040004
49c49
< ./arm-wbregs gpio 0x00070000
---
> ./pc-wbregs -n mypi3-1 gpio 0x00070000
Adding SDRAM to catzip
Starting with this version of catzip
catzip
commit 1e0dd38e890187ae3d6629fd35ddeead39a6701
Author: Edward Vidal Jr <develone@sbcglobal.net>
Date: Mon Aug 13 02:04:34 2018 +0000

```

*speechfifo not working*  
*Using this version of learning\_hdl to copy the files to add*  
*the sdram support to catzip*

```

commit 59da9a3ae53a03c20d516ee4c75da5597e448205
Author: Edward Vidal Jr <develone@sbcglobal.net>

```



Date: Wed Oct 24 16:51:00 2018 -0600

using hardware

./config\_catzip\_simulation.sh

~/testbuilds/catzip\_simulation/catzip

. myenv.sh

make datestamp

make autodata

~/testbuilds/catzip\_simulation/catzip/rtl/catzip

. ../myenv.sh

make clean

make cpudefs.h

make design.h

make verilated

make bin

sudo config\_cat catzip.bin

~/testbuilds/catzip\_simulation/catzip/sim/verilated

. ../myenv.sh

make clean

make

~/testbuilds/catzip\_simulation/catzip/sw/host

. ../myenv.sh

make clean

make

~/testbuilds/catzip\_simulation/catzip/sw/host \$ ./arm-netpport

pi@mypi3-1:~/testbuilds/catzip\_simulation/catzip/sw/host \$ ./test\_sim102218.sh

00c00010 ( VERSION ) : [...] 20181029

02000004 ( )-> 55aaaa55

02000004 ( ) : [.U.U] aa55aa55

020ffff8 ( )-> 55aaaa55

020ffff8 ( ) : [.U.U] aa55aa55

02800004 ( )-> 55aaaa55

02800004 ( ) : [.U.U] aa55aa55

028ffff8 ( )-> 55aaaa55

028ffff8 ( ) : [.U.U] aa55aa55

02c00004 ( )-> 55aaaa55

02c00004 ( ) : [.U.U] aa55aa55

02cffff8 ( )-> 55aaaa55

02cffff8 ( ) : [.U.U] aa55aa55

02f00004 ( )-> 55aaaa55

02f00004 ( ) : [.U.U] aa55aa55

02fffff8 ( )-> 55aaaa55

02fffff8 ( ) : [.U.U] aa55aa55

pi@mypi3-1:~/testbuilds/catzip\_simulation/catzip/rtl/catzip \$ diff wbsdram.v

~/testbuilds/xulalx25soc/rtl/wbsdram.v

66c66

```

<      parameter [0:0]      F_OPT_CLK2FFLOGIC = 1'b1;
---
>      parameter [0:0]      F_OPT_CLK2FFLOGIC = 1'b0;
122,123c122
<          refresh_clk <= 10'd391; // Make suitable for 50 MHz clk
<          //refresh_clk <= 10'd625; // Make suitable for 80 MHz clk
---
>          refresh_clk <= 10'd625; // Make suitable for 80 MHz clk
183c182
<      //initial      fwd_addr = 1;
---
>      initial fwd_addr = 1;
cd ../basic
~/testbuilds/catzip_simulation/catzip/rtl/basic
make clean
make
sudo config_cat blinky.bin
sudo config_cat dimmer.bin
sudo config_cat clktest.bin
pmodtest.bin not testing.
cd ../leddigits/
~/testbuilds/catzip_simulation/catzip/rtl/leddigits
make clean
make
sudo config_cat leddigits.bin
cd ../switch_leds/
~/testbuilds/catzip_simulation/catzip/rtl/switch_leds
make clean
make
sudo config_cat switch_leds.bin
cd ../pptest/
~/testbuilds/catzip_simulation/catzip/rtl/pptest
make clean
make
sudo config_cat hellopp.bin
. Hello, World!
sudo config_cat speechpp.bin
. |=====|
. |
. |
. | Four score and seven years ago our fathers brought forth on this |
. | continent, a new nation, conceived in Liberty, and dedicated to |
. | the proposition that all men are created equal. |
. |
. |
. | Now we are engaged in a great civil war, testing whether that |
. | nation, or any nation so conceived and so dedicated, can long |
. | endure. We are met on a great battle-field of that war. We have |
. | come to dedicate a portion of that field, as a final resting |
. | place for those who here gave their lives that that nation might |
. | live. It is altogether fitting and proper that we should do this. |
. |
. | But, in a larger sense, we can not dedicate-we can not consecrate-
. | we can not hallow-this ground. The brave men, living and dead, |

```

. | who struggled here, have consecrated it, far above our poor power |  
. | to add or detract. The world will little note, nor long remember |  
. | what we say here, but it can never forget what they did here. It |  
. | is for us the living, rather, to be dedicated here to the |  
. | unfinished work which they who fought here have thus far so nobly |  
. | advanced. It is rather for us to be here dedicated to the great |  
. | task remaining before us-that from these honored dead we take |  
. | increased devotion to that cause for which they gave the last |  
. | full measure of devotion-that we here highly resolve that these |  
. | dead shall not have died in vain-that this nation, under God, |  
. | shall have a new birth of freedom-and that government of the |  
. | people, by the people, for the people, shall not perish from the |  
. | earth. |

. |  
. |  
. |=====|

cd ../uart/

~/testbuilds/catzip\_simulation/catzip/rtl/uart

make clean

make

sudo config\_cat helloworld.bin

pi@mypi3-1:~/testbuilds/catzip\_simulation/catzip/sw/host \$ ./sim\_hw\_test.sh

he date built

00c00010 ( VERSION) : [...] 20181029

01000000 ( RAM)-> 10000001

01000004 ( )-> 10000002

01000008 ( )-> 10000003

0100000c ( )-> 10000004

01000000 ( RAM)-> 10000001

01000004 ( )-> 10000002

01000008 ( )-> 10000003

0100000c ( )-> 10000004

01000000 ( RAM) : [...] 10000001

01000004 ( ) : [...] 10000002

01000008 ( ) : [...] 10000003

0100000c ( ) : [...] 10000004

01000000 ( RAM) : [...] 10000001

01000004 ( ) : [...] 10000002

01000008 ( ) : [...] 10000003

0100000c ( ) : [...] 10000004

Turning on the 4th led

00c00008 ( GPIO)-> 00010001

Turning on the 1st led

00c00008 ( GPIO)-> 00020002

Turning on the 2nd led

00c00008 ( GPIO)-> 00040004

Turning off the leds

00c00008 ( GPIO)-> 00070000

Versions of support support software to

\*\*\*\*\*

autofpga

**commit 2f443503d1edc1a401d30207790906cb01df32**  
**Author: ZipCPU <dgisselq@ieee.org>**  
**Date: Sun Aug 5 20:55:25 2018 -0400**

**Fixed an uninitialized error in the subdirectory string**  
**icestorm**

**commit 8cac6c584044034210fe0ba1e6b930ff1cc59465**  
**Author: Clifford Wolf <clifford@clifford.at>**  
**Date: Mon Jul 30 16:04:04 2018 +0200**

**Also install text timing databases**

**Signed-off-by: Clifford Wolf <clifford@clifford.at>**  
**arachne-pnr**  
**commit 5d830dd94ad956d17d77168fe7718f22f8b55b33**  
**Merge: 3a40328 9763e6e**  
**Author: Clifford Wolf <clifford@clifford.at>**  
**Date: Sun May 13 20:58:41 2018 +0200**

**Merge pull request #115 from awygle/lm**

**Add basic lm4k support (no hard IP)**  
**yosys**  
**commit e275692e84c935d0cdf42c2a4adf7ac949a88132**  
**Author: Clifford Wolf <clifford@clifford.at>**  
**Date: Sun Jul 22 18:44:05 2018 +0200**

**Verific: Produce errors for instantiating unknown module**

**Because if the unknown module is connected to any constants, Verific will actually break all constants in the same module, even if they have nothing to do structurally with that instance of an unknown module.**

**Signed-off-by: Clifford Wolf <clifford@clifford.at>**  
**commit ab82a886305ceec79b5516d7fc356f95a762c9fd**  
**Author: ZipCPU <dgisselq@ieee.org>**  
**Date: Fri Apr 20 12:49:05 2018 -0400**

**Renamed the autoreload value of the ziptimer to be the interval count**  
**verilator v3.926**  
**commit c8e437c45cf0a9849e0a0465ecca882dbb66933a**  
**Author: Wilson Snyder <wsnyder@wsnyder.org>**  
**Date: Wed Aug 22 18:09:06 2018 -0400**

**Version bump**

**The following information is from <https://github.com/ZipCPU/zipcpu/blob/master/doc/spec.pdf>**

## **Introduction**

**The goal of the ZipCPU was to be a very simple CPU. You might think of it as a poor man's alternative to the OpenRISC architecture. You might also think of it as an Open Source microcontroller. For this reason, all instructions have been designed to be as simple as possible, and the base instructions are all designed to be executed in one instruction cycle per instruction,**

**barring pipeline stalls.**<sup>1</sup> Indeed, even the bus has been simplified to a constant 32-bit width, with no option for more or less. This has resulted in the choice to drop push and pop instructions, pre-increment and post-decrement addressing modes, the integrated memory management unit (MMU), and more

*For those who like buzz words, the ZipCPU is:*

**A 32-bit CPU:** All registers are 32-bits, addresses are 32-bits, instructions are 32-bits wide, etc.

**A RISC CPU.** There is no microcode for executing instructions. All instructions are designed to be completed in one clock cycle.

**A Load/Store architecture.** (Only load and store instructions can access memory.)

**Wishbone compliant.** All peripherals are accessed just like memory across this bus.

**A Von-Neumann architecture.** The instructions and data share a common bus.

**A pipelined architecture,** having stages for Prefetch, Decode, Read-Operand, a combined stage containing the ALU, Memory, Divide, and Floating Point units, and then the final Write-back stage. See Fig. 1.1 for a diagram of this structure.

**Completely open source,** licensed under the GPL.<sup>3</sup>

OpCode	A-Reg	Instruction	Sets CC
5'h00	SUB	Subtract	Y
5'h01	AND	Bitwise And	
5'h02	ADD	Add two numbers	
5'h03	OR	Bitwise Or	
5'h04	XOR	Bitwise Exclusive Or	
5'h05	LSR	Logical Shift Right	
5'h06	LSL	Logical Shift Left	
5'h07	ASR	Arithmetic Shift Right	
5'h08	BREV	Bit Reverse B operand into result	N
5'h09	LDILO	Load Immediate Low	
5'h0a	MPYUHI	Upper 32 of 64 bits from an unsigned 32x32 multiply	Y
5'h0b	MPYSHI	Upper 32 of 64 bits from a signed 32x32 multiply	
5'h0c	MPY	32x32 bit multiply	N
5'h0d	MOV	Move OpB into Ra	
5'h0e	DIVU	R0-R13 Divide, unsigned	Y
5'h0f	DIVS	R0-R13 Divide, signed	
5'h10	CMP	Compare (Ra-OpB) to zero	Y
5'h11	TST	Test (AND w/o setting result)	
5'h12	LW	Load a 32-bit word from memory (OpB) into Ra	N
5'h13	SW	Store a 32-bit word from Ra into memory at (OpB)	
5'h14	LH	Load 16-bits from memory (OpB) into Ra, clear upper 16 bits	
5'h15	SH	Store the lower 16-bits of Ra into memory at (OpB)	
5'h16	LB	Load 8-bits from memory (OpB) into Ra, clear upper 24 bits	
5'h17	SB	Store the lower 8-bits of Ra into memory at (OpB)	
5'h18/9	LDI	Load 23-bit signed immediate	N
5'h1a	FPADD	R0-R13 Floating point add	Y
5'h1b	FPSUB	R0-R13 Floating point subtract	
5'h1c	FPMPY	R0-R13 Floating point multiply	
5'h1d	FPDIV	R0-R13 Floating point divide	
5'h1e	FPI2F	R0-R13 Convert integer to floating point	
5'h1f	FPF2I	R0-R13 Convert floating point to integer	
5'h1c	BREAK	None(15)	N
5'h1d	LOCK	None(15)	
5'h1e	SIM	None(15)	
5'h1f	NOOP	None(15)	

Table 2.2: ZipCPU OpCodes

***“export PATH=/home/pi/zipcpu/sw/install/cross-tools/bin:/home/pi/autofpga/sw:\$PATH”***

***“cd catzip”***

***“make clean”***

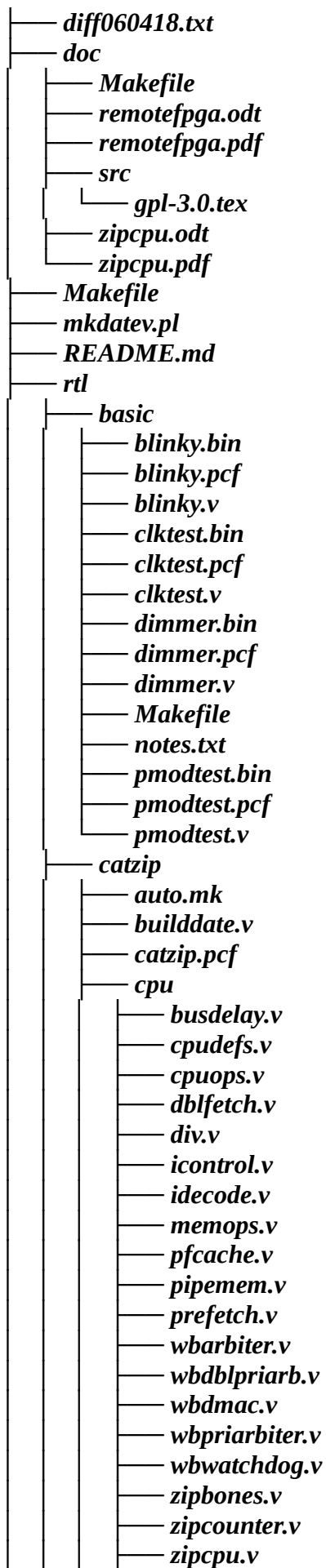
***“make” This creates the 2 executeables arm-netpport & arm-wbregs used to communicate with the FPGA.in files for download to FPGA***

***In additon compiles the***

***The rtl has several folders basic, uart,catzip, leddigits, pptest, switch\_leds, and sdram where \*.bin files are created.***

***The sw/host has 2 executeables arm-netpport & arm-wbregs used to communicate with the FPGA.***

- 20180605-build.v
- 20180605-cat.tjz
- auto-data
  - bkram.txt
  - board.h
  - board.ld
  - buserr.txt
  - clock.txt
  - dlyarbiter.txt
  - global.txt
  - gpio.txt
  - hbconsole.txt
  - legalgen.txt
  - main\_tb.cpp
  - main.v
  - Makefile
  - pic.txt
  - pwrcount.txt
  - regdefs.cpp
  - regdefs.h
  - rtl.make.inc
  - testb.h
  - toplevel.v
  - version.txt
  - wbuconsole.txt
  - zipbones.txt



- zipjiffies.v
- zipsystem.v
- ziptimer.v
- cpudefs.h
- dbg.png
- design.h
- flashconfig.v
- hdr.png
- icozip.pcf
- leds.png
- main.v
- Makefile
- memdev.v
- obj-arm
  - Vmain\_\_ALL.a
  - Vmain\_\_ALLcls.cpp
  - Vmain\_\_ALLcls.d
  - Vmain\_\_ALLcls.o
  - Vmain\_\_ALLsup.cpp
  - Vmain\_\_ALLsup.d
  - Vmain\_\_ALLsup.o
  - Vmain\_\_classes.mk
  - Vmain.cpp
  - Vmain\_\_Dpi.cpp
  - Vmain\_\_Dpi.h
  - Vmain.h
  - Vmain.mk
  - Vmain\_\_Syms.cpp
  - Vmain\_\_Syms.h
  - Vmain\_\_Trace.cpp
  - Vmain\_\_Trace\_\_Slow.cpp
  - Vmain\_\_ver.d
  - Vmain\_\_verFiles.dat
- pbsw.png
- rtcdate.v
- rxuartlite.v
- rxuart.v
- simple.log
- spio.v
- sw.png
- testmain.v
- toplevel.v
- txuartlite.v
- txuart.v
- ufifo.v
- wbgpio.v
- wbpwmaudio.v
- wbqspiflash.v
- wbscopc.v
- wbscope.v
- wbubus
- wbconsole.v



- **wbubus.v**
- **wbucompactlines.v**
- **wbucompress.v**
- **wbuconsole.v**
- **wbudecompress.v**
- **wbudeword.v**
- **wbuexec.v**
- **wbufifo.v**
- **wbuidleint.v**
- **wbuinput.v**
- **wbuoutput.v**
- **wbureadcw.v**
- **wbusixchar.v**
- **wbutohex.v**

- **clktest.asc**

- **hexbus**

- **console.v**
- **hbbus.v**
- **hbconsole.v**
- **hbdechex.v**
- **hbdeword.v**
- **hbexec.v**
- **hbgenhex.v**
- **hbidle.v**
- **hbints.v**
- **hbnewline.v**
- **hbpack.v**

- **leddigits**

- **leddigits.pcf**
- **leddigits.v**
- **Makefile**

- **Makefile**

- **pmodleds**

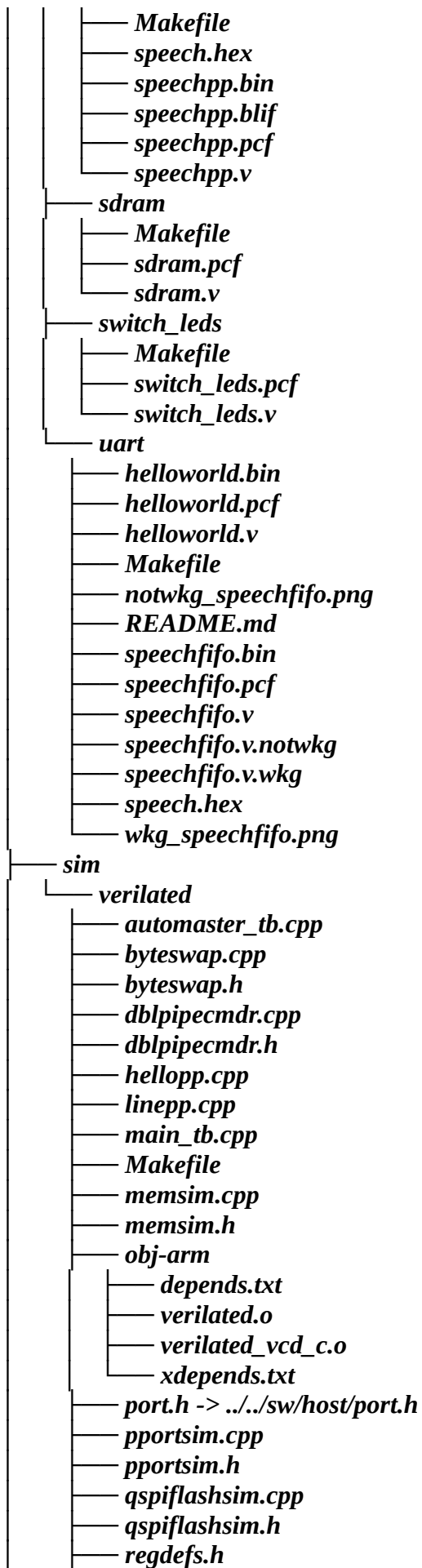
- **ledbouncer.pcf**
- **ledbouncer.v**
- **ledwalker.pcf**
- **ledwalker.v**
- **Makefile**

- **pport**

- **ppio.v**
- **pport.v**
- **ufifo.v**
- **wbppport.v**

- **pptest**

- **hellopp.bin**
- **hellopp.blif**
- **hellopp.pcf**
- **hellopp.v**
- **linepp.bin**
- **linepp.blif**
- **linepp.pcf**
- **linepp.v**



```

|
|—— speechpp.cpp
|—— tags
|—— tbclock.h
|—— testb.h
|—— twoc.cpp
|—— twoc.h
|—— uartsim.cpp
|—— uartsim.h
|—— zipelf.cpp
|—— zipelf.h
|—— sim-err.txt

```

Initial testing  
06/05/18

cd catzip/rtl/catzip

sudo config\_cat catzip.bin This programs the FPGA

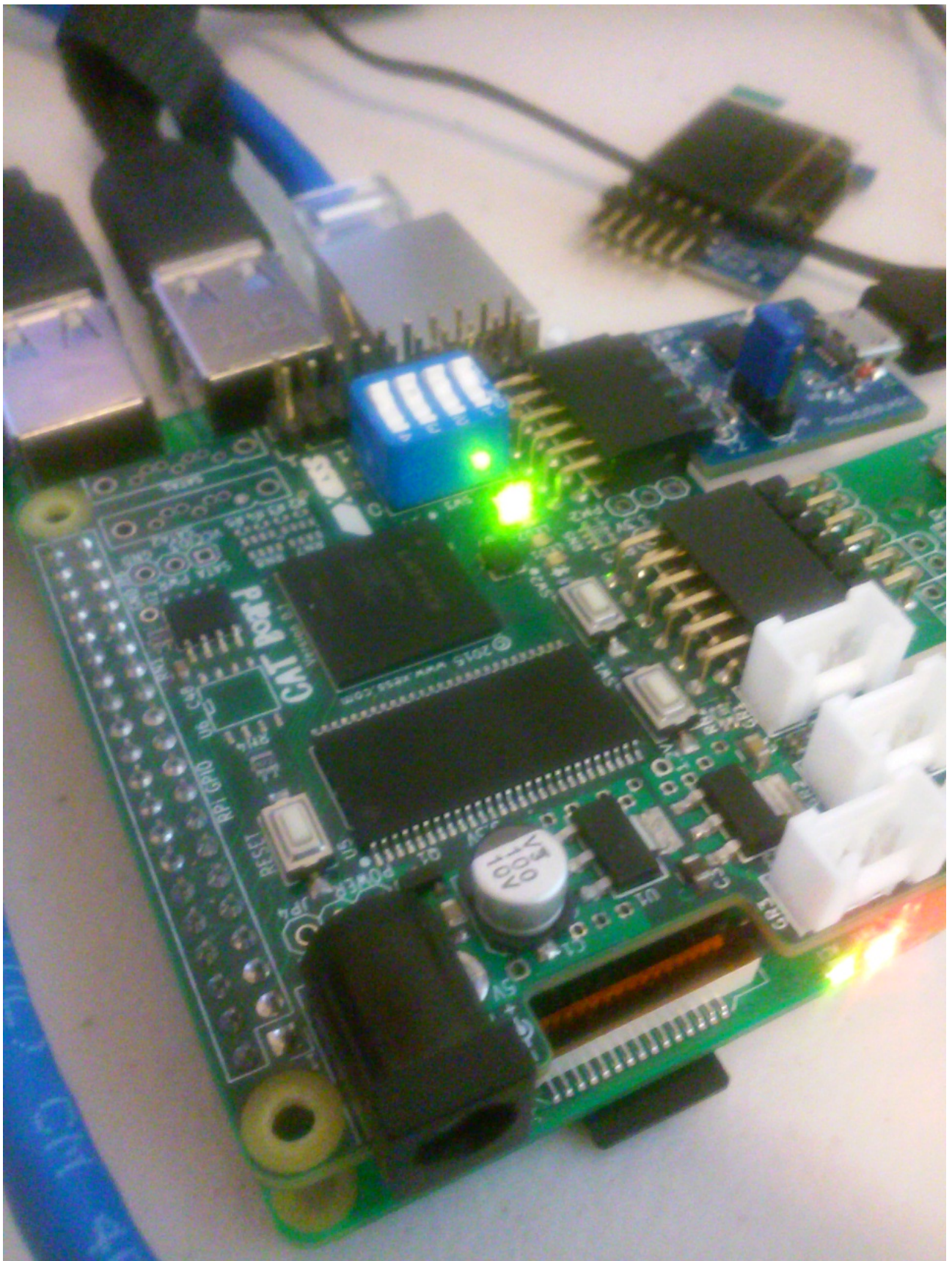
cd catzip/sw/host

./arm-netppport  
Listening on port 8363  
Listening on port 8364

cd catzip/sw/host

./arm-wbregs version  
00001010 ( VERSION) : [...] 20180605

1st Led on  
/arm-wbregs gpio 0x00010001  
00001008 ( GPIO)-> 00010001



1st Led off

```
./arm-wbregs gpio 0x00010000
```

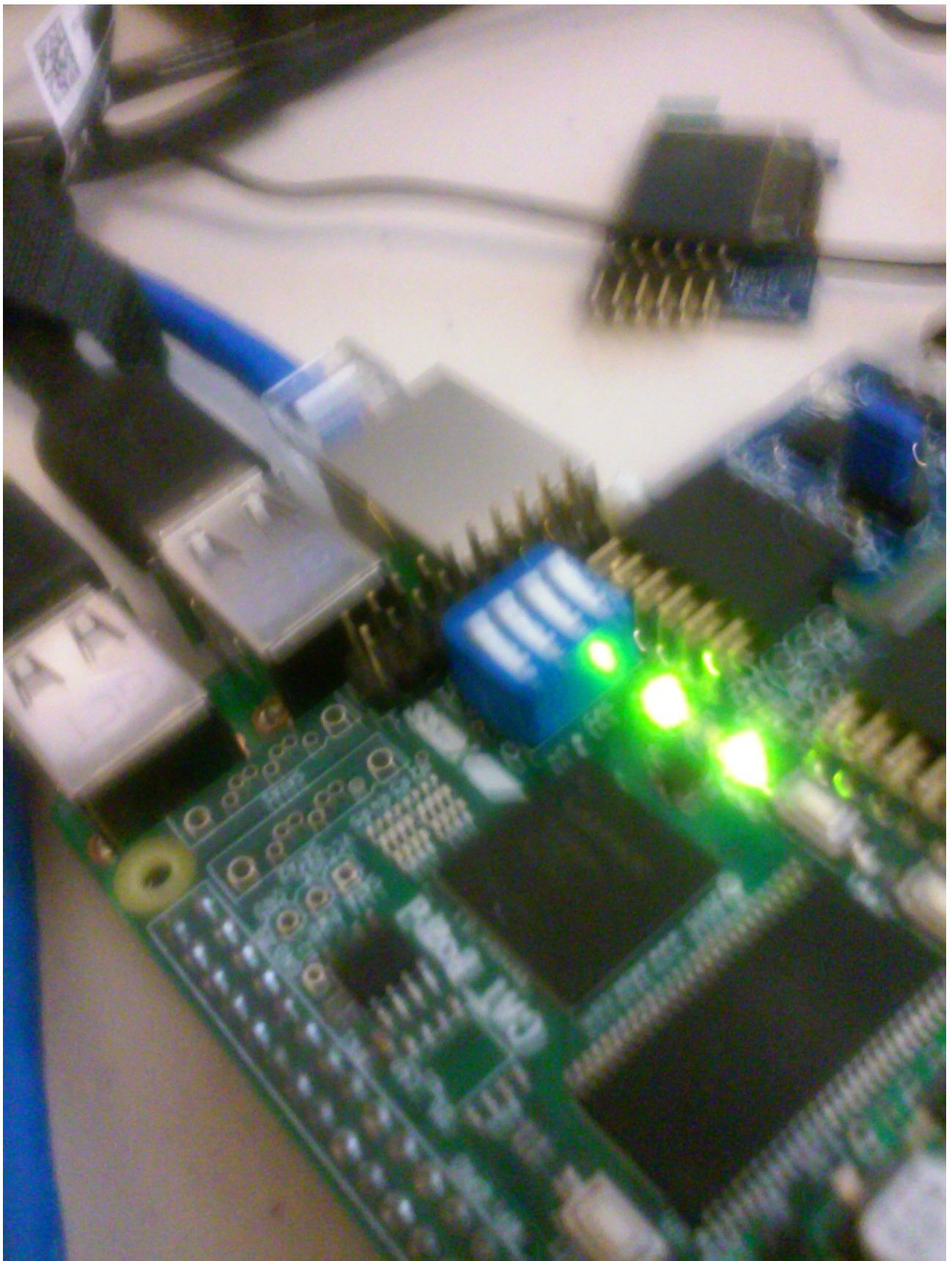
```
00001008 ( GPIO)-> 00010000
```

2n led on

```
./arm-wbregs gpio 0x00020002
```

```
00001008 ( GPIO)-> 00020002
```





2nd led off

```
./arm-wbregs gpio 0x00020000
```

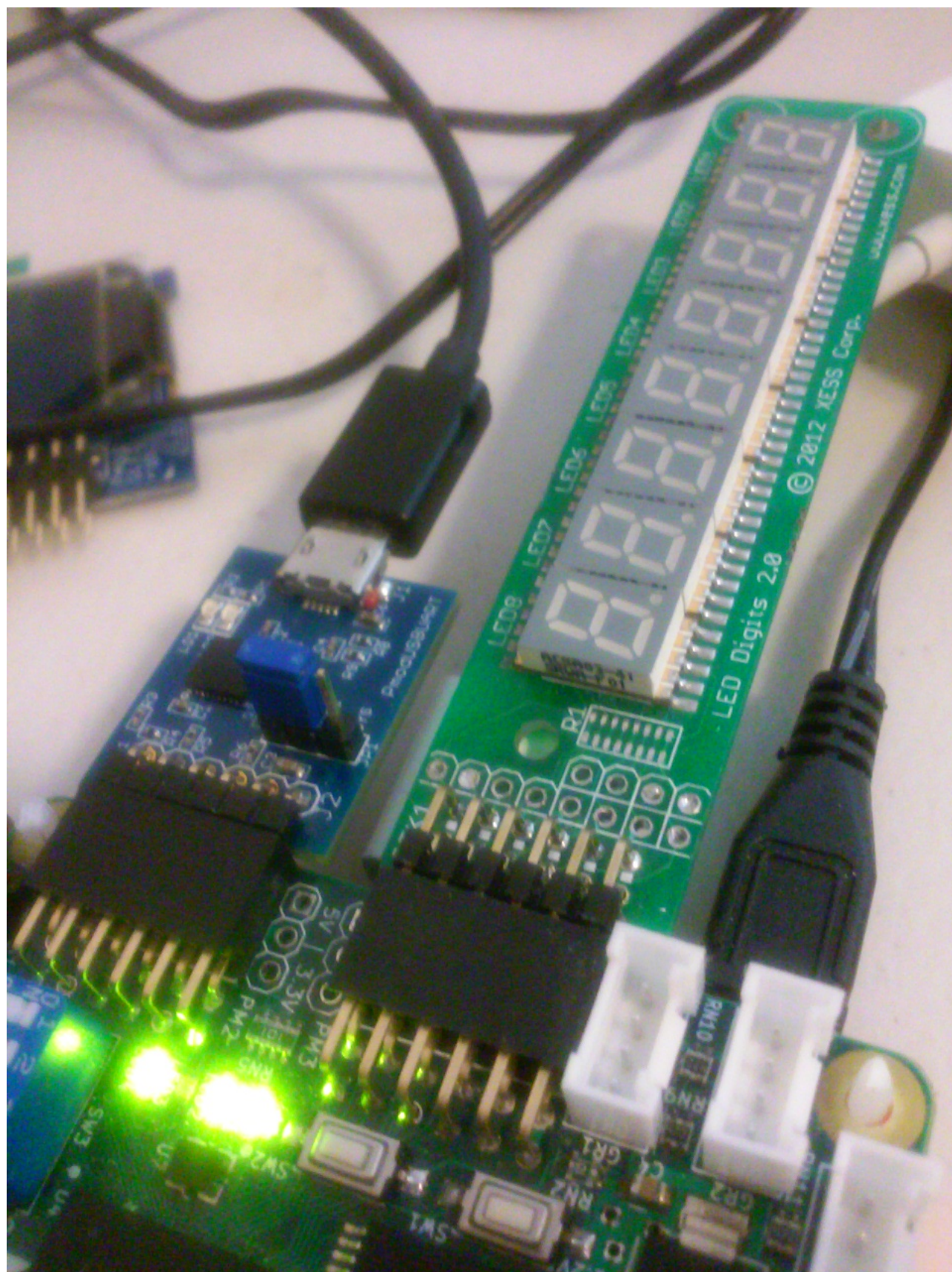
```
00001008 ( GPIO)-> 00020000
```

3<sup>rd</sup> led on

```
./arm-wbregs gpio 0x00040004
```

```
00001008 ( GPIO)-> 00040004
```







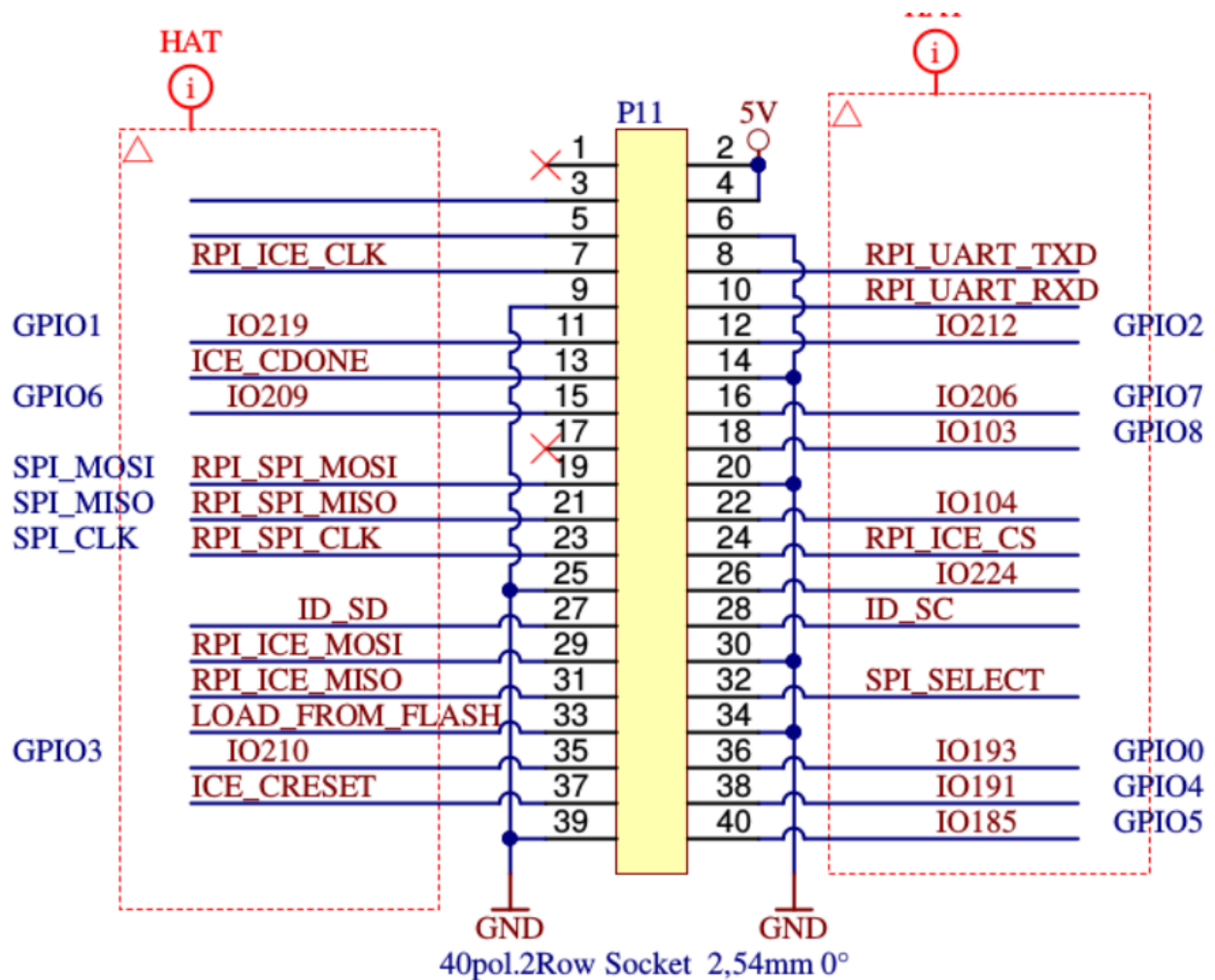
3<sup>rd</sup> led off

```
./arm-wbregs gpio 0x00040000  
00001008 ( GPIO)-> 00040000
```

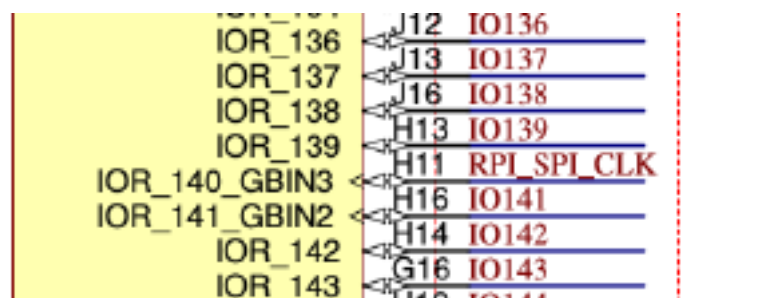
```
./arm-wbregs 0x2000 0x01  
00002000 ( RAM)-> 00000001  
pi@pi3-5:~/catzip/sw/host $ ./arm-wbregs ram  
00002000 ( RAM) : [...] 00000001  
pi@pi3-5:~/catzip/sw/host $ ./arm-wbregs 0x2000 0x02  
00002000 ( RAM)-> 00000002  
pi@pi3-5:~/catzip/sw/host $ ./arm-wbregs ram  
00002000 ( RAM) : [...] 00000002
```

```
./arm-wbregs pic  
00001004 ( PIC) : [...] 00000003
```

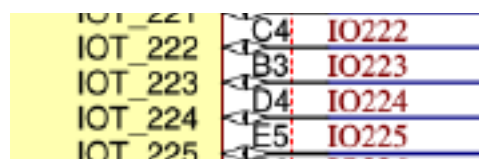
```
./arm-wbregs ufifo  
00000804 ( UFIFO) : [ @?@. ] 403f4000  
ICOBORD RPi
```



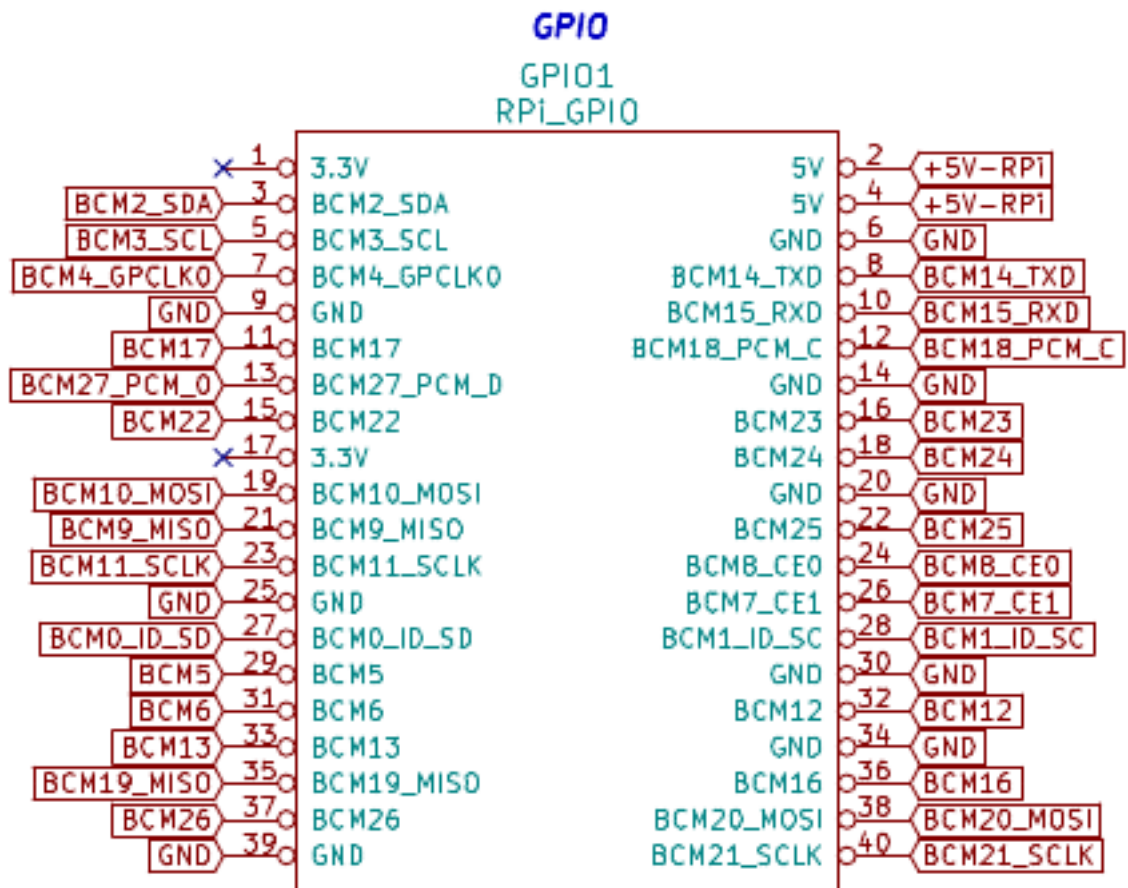
RPI\_SPI\_CLK H11 Pin 23 Pi icoboard



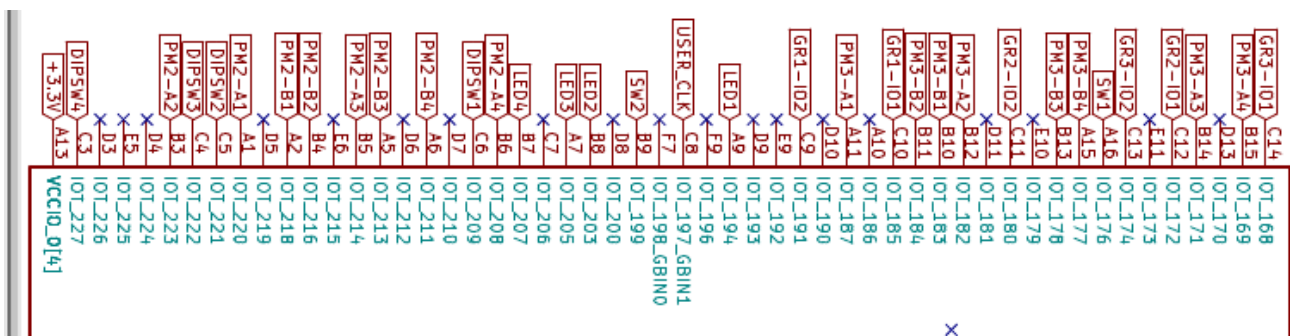
rpi\_cs D4 IOT\_224 Pin 26 Pi icoboard



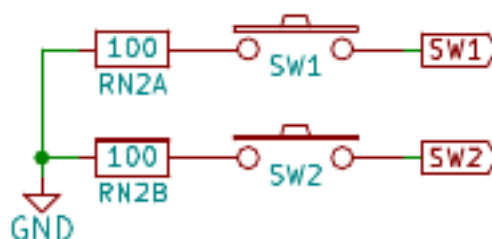
CATBOARD RPi



CATBOARD connection to FPGA pins PMOD 2 & PMOD 3 push button switches, dip switch, and leds.



CATBOARD sw1 & sw2



The diagram shows four parallel LED circuits. Each circuit consists of an LED (LED1, LED2, LED3, LED4) connected in series with a 100 ohm resistor (RN5D, RN5C, RN5B, RN5A). The LEDs are connected to a common ground (GND) through their cathodes. The anodes of the LEDs are connected to a common line that branches into four separate lines, each leading to a resistor. The resistors are connected to a common ground (GND) through their other terminals.

U4F  
iCE40-HX8K-CT256

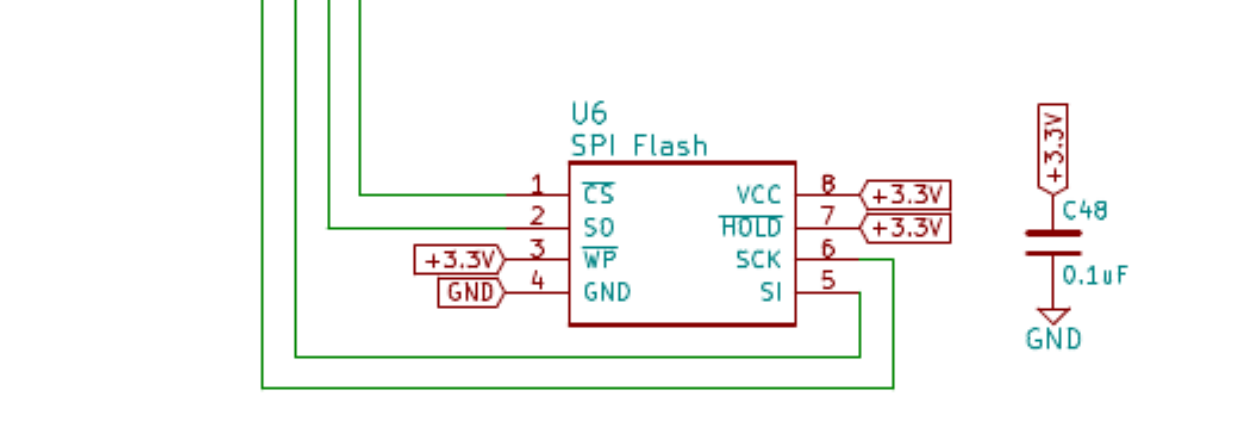
BCM9\_MISO  
BCM10\_MOSI  
BCM11\_SCLK  
BCM25

P12  
P11  
R11  
R12  
N13  
+3.3V

IOB\_105\_SDO  
IOB\_106\_SDI  
IOB\_107\_SCK  
IOB\_108\_SS  
VCC\_SPI

+3.3V  
4.7K  
RN3A  
+3.3V  
4.7K  
RN3B

+3.3V  
C47  
0.1uF  
GND



BCM7	L9	IOB_73
	X	IOB_74
BCM7_CE1	T7	IOB_75
BCM8_CEO	T8	IOB_76
	X	IOB_77
	X	IOB_78

## CATBOARD

HDR1-9	F2	IOB_79
	X	IOB_80
	H6	IOB_81
HDR1-10	F1	IOB_82
	X	IOB_83
	H4	IOB_84
HDR1-7	G2	IOB_85
	X	IOB_86
	J4	IOB_87
HDR1-6	H2	IOB_88
	X	IOB_89
	J5	IOB_90
HDR1-8	G1	IOB_91
	X	IOB_92
	J3	IOB_93
HDR1-3	H1	IOB_94
HDR1-4	J2	IOB_95
HDR1-1	J1	IOB_96
HDR1-2	K1	IOB_97
	X	IOB_98
	K3	IOB_99

- 2.) The 2<sup>nd</sup> issue is the PMOD connections to FPGA are different.
- 3.) Third, I do not have a Digilent PMOD 4 push button switch module.
- 4.) The 4<sup>th</sup> issue is the PHASE LOCK LOOP difference.

Post on #yosys

*Pin C8 is my USER\_CLK comes from a 100MHz osc. It is connected to IOT\_197\_GBIN1 on HX8K. When I try using it for as an input to PLL I get the fatal error: bad constraint on `i\_clk': no PLL at pin C8.*

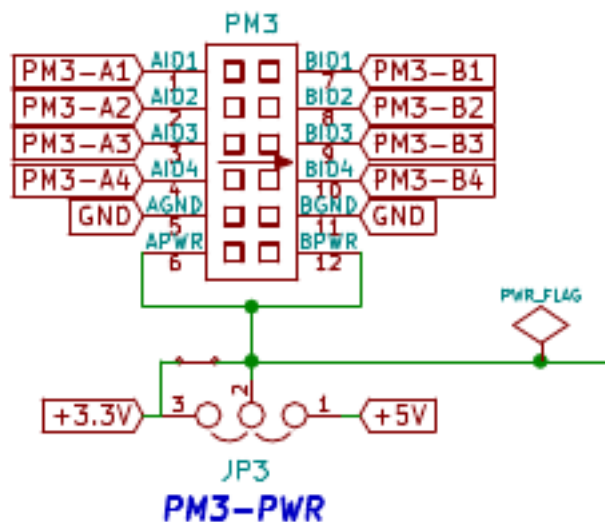
*Can only certain pins be used as inputs to PLL?*

*daveshah*

*develonepi3: use the SB\_PLL40\_CORE instead of SB\_PLL40\_PAD variant (and REFERENCECLK in instead of PACKAGEPIN)*

```
set_io clk_100mhz C8 #R9
```

```
set_io pmod1_1 A11 #D8
set_io pmod1_2 B12 #B9
set_io pmod1_3 B14 #B10
set_io pmod1_4 B15 #B11
# 654321 catboard # 654321 icoboard
# xxxxxx PMOD3 A # xxxxxx PMOD1 A
# xxxxxx PMOD3 B # xxxxxx PMOD1 B
# 654321 # 654321
#
set_io pmod1_7 B10 #B8
set_io pmod1_8 B11 #A9
set_io pmod1_9 B13 #A10
set_io pmod1_10 A15 #A11
```

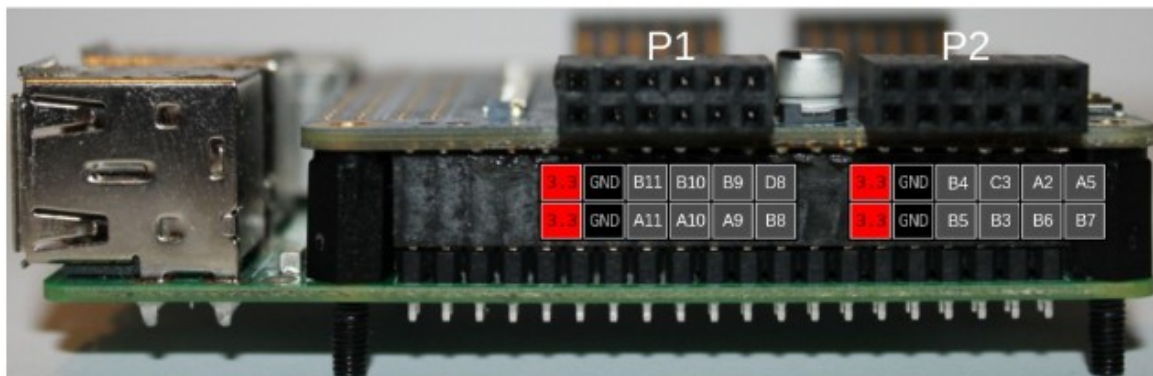


GR3-101	C14	I01.168
PM3-A4	B15	I01.169
PM3-A3	D13	I01.170
GR2-101	C12	I01.171
GR2-101	E11	I01.172
GR3-102	C13	I01.173
SW1	A16	I01.174
PM3-B4	A15	I01.176
PM3-B3	B13	I01.177
PM3-B3	E10	I01.178
GR2-102	C11	I01.179
PM3-A2	D11	I01.180
PM3-B1	B10	I01.181
PM3-B2	B11	I01.182
GR1-101	C10	I01.183
PM3-A1	A11	I01.184
GR1-102	C9	I01.185
PM3-A1	D10	I01.186
GR1-102	E9	I01.187
GR1-102	C9	I01.190
GR1-102	E9	I01.191
LED1	A9	I01.192
LED1	F9	I01.193
LED1	A9	I01.194
LED1	F9	I01.196
USER_CLK	C8	I01.197
USER_CLK	F7	I01.198
SW2	B9	I01.199
LED2	B8	I01.200
LED3	A7	I01.203
LED3	C7	I01.205
LED4	B7	I01.206
PM2-A4	B6	I01.207
DIPSW1	C6	I01.208
PM2-B4	D7	I01.209
PM2-B4	A6	I01.210
PM2-B3	A5	I01.211
PM2-A3	B5	I01.212
PM2-A3	E6	I01.213
PM2-B2	B4	I01.215
PM2-B1	A2	I01.216
PM2-B1	D5	I01.218
PM2-A1	A1	I01.219
DIPSW2	C4	I01.220
DIPSW3	B3	I01.221
PM2-A2	B3	I01.222
PM2-A2	D4	I01.223
PM2-A2	E5	I01.224
PM2-A2	D3	I01.225
PM2-A2	C3	I01.226
PM2-A2	A3	I01.227
+3.3V	A13	I01.227
VCCIO_0[4]		I01.227

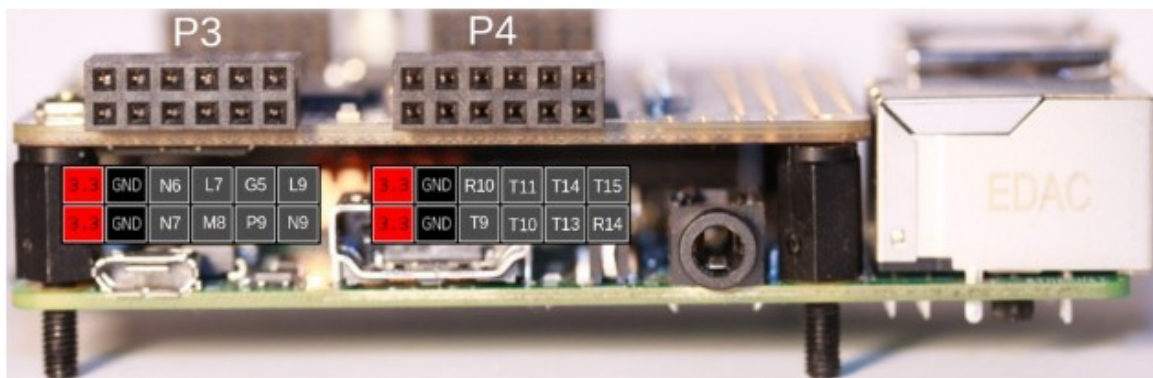
```
module top(clk_100mhz, pmod1_1, pmod1_2, pmod1_3, pmod1_4, pmod1_7, pmod1_8,
pmod1_9, pmod1_10, pmod2_7, pmod2_8, pmod2_9, pmod2_10, rpi_sck, rpi_cs,
rpi_mosi);
```

```
spi_ram_slave spi_ram_slave(clk, rpi_sck, rpi_cs, rpi_mosi,
    ram_addr, ram_data, ram_wr);
module spi_ram_slave(clk, sck, cs, mosi, ram_addr, ram_data, ram_wr);
PMOD pin out on icoboard
```

Pinout Pmod P1 and P2



Pinout PMOD P3 and P4



```
"lrwxrwxrwx 1 root staff 34 May 18 20:10 /usr/local/bin/config_cat ->
/home/pi/catboard_yosys/config_cat"
```

```
#!/bin/bash
```

```
# A script to configure Lattice iCE40 FPGA by SPI from Raspberry Pi
#
# Copyright (C) 2015 Jan Marjanovic <jan@marjanovic.pro>
#
# This program is free software: you can redistribute it and/or modify
# it under the terms of the GNU General Public License as published by
# the Free Software Foundation, either version 3 of the License, or
# (at your option) any later version.
#
# This program is distributed in the hope that it will be useful,
```



```
# but WITHOUT ANY WARRANTY; without even the implied warranty of
# MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE. See the
# GNU General Public License for more details.
#
# You should have received a copy of the GNU General Public License
# along with this program. If not, see <http://www.gnu.org/licenses/>.
```

```
echo ""
if [ $# -ne 1 ]; then
    echo "Usage: $0 FPGA-bin-file "
    exit 1
fi

if [ $EUID -ne 0 ]; then
    echo "This script must be run as root" 1>&2
    exit 1
fi
```

```
if [ ! -d /sys/class/gpio/gpio25 ]; then
    echo "GPIO 25 not exported, trying to export..."
    echo 25 > /sys/class/gpio/export
    if [ ! -d /sys/class/gpio/gpio25 ]; then
        echo "ERROR: directory /sys/class/gpio/gpio25 does not exist"
        exit 1
    fi
else
    echo "OK: GPIO 25 exported"
fi
```

```
if [ ! -d /sys/class/gpio/gpio17 ]; then
    echo "GPIO 17 not exported, trying to export..."
    echo 17 > /sys/class/gpio/export
    if [ ! -d /sys/class/gpio/gpio17 ]; then
        echo "ERROR: directory /sys/class/gpio/gpio17 does not exist"
        exit 1
    fi
else
    echo "OK: GPIO 17 exported"
fi
```

```
if [ ! -d /sys/class/gpio/gpio22 ]; then
    echo "GPIO 22 not exported, trying to export..."
    echo 22 > /sys/class/gpio/export
    if [ ! -d /sys/class/gpio/gpio22 ]; then
        echo "ERROR: directory /sys/class/gpio/gpio22 does not exist"
        exit 1
    fi
else
    echo "OK: GPIO 22 exported"
fi
```

```

echo ""
if [ -e /dev/spidev0.0 ]; then
    echo "OK: SPI driver loaded"
else
    echo "spidev does not exist"

    lsmod | grep spi_bcm2708 >& /dev/null

    if [ $? -ne 0 ]; then
        echo "SPI driver not loaded, try to load it..."
        modprobe spi_bcm2708

        if [ $? -eq 0 ]; then
            echo "OK: SPI driver loaded"
        else
            echo "Could not load SPI driver"
            exit 1
        fi
    fi
fi

echo ""
echo "Setting GPIO directions"
echo out > /sys/class/gpio/gpio25/direction
cat /sys/class/gpio/gpio25/direction
echo out > /sys/class/gpio/gpio22/direction
cat /sys/class/gpio/gpio22/direction
echo in > /sys/class/gpio/gpio17/direction
cat /sys/class/gpio/gpio17/direction

echo "Setting output to low"
echo 0 > /sys/class/gpio/gpio25/value
cat /sys/class/gpio/gpio25/value

#echo ""
#echo "Please reset the iCE40 FPGA board"
#echo "Press any key..."
#read

echo "Reseting FPGA"
echo 0 > /sys/class/gpio/gpio22/value
cat /sys/class/gpio/gpio22/value
echo 1 > /sys/class/gpio/gpio22/value
cat /sys/class/gpio/gpio22/value

echo "Checking DONE pin"
cat /sys/class/gpio/gpio17/value

echo "Continuing with configuration procedure"
dd if=$1 of=/dev/spidev0.0

```

```
echo -e "\x0\x0\x0\x0\x0\x0\x0" > /dev/spidev0.0
```

```
echo "Setting output to high"
```

```
echo 1 > /sys/class/gpio/gpio25/value
```

```
cat /sys/class/gpio/gpio25/value
```

```
echo "Checking DONE pin"
```

```
cat /sys/class/gpio/gpio17/value
```

```
"cd otl-icoboard-pmodoledrgb-demo/stream-tool/"
```

```
"ffmpeg -f v4l2 -i /dev/video0 -s 96x64 -f rawvideo -pix_fmt rgb565 - | ./stream-tool"
```