devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/board \$ make

Building dependency file(s)

zip-gcc -O3 -I../zlib -I../../rtl/catzip -I. -c -Wa,-nocis -fno-builtin cputest.c -o obj-zip/cputest.o zip-gcc -O3 -I../zlib -I../../rtl/catzip -I. -T boardram.ld -fno-builtin -Wl,-Map=obj-zip/cputest.map obj-zip/cputest.o -o cputest

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/board \$ zip-objdump -d cputest > cputest-disasm.txt

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-zipload -v ../board/cputest Halting the CPU

Memory regions:

Block RAM: 01400000 - 01402000 SDRAM : 02000000 - 03000000

Loading: ../board/cputest

Section 0: 02000000 - 02003e94

Writing to MEM: 02000000-02003e94

Clearing the CPUs registers Setting PC to 02000000

The CPU should be fully loaded, you may now

start it (from reset/reboot) with:

> wbregs cpu 0x0f

CPU Status is: 0000060f

```
2003d7c:
            4e 6f 74 20
                         LDI
                                 $-1084384,R9
            73 75 70 70
                         MOV.GE
2003d80:
                                    $-3984+uR5,uCC
2003d84:
            6f 72 74 65
                         ILL 6f727465
2003d88:
            64 0d 0a 00
                         CMP.Z
                                  $2560+R4,R12
2003d8c:
            53 75 70 70
                         MOV.GE
                                    $-3984+uR5,uR10
            6f 72 74 65
2003d90:
                         ILL 6f727465
2003d94:
            64 0d 0a 00
                         CMP.Z
                                  $2560+R4,R12
2003d98:
            4e 6f 20 4d
                         LDI
                                 $-1105843,R9
2003d9c:
            75 6c 74 69
                         SH.NZ
                                  CC,$-2967(R1)
            70 6c 79 20
                                    $-1760+R1,CC
2003da0:
                         AND.NZ
2003da4:
            49 6d 70 6c
                         LSR.NZ
                                   $-3988+R5,R9
```

```
devel@mypi3-16: \sim / testbuilds/catzip-tst/catzip/sw/host \$./arm-wbregs \ 0x2003d7c
```

02003d7c (): [Not.] 4e6f7420

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-wbregs 0x2003d80

02003d80 (): [supp] 73757070

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-wbregs 0x2003d84

02003d84 (): [orte] 6f727465

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-wbregs 0x2003d88

02003d88 (): [d...] 640d0a00

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-wbregs 0x2003d90

02003d90 (): [orte] 6f727465

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-wbregs 0x2003d94

02003d94 (): [d...] 640d0a00

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-wbregs 0x2003d98

02003d98 (): [No.M] 4e6f204d

```
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2003d9c
02003d9c (
               ): [ulti] 756c7469
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2003da0
02003da0 (
               ): [ply.] 706c7920
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2003da4
               ): [Impl] 496d706c
02003da4 (
Adding break at line 1111 in
void
       txstr(const char *str) {
       const char *ptr = str;
       zip_break();
       while(*ptr)
              txchr(*ptr++);
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/board/cputest.c
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/board $ make
Building dependency file(s)
zip-gcc -O3 -I../zlib -I../../rtl/catzip -I. -c -Wa,-nocis -fno-builtin cputest.c -o obj-zip/cputest.o
zip-gcc -O3 -I../zlib -I../../rtl/catzip -I. -T boardram.ld -fno-builtin -Wl,-Map=obj-zip/cputest.map
obj-zip/cputest.o -o cputest
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/board $ zip-objdump -d cputest > cputest-
disasm.txt
02001120 <txstr>:
                                     $8,SP
2001120:
              68 00 00 08
                            SUB
2001124:
              04 c7 40 00
                            SW
                                     R0,(SP)
                                     R5,$4(SP)
2001128:
              2c c7 40 04
                            SW
200112c:
              2b 40 40 00
                                      R1,R5
                           MOV
2001130:
              7f 00 00 00
                            BREAK
                                        @0x02001134 // 2001134 < txstr+0x14>
2001134:
              0d 84 40 00
                           LB
                                    (R1),R1
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2001120
02001120 (
               ): [h...] 68000008
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2001124
02001124 (
               ): [..@.] 04c74000
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2001128
02001128 (
               ): [,.@.] 2cc74004
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x200112c
0200112c (
               ): [+@@.] 2b404000
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2001130
02001130 (
               ): [....] 7f000000
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-wbregs 0x2001134
02001134 (
               ): [..@.] 0d844000
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-zipload -v ../board/cputest
Halting the CPU
Memory regions:
       Block RAM: 01400000 - 01402000
       SDRAM
                   : 02000000 - 03000000
Loading: ../board/cputest
Section 0: 02000000 - 02003e98
Writing to MEM: 02000000-02003e98
```

Clearing the CPUs registers
Setting PC to 02000000
The CPU should be fully loaded, you may now start it (from reset/reboot) with:
> wbregs cpu 0x0f

CPU Status is: 0000060f

Needs to be restarted after every break.

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sim/verilated $\$./arm-main_tb Listening on port 8363 Listening on port 8364 > T

CMD: Only sent 0 bytes of 3!

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-zipload -v ../board/cputest Halting the CPU Memory regions:

Block RAM: 01400000 - 01402000 SDRAM : 02000000 - 03000000

Loading: ../board/cputest

Section 0: 02000000 - 02003e98

Writing to MEM: 02000000-02003e98

Clearing the CPUs registers Setting PC to 02000000

The CPU should be fully loaded, you may now

start it (from reset/reboot) with:

> wbregs cpu 0x0f

CPU Status is: 0000060f

devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host \$./arm-zipdbg

When g is pressed.

SUCCESS

sR0: 02002238 sR1: 02003d7c sR2: 02003e98 sR3: 00000000 sR4: 00000000 sR5: 02003d7c sR6: 02003e18 sR7: 00000000 sR8: 00000000 sR9: 00000000 sR10: 00000000 sR11: 00000000 sR12: 00000000 sPC: 02001130

uR0: 00000000 uR1: 00000000 uR2: 00000000 uR3: 00000000 uR4: 00000000 uR5: 00000000 uR6: 00000000 uR7: 00000000 uR8: 00000000 uR9: 00000000 uR10: 00000000 uR11: 00000000 uR12: 00000000 uSP: 00000000 uCC: 00000020 uPC: 00000000