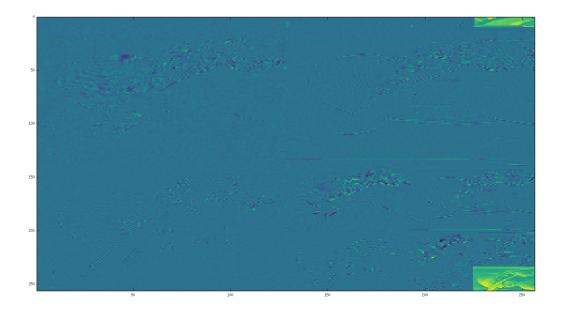
This is an attempt at trying to understand why cputest and jpeg fail in hardware on mypi3-21. Several software packages aree needed (autofpga, icestorm, nextpnr, yoysys, zipcpu, and verilator). Additional Verilog (wbxbar, skidbuffer.v, and addrdecode.v) files were needed with autofpga ver 08/14/20.

	Мурі3-18		Mypi3-16	Mypi3-20		upgraded	No-upgrade	githu	b	Upgraded-on
autofpga	Χ		Χ	Χ		08/14/20	01/01/20	no		Mypi3-16
icestorm	Χ		Χ	Χ		03/09/21		no		Mypi3-16
nextpnr	Χ		Χ			03/26/21	02/03/20	no		Mypi3-16
yosys			Χ			03/30/21	02/09/20	no		Mypi3-16
verilator		4.1	4	.1	4.1	-				
zipcpu	Χ			Χ		11/11/21	04/01/19	1	11/11/21	Mypi3-20
Catzip-tst			Х							
Mypi3-21	Tb3-18		Tb3-18-tst	tb3-20-tst		Tb3-16	Tb3-20			
jpgeg						X	X			Tb3-16Tb3-20 im4(1:10,1:1)=0
cputest						Х	X			
sdram test hw	'X		Χ	Χ						
Arachne-pnr	no		no	no		binary	no			tb3-18-tsttb3-20-tst modified: Makefile
	0x0100f12	0	0x0200f120	0x0200f12	20	0x0100f120	0x0100f120			
version	20210	419	2021042	20 20210	420	20200702	20210419	ı		

On tb3-20 ver 20210419 & tb3-16 ver 20200702 show same results with jpeg.



octave:3> im4(1:10,1:1) ans =

237118588 232923267 237114485

```
238166139
 236071034
 237115516
 235018352
 233970337
 230821997
      0
octave:5 im4(1:10,1:1)=0;
octave:6> imagesc(im4)
Additional notes are found in fpgatools-upgrade-mypi3-18.txt & fpgatools-upgrade-mypi3-20.txt.
Testing upgrading vosys which does not work. Testing upgrading nextpnr.
upgrade yosys & dn-grading autofpga
devel@mypi3-20:~ $ mv yosys/ yosys-pre
devel@mypi3-20:~ $ sudo unsquashfs -d yosys
[sudo] password for devel:
Parallel unsquashfs: Using 4 processors
6720 inodes (14490 blocks) to write
[=========]] 14490/14490 100%
created 6720 files
created 412 directories
created 0 symlinks
created 0 devices
created 0 fifos
devel@mypi3-20:~ $ cd yosys
devel@mypi3-20:~/yosys $ sudo make install
[Makefile.conf] CONFIG := gcc
mkdir -p /usr/local/bin
cp yosys yosys-config yosys-abc yosys-filterlib yosys-smtbmc /usr/local/bin
strip -S /usr/local/bin/yosys
strip /usr/local/bin/yosys-abc
strip /usr/local/bin/yosys-filterlib
mkdir -p /usr/local/share/yosys
cp -r share/. /usr/local/share/yosys/.
downgrading autofpga
devel@mypi3-20:~ $ mv autofpga autofpga-upgraded
devel@mypi3-20:~ $ cp -R autofpga033021/ autofpga
devel@mypi3-20:~/autofpga $ Is -la /usr/local/bin/autofpga
lrwxrwxrwx 1 root root 32 Jun 17 2020 /usr/local/bin/autofpga -> /home/devel/autofpga/sw/autofpga
verilator -Wno-TIMESCALEMOD -O3 -Mdir ./obj-arm -trace -cc -y cpu -y ../hexbus -y ../pport main.v
cd ./obj-arm; make -f Vmain.mk
/usr/bin/perl /usr/local/share/verilator/bin/verilator includer -DVL INCLUDE OPT=include Vmain.cpp
Vmain Dpi.cpp Vmain Trace.cpp Vmain Slow.cpp Vmain Syms.cpp Vmain Trace Slow.cpp >
Vmain ALL.cpp
q++ -I. -MMD -l/usr/local/share/verilator/include -l/usr/local/share/verilator/include/vltstd -
DVM COVERAGE=0 -DVM SC=0 -DVM TRACE=1 -faligned-new -fcf-protection=none -Wno-bool-
operation -Wno-sign-compare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-unused-parameter -
Wno-unused-variable -Wno-shadow
                                   -std=gnu++14 -Os -c -o Vmain ALL.o Vmain ALL.cpp
Archive ar -cr Vmain_ ALL.a Vmain_ ALL.o
yosys -ql simple.log -p synth ice40 -blif catzip.blif -json catzip.json -top toplevel ...
Warning: reg '\txf wb write' is assigned in a continuous assignment at ../hexbus/console.v:301.10-301.39.
```

Warning: reg '\txf wb data' is assigned in a continuous assignment at ../hexbus/console.v:302.10-302.38.

```
ERROR: Cell port main.genbus.o wb sel is driving constant bits: \hb sel <= \genbus.o wb sel
make[2]: *** [Makefile:108: catzip.blif] Error 1
make[1]: *** [Makefile:68: catzip] Error 2
make: *** [Makefile:156: rtl] Error 2
devel@mypi3-20:~/testbuilds/catzip $ git diff rtl/catzip/Makefile
diff --git a/rtl/catzip/Makefile b/rtl/catzip/Makefile
index 1102df7..a38dfa5 100644
--- a/rtl/catzip/Makefile
+++ b/rtl/catzip/Makefile
@@ -68,7 +68,7 @@ verilated: $(VDIRFB)/Vmain ALL.a
$(VDIRFB)/Vmain.cpp: $(VDIRFB)/Vmain.h
$(VDIRFB)/Vmain.mk: $(VDIRFB)/Vmain.h
$(VDIRFB)/Vmain.h: main.v $(VFLIST)
    verilator -Wno-TIMESCALEMOD -O3 -Mdir $(VDIRFB) -trace -cc $(AUTOVDIRS) main.v
     verilator -Wall -Wno-TIMESCALEMOD -O3 -Mdir $(VDIRFB) -trace -cc $(AUTOVDIRS) main.v
cpudefs.h: cpu/cpudefs.v
     @echo "Building cpudefs.h"
dn-grading yosys & dn-grading autofpga
devel@mypi3-20:~ $ mv yosys yosys-upgraded
devel@mypi3-20:~ $ cp -R yosys-pre/ yosys
devel@mypi3-20:~ $ cd yosys
devel@mypi3-20:~/yosys $ sudo make install
[ 0%] Building kernel/driver.o
[ 1%] Building kernel/register.o
[ 1%] Building kernel/log.o
[ 2%] Building kernel/calc.o
[ 7%] Building libs/ezsat/ezminisat.o
[77%] Building backends/smv/smv.o
[77%] Building backends/blif/blif.o
[ 78%] Building backends/smt2/smt2.o
[ 78%] Building backends/spice/spice.o
[100%] Building yosys
[100%] Building yosys-abc
mkdir -p /usr/local/bin
cp yosys yosys-config yosys-abc yosys-filterlib yosys-smtbmc /usr/local/bin
strip -S /usr/local/bin/yosys
strip /usr/local/bin/yosys-abc
strip /usr/local/bin/yosys-filterlib
mkdir -p /usr/local/share/yosys
cp -r share/. /usr/local/share/yosys/.
devel@mypi3-20:~/yosys $ yosys -V
Yosys 0.9+1706 (git sha1 7cc9d487, clang 7.0.1-8+rpi3+deb10u2 -fPIC -Os)
devel@mypi3-20:~/testbuilds/catzip $ git checkout rtl/catzip/Makefile
devel@mypi3-20:~/testbuilds/catzip $ make clean; make
upgrading nextpnr
sudo mv nextpnr nextpnr-pre
devel@mvpi3-20:~ $ sudo unsquashfs -d nextpnr
/media/devel/1b763776-4e1d-499c-9f24-a116a58c161f/fpgatools/testing03021/nextpnr032621 4419c36.img
cd nextpnr
```

sudo make install

devel@mypi3-20:~/testbuilds/catzip \$ nextpnr-ice40 -V nextpnr-ice40 -- Next Generation Place and Route (Version 4419c36d)

devel@mypi3-20:~/nextpnr \$ git log

commit 4419c36db5556d2a7f600517d6a4b5673067579d (HEAD -> master, upstream/master)

Merge: 0e9a1abc d0bc033a Author: gatecat <gatecat@ds0.me> Date: Fri Mar 26 18:39:18 2021 +0000

testing testbuilds/tb3-20b

devel@mypi3-20:~/testbuilds \$ rsync -avl --delete catzip mypi3-21:~/testbuilds/tb3-20b/

devel@mypi3-21:~/testbuilds/tb3-20b/catzip/sw/host \$ sudo config cat ../../rtl/catzip/catzip.bin

devel@mypi3-21:~/testbuilds/tb3-20b/catzip/sw/host \$ sudo ./arm-netpport Listening on port 8363 Listening on port 8364

devel@mypi3-21:~/testbuilds/tb3-20b/catzip/sw/host \$./arm-zipload -v ../board/cputest

Halting the CPU Memory regions:

Block RAM: 00a00000 - 00a02000 SDRAM : 01000000 - 02000000

Loading: ../board/cputest

Section 0: 01000000 - 01003e94 Writing to MEM: 01000000-01003e94

Clearing the CPUs registers Setting PC to 01000000

The CPU should be fully loaded, you may now

start it (from reset/reboot) with:

> wbregs cpu 0x0f

CPU Status is: 0000060f

devel@mypi3-21:~/testbuilds/tb3-20b/catzip/sw/host $\$./arm-wbregs cpu 0x0f 02000000 ()-> 0000000f

. Running CPU self-test

_ -----Pass . SIM Instructions . CIS Instructions Supported . Break test #1 Pass . Break test #2 Pass . Break test #3 Pass . Early Branch test Pass . Trap test/AND Pass Pass . Trap test/CLR . Overflow test Pass . Carry test Pass . Loop test Pass . Shift test Pass . Pipeline test Pass . Mem-Pipeline test Pass

- . Conditional Execution test Pass
- . No-waiting pipeline test Pass. Conditional Branching test Pass
- . Ill Instruction test, NULL PC Pass
- . III Instruction test, two Pass

```
. Comparison test, ==
                             Pass
. Comparison test, !=
                            Pass
. CC Register test
                           Pass
. Multi-Arg test
                         Pass
. Multiply test
                        Pass
. Multiply HI-word test
                            Pass
. Divide test
                        Pass
. All tests passed. Halting CPU.
devel@mypi3-21:~/testbuilds/tb3-20b/catzip/sw/host $ ./arm-wbregs version
00800010 ( VERSION) : [.!..] 20210420
FPGA was interrupted
devel@mypi3-21:~/testbuilds/tb3-20b/catzip/sw/host $ ./runjpeg.sh
00a01000 (
                )-> 00000002
00a01004 (
                )-> 0000001
Halting the CPU
Memory regions:
    Block RAM: 00a00000 - 00a02000
    SDRAM
                : 01000000 - 02000000
Loading: ../board/jpeg
Section 0: 01000000 - 0104f1b4
Writing to MEM: 01000000-0104f1b4
Clearing the CPUs registers
Setting PC to 01000000
The CPU should be fully loaded, you may now
start it (from reset/reboot) with:
> wbregs cpu 0x0f
CPU Status is: 0000060f
The size of the buffer is 0x010000 or 65536 words
READ-COMPLETE
               )-> 0000000f
02000000 (
Write-COMPLETE
The size of the buffer is 0x010000 or 65536 words
. ptrs.inpbuf = 0x100f144 buf red = 0xdd20c80
. fwd inv = 0xdda0c88
x = 0xde22c76 sp = 0x76 z = 0x76
x = 0xdf2006a sp = 0x6a z = 0x6a
x = 0xde20c69 sp = 0x69 z = 0x69
x = 0xdb2106f sp = 0x6f z = 0x6f
x = 0x0 \text{ sp} = 0x0 \text{ z} = 0x0
x = 0x0 \text{ sp} = 0x0 \text{ z} = 0x0
. spliting blue sub band
. fwd lifting step only
. w = 0x100 wptr = 0xdd20c80 alt = 0xdd60c80 fwd inverse = 0xdda0c88 fwd inver. = 0x1
. starting red dwt
. in singlelift
. testing test fwd
. finished ted dwt
```

libEGL warning: DRI3: failed to query the version libEGL warning: DRI2: failed to authenticate GNU Octave, version 4.4.1 Copyright (C) 2018 John W. Eaton and others. This is free software; see the source code for copying conditions. There is ABSOLUTELY NO WARRANTY; not even for MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE. For details, type 'warranty'.

Octave was configured for "arm-unknown-linux-gnueabihf".

Additional information about Octave is available at https://www.octave.org.

Please contribute if you find this software useful. For more information, visit https://www.octave.org/get-involved.html

Read https://www.octave.org/bugs.html to learn how to submit bug reports. For information about changes from previous versions, type 'news'.

```
octave:1> rgb
octave:2> im4(1:10,1:1)
ans =
 237118588
 232923267
 237114485
 238166139
 236071034
 237115516
 235018352
 233970337
 230821997
      0
octave:3> im4(1:10,1:1)=0;
octave:4> imagesc(im4)
nextpnr upgrades ok
```