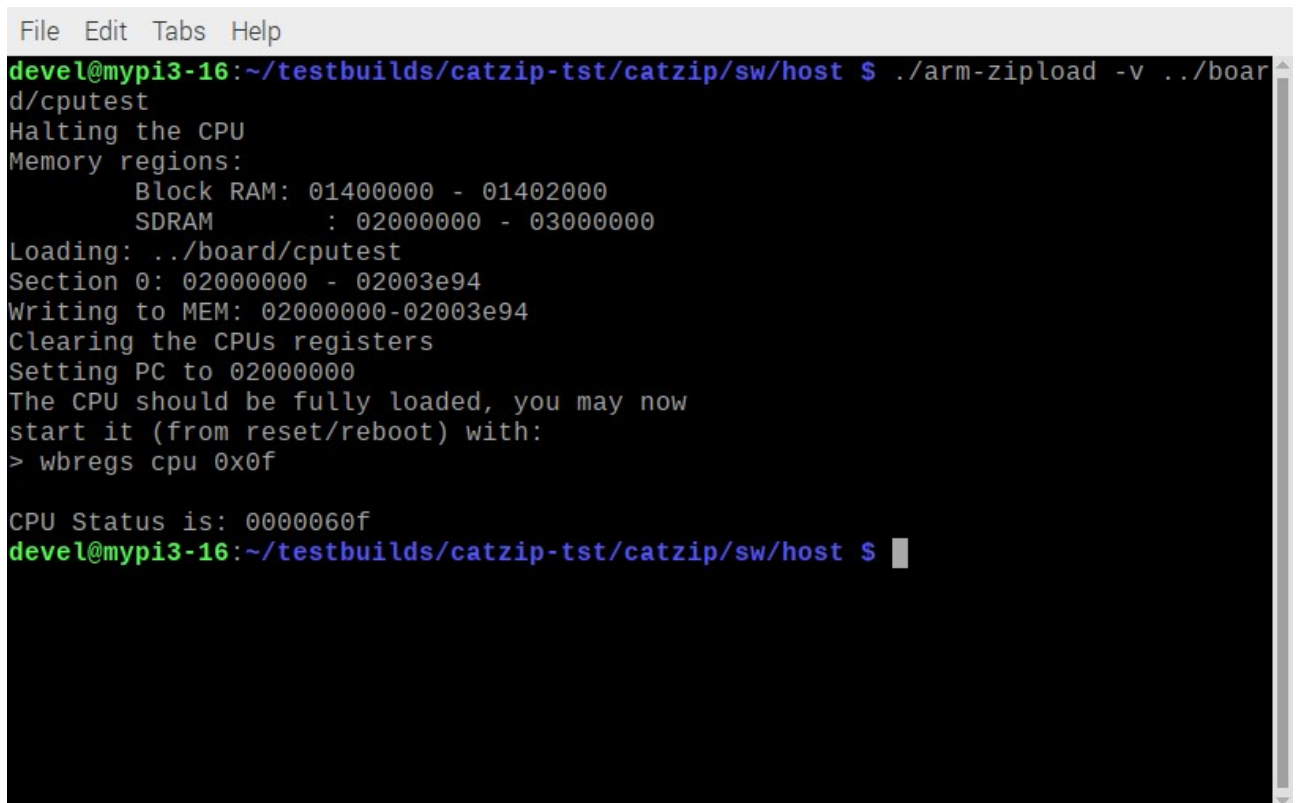


Starting the simulation.

```
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sim/verilated $ ./arm-main_tb  
Listening on port 8363  
Listening on port 8364  
> T  
CMD: Only sent 0 bytes of 3!
```

Loading the cputest program.



```
File Edit Tabs Help  
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-zipload -v ../board/cputest  
Halting the CPU  
Memory regions:  
    Block RAM: 01400000 - 01402000  
    SDRAM      : 02000000 - 03000000  
Loading: ../board/cputest  
Section 0: 02000000 - 02003e94  
Writing to MEM: 02000000-02003e94  
Clearing the CPUs registers  
Setting PC to 02000000  
The CPU should be fully loaded, you may now  
start it (from reset/reboot) with:  
> wbrege cpu 0x0f  
  
CPU Status is: 0000060f  
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $
```

Starting the debugger.

```
devel@mypi3-16:~/testbuilds/catzip-tst/catzip/sw/host $ ./arm-zipdbg
```

```

File Edit Tabs Help
Peripherals CPU State: 0x00000613 Supervisor mode
>PIC > 0x00000000< WDT : 0x00000000 WBUS: 0x00000000 PIC2: 0x00000000
TMRA: 0x00000000 TMRB: 0x00000000 TMRC: 0x00000000 JIF : 0x00000000
MTSK: 0x00000000 MOST: 0x00000000 MPST: 0x00000000 MICT: 0x00000000

Supervisor Registers
sR0 : 0x00000000 sR1 : 0x00000000 sR2 : 0x00000000 sR3 : 0x00000000
sR4 : 0x00000000 sR5 : 0x00000000 sR6 : 0x00000000 sR7 : 0x00000000
sR8 : 0x00000000 sR9 : 0x00000000 sR10: 0x00000000 sR11: 0x00000000
sR12: 0x00000000 sSP : 0x00000000 sCC : sPC : 0x02000000

User Registers
uR0 : 0x00000000 uR1 : 0x00000000 uR2 : 0x00000000 uR3 : 0x00000000
uR4 : 0x00000000 uR5 : 0x00000000 uR6 : 0x00000000 uR7 : 0x00000000
uR8 : 0x00000000 uR9 : 0x00000000 uR10: 0x00000000 uR11: 0x00000000
uR12: 0x00000000 uSP : 0x00000000 uCC : uPC : 0x00000000

0x02000008 0x16000000 CLR R2 >00000000 (Bus Err)
0x02000004 0x0e000000 CLR R1 00000004 (Bus Err)
>0x02000000 0x06000000 CLR R0 00000008 (Bus Err)
0x01ffffff 0x----- (Bus Error) 0000000c (Bus Err)
00000010 (Bus Err)

```

```

01000000 <_start>:
1000000: 06 00 00 00 CLR R0
1000004: 0e 00 00 00 CLR R1
1000008: 16 00 00 00 CLR R2
100000c: 1e 00 00 00 CLR R3
1000010: 26 00 00 00 CLR R4
1000014: 2e 00 00 00 CLR R5
1000018: 36 00 00 00 CLR R6
100001c: 3e 00 00 00 CLR R7
1000020: 46 00 00 00 CLR R8
1000024: 4e 00 00 00 CLR R9
1000028: 56 00 00 00 CLR R10
100002c: 5e 00 00 00 CLR R11
1000030: 66 00 00 00 CLR R12

```

After several steps the sSP is set 0x03000000 to the top of sdram. The sPC is at 0x0200003c

File Edit Tabs Help

Peripherals CPU State: 0x00000613 Supervisor mode  
>PIC > 0x00000000< WDT : 0x00000000 WBUS: 0x00000000 PIC2: 0x00000000  
TMRA: 0x00000000 TMRB: 0x00000000 TMRC: 0x00000000 JIF : 0x00000000  
MTSK: 0x00000000 MOST: 0x00000000 MPST: 0x00000000 MICT: 0x00000000

### Supervisor Registers

sR0 : 0x00000000 sR1 : 0x00000000 sR2 : 0x00000000 sR3 : 0x00000000  
sR4 : 0x00000000 sR5 : 0x00000000 sR6 : 0x00000000 sR7 : 0x00000000  
sR8 : 0x00000000 sR9 : 0x00000000 sR10: 0x00000000 sR11: 0x00000000  
sR12: 0x00000000 sSP : 0x03000000 sCC : sPC : 0x0200003c

### User Registers

uR0 : 0x00000000 uR1 : 0x00000000 uR2 : 0x00000000 uR3 : 0x00000000  
uR4 : 0x00000000 uR5 : 0x00000000 uR6 : 0x00000000 uR7 : 0x00000000  
uR8 : 0x00000000 uR9 : 0x00000000 uR10: 0x00000000 uR11: 0x00000000  
uR12: 0x00000000 uSP : 0x00000000 uCC : uPC : 0x00000000

0x02000044 0x7c87c000 LJMP >03000000 (Bus Err)  
0x02000040 0x0343c002 MOV 0x0200004c, R0 03000004 (Bus Err)  
>0x0200003c 0x76000000 TRAP 03000008 (Bus Err)  
0x0200003c 0x76000000 TRAP 0300000c (Bus Err)  
03000010 (Bus Err)