

```
ppio #(.W(16))
    sdramioi(o_ram_we_n, io_ram_data, o_ram_data, i_ram_data);
module ppio(i_dir, io_data, i_data, o_data);
    parameter W=8;
                     i dir:
    input
    inout [(W-1):0]io_data;
    input [(W-1):0]i_data;
    output [(W-1):0] o data;
    genvar k;
    generate
    for(k=0; k<W; k=k+1)
        SB_IO #(.PULLUP(1'b0),
            .PIN TYPE(6'b101001))
            theio(
                 .OUTPUT ENABLE(!i dir),
                 .PACKAGE_PIN(io_data[k]),
                 .D OUT 0(i data[k]),
                .D IN 0( o data[k])
    endgenerate
endmodule
```

Chg'ed catzip toplevl to be similar to xulalx25soc

```
assign io_ram_data = (ram_drive_data) ? o_ram_data : 16'bzzzz_zzzz_zzzz_zzzz;
reg [15:0]    r_ram_data_ext_clk;
// always @(posedge intermediate_clk_n)
always @(posedge s_clk)
    r_ram_data_ext_clk <= io_ram_data;
always @(posedge s_clk)
    i_ram_data <= r_ram_data_ext_clk;
assign o_ram_clk = s_clk;</pre>
```

Write 0x2000000 0x55AAAA55 Address 0x0000 o_ram_data 0x55AA o_ram_we_n & o_ram_cas_n & o_ram_dmod catzip

Lower 16 bits get written to File Edit Search Time Markers View Help upper 16 bits hw To: 5924881 ps | G | Marker: 2393897 ps | Cursor: 2392563 ps ∃ SST Waves Signals ⊼ Time - 🚠 buspici i clk=1 i wb cvc=1 i_wb_sel[3:0]=F ⊕ i aenbus i wb stb=0 - 🚠 gpioi i_wb_we =1 o_wb_stall=0 o_wb_ack=0 - 🚠 hbi_pp i_wb_addr[22:0]=000000 i wb data[31:0]=55AAAA55 55AAAA55 i_ram_data[15:0] =0000 55AA AA55 0000 ⊕ iii swic o_ram_data[15:0] =55AA AA55 55AA o ram addr[12:0] =0000 L ... watchdogi o ram we n=0 last ram data[15:0] =0000 55AA AA55 0000 Type Signals o_ram_bs[1:0] =00 wire r_addr[22:0] o_ram_cas_n =0 wire r_bank_valid o ram cke=1 o_ram_cs_n =0 wire r_barrell_ack[5:0] o ram dmod =1 o ram dgm[1:0]=00 wire r data[31:0] o_ram_ras_n =1 wire r_pending refresh_clk[9:0] =109 11F | 11E | 11D | 11C | 11B | 11A | 119 | 118 | 117 | 116 | 115 | 114 | 113 | 112 | 111 | 110 | 10F | 10E | 10D | 10C | 10B | 10A | 109 | 108 | 107 | 106 | 105 | 104 | 103 | 102 | 101 | 100 | 0FF | 0FE | 106 wire r_sel[3:0] wire r_we wire ram_data[15:0] wire refresh_cmd wire startup_hold wire startup_idle[15:0] wire trigger wire unused[2:0] Filter: Append Insert Replace

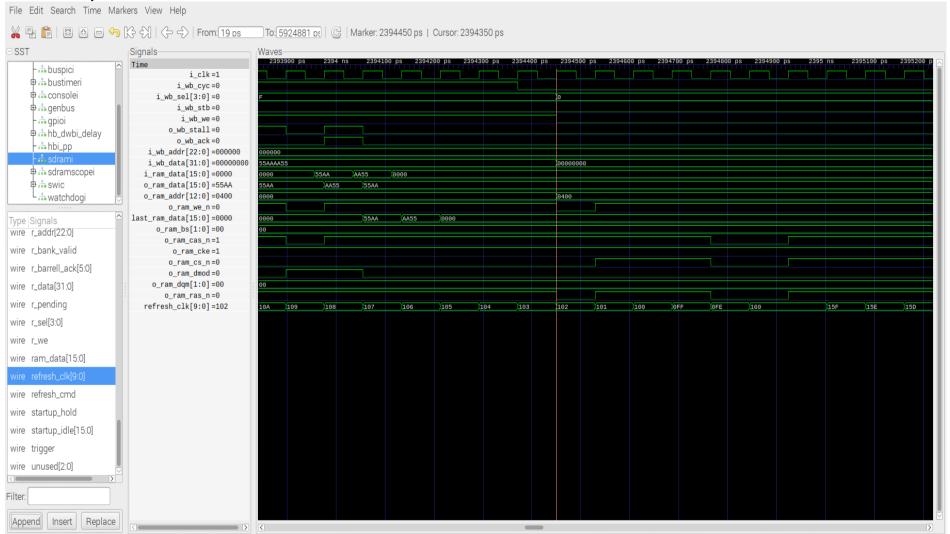
Frror in simulation no lower

o ram data should be 0xaa55

16 bits & hw

Write 0x2000000 0x55AAAA55 Address 0x0400 o_ram_data 0x55AA o_ram_we_n & o_ram_ras_n catzip

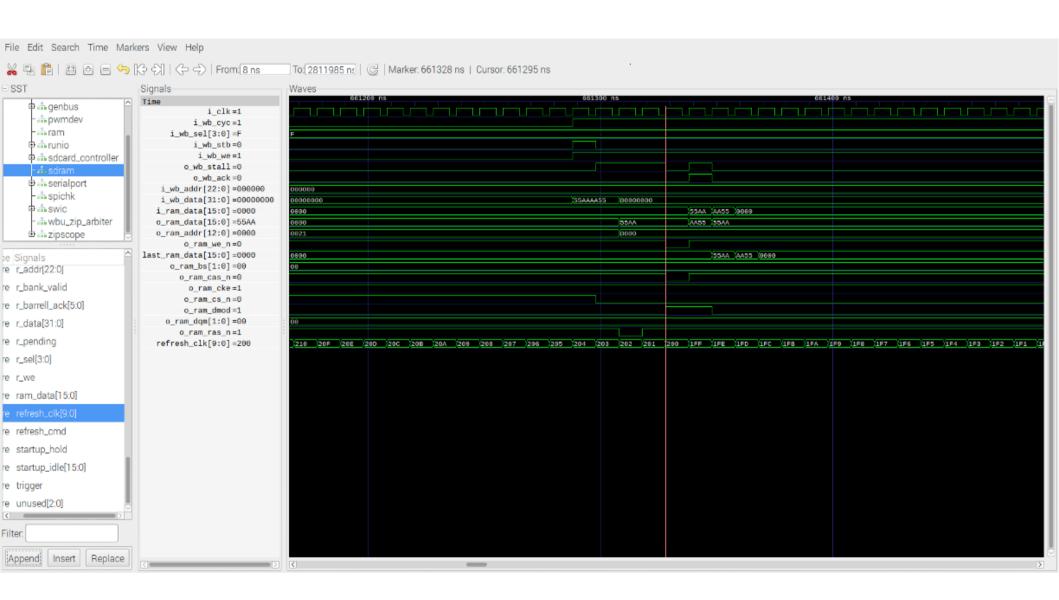
Error in simulation no lower 16 bits & hw o_ram_data should be 0xaa55
Lower 16 bits get written to upper 16 bits hw



xula2lx25soc toplevel

```
wire ram drive data
reg [15:0] r ram data, // Data lines (input)
wire [15:0] ram data, // Data lines (output)
assign io_ram_data = (ram_drive_data) ? ram_data : 16'bzzzz_zzzz_zzzz_zzzz;
reg [15:0] r ram data ext clk;
// always @(posedge intermediate clk n)
always @(posedge clk s)
    r ram data ext clk <= io ram data;
always @(posedge clk s)
    r ram data <= r ram data ext clk;
module busmaster(i clk, i rst,
        i rx stb, i rx_data, o_tx_stb, o_tx_data, i_tx_busy,
        // The SPI Flash lines
        o sf cs n, o sd cs n, o spi sck, o spi mosi, i spi miso,
        // The SDRAM lines
        o ram cs n, o ram cke, o ram ras n, o ram cas n,
            o ram we n, o ram bs, o ram addr,
            o ram_drive_data, i_ram_data, o_ram_data,
```

Write 0x2000000 0x55AAAA55 Address 0x0000 o_ram_data 0x55AA o_ram_we_n & o_ram_cas_n & o_ram_dmod xulalx25soc



Write 0x2000000 0x55AAAA55
Address 0x0400 o_ram_data 0x55AA
o_ram_we_n & o_ram_ras_n
xulalx25soc

Error in simulation hw okay xulalx25soc Should be o_ram_data 0xaa55

