**********DRAFT**********

SDRAM

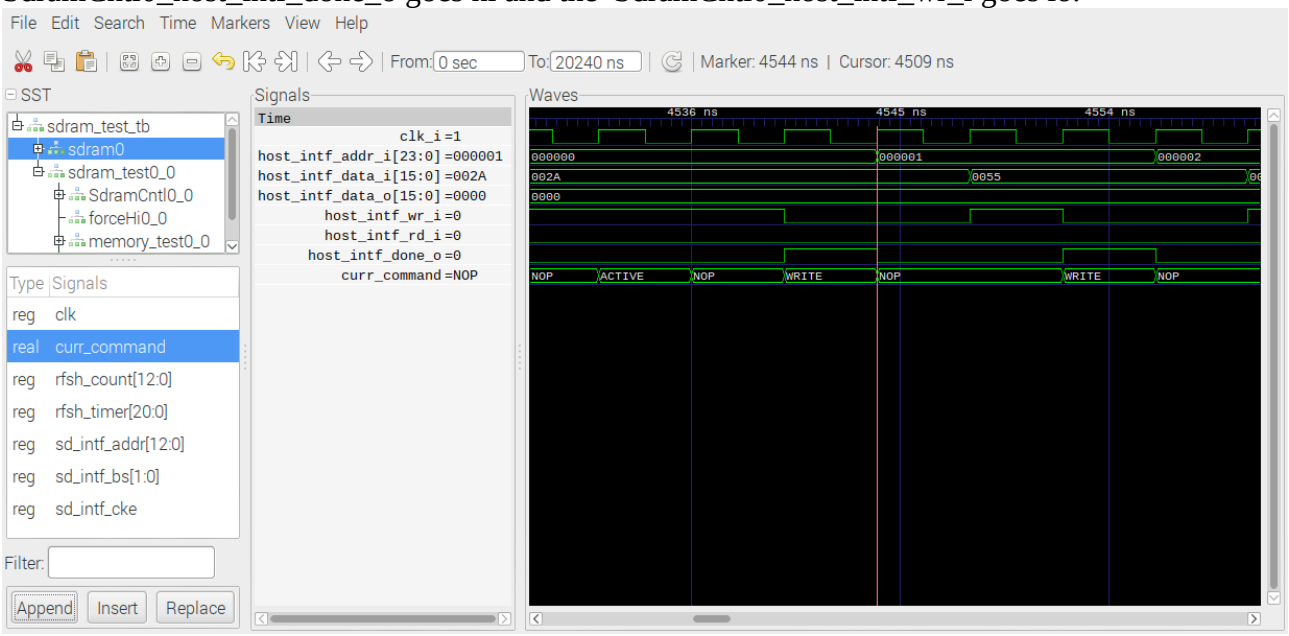
09/11/18

**********DRAFT**********

Host interface signals
wire [23:0] SdramCntl0_host_intf_addr_i;
wire SdramCntl0_host_intf_rd_i;
wire [15:0] SdramCntl0_host_intf_data_i;
wire [15:0] SdramCntl0_host_intf_data_o;
wire SdramCntl0_host_intf_done_o;
wire SdramCntl0_host_intf_wr_i;

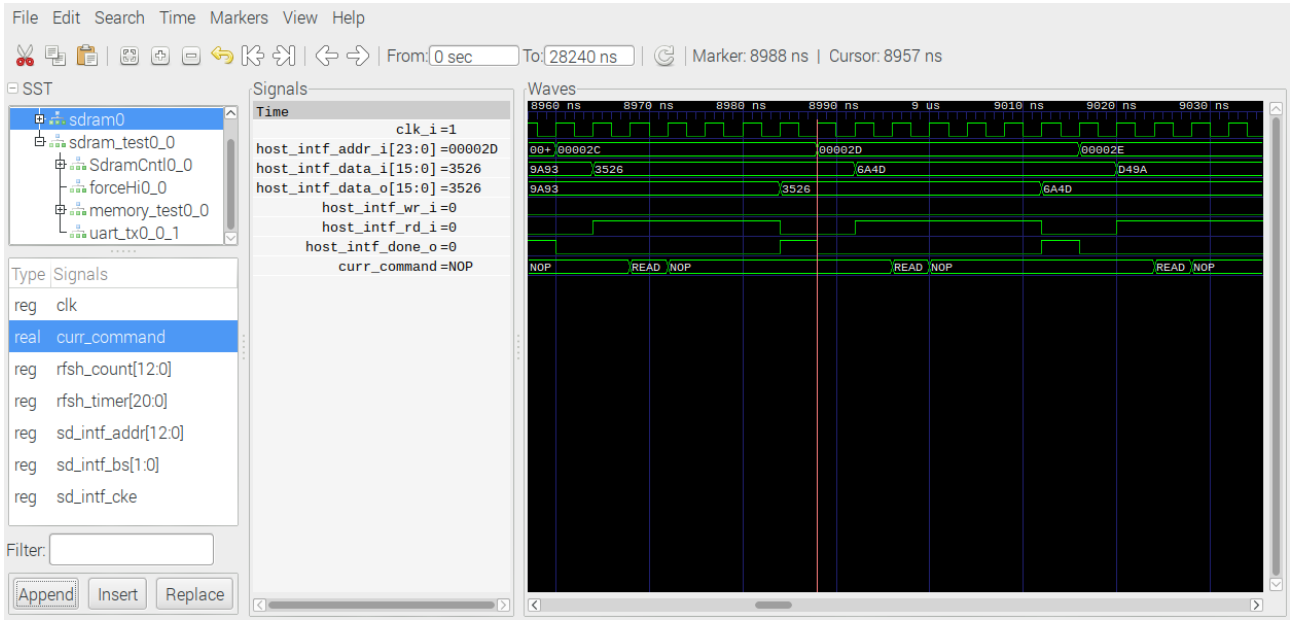
Write function

The 24 bit SdramCntl0_host_intf_addr_i is set on the raising edge of clk. One clk later the 16 bit SdramCntl0_host_intf_data_i and SdramCntl0_host_intf_wr_i goes hi. A clk later the SdramCntl0_host_intf_done_o goes hi and the SdramCntl0_host_intf_wr_i goes lo.

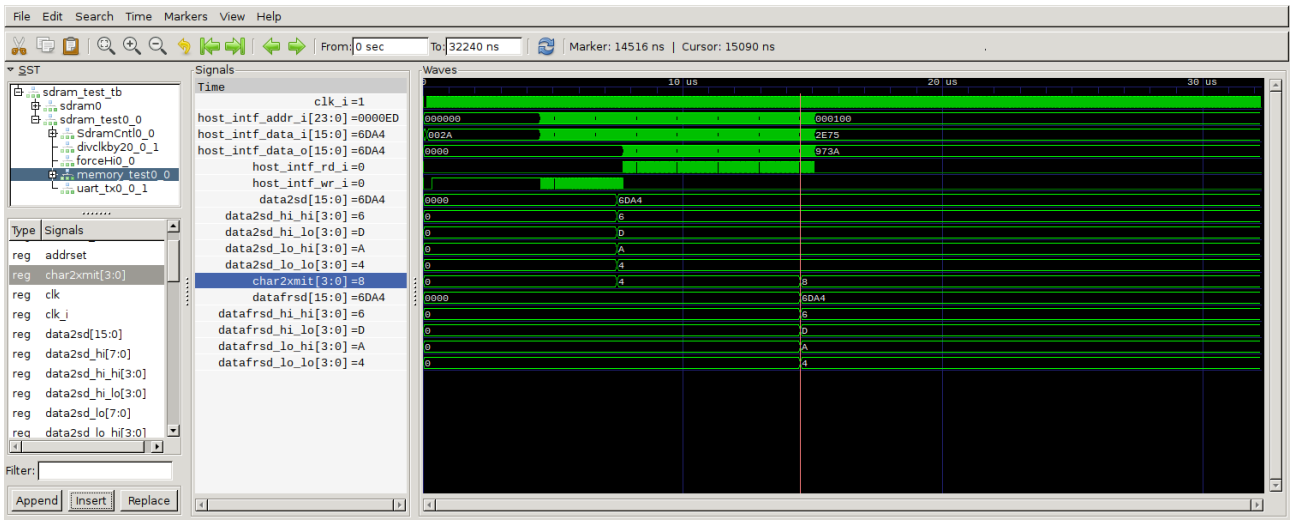


Read function

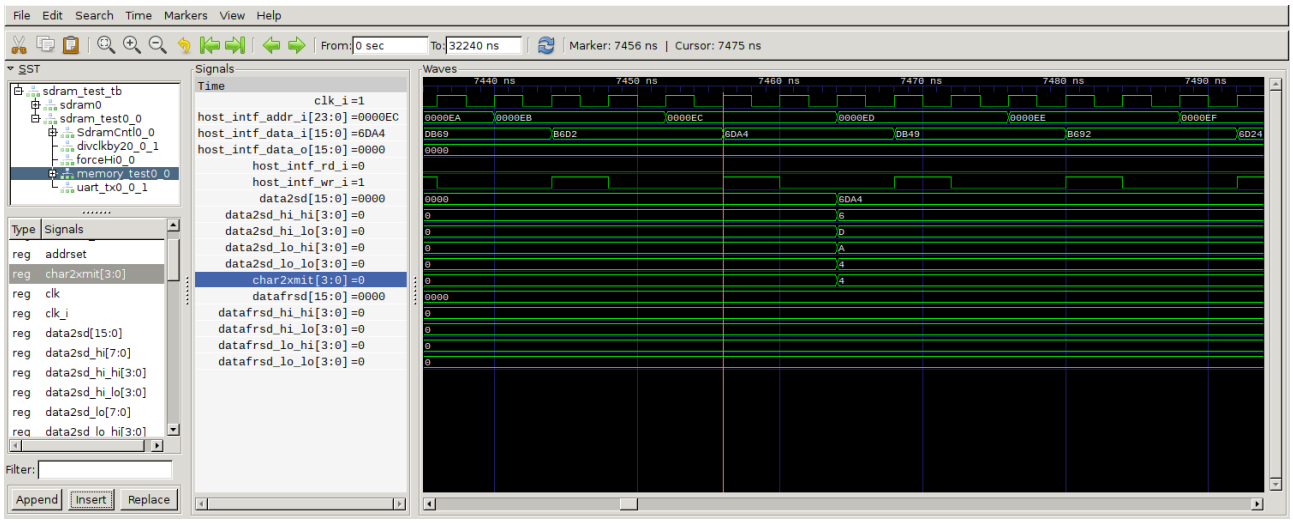
The 24 bit SdramCntl0_host_intf_addr_i is set on the raising edge of clk. One clk later the 16 bit SdramCntl0_host_intf_data_i is set and SdramCntl0_host_intf_rd_i goes hi. Five clk later the SdramCntl0_host_intf_done_o goes hi and the SdramCntl0_host_intf_rd_i goes lo.
During the first part of the memory_test Write takes place.



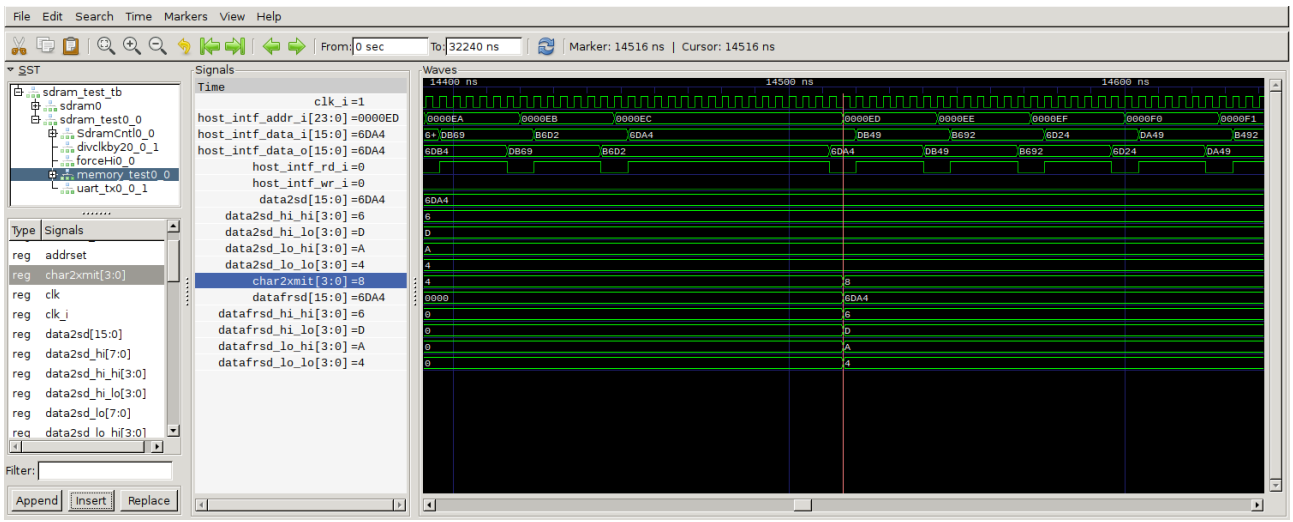
During the first part of the memory_test a write is performed WRRD_ADDRESS = 0x0000EB + 1.



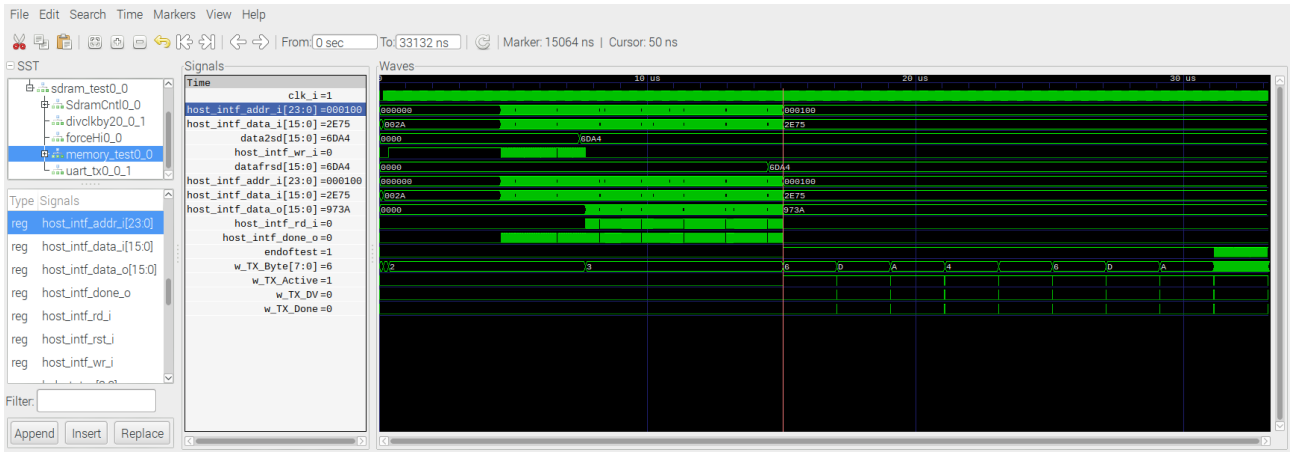
Write split



Read split.



The characters to transmit the write 0x6DA4 were converted to Ascii as were the read characters converted to Ascii



python sdram_test_uart.py
line 68 of sdram_test.v is modified reg [2:0] state_tx; → reg [2:0] state_tx=0;
make
sudo config_cat sdram_test.bin
sudo minicom -s

```
File  Edit  Tabs  Help
46DA4 6DA444444446DA4 6DA444444446DA4 6DA444444446DA4 6DA444444446DA4 6DA4444444
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```

2^24 16777216 0x000000 0xFFFFFF 16Bits

@PREFIX=sdram
@DEVID=SDRAM
@$LGMEMSZ=24
@LGMEMSZ.FORMAT=%d
@$NADDR=(1<<(@$THIS.LGMEMSZ-2))
@$NBYTES=(1<<(@$THIS.LGMEMSZ))
@NBYTES.FORMAT=0x%08x
@ACCESS=@$(DEVID)_ACCESS
@SLAVE.TYPE=MEMORY
@SLAVE.BUS=wb
@LD.PERM=wx