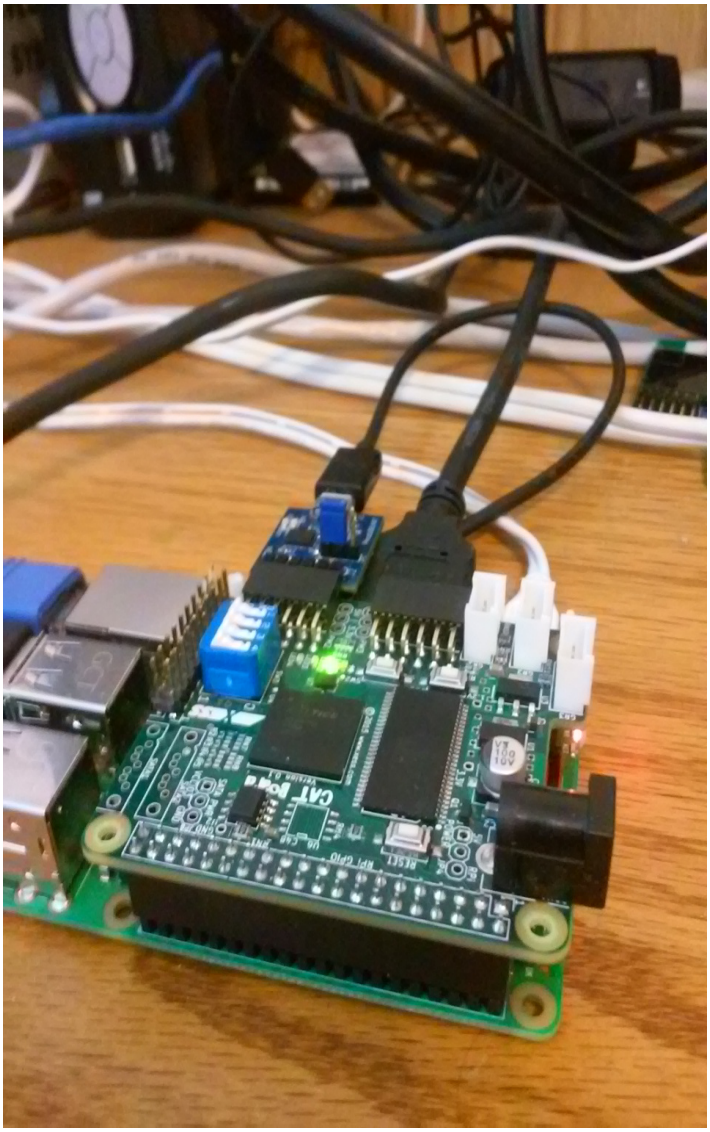
**********DRAFT**********
SDRAM
09/15/18
**********DRAFT**********

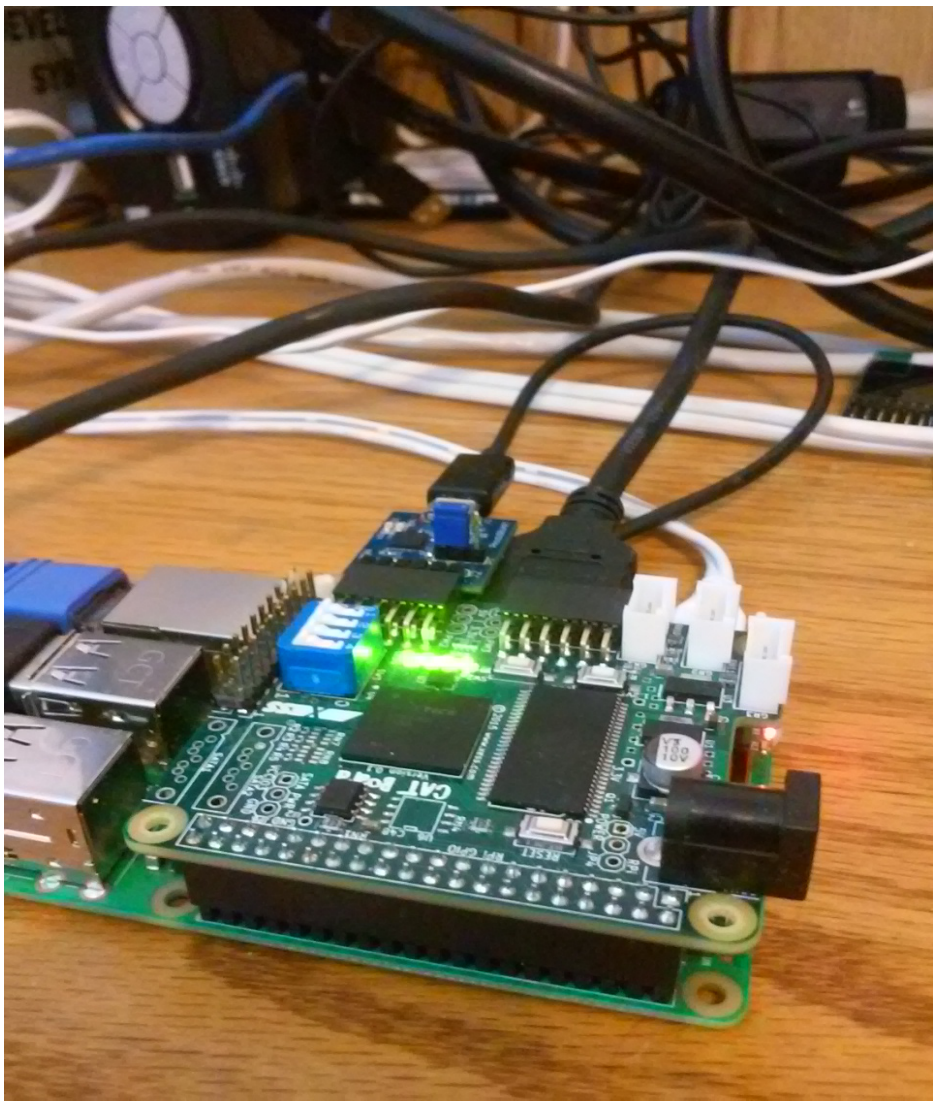
The memory_test takes approximately 3.5 sec or 175e6 clocks to complete at 50MHz. The memory_test writes to 16777215 locations and reads the data written.

Catboard running top.bin after the program has been load starting to write to memory during the memory_test



Catboard running top.bin after the program has been load starting to read from memory during the memory_test

Catboard running top.bin after the program has been load and the end memory memory_test. Note all 4 leds are on.



Now the sdram_test is memdev

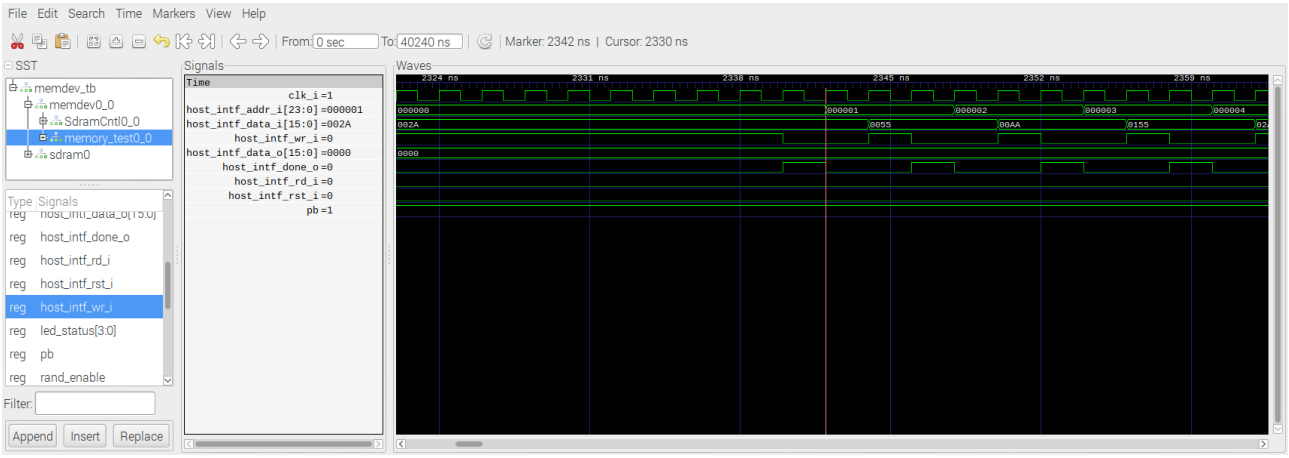
```
module top (
    clk100MHz,
    sdram_clk,
    sdram_return_clk,
    led_status,
    pb,
    memdev0_SdramCntl0_sd_intf_cke,
    memdev0_SdramCntl0_sd_intf_we,
    memdev0_SdramCntl0_sd_intf_addr,
    memdev0_SdramCntl0_sd_intf_dqml,
    memdev0_SdramCntl0_sd_intf_cas,
    memdev0_SdramCntl0_sd_intf_dqmh,
    memdev0_SdramCntl0_sd_intf_ras,
    memdev0_SdramCntl0_sd_intf_bs,
    memdev0_SdramCntl0_sd_intf_cs,
    memdev0_SdramCntl0_sd_intf_dq
);
=== top ===

   Number of wires:                441
```

```
   Number of wire bits:            968
   Number of public wires:          84
   Number of public wire bits:     537
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                719
     $_TBUF_                       16
     SB_CARRY                      68
     SB_DFF                         4
     SB_DFFE                        4
     SB_DFFER                      98
     SB_DFFES                       1
     SB_DFFESR                     45
     SB_DFFESS                      4
     SB_DFFR                       52
     SB_DFFS                        8
     SB_DFFSR                       3
     SB_DFFSS                       4
     SB_LUT4                      412
```

Host interface signals
wire [23:0] memdev0_SdramCntl0_host_intf_addr_i;
wire [15:0] memdev0_SdramCntl0_host_intf_data_i;
wire [15:0] memdev0_SdramCntl0_host_intf_data_i;
wire [15:0] memdev0_SdramCntl0_host_intf_data_o;
wire memdev0_SdramCntl0_host_intf_done_o;
wire memdev0_SdramCntl0_host_intf_wr_i;
wire memdev0_memory_test0_host_intf_rst_i;

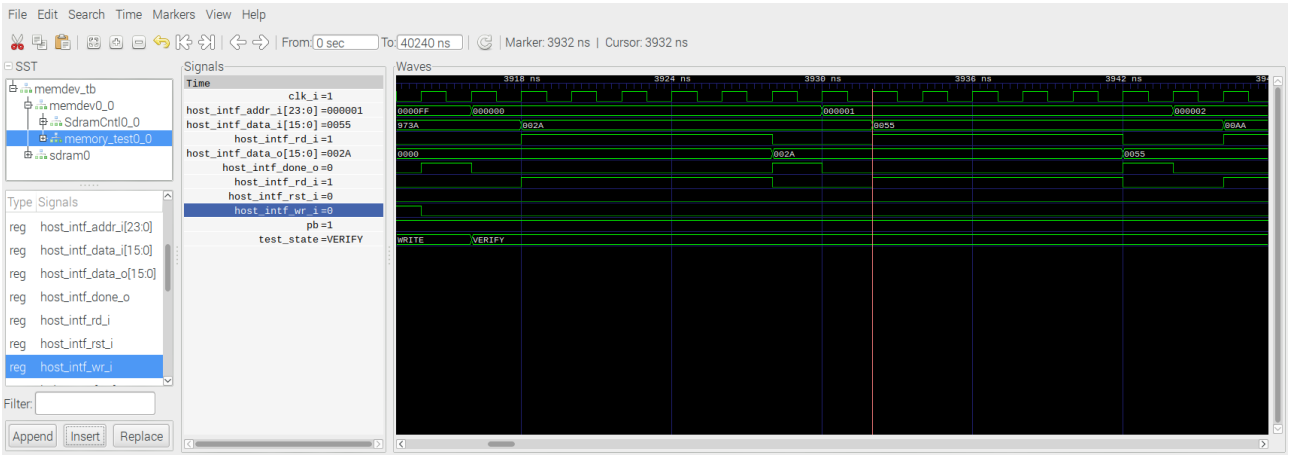
Write function
during a write
4 clks in between address chg
4 clks in between data chg
80 nsec

The 24 bit memdev0_SdramCntl0_host_intf_addr_i is set on the raising edge of clk. One clk later the 16 bit
memdev0_SdramCntl0_host_intf_data_i and memdev0_SdramCntl0_host_intf_wr_i goes hi. A clk later the memdev0_SdramCntl0_host_intf_done_o goes hi and the memdev0_SdramCntl0_host_intf_wr_i goes lo.



Read function

The 24 bit memdev0_SdramCntl0_host_intf_addr_i is set on the raising edge of clk. One clk later the 16 bit memdev0_SdramCntl0_host_intf_rd_i goes hi. Five clk later the memdev0_SdramCntl0_host_intf_done_o goes hi, memdev0_SdramCntl0_host_intf_data_o is valid and the memdev0_SdramCntl0_host_intf_rd_i goes lo.



During the first part of the memory_test Write takes place.

python memdev.py

make
sudo config_cat top.bin

2^24 16777216 0x000000 0xFFFFFF 16Bits
@PREFIX=sdram
@DEVID=SDRAM
@$LGMEMSZ=24
@LGMEMSZ.FORMAT=%d
@$NADDR=(1<<(@$THIS.LGMEMSZ-2))
@$NBYTES=(1<<(@$THIS.LGMEMSZ))
@NBYTES.FORMAT=0x%08x
@ACCESS=@$(DEVID)_ACCESS

@SLAVE.TYPE=MEMORY
@SLAVE.BUS=wb
@LD.PERM=wx