Sdram xulalx25soc

- ubuntu12.04$ xsload --usb 0 --fpga ~/testbuilds/learning_hdl/MyHDL/sdram/toplevel.bit
- MyHDL wishbone https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/sdramdev.py
- What is the xsload command to keep the program when power is restored

Sdram MyHDL

- MyHDL https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/memdev.py
- python memdev.py ;make top; sudo config_cat top.bin
- MyHDL https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/sdramdev.py

Sdram catzip xulalx25soc

- Autofpga project sdramdev.txt
- Catzip HX8K FPGA
- 50 MHz refresh_clk <= 10'd391
- wbsdram.v wishbone interface & sdramcontroller
- Verilator simulation arm-main_tb compiled with sdramsim.cpp & sdramsim.h
- Wishbone 32 bit addr & 32 bit data
- 0x2000000 to 0x2FFFFFF
- Write ./arm-wbregs 0x2000004 0x55aaaa55
- toplevel.v
  - main.v
    - Wbsdram.v

- Non Autofpga project maybe soon
- Xulalx25soc LX25 or LX9 FPGA
- 80 MHz refresh_clk <= 10'd625;
- wbsdram.v wishbone interface & sdramcontroller
- Verilator simulation busmaster_tb compiled with sdramsim.cpp & sdramsim.h
- Wishbone 32 bit addr & 32 bit data
- 0x2000000 to 0x2FFFFFF
- Write ./wbregs 0x2000004 0x55aaaa55
- Read ./wbregs 0x2000004
- toplevel.v
  - busmaster,v
    - Wbsdram.v

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- ubuntu12.04$ xsload --usb 0 --fpga ~/testbuilds/learning_hdl/MyHDL/sdram/toplevel.bit

- xula2-lx9 toplevel.bit https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/toplevel.bit
- lse build https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/wbsdram_ise_win8.pdf