Debugging Abort Issue
10/14/18

The simulation pc-main_tb Aborts when 9th

short SDRAMSIM::operator()(int clk, int cke, int cs_n, int ras_n, int cas_n, int we_n, int bs, unsigned addr, int driv, short data, short dqm)

parameter is sets to m_core→i_ram_data.
In the xulalx25soc the 9th parameter is set m_core→o_ram_drive_data.
The following is in toplevel of xulalx25soc design.

```
assign io_ram_data = (ram_drive_data) ? ram_data : 16'bzzzz_zzzz_zzzz_zzzz;
reg    [15:0]  r_ram_data_ext_clk;
// always @(posedge intermediate_clk_n)
always @(posedge clk_s)
        r_ram_data_ext_clk <= io_ram_data;
always @(posedge clk_s)
        r_ram_data <= r_ram_data_ext_clk;
```

When setting the 9th parameter to 21930 0x55aa the simulation does not Abort.
Setting the 9th parameter to o_ram_drive_data the simulation does not compile.

```
 @SIM.TICK=
#ifdef  @$(ACCESS)

m_core->i_ram_data = (*m_@$(MEM.NAME))(1,m_core->o_ram_cke,
m_core->o_ram_cs_n,m_core->o_ram_ras_n,m_core->o_ram_cas_n,
m_core->o_ram_we_n,m_core->o_ram_bs,m_core->o_ram_addr,
//m_core->o_ram_drive_data,m_core->o_ram_data,m_core->o_ram_dqm);
//21930,m_core->o_ram_data,m_core->o_ram_dqm);
m_core->i_ram_data,m_core->o_ram_data,m_core->o_ram_dqm);
#endif // @$(ACCESS)
```

```
./pc-wbregs 0x1000004 0x55aa
01000004 (        )-> 000055aa
```

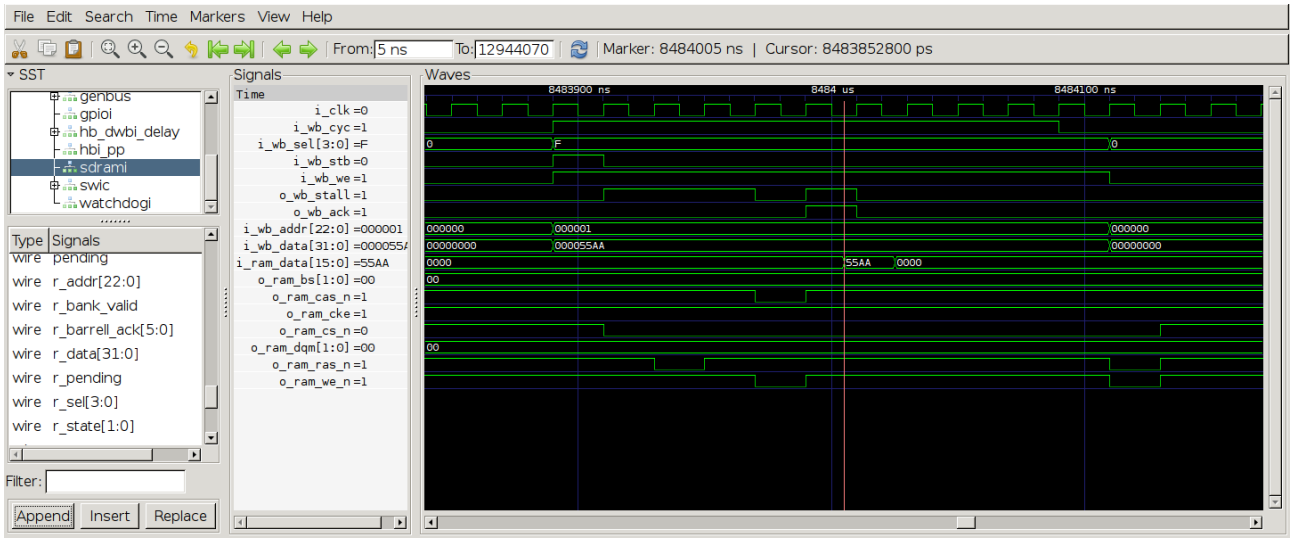
```
./pc-main_tb
Listening on port 8363
Listening on port 8364
Successful settup!  SDRAM switching to operational
Accepted CMD connection
POLL = 1
RCVD: 14 bytes
< A1000005W55aa
R/W Op
SDRAM[00000002] <= 0000
pc-main_tb: sdramsim.cpp:187: short int SDRAMSIM::operator()(int, int, int, int, int, int, int,
unsigned int, int, short int, short int): Assertion `driv' failed.
Aborted (core dumped)
```

From toplevel.v xulalx25soc

```
assign io_ram_data = (ram_drive_data) ? ram_data : 16'bzzzz_zzzz_zzzz_zzzz;
        reg    [15:0]  r_ram_data_ext_clk;
        // always @(posedge intermediate_clk_n)
```

```
        always @(posedge clk_s)
                r_ram_data_ext_clk <= io_ram_data;
        always @(posedge clk_s)
                r_ram_data <= r_ram_data_ext_clk;

m_core->i_ram_data = m_sdram(1,
                        m_core->o_ram_cke, m_core->o_ram_cs_n,
                        m_core->o_ram_ras_n, m_core->o_ram_cas_n,
                        m_core->o_ram_we_n, m_core->o_ram_bs,
                        m_core->o_ram_addr, m_core->o_ram_drive_data,
                        m_core->o_ram_data, m_core->o_ram_dqm);
0x55AA 21930

@SIM.TICK=
#ifdef  @$(ACCESS)

m_core->i_ram_data = (*m_@$(MEM.NAME))(1,m_core->o_ram_cke,
m_core->o_ram_cs_n,m_core->o_ram_ras_n,m_core->o_ram_cas_n,
m_core->o_ram_we_n,m_core->o_ram_bs,m_core->o_ram_addr,
21930,m_core->o_ram_data,m_core->o_ram_dqm);
//m_core->i_ram_data,m_core->o_ram_data,m_core->o_ram_dqm);
#endif // @$(ACCESS)


./pc-wbregs 0x1000004 0x55aa
01000004 (        )-> 000055aa

./pc-main_tb
Listening on port 8363
Listening on port 8364
Successful settup!  SDRAM switching to operational
Accepted CMD connection
POLL = 1
RCVD: 14 bytes
< A1000005W55aa
R/W Op
SDRAM[00000002] <= 0000
SDRAM[00000002] <= 0000
SDRAM[00000003] <= 55aa
> A01000005K00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A1000005R
R/W Op
SDRAM.Q[ 7] 55aa <= SDRAM[00000003]
> A01000005R00000000
POLL = 1
RCVD: 0 bytes
```

< [CLOSED]
^C


File Edit Search Time Markers View Help
From: 5 ns
To: 12944070
Marker: 8484005 ns | Cursor: 8483852800 ps
SST
genbus
gpioi
hb_dwbi_delay
hbi_pp
sdrami
swic
watchdogi
Type Signals
wire pending
wire r_addr[22:0]
wire r_bank_valid
wire r_barrell_ack[5:0]
wire r_data[31:0]
wire r_pending
wire r_sel[3:0]
wire r_state[1:0]
Filter:
Append
Insert
Replace
Signals
Time
i_clk =0
i_wb_cyc =1
i_wb_sel[3:0] =F
i_wb_stb =0
i_wb_we =1
o_wb_stall =1
o_wb_ack =1
i_wb_addr[22:0] =000001
i_wb_data[31:0] =000055A
i_ram_data[15:0] =55AA
o_ram_bs[1:0] =00
o_ram_cas_n =1
o_ram_cke =1
o_ram_cs_n =0
o_ram_dqm[1:0] =00
o_ram_ras_n =1
o_ram_we_n =1
Waves
8483900 ns
8484 us
8484100 ns
0
F
0
000000
000001
000000
00000000
000055AA
00000000
0000
55AA
0000
00
00