

```
ppio #(.W(16))
    sdramioi(o_ram_we_n, io_ram_data, o_ram_data, i_ram_data);
module ppio(i_dir, io_data, i_data, o_data);
    parameter W=8;
                     i dir:
    input
    inout [(W-1):0]io_data;
    input [(W-1):0]i_data;
    output [(W-1):0] o data;
    genvar k;
    generate
    for(k=0; k<W; k=k+1)
        SB_IO #(.PULLUP(1'b0),
            .PIN TYPE(6'b101001))
            theio(
                 .OUTPUT ENABLE(!i dir),
                 .PACKAGE_PIN(io_data[k]),
                 .D OUT 0(i data[k]),
                .D IN 0( o data[k])
    endgenerate
endmodule
```

Write 0x2000000 0x55AAAA55 Address 0x0000 o\_ram\_data 0x55AA o\_ram\_we\_n & o\_ram\_cas\_n & o\_ram\_dmod catzip

Lower 16 bits get written to File Edit Search Time Markers View Help upper 16 bits hw To: 5924881 ps | G | Marker: 2393897 ps | Cursor: 2392563 ps ∃ SST Waves Signals ⊼ Time - 🚠 buspici i clk=1 i wb cvc=1 i\_wb\_sel[3:0]=F ⊕ i aenbus i wb stb=0 - 🚠 gpioi i\_wb\_we =1 o\_wb\_stall=0 o\_wb\_ack=0 - 🚠 hbi\_pp i\_wb\_addr[22:0]=000000 i wb data[31:0]=55AAAA55 55AAAA55 i\_ram\_data[15:0] =0000 55AA AA55 0000 ⊕ iii swic o\_ram\_data[15:0] =55AA AA55 55AA o ram addr[12:0] =0000 L ... watchdogi o ram we n=0 last ram data[15:0] =0000 55AA AA55 0000 Type Signals o\_ram\_bs[1:0] =00 wire r\_addr[22:0] o\_ram\_cas\_n =0 wire r\_bank\_valid o ram cke=1 o\_ram\_cs\_n =0 wire r\_barrell\_ack[5:0] o ram dmod =1 o ram dgm[1:0]=00 wire r data[31:0] o\_ram\_ras\_n =1 wire r\_pending refresh\_clk[9:0] =109 11F | 11E | 11D | 11C | 11B | 11A | 119 | 118 | 117 | 116 | 115 | 114 | 113 | 112 | 111 | 110 | 10F | 10E | 10D | 10C | 10B | 10A | 109 | 108 | 107 | 106 | 105 | 104 | 103 | 102 | 101 | 100 | 0FF | 0FE | 106 wire r\_sel[3:0] wire r\_we wire ram\_data[15:0] wire refresh\_cmd wire startup\_hold wire startup\_idle[15:0] wire trigger wire unused[2:0] Filter: Append Insert Replace

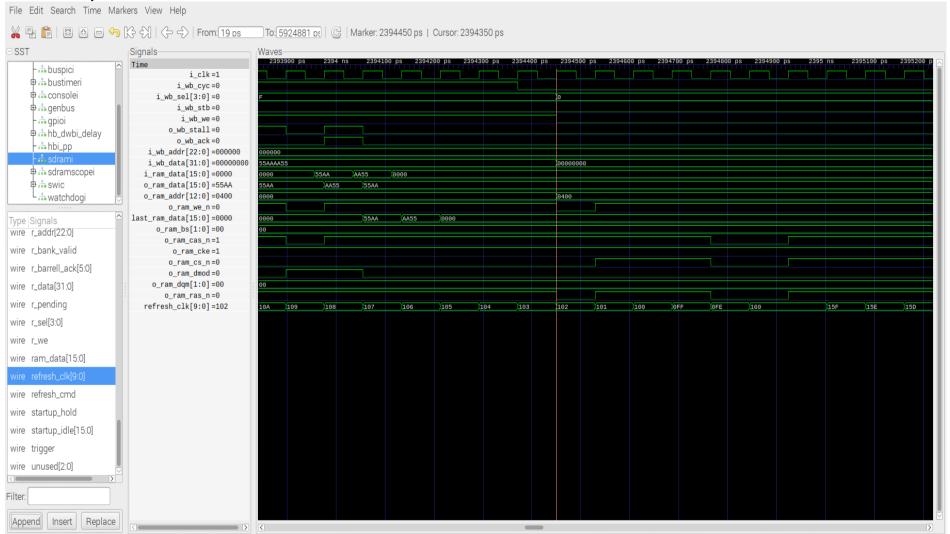
Frror in simulation no lower

o ram data should be 0xaa55

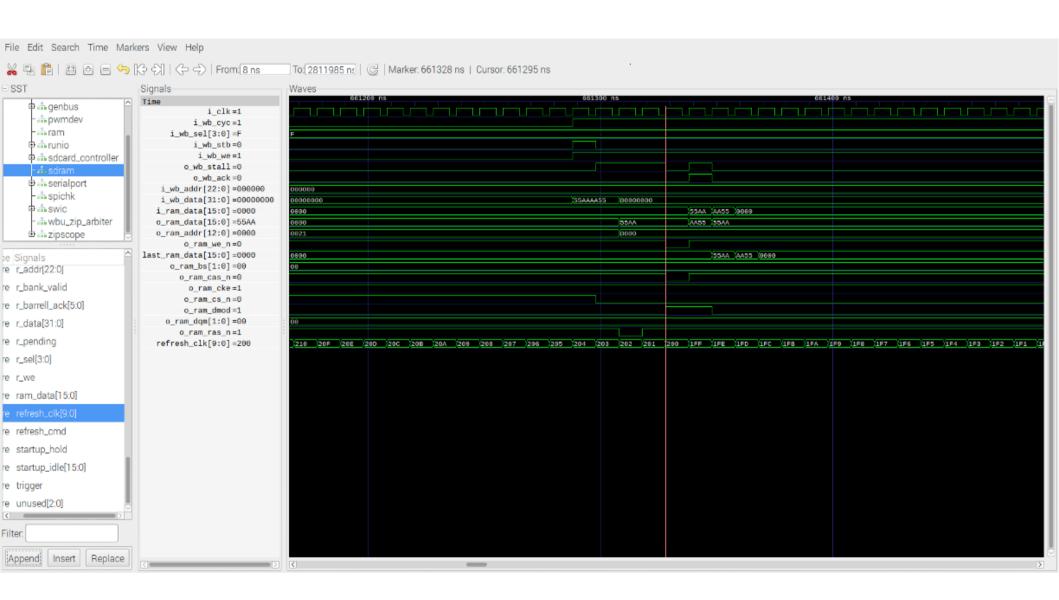
16 bits & hw

Write 0x2000000 0x55AAAA55 Address 0x0400 o\_ram\_data 0x55AA o\_ram\_we\_n & o\_ram\_ras\_n catzip

Error in simulation no lower 16 bits & hw o\_ram\_data should be 0xaa55
Lower 16 bits get written to upper 16 bits hw



## Write 0x2000000 0x55AAAA55 Address 0x0000 o\_ram\_data 0x55AA o\_ram\_we\_n & o\_ram\_cas\_n & o\_ram\_dmod xulalx25soc



Write 0x2000000 0x55AAAA55
Address 0x0400 o\_ram\_data 0x55AA
o\_ram\_we\_n & o\_ram\_ras\_n
xulalx25soc

Error in simulation hw okay xulalx25soc Should be o\_ram\_data 0xaa55

