Debugging Abort Issue
10/15/18

The simulation pc-main_tb Aborts when 9th

short SDRAMSIM::operator()(int clk, int cke, int cs_n, int ras_n, int cas_n, int we_n, int bs, unsigned addr, int driv, short data, short dqm)

parameter is sets to m_core→i_ram_data.

In the xulalx25soc the 9th parameter is set m_core→o_ram_drive_data.

The following is in toplevel of xulalx25soc design.

```
assign io_ram_data = (ram_drive_data) ? ram_data : 16'bzzzz_zzzz_zzzz_zzzz;
reg    [15:0]  r_ram_data_ext_clk;
// always @(posedge intermediate_clk_n)
always @(posedge clk_s)
        r_ram_data_ext_clk <= io_ram_data;
always @(posedge clk_s)
        r_ram_data <= r_ram_data_ext_clk;
```

When setting the 9th parameter to 21930 0x55aa the simulation does not Abort.

Setting the 9th parameter to o_ram_drive_data the simulation does not compile.

Adding io_ram_data to

@MAIN.PORTLIST

```
i_wb_cyc, i_wb_stb, i_wb_we, i_wb_addr, i_wb_data, i_wb_sel,
                o_wb_ack, o_wb_stall, o_wb_data,
        o_ram_cs_n, o_ram_cke, o_ram_ras_n, o_ram_cas_n, o_ram_we_n,
                o_ram_bs, o_ram_addr,
                o_ram_dmod, i_ram_data, o_ram_data, o_ram_dqm,
        o_debug, io_ram_data
```

and adding @MAIN.IODECL=

```
inout   wire    [15:0]  io_ram_data;
```

Now the simulation compiles.

@SIM.TICK=

```
#ifdef  @$(ACCESS)
        m_core->i_ram_data = (*m_@$(MEM.NAME))(1,m_core->o_ram_cke,
        m_core->o_ram_cs_n,m_core->o_ram_ras_n,m_core->o_ram_cas_n,
        m_core->o_ram_we_n,m_core->o_ram_bs,m_core->o_ram_addr,
        //m_core->o_ram_drive_data,m_core->o_ram_data,m_core->o_ram_dqm);
        //21930,m_core->o_ram_data,m_core->o_ram_dqm);
        m_core->io_ram_data,m_core->o_ram_data,m_core->o_ram_dqm);
#endif // @$(ACCESS)
```

```
./pc-wbregs 0x1000004 0x55aa
01000004 (        )-> 000055aa
```

```
./pc-main_tb
Listening on port 8363
Listening on port 8364
Successful settup!  SDRAM switching to operational
Accepted CMD connection
POLL = 1
RCVD: 14 bytes
< A1000005W55aa
R/W Op
```

SDRAM[00000002] <= 0000
pc-main_tb: sdramsim.cpp:187: short int SDRAMSIM::operator()(int, int, int, int, int, int, int, unsigned int, int, short int, short int): Assertion `driv' failed.
Aborted (core dumped)

From toplevel.v xulalx25soc

```
assign io_ram_data = (ram_drive_data) ? ram_data : 16'bzzzz_zzzz_zzzz_zzzz;
        reg     [15:0]  r_ram_data_ext_clk;
        // always @(posedge intermediate_clk_n)
        always @(posedge clk_s)
                r_ram_data_ext_clk <= io_ram_data;
        always @(posedge clk_s)
                r_ram_data <= r_ram_data_ext_clk;

m_core->i_ram_data = m_sdram(1,
                        m_core->o_ram_cke, m_core->o_ram_cs_n,
                        m_core->o_ram_ras_n, m_core->o_ram_cas_n,
                        m_core->o_ram_we_n, m_core->o_ram_bs,
                        m_core->o_ram_addr, m_core->o_ram_drive_data,
                        m_core->o_ram_data, m_core->o_ram_dqm);
```

0x55AA 21930

```
@SIM.TICK=
#ifdef  @$(ACCESS)

m_core->i_ram_data = (*m_@$(MEM.NAME))(1,m_core->o_ram_cke,
m_core->o_ram_cs_n,m_core->o_ram_ras_n,m_core->o_ram_cas_n,
m_core->o_ram_we_n,m_core->o_ram_bs,m_core->o_ram_addr,
21930,m_core->o_ram_data,m_core->o_ram_dqm);
//m_core->i_ram_data,m_core->o_ram_data,m_core->o_ram_dqm);
#endif // @$(ACCESS)
```

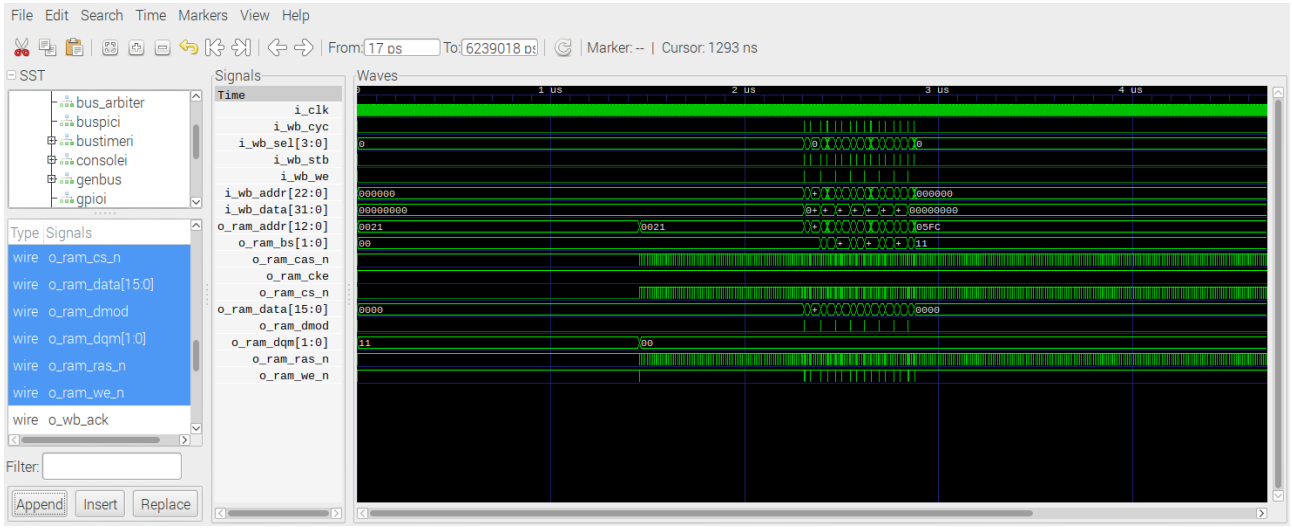
```
pi@mypi3-1:~/testbuilds/catzip_simulation/catzip/sw/host $ ./ttt.sh
01000004 (        )-> 55aaaa55
01000004 (        ) : [....] 00000000
010ffff8 (        )-> 55aaaa55
010ffff8 (        ) : [....] 00000000
01800004 (        )-> 55aaaa55
01800004 (        ) : [....] 00000000
018ffff8 (        )-> 55aaaa55
018ffff8 (        ) : [....] 00000000
01c00004 (        )-> 55aaaa55
01c00004 (        ) : [....] 00000000
01cffff8 (        )-> 55aaaa55
01cffff8 (        ) : [....] 00000000
01f00004 (        )-> 55aaaa55
01f00004 (        ) : [....] 00000000
01fffff8 (        )-> 55aaaa55
01fffff8 (        ) : [....] 00000000
```

```
pi@mypi3-1:~/testbuilds/catzip_simulation/catzip/sim/verilated $ ./arm-main_tb -d
Listening on port 8363
Listening on port 8364
Opening Bus-master with
        Debug Access port = 8363
        Serial Console    = 8364
        VCD File          = trace.vcd
Successful settup!  SDRAM switching to operational
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
< A1000005W55aaaa55
R/W Op
SDRAM[00000002] <= 55aa
SDRAM[00000003] <= aa55
> A01000005
> K00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A1000005R
R/W Op
SDRAM.Q[ 6] 55aa <= SDRAM[00000002]
SDRAM.Q[ 7] aa55 <= SDRAM[00000003]
> A01000005R00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
< A10ffff9W55aaaa55
R/W Op
SDRAM[0007fffc] <= 55aa
SDRAM[0007fffd] <= aa55
> A010ffff9
> K00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A10ffff9R
R/W Op
SDRAM.Q[14] 55aa <= SDRAM[0007fffc]
SDRAM.Q[15] aa55 <= SDRAM[0007fffd]
> A010ffff9R00000000
```

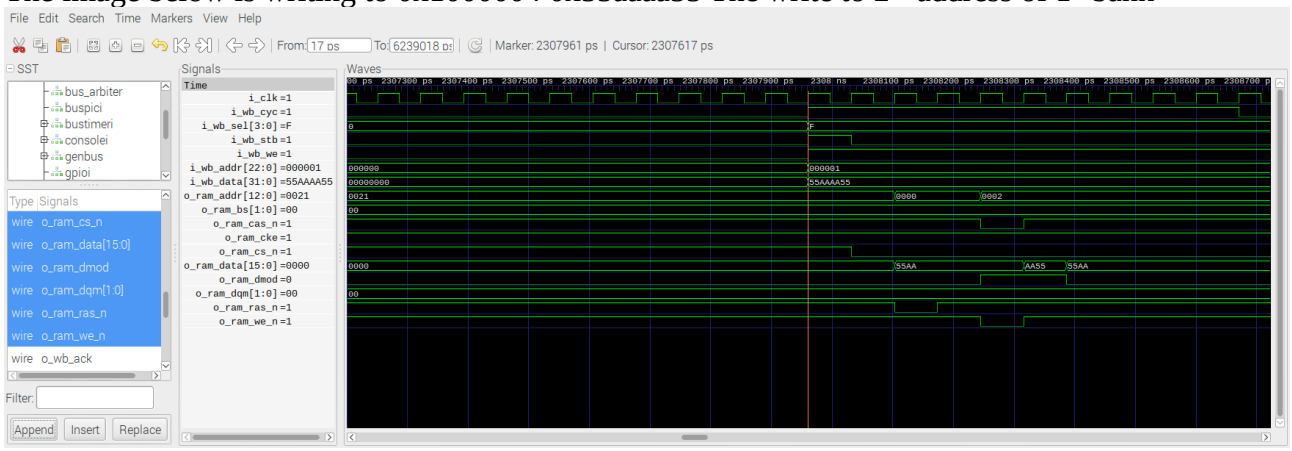
```
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
< A1800005W55aaaa55
R/W Op
SDRAM[00400002] <= 55aa
SDRAM[00400003] <= aa55
> A01800005
> K00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A1800005R
R/W Op
SDRAM.Q[ 6] 55aa <= SDRAM[00400002]
SDRAM.Q[ 7] aa55 <= SDRAM[00400003]
> A01800005R00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
< A18ffff9W55aaaa55
R/W Op
SDRAM[0047fffc] <= 55aa
SDRAM[0047fffd] <= aa55
> A018ffff9
> K00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A18ffff9R
R/W Op
SDRAM.Q[ 6] 55aa <= SDRAM[0047fffc]
SDRAM.Q[ 7] aa55 <= SDRAM[0047fffd]
> A018ffff9R00000000
POLL = 1
RCVD: 0 bytes
<  [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
```

< A1c00005W55aaaa55
R/W Op
SDRAM[00600002] <= 55aa
SDRAM[00600003] <= aa55
> A01c00005
> K00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A1c00005R
R/W Op
SDRAM.Q[6] 55aa <= SDRAM[00600002]
SDRAM.Q[7] aa55 <= SDRAM[00600003]
> A01c00005R00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
< A1cffff9W55aaaa55
R/W Op
SDRAM[0067fffc] <= 55aa
SDRAM[0067fffd] <= aa55
> A01cffff9
> K00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A1cffff9R
R/W Op
SDRAM.Q[6] 55aa <= SDRAM[0067fffc]
SDRAM.Q[7] aa55 <= SDRAM[0067fffd]
> A01cffff9R00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
< A1f00005W55aaaa55
R/W Op
SDRAM[00780002] <= 55aa
SDRAM[00780003] <= aa55
> A01f00005
> K00000000

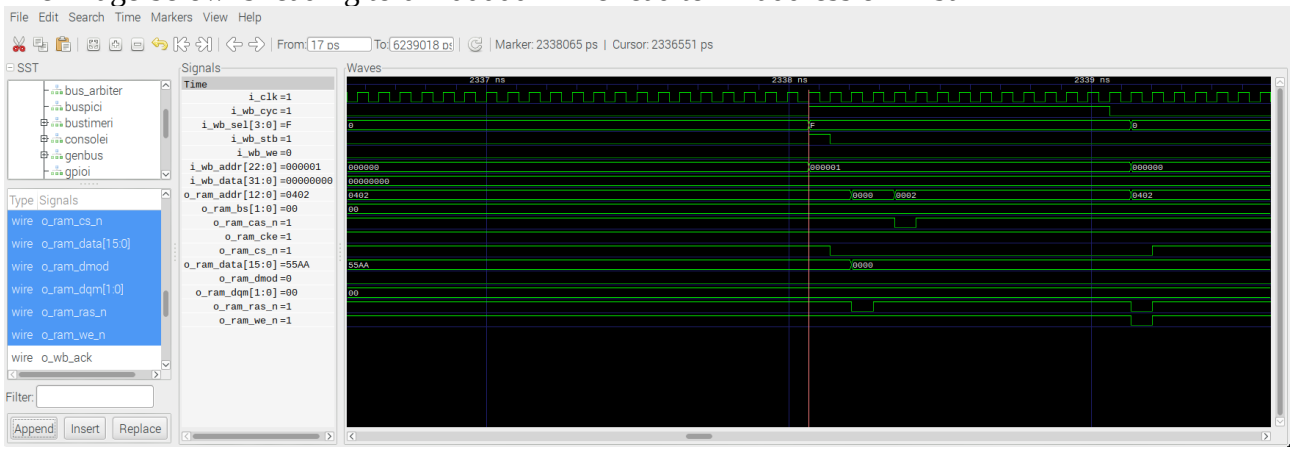
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A1f00005R
R/W Op
SDRAM.Q[14] 55aa <= SDRAM[00780002]
SDRAM.Q[15] aa55 <= SDRAM[00780003]
> A01f00005R00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 18 bytes
< A1fffff9W55aaaa55
R/W Op
SDRAM[007ffffc] <= 55aa
SDRAM[007ffffd] <= aa55
> A01fffff9
> K00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
Accepted CMD connection
POLL = 1
RCVD: 10 bytes
< A1fffff9R
R/W Op
SDRAM.Q[14] 55aa <= SDRAM[007ffffc]
SDRAM.Q[15] aa55 <= SDRAM[007ffffd]
> A01fffff9R00000000
POLL = 1
RCVD: 0 bytes
< [CLOSED]
^C
The image below is the 2 writes & 2 reads to each of the 4 banks



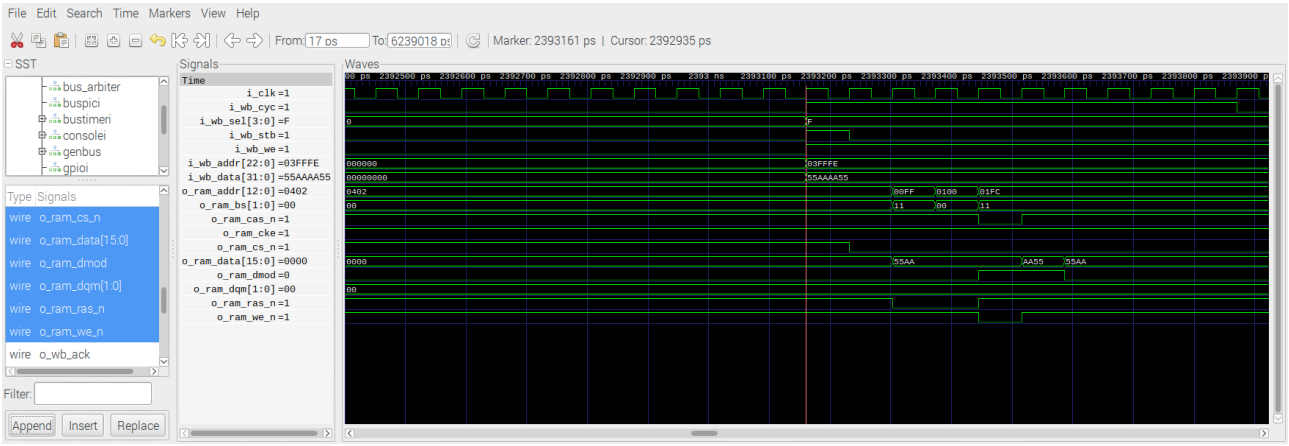
The image below is writing to 0x1000004 0x55aaaa55 The write to 2nd address of 1st bank



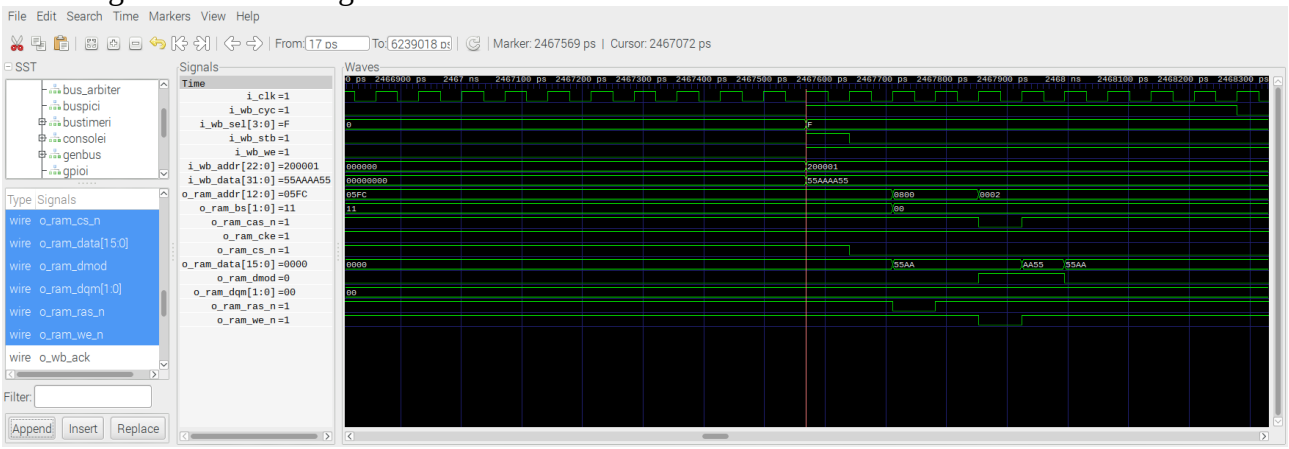
The image below is reading to 0x1000004 The read to 2nd address of 1st bank



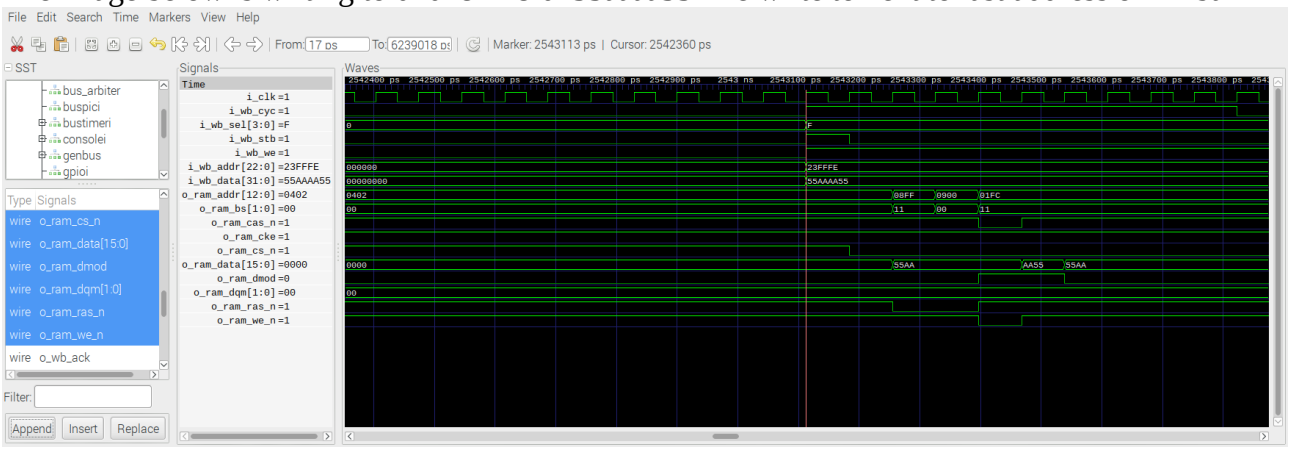
The image below is writing to 0x010ffff8 0x55aaaa55 The write to next to last address of 1st bank



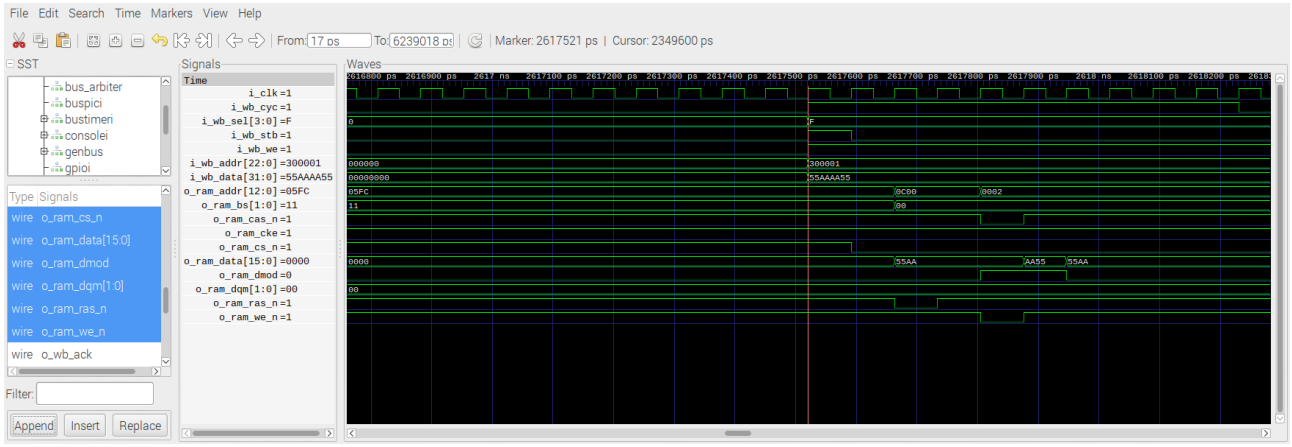
The image below is writing to 0x01800004 0x55aaaa55 The write to 2nd address of 2nd bank



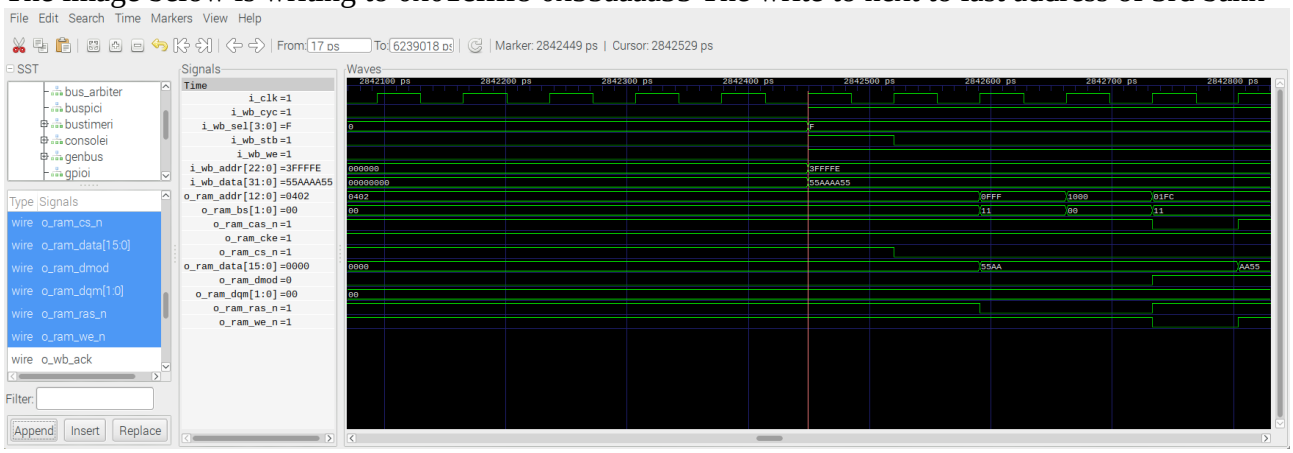
The image below is writing to 0x018ffff8 0x55aaaa55 The write to next to last address of 2nd bank



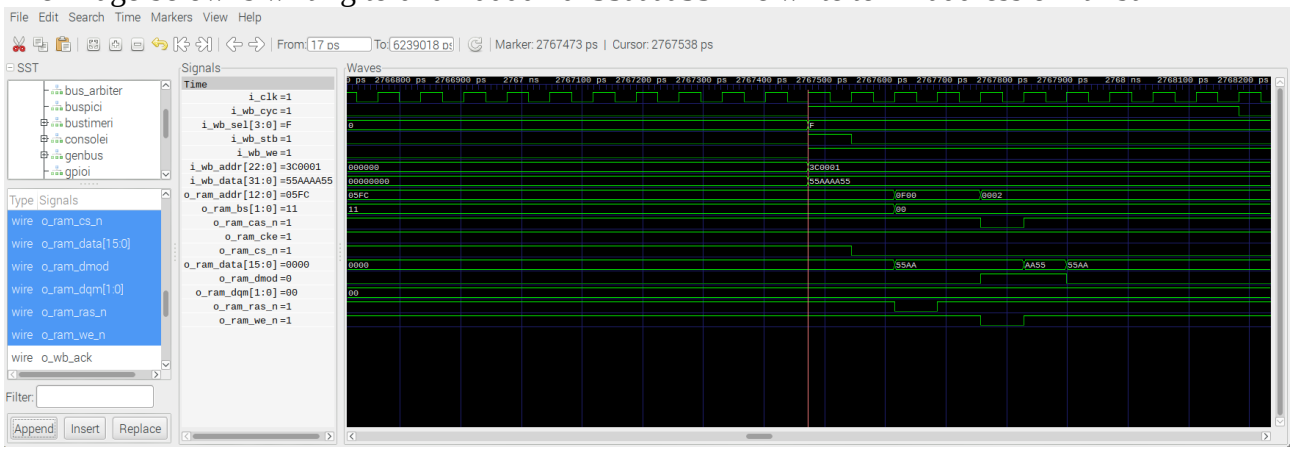
The image below is writing to 0x01c00004 0x55aaaa55 The write to 2nd address of 3rd bank



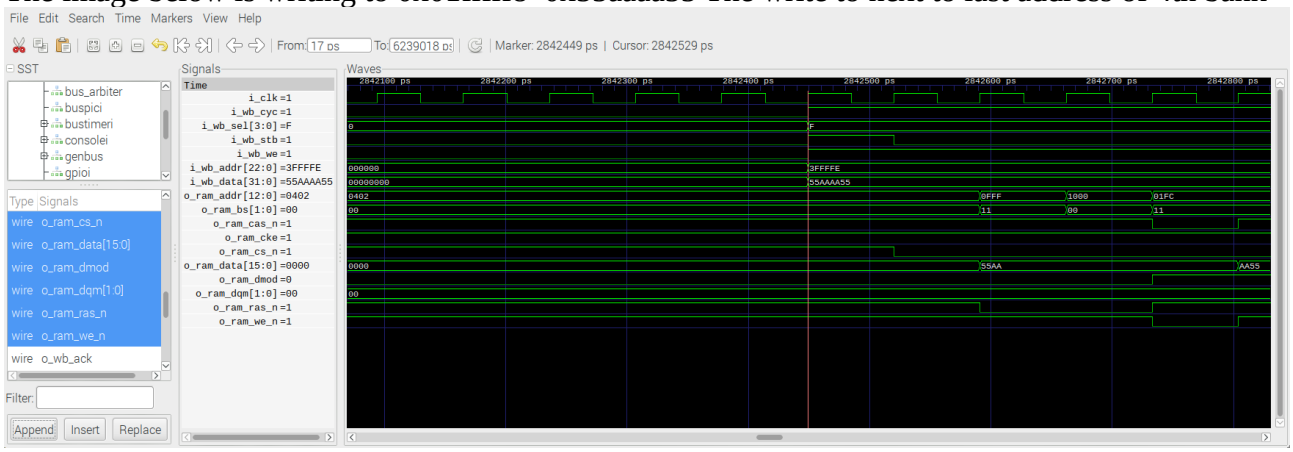
The image below is writing to 0x01cffff8 0x55aaaa55 The write to next to last address of 3rd bank



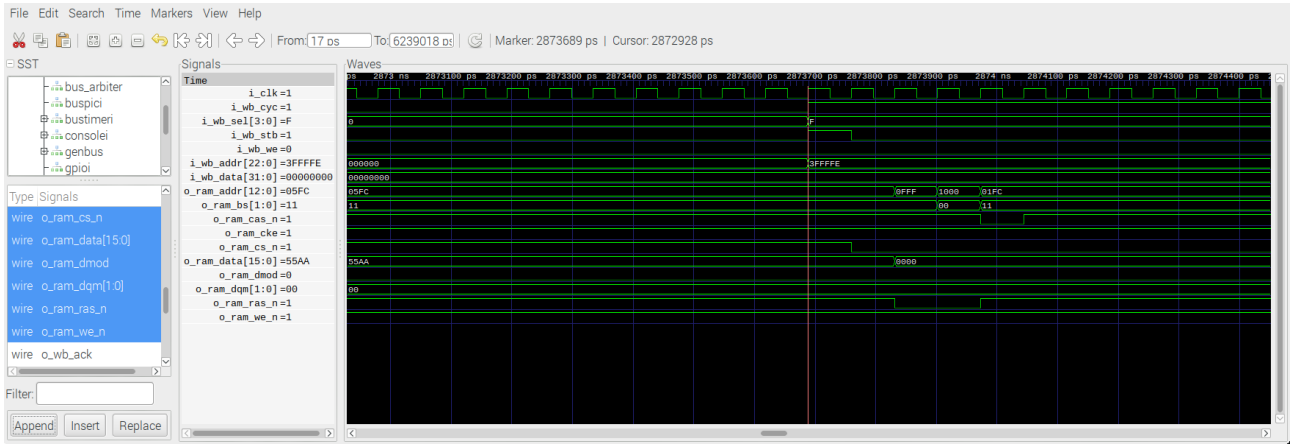
The image below is writing to 0x01f00004 0x55aaaa55 The write to 2nd address of 4th bank



The image below is writing to 0x01fffff8 0x55aaaa55 The write to next to last address of 4th bank



The image below is reading to 0x01fffff8 The read to next to last address of 4th bank


File Edit Search Time Markers View Help
From: 17 ps
To: 6239018 ps
Marker: 2873689 ps | Cursor: 2872928 ps
SST
bus_arbiter
buspici
bustimeri
consolei
genbus
gpioi
Type Signals
wire o_ram_cs_n
wire o_ram_data[15:0]
wire o_ram_dmod
wire o_ram_dqm[1:0]
wire o_ram_ras_n
wire o_ram_we_n
wire o_wb_ack
Filter:
Append
Insert
Replace
Signals
Time
i_clk =1
i_wb_cyc =1
i_wb_sel[3:0] =F
i_wb_stb =1
i_wb_we =0
i_wb_addr[22:0] =3FFFFE
i_wb_data[31:0] =00000000
o_ram_addr[12:0] =05FC
o_ram_bs[1:0] =11
o_ram_cas_n =1
o_ram_cke =1
o_ram_cs_n =1
o_ram_data[15:0] =55AA
o_ram_dmod =0
o_ram_dqm[1:0] =00
o_ram_ras_n =1
o_ram_we_n =1
Waves
2873 ns
2873100 ps
2873200 ps
2873300 ps
2873400 ps
2873500 ps
2873600 ps
2873700 ps
2873800 ps
2873900 ps
2874 ns
2874100 ps
2874200 ps
2874300 ps
2874400 ps
0
F
000000
3FFFFE
00000000
05FC
0FFF
1000
01FC
11
00
11
55AA
0000
00