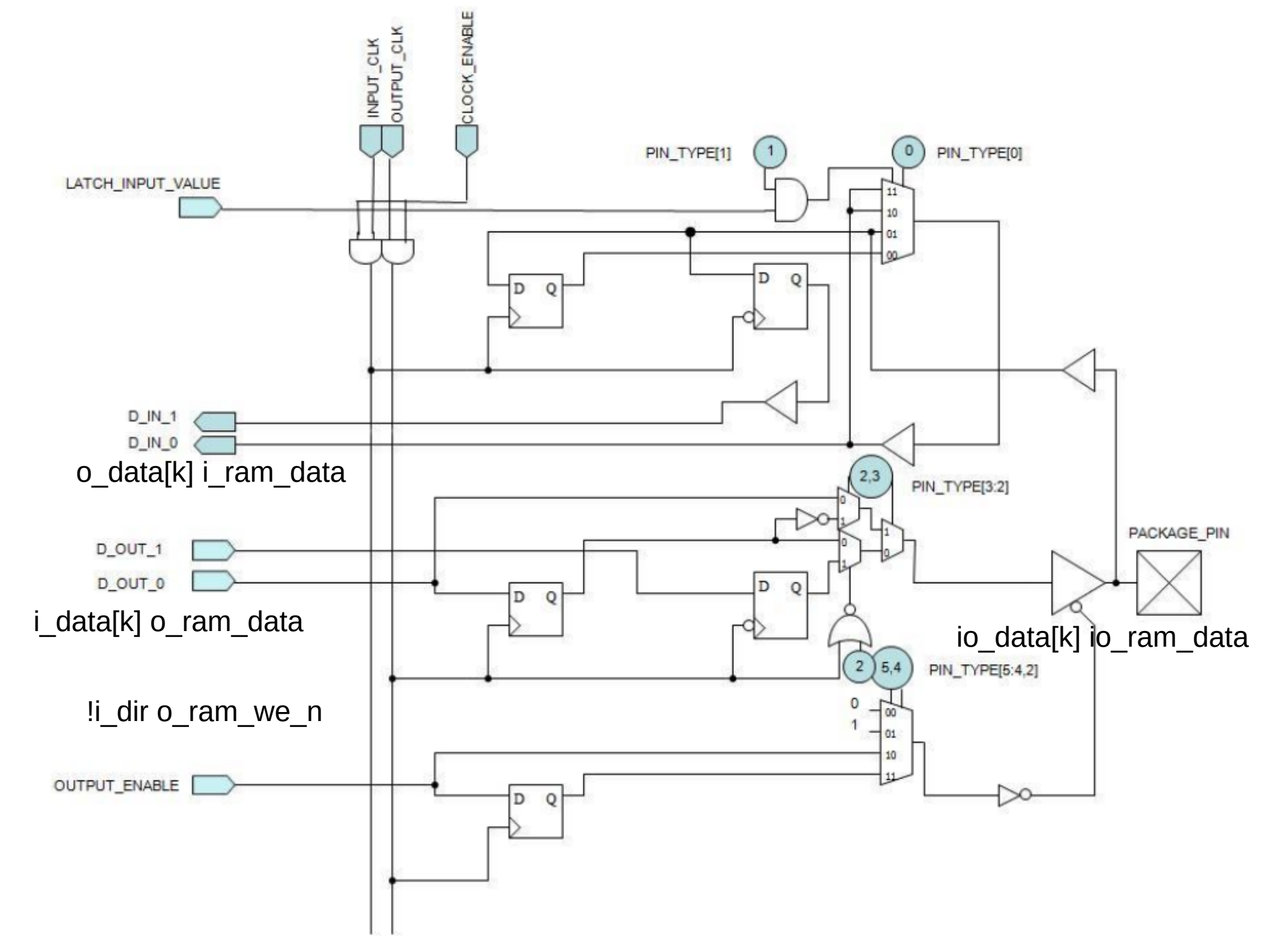

INPUT_CLK
OUTPUT_CLK
CLOCK_ENABLE
LATCH_INPUT_VALUE
PIN_TYPE[1]
1
0
PIN_TYPE[0]
11
10
01
00
D Q
D_IN_1
D_IN_0
o_data[k] i_ram_data
2,3
PIN_TYPE[3:2]
PACKAGE_PIN
D_OUT_1
D_OUT_0
i_data[k] o_ram_data
io_data[k] io_ram_data
2
5,4
PIN_TYPE[5:4,2]
!i_dir o_ram_we_n
OUTPUT_ENABLE

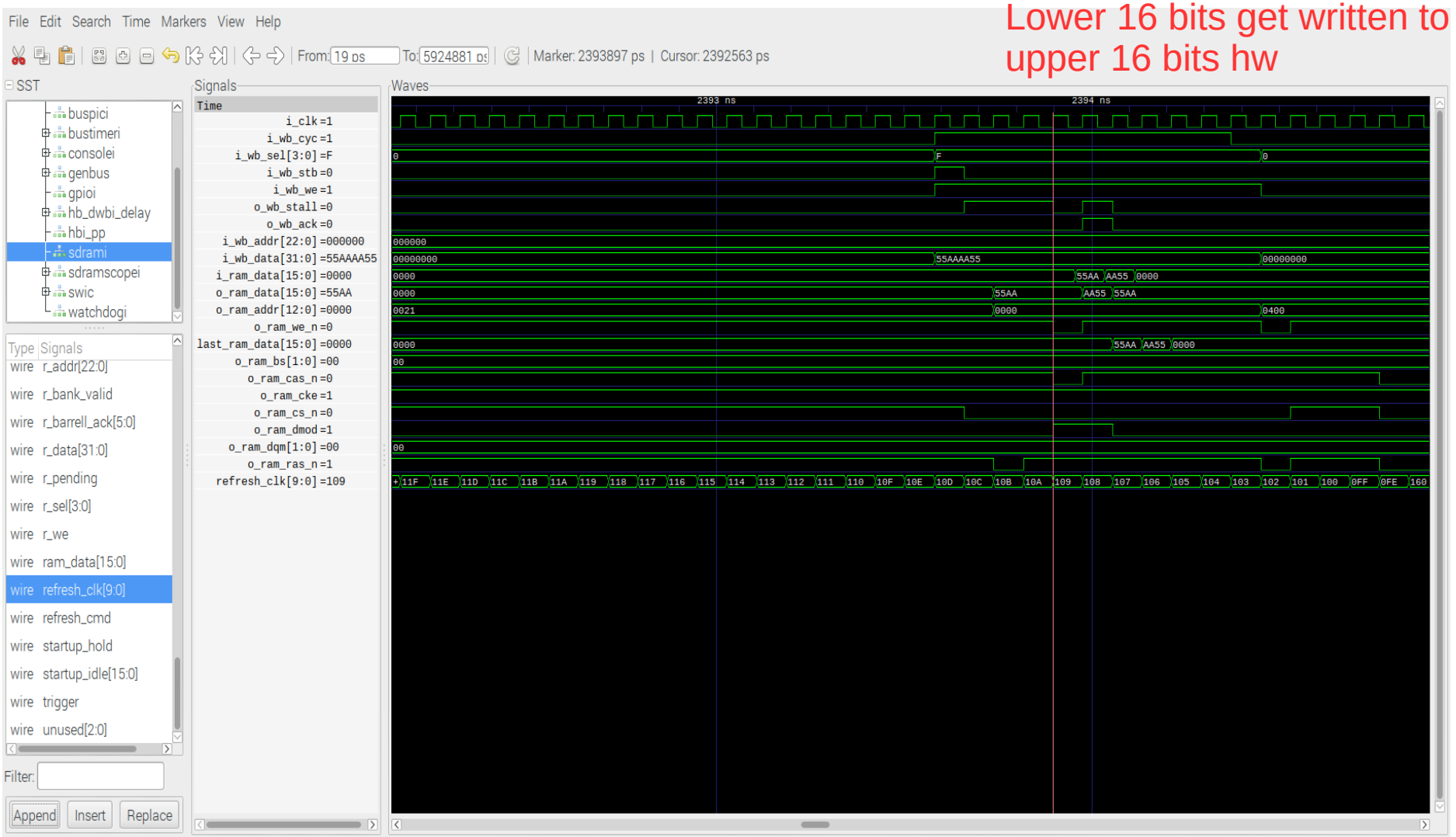
```
ppio #(.W(16))
      sdramioi(o_ram_we_n, io_ram_data, o_ram_data, i_ram_data);

module   ppio(i_dir, io_data, i_data, o_data);
      parameter     W=8;
      input                 i_dir;
      inout      [(W-1):0] io_data;
      input      [(W-1):0] i_data;
      output     [(W-1):0] o_data;

      genvar    k;
      generate
      for(k=0; k<W; k = k+1)
            SB_IO #(.PULLUP(1'b0),
                  .PIN_TYPE(6'b101001))
                  theio(
                        .OUTPUT_ENABLE(!i_dir),
                        .PACKAGE_PIN(io_data[k]),
                        .D_OUT_0(i_data[k]),
                        .D_IN_0( o_data[k])
                  );
      endgenerate

endmodule
```

Chg’ed catzip toplevl to be similar to xulalx25soc

```
assign io_ram_data = (ram_drive_data) ? o_ram_data : 16'bzzzz_zzzz_zzzz_zzzz;
reg  [15:0]     r_ram_data_ext_clk;
// always @(posedge intermediate_clk_n)
always @(posedge s_clk)
      r_ram_data_ext_clk <= io_ram_data;
always @(posedge s_clk)
      i_ram_data <= r_ram_data_ext_clk;
assign o_ram_clk = s_clk;
```

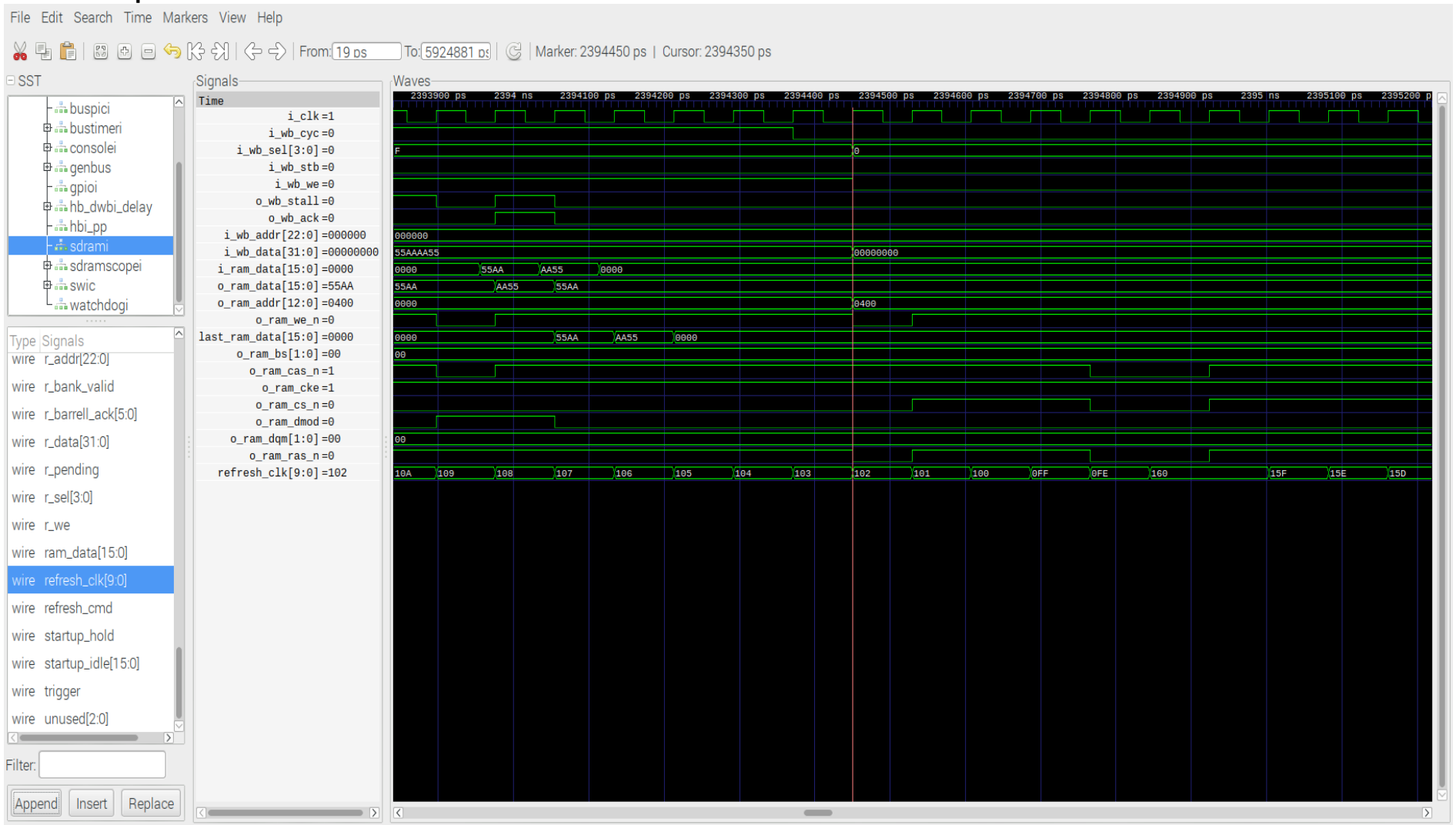
Write 0x2000000 0x55AAAA55
Address 0x0000 o_ram_data 0x55AA
o_ram_we_n & o_ram_cas_n & o_ram_dmod catzip

Error in simulation no lower 16 bits & hw
o_ram_data should be 0xaa55
Lower 16 bits get written to upper 16 bits hw



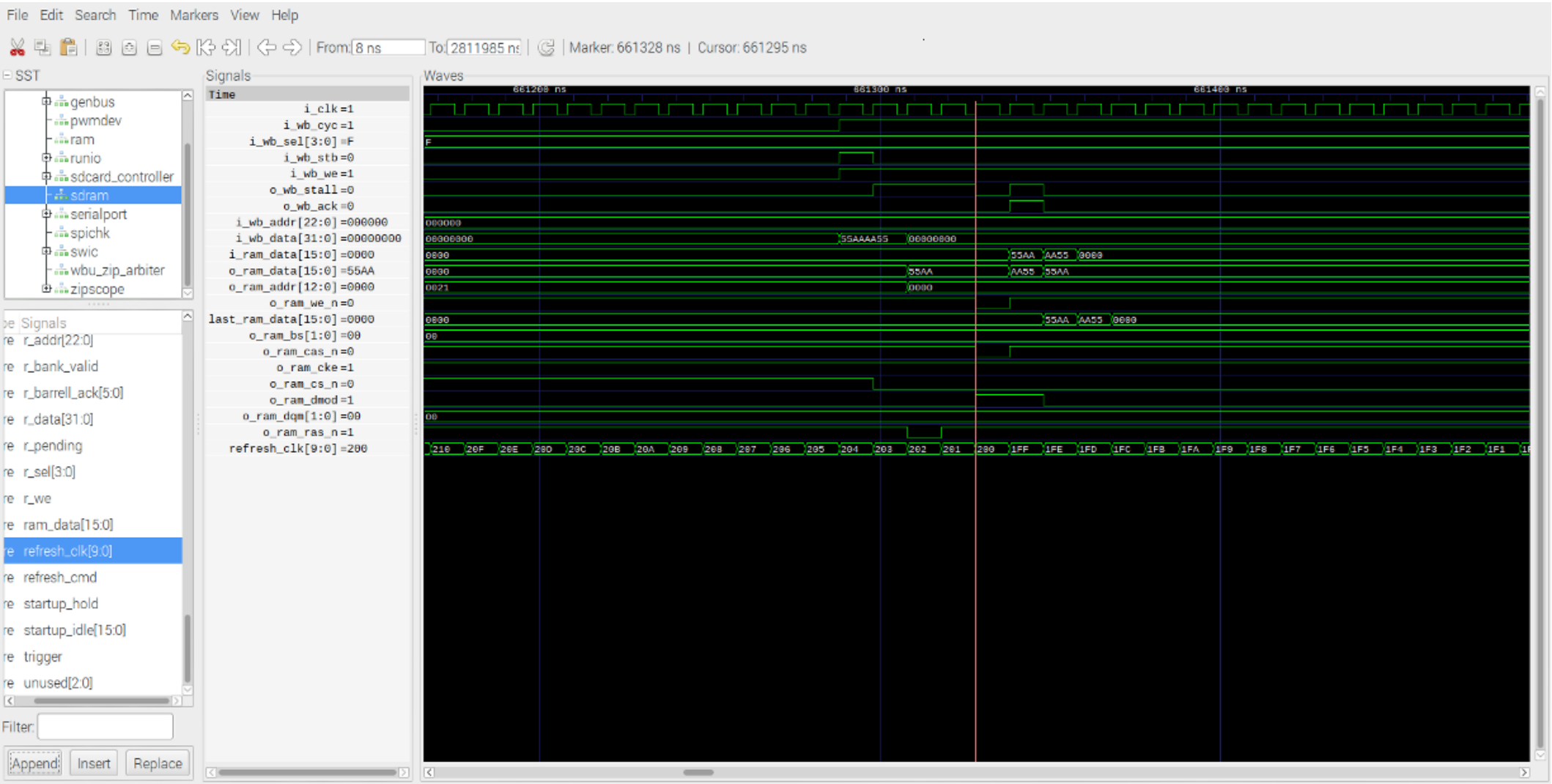
Write 0x2000000 0x55AAAA55
Address 0x0400 o_ram_data 0x55AA
o_ram_we_n & o_ram_ras_n
catzip

Error in simulation no lower 16 bits & hw
o_ram_data should be 0xaa55
Lower 16 bits get written to upper 16 bits hw



```
wire ram_drive_data
reg [15:0] r_ram_data,// Data lines (input)
wire [15:0] ram_data,  // Data lines (output)

assign io_ram_data = (ram_drive_data) ? ram_data : 16'bzzzz_zzzz_zzzz_zzzz;

reg  [15:0]     r_ram_data_ext_clk;
// always @(posedge intermediate_clk_n)
always @(posedge clk_s)
      r_ram_data_ext_clk <= io_ram_data;
always @(posedge clk_s)
      r_ram_data <= r_ram_data_ext_clk;



module   busmaster(i_clk, i_rst,
            i_rx_stb, i_rx_data, o_tx_stb, o_tx_data, i_tx_busy,
            // The SPI Flash lines
            o_sf_cs_n, o_sd_cs_n, o_spi_sck, o_spi_mosi, i_spi_miso,
            // The SDRAM lines
            o_ram_cs_n, o_ram_cke, o_ram_ras_n, o_ram_cas_n,
                  o_ram_we_n, o_ram_bs, o_ram_addr,
                  o_ram_drive_data, i_ram_data, o_ram_data,
```

Write 0x2000000 0x55AAAA55
Address 0x0000 o_ram_data 0x55AA
o_ram_we_n & o_ram_cas_n & o_ram_dmod xulalx25soc



Write 0x2000000 0x55AAAA55
Address 0x0400 o_ram_data 0x55AA
o_ram_we_n & o_ram_ras_n
xulalx25soc

Error in simulation hw
okay xulalx25soc
Should be o_ram_data
0xaa55