CATBOARD vs ICOBOARD

- Catboard SDRAM 33554432
- Autofaga project
- 2 PMODS, 4 pin dipsw, 4 leds, 2 push button switches & 20 pin header
- 50 MHz clock with PLL
- Ver 0.01 catboard has issues with spiflash
- Yosys tool chain
- Interface to Rpi
- HX8K FPGA

- ICOboard SRAM 131072
- Autofpga project
- 4 PMODS
- 50 MHz clock no PLL
- Spixpress works on gamma version
- Yosys tool chain
- Interface to Rpi
- HX8K FPGA

CLOCK for ICOBOARD

- Reason the ICOBOARD does use a PLL for clock.
- 2018-09-03
- 14:45 <ZipCPU> The iCE40 PLL is tied to some specific pins. If you use it, you may no longer get the special pin I/O function you want. For exmple, if I used the ice40 PLL's, I wouldn't be able to access the SRAM on my icoboard.

Sdram xulalx25soc

- ubuntu12.04$ xsload --usb 0 --fpga ~/testbuilds/learning_hdl/MyHDL/sdram/toplevel.bit
- MyHDL wishbone https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/sdramdev.py
- What is the xsload command to keep the program when power is restored

Sdram MyHDL

- MyHDL https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/memdev.py
- python memdev.py ;make top; sudo config_cat top.bin
- MyHDL https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/sdramdev.py

Sdram catzip xulalx25soc

- Autofpga project sdramdev.txt
- Catzip HX8K FPGA
- 50 MHz refresh_clk <= 10'd391
- wbsdram.v wishbone interface & sdramcontroller
- Verilator simulation arm-main_tb compiled with sdramsim.cpp & sdramsim.h
- Wishbone 32 bit addr & 32 bit data
- 0x2000000 to 0x2FFFFFF
- Write ./arm-wbregs 0x2000004 0x55aaaa55
- toplevel.v
  - main.v
    - Wbsdram.v

- Non Autofpga project maybe soon
- Xulalx25soc LX25 or LX9 FPGA
- 80 MHz refresh_clk <= 10'd625;
- wbsdram.v wishbone interface & sdramcontroller
- Verilator simulation busmaster_tb compiled with sdramsim.cpp & sdramsim.h
- Wishbone 32 bit addr & 32 bit data
- 0x2000000 to 0x2FFFFFF
- Write ./wbregs 0x2000004 0x55aaaa55
- Read ./wbregs 0x2000004
- toplevel.v
  - busmaster,v
    - Wbsdram.v

Sdram xulalx25soc

- ubuntu12.04$ xsload --usb 0 --fpga ~/testbuilds/learning_hdl/MyHDL/sdram/toplevel.bit
- xula2-lx9 toplevel.bit https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/toplevel.bit
- Ise build https://github.com/develone/learning_hdl/blob/master/MyHDL/sdram/wbsdram_ise_win8.pdf