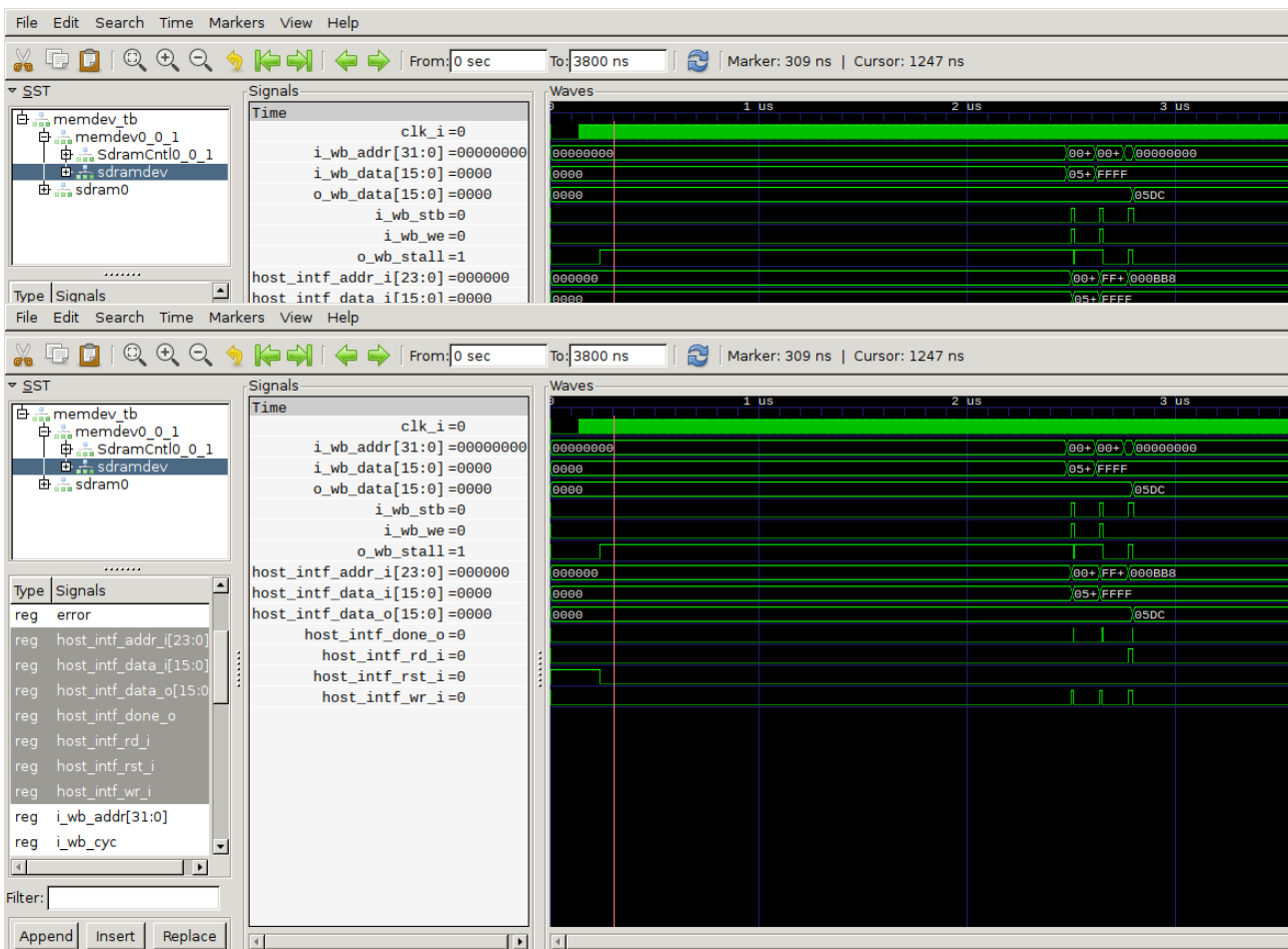


*****DRAFT*****
SDRAM
09/24/18
*****DRAFT*****

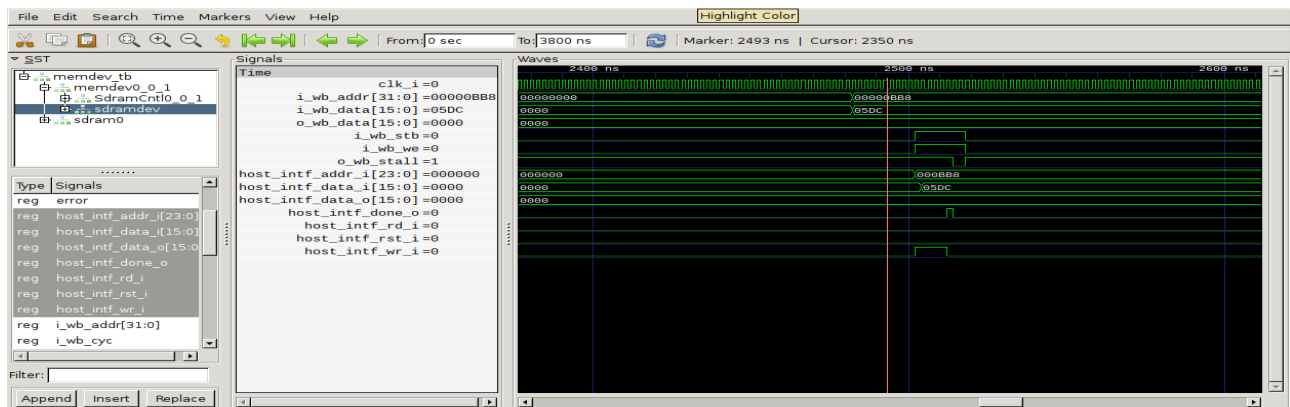
BANK 0 STATE : [CHANGE] Uninitialized -> Initialized @ 2138
BANK 1 STATE : [CHANGE] Uninitialized -> Initialized @ 2138
BANK 2 STATE : [CHANGE] Uninitialized -> Initialized @ 2138
BANK 3 STATE : [CHANGE] Uninitialized -> Initialized @ 2138

Mode	CAS	Burst
Burst | 3 | 1

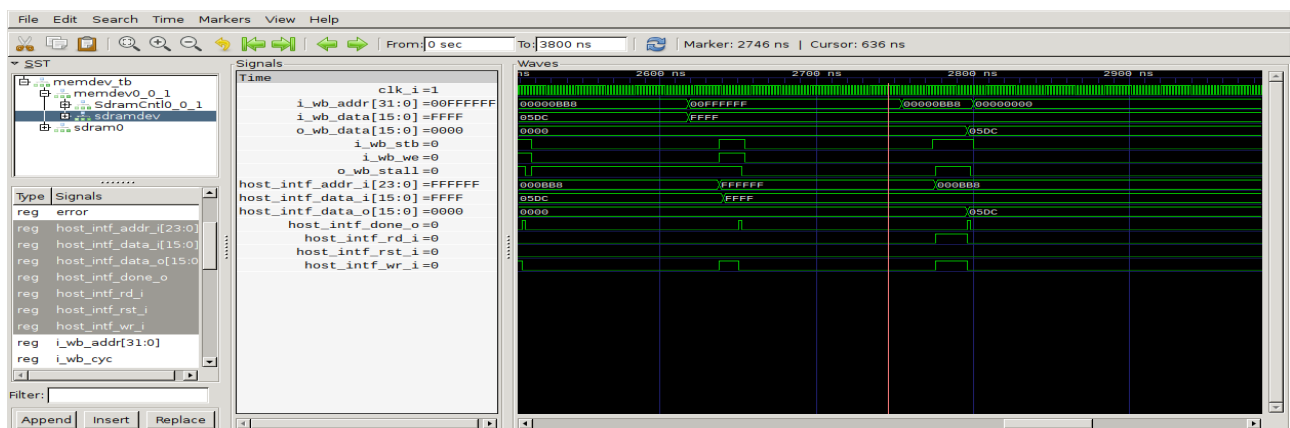
SDRAM : Bank 0 has active row 0005
BANK 0 STATE : WRITING @ 2514
DATA : [WRITE] Addr: 440 Data: 1500
BANK 0 STATE : WRITING TO 01b8:440
4400440: 1500
SDRAM : Bank 3 has active row 1fff
BANK 3 STATE : WRITING @ 2652
DATA : [WRITE] Addr: 511 Data: 65535
BANK 3 STATE : WRITING TO 01ff:511
4400440: 1500
5110511: 65535
SDRAM : Bank 0 has active row 0005
BANK 0 STATE : READING @ 2790
SDRAM : [READ] Commnad registered
BANK 0 STATE : READING FROM 01b8:440
STATE : [READ] Data Ready @ 2794 value : 1500



SDRAM : Bank 0 has active row 0005
 BANK 0 STATE : WRITING @ 2514
 DATA : [WRITE] Addr: 440 Data: 1500
 BANK 0 STATE : WRITING TO 01b8:440

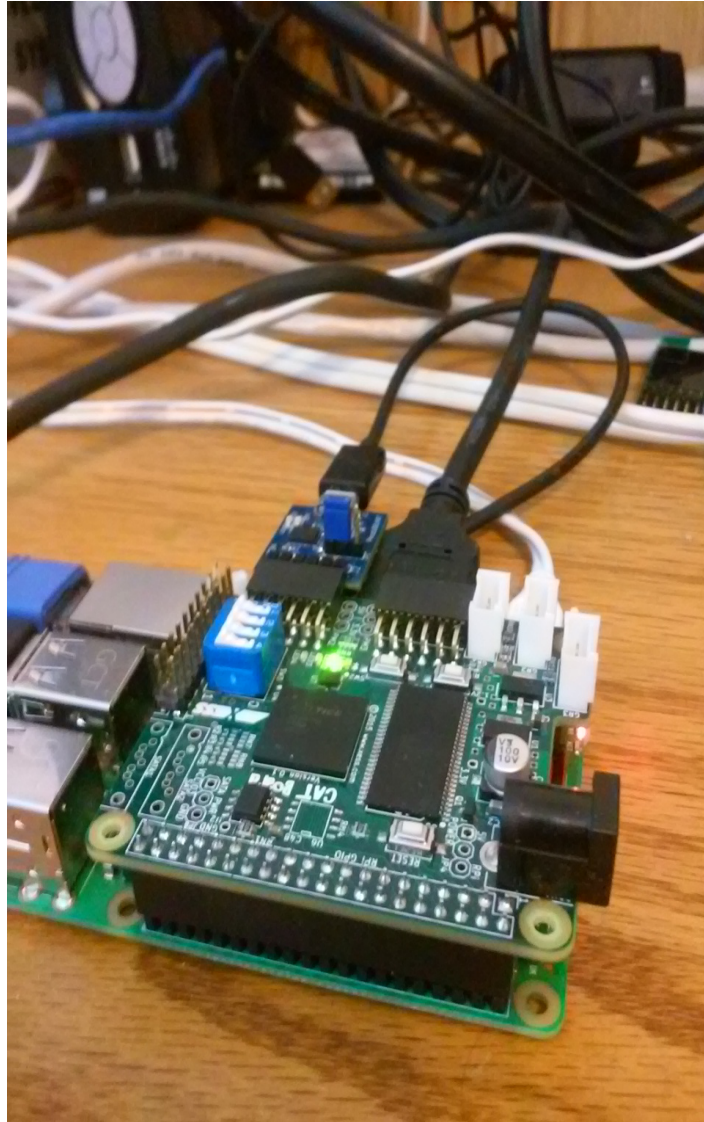


BANK 0 STATE : READING @ 2790
 SDRAM : [READ] Commnad registered
 BANK 0 STATE : READING FROM 01b8:440
 STATE : [READ] Data Ready @ 2794 value : 1500

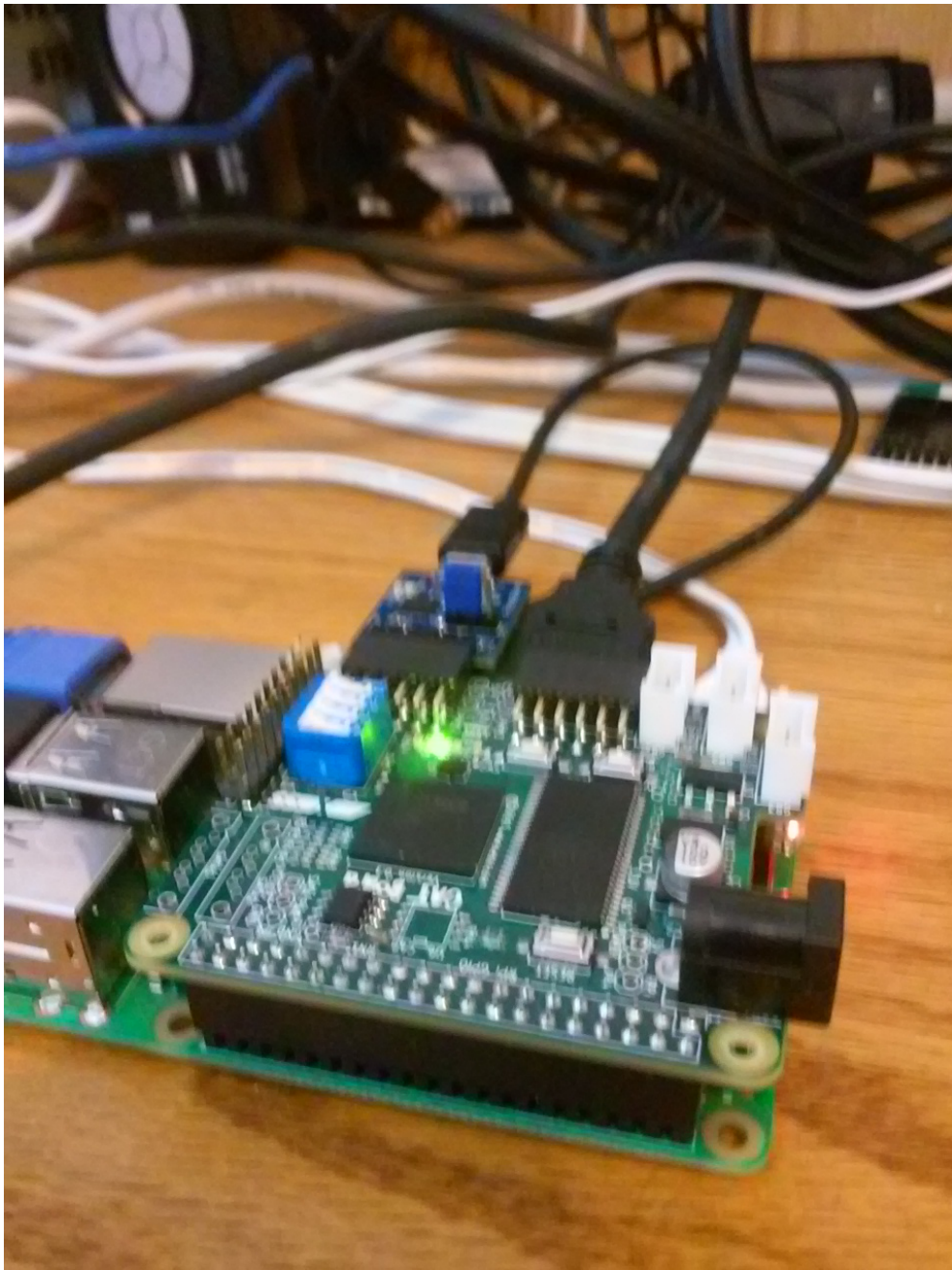


The memory_test takes approximately 3.5 sec or 175e6 clocks to complete at 50MHz. The memory_test writes to 16777215 locations and reads the data written.

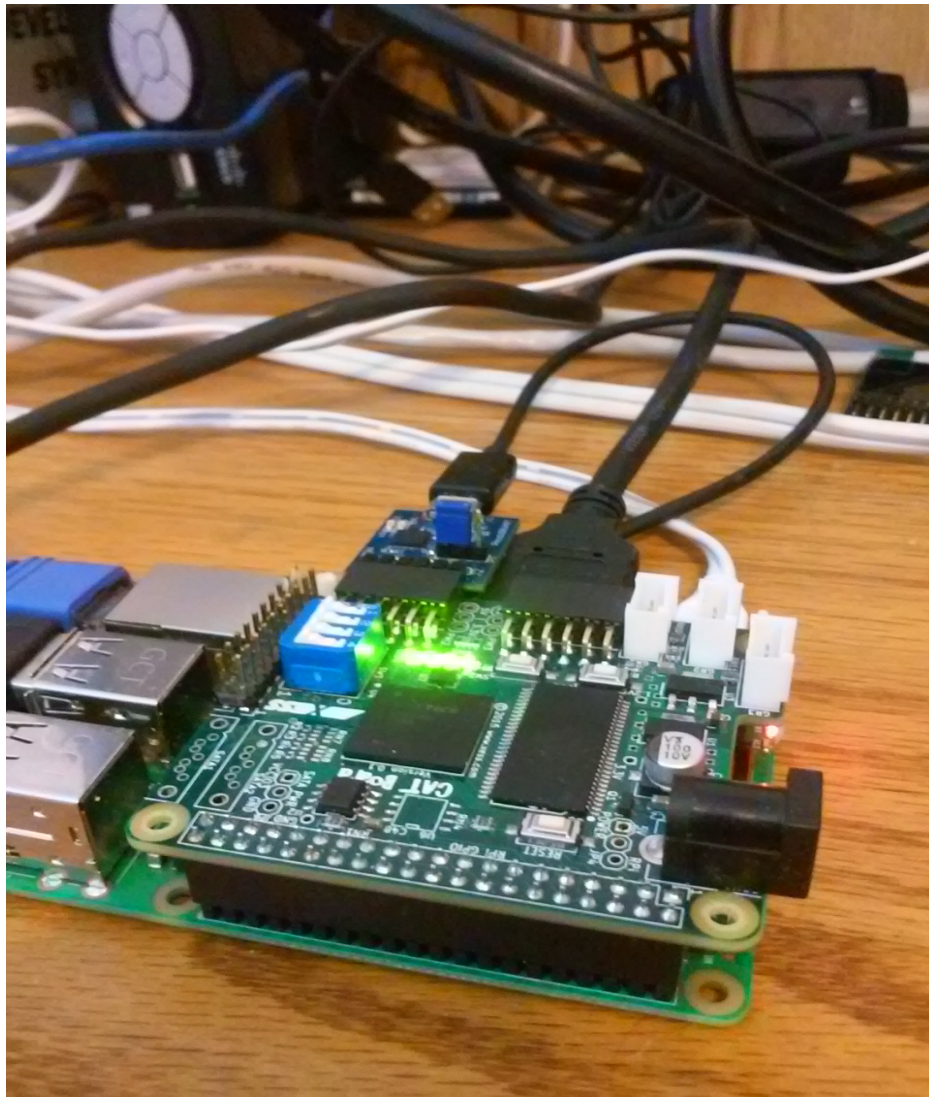
Catboard running top.bin after the program has been load starting to write to memory during the memory_test



Catboard running top.bin after the program has been load starting to read from memory during the memory_test



Catboard running top.bin after the program has been load and the end memory memory_test. Note all 4 leds are on.



Now the sdram_test is memdev

```
module top (
    clk100MHz,
    sdram_clk,
    sdram_return_clk,
    led_status,
    pb,
    memdev0_SdramCntl0_sd_intf_cke,
    memdev0_SdramCntl0_sd_intf_we,
    memdev0_SdramCntl0_sd_intf_addr,
    memdev0_SdramCntl0_sd_intf_dqml,
    memdev0_SdramCntl0_sd_intf_cas,
    memdev0_SdramCntl0_sd_intf_dqmh,
    memdev0_SdramCntl0_sd_intf_ras,
    memdev0_SdramCntl0_sd_intf_bs,
    memdev0_SdramCntl0_sd_intf_cs,
    memdev0_SdramCntl0_sd_intf_dq
);
=== top ===
```

Number of wires:

441

Number of wire bits:	968
Number of public wires:	84
Number of public wire bits:	537
Number of memories:	0
Number of memory bits:	0
Number of processes:	0
Number of cells:	719
\$_TBUF_	16
SB_CARRY	68
SB_DFF	4
SB_DFFE	4
SB_DFFER	98
SB_DFFES	1
SB_DFFESR	45
SB_DFFESS	4
SB_DFFR	52
SB_DFFS	8
SB_DFFSR	3
SB_DFFSS	4
SB_LUT4	412

Host interface signals

```

wire [23:0] memdev0_SdramCntl0_host_intf_addr_i;
wire [15:0] memdev0_SdramCntl0_host_intf_data_i;
wire [15:0] memdev0_SdramCntl0_host_intf_data_i;
wire [15:0] memdev0_SdramCntl0_host_intf_data_o;
wire memdev0_SdramCntl0_host_intf_done_o;
wire memdev0_SdramCntl0_host_intf_wr_i;
wire memdev0_memory_test0_host_intf_rst_i;

```

Write function

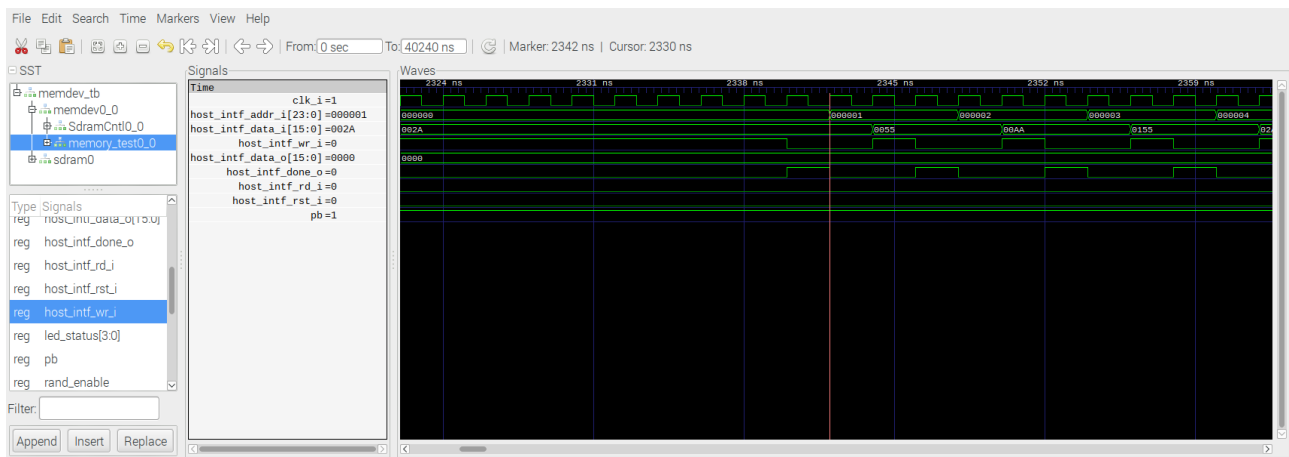
```

    during a write
    4 clks in between address chg
    4 clks in between data chg
    80 nsec

```

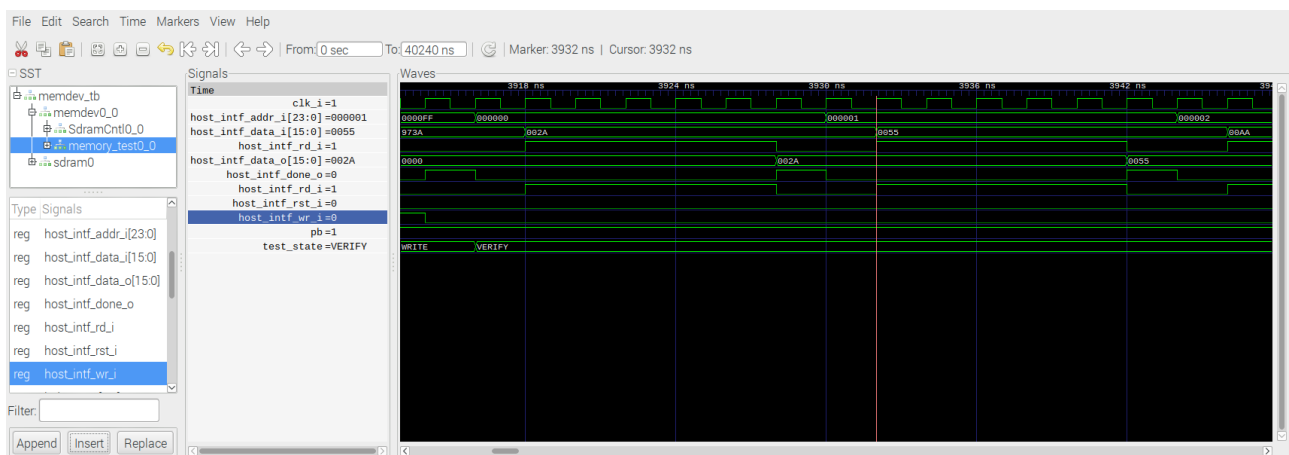
The 24 bit memdev0_SdramCntl0_host_intf_addr_i is set on the raising edge of clk. One clk later the 16 bit

memdev0_SdramCntl0_host_intf_data_i and memdev0_SdramCntl0_host_intf_wr_i goes hi. A clk later the memdev0_SdramCntl0_host_intf_done_o goes hi and the memdev0_SdramCntl0_host_intf_wr_i goes lo.



Read function

The 24 bit memdev0_Sdr0Cntl0_host_intf_addr_i is set on the raising edge of clk. One clk later the 16 bit memdev0_Sdr0Cntl0_host_intf_rd_i goes hi. Five clk later the memdev0_Sdr0Cntl0_host_intf_done_o goes hi, memdev0_Sdr0Cntl0_host_intf_data_o is valid and the memdev0_Sdr0Cntl0_host_intf_rd_i goes lo.



During the first part of the memory_test Write takes place.

python memdev.py

make

sudo config_cat top.bin

```
2^24      16777216    0x000000    0xFFFFFFFF    16Bits
@PREFIX=sdr0
@DEVID=SDRAM
@$LGMEMSZ=24
@$LGMEMSZ.FORMAT=%d
@$NADDR=(1<<(@$THIS.LGMEMSZ-2))
@$NBYTES=(1<<(@$THIS.LGMEMSZ))
@$NBYTES.FORMAT=0x%08x
@ACCESS=@$(DEVID)_ACCESS
```

@SLAVE.TYPE=MEMORY

@SLAVE.BUS=wb

@LD.PERM=wx