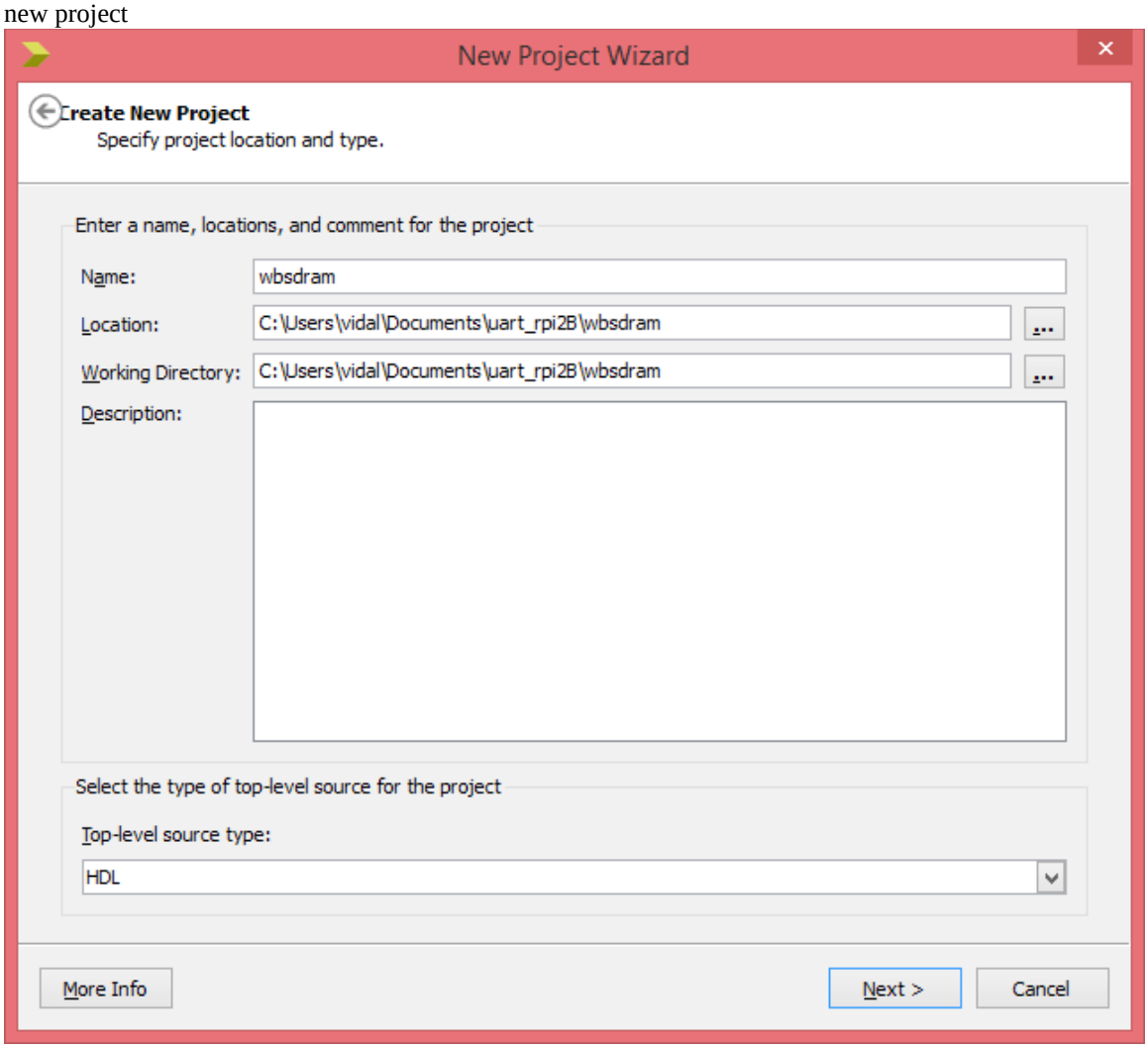
**********Draft**********

Xulalx25soc built for xula2-lx9

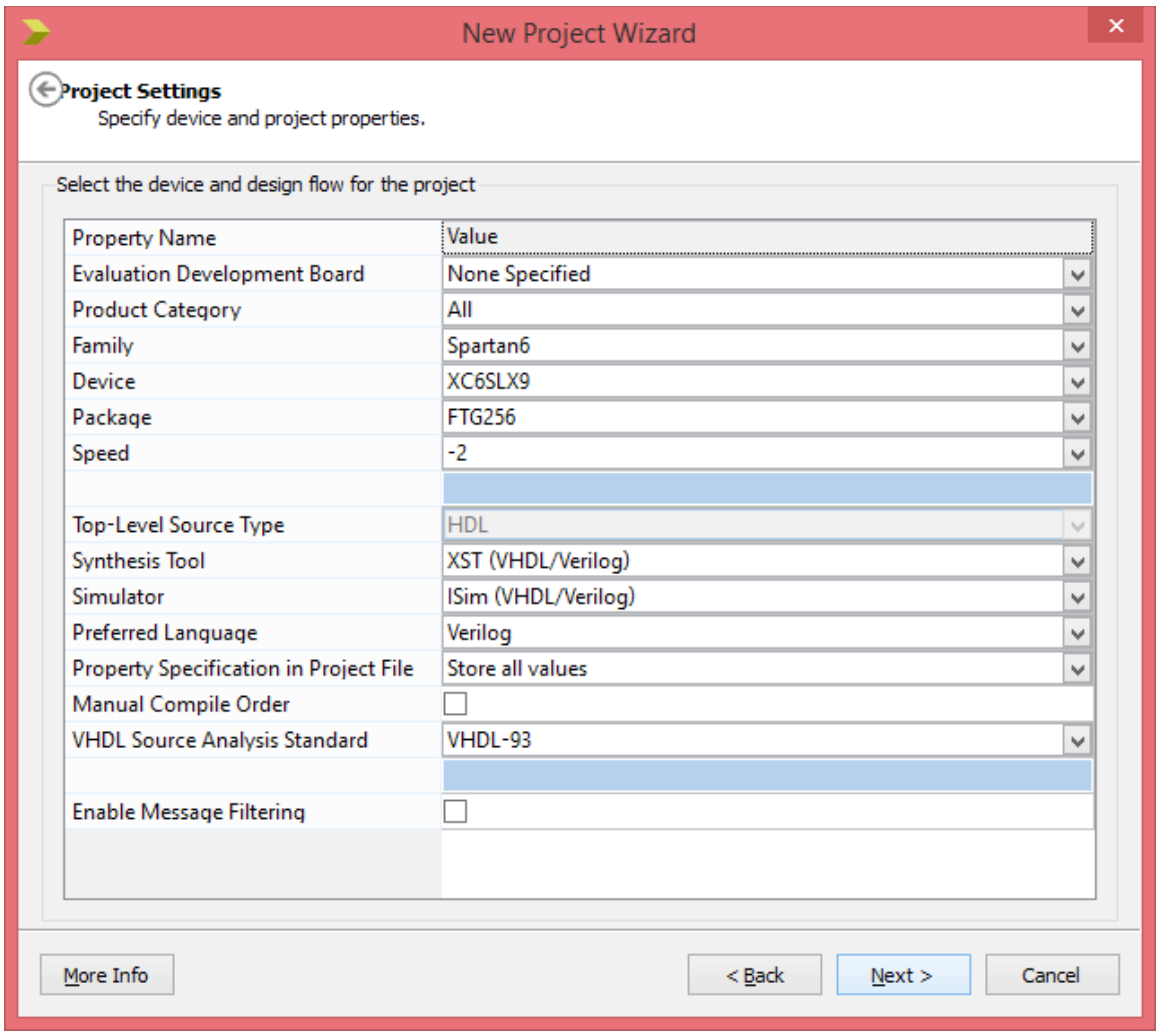
10/28/18

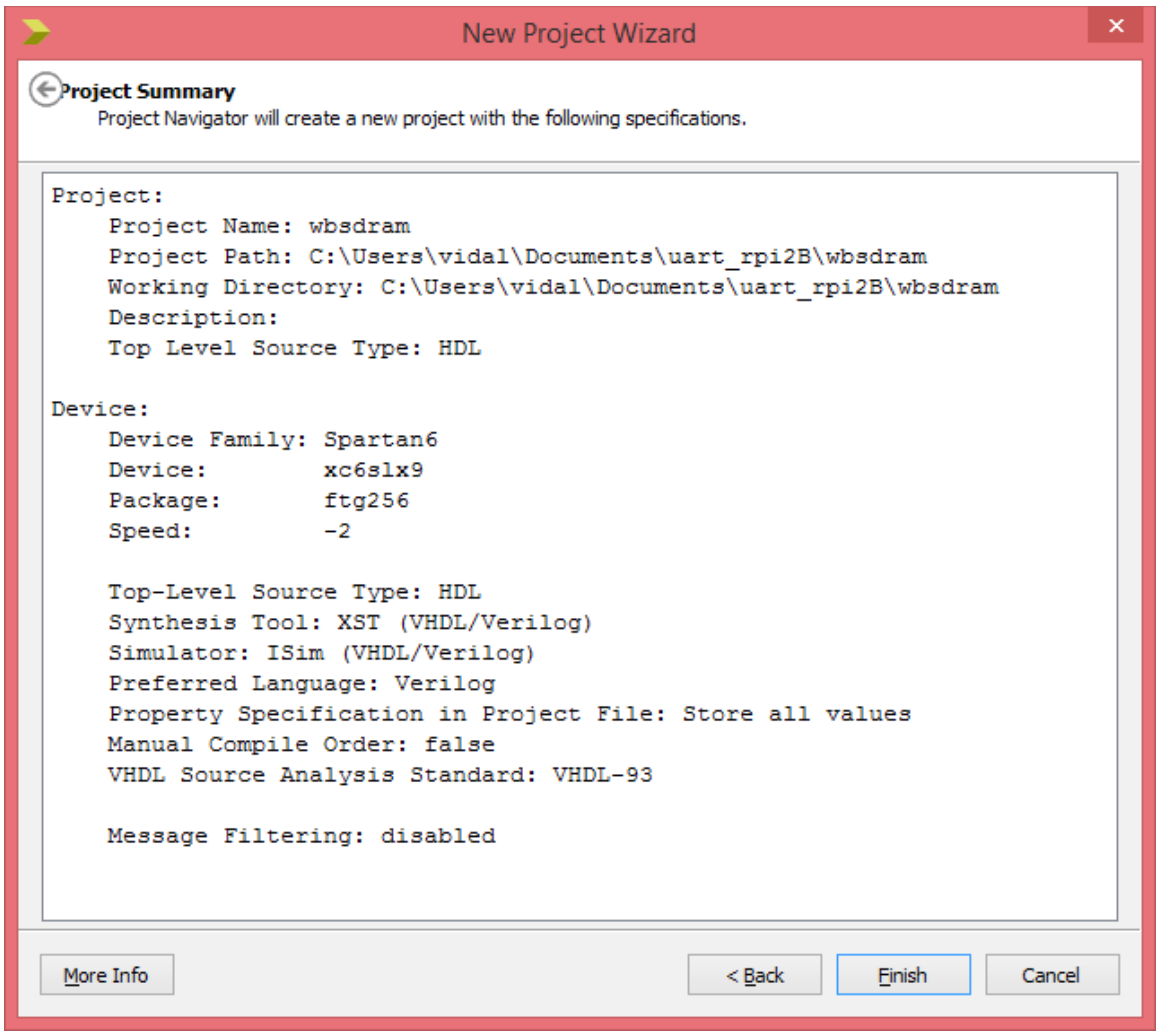
**********Draft**********

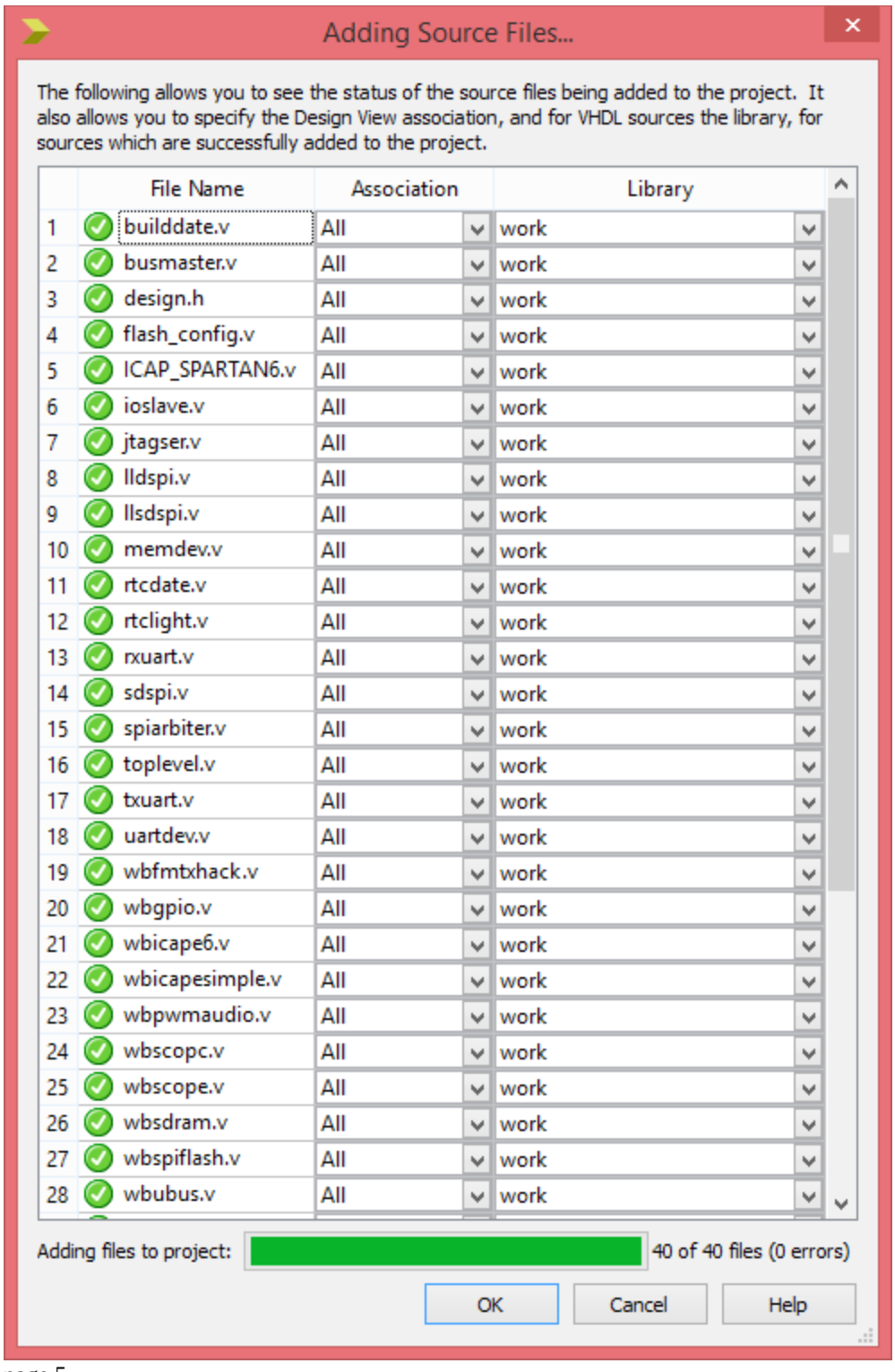
new project

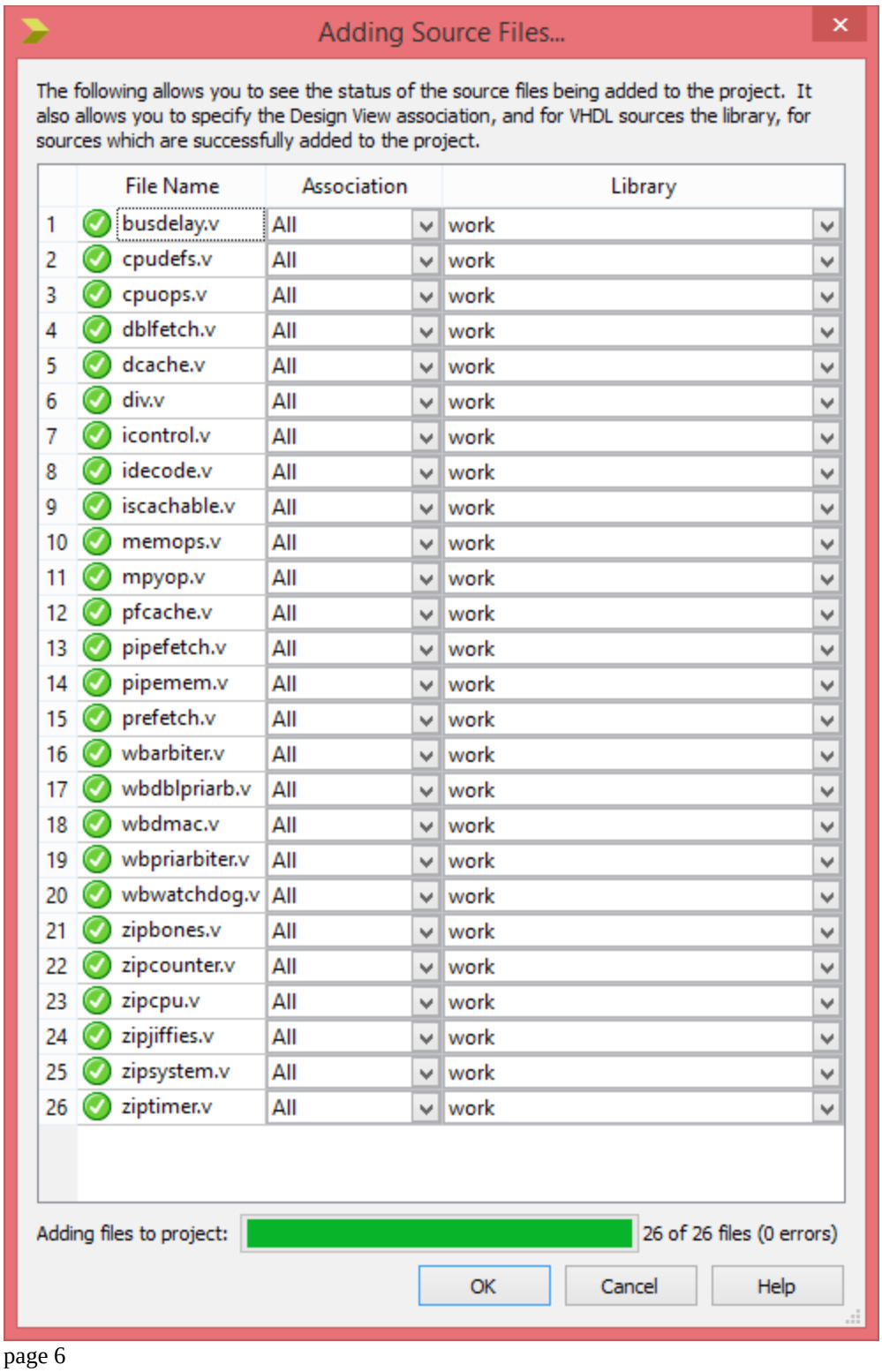


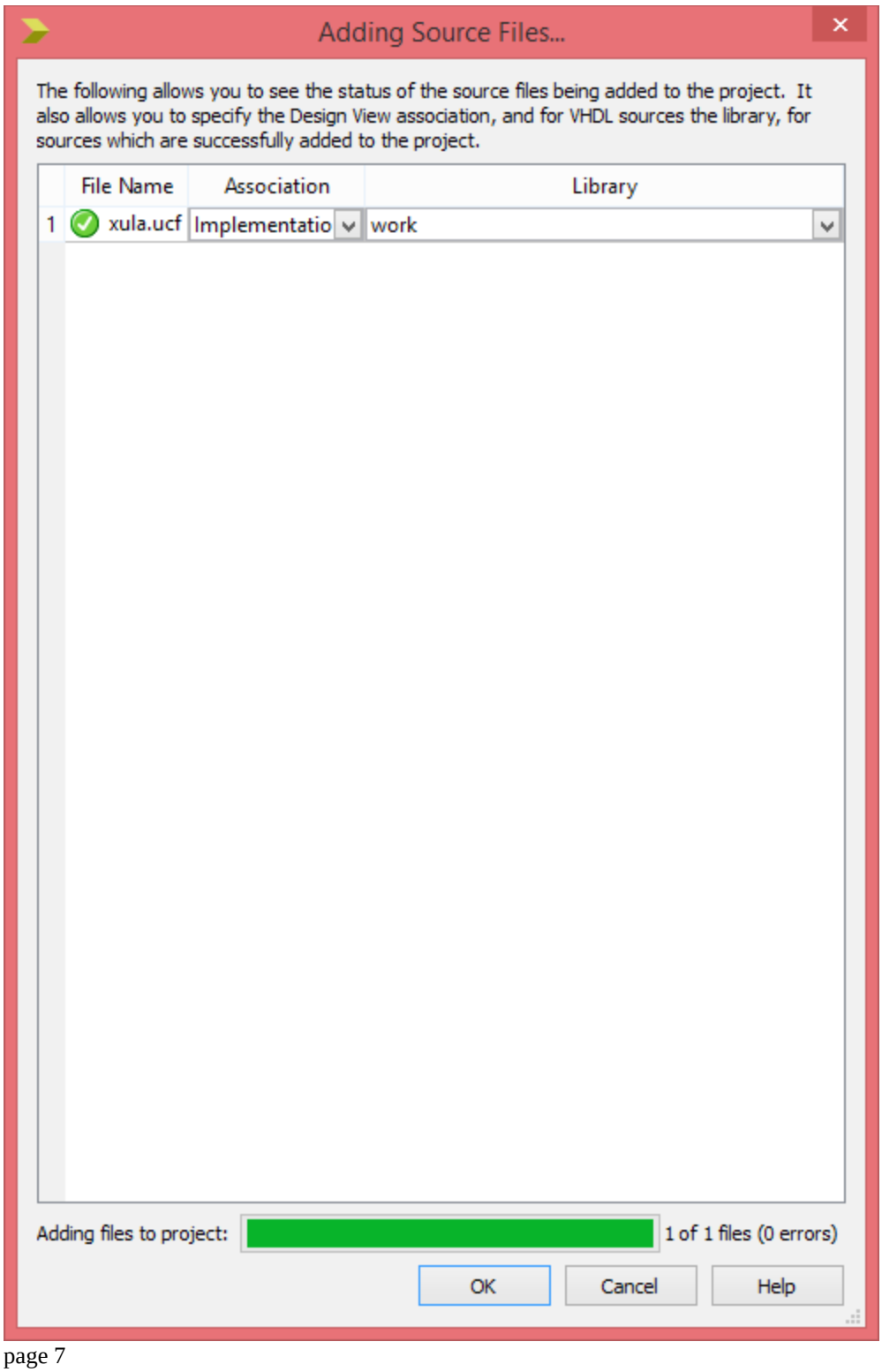
page 2

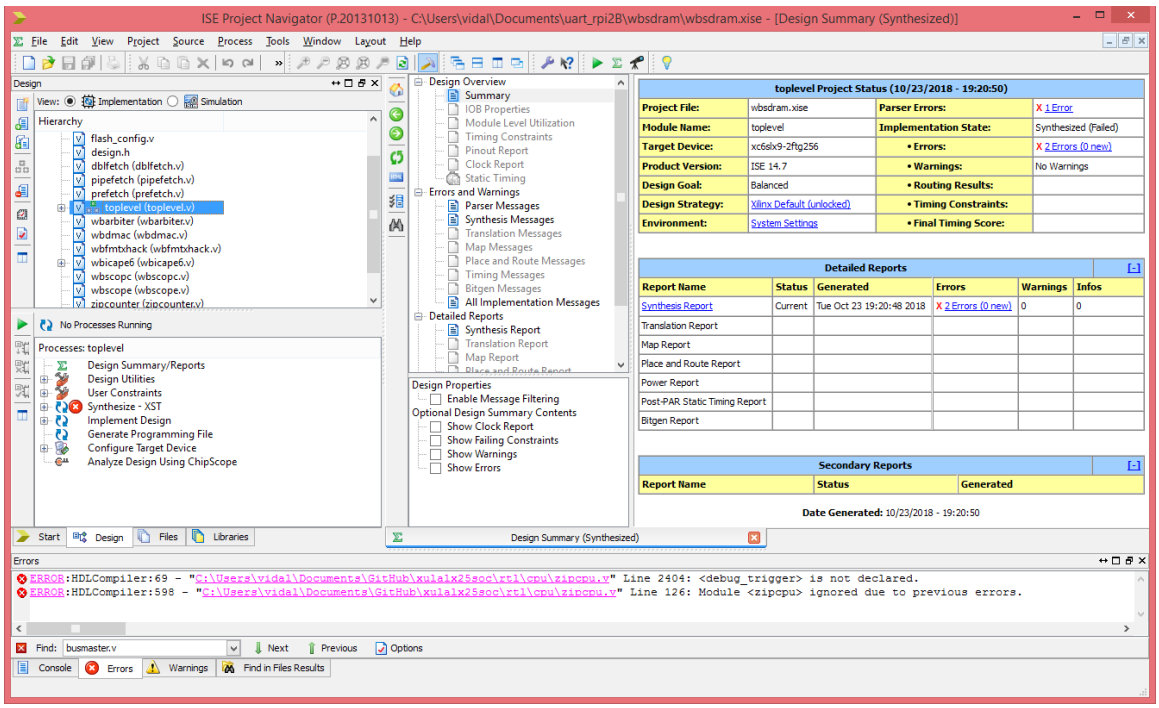

New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Spartan6
Device
XC6SLX9
Package
FTG256
Speed
-2
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
< Back
Next >
Cancel


New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: wbsdram
Project Path: C:\Users\vidal\Documents\uart_rpi2B\wbsdram
Working Directory: C:\Users\vidal\Documents\uart_rpi2B\wbsdram
Description:
Top Level Source Type: HDL
Device:
Device Family: Spartan6
Device: xc6slx9
Package: ftg256
Speed: -2
Top-Level Source Type: HDL
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISim (VHDL/Verilog)
Preferred Language: Verilog
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
Message Filtering: disabled
More Info
< Back
Finish
Cancel


Adding Source Files...
The following allows you to see the status of the source files being added to the project. It also allows you to specify the Design View association, and for VHDL sources the library, for sources which are successfully added to the project.
File Name
Association
Library
1 builddate.v All work
2 busmaster.v All work
3 design.h All work
4 flash_config.v All work
5 ICAP_SPARTAN6.v All work
6 ioslave.v All work
7 jtagser.v All work
8 lldspi.v All work
9 llsdspi.v All work
10 memdev.v All work
11 rtcdate.v All work
12 rtclight.v All work
13 rxuart.v All work
14 sdspi.v All work
15 spiarbiter.v All work
16 toplevel.v All work
17 txuart.v All work
18 uartdev.v All work
19 wbfmtxhack.v All work
20 wbgpio.v All work
21 wbicape6.v All work
22 wbicapesimple.v All work
23 wbpwmaudio.v All work
24 wbscopc.v All work
25 wbscope.v All work
26 wbsdram.v All work
27 wbspiflash.v All work
28 wbubus.v All work
Adding files to project:
40 of 40 files (0 errors)
OK
Cancel
Help

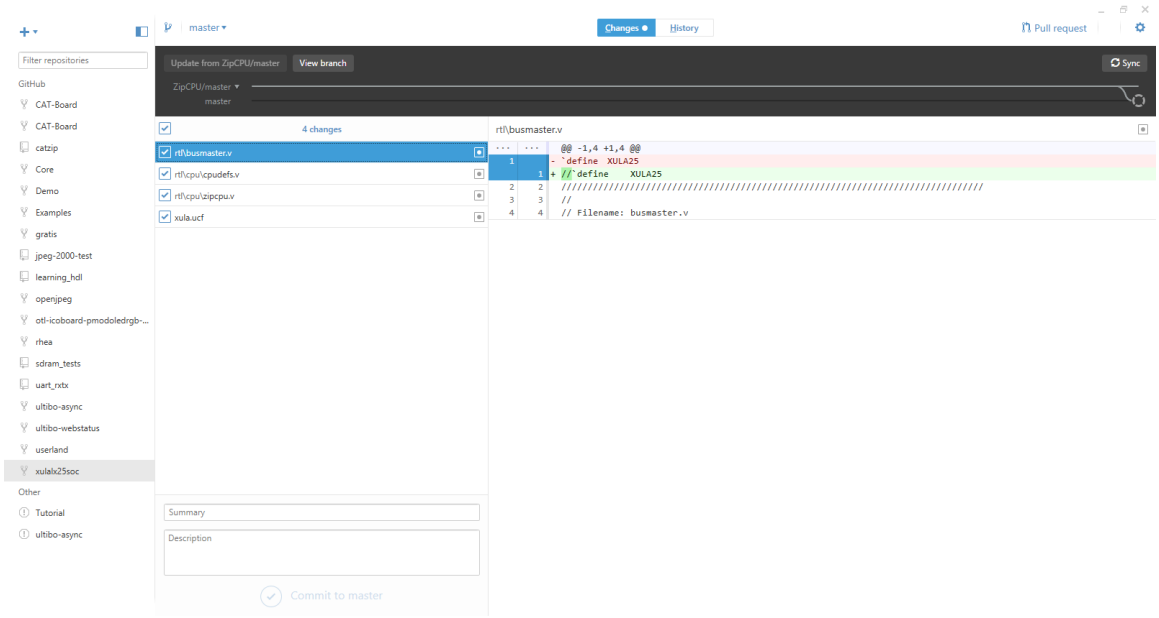

Adding Source Files...
The following allows you to see the status of the source files being added to the project. It also allows you to specify the Design View association, and for VHDL sources the library, for sources which are successfully added to the project.
File Name
Association
Library
1 busdelay.v All work
2 cpudefs.v All work
3 cpuops.v All work
4 dblfetch.v All work
5 dcache.v All work
6 div.v All work
7 icontrol.v All work
8 idecode.v All work
9 iscachable.v All work
10 memops.v All work
11 mpyop.v All work
12 pfcache.v All work
13 pipefetch.v All work
14 pipemem.v All work
15 prefetch.v All work
16 wbarbiter.v All work
17 wbdblpriarb.v All work
18 wbdmac.v All work
19 wbpriarbiter.v All work
20 wbwatchdog.v All work
21 zipbones.v All work
22 zipcounter.v All work
23 zipcpu.v All work
24 zipjiffies.v All work
25 zipsystem.v All work
26 ziptimer.v All work
Adding files to project:
26 of 26 files (0 errors)
OK
Cancel
Help


Adding Source Files...
The following allows you to see the status of the source files being added to the project. It also allows you to specify the Design View association, and for VHDL sources the library, for sources which are successfully added to the project.
File Name
Association
Library
1
xula.ucf
Implementatio
work
Adding files to project:
1 of 1 files (0 errors)
OK
Cancel
Help


ISE Project Navigator (P.20131013) - C:\Users\vidal\Documents\uart_rpi2B\wbsdram\wbsdram.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
flash_config.v
design.h
dblfetch (dblfetch.v)
pipefetch (pipefetch.v)
prefetch (prefetch.v)
toplevel (toplevel.v)
wbarbiter (wbarbiter.v)
wbdmac (wbdmac.v)
wbfmtxhack (wbfmtxhack.v)
wbicape6 (wbicape6.v)
wbscopc (wbscopc.v)
wbscope (wbscope.v)
zipcounter (zipcounter.v)
No Processes Running
Processes: toplevel
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Translation Report
Map Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
toplevel Project Status (10/23/2018 - 19:20:50)
Project File: wbsdram.xise
Parser Errors: X 1 Error
Module Name: toplevel
Implementation State: Synthesized (Failed)
Target Device: xc6slx9-2ftg256
• Errors: X 2 Errors (0 new)
Product Version: ISE 14.7
• Warnings: No Warnings
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Oct 23 19:20:48 2018 | X 2 Errors (0 new) | 0 | 0
Translation Report
Map Report
Place and Route Report
Power Report
Post-PAR Static Timing Report
Bitgen Report
Secondary Reports
Report Name | Status | Generated
Date Generated: 10/23/2018 - 19:20:50
Start Design Files Libraries
Design Summary (Synthesized)
Errors
ERROR:HDLCompiler:69 - "C:\Users\vidal\Documents\GitHub\xulalx25soc\rtl\cpu\zipcpu.v" Line 2404: <debug_trigger> is not declared.
ERROR:HDLCompiler:598 - "C:\Users\vidal\Documents\GitHub\xulalx25soc\rtl\cpu\zipcpu.v" Line 126: Module <zipcpu> ignored due to previous errors.
Find: busmaster.v
Next
Previous
Options
Console Errors Warnings Find in Files Results

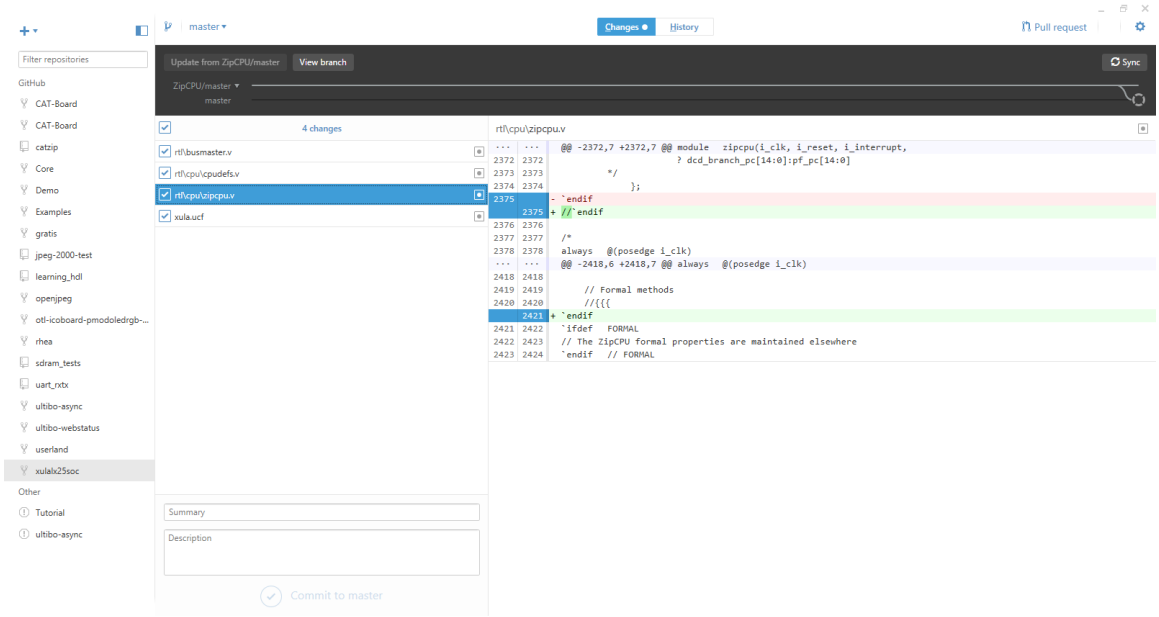
10/28/18

busmaster.v



cpudefs.v & busmaster.v

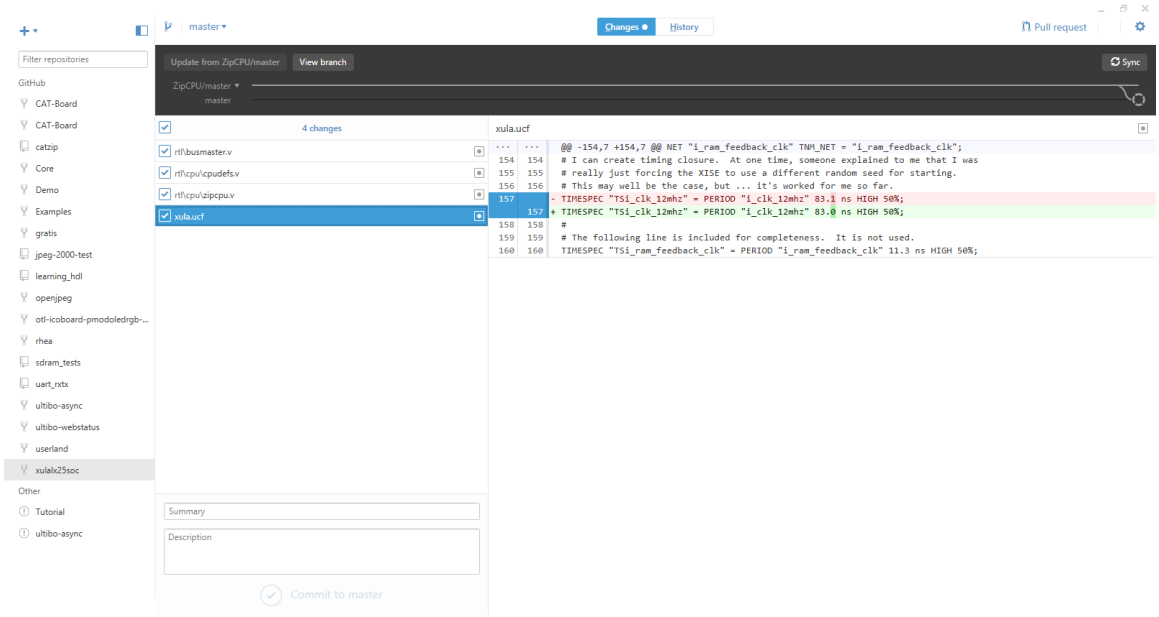
//`define XULA25
changed OPT_MULITPY from 4 to 2
commented OPT_DIVIDE
commented OPT_CIS
added to zipcpu.v at line 2421 `endif  and commented out 2475 //`endif



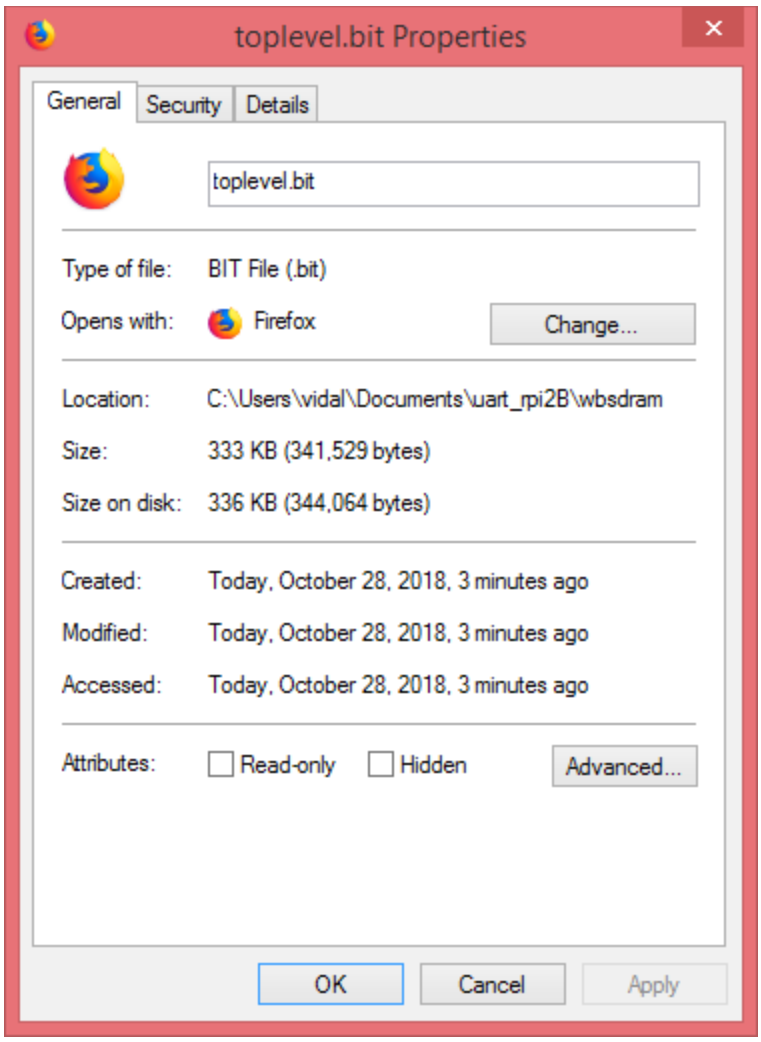
changed xula.ucf
TIMESPEC "TSi_clk_12mhz" = PERIOD "i_clk_12mhz" 83.1 ns HIGH 50%;
TIMESPEC "TSi_clk_12mhz" = PERIOD "i_clk_12mhz" 83.0 ns HIGH 50%;

Design Summary

Number of errors: 0
Number of warnings: 100
Slice Logic Utilization:
Number of Slice Registers: 3,594 out of 11,440 31%
Number used as Flip Flops: 3,592
Number used as Latches: 0
Number used as Latch-thrus: 0
Number used as AND/OR logics: 2
Number of Slice LUTs: 5,622 out of 5,720 98%
Number used as logic: 5,090 out of 5,720 88%
Number using O6 output only: 3,746
Number using O5 output only: 271



Number using O5 and O6: 1,073
toplevel.bit


toplevel.bit Properties
General
Security
Details
toplevel.bit
Type of file:
BIT File (.bit)
Opens with:
Firefox
Change...
Location:
C:\Users\vidal\Documents\uart_rpi2B\wbsdram
Size:
333 KB (341,529 bytes)
Size on disk:
336 KB (344,064 bytes)
Created:
Today, October 28, 2018, 3 minutes ago
Modified:
Today, October 28, 2018, 3 minutes ago
Accessed:
Today, October 28, 2018, 3 minutes ago
Attributes:
Read-only
Hidden
Advanced...
OK
Cancel
Apply