Trying to modify the exmaple of Jan Marjanovic, 2015 to test a Cosimulation of echotest.v with module echotest, txuartlite, and rxuartlite.

python echo_test.py

os.system('iverilog -o uu echotest.v echo_top.v')
return Cosimulation('vvp -m ./myhdl.vpi uu', clk=i_clk, uart_rx=i_uart_rx, uart_tx=o_uart_tx)

gtkwave echo_top.vcd