*********DRAFT*********
Adapting the OLED designed for the ICOBOARD
to the CATBOARD
05/27/18
*********DRAFT*********

The youtube video https://www.youtube.com/watch?v=UMDcnwZA2YE describes the interface between an OLED display and the ICOBOARD.
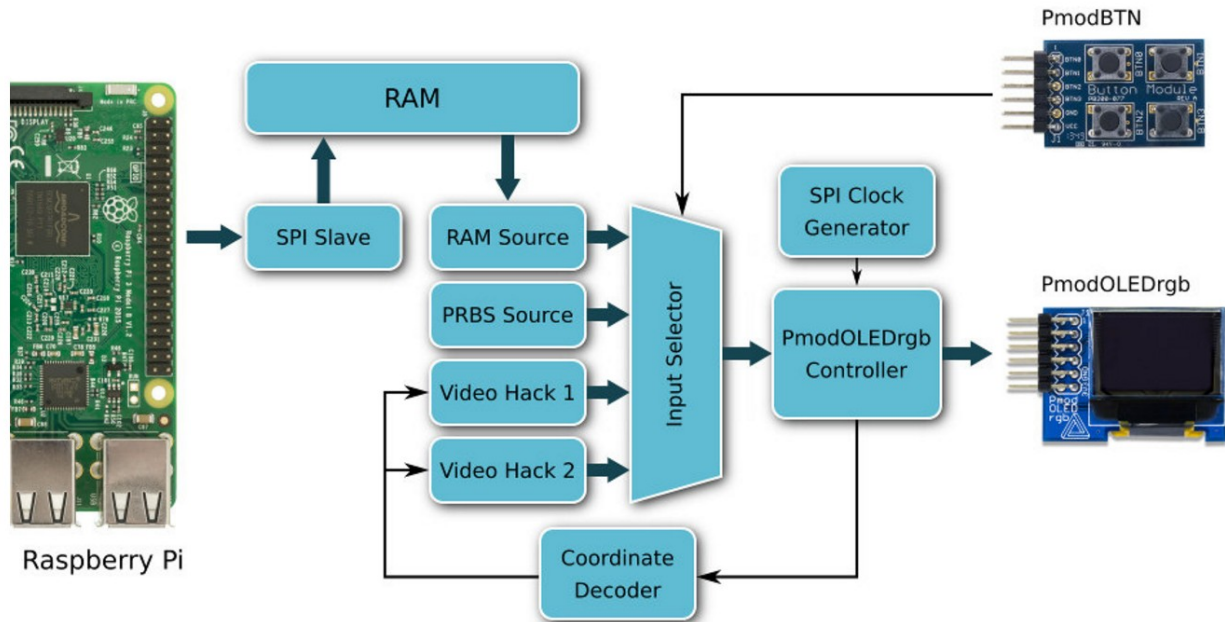
Goal of this effor: Is to perform the same functions using the CATBOARD instead of the ICOBOARD.

otl-icoboard-pmodoldergb-demo

Design Block Diagram

Design Structure

First forked the repository ttps://github.hcom/jhol/otl-icoboard-pmodoledrgb-demo

git clone https://github.com/develone/otl-icoboard-pmodoledrgb-demo.git

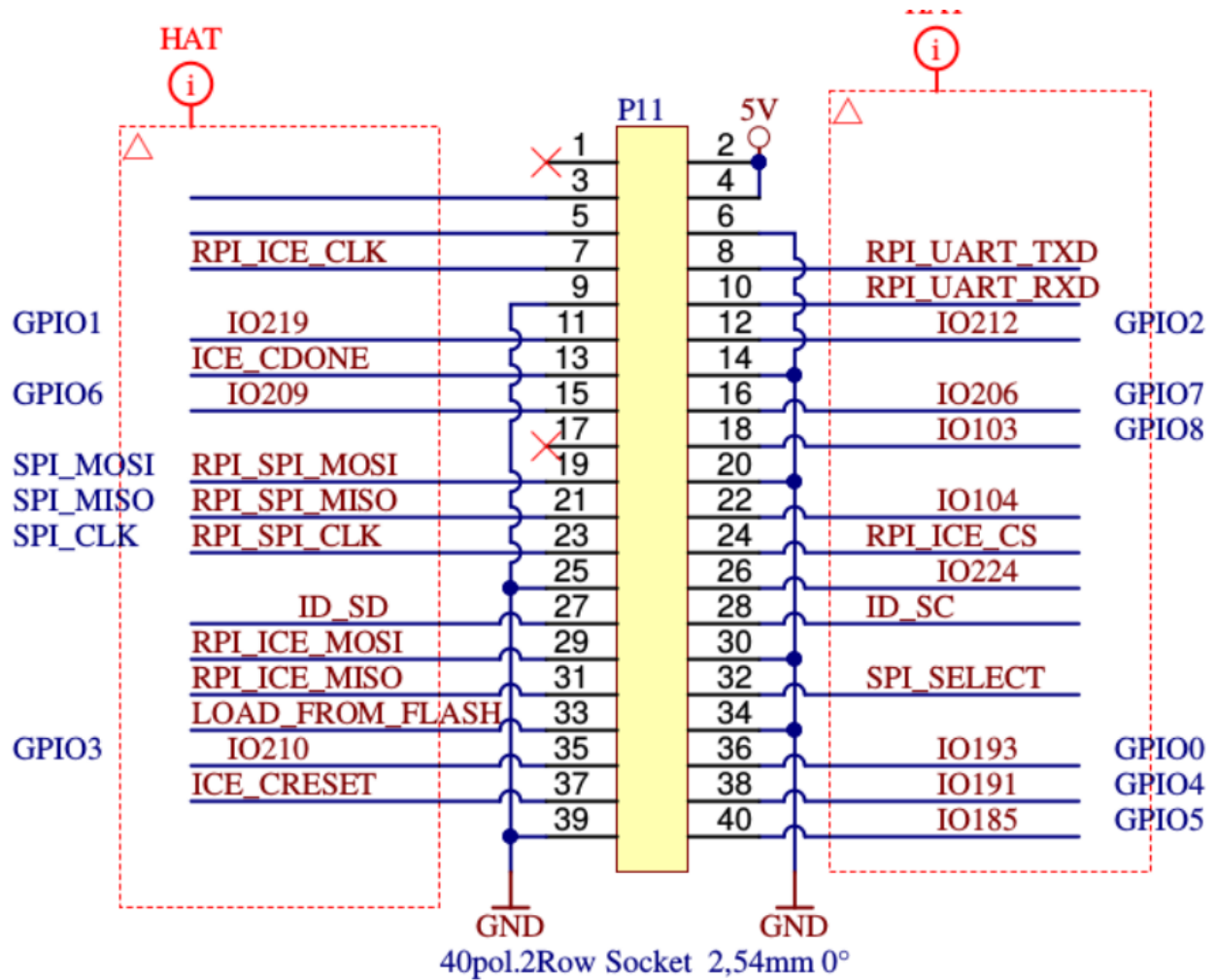*"cd otl-icoboard-pmodoledrgb-demo/"*

Need to create a new branch to track the changes required for the CATBOARD.
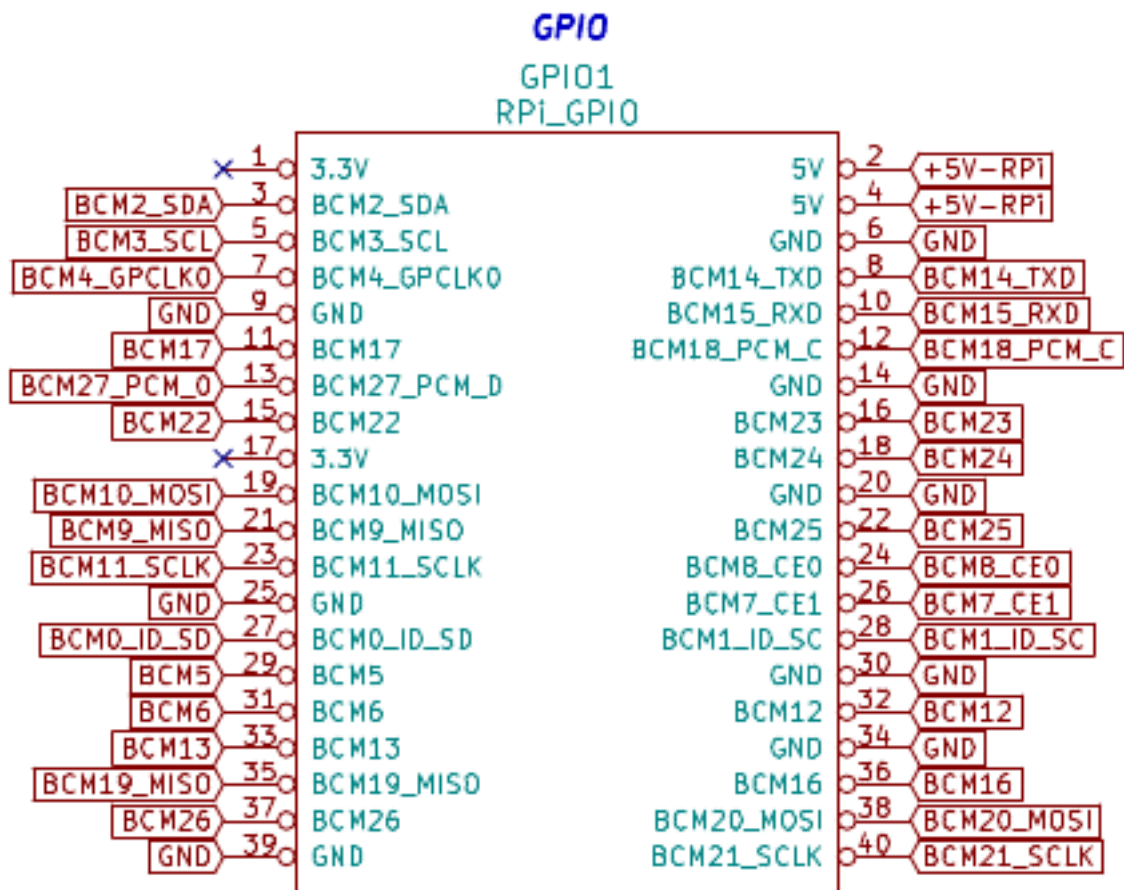*"git branch catboard"*
Even though the FPGAs ice40 HX8K are same for the CATBOARD and the ICOBOARD.

1.)   The first issue is the interface between the Raspberry Pi and FPGA hat.

ICOBOARD RPi

ⓘ

	P11		
✕	1	2 ○	5V
	3	4	
	5	6	
RPI_ICE_CLK	7	8	RPI_UART_TXD
	9	10	RPI_UART_RXD
GPIO1 IO219	11	12	IO212 GPIO2
ICE_CDONE	13	14	
GPIO6 IO209	15	16	IO206 GPIO7
✕	17	18	IO103 GPIO8
SPI_MOSI RPI_SPI_MOSI	19	20	
SPI_MISO RPI_SPI_MISO	21	22	IO104
SPI_CLK RPI_SPI_CLK	23	24	RPI_ICE_CS
	25	26	IO224
ID_SD	27	28	ID_SC
RPI_ICE_MOSI	29	30	
RPI_ICE_MISO	31	32	SPI_SELECT
LOAD_FROM_FLASH	33	34	
GPIO3 IO210	35	36	IO193 GPIO0
ICE_CRESET	37	38	IO191 GPIO4
	39	40	IO185 GPIO5

GND   GND
40pol.2Row Socket 2,54mm 0°

CATBOARD RPi

GPIO

GPIO1
RPi_GPIO

	Pin	Signal		Signal	Pin	
✕	1	3.3V		5V	2	+5V—RPi
BCM2_SDA	3	BCM2_SDA		5V	4	+5V—RPi
BCM3_SCL	5	BCM3_SCL		GND	6	GND
BCM4_GPCLK0	7	BCM4_GPCLK0		BCM14_TXD	8	BCM14_TXD
GND	9	GND		BCM15_RXD	10	BCM15_RXD
BCM17	11	BCM17		BCM18_PCM_C	12	BCM18_PCM_C
BCM27_PCM_0	13	BCM27_PCM_D		GND	14	GND
BCM22	15	BCM22		BCM23	16	BCM23
✕	17	3.3V		BCM24	18	BCM24
BCM10_MOSI	19	BCM10_MOSI		GND	20	GND
BCM9_MISO	21	BCM9_MISO		BCM25	22	BCM25
BCM11_SCLK	23	BCM11_SCLK		BCM8_CE0	24	BCM8_CE0
GND	25	GND		BCM7_CE1	26	BCM7_CE1
BCM0_ID_SD	27	BCM0_ID_SD		BCM1_ID_SC	28	BCM1_ID_SC
BCM5	29	BCM5		GND	30	GND
BCM6	31	BCM6		BCM12	32	BCM12
BCM13	33	BCM13		GND	34	GND
BCM19_MISO	35	BCM19_MISO		BCM16	36	BCM16
BCM26	37	BCM26		BCM20_MOSI	38	BCM20_MOSI
GND	39	GND		BCM21_SCLK	40	BCM21_SCLK

2.)   The 2nd issue is the PMOD connections to FPGA are different.
3.)   Third, I do not have a Diglient PMOD 4 push button switch module.
4.)   The 4th issue is the PHASE LOCK LOOP difference.
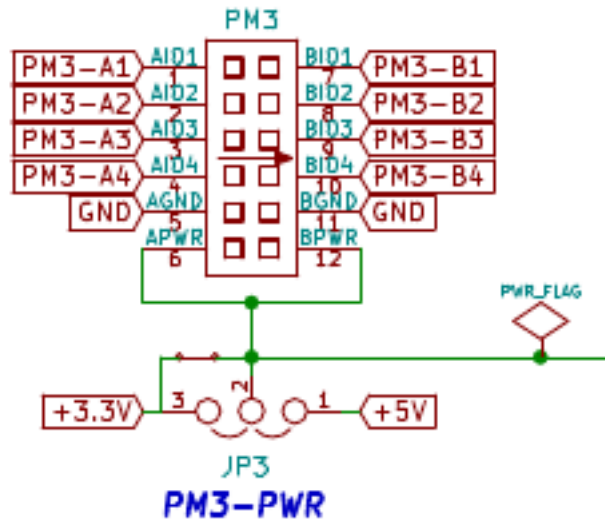
```
set_io clk_100mhz C8    #R9

set_io pmod1_1 A11      #D8
set_io pmod1_2 B12      #B9
```
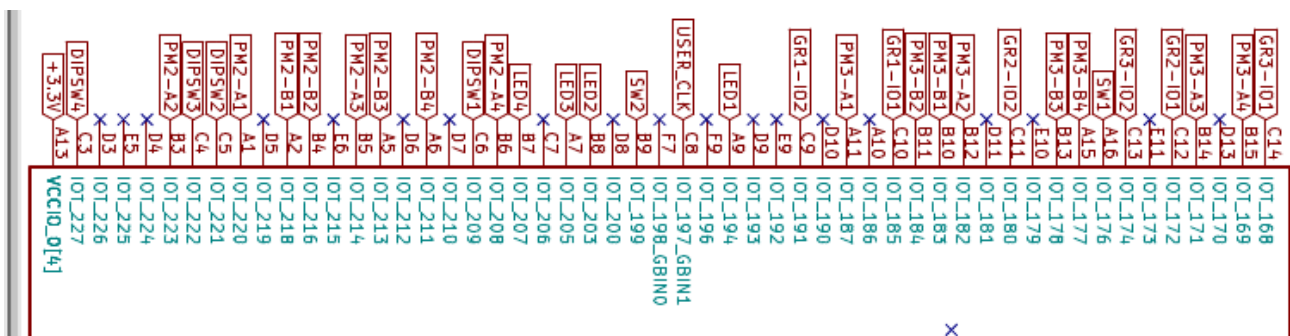
```
set_io pmod1_3 B14     #B10
set_io pmod1_4 B15     #B11
# 654321    catboard   # 654321  icoboard
#    xxxxxx PMOD3 A     #     xxxxxx PMOD1 A
#    xxxxxx PMOD3 B     #     xxxxxx PMOD1 B
# 654321                # 654321
#
set_io pmod1_7 B10     #B8
set_io pmod1_8 B11     #A9
set_io pmod1_9 B13     #A10
set_io pmod1_10 A15    #A11
```


CATBOARD connection to FPGA pins PMOD 2 & PMOD 3 push button switches, dip switch, and leds.

In top.v

```
module top(clk_100mhz, pmod1_1, pmod1_2, pmod1_3, pmod1_4, pmod1_7, pmod1_8,
  pmod1_9, pmod1_10, pmod2_7, pmod2_8, pmod2_9, pmod2_10, rpi_sck, rpi_cs,
  rpi_mosi);
```
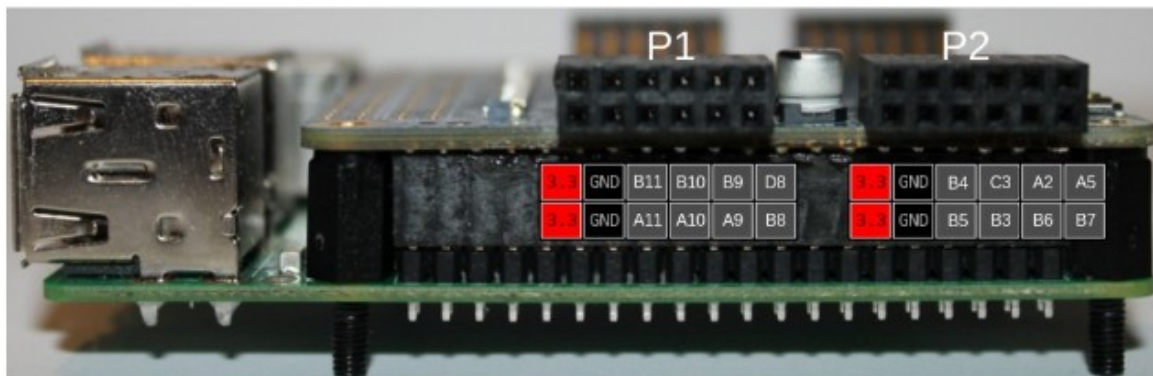
input rpi_sck, rpi_cs, rpi_mosi;
rpi_sck
rpi_cs
rpi_mosi

spi_ram_slave spi_ram_slave(clk, rpi_sck, rpi_cs, rpi_mosi,
 ram_addr, ram_data, ram_wr);
module spi_ram_slave(clk, sck, cs, mosi, ram_addr, ram_data, ram_wr);
PMOD pin out on icoboard

Pinout Pmod P1 and P2

Pinout PMOD P3 and P4