*********DRAFT*********

Adapting the OLED designed for the ICOBOARD to the CATBOARD

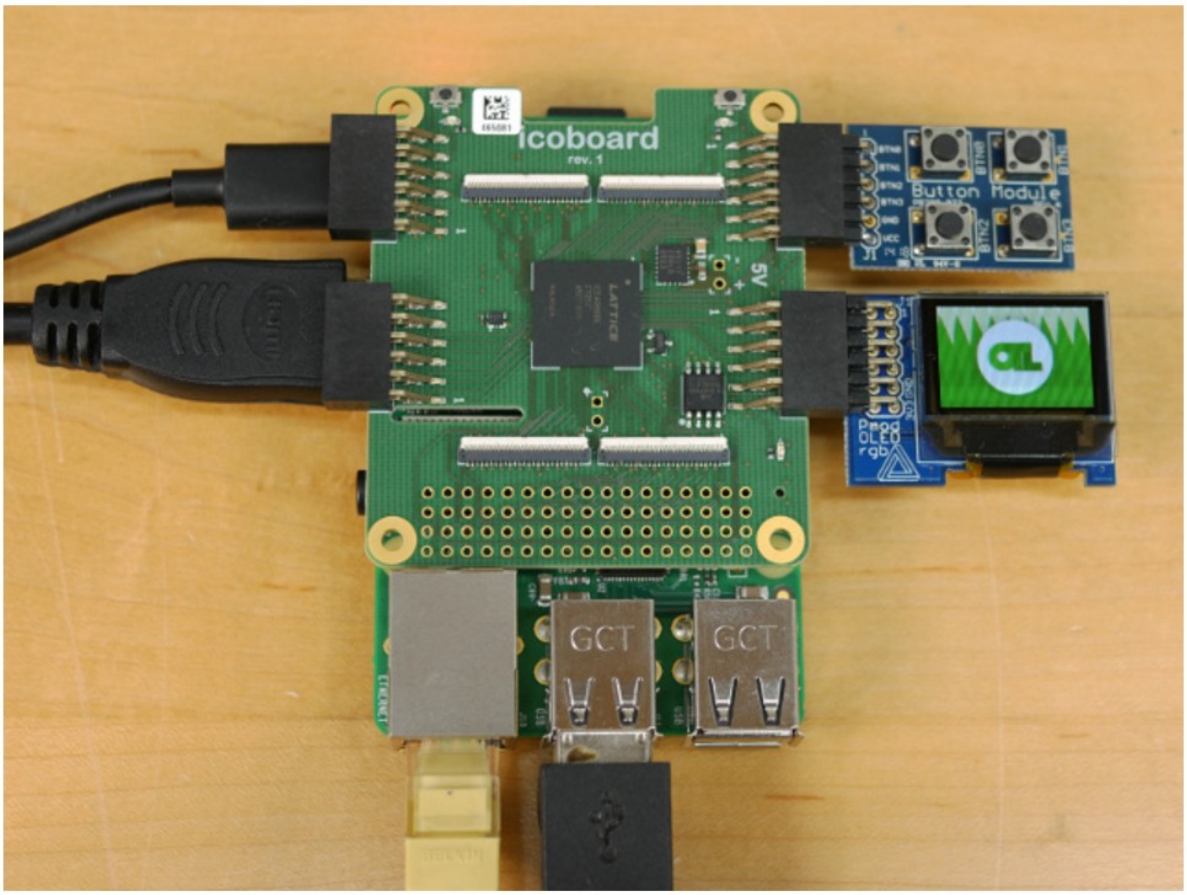
05/28/18

*********DRAFT*********

The youtube video https://www.youtube.com/watch?v=UMDcnwZA2YE describes the interface between an OLED display and the ICOBOARD.

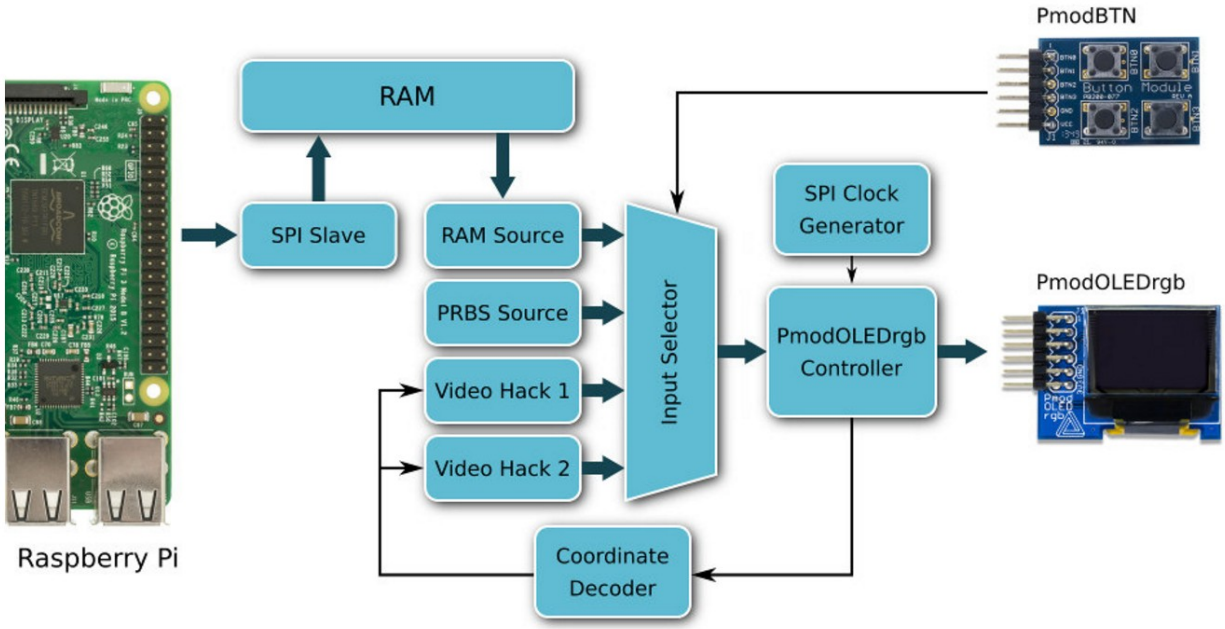
Goal of this effor: Is to perform the same functions using the CATBOARD instead of the ICOBOARD.

otl-icoboard-pmodoldergb-demo



Design Block Diagram

Design Structure



First forked the repository ttps://github.hcom/jhol/otl-icoboard-pmodoledrgb-demo

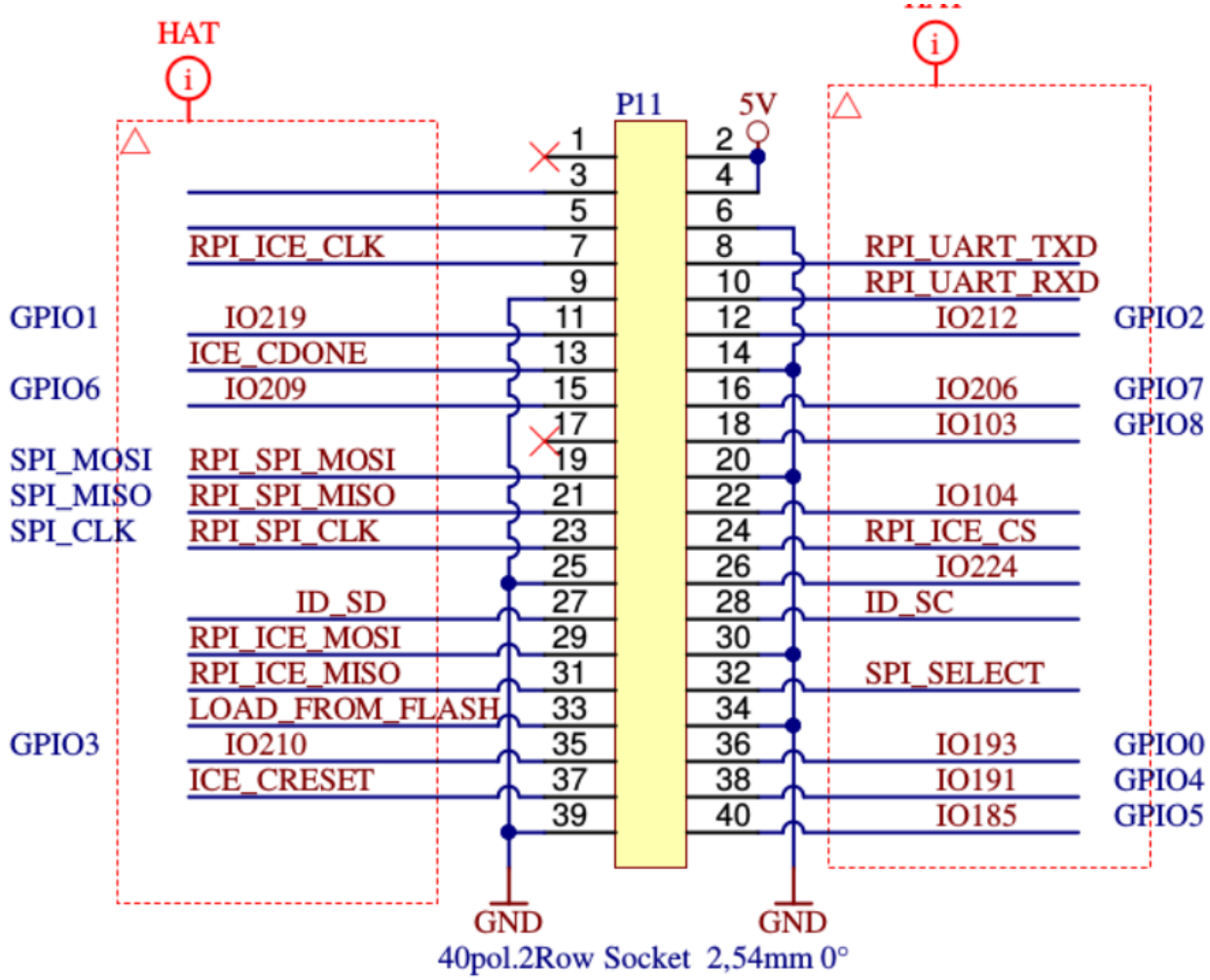
git clone https://github.com/develone/otl-icoboard-pmodoledrgb-demo.git

"cd otl-icoboard-pmodoledrgb-demo/"

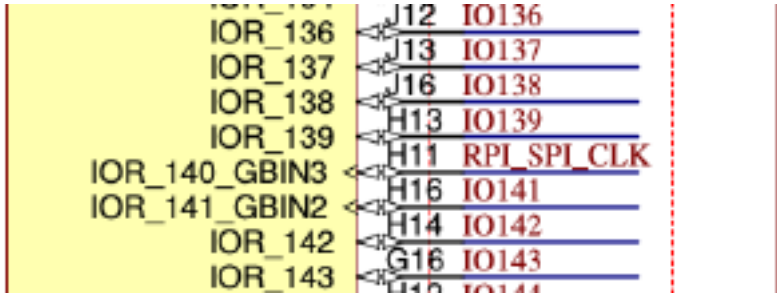
Need to create a new branch to track the changes required for the CATBOARD.
"git branch catboard"
Even though the FPGAs ice40 HX8K are same for the CATBOARD and the ICOBOARD.

1.) The first issue is the interface between the Raspberry Pi and FPGA hat.

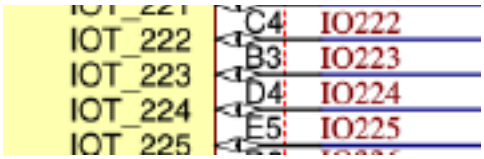
ICOBOARD RPi



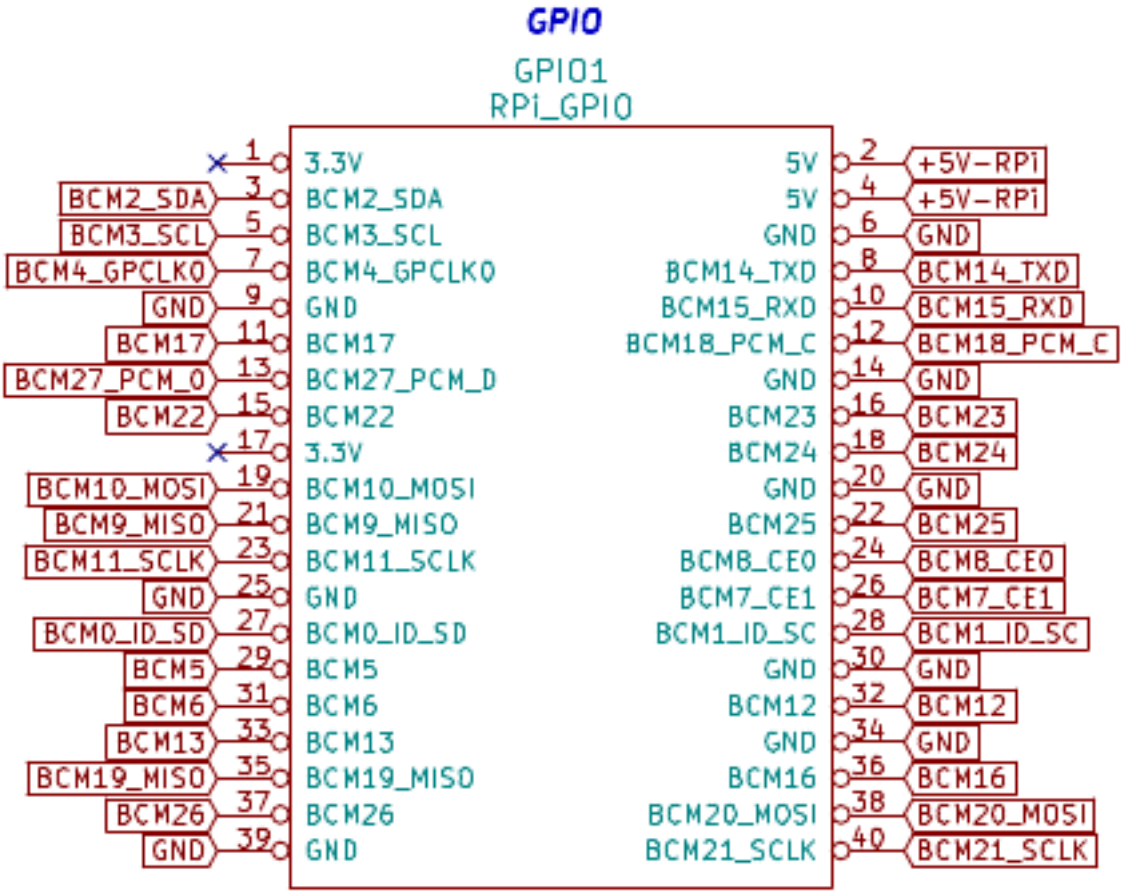
RPI_SPI_CLK H11 Pin 23 Pi icoboard



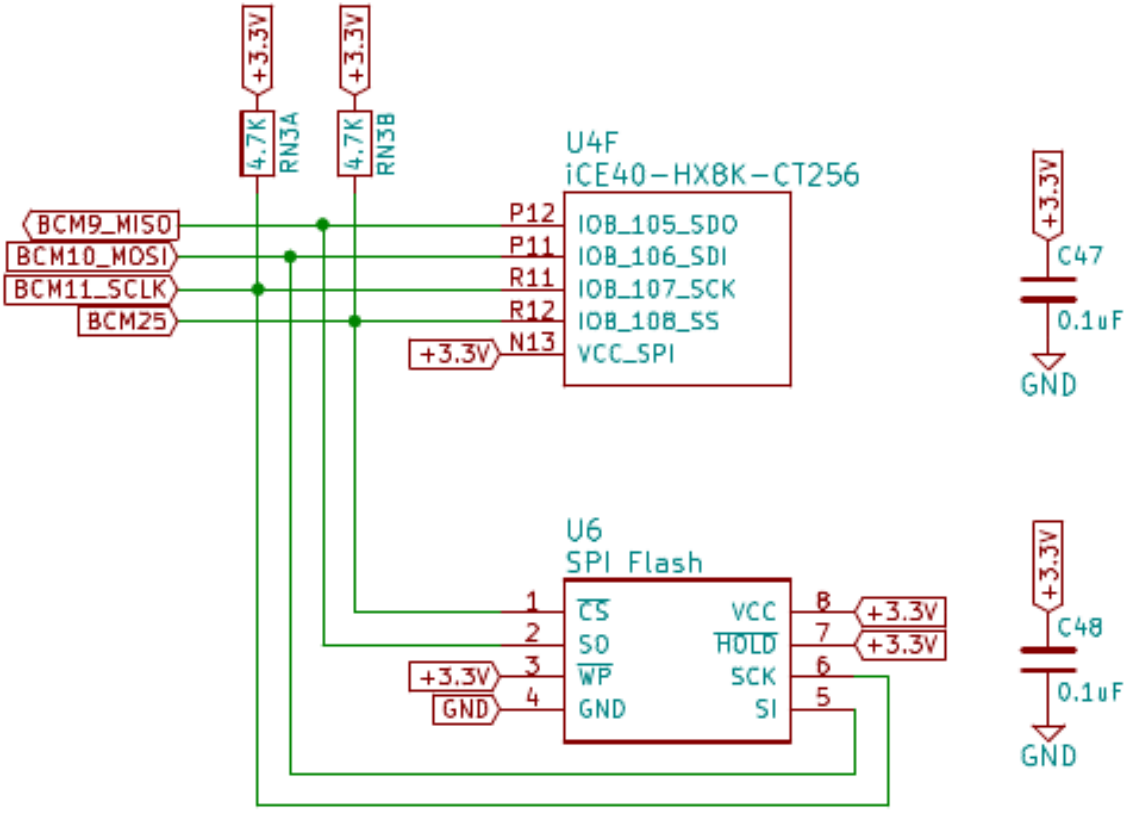
rpi_cs D4 IOT_224 Pin 26 Pi icoboard



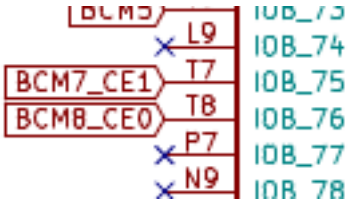
CATBOARD RPi



BCM11_SCLK Pin 23 CATBOARD



BCM7_CE1 Pin 26 CATBOARD

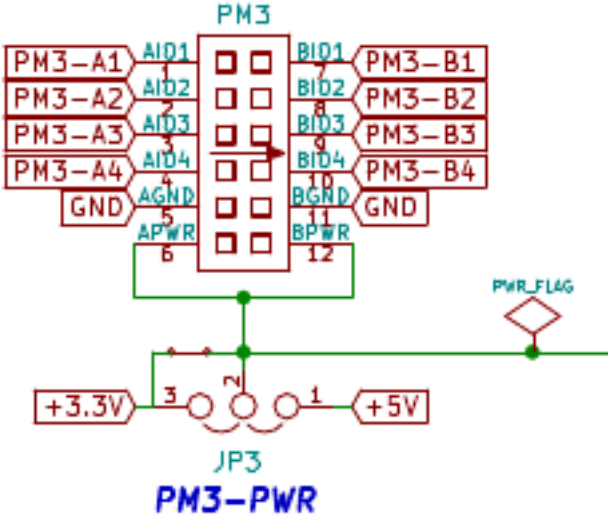


2.) The 2nd issue is the PMOD connections to FPGA are different.
3.) Third, I do not have a Diglient PMOD 4 push button switch module.
4.) The 4th issue is the PHASE LOCK LOOP difference.

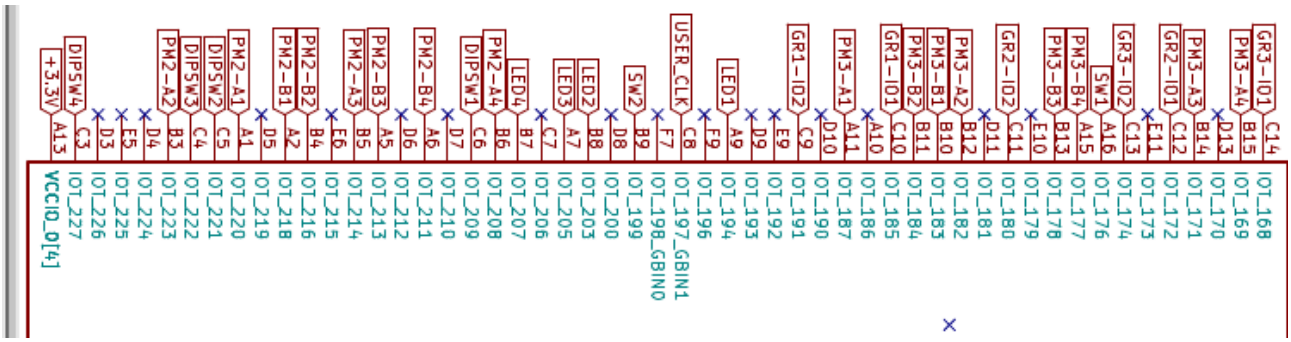
Post on #yosys

Pin C8 is my USER_CLK comes from a 100MHz osc. It is connected to IOT_197_GBIN1 on HX8K. When I try using it for as an input to PLL I get the fatal error: bad constraint on `i_clk': no PLL at pin C8.
Can only certain pins be used as inputs to PLL?
daveshah
develonepi3: use the SB_PLL40_CORE instead of SB_PLL40_PAD variant (and REFERENCECLK in instead of PACKAGEPIN)

```
set_io clk_100mhz C8    #R9

set_io pmod1_1 A11      #D8
set_io pmod1_2 B12      #B9
set_io pmod1_3 B14      #B10
set_io pmod1_4 B15      #B11
#   654321      catboard    #   654321  icoboard
#       xxxxxx  PMOD3 A         #       xxxxxx  PMOD1 A
#       xxxxxx  PMOD3 B         #       xxxxxx  PMOD1 B
#   654321                      #   654321
#
set_io pmod1_7 B10      #B8
set_io pmod1_8 B11      #A9
set_io pmod1_9 B13
#A10
set_io pmod1_10 A15
#A11
```



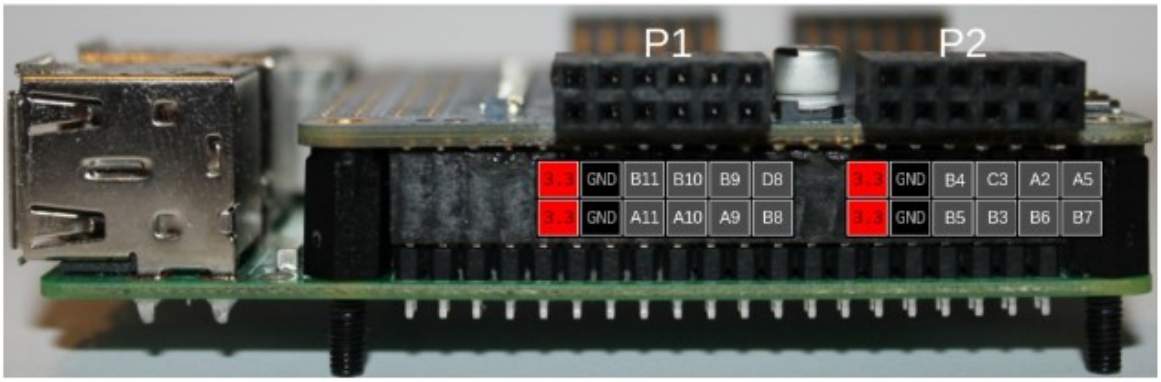
CATBOARD connection to FPGA pins PMOD 2 & PMOD 3 push button switches, dip switch, and leds.



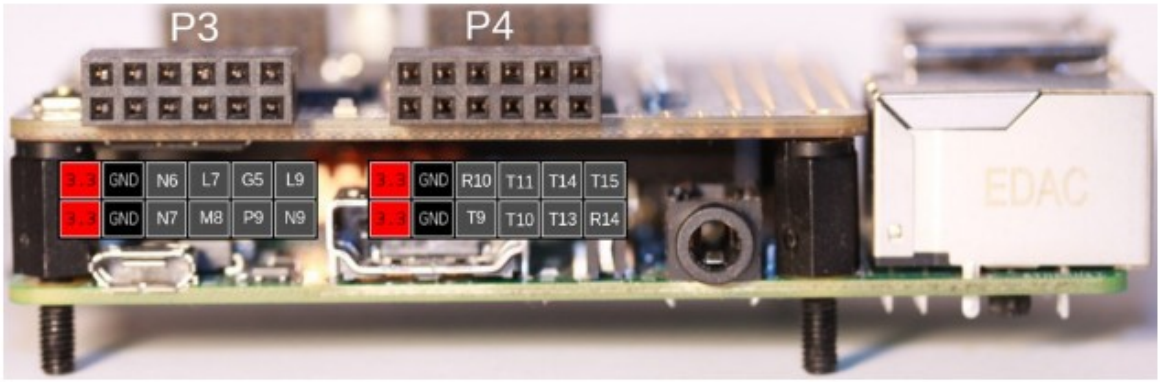
In top.v

```
module top(clk_100mhz, pmod1_1, pmod1_2, pmod1_3, pmod1_4, pmod1_7, pmod1_8,
  pmod1_9, pmod1_10, pmod2_7, pmod2_8, pmod2_9, pmod2_10, rpi_sck, rpi_cs,
  rpi_mosi);

input rpi_sck, rpi_cs, rpi_mosi;
rpi_sck
rpi_cs
rpi_mosi

spi_ram_slave spi_ram_slave(clk, rpi_sck, rpi_cs, rpi_mosi,
  ram_addr, ram_data, ram_wr);
module spi_ram_slave(clk, sck, cs, mosi, ram_addr, ram_data, ram_wr);
PMOD pin out on  icoboard
```

Pinout Pmod P1 and P2



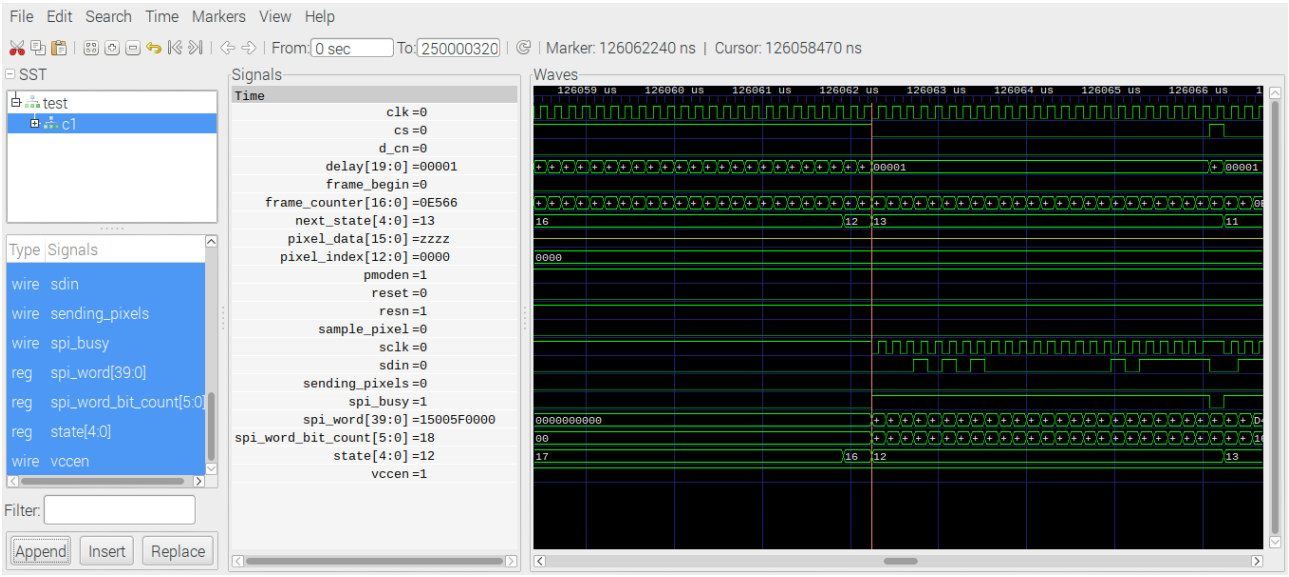
Pinout PMOD P3 and P4



"cd otl-icoboard-pmodoledrgb-demo/fw"

"make"

"make simulate-pmodoledrgb_controller" Creates the VCD file pmodoledrgb_controller.vcd .



"make simulate-spi_ram_slave" Creates the VCD file spi_ram_slave.vcd.