

\*\*\*\*\*DRAFT\*\*\*\*\*

## *Adapting the OLED designed for the ICOWBOARD to the CATBOARD*

05/28/18

\*\*\*\*\*DRAFT\*\*\*\*\*

The youtube video <https://www.youtube.com/watch?v=UMDcnwZA2YE> describes the interface between an OLED display and the ICOWBOARD.

**Goal of this effort:** Is to perform the same functions using the CATBOARD instead of the ICOWBOARD.

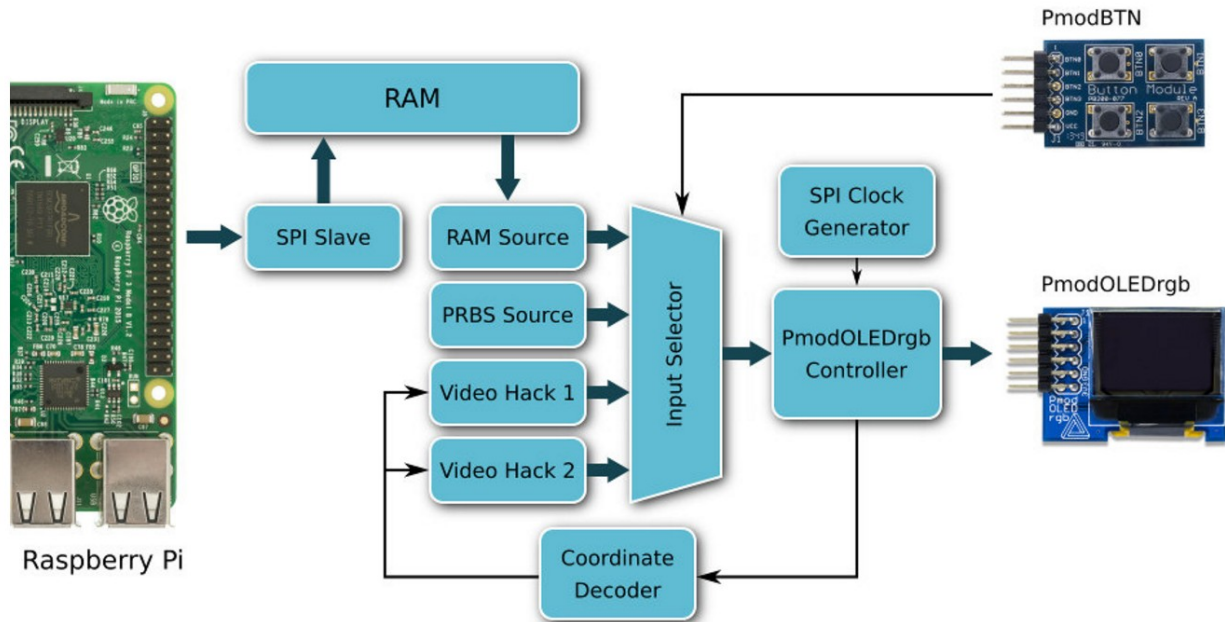
## otl-icowboard-pmodoldergb-demo

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Design Block Diagram

## Design Structure



First forked the repository <https://github.com/jhol/otl-icoboard-pmodoledrgb-demo>

***git clone <https://github.com/develone/otl-icoboard-pmodoledrgb-demo.git>***

***“cd otl-icoboard-pmodoledrgb-demo/”***

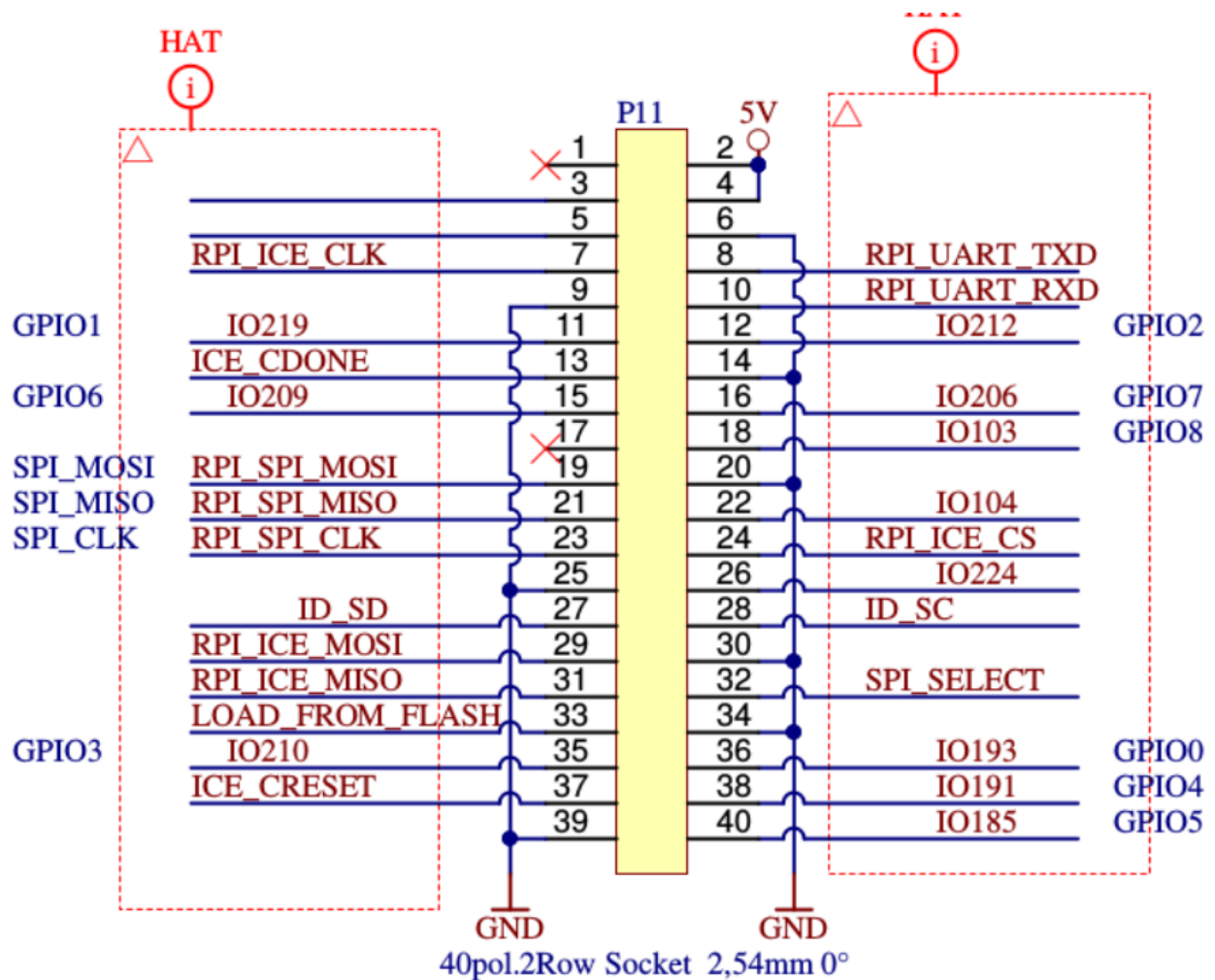
Need to create a new branch to track the changes required for the CATBOARD.

***“git branch catboard”***

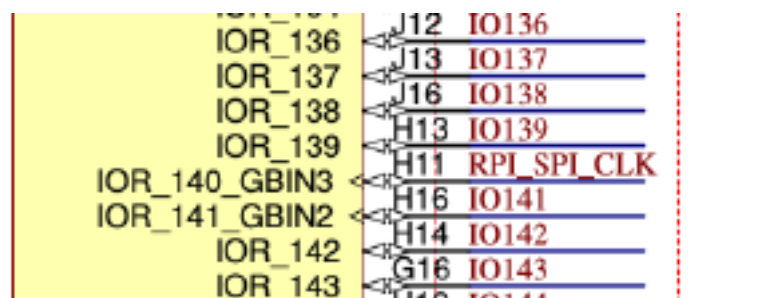
Even though the FPGAs ice40 HX8K are same for the CATBOARD and the ICOBOARD.

1.) The first issue is the interface between the Raspberry Pi and FPGA hat.

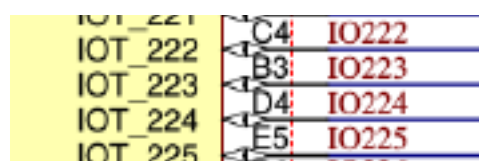
ICOBOARD RPi



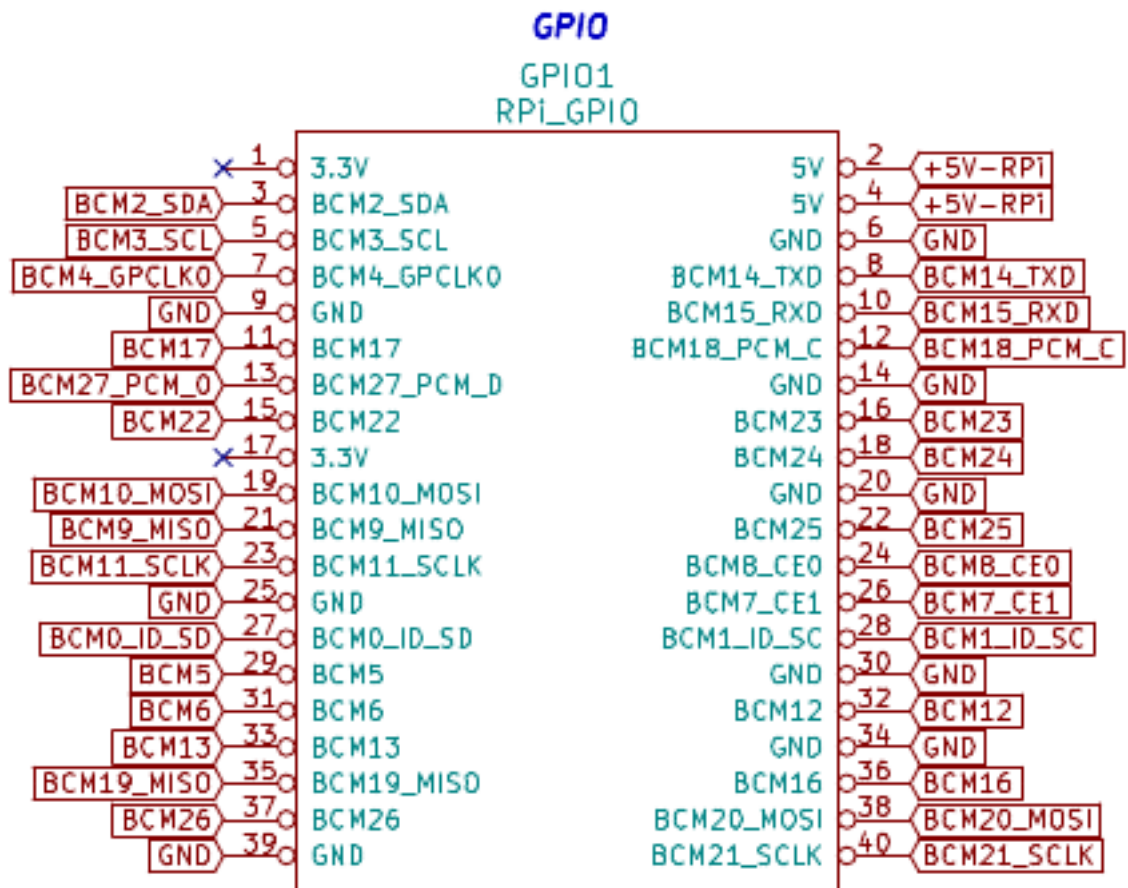
RPI\_SPI\_CLK H11 Pin 23 Pi icoboard



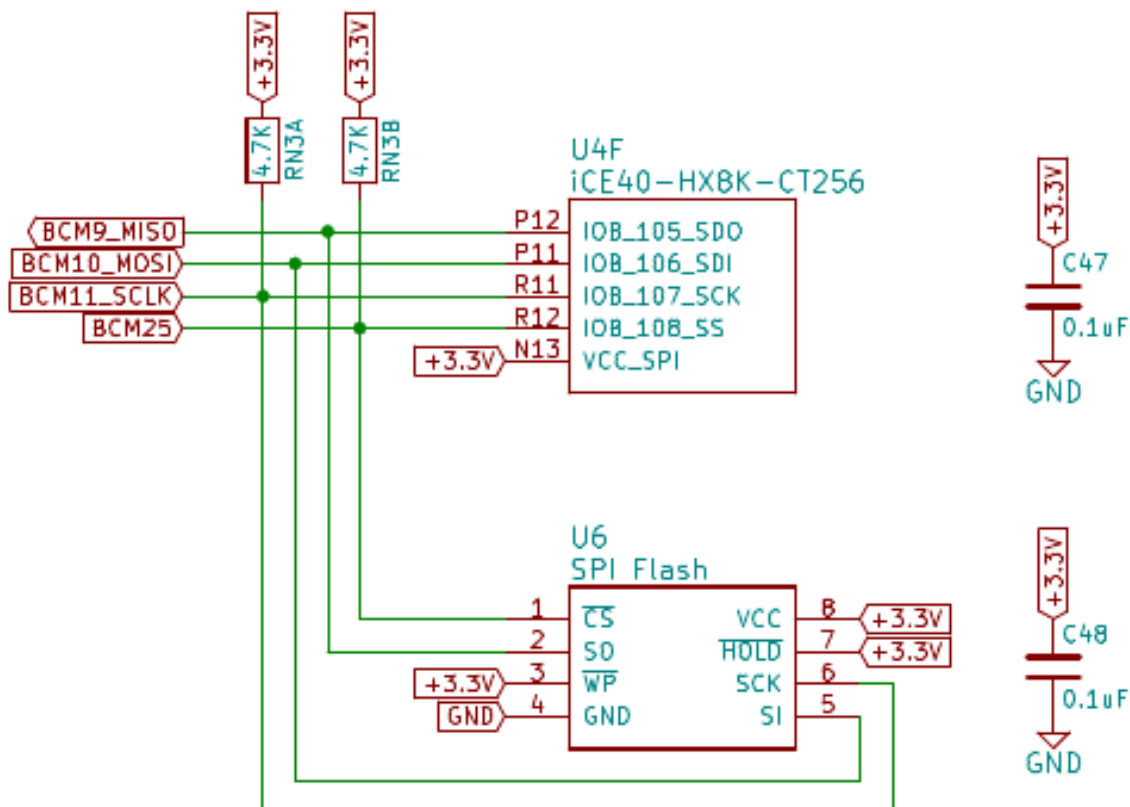
rpi\_cs D4 IOT\_224 Pin 26 Pi icoboard



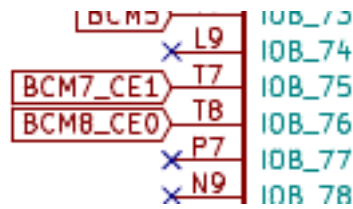
CATBOARD RPi



BCM11\_SCLK Pin 23 CATBOARD



## BCM7\_CE1 Pin 26 CATBOARD



- 2.) The 2<sup>nd</sup> issue is the PMOD connections to FPGA are different.
- 3.) Third, I do not have a Digilent PMOD 4 push button switch module.
- 4.) The 4<sup>th</sup> issue is the PHASE LOCK LOOP difference.

Post on #yosys

*Pin C8 is my USER\_CLK comes from a 100MHz osc. It is connected to IOT\_197\_GBIN1 on HX8K. When I try using it for as an input to PLL I get the fatal error: bad constraint on `i\_clk': no PLL at pin C8.*

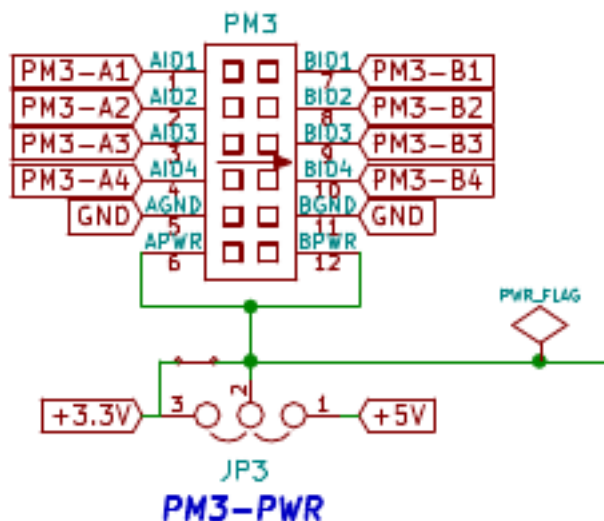
*Can only certain pins be used as inputs to PLL?*

*daveshah*

*develonepi3: use the SB\_PLL40\_CORE instead of SB\_PLL40\_PAD variant (and REFERENCECLK in instead of PACKAGEPIN)*

set\_io clk\_100mhz C8 #R9

```
set_io pmod1_1 A11 #D8
set_io pmod1_2 B12 #B9
set_io pmod1_3 B14 #B10
set_io pmod1_4 B15 #B11
# 654321 catboard # 654321 icoboard
# xxxxxx PMOD3 A # xxxxxx PMOD1 A
# xxxxxx PMOD3 B # xxxxxx PMOD1 B
# 654321 # 654321
#
set_io pmod1_7 B10 #B8
set_io pmod1_8 B11 #A9
set_io pmod1_9 B13
#A10
set_io pmod1_10 A15
#A11
```



GR3-101	C14	I01.168	
PM3-A4	B15	I01.169	
PM3-A3	D13	I01.170	
GR2-101	C12	I01.171	
	E11	I01.172	
GR3-102	C13	I01.173	
	F6	I01.174	
15W1	A16	I01.176	
PM3-B4	B13	I01.177	
PM3-B3	A15	I01.178	
	E10	I01.179	
GR2-102	C11	I01.180	
	D11	I01.181	
PM3-A2	B12	I01.182	
PM3-B1	B10	I01.183	
PM3-B2	B11	I01.184	
GR1-101	C10	I01.185	
	A10	I01.186	
PM3-A1	A11	I01.187	
	D10	I01.190	
GR1-102	C9	I01.191	
	E9	I01.192	
	D9	I01.193	
LED1	A9	I01.194	
	F9	I01.196	
USER_CLK	C8	I01.197 GBIN1	
	F7	I01.198 GBIN0	
5W2	B9	I01.199	
	D8	I01.200	
LED2	B8	I01.203	
LED3	A7	I01.205	
	C7	I01.206	
LED4	B7	I01.207	
PM2-A4	B6	I01.208	
DIPSW1	C6	I01.209	
	D7	I01.210	
PM2-B4	A6	I01.211	
	D6	I01.212	
PM2-B3	A5	I01.213	
PM2-A3	B5	I01.214	
	F6	I01.215	
PM2-B2	B4	I01.216	
PM2-B1	A2	I01.218	
	D5	I01.219	
PM2-A1	A1	I01.220	
DIPSW2	C4	I01.221	
DIPSW3	B3	I01.222	
PM2-A2	B3	I01.223	
	D4	I01.224	
	F5	I01.225	
	D3	I01.226	
DIPSW4	C3	I01.227	
+3.3V	A13		
VCCIO_0[14]			

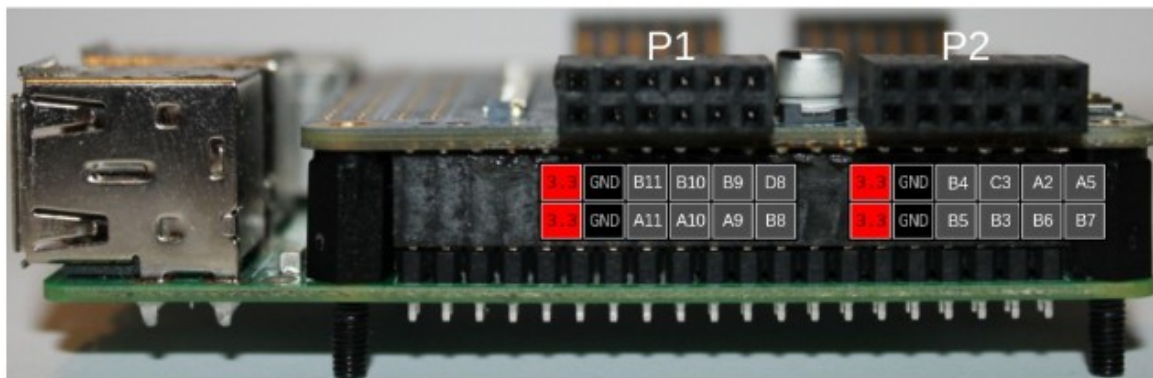
```
module top(clk_100mhz, pmod1_1, pmod1_2, pmod1_3, pmod1_4, pmod1_7, pmod1_8,
pmod1_9, pmod1_10, pmod2_7, pmod2_8, pmod2_9, pmod2_10, rpi_sck, rpi_cs,
rpi_mosi);
```

rpi\_mosi

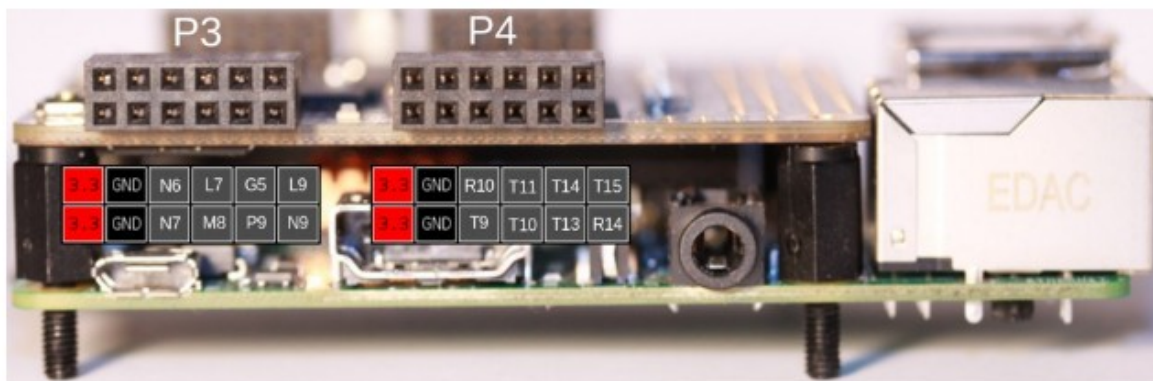
```
module spi_ram_slave(clk, sck, cs, mosi, ram_addr, ram_data, ram_wr);
PMOD pin out on icoboard
```



Pinout Pmod P1 and P2



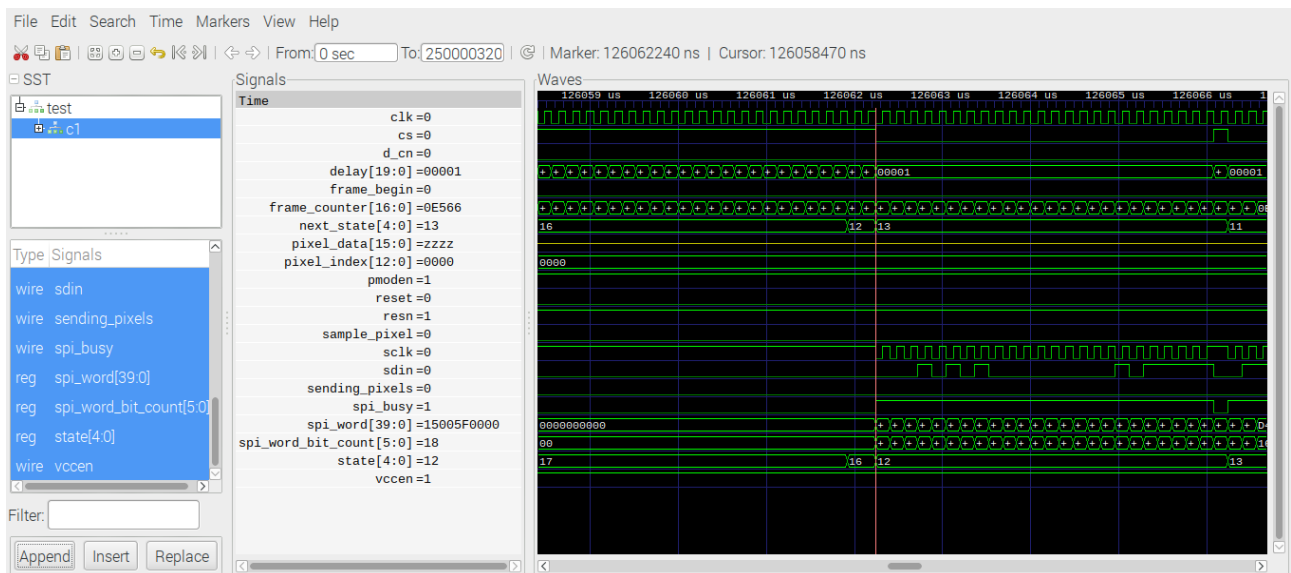
Pinout PMOD P3 and P4



***“cd otl-icoboard-pmodoledrgb-demo/fw”***

***“make”***

***“make simulate-pmodoledrgb\_controller”*** Creates the VCD file *pmodoledrgb\_controller.vcd* .



***“make simulate-spi\_ram\_slave”*** Creates the VCD file spi\_ram\_slave.vcd.

