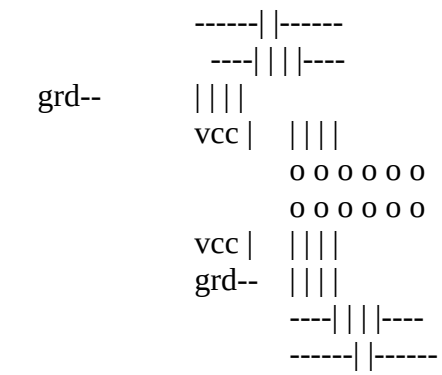
**********Default**********
PipelineC Ethernet PMOD
02/15/25

**********Default**********

02/13/25



02/15/25
**********pi5-80**********
export PIPELINEC_REPO="$HOME/PipelineC"
export OSS_CAD_SUITE=$HOME/oss-cad-suite/
export PATH="$HOME/.pyenv/bin:$HOME/local/openocd/bin:$PATH"

devel@pi5-70:~/PipelineC $
devel@pi5-80:~/PipelineC $ git log
commit ff24c29192f5a479eed5e34c54ba3eabc5d1ec67 (HEAD -> test-dev, origin/test-dev)
Merge: cb8e24b 707142c
Author: develone <develone@sbcglobal.net>
Date: Fri Feb 14 20:25:24 2025 -0700

    Merge branch 'JulianKemmerer:master' into test-dev

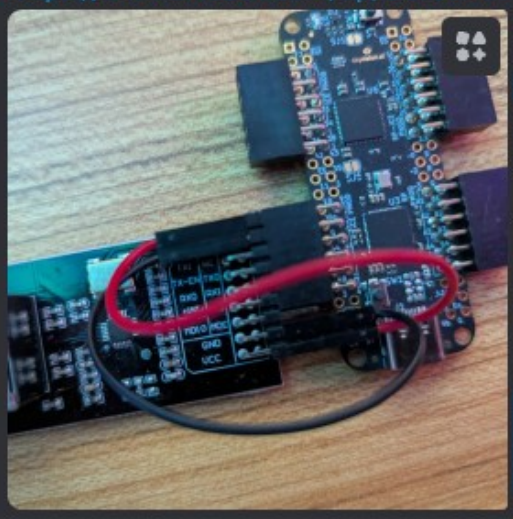
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ make clean
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ ls
eth_clocks.py ethernet_top.sv Makefile README.md top.h top.sv
ethernet_top.c ice40.pcf pong_top.c top.c top_pins.svh
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ make pipelinec
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec top.c --top pipelinec_top --out_dir pipelinec_output --comb --no_synth > pipelinec.log

```
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ make gateware.bin
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -q -m ghdl -p "ghdl --std=08 -frelaxed `cat
pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv top.sv pll.v; synth_ice40 -top top
-json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -q --randomize-seed --up5k --package sg48 --pcf
ice40.pcf --json gateware.json --asc gateware.asc --freq 25.0
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ bin2uf2 -o
gateware.uf2 gateware.bin
**********pi5-70**********
devel@pi5-70:~/PipelineC $
commit ff24c29192f5a479eed5e34c54ba3eabc5d1ec67 (HEAD -> test-dev, origin/test-dev)
Merge: cb8e24b 707142c
Author: develone <develone@sbcglobal.net>
Date:   Fri Feb 14 20:25:24 2025 -0700

    Merge branch 'JulianKemmerer:master' into test-dev

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ ls
eth_clocks.py    gateware.uf2      pll_clk_mhz.h  top_pins.svh
ethernet_top.c   ice40.pcf         pll.v          top.sv
ethernet_top.sv  lextab.py         pong_top.c     yacctab.py
gateware.asc     Makefile          README.md      yosys_stderr.log
gateware.bin     pipelinec.log     top.c
gateware.json    pipelinec_output  top.h

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ make clean
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ make pipelinec
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec top.c --top pipelinec_top --out_dir pipelinec_output --comb --
no_synth > pipelinec.log
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ make gateware.bin
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -q -m ghdl -p "ghdl --std=08 -frelaxed `cat
pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv top.sv pll.v; synth_ice40 -top top
-json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -q --randomize-seed --up5k --package sg48 --pcf
ice40.pcf --json gateware.json --asc gateware.asc --freq 25.0
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $ bin2uf2 -o
gateware.uf2 gateware.bin
```

absurdfatalism Yesterday at 6:06 PM

Yay confirmed this ethernet phy pmod-like thing works with pico ice and # pipelinec 🙌

https://www.amazon.com/dp/B07S8MRH92?ref=ppx_yo2ov_dt_b_fed_asin_title&th=1

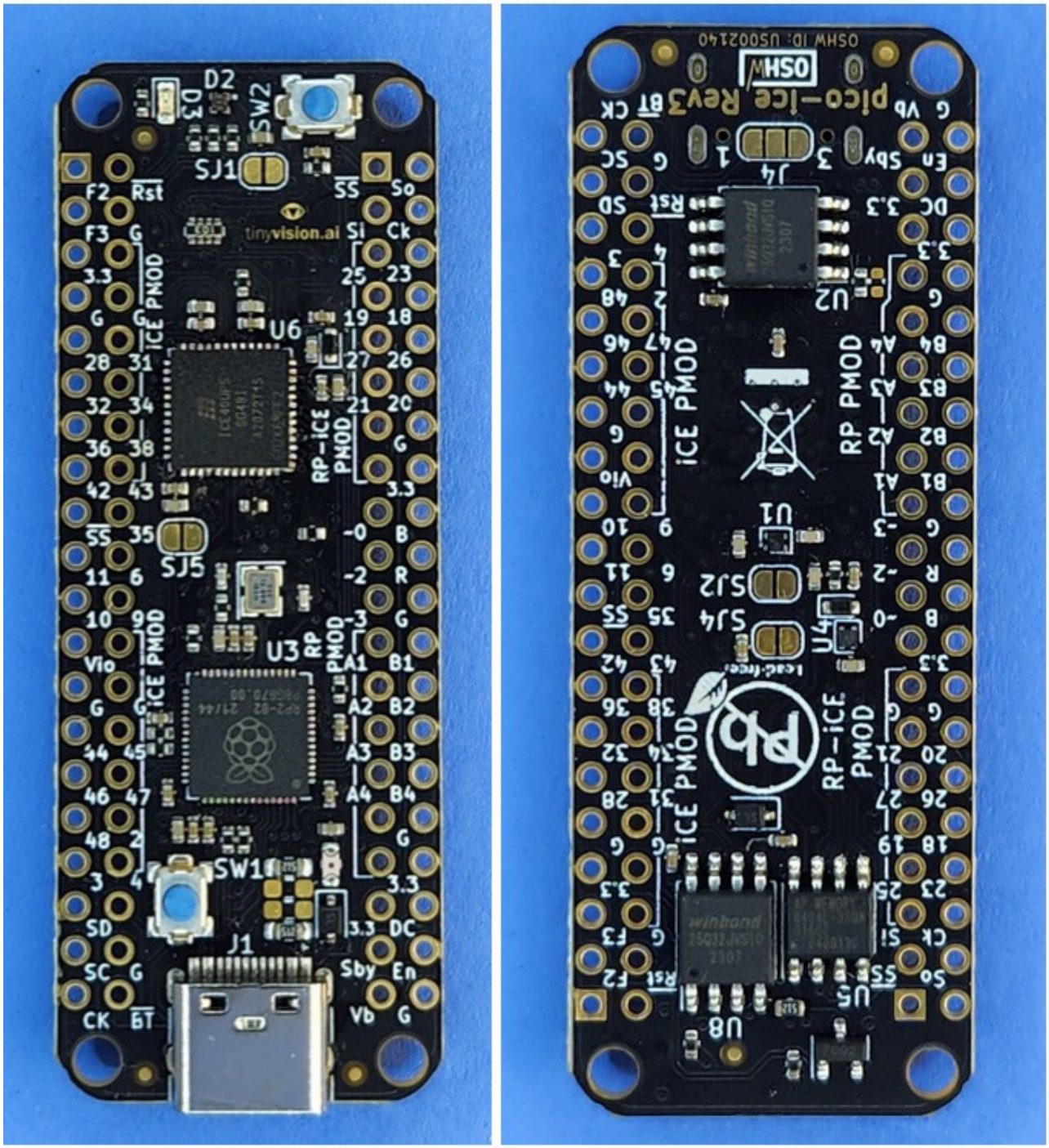


The FPGA is just passing through frames that match a specific MAC address, that a0:b1 etc one in image

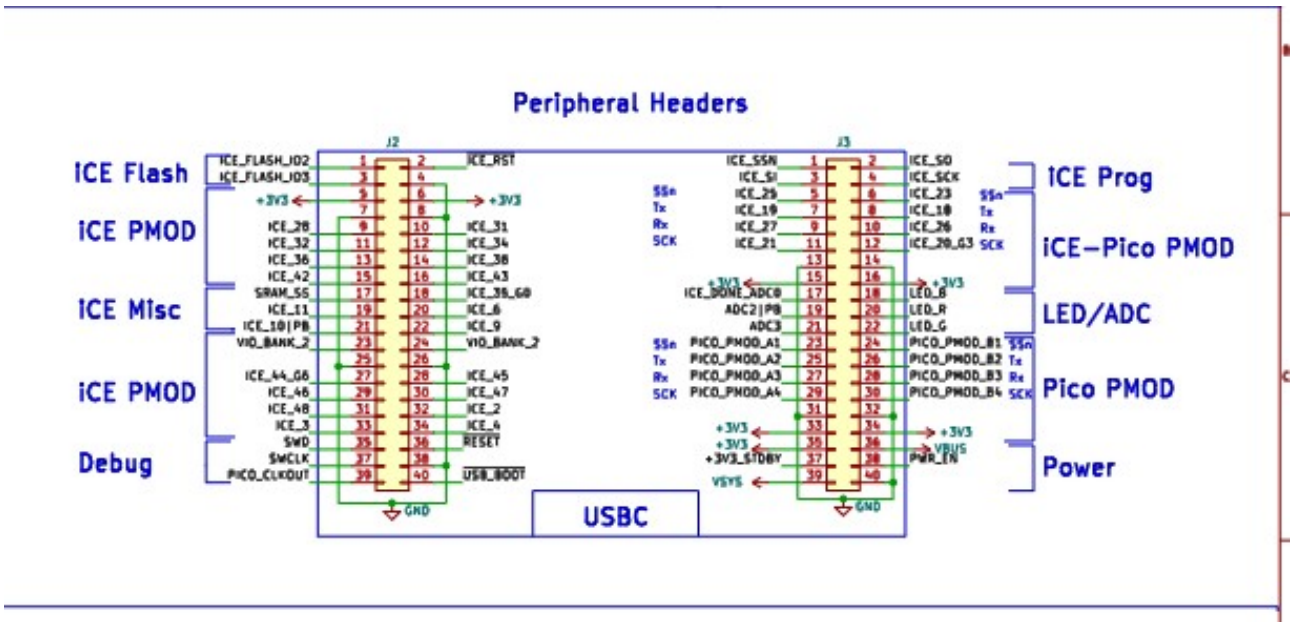
parses the ethernet header src and dst mac

and sends the frame back to where it came

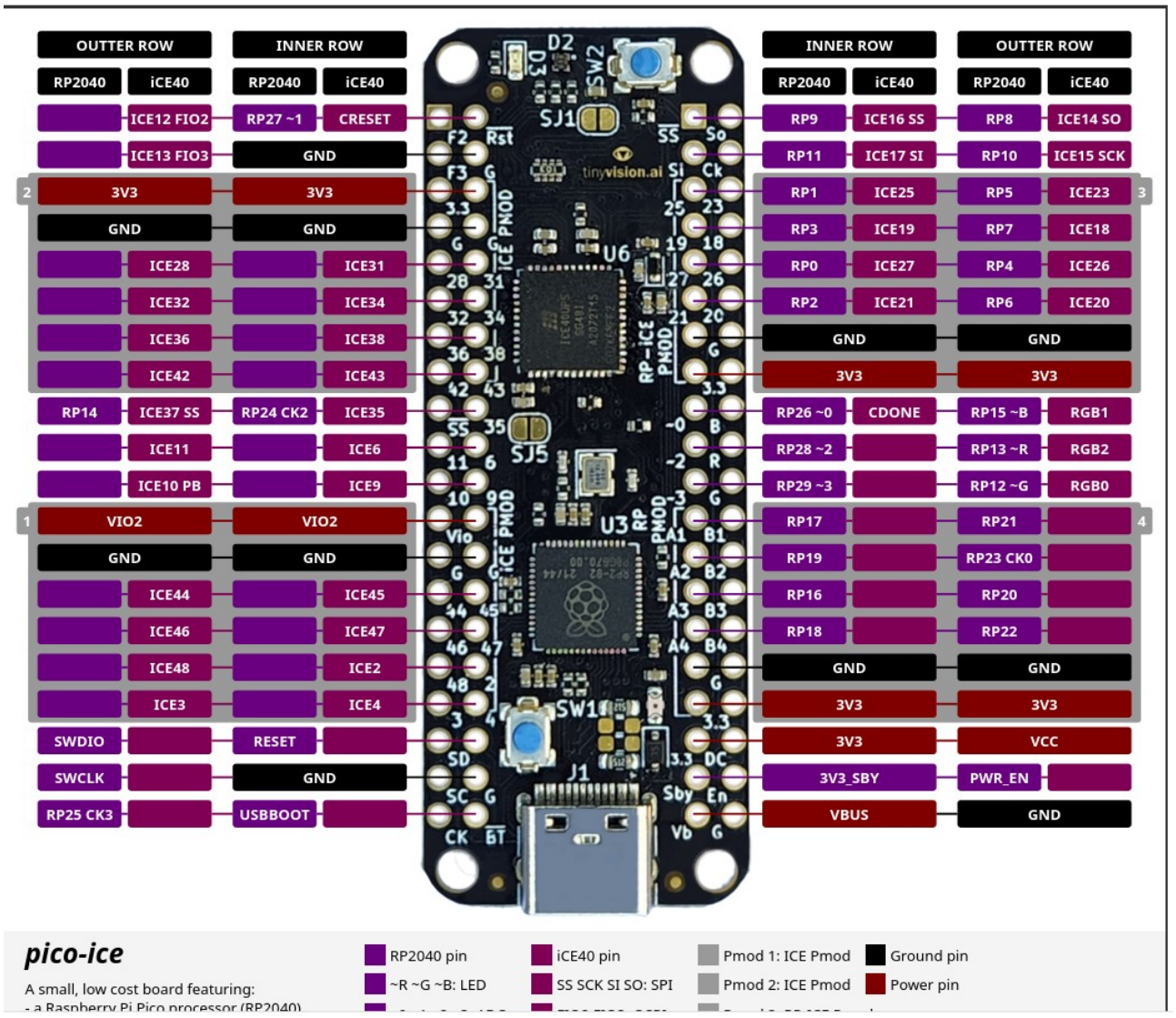
xx


D2
D3
SW2
SJ1
F2
Rst
SS
So
F3
G
tinyvision.ai
Si
Ck
3.3
ICE PMOD
25
23
U6
19
18
28
31
27
26
32
34
21
20
RP-ICE PMOD
36
38
G
42
43
3.3
SS
35
SJ5
-0
B
11
6
-2
R
10
9
-3
G
Vio
U3
RP PMOD
A1
B1
G
A2
B2
44
45
A3
B3
46
47
A4
B4
48
2
G
3
4
SW1
3.3
SD
3.3
DC
J1
SC
G
Sby
En
CK
BT
Vb
G
OSHW ID: US002140
OSHW
pico-ice Rev3
BT
CK
G
Vb
J4
1
3
Sby
En
G
SC
SD
Rst
DC
3.3
U2
3
3.3
4
2
48
G
47
46
A4
B4
ICE PMOD
RP PMOD
45
44
A3
B3
G
A2
B2
Vio
U1
9
10
A1
B1
-3
G
SJ2
6
11
-2
R
SJ4
SS
35
U4
-0
B
43
42
3.3
38
36
G
32
34
RP-iCE PMOD
20
21
31
28
26
27
G
18
19
3.3
23
25
F3
G
CK
SI
Rst
F2
SS
SO
U5
U8

xx


Peripheral Headers
ICE Flash
iCE PMOD
iCE Misc
iCE PMOD
Debug
ICE Prog
iCE–Pico PMOD
LED/ADC
Pico PMOD
Power
USBC
J2
J3

XX


OUTTER ROW
INNER ROW
INNER ROW
OUTTER ROW
RP2040
iCE40
ICE12 FIO2
ICE13 FIO3
3V3
GND
ICE28
ICE32
ICE36
ICE42
RP14
ICE37 SS
ICE11
ICE10 PB
VIO2
GND
ICE44
ICE46
ICE48
ICE3
SWDIO
SWCLK
RP25 CK3
RP27 ~1
CRESET
GND
3V3
GND
ICE31
ICE34
ICE38
ICE43
RP24 CK2
ICE35
ICE6
ICE9
VIO2
GND
ICE45
ICE47
ICE2
ICE4
RESET
GND
USBBOOT
RP9
ICE16 SS
RP11
ICE17 SI
RP1
ICE25
RP3
ICE19
RP0
ICE27
RP2
ICE21
GND
3V3
RP26 ~0
CDONE
RP28 ~2
RP29 ~3
RP17
RP19
RP16
RP18
GND
3V3
3V3
3V3_SBY
VBUS
RP8
ICE14 SO
RP10
ICE15 SCK
RP5
ICE23
RP7
ICE18
RP4
ICE26
RP6
ICE20
GND
3V3
RP15 ~B
RGB1
RP13 ~R
RGB2
RP12 ~G
RGB0
RP21
RP23 CK0
RP20
RP22
GND
3V3
VCC
PWR_EN
GND
tinyvision.ai
pico-ice
A small, low cost board featuring:
RP2040 pin
~R ~G ~B: LED
iCE40 pin
SS SCK SI SO: SPI
Pmod 1: ICE Pmod
Pmod 2: ICE Pmod
Ground pin
Power pin