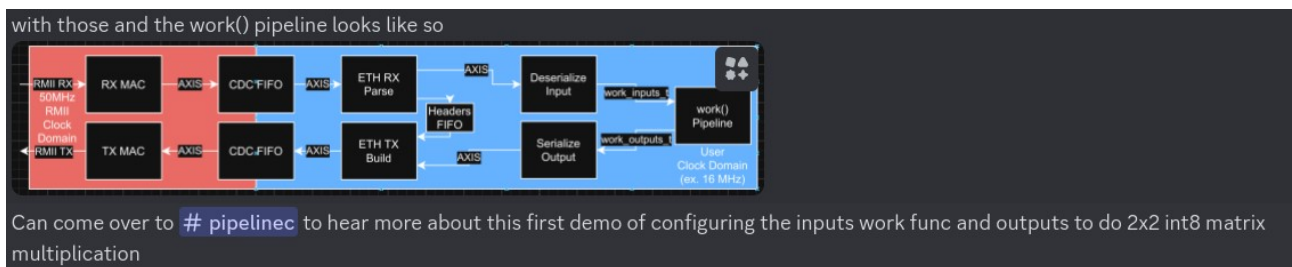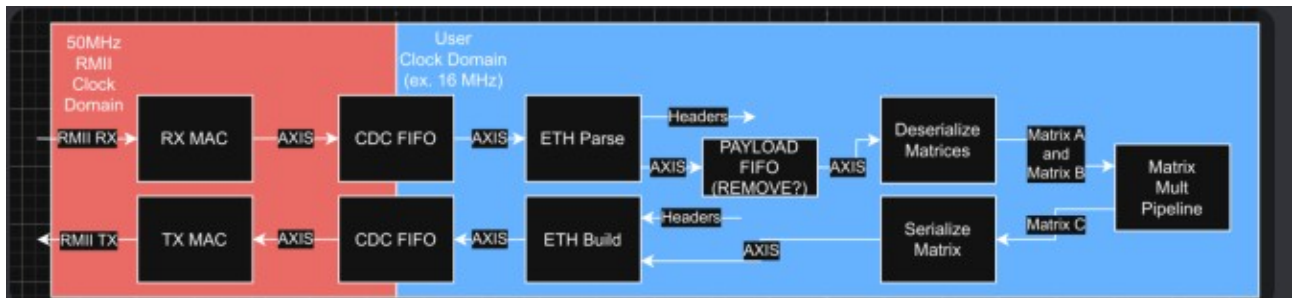**PipelineC PMOD Ethernet connected to a pico-ice**
03/06/25

The current image which does work in the form matrix multiply.

Tested 03/06/25 in pico-ice repo branch test-dev-100424 in two shell below.
Following **"git clone https://github.com/develone/pico-ice.git -b test-dev-100424"**

If the command in the left image below is done before the command in right image below.

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/net $ **./compile-work_test.sh**

In file included from work_test.c:30:
work.h:26:10: **fatal error:** type_bytes_t.h/work_inputs_t_bytes_t.h/work_inputs_t_bytes.h: No
such file or directory
   26 | #include **"type_bytes_t.h/work_inputs_t_bytes_t.h/work_inputs_t_bytes.h"**
      | ^~~~~~~
compilation terminated.

make clean all TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"

rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
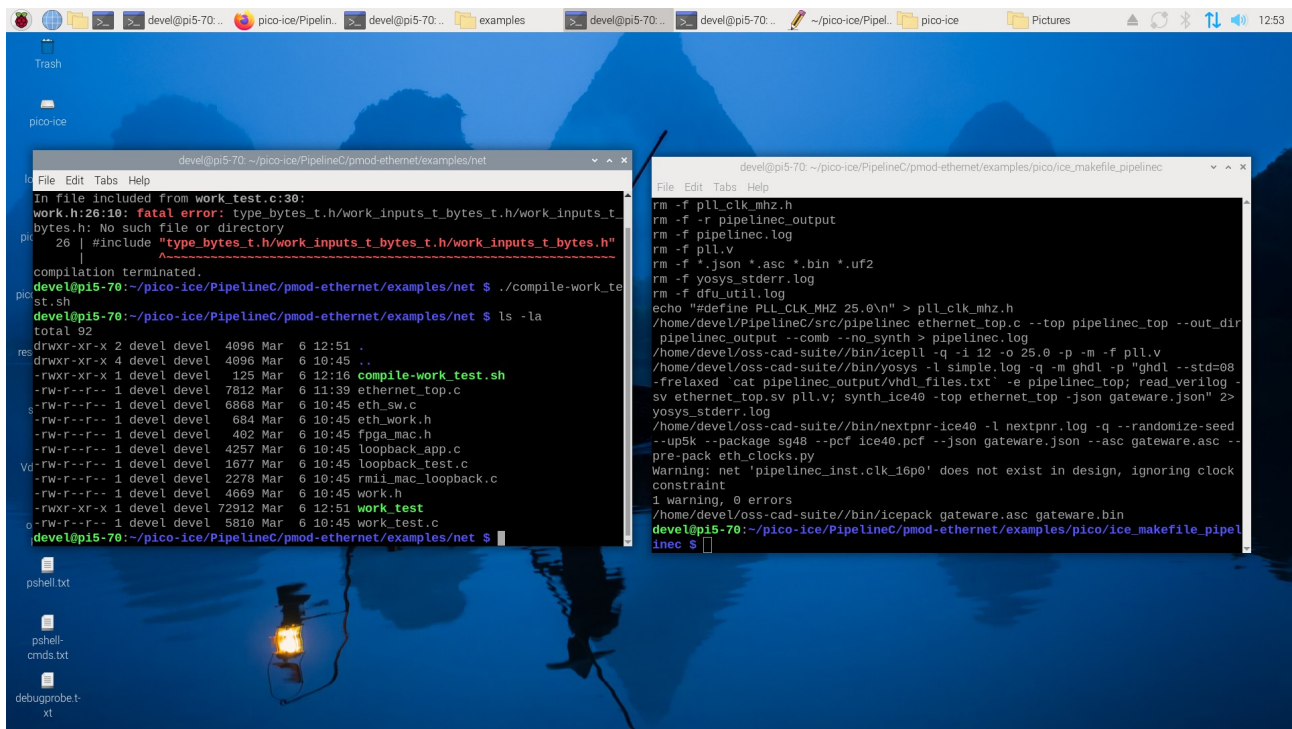**rm -f pipelinec.log**
rm -f pll.v

```
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec ethernet_top.c --top pipelinec_top --out_dir
pipelinec_output --comb --no_synth > pipelinec.log
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -l simple.log -q -m ghdl -p "ghdl --std=08 -frelaxed `cat
pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv ethernet_top.sv pll.v;
synth_ice40 -top ethernet_top -json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -l nextpnr.log -q --randomize-seed --up5k --
package sg48 --pcf ice40.pcf --json gateware.json --asc gateware.asc --pre-pack eth_clocks.py
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/pico/ice_makefile_pipelinec $
bin2uf2 -o gateware.uf2 gateware.bin

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/pico/ice_makefile_pipelinec $ scp
gateware.uf2 pi5-90:/media/devel/pico-ice/
gateware.uf2                     100%  204KB  10.4MB/s   00:00

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/net $ ./compile-work_test.sh

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/net $ sudo ./work_test
CPU threads: 1
n 'work()'s: 1
Total tx bytes: 8
Total rx bytes: 4
CPU took 0.000290 seconds to execute
CPU iteration time: 0.000290 seconds
CPU bytes per sec: 41391.157895 B/s
FPGA took 0.000207 seconds to execute
FPGA iteration time: 0.000207 seconds
FPGA bytes per sec: 57985.769585 B/s
Speedup: 1.400922
```

This image was loopback tested on 02/17/25

this is what the current design implements

50MHz RMII Clock Domain

User Clock Domain (ex. 16 MHz)

RMII RX → RX MAC → AXIS → CDC FIFO → AXIS → ETH Parse → HEADER FIFO

RMII TX ← TX MAC ← AXIS ← CDC FIFO ← AXIS ← ETH Build ← PAYLOAD FIFO

AXIS buses are 8b wide
user clock could be as low as 50M/4 = 12.5M
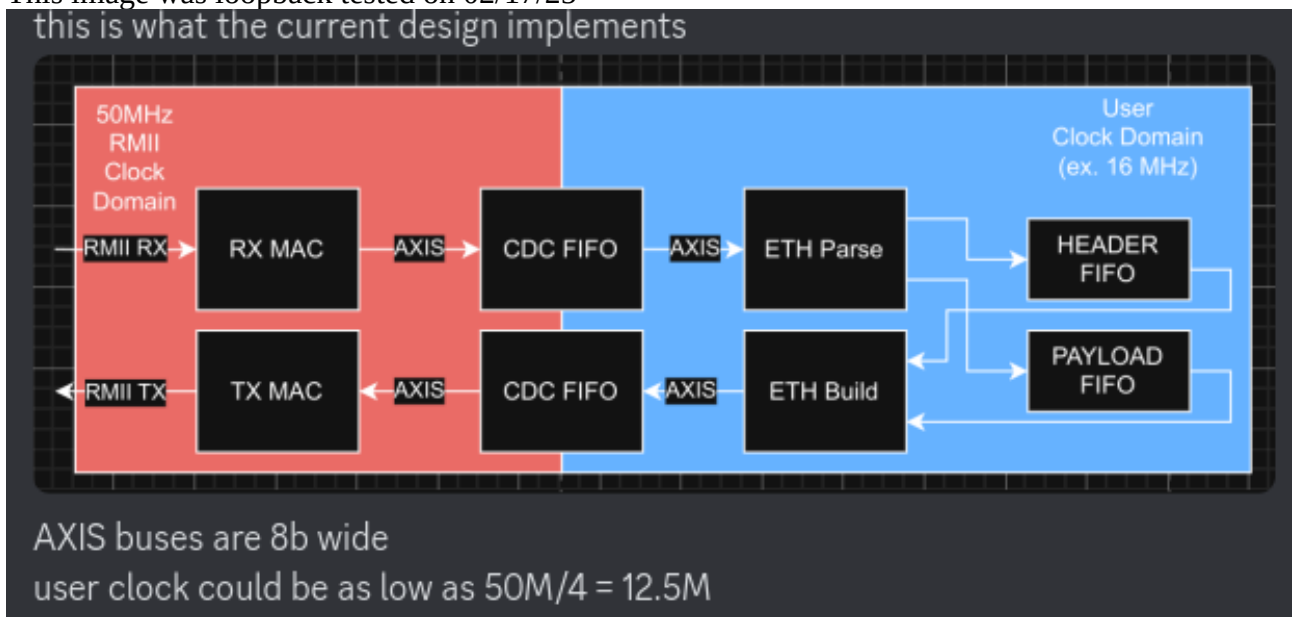
pico-ice Running gateware.bin provided by Discord user absurfatalism. Led blink red.
This was fixed with added make parameters.
make clean
make pipelinec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
make gateware.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
bin2uf2 -o gateware.uf2 gateware.bin
scp gateware.uf2 pi5-90:/media/devel/pico-ice/

3.3 grd A4 A3 A2 A1

□ □ □ □ □ □
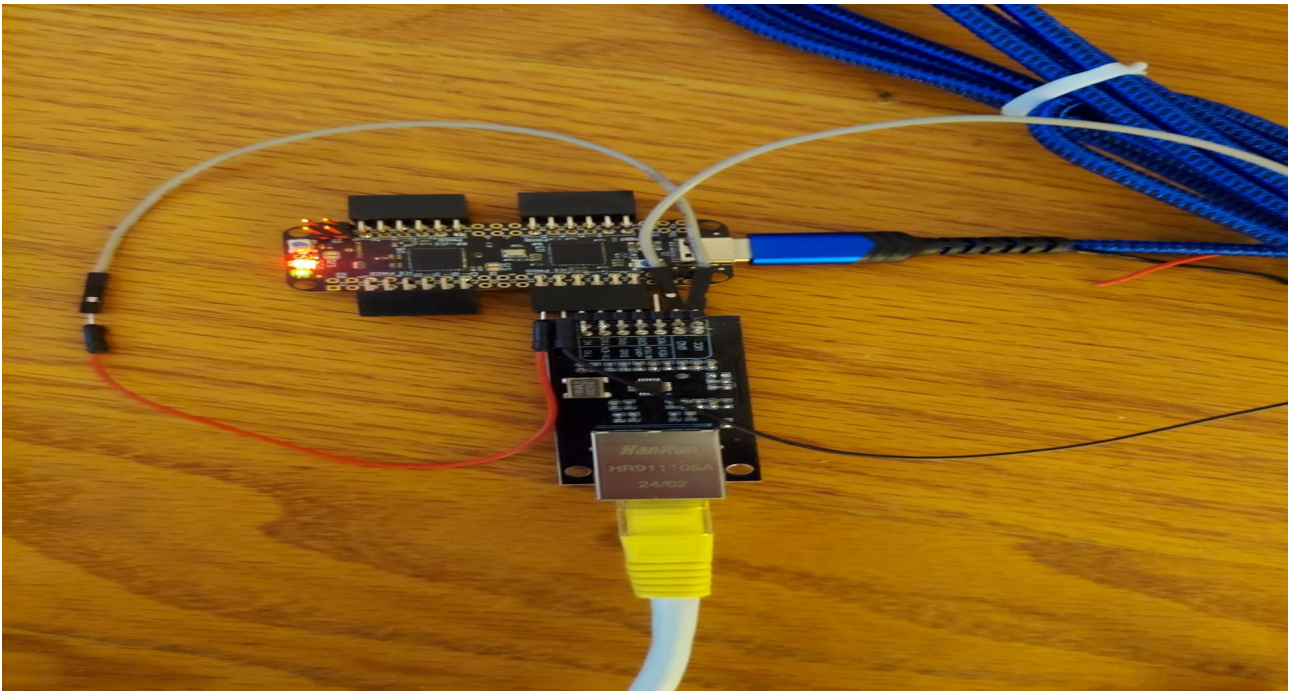
pico-ice

3.3 grd A4 A3 A2 A1

□ □ □ □ □ □

□ □ □ □ □ □

□ □ □ □ □ □

3.3 grd B4 B3 A2 B1

3.3 grd B4 B3 B2 B1

A1-43   B1-42
A2-38   B2-36
A3-34   B3-32
A4-31   B4-28

A1-4   B1-3
A2-2   B2-48
A3-47   B3-46
A4- 45   B4-44

USB

xx

pico-ice

A small, low cost board featuring:
- a Raspberry Pi Pico processor (RP2040)

OUTTER ROW		INNER ROW			INNER ROW		OUTTER ROW	
RP2040	iCE40	RP2040	iCE40		RP2040	iCE40	RP2040	iCE40
	ICE12 FIO2	RP27 ~1	CRESET		RP9	ICE16 SS	RP8	ICE14 SO
	ICE13 FIO3	GND			RP11	ICE17 SI	RP10	ICE15 SCK
3V3		3V3			RP1	ICE25	RP5	ICE23
GND		GND			RP3	ICE19	RP7	ICE18
	ICE28		ICE31		RP0	ICE27	RP4	ICE26
	ICE32		ICE34		RP2	ICE21	RP6	ICE20
	ICE36		ICE38		GND		GND	
	ICE42		ICE43		3V3		3V3	
RP14	ICE37 SS	RP24 CK2	ICE35		RP26 ~0	CDONE	RP15 ~B	RGB1
	ICE11		ICE6		RP28 ~2		RP13 ~R	RGB2
	ICE10 PB		ICE9		RP29 ~3		RP12 ~G	RGB0
VIO2		VIO2			RP17		RP21	
GND		GND			RP19		RP23 CK0	
	ICE44		ICE45		RP16		RP20	
	ICE46		ICE47		RP18		RP22	
	ICE48		ICE2		GND		GND	
	ICE3		ICE4		3V3		3V3	
SWDIO		RESET			3V3		VCC	
SWCLK		GND			3V3_SBY		PWR_EN	
RP25 CK3		USBBOOT			VBUS		GND	

Legend:
- RP2040 pin
- iCE40 pin
- ~R ~G ~B: LED
- SS SCK SI SO: SPI
- Pmod 1: ICE Pmod
- Pmod 2: ICE Pmod
- Ground pin
- Power pin

raspberry-pi-5 devel@pi5-90:~/PipelineC/examples/arty/src/eth $ sudo ./loopback_test

pico-ice with Ethernet pmod devel@pi5-90:~/PipelineC/examples/arty/src/eth $ sudo ./loopback_test
Test passed!

sch

Peripheral Headers
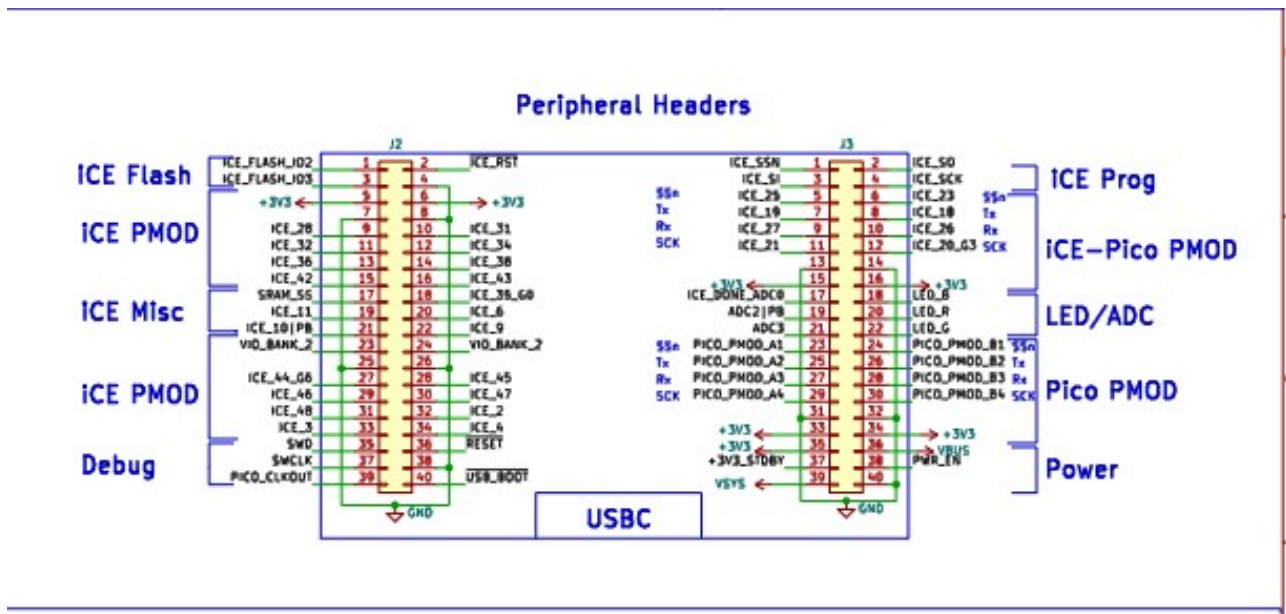
sch

pi5-70 or pi5-80

```
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $
make clean
make pipelinec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
make gateware.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
bin2uf2 -o gateware.uf2 gateware.bin
scp gateware.uf2 pi5-90:/media/devel/pico-ice/
devel@pi5-90:~/PipelineC/examples/arty/src/eth $ sudo ./loopback_test
Test passed!
```