**********Default**********

PipelineC
vga_pll & vga_pong
with UART
01/12/25

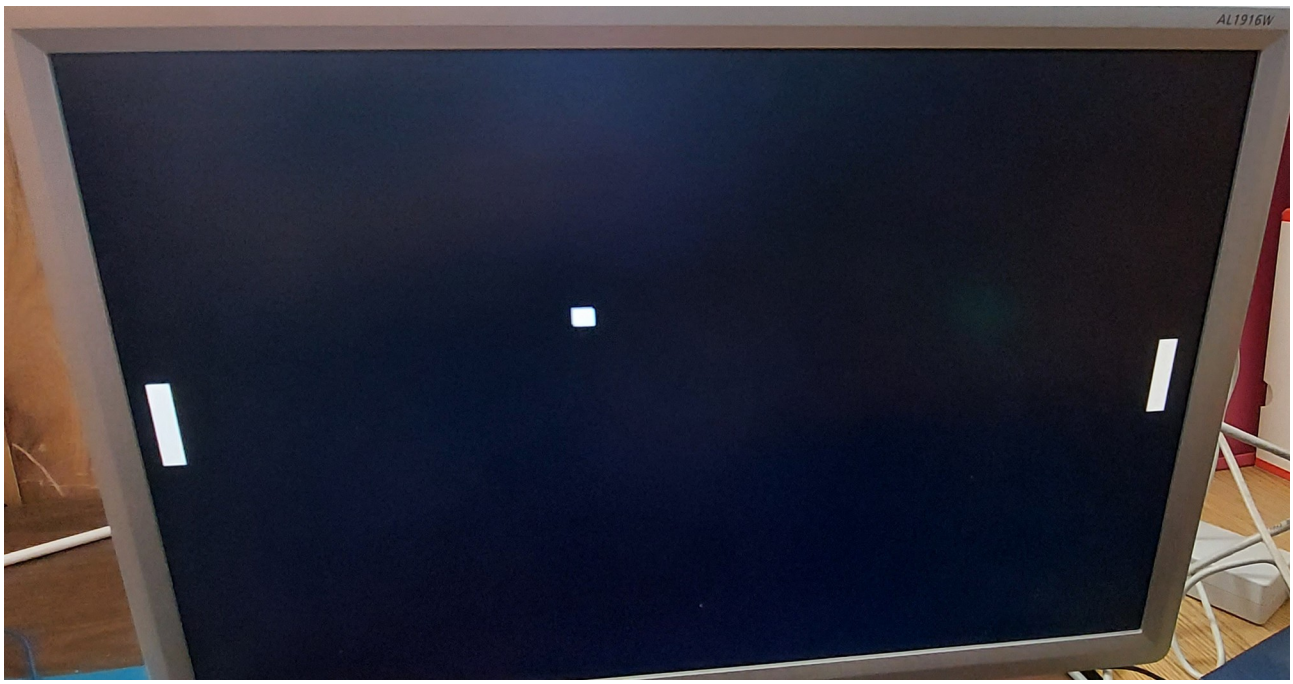
**********Default**********

Testing on 01/12/25
https://discord.com/channels/644405956494753803/985342148884987934/1326366164468895805

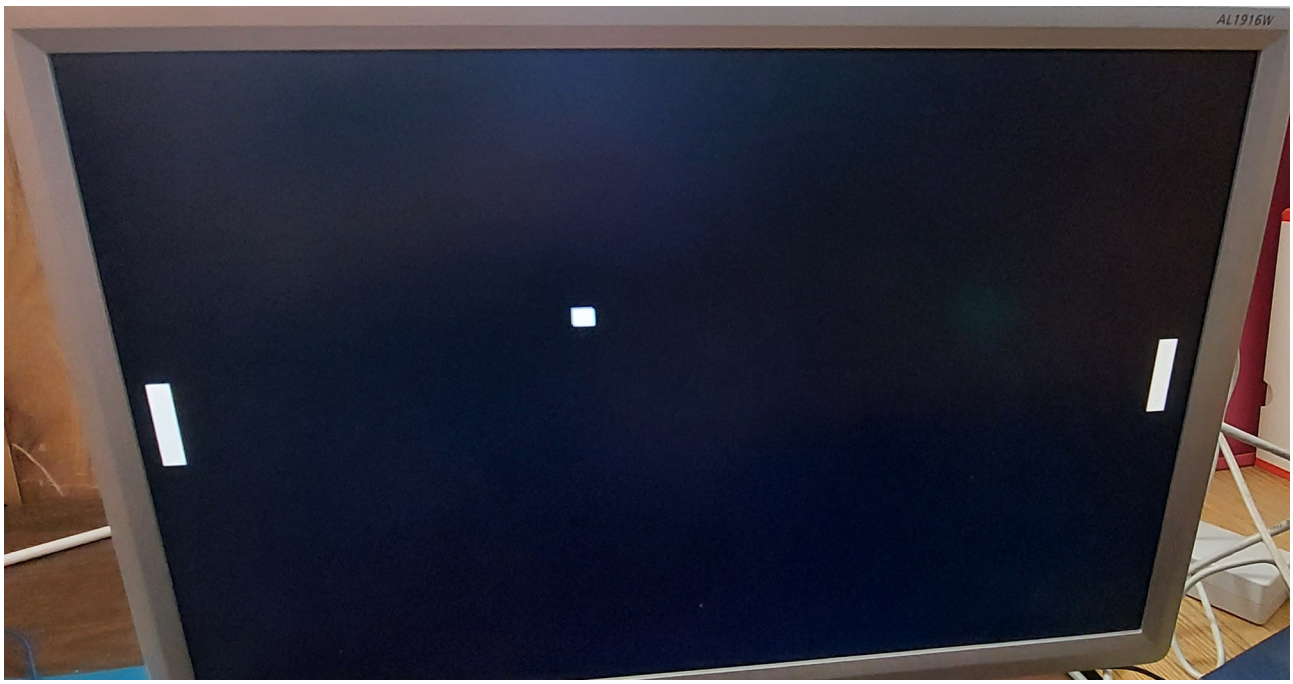
vga_pong works okay in two repos

~/PipelineC/examples/pico-ice/ice_makefile_pipelinec
~/pico-ice/PipelineC/vga-pong/examples/pico-ice/ice_makefile_pipelinec

```
devel@pi5-80:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ make clean
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
devel@pi5-80:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ make pipelinec
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec pong_top.c --top pipelinec_top --out_dir pipelinec_output --
comb --no_synth > pipelinec.log
devel@pi5-80:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ make gateware.bin
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -q -m ghdl -p "ghdl --std=08 -frelaxed `cat
pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv top.sv pll.v; synth_ice40 -top top
-json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -q --randomize-seed --up5k --package sg48 --pcf
ice40.pcf --json gateware.json --asc gateware.asc --freq 25.0
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin
devel@pi5-80:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ bin2uf2 -o gateware.uf2
gateware.bin
devel@pi5-80:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ cp gateware.uf2
/media/devel/pico-ice/
```




```
export PIPELINEC_REPO="$HOME/PipelineC"
export OSS_CAD_SUITE=$HOME/oss-cad-suite/
devel@pi5-80:~/pico-ice/PipelineC/vga-pong/examples/pico-ice/ice_makefile_pipelinec $ make clean
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
devel@pi5-80:~/pico-ice/PipelineC/vga-pong/examples/pico-ice/ice_makefile_pipelinec $ make pipelinec
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec pong_top.c --top pipelinec_top --out_dir pipelinec_output --comb --no_synth > pipelinec.log
devel@pi5-80:~/pico-ice/PipelineC/vga-pong/examples/pico-ice/ice_makefile_pipelinec $ make gateware.bin
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -q -m ghdl -p "ghdl --std=08 -frelaxed `cat pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv top.sv pll.v; synth_ice40 -top top -json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -q --randomize-seed --up5k --package sg48 --pcf ice40.pcf --json gateware.json --asc gateware.asc --freq 25.0
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin
devel@pi5-80:~/pico-ice/PipelineC/vga-pong/examples/pico-ice/ice_makefile_pipelinec $ bin2uf2 -o gateware.uf2 gateware.bin
devel@pi5-80:~/pico-ice/PipelineC/vga-pong/examples/pico-ice/ice_makefile_pipelinec $ cp gateware.uf2 /media/devel/pico-ice/
```




```
devel@pi5-80:~ $ minicom ACM1
devel@pi5-80:~/pico-ice/PipelineC/vga-pong/examples/pico-ice/ice_makefile_pipelinec $
cd ../../../../vga-pll/ice_makefile_pipelinec/
devel@pi5-80:~/pico-ice/PipelineC/vga-pll/ice_makefile_pipelinec $ make clean
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
devel@pi5-80:~/pico-ice/PipelineC/vga-pll/ice_makefile_pipelinec $ make pipelinec
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec top.c --top pipelinec_top --out_dir pipelinec_output --comb --
no_synth > pipelinec.log
devel@pi5-80:~/pico-ice/PipelineC/vga-pll/ice_makefile_pipelinec $ make gateware.bin
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -q -m ghdl -p "ghdl --std=08 -frelaxed `cat
pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv top.sv pll.v; synth_ice40 -top top
-json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -q --randomize-seed --up5k --package sg48 --pcf
ice40.pcf --json gateware.json --asc gateware.asc --freq 25.0
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin
devel@pi5-80:~/pico-ice/PipelineC/vga-pll/ice_makefile_pipelinec $ bin2uf2 -o gateware.uf2
gateware.bin
devel@pi5-80:~/pico-ice/PipelineC/vga-pll/ice_makefile_pipelinec $ cp gateware.uf2
/media/devel/pico-ice/
```