

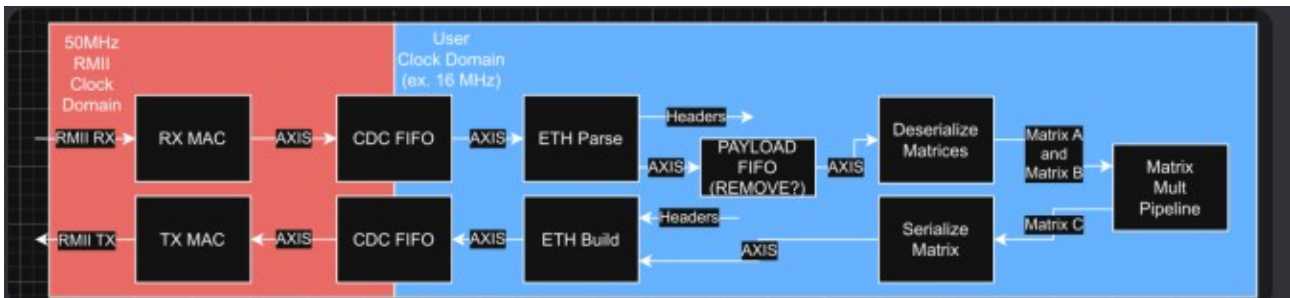
*****Default*****

PipelineC Ethernet PMOD

02/28/25

*****Default*****

The current image which does work in the form matrix multiply.



with those and the work() pipeline looks like so



Can come over to [# pipelinec](#) to hear more about this first demo of configuring the inputs work func and outputs to do 2x2 int8 matrix multiplication

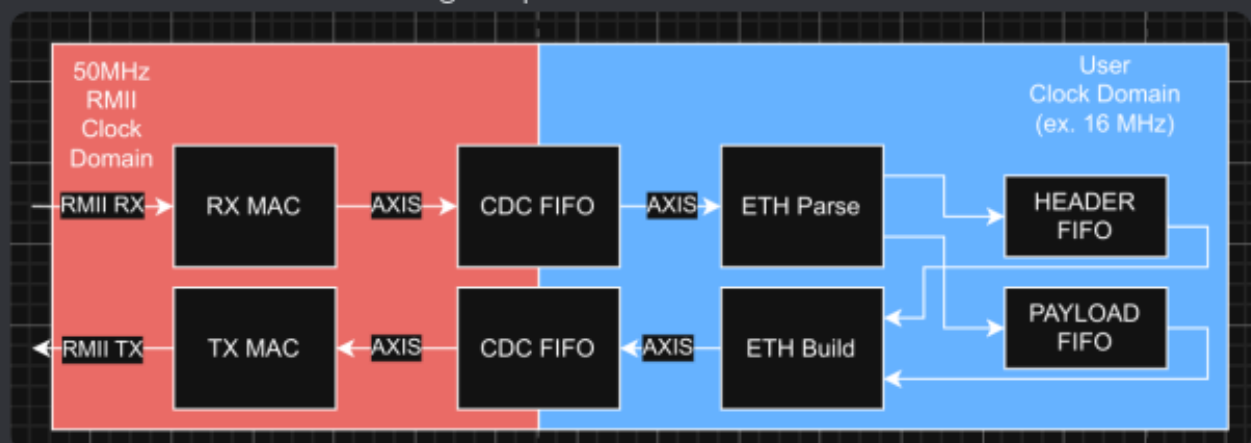
Tested 02/28/25 in PipelineC repo.

```
File Edit Tabs Help
devel@pi5-70: ~/PipelineC/examples/net
devel@pi5-70:~/PipelineC/examples/net $ gcc -I ../include -I ~/PipelineC/exa
ples/pico-ice/ice_makefile_pipelinec/pipelinec_output -Wall -pthread work_test.
c -o work_test
devel@pi5-70:~/PipelineC/examples/net $ sudo ./work_test
CPU threads: 1
n 'work()'s: 1
Total tx bytes: 8
Total rx bytes: 4
CPU took 0.000328 seconds to execute
CPU iteration time: 0.000328 seconds
CPU bytes per sec: 36578.232558 B/s
FPGA took 0.000216 seconds to execute
FPGA iteration time: 0.000216 seconds
FPGA bytes per sec: 55553.695364 B/s
Speedup: 1.518764
devel@pi5-70:~/PipelineC/examples/net $

File Edit Tabs Help
devel@pi5-70: ~/PipelineC/examples/pico-ice/ice_makefile_pipelinec
devel@pi5-70:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ make clean
rm -f lextab.py
rm -f yaccstab.py
rm -f pll_clk_mhz.h
rm -f r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f Yosys_stderr.log
rm -f dfu_util.log
devel@pi5-70:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ make pipeli
nec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec ethernet_top.c --top pipelinec_top --out_di
r pipelinec_output --comb --no_synth > pipelinec.log
devel@pi5-70:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ make gatewa
re.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
/home/devel/oss-cad-suite/bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite/bin/yosys -l simple.log -q -m ghdl -p "ghdl --std=08
-frelaxed 'cat pipelinec_output/vhdl_files.txt' -e pipelinec_top; read_verilog
-sv ethernet_top.sv pll.v; synth_ice40 -top ethernet_top -json gateway.json"
2> Yosys_stderr.log
/home/devel/oss-cad-suite/bin/nextpnr-ice40 -l nextpnr.log -q --seed 1 --up5k
--package sg48 --pcf ice40.pcf --json gateway.json --asc gateway.asc --pre-pa
ck eth_clocks.py
/home/devel/oss-cad-suite/bin/icepack gateway.asc gateway.bin
devel@pi5-70:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ bin2uf2 -o
gateway.uf2 gateway.bin
devel@pi5-70:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $ scp gatewar
e.uf2 pi5-90:/media/devel/pico-ice/
gateway.uf2 100% 204KB 10.3MB/s 00:00
devel@pi5-70:~/PipelineC/examples/pico-ice/ice_makefile_pipelinec $
```

This image was loopback tested on 02/17/25

this is what the current design implements



AXIS buses are 8b wide

user clock could be as low as $50M/4 = 12.5M$

pico-ice Running gateway.bin provided by Discord user absurdfatalism. Led blink red.

This was fixed with added make parameters.

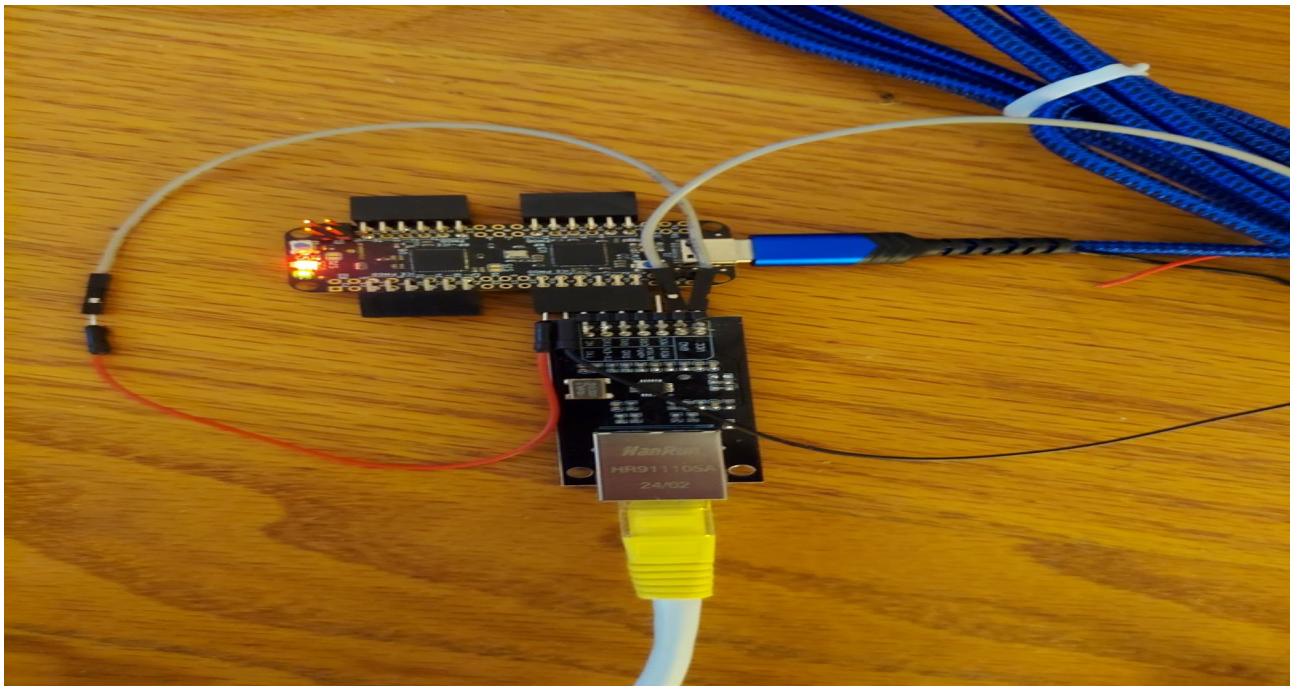
make clean

make pipelinec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"

make gateway.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"

bin2uf2 -o gateway.uf2 gateway.bin

scp gateway.uf2 pi5-90:/media/devel/pico-ice/



3.3 grd A4 A3 A2 A1



3.3 grd B4 B3 B2 B1

A1-43 B1-42
A2-38 B2-36
A3-34 B3-32
A4-31 B4-28

3.3 grd A4 A3 A2 A1

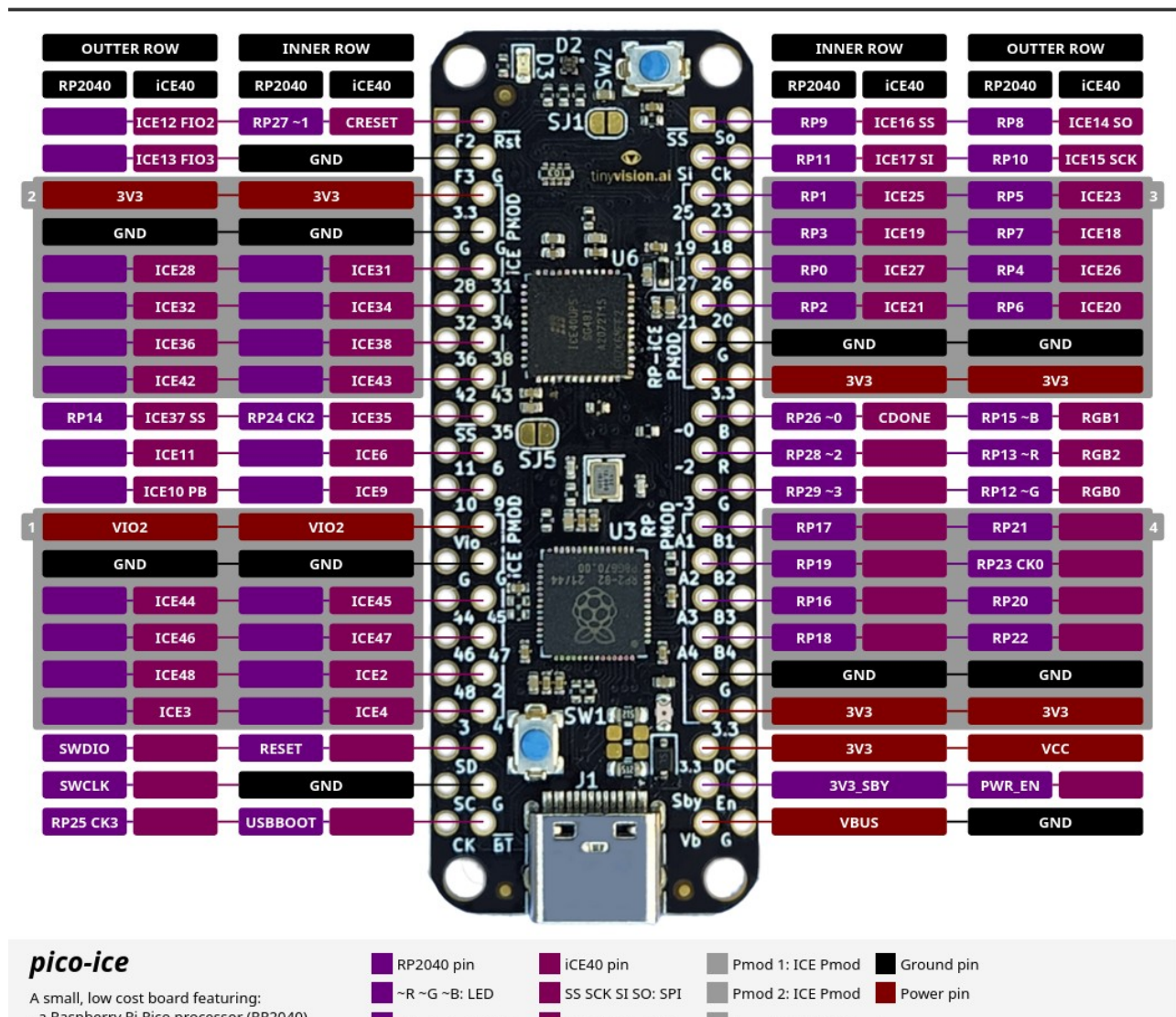


3.3 grd B4 B3 B2 B1

A1-4 B1-3
A2-2 B2-8
A3-47 B3-46
A4- 45 B4-44

USB

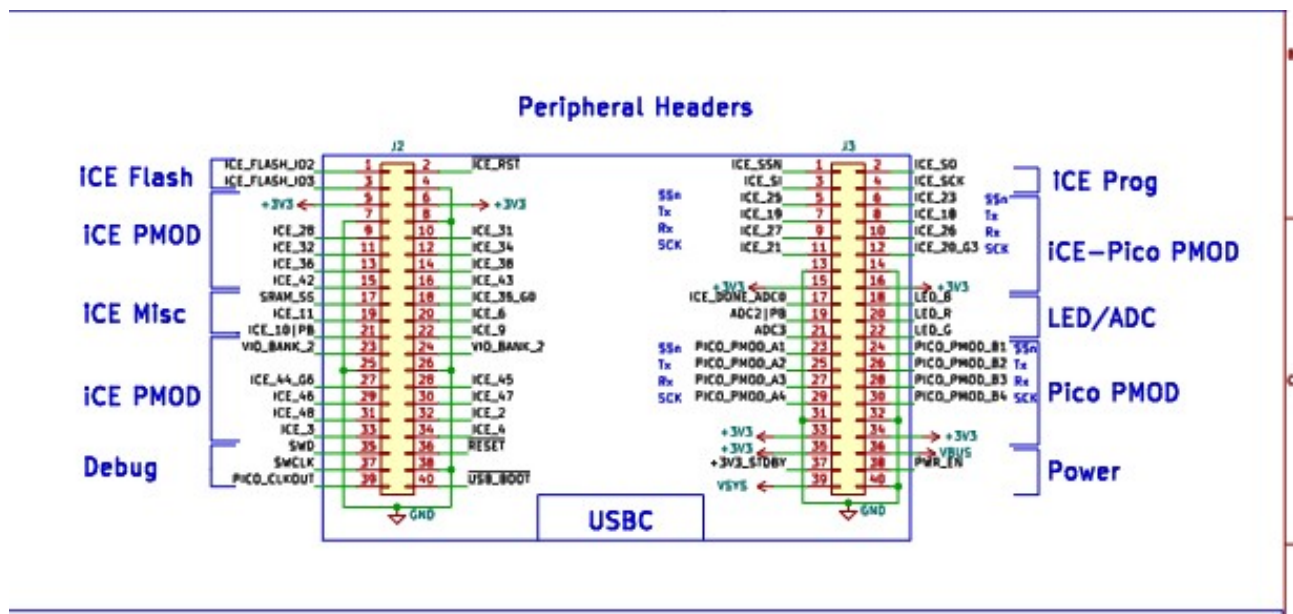
XX




```
raspberrypi-5 devel@pi5-90:~/PipelineC/examples/arti/src/eth $ sudo ./loopback_test
```

```
pico-ice with Ethernet pmod devel@pi5-90:~/PipelineC/examples/arti/src/eth $ sudo
./loopback_test
Test passed!
```

sch



sch

```
pi5-70 or pi5-80
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $
make clean
make pipelinec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
make gateway.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
bin2uf2 -o gateway.uf2 gateway.bin
scp gateway.uf2 pi5-90:/media/devel/pico-ice/
devel@pi5-90:~/PipelineC/examples/arti/src/eth $ sudo ./loopback_test
Test passed!
```