**********Default**********

Nandland UART Verilog
08/12/24

**********Default**********

The UART_RX.v & UART_TX.v are less than 1000 lines of Verilog code.

With pico_ice_default_firmware_v1.6.1 firm I have tested ICE_25 signal can be detected by the iCE40UP5K. I made some medications to the Verilog main.v from ice_makefile_blinky example see https://github.com/develone/pico-ice/blob/test-dev/myDocs/rx_tx_setup.pdf which describes the changes and the results detecting ICE_25 signal.

git clone https://github.com/develone/nandland.git -b dev

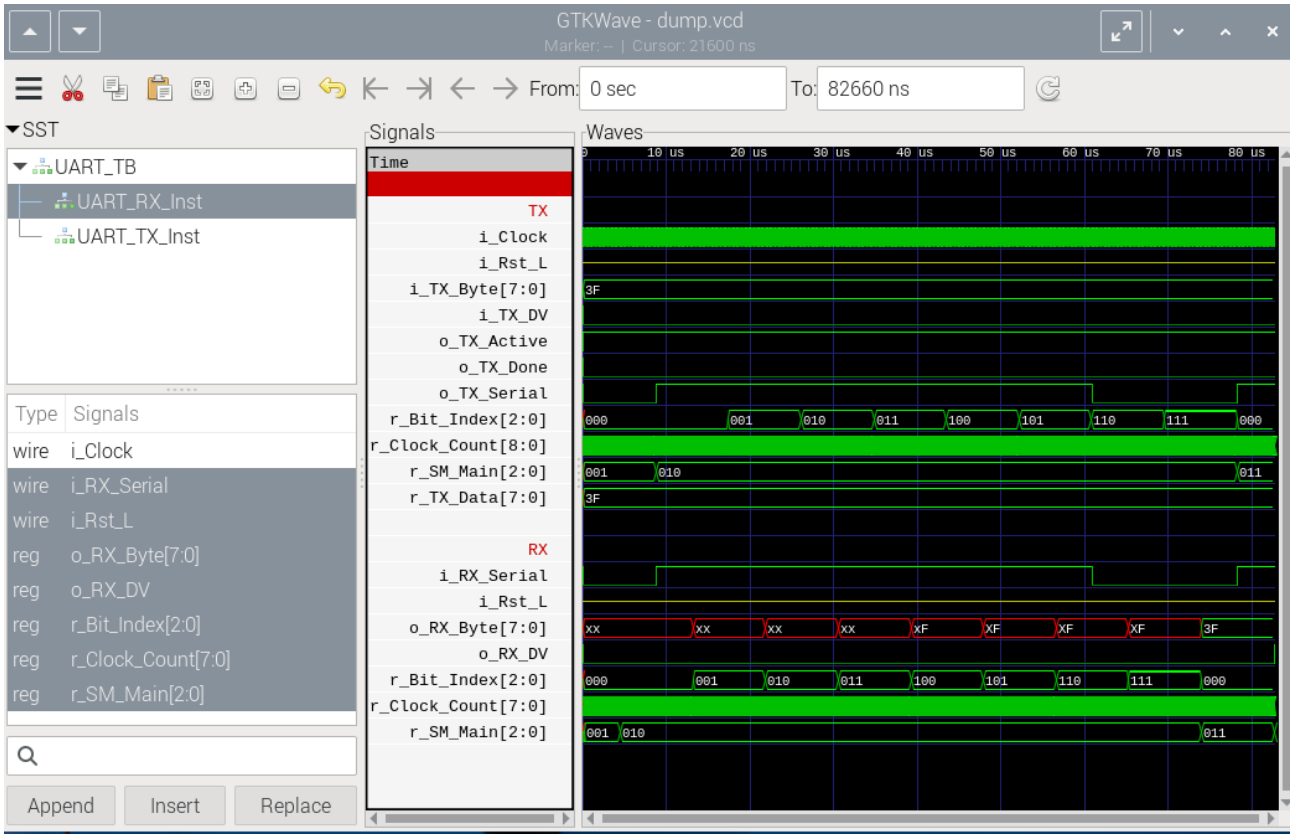
cd nandland/uart/Verilog/sim

iverilog -o dsn iverilog -o dsn UART_TB.v

vvp dsn

gtkdump dump.vcd

3F is sent and 3F is received



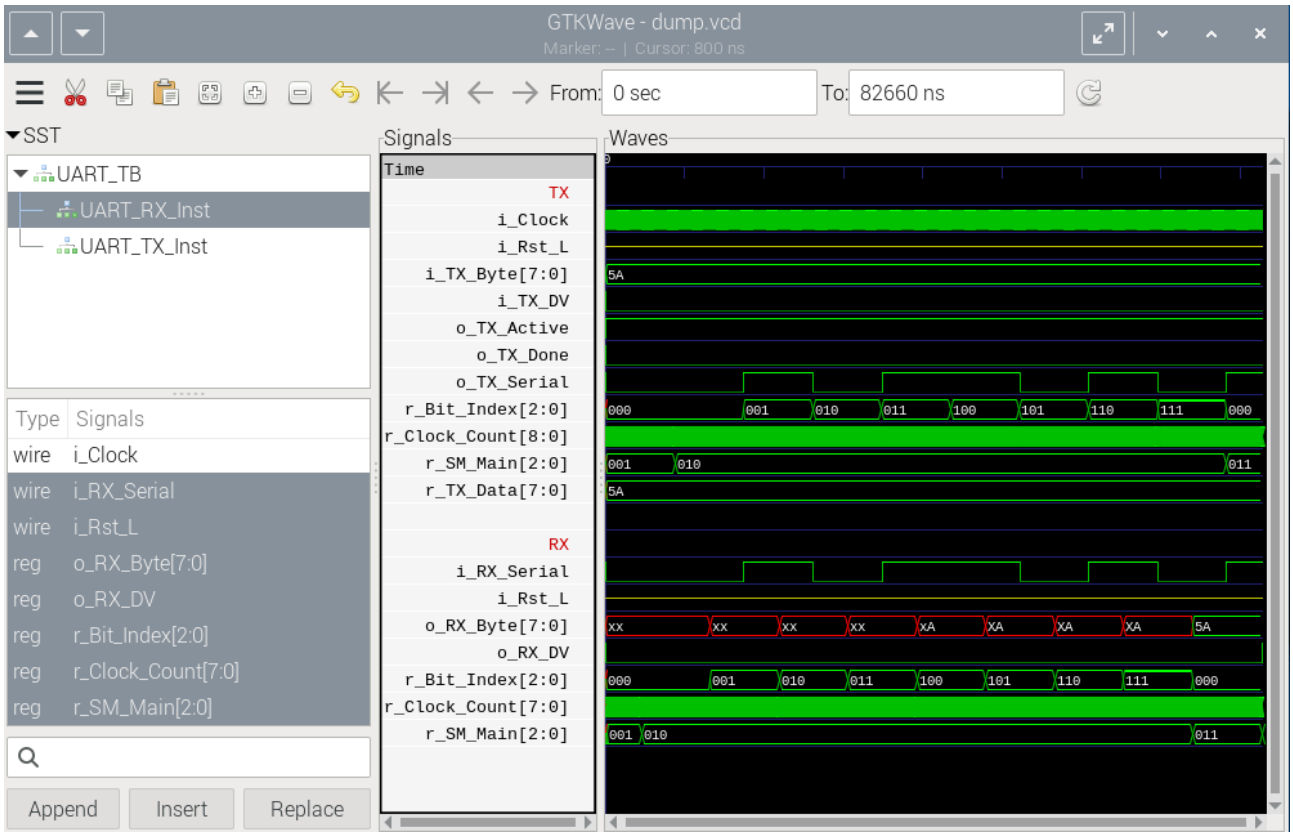
Modifying the UART_TB.v in 2 places.

iverilog -o dsn iverilog -o dsn UART_TB.v

vvp dsn

gtkdump dump.vcd

5A is sent and 5A is received



LSB MSB
10101010
01010101