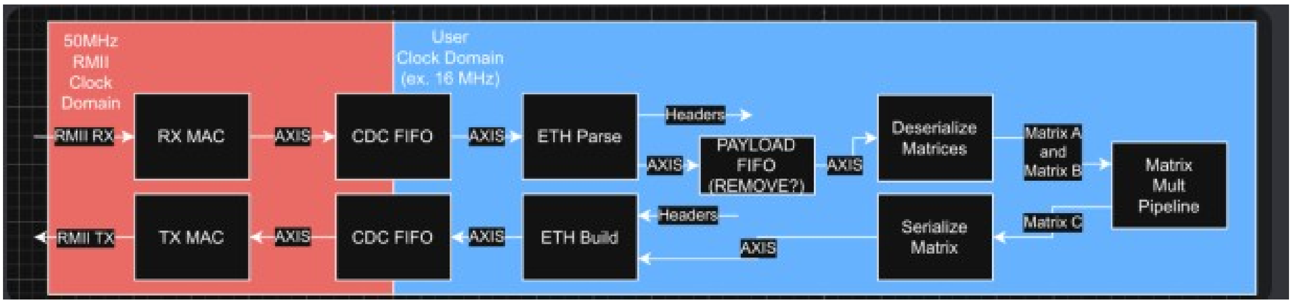
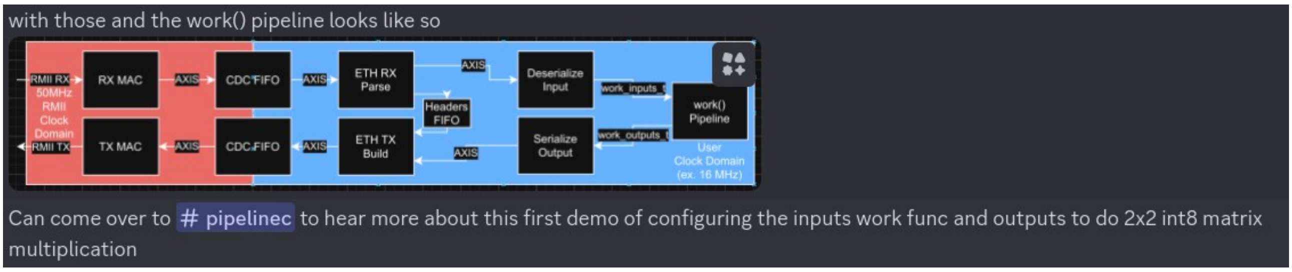
************************Default*************************

PipelineC PMOD Ethernet JPEG Block connected to a pico-ice
03/14/25

************************Default*************************

The current image which does work in the form matrix multiply.





Tested 03/06/25 in pico-ice repo branch test-dev-100424 in two shell below.
Following **"git clone https://github.com/develone/pico-ice.git -b test-dev-100424"**

If the command in the left image below is done before the command in right image below.

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/net $ **./compile-work_test.sh**

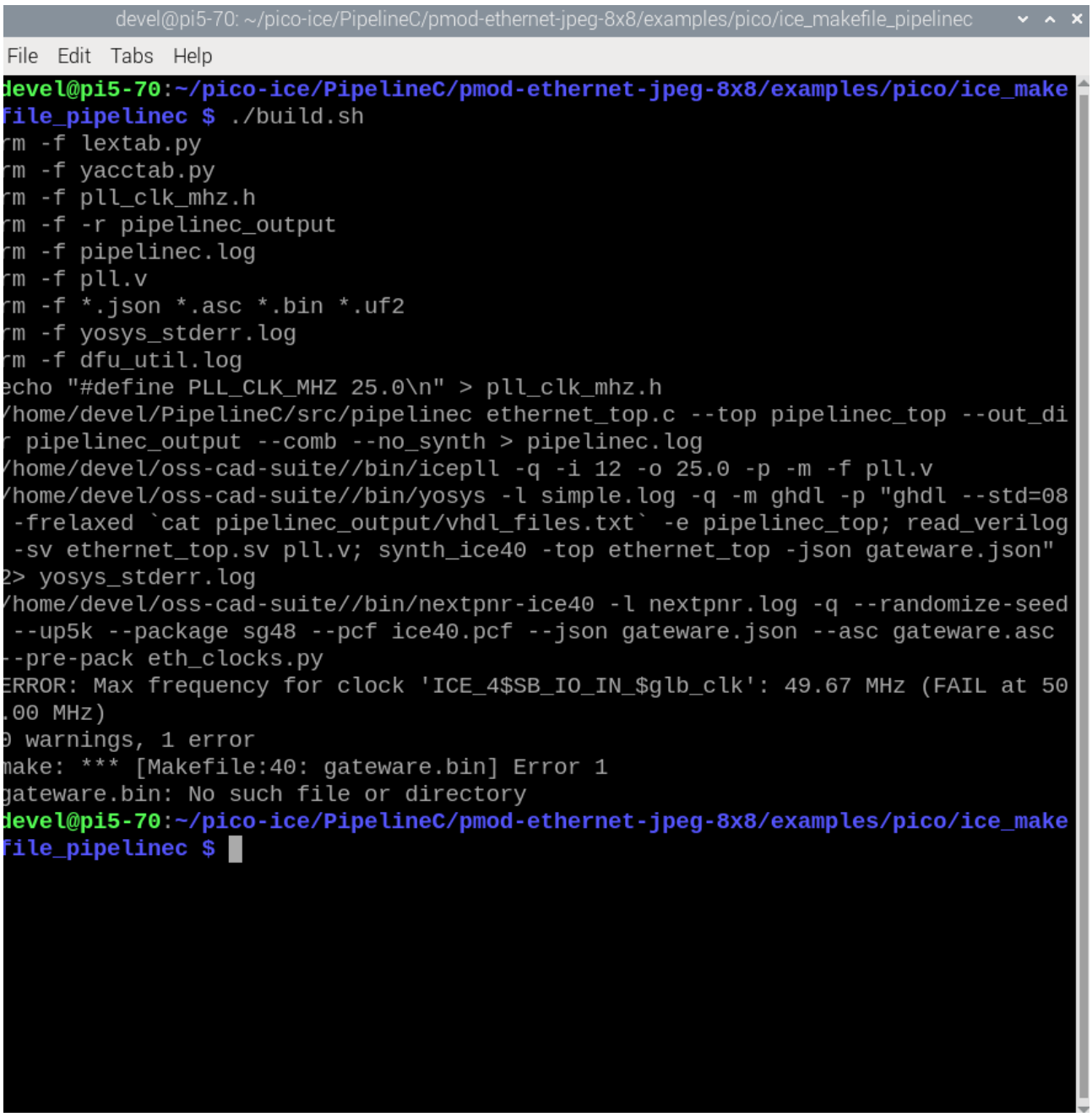
The work_test.c is dependent on the successful build of gateware.bin see Appendix A.

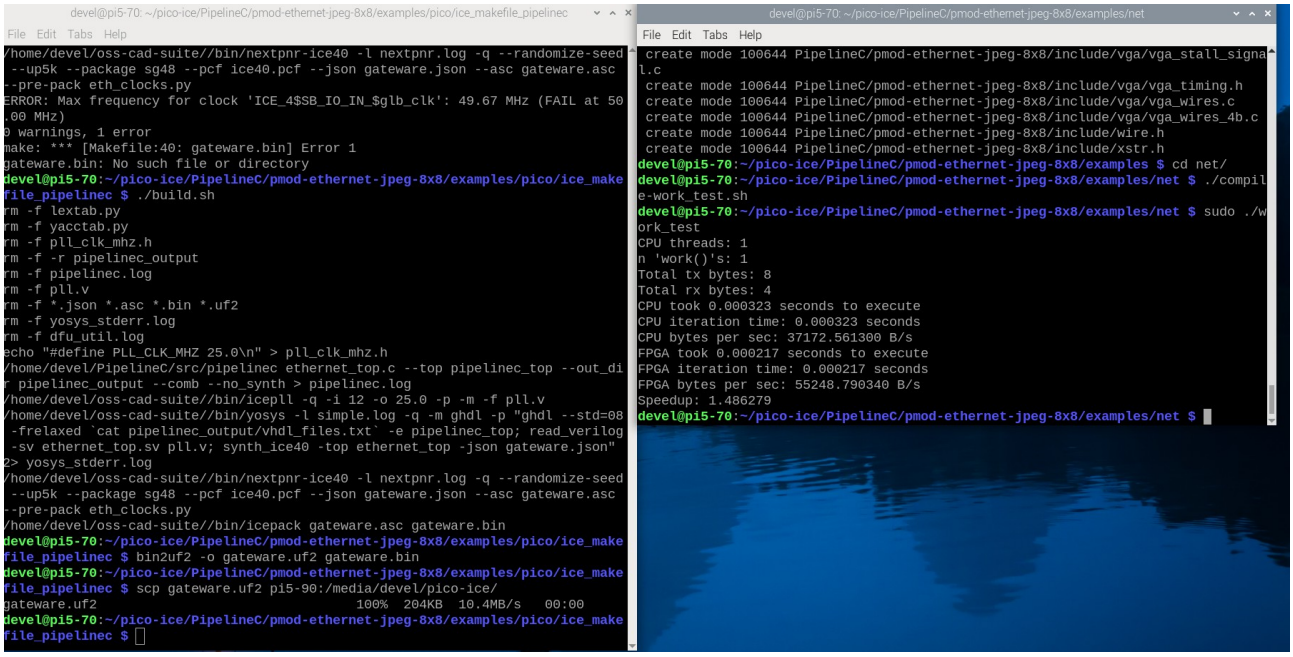
```
In file included from work_test.c:30:
work.h:26:10: fatal error: type_bytes_t.h/work_inputs_t_bytes_t.h/work_inputs_t_bytes.h: No such file or directory
   26 | #include "type_bytes_t.h/work_inputs_t_bytes_t.h/work_inputs_t_bytes.h"
      |          ^~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
compilation terminated.
```

make clean all TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"

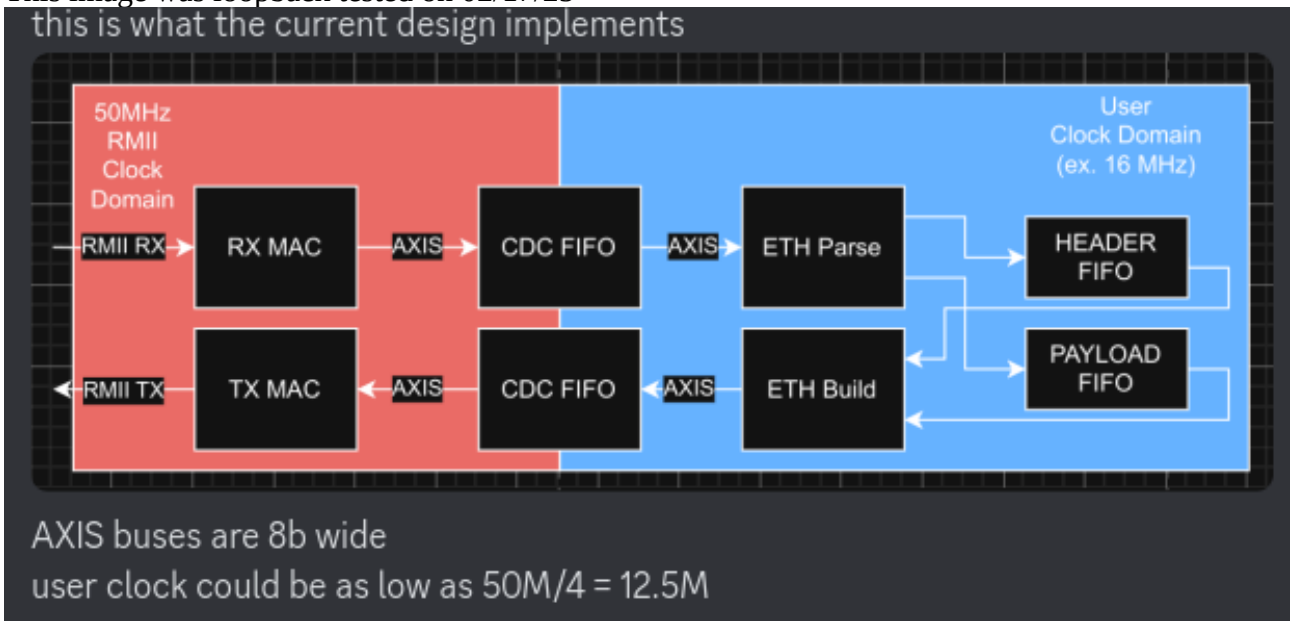
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output

```
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec ethernet_top.c --top pipelinec_top --out_dir
pipelinec_output --comb --no_synth > pipelinec.log
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -l simple.log -q -m ghdl -p "ghdl --std=08 -frelaxed `cat
pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv ethernet_top.sv pll.v;
synth_ice40 -top ethernet_top -json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -l nextpnr.log -q --randomize-seed --up5k --
package sg48 --pcf ice40.pcf --json gateware.json --asc gateware.asc --pre-pack eth_clocks.py
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/pico/ice_makefile_pipelinec $
bin2uf2 -o gateware.uf2 gateware.bin

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/pico/ice_makefile_pipelinec $ scp
gateware.uf2 pi5-90:/media/devel/pico-ice/
gateware.uf2                                  100%  204KB  10.4MB/s   00:00

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/net $ ./compile-work_test.sh

devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/examples/net $ sudo ./work_test
CPU threads: 1
n 'work()'s: 1
Total tx bytes: 8
Total rx bytes: 4
CPU took 0.000290 seconds to execute
CPU iteration time: 0.000290 seconds
CPU bytes per sec: 41391.157895 B/s
FPGA took 0.000207 seconds to execute
FPGA iteration time: 0.000207 seconds
FPGA bytes per sec: 57985.769585 B/s
Speedup: 1.400922
```

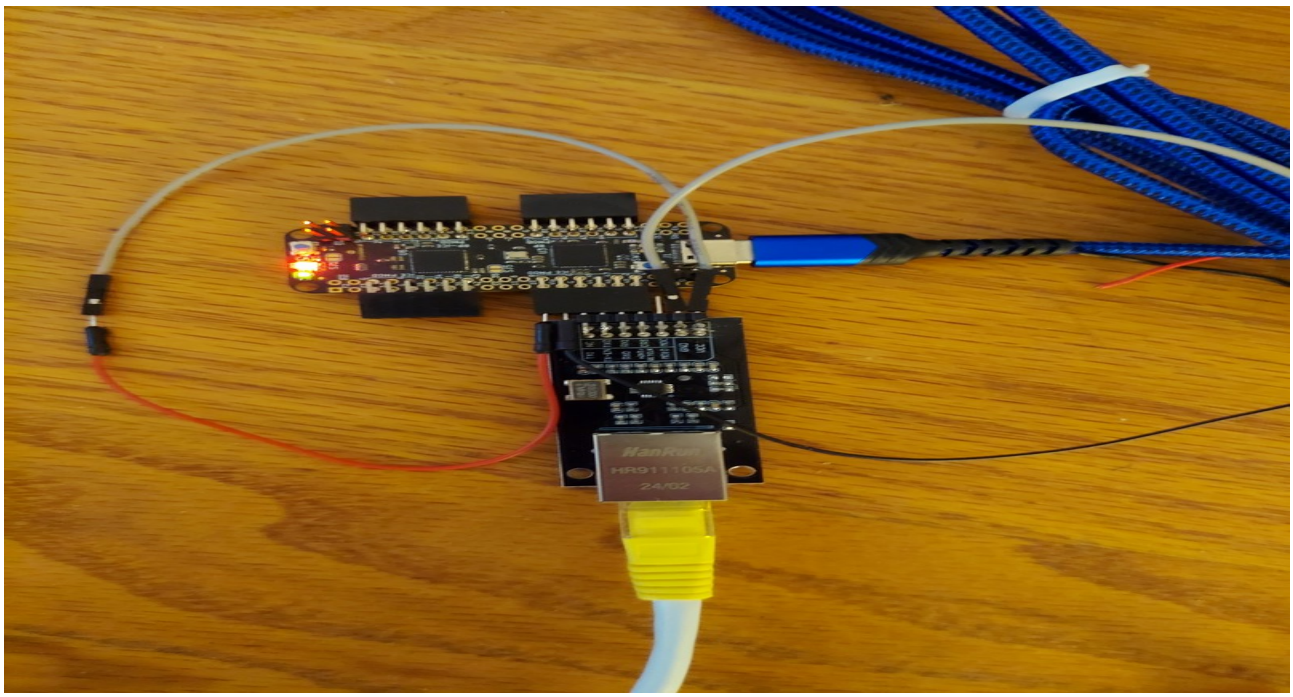

devel@pi5-70: ~/pico-ice/PipelineC/pmod-ethernet-jpeg-8x8/examples/pico/ice_makefile_pipelinec
File Edit Tabs Help
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet-jpeg-8x8/examples/pico/ice_makefile_pipelinec $ ./build.sh
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec ethernet_top.c --top pipelinec_top --out_dir pipelinec_output --comb --no_synth > pipelinec.log
/home/devel/oss-cad-suite//bin/icepll -q -i 12 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -l simple.log -q -m ghdl -p "ghdl --std=08 -frelaxed `cat pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv ethernet_top.sv pll.v; synth_ice40 -top ethernet_top -json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -l nextpnr.log -q --randomize-seed --up5k --package sg48 --pcf ice40.pcf --json gateware.json --asc gateware.asc --pre-pack eth_clocks.py
ERROR: Max frequency for clock 'ICE_4$SB_IO_IN_$glb_clk': 49.67 MHz (FAIL at 50.00 MHz)
0 warnings, 1 error
make: *** [Makefile:40: gateware.bin] Error 1
gateware.bin: No such file or directory
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet-jpeg-8x8/examples/pico/ice_makefile_pipelinec $



This image was loopback tested on 02/17/25



pico-ice Running gateware.bin provided by Discord user absurfatalism. Led blink red.
This was fixed with added make parameters.
make clean
make pipelinec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
make gateware.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
bin2uf2 -o gateware.uf2 gateware.bin
scp gateware.uf2 pi5-90:/media/devel/pico-ice/



3.3 grd A4 A3 A2 A1

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3.3 grd B4 B3 A2 B1

pico-ice

3.3 grd A4 A3 A2 A1

☐ ☐ ☐ ☐ ☐ ☐

☐ ☐ ☐ ☐ ☐ ☐

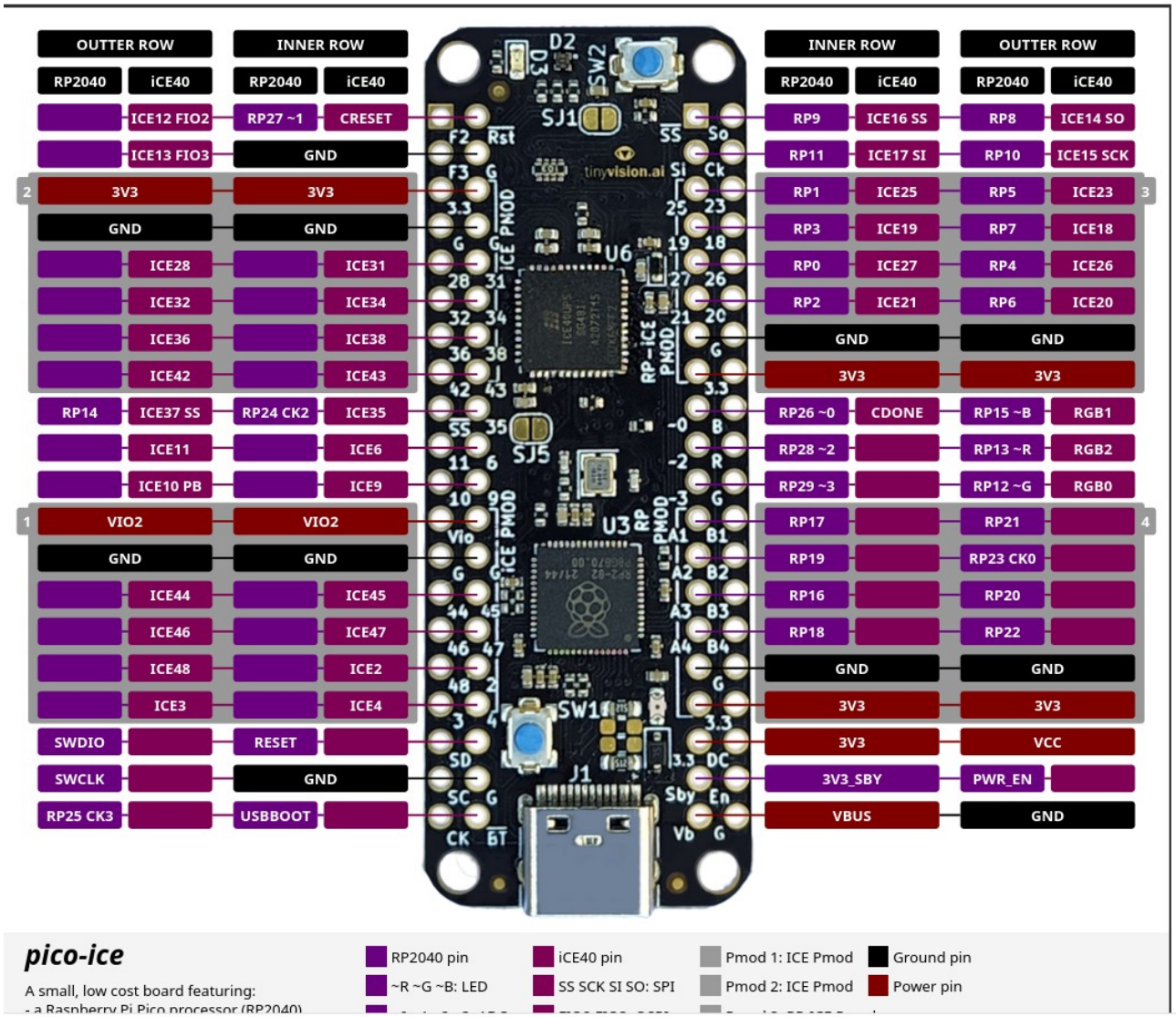
3.3 grd B4 B3 B2 B1

A1-43	B1-42
A2-38	B2-36
A3-34	B3-32
A4-31	B4-28

A1-4	B1-3
A2-2	B2-48
A3-47	B3-46
A4- 45	B4-44

USB

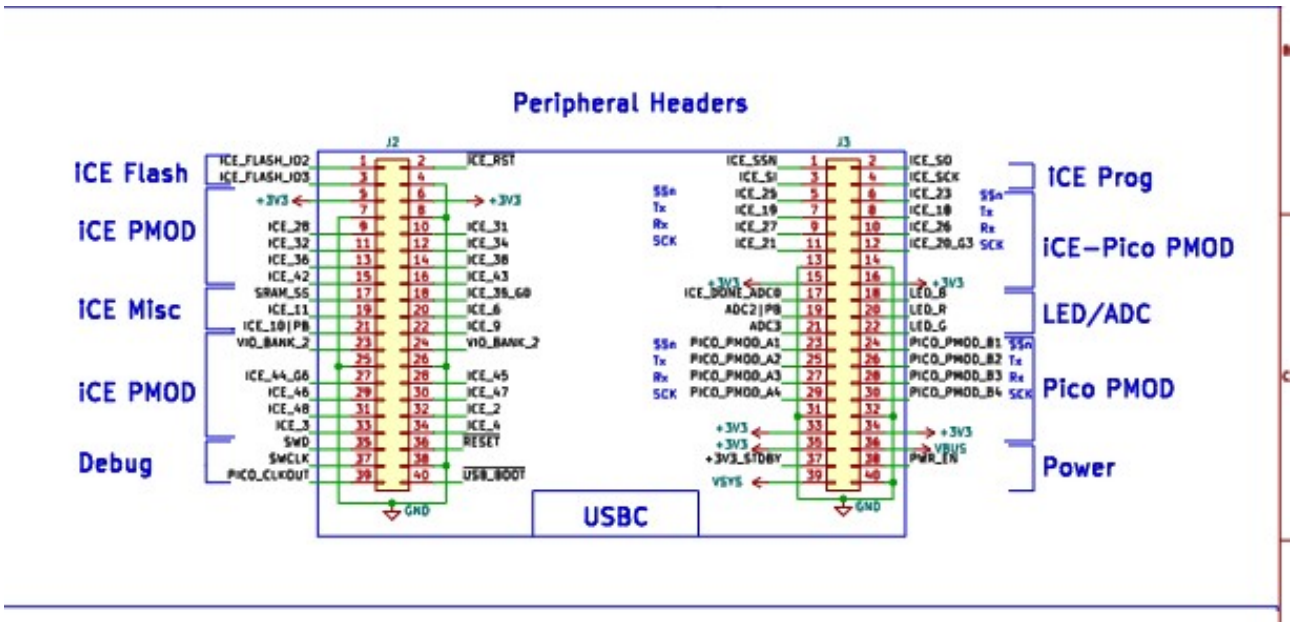
xx



raspberry-pi-5 devel@pi5-90:~/PipelineC/examples/arty/src/eth $ sudo ./loopback_test

pico-ice with Ethernet pmod devel@pi5-90:~/PipelineC/examples/arty/src/eth $ sudo ./loopback_test
Test passed!

sch



sch

pi5-70 or pi5-80
devel@pi5-80:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $
devel@pi5-70:~/pico-ice/PipelineC/pmod-ethernet/ice_makefile_pipelinec $
make clean
make pipelinec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
make gateware.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
bin2uf2 -o gateware.uf2 gateware.bin
scp gateware.uf2 pi5-90:/media/devel/pico-ice/
devel@pi5-90:~/PipelineC/examples/arty/src/eth $ sudo ./loopback_test
Test passed!

Appendix A

```
#pragma once
#include "type_bytes_t.h/int8_t_bytes_t.h/int8_t_bytes.h"
#define work_inputs_t_SIZE 8

void work_inputs_t_to_bytes(work_inputs_t* x, uint8_t* bytes)
{
size_t pos = 0;
// matrix0
size_t matrix0_dim_0;
for(matrix0_dim_0=0;matrix0_dim_0<2;matrix0_dim_0=matrix0_dim_0+1){
size_t matrix0_dim_1;
for(matrix0_dim_1=0;matrix0_dim_1<2;matrix0_dim_1=matrix0_dim_1+1){
 int8_t_to_bytes(&(x->matrix0[matrix0_dim_0][matrix0_dim_1]), &(bytes[pos]));
 pos = pos + 1; // not sizeof()
}
}
// matrix1
```

```
size_t matrix1_dim_0;
for(matrix1_dim_0=0;matrix1_dim_0<2;matrix1_dim_0=matrix1_dim_0+1){
size_t matrix1_dim_1;
for(matrix1_dim_1=0;matrix1_dim_1<2;matrix1_dim_1=matrix1_dim_1+1){
 int8_t_to_bytes(&(x->matrix1[matrix1_dim_0][matrix1_dim_1]), &(bytes[pos]));
 pos = pos + 1; // not sizeof()
}
}

}

void bytes_to_work_inputs_t(uint8_t* bytes, work_inputs_t* x)
{
size_t pos = 0;
// matrix0
size_t matrix0_dim_0;
for(matrix0_dim_0=0;matrix0_dim_0<2;matrix0_dim_0=matrix0_dim_0+1){
size_t matrix0_dim_1;
for(matrix0_dim_1=0;matrix0_dim_1<2;matrix0_dim_1=matrix0_dim_1+1){
 bytes_to_int8_t(&(bytes[pos]), &(x->matrix0[matrix0_dim_0][matrix0_dim_1]));
 pos = pos + 1; // not sizeof()
}
}
// matrix1
size_t matrix1_dim_0;
for(matrix1_dim_0=0;matrix1_dim_0<2;matrix1_dim_0=matrix1_dim_0+1){
size_t matrix1_dim_1;
for(matrix1_dim_1=0;matrix1_dim_1<2;matrix1_dim_1=matrix1_dim_1+1){
 bytes_to_int8_t(&(bytes[pos]), &(x->matrix1[matrix1_dim_0][matrix1_dim_1]));
 pos = pos + 1; // not sizeof()
}
}

}
```