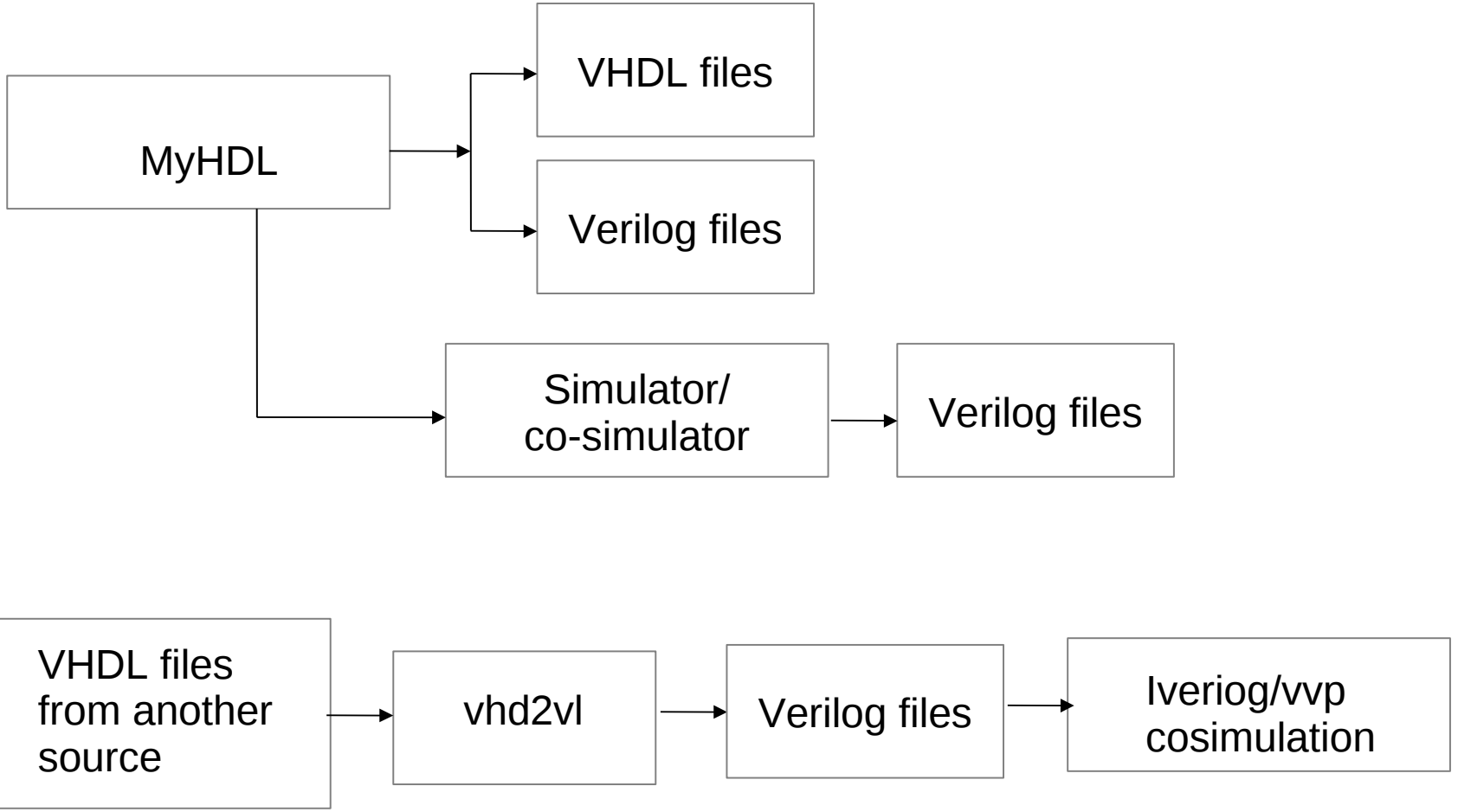
Simulation/Co-Simulations Tools

Edward Vidal Jr.
08/31/15


MyHDL
VHDL files
Verilog files
Simulator/
co-simulator
Verilog files
VHDL files
from another
source
vhd2vl
Verilog files
Iveriog/vvp
cosimulation

Tools

- MyHDL
- VHD2VL
- Iverilog
- Python

Steps to Create Simulation

- Create test_xxx.py file
    - create the signals that are to be test
    - define stimlus
    - create a clkgen
    - prepare the cosimulation environment
        - cmd = "iverilog -o ifchain ../ifchain.v ./tb_ifchain.v"
        - cmd = "vvp -m ./myhdl.vpi ifchain"
        - cosim = Cosimulation(cmd, **sigs)
- Create tb_xxx.v file
    - Defines where the vcd file will be
    - Defines name of vcd file