Section of the tb_xxx.v file

```
`timescale 1ns/10ps

module tb_maths1;

reg  [15:0] x;
reg  [15:0] y;
wire [15:0] vm, vb, vc;
```

The lines below define the location and name of the vcd file.
This also defines the name of module to be sent to vcd file

```
initial begin
   $dumpfile("vcd/maths1.vcd");
   $dumpvars(0, tb_maths1);
end
```

The next lines provide for the communication between MyHDL
and the Co-Simulation

```
initial begin
   $from_myhdl(
      x,
      y
   );
   $to_myhdl(
      vm,
      vb,
      vc
   );
end
```

The next lines instantiate several modules mm_maths1, mb_maths1, and mc_maths1
to be stimluated by MyHDL or by stimlus in the tb_xxx.v

```
/** the myhdl verilog */
mm_maths1 dut_myhdl(x, y, vm);
```

mm_maths1 in the line above is the name of the module in the file mm_math1.v

```
/** the bluespec verilog */
wire clock, reset;
mb_maths1 dut_bsv(clock, reset, x, y, vb);

/** the chisel verilog */
mc_maths1 dut_chisel(x, y, vc);

endmodule
```