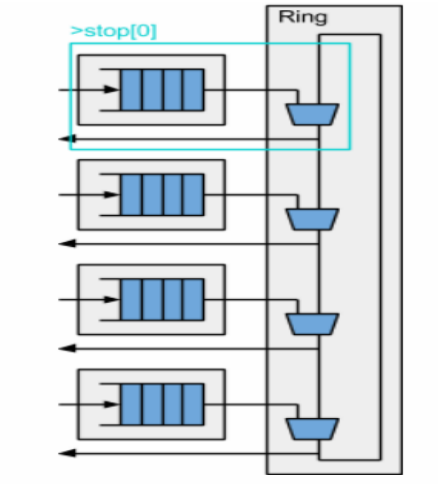
TUTORIAL-Flow

Data packets are queued in the input FIFOs (First In First Out buffers). Packets await their opportunity to inject into the ring, and travel around the ring to exit at their destination.



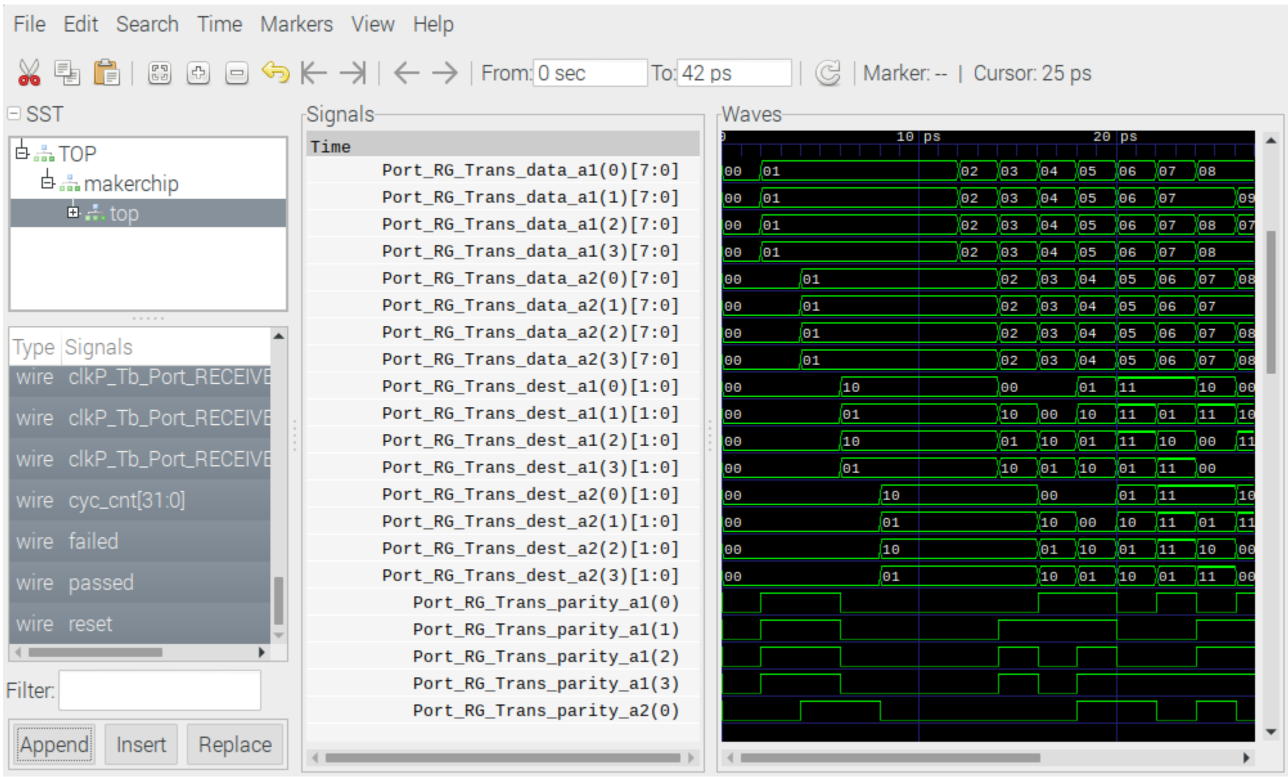
The design is very little code because it is constructed from M4 macros for the FIFOs **(m4+simple_bypass_fifo_v2)** the Ring **(m4+simple_ring)** and a testbench **(m4+router_testbench)**.

Before exploring how this transaction flow is coded, let’s see what it can do. Let’s imagine, we need to add data protection to the packet by adding a parity field.

With that simple two-line change, you implemented or changed 19 lines of RTL! These changes carried the new parity field through the FIFOs, into the ring, and out. In a real-world design, a simple change like this could change hundreds of lines of RTL!

```
diff ring_parity/top.tlv ring_parity_8port/top.tlv
41c41
<    m4_define_hier(M4_PORT, 4, 0)   // Defines constants for /port[3:0].
---
>    m4_define_hier(M4_PORT, 8, 0)   // Defines constants for /port[3:0].
```

4port



From: 0 sec To: 42 ps Marker: -- | Cursor: 25 ps

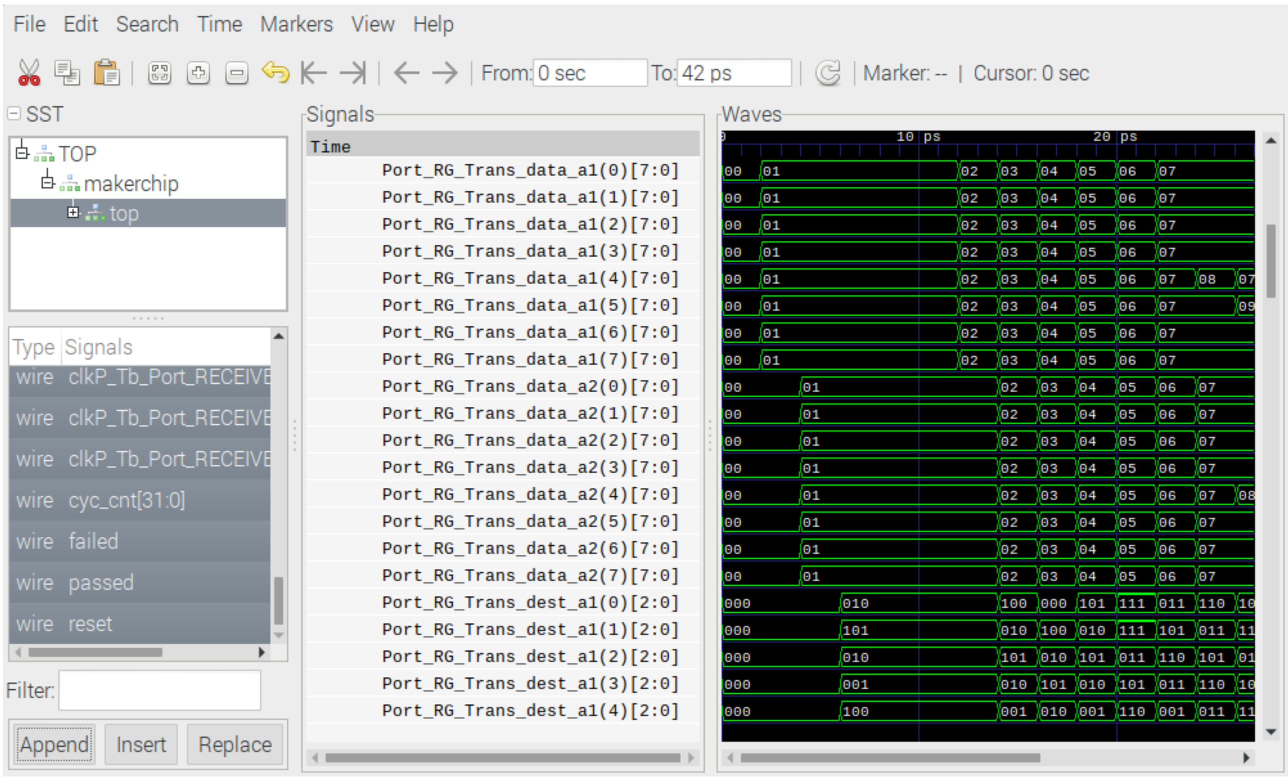
TOP
makerchip
top

Type	Signals
wire	clkP_Tb_Port_RECEIVE
wire	clkP_Tb_Port_RECEIVE
wire	clkP_Tb_Port_RECEIVE
wire	cyc_cnt[31:0]
wire	failed
wire	passed
wire	reset

Filter:

```
Time
Port_RG_Trans_data_a1(0)[7:0]
Port_RG_Trans_data_a1(1)[7:0]
Port_RG_Trans_data_a1(2)[7:0]
Port_RG_Trans_data_a1(3)[7:0]
Port_RG_Trans_data_a2(0)[7:0]
Port_RG_Trans_data_a2(1)[7:0]
Port_RG_Trans_data_a2(2)[7:0]
Port_RG_Trans_data_a2(3)[7:0]
Port_RG_Trans_dest_a1(0)[1:0]
Port_RG_Trans_dest_a1(1)[1:0]
Port_RG_Trans_dest_a1(2)[1:0]
Port_RG_Trans_dest_a1(3)[1:0]
Port_RG_Trans_dest_a2(0)[1:0]
Port_RG_Trans_dest_a2(1)[1:0]
Port_RG_Trans_dest_a2(2)[1:0]
Port_RG_Trans_dest_a2(3)[1:0]
Port_RG_Trans_parity_a1(0)
Port_RG_Trans_parity_a1(1)
Port_RG_Trans_parity_a1(2)
Port_RG_Trans_parity_a1(3)
Port_RG_Trans_parity_a2(0)
```

8port



From: 0 sec To: 42 ps Marker: -- | Cursor: 0 sec

TOP
makerchip
top

Type	Signals
wire	clkP_Tb_Port_RECEIVE
wire	clkP_Tb_Port_RECEIVE
wire	clkP_Tb_Port_RECEIVE
wire	cyc_cnt[31:0]
wire	failed
wire	passed
wire	reset

Filter:

```
Time
Port_RG_Trans_data_a1(0)[7:0]
Port_RG_Trans_data_a1(1)[7:0]
Port_RG_Trans_data_a1(2)[7:0]
Port_RG_Trans_data_a1(3)[7:0]
Port_RG_Trans_data_a1(4)[7:0]
Port_RG_Trans_data_a1(5)[7:0]
Port_RG_Trans_data_a1(6)[7:0]
Port_RG_Trans_data_a1(7)[7:0]
Port_RG_Trans_data_a2(0)[7:0]
Port_RG_Trans_data_a2(1)[7:0]
Port_RG_Trans_data_a2(2)[7:0]
Port_RG_Trans_data_a2(3)[7:0]
Port_RG_Trans_data_a2(4)[7:0]
Port_RG_Trans_data_a2(5)[7:0]
Port_RG_Trans_data_a2(6)[7:0]
Port_RG_Trans_data_a2(7)[7:0]
Port_RG_Trans_dest_a1(0)[2:0]
Port_RG_Trans_dest_a1(1)[2:0]
Port_RG_Trans_dest_a1(2)[2:0]
Port_RG_Trans_dest_a1(3)[2:0]
Port_RG_Trans_dest_a1(4)[2:0]
```