==========

# Time-Division Multiplexer and De-multiplexing
# 10/29/20

==========

Started in Makerchip.com

Downloaded top.tlv, top.m4.pre, and top.m4.

java -jar /home/devel/SandPiper_1.9-2018_02_11-beta_distro/target/sandpiper.jar --debugSigs --viz --dhtml --stats --compiler verilator --graphTrans -i top.m4 -o top.sv

dot -Tpdf top_trans.dot -o top_trans.pdf

qpdfview top_trans.pdf &

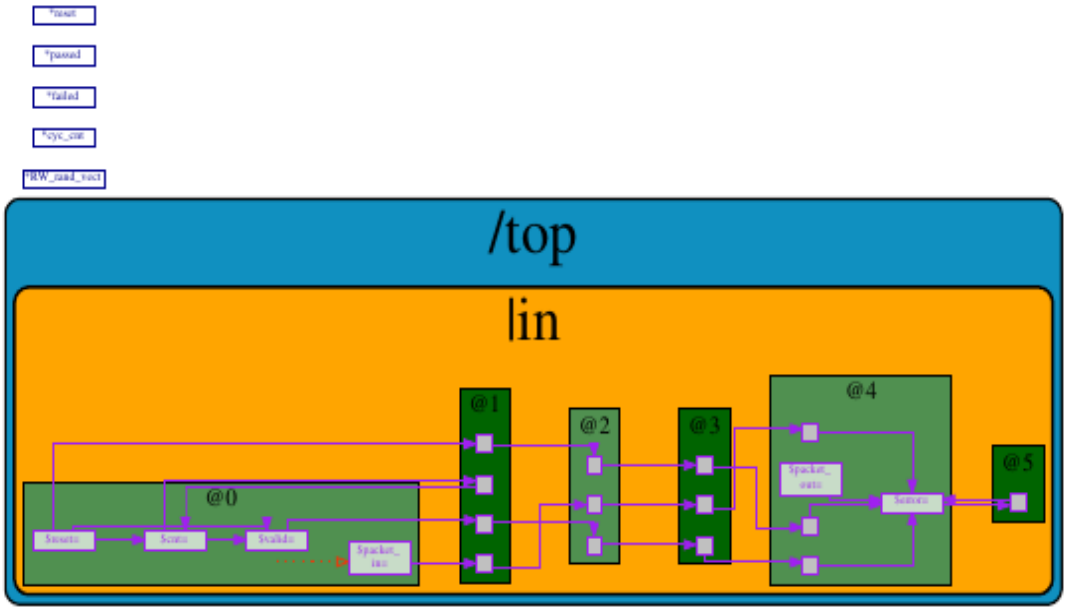
cp ../extra_files/* .

https://raw.githubusercontent.com/stevehoover/tlv_flow_lib/master/makerchip_files/verilog/sandhost/sqrt32.v

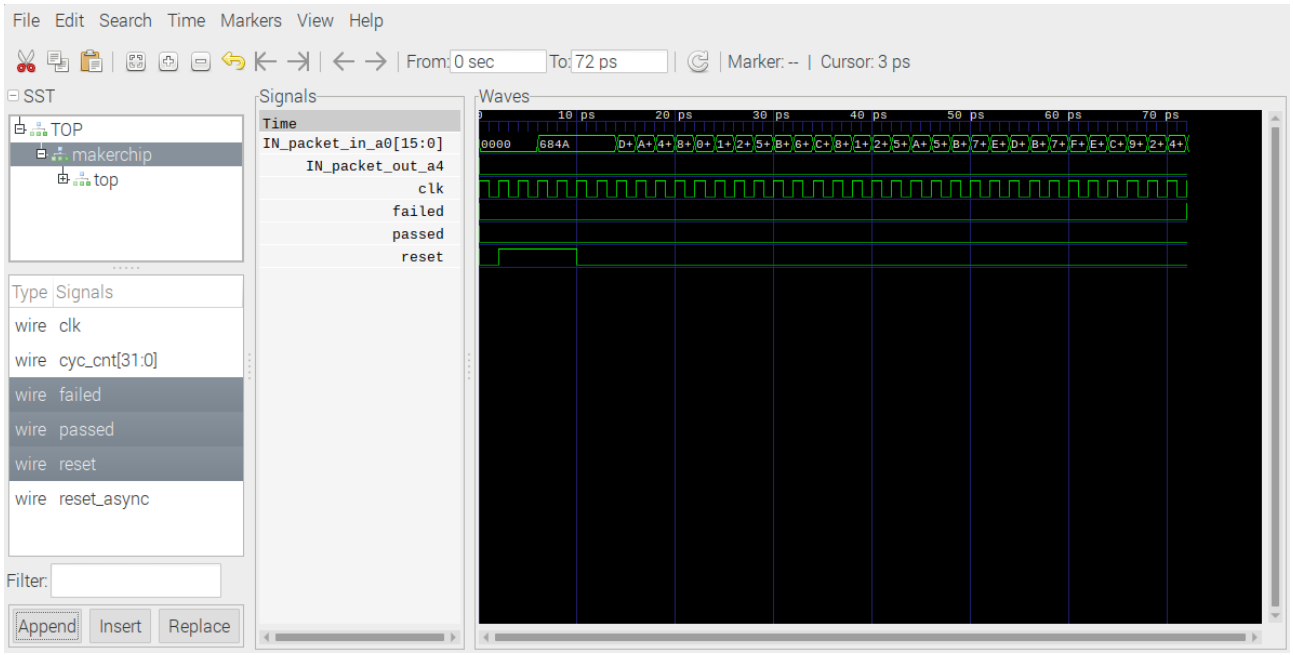
cp ~/warp-v/formal/verilog/clk_gate.v

//`include "sp_verilog.vh" in clk_gate.v
verilator --trace --debug --debugi 0 -gdbbt --no-dump-tree --cc makerchip.sv --exe --build sim_main.cpp

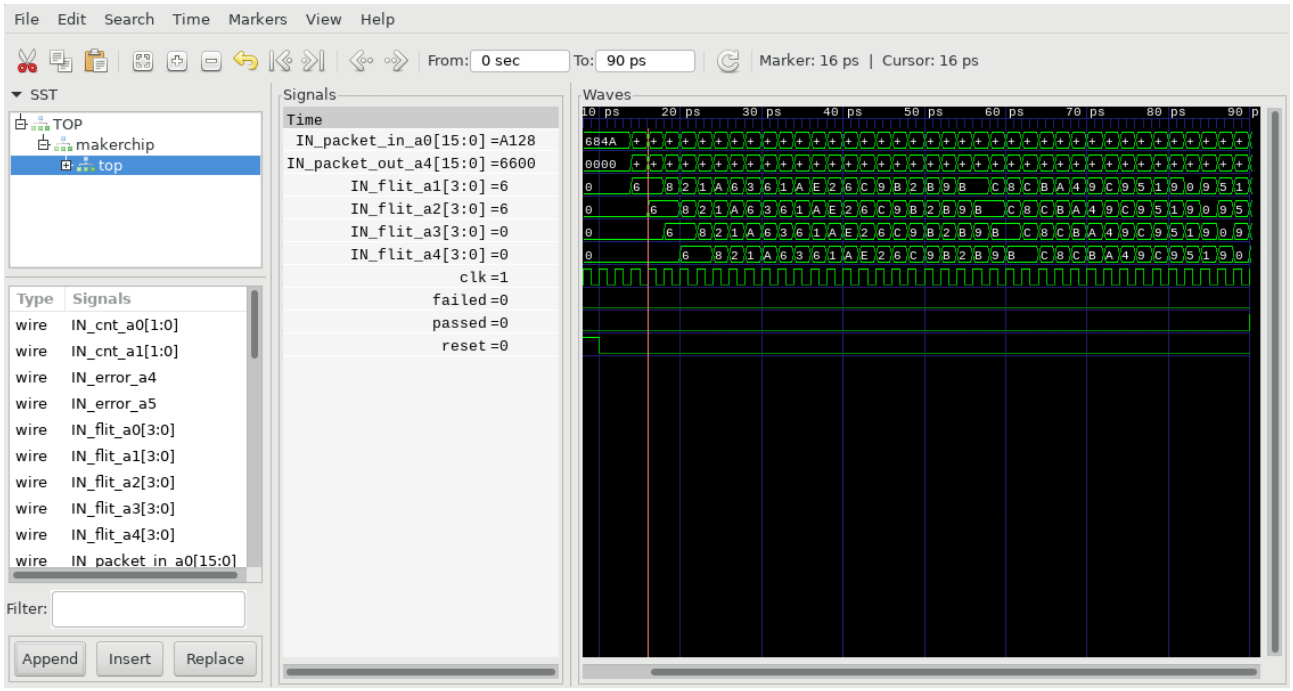
A wide vector, at a 1/4 "frequency" (1 valid cycle, followed by 3 invalid ones)
is time-division multiplexed (TDM) into a narrow vector, carrying one of n pieces per cycle,
(1st, least-significant flit in stage 0, 2nd in stage 2, etc.)
and this is de-multiplexed into a stream similar to the original in the same pipeline.
This is a useful design pattern for reducing wire routing.



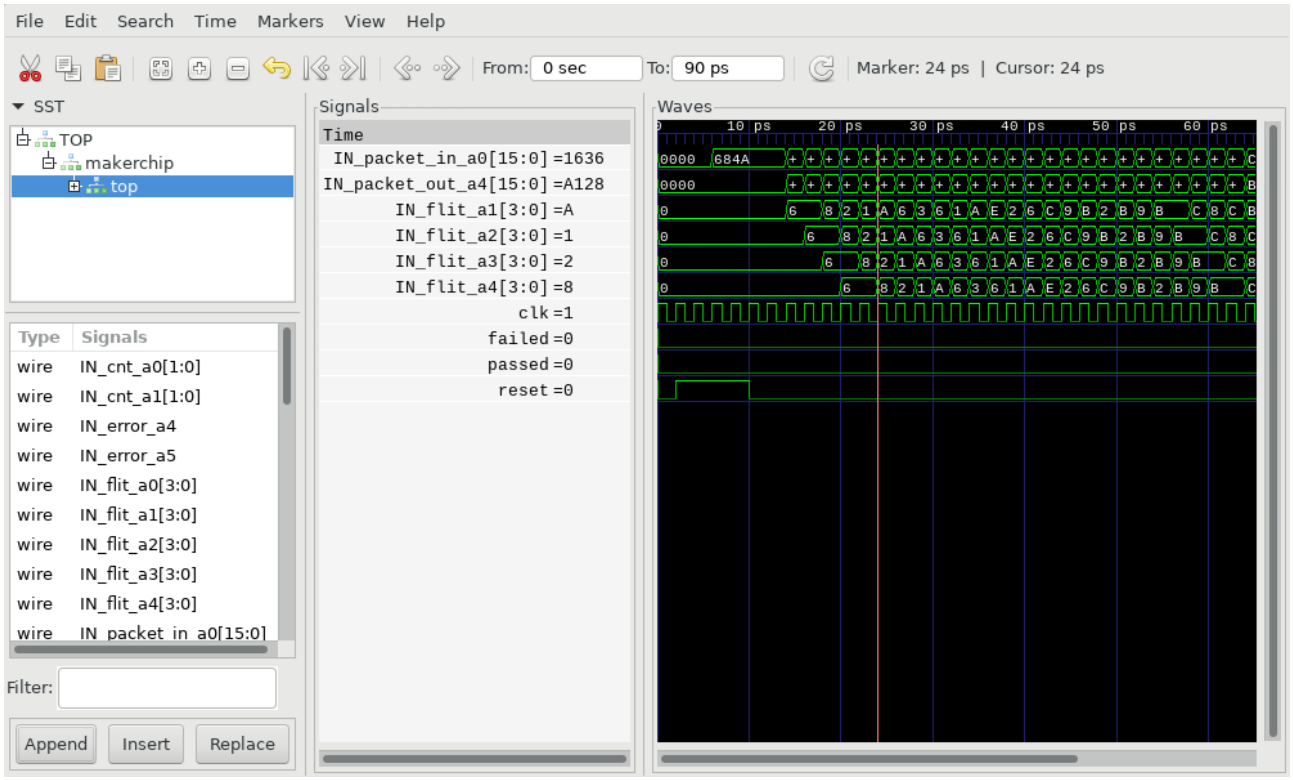

```
diff output.txt ../output.txt
2,11c2,9
< a128 became a128
< 1636 became 1636
< 62ea became 62ea
< 2b9c became 2b9c
< bb9b became bb9b
< bc8c became bc8c
< c94a became c94a
< 9159 became 9159
< 1590 became 1590
< Simulation PASSED!!!
---
> a128 became 0
> 1636 became 0
> 62ea became 0
> 2b9c became 0
> bb9b became 0
> bc8c became 0
> c94a became 0
> Simulation FAILED!!!
```



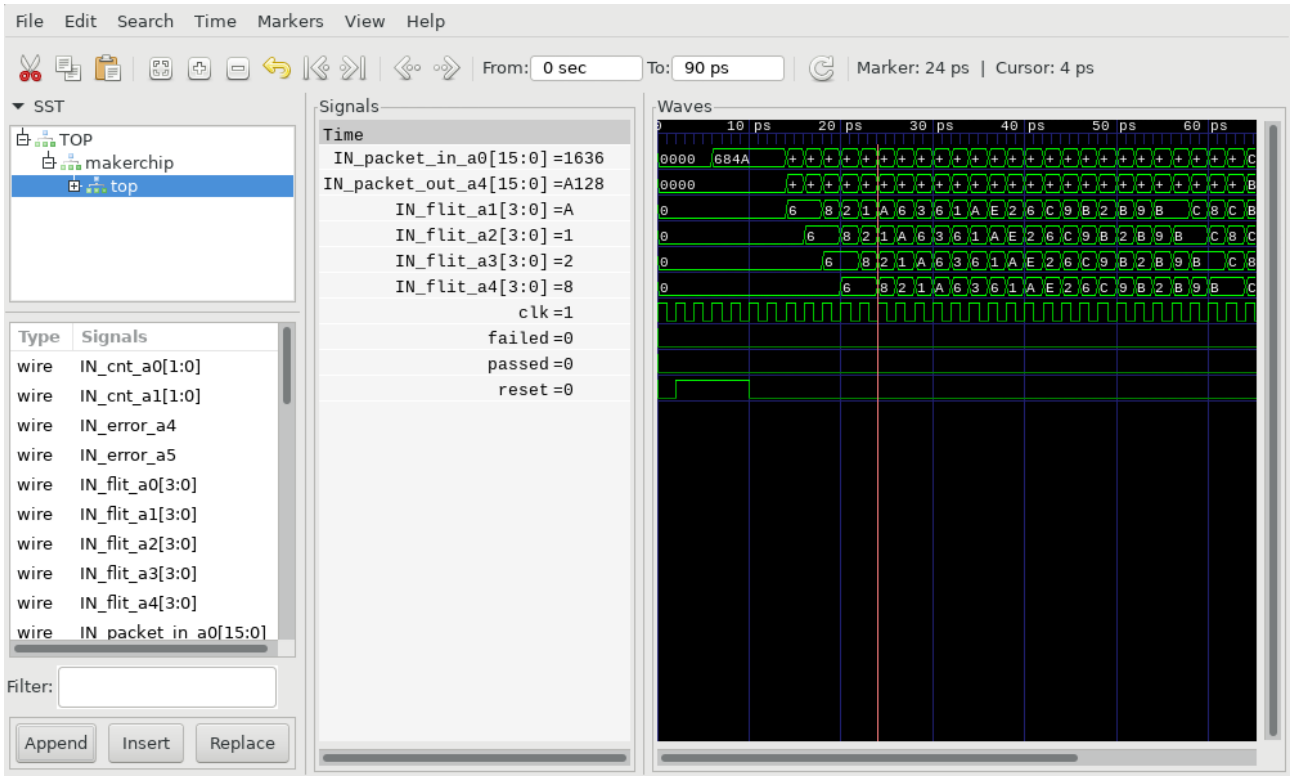

```
diff top.m4 ../top.m4
31,34c31,35
<         $flit[3:0] = >>0$valid ? >>0$packet_in[3:0] :
<                      >>1$valid ? >>1$packet_in[7:4] :
<                      >>2$valid ? >>2$packet_in[11:8] :
<                                  >>3$packet_in[15:12];
---
>
>         // LAB PART 1
>         // FILL IN THIS LINE:
>         // $flit[3:0] = ...;  // HINT: Use ? : ? : ...
>
39c40,43
<            $packet_out[15:0] = {<<3$flit, <<2$flit, <<1$flit, <>0$flit};
---
>
>            // LAB PART 2
>            // FILL IN THIS LINE:
>            // $packet_out[15:0] = ...;  // HINT: Use { , , …}
```



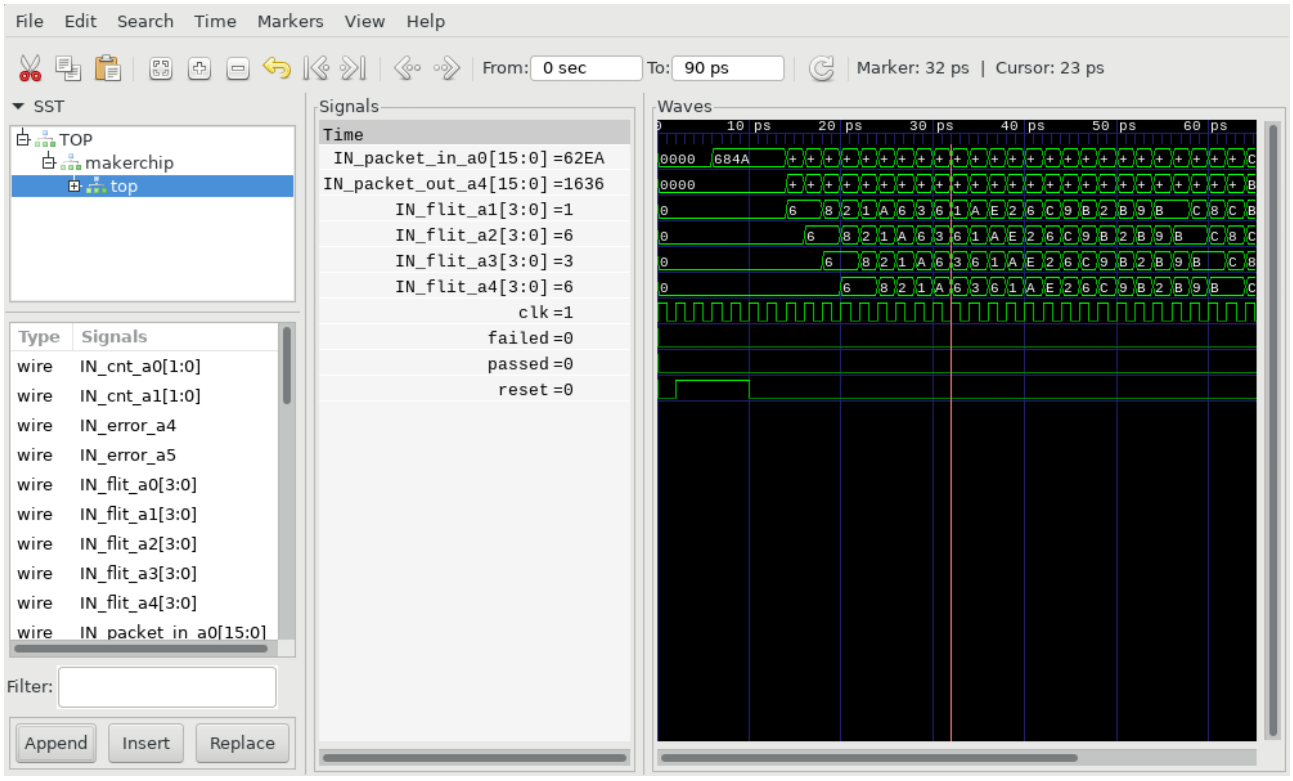

packet_1_in



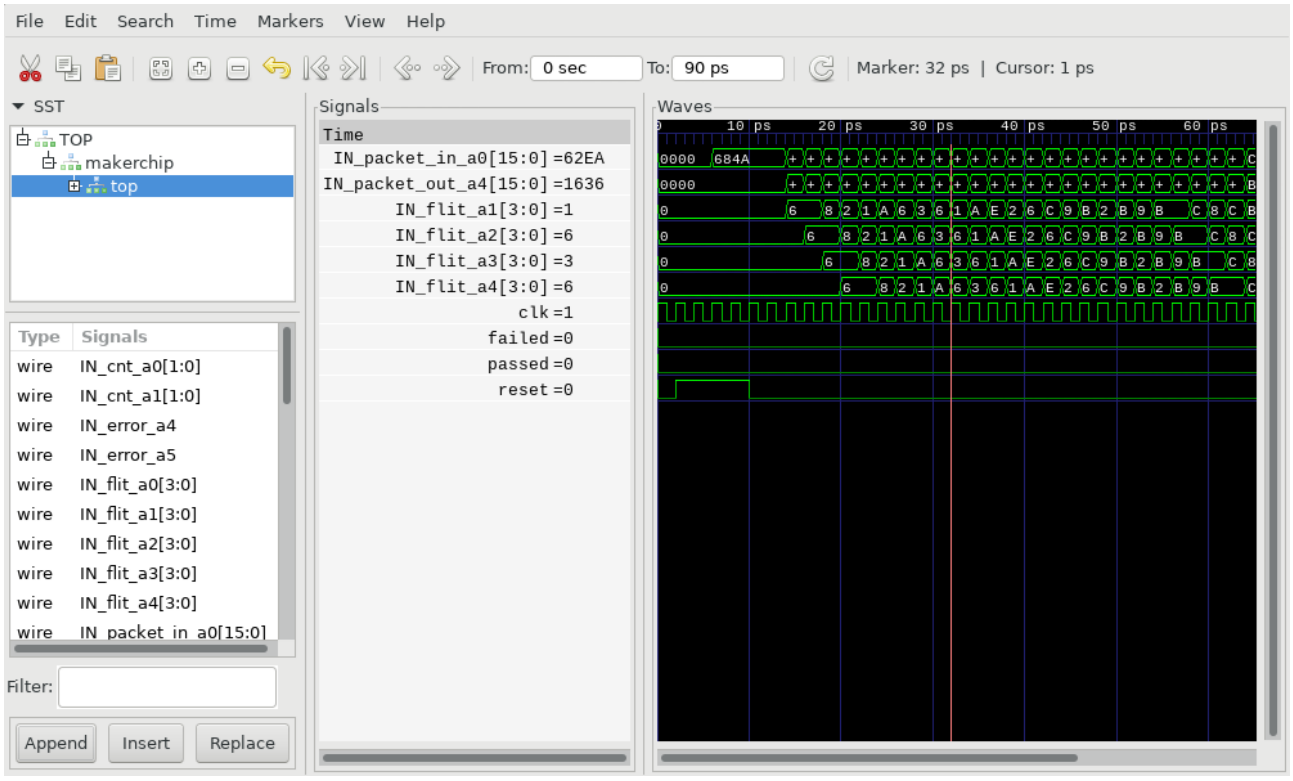

packet_1_out


File Edit Search Time Markers View Help
From: 0 sec
To: 90 ps
Marker: 24 ps | Cursor: 4 ps
SST
TOP
makerchip
top
Type Signals
wire IN_cnt_a0[1:0]
wire IN_cnt_a1[1:0]
wire IN_error_a4
wire IN_error_a5
wire IN_flit_a0[3:0]
wire IN_flit_a1[3:0]
wire IN_flit_a2[3:0]
wire IN_flit_a3[3:0]
wire IN_flit_a4[3:0]
wire IN_packet_in_a0[15:0]
Filter:
Append
Insert
Replace
Signals
Time
IN_packet_in_a0[15:0] =1636
IN_packet_out_a4[15:0] =A128
IN_flit_a1[3:0] =A
IN_flit_a2[3:0] =1
IN_flit_a3[3:0] =2
IN_flit_a4[3:0] =8
clk =1
failed =0
passed =0
reset =0
Waves
10 ps
20 ps
30 ps
40 ps
50 ps
60 ps

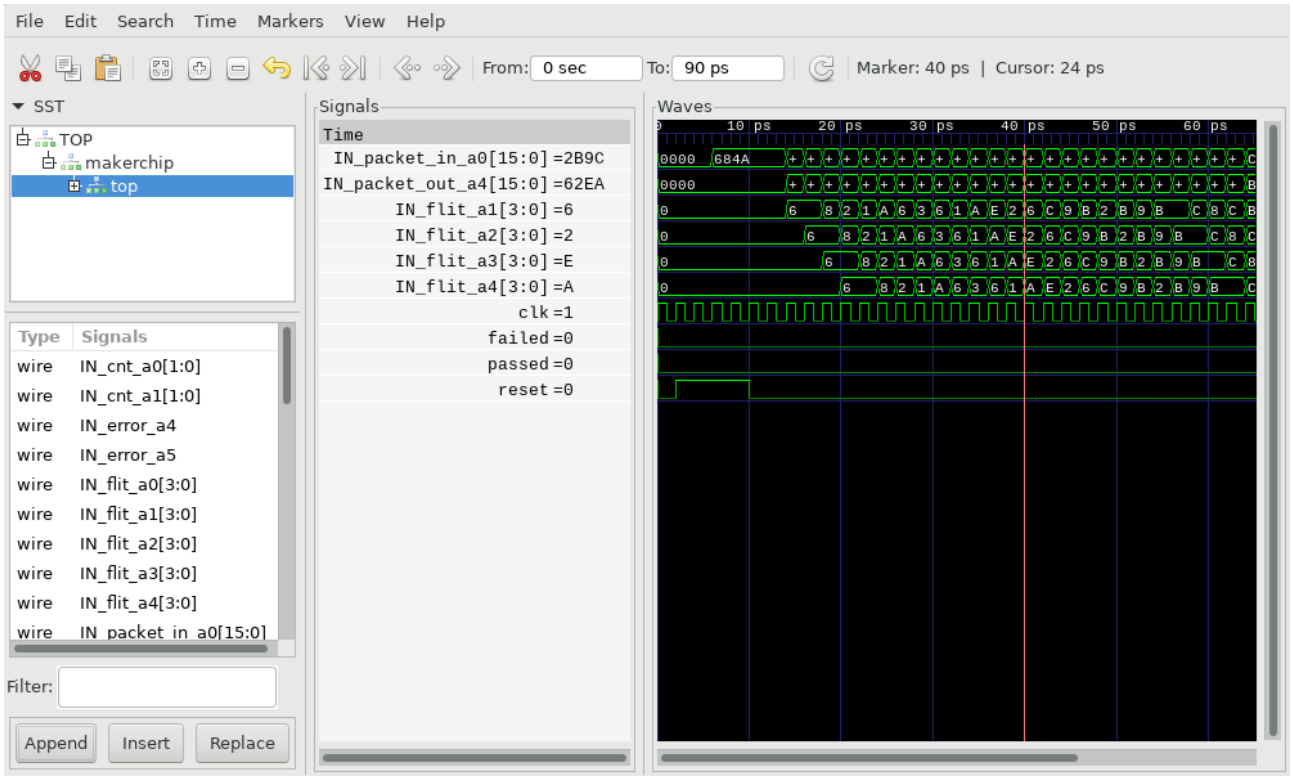
packet_2_in


File Edit Search Time Markers View Help
From: 0 sec
To: 90 ps
Marker: 32 ps | Cursor: 23 ps
SST
TOP
makerchip
top
Type Signals
wire IN_cnt_a0[1:0]
wire IN_cnt_a1[1:0]
wire IN_error_a4
wire IN_error_a5
wire IN_flit_a0[3:0]
wire IN_flit_a1[3:0]
wire IN_flit_a2[3:0]
wire IN_flit_a3[3:0]
wire IN_flit_a4[3:0]
wire IN_packet_in_a0[15:0]
Filter:
Append
Insert
Replace
Signals
Time
IN_packet_in_a0[15:0] =62EA
IN_packet_out_a4[15:0] =1636
IN_flit_a1[3:0] =1
IN_flit_a2[3:0] =6
IN_flit_a3[3:0] =3
IN_flit_a4[3:0] =6
clk =1
failed =0
passed =0
reset =0
Waves
10 ps
20 ps
30 ps
40 ps
50 ps
60 ps

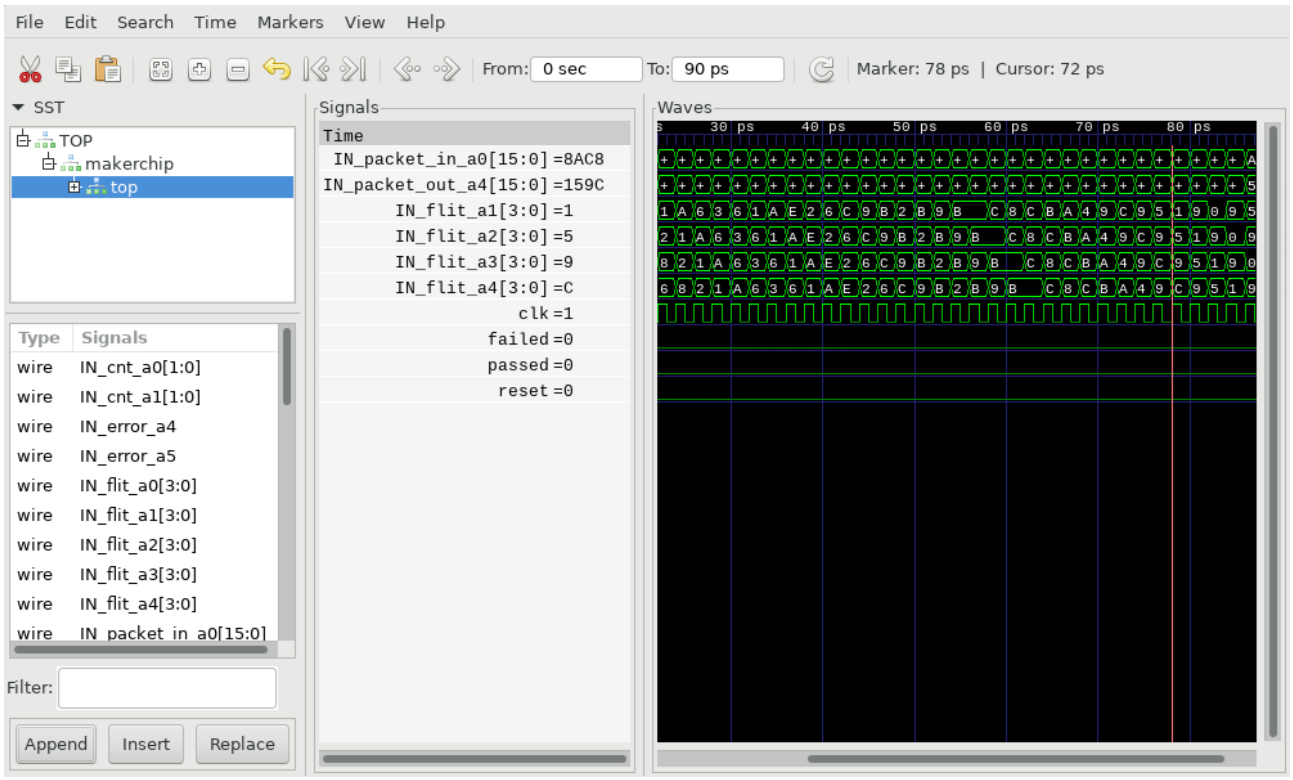
packet_2_out


File Edit Search Time Markers View Help
From: 0 sec
To: 90 ps
Marker: 32 ps | Cursor: 1 ps
SST
TOP
makerchip
top
Type Signals
wire IN_cnt_a0[1:0]
wire IN_cnt_a1[1:0]
wire IN_error_a4
wire IN_error_a5
wire IN_flit_a0[3:0]
wire IN_flit_a1[3:0]
wire IN_flit_a2[3:0]
wire IN_flit_a3[3:0]
wire IN_flit_a4[3:0]
wire IN_packet_in_a0[15:0]
Filter:
Append
Insert
Replace
Signals
Time
IN_packet_in_a0[15:0] =62EA
IN_packet_out_a4[15:0] =1636
IN_flit_a1[3:0] =1
IN_flit_a2[3:0] =6
IN_flit_a3[3:0] =3
IN_flit_a4[3:0] =6
clk =1
failed =0
passed =0
reset =0
Waves
10 ps
20 ps
30 ps
40 ps
50 ps
60 ps

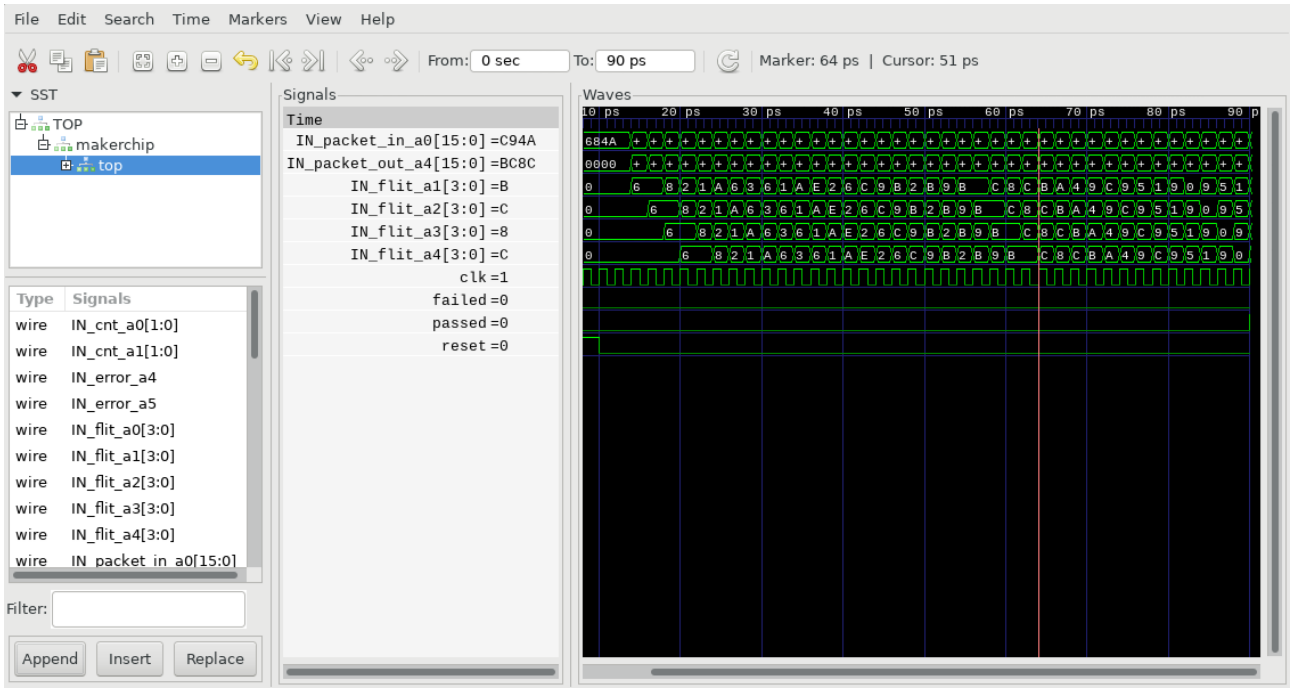
packet_3_in



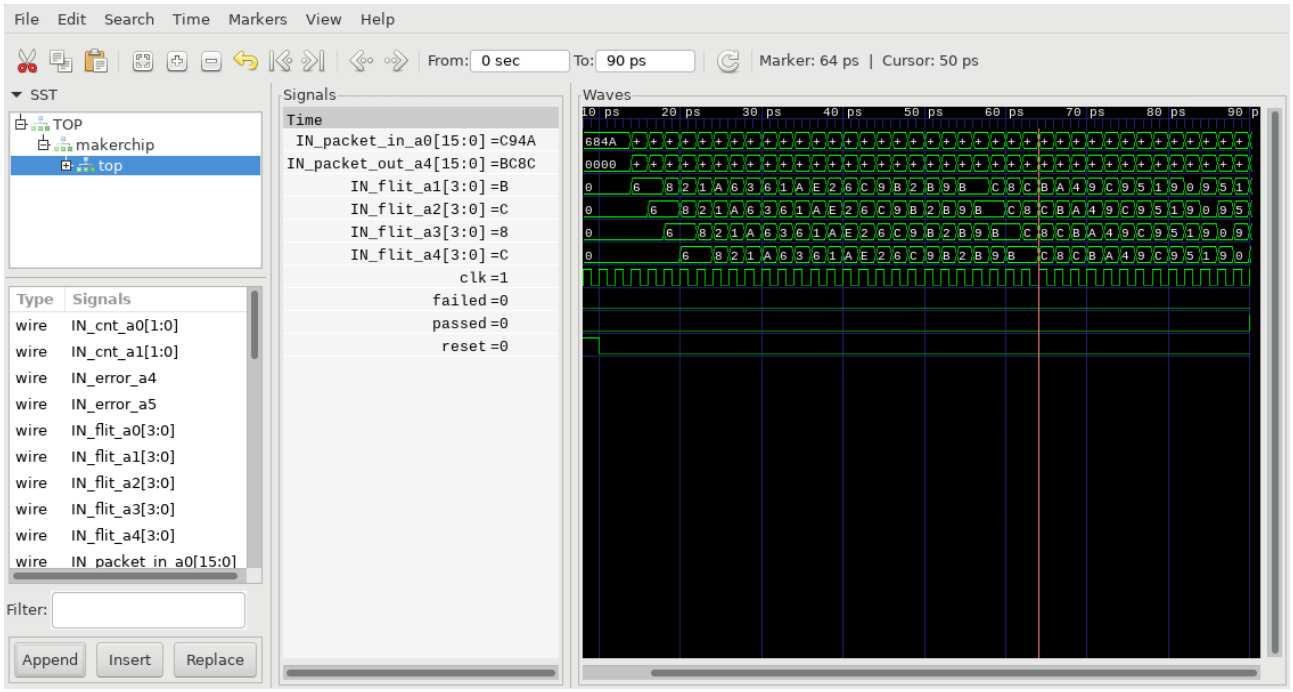

packet_3_out



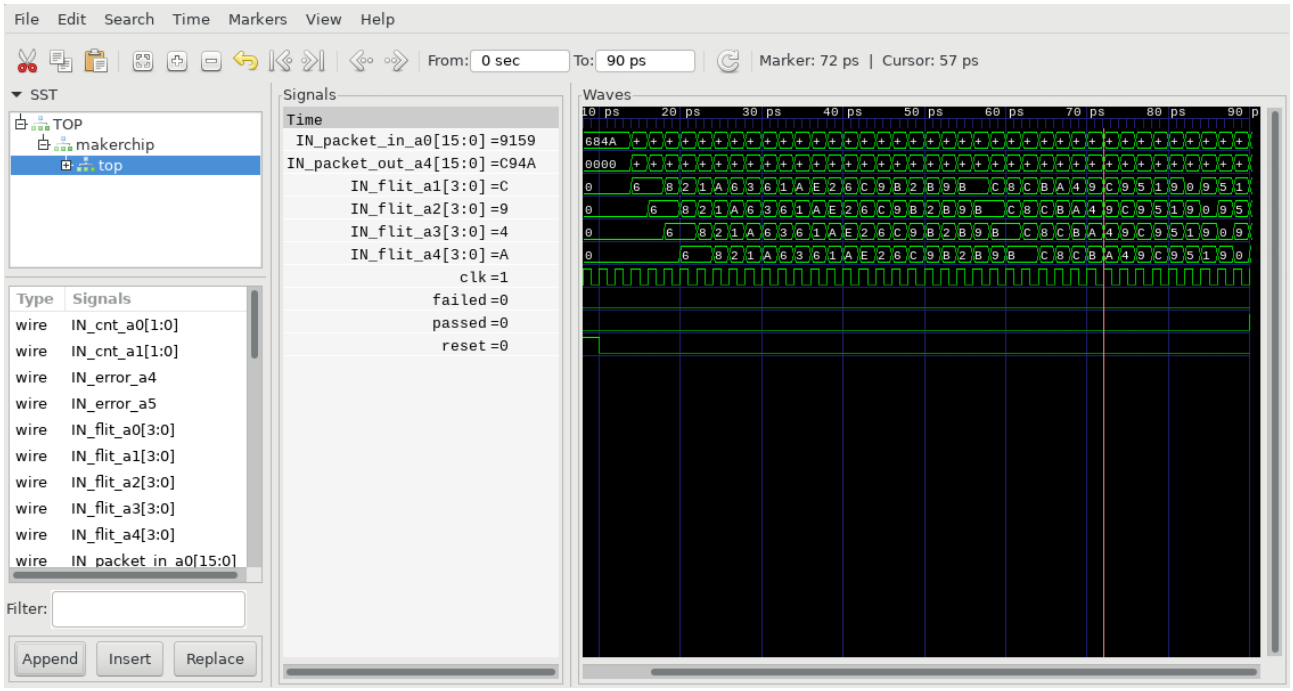

packet_6_in




packet_6_out




packet_7_in


File Edit Search Time Markers View Help
From: 0 sec
To: 90 ps
Marker: 72 ps | Cursor: 57 ps
SST
TOP
makerchip
top
Signals
Time
IN_packet_in_a0[15:0] =9159
IN_packet_out_a4[15:0] =C94A
IN_flit_a1[3:0] =C
IN_flit_a2[3:0] =9
IN_flit_a3[3:0] =4
IN_flit_a4[3:0] =A
clk =1
failed =0
passed =0
reset =0
Waves
10 ps
20 ps
30 ps
40 ps
50 ps
60 ps
70 ps
80 ps
Type Signals
wire IN_cnt_a0[1:0]
wire IN_cnt_a1[1:0]
wire IN_error_a4
wire IN_error_a5
wire IN_flit_a0[3:0]
wire IN_flit_a1[3:0]
wire IN_flit_a2[3:0]
wire IN_flit_a3[3:0]
wire IN_flit_a4[3:0]
wire IN_packet_in_a0[15:0]
Filter:
Append
Insert
Replace

packet_7_out