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EDITOR NAV-TLV DIAGRAM VIZ WAVEFORM Cycle: 0

```

226
227
228
229
230 @5
231     $ld_da
232 // Assert th
233 // *passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243     m4+imem(@
244     m4+rf(@2,
245     m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250     endmodule
251

```

	Reg	File	Mini DMem
0	0	0: 0	0: 0
1	1	1: 1	1: 1
2	2	2: 2	2: 2
3	3	3: 3	3: 3
4	4	4: 4	4: 4
5	5	5: 5	5: 5
6	6	6: 6	6: 6
7	7	7: 7	7: 7
8	8	8: 8	8: 8
9	9	9: 9	9: 9
10	10	10: 10	10: 10
11	11	11: 11	11: 11
12	12	12: 12	12: 12
13	13	13: 13	13: 13
14	14	14: 14	14: 14
15	15	15: 15	15: 15
16	16	16: 16	
17	17	17: 17	

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EDITOR NAV-TLV DIAGRAM VIZ WAVEFORM

Cycle: 1

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	10	10: 10
11:	11	11: 11
12:	12	12: 12
13:	13	13: 13
14:	14	14: 14
15:	15	15: 15
16:	16	16: 16
17:	17	17: 17

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EDITOR NAV-TLV DIAGRAM VIZ WAVEFORM

Cycle: 3

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	10	10: 10
11:	11	11: 11
12:	12	12: 12
13:	13	13: 13
14:	14	14: 14
15:	15	15: 15
16:	16	16: 16
17:	17	17: 17

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Cycle: 4

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	0(10)	10: 10
11:	11	11: 11
12:	12	12: 12
13:	13	13: 13
14:	14	14: 14
15:	15	15: 15
16:	16	16: 16
17:	17	17: 17

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EDITOR NAV-TLV DIAGRAM VIZ WAVEFORM

Cycle: 5

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	0	10: 10
11:	11	11: 11
12:	12	12: 12
13:	13	13: 13
14:	0(14)	14: 14
15:	15	15: 15
16:	16	
17:	17	

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EDITOR **NAV-TLV** **DIAGRAM** **VIZ** **WAVEFORM**

Cycle: 6

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

	Reg File	Mem DMem
0: 0	0: 0	0: 0
1: 1	1: 1	1: 1
2: 2	2: 2	2: 2
3: 3	3: 3	3: 3
4: 4	4: 4	4: 4
5: 5	5: 5	5: 5
6: 6	6: 6	6: 6
7: 7	7: 7	7: 7
8: 8	8: 8	8: 8
9: 9	9: 9	9: 9
10: 0	10: 10	
11: 11	11: 11	
12: 10(12)	12: 12	
13: 13	13: 13	
14: 0	14: 14	
15: 15	15: 15	
16: 16	16: 16	
17: 17	17: 17	

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Cycle: 8

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	0	10: 10
11:	11	11: 11
12:	10	12: 12
13:	0	13: 13
14:	0(0)	14: 14
15:	15	15: 15
16:	16	
17:	17	

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```
226
227 // Edmon
228 // E ▾
229 // 230 @5
231 $ld_da
232 // Assert th
233 // *passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@,
245 m4+dmem(@
246
247 m4+cpu viz(@

(R) ADD r10,r0,r0 : 00000000000000000000000010100110011
(R) ADD r14,r10,r0 : 00000000000000001010000011100110011
(I) ADDI r12,r10,1010 : 0000000001010010100000110000100011
(R) ADD r13,r10,r0 : 0000000000000000101000001110101100011
(R) ADD r14,r13,r14 : 000000000111001101000011100110011
-> (I) ADDI r13,r13,1 : 0000000000010110100000110100100011
(B) BLT r13,r12,1111111111000 : 1111111011000110110011000111
(R) ADD r10,r14,r0 : 000000000000001110000010100110011
(S) SW r0,r10,100 : 000000000101000000010001000100011
(I) LW r15,r0,100 : 0000000001000000001000111100000011
```

	Reg File	Mem DMem
r13 (1)	0: 0	0: 0
= ADDI	1: 1	1: 1
r13 (0)	2: 2	2: 2
i[1]	3: 3	3: 3
	4: 4	4: 4
	5: 5	5: 5
	6: 6	6: 6
	7: 7	7: 7
	8: 8	8: 8
	9: 9	9: 9
	10: 0	10: 10
	11: 11	11: 11
	12: 10	12: 12
	13: 1(0)	13: 13
	14: 0	14: 14
	15: 15	15: 15
	16: 16	Last updated an hour ago
	17: 17	

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yt dump.ycd ^ top.m4

top.m4.pre

top.tlv

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EDITOR NAV-TLV DIAGRAM VIZ WAVEFORM

Cycle: 10

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	10	10: 10
11:	11	11: 11
12:	10	12: 12
13:	1	13: 13
14:	0	14: 14
15:	15	15: 15
16:	16	16: 16
17:	17	17: 17

rx = BLT
r13 (1)
r12 (10)
i[4294967288]

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 11

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	0	10: 10
11:	11	11: 11
12:	10	12: 12
13:	1	13: 13
14:	0	14: 14
15:	15	15: 15
16:	16	16: 16
17:	17	17: 17

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 12

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	10	10: 10
11:	11	11: 11
12:	10	12: 12
13:	1	13: 13
14:	0	14: 14
15:	15	15: 15
16:	16	16: 16
17:	17	17: 17

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 13

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	0	10: 10
11:	11	11: 11
12:	10	12: 12
13:	1	13: 13
14:	1(0)	14: 14
15:	15	15: 15
16:	16	
17:	17	

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```
226 // Sdmom
227 // E ▾
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 // *passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 @
248
249 @
250 m4+cpu_viz(@
251 \SV
252 endmodule
```

(R) ADD r10,r0,r0	:	0000000000000000000000000000000010100110011
(R) ADD r14,r10,r0	:	00000000000000001010000011100110011
(I) ADDI r12,r10,1010	:	00000000101001010000011000010011
(R) ADD r13,r10,r0	:	00000000000000001010000011010110011
(R) ADD r14,r13,r14	:	000000000111001101000011100110011
-> (I) ADDI r13,r13,1	:	000000000001011010000110100100110011
(B) BLT r13,r12,1111111111000	:	111111101100011011001100111100011
(R) ADD r10,r14,r0	:	000000000000011100000101001100110011
(S) SW r0,r10,100	:	00000000101000000010010001000100011
(I) LW r15,r0,100	:	00000000010000000010011110000011

	Reg File	Mem DMem
r13 (2)	0: 0	0: 0
= ADDI	1: 1	1: 1
r13 (1)	2: 2	2: 2
i[1]	3: 3	3: 3
	4: 4	4: 4
	5: 5	5: 5
	6: 6	6: 6
	7: 7	7: 7
	8: 8	8: 8
	9: 9	9: 9
	10: 0	10: 10
	11: 11	11: 11
	12: 10	12: 12
	13: 2(1)	13: 13
	14: 1	14: 14
	15: 15	15: 15
	16: 16	Last updated an hour ago
	17: 17	

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 15

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

	Reg File	Mem DMem
0: 0	0: 0	0: 0
1: 1	1: 1	1: 1
2: 2	2: 2	2: 2
3: 3	3: 3	3: 3
4: 4	4: 4	4: 4
5: 5	5: 5	5: 5
6: 6	6: 6	6: 6
7: 7	7: 7	7: 7
8: 8	8: 8	8: 8
9: 9	9: 9	9: 9
10: 0	10: 10	
11: 11	11: 11	
12: 10	12: 12	
13: 2	13: 13	
14: 1	14: 14	
15: 15	15: 15	
16: 16	16: 16	
17: 17	17: 17	

rx = BLT
r13 (2)
r12 (10)
i[4294967288]

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 16

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

	Reg	File	Mem
0: 0	0: 0	0: 0	
1: 1	1: 1	1: 1	
2: 2	2: 2	2: 2	
3: 3	3: 3	3: 3	
4: 4	4: 4	4: 4	
5: 5	5: 5	5: 5	
6: 6	6: 6	6: 6	
7: 7	7: 7	7: 7	
8: 8	8: 8	8: 8	
9: 9	9: 9	9: 9	
10: 0	10: 0	10: 10	
11: 11	11: 11	11: 11	
12: 10	12: 10	12: 12	
13: 2	13: 2	13: 13	
14: 1	14: 1	14: 14	
15: 15	15: 15	15: 15	
16: 16	16: 16	16: 16	
17: 17	17: 17	17: 17	

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 17

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

	Reg File	Mem DMem
0: 0	0: 0	0: 0
1: 1	1: 1	1: 1
2: 2	2: 2	2: 2
3: 3	3: 3	3: 3
4: 4	4: 4	4: 4
5: 5	5: 5	5: 5
6: 6	6: 6	6: 6
7: 7	7: 7	7: 7
8: 8	8: 8	8: 8
9: 9	9: 9	9: 9
10: 0	10: 10	
11: 11	11: 11	
12: 10	12: 12	
13: 2	13: 13	
14: 1	14: 14	
15: 15	15: 15	
16: 16	16: 16	
17: 17	17: 17	

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 18

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	0	10: 10
11:	11	11: 11
12:	10	12: 12
13:	2	13: 13
14:	3(1)	14: 14
15:	15	15: 15
16:	16	
17:	17	

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EDITOR NAV-TLV DIAGRAM VIZ WAVEFORM

Cycle: 19

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

Reg	File	Mem
0:	0	0: 0
1:	1	1: 1
2:	2	2: 2
3:	3	3: 3
4:	4	4: 4
5:	5	5: 5
6:	6	6: 6
7:	7	7: 7
8:	8	8: 8
9:	9	9: 9
10:	0	10: 10
11:	11	11: 11
12:	10	12: 12
13:	3(2)	13: 13
14:	3	14: 14
15:	15	15: 15
16:	16	
17:	17	

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 20

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

	Reg File	Mem DMem
0: 0	0: 0	0: 0
1: 1	1: 1	1: 1
2: 2	2: 2	2: 2
3: 3	3: 3	3: 3
4: 4	4: 4	4: 4
5: 5	5: 5	5: 5
6: 6	6: 6	6: 6
7: 7	7: 7	7: 7
8: 8	8: 8	8: 8
9: 9	9: 9	9: 9
10: 0	10: 10	
11: 11	11: 11	
12: 10	12: 12	
13: 3	13: 13	
14: 3	14: 14	
15: 15		15: 15
16: 16		16: 16
17: 17		17: 17

rx = BLT
r13 (3)
r12 (10)
i[4294967288]

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 21

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 [cpu]
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

	Reg	File	Mem
0: 0	0: 0	0: 0	
1: 1	1: 1	1: 1	
2: 2	2: 2	2: 2	
3: 3	3: 3	3: 3	
4: 4	4: 4	4: 4	
5: 5	5: 5	5: 5	
6: 6	6: 6	6: 6	
7: 7	7: 7	7: 7	
8: 8	8: 8	8: 8	
9: 9	9: 9	9: 9	
10: 0	10: 0	10: 10	
11: 11	11: 11	11: 11	
12: 10	12: 10	12: 12	
13: 3	13: 3	13: 13	
14: 3	14: 3	14: 14	
15: 15	15: 15	15: 15	
16: 16	16: 16	16: 16	
17: 17	17: 17	17: 17	

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EDITOR NAV-TIV DIAGRAM VIZ WAVEFORM

Cycle: 22

```

226
227 // E
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 /*passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rf(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251

```

	Reg File	Mem DMem
0: 0	0: 0	0: 0
1: 1	1: 1	1: 1
2: 2	2: 2	2: 2
3: 3	3: 3	3: 3
4: 4	4: 4	4: 4
5: 5	5: 5	5: 5
6: 6	6: 6	6: 6
7: 7	7: 7	7: 7
8: 8	8: 8	8: 8
9: 9	9: 9	9: 9
10: 0	10: 10	
11: 11	11: 11	
12: 10	12: 12	
13: 3	13: 13	
14: 3	14: 14	
15: 15	15: 15	
16: 16	16: 16	
17: 17	17: 17	

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```
226 // Sdmom
227 // E ▾
228 //
229 //
230 @5
231 $ld_da
232 // Assert th
233 // *passed =
234 *passed = |c
235 *failed = 1'
236
237 // Macro ins
238 // o instru
239 // o regist
240 // o data m
241 // o CPU vi
242 |cpu
243 m4+imem(@
244 m4+rif(@2,
245 m4+dmem(@
246
247 m4+cpu_viz(@
248
249 \SV
250 endmodule
251
```

(R) ADD r10,r0,r0	:	0000000000000000000000000000000010100110011
(R) ADD r14,r10,r0	:	00000000000000001010000011100110011
(I) ADDI r12,r10,1010	:	00000000101001010000011000010011
(R) ADD r13,r10,r0	:	00000000000000001010000011010110011
-> (R) ADD r14,r13,r14	:	00000000111001101000011100110011
(I) ADDI r13,r13,1	:	000000000000101101000011010010011
(B) BLT r13,r12,1111111111000	:	111111101100011011001100111100011
(R) ADD r10,r14,r0	:	00000000000000001100000010100110011
(S) SW r0,r10,100	:	0000000000101000000010010001000110011
(I) LW r15,r0,100	:	000000000010000000100111100000011

	Reg File	Mem DMem
r14 (6)	0: 0	0: 0
= ADD	1: 1	1: 1
r13 (3)	2: 2	2: 2
r14 (3)	3: 3	3: 3
i[0]	4: 4	4: 4
	5: 5	5: 5
	6: 6	6: 6
	7: 7	7: 7
	8: 8	8: 8
	9: 9	9: 9
	10: 0	10: 10
	11: 11	11: 11
	12: 10	12: 12
	13: 3	13: 13
	14: 6(3)	14: 14
	15: 15	15: 15
	16: 16	
	17: 17	

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