*reset
*passed
*failed
*syc_ent
*clk
*RW_nacl_vect

/top

/ring_stop[3:0]

|fifo2_out
/trans
$ANY=...

|arb_out
/trans
$ANY=...

|ring_out
/trans
$ANY=...

|rg
/trans
$ANY=...

|ring_in
/trans
$ANY=...

|bypass
/trans
$ANY=...

|bp3
/trans
$ANY=...

|bp2
/trans
$ANY=...

|bp1
/trans
$ANY=...

|bp0
/fifo_head
/trans
$ANY=...
/trans
$ANY=...
/head
/trans
$ANY=...
/entry[(4)-1:0]
/read_masked
/trans
$ANY=...
/accum
/trans
$ANY=...

|stall3
/entry[(4)-1:0]
/trans
$ANY=...

/trans
$ANY=...

|stall2
/trans
$ANY=...

|stall1
/trans
$ANY=...

|stall0
/trans
$ANY=...

/tb

/ring_stop[3:0]

|send
/gen_trans
/trans_out
$ANY=...

|receive2
/trans
$ANY=...

|passed

|receive1
/trans
$ANY=...

|count