**********Default**********

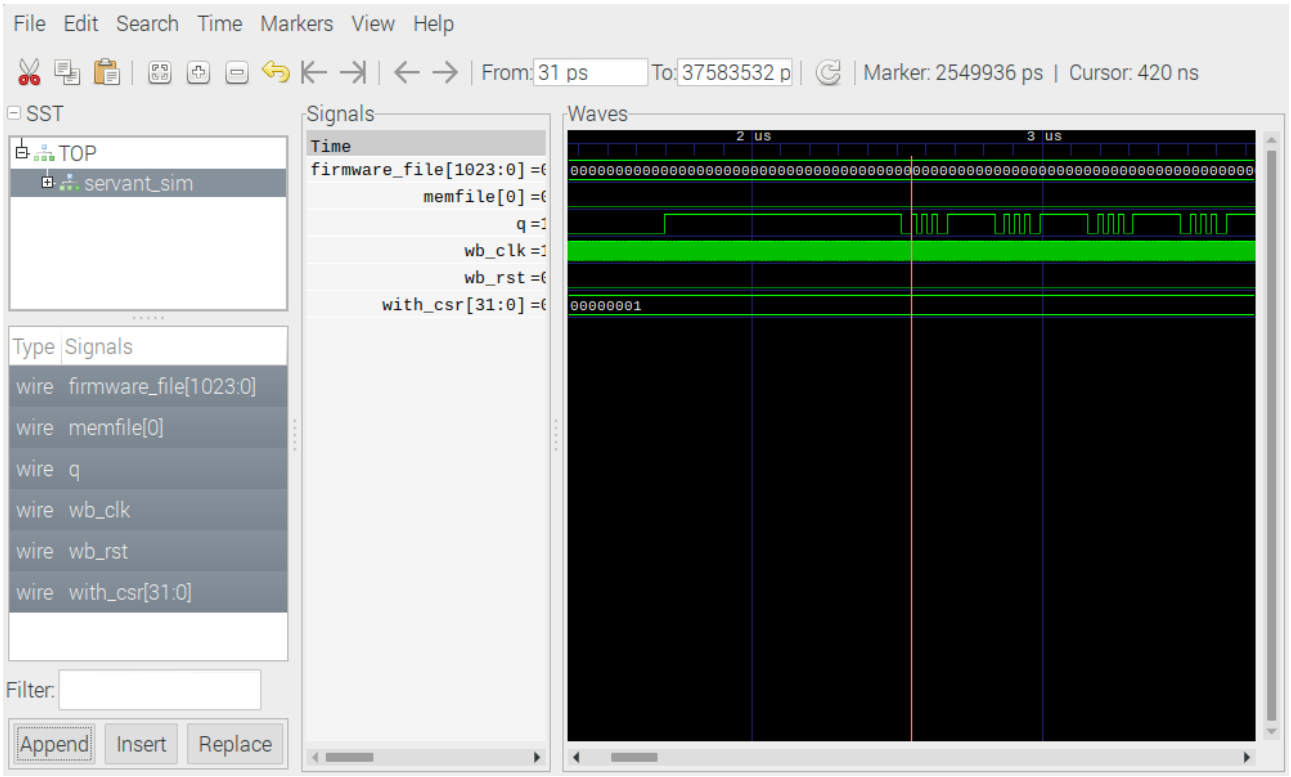
catzip-icestorm
Risc-V servant
initial build
service
09/08/21

**********Default**********

```
devel@mypi3-20:~/WORKSPACE $ export WORKSPACE=/home/devel/WORKSPACE/
devel@mypi3-20:~/WORKSPACE $ export
SERV=/home/devel/WORKSPACE/fusesoc_libraries/serv
devel@mypi3-20:~/WORKSPACE $ fusesoc run --target=verilator_tb servant --vcd --
uart_baudrate=57600 --firmware=$SERV/sw/zephyr_hello.hex
INFO: Preparing ::serv:1.1.0
INFO: Preparing ::servant:1.1.0
INFO: Setting up project

INFO: Building simulation model
verilator -f servant_1.1.0.vc --trace
make  -f Vservant_sim.mk
make[1]: Entering directory '/home/devel/WORKSPACE/build/servant_1.1.0/verilator_tb-verilator'
g++  -I.  -MMD -I/usr/local/share/verilator/include -I/usr/local/share/verilator/include/vltstd -
DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -faligned-new -fcf-protection=none -Wno-
bool-operation -Wno-sign-compare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-
unused-parameter -Wno-unused-variable -Wno-shadow      -std=gnu++14 -Os -c -o servant_tb.o
../src/servant_1.1.0/bench/servant_tb.cpp
g++  -I.  -MMD -I/usr/local/share/verilator/include -I/usr/local/share/verilator/include/vltstd -
DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -faligned-new -fcf-protection=none -Wno-
bool-operation -Wno-sign-compare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-
unused-parameter -Wno-unused-variable -Wno-shadow      -std=gnu++14 -Os -c -o verilated.o
/usr/local/share/verilator/include/verilated.cpp
g++  -I.  -MMD -I/usr/local/share/verilator/include -I/usr/local/share/verilator/include/vltstd -
DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -faligned-new -fcf-protection=none -Wno-
bool-operation -Wno-sign-compare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-
unused-parameter -Wno-unused-variable -Wno-shadow      -std=gnu++14 -Os -c -o verilated_dpi.o /
usr/local/share/verilator/include/verilated_dpi.cpp
g++  -I.  -MMD -I/usr/local/share/verilator/include -I/usr/local/share/verilator/include/vltstd -
DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -faligned-new -fcf-protection=none -Wno-
bool-operation -Wno-sign-compare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-
unused-parameter -Wno-unused-variable -Wno-shadow      -std=gnu++14 -Os -c -o
verilated_vcd_c.o /usr/local/share/verilator/include/verilated_vcd_c.cpp
/usr/bin/perl /usr/local/share/verilator/bin/verilator_includer -DVL_INCLUDE_OPT=include
Vservant_sim.cpp Vservant_sim_servant_sim.cpp Vservant_sim_servant__Mz1_MB2000_S1.cpp
Vservant_sim_servant_ram__pi1.cpp Vservant_sim__Dpi.cpp Vservant_sim__Trace.cpp
Vservant_sim__Slow.cpp Vservant_sim_servant_sim__Slow.cpp
Vservant_sim_servant__Mz1_MB2000_S1__Slow.cpp
```

```
Vservant_sim_servant_ram__pi1__Slow.cpp Vservant_sim__Syms.cpp
Vservant_sim__Trace__Slow.cpp > Vservant_sim__ALL.cpp
g++  -I.  -MMD -I/usr/local/share/verilator/include -I/usr/local/share/verilator/include/vltstd -
DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -faligned-new -fcf-protection=none -Wno-
bool-operation -Wno-sign-compare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-
unused-parameter -Wno-unused-variable -Wno-shadow      -std=gnu++14 -Os -c -o
Vservant_sim__ALL.o Vservant_sim__ALL.cpp
Archive ar -cr Vservant_sim__ALL.a Vservant_sim__ALL.o
g++    servant_tb.o verilated.o verilated_dpi.o verilated_vcd_c.o Vservant_sim__ALL.a      -o
Vservant_sim
make[1]: Leaving directory '/home/devel/WORKSPACE/build/servant_1.1.0/verilator_tb-verilator'
INFO: Running
INFO: Running simulation
Loading RAM from /home/devel/WORKSPACE/fusesoc_libraries/serv/sw/zephyr_hello.hex
***** Booting Zephyr OS zephyr-v1.14.1-4-gc7c2d62513fe *****
Hello World! Service
```



The image below is suppose to look like the first seven lines when the **sudo config_cat ~/servant_1.1.0.bin**. The first seven lines are when iCE40 FPGA is programmed with **sudo config_cat helloworld.bin in the testbuilds/catzip/rtl/uart folder.**

```
File  Edit  Tabs  Help
Hello, World!
Hello, World!
Hello, World!
Hello, World!
Hello, World!
Hello, World!
Hello, World!
ÔÔÔÔÔÐà÷÷úÕöóÐìóøÔýøÐçéÐüóøôýø×úÙÖÙÚÖÙ×Ú×óñÛñØòÚØÛÙÙòÓÐÔÔÔÔÔÇÄäóöö÷Ðë÷øöòÑÐùóøúÄ
```

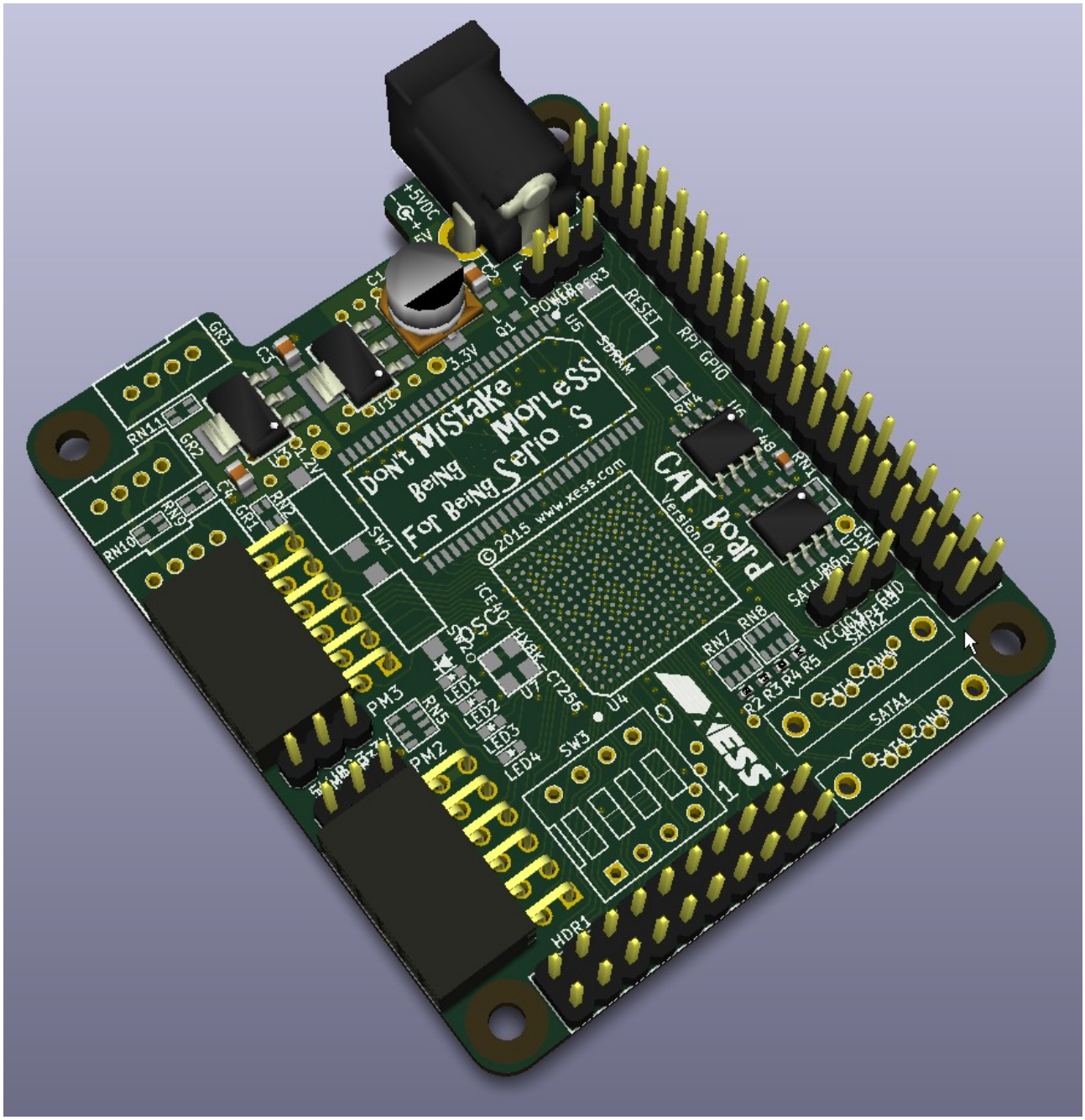
A pmodusb is connected to PM2 on Catboard.

Features include:

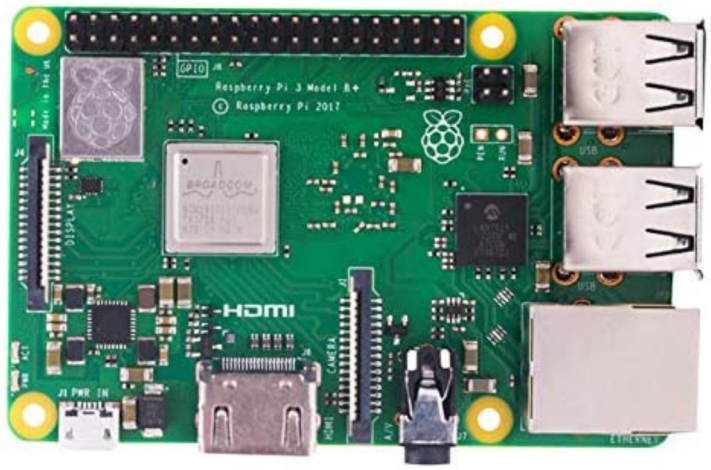
- USB to serial UART interface
- Option to power the system board through the FTDI chip

The PmodUSBUART.

CatBoard



Raspberry Pi 3B+ is running Raspberry Pi OS.



The USB is connected to The USB on Raspberry Pi3B+ which also has a catboard mounted on the 40 GPIO connector.

The serial port is setup as follows.

```
File  Edit  Tabs  Help
Hello, World!
Hello, World!
Hello, World!
Hell+--------------------------------------------------------------------------+
Hell| A -    Serial Device      : /dev/ttyUSB0                                 |
Hell| B - Lockfile Location     : /var/lock                                    |
Hell| C -   Callin Program      :                                              |
ÔÔÔÔ| D -  Callout Program      :                                             |øúÄ
    | E -    Bps/Par/Bits       : 115200 8N1                                   |
    | F - Hardware Flow Control : No                                           |
    | G - Software Flow Control : No                                           |
    |                                                                          |
    |    Change which setting?                                                 |
    +--------------------------------------------------------------------------+
          | Screen and keyboard      |
          | Save setup as dfl        |
          | Save setup as..          |
          | Exit                     |
          +--------------------------+

CTRL-A Z for help | 115200 8N1 | NOR | Minicom 2.7.1 | VT102 | Offline | tyUSB0
```

Other tools required are icestorm, yosys, nextpnr, and verilator.

Needed to install fusesoc

pip3 install --upgrade --user fusesoc

fusesoc --version
1.12.0

Forked https://github.com/olofk/serv

git clone git@github.com:develone/serv.git

Created a Pull request.

mkdir WORKSPACE

cd WORKSPACE/

export WORKSPACE=/home/devel/WORKSPACE/

echo $WORKSPACE
/home/devel/WORKSPACE/

export SERV=/home/devel/WORKSPACE/fusesoc_libraries/serv

echo $SERV
/home/devel/WORKSPACE/fusesoc_libraries/serv

fusesoc library add fusesoc_cores https://github.com/fusesoc/fusesoc-cores

fusesoc library add serv https://github.com/olofk/serv

cp ~/serv/servant.core ~/WORKSPACE/fusesoc_libraries/serv/
cp ~/serv/data/catzip.pcf ~/WORKSPACE/fusesoc_libraries/serv/data

fusesoc run --target=catzip servant creates the folder
build/servant_1.1.0/catzip-icestorm/
blinky.hex servant_1.1.0.bin servant_1.1.0.mk
edalize_yosys_procs.tcl servant_1.1.0.blif servant_1.1.0_next.asc
edalize_yosys_template.tcl servant_1.1.0.eda.yml yosys.log
Makefile servant_1.1.0.edif zephyr_hello.hex
next.log servant_1.1.0.json

serv/servant/service.v

```
`default_nettype none
module service
(
```

```
 input wire  i_clk,
 output wire q);

   parameter memfile = "zephyr_hello.hex";
   parameter memsize = 8192;
   parameter PLL = "NONE";

   wire      wb_clk;
   wire      wb_rst;

   servant_clock_gen #(.PLL (PLL))
   clock_gen
     (.i_clk (i_clk),
      .o_clk (wb_clk),
      .o_rst (wb_rst));

   servant
     #(.memfile (memfile),
       .memsize (memsize))
   servant
     (.wb_clk (wb_clk),
      .wb_rst (wb_rst),
      .q      (q));

endmodule
```

serv/servant/servant_clock_gen.v

```
`default_nettype none
module servant_clock_gen
  (
   input wire  i_clk,
   output wire o_clk,
   output wire o_rst);

   parameter [79:0] PLL = "NONE";

   generate
      if ((PLL == "ICE40_CORE") || (PLL == "ICE40_PAD")) begin
            ice40_pll #(.PLL (PLL)) pll
              (.i_clk (i_clk),
               .o_clk (o_clk),
               .o_rst (o_rst));
      end else begin
            assign o_clk = i_clk;

            reg [4:0] rst_reg = 5'b11111;

            always @(posedge o_clk)
              rst_reg <= {1'b0, rst_reg[4:1]};
            assign o_rst = rst_reg[0];
      end
```

```
  endgenerate
endmodule
```

build/servant_1.1.0/src/servant-catzip_pll_1.1.0/pll.vh

```
/**
 * PLL configuration
 *
 * This Verilog header file was generated automatically
 * using the icepll tool from the IceStorm project.
 * It is intended for use with FPGA primitives SB_PLL40_CORE,
 * SB_PLL40_PAD, SB_PLL40_2_PAD, SB_PLL40_2F_CORE or SB_PLL40_2F_PAD.
 * Use at your own risk.
 *
 * Given input frequency:       100.000 MHz
 * Requested output frequency:   40.000 MHz
 * Achieved output frequency:    40.000 MHz
 */

.FEEDBACK_PATH("SIMPLE"),
.DIVR(4'b0100),                 // DIVR =  4
.DIVF(7'b0011111),    // DIVF = 31
.DIVQ(3'b100),                  // DIVQ =  4
.FILTER_RANGE(3'b010)    // FILTER_RANGE = 2
```

serv/servant/servant.v

serv/servant/servant_abriter.v

serv/servant/servant_mux.v

serv/servant/servant_ram.v

serv/servant/servant_gpio.v

```
`default_nettype none
module servant
(
 input wire  wb_clk,
 input wire  wb_rst,
 output wire q);

   parameter memfile = "zephyr_hello.hex";
   parameter memsize = 8192;
   parameter reset_strategy = "MINI";
   parameter sim = 0;
   parameter with_csr = 1;

   wire  timer_irq;

   wire [31:0]   wb_ibus_adr;
   wire  wb_ibus_cyc;
   wire [31:0]   wb_ibus_rdt;
   wire  wb_ibus_ack;

   wire [31:0]   wb_dbus_adr;
```

```
wire [31:0]   wb_dbus_dat;
wire [3:0]    wb_dbus_sel;
wire  wb_dbus_we;
wire  wb_dbus_cyc;
wire [31:0]   wb_dbus_rdt;
wire  wb_dbus_ack;

wire [31:0]   wb_dmem_adr;
wire [31:0]   wb_dmem_dat;
wire [3:0]    wb_dmem_sel;
wire  wb_dmem_we;
wire  wb_dmem_cyc;
wire [31:0]   wb_dmem_rdt;
wire  wb_dmem_ack;

wire [31:0]   wb_mem_adr;
wire [31:0]   wb_mem_dat;
wire [3:0]    wb_mem_sel;
wire  wb_mem_we;
wire  wb_mem_cyc;
wire [31:0]   wb_mem_rdt;
wire  wb_mem_ack;

wire  wb_gpio_dat;
wire  wb_gpio_we;
wire  wb_gpio_cyc;
wire  wb_gpio_rdt;

wire [31:0]   wb_timer_dat;
wire  wb_timer_we;
wire  wb_timer_cyc;
wire [31:0]   wb_timer_rdt;

wire [31:0] mdu_rs1;
wire [31:0] mdu_rs2;
wire [ 2:0] mdu_op;
wire        mdu_valid;
wire [31:0] mdu_rd;
wire        mdu_ready;

servant_arbiter arbiter
  (.i_wb_cpu_dbus_adr (wb_dmem_adr),
   .i_wb_cpu_dbus_dat (wb_dmem_dat),
   .i_wb_cpu_dbus_sel (wb_dmem_sel),
   .i_wb_cpu_dbus_we  (wb_dmem_we ),
   .i_wb_cpu_dbus_cyc (wb_dmem_cyc),
   .o_wb_cpu_dbus_rdt (wb_dmem_rdt),
   .o_wb_cpu_dbus_ack (wb_dmem_ack),

   .i_wb_cpu_ibus_adr (wb_ibus_adr),
   .i_wb_cpu_ibus_cyc (wb_ibus_cyc),
   .o_wb_cpu_ibus_rdt (wb_ibus_rdt),
```

```
    .o_wb_cpu_ibus_ack (wb_ibus_ack),

    .o_wb_cpu_adr (wb_mem_adr),
    .o_wb_cpu_dat (wb_mem_dat),
    .o_wb_cpu_sel (wb_mem_sel),
    .o_wb_cpu_we  (wb_mem_we ),
    .o_wb_cpu_cyc (wb_mem_cyc),
    .i_wb_cpu_rdt (wb_mem_rdt),
    .i_wb_cpu_ack (wb_mem_ack));

servant_mux #(sim) servant_mux
  (
    .i_clk (wb_clk),
    .i_rst (wb_rst & (reset_strategy != "NONE")),
    .i_wb_cpu_adr (wb_dbus_adr),
    .i_wb_cpu_dat (wb_dbus_dat),
    .i_wb_cpu_sel (wb_dbus_sel),
    .i_wb_cpu_we  (wb_dbus_we),
    .i_wb_cpu_cyc (wb_dbus_cyc),
    .o_wb_cpu_rdt (wb_dbus_rdt),
    .o_wb_cpu_ack (wb_dbus_ack),

    .o_wb_mem_adr (wb_dmem_adr),
    .o_wb_mem_dat (wb_dmem_dat),
    .o_wb_mem_sel (wb_dmem_sel),
    .o_wb_mem_we  (wb_dmem_we),
    .o_wb_mem_cyc (wb_dmem_cyc),
    .i_wb_mem_rdt (wb_dmem_rdt),

    .o_wb_gpio_dat (wb_gpio_dat),
    .o_wb_gpio_we  (wb_gpio_we),
    .o_wb_gpio_cyc (wb_gpio_cyc),
    .i_wb_gpio_rdt (wb_gpio_rdt),

    .o_wb_timer_dat (wb_timer_dat),
    .o_wb_timer_we  (wb_timer_we),
    .o_wb_timer_cyc (wb_timer_cyc),
    .i_wb_timer_rdt (wb_timer_rdt));

servant_ram
  #(.memfile (memfile),
    .depth (memsize),
    .RESET_STRATEGY (reset_strategy))
ram
  (// Wishbone interface
    .i_wb_clk (wb_clk),
    .i_wb_rst (wb_rst),
    .i_wb_adr (wb_mem_adr[$clog2(memsize)-1:2]),
    .i_wb_cyc (wb_mem_cyc),
    .i_wb_we  (wb_mem_we) ,
    .i_wb_sel (wb_mem_sel),
    .i_wb_dat (wb_mem_dat),
```

```
    .o_wb_rdt (wb_mem_rdt),
    .o_wb_ack (wb_mem_ack));

  generate
    if (with_csr) begin
          servant_timer
            #(.RESET_STRATEGY (reset_strategy),
              .WIDTH (32))
          timer
            (.i_clk    (wb_clk),
             .i_rst    (wb_rst),
             .o_irq    (timer_irq),
             .i_wb_cyc (wb_timer_cyc),
             .i_wb_we  (wb_timer_we) ,
             .i_wb_dat (wb_timer_dat),
             .o_wb_dat (wb_timer_rdt));
    end else begin
          assign wb_timer_rdt = 32'd0;
          assign timer_irq = 1'b0;
    end
  endgenerate

  servant_gpio gpio
    (.i_wb_clk (wb_clk),
     .i_wb_dat (wb_gpio_dat),
     .i_wb_we  (wb_gpio_we),
     .i_wb_cyc (wb_gpio_cyc),
     .o_wb_rdt (wb_gpio_rdt),
     .o_gpio   (q));

  serv_rf_top
    #(.RESET_PC (32'h0000_0000),
      .RESET_STRATEGY (reset_strategy),
`ifdef MDU
      .MDU(1),
`endif
      .WITH_CSR (with_csr))
  cpu
    (
     .clk      (wb_clk),
     .i_rst    (wb_rst),
     .i_timer_irq  (timer_irq),
`ifdef RISCV_FORMAL
     .rvfi_valid     (),
     .rvfi_order     (),
     .rvfi_insn      (),
     .rvfi_trap      (),
     .rvfi_halt      (),
     .rvfi_intr      (),
     .rvfi_mode      (),
     .rvfi_ixl       (),
     .rvfi_rs1_addr  (),
```

```
      .rvfi_rs2_addr  (),
      .rvfi_rs1_rdata (),
      .rvfi_rs2_rdata (),
      .rvfi_rd_addr   (),
      .rvfi_rd_wdata  (),
      .rvfi_pc_rdata  (),
      .rvfi_pc_wdata  (),
      .rvfi_mem_addr  (),
      .rvfi_mem_rmask (),
      .rvfi_mem_wmask (),
      .rvfi_mem_rdata (),
      .rvfi_mem_wdata (),
`endif

      .o_ibus_adr   (wb_ibus_adr),
      .o_ibus_cyc   (wb_ibus_cyc),
      .i_ibus_rdt   (wb_ibus_rdt),
      .i_ibus_ack   (wb_ibus_ack),

      .o_dbus_adr   (wb_dbus_adr),
      .o_dbus_dat   (wb_dbus_dat),
      .o_dbus_sel   (wb_dbus_sel),
      .o_dbus_we    (wb_dbus_we),
      .o_dbus_cyc   (wb_dbus_cyc),
      .i_dbus_rdt   (wb_dbus_rdt),
      .i_dbus_ack   (wb_dbus_ack),

      //Extension
      .o_ext_rs1    (mdu_rs1),
      .o_ext_rs2    (mdu_rs2),
      .o_ext_funct3 (mdu_op),
      .i_ext_rd     (mdu_rd),
      .i_ext_ready  (mdu_ready),
      //MDU
      .o_mdu_valid  (mdu_valid));

`ifdef MDU
    mdu_top mdu_serv
    (
     .i_clk(wb_clk),
     .i_rst(wb_rst),
     .i_mdu_rs1(mdu_rs1),
     .i_mdu_rs2(mdu_rs2),
     .i_mdu_op(mdu_op),
     .i_mdu_valid(mdu_valid),
     .o_mdu_ready(mdu_ready),
     .o_mdu_rd(mdu_rd));
`else
    assign mdu_ready = 1'b0;
    assign mdu_rd = 32'b0;
`endif
```

```
endmodule
```

serv/servant/servant_arbiter.v

```
/* Arbitrates between dbus and ibus accesses.
 * Relies on the fact that not both masters are active at the same time
 */
module servant_arbiter
  (
   input wire [31:0]  i_wb_cpu_dbus_adr,
   input wire [31:0]  i_wb_cpu_dbus_dat,
   input wire [3:0]   i_wb_cpu_dbus_sel,
   input wire         i_wb_cpu_dbus_we,
   input wire         i_wb_cpu_dbus_cyc,
   output wire [31:0] o_wb_cpu_dbus_rdt,
   output wire        o_wb_cpu_dbus_ack,

   input wire [31:0]  i_wb_cpu_ibus_adr,
   input wire         i_wb_cpu_ibus_cyc,
   output wire [31:0] o_wb_cpu_ibus_rdt,
   output wire        o_wb_cpu_ibus_ack,

   output wire [31:0] o_wb_cpu_adr,
   output wire [31:0] o_wb_cpu_dat,
   output wire [3:0]  o_wb_cpu_sel,
   output wire        o_wb_cpu_we,
   output wire        o_wb_cpu_cyc,
   input wire [31:0]  i_wb_cpu_rdt,
   input wire         i_wb_cpu_ack);

   assign o_wb_cpu_dbus_rdt = i_wb_cpu_rdt;
   assign o_wb_cpu_dbus_ack = i_wb_cpu_ack & !i_wb_cpu_ibus_cyc;

   assign o_wb_cpu_ibus_rdt = i_wb_cpu_rdt;
   assign o_wb_cpu_ibus_ack = i_wb_cpu_ack & i_wb_cpu_ibus_cyc;

   assign o_wb_cpu_adr = i_wb_cpu_ibus_cyc ? i_wb_cpu_ibus_adr : i_wb_cpu_dbus_adr;
   assign o_wb_cpu_dat = i_wb_cpu_dbus_dat;
   assign o_wb_cpu_sel = i_wb_cpu_dbus_sel;
   assign o_wb_cpu_we  = i_wb_cpu_dbus_we & !i_wb_cpu_ibus_cyc;
   assign o_wb_cpu_cyc = i_wb_cpu_ibus_cyc | i_wb_cpu_dbus_cyc;

endmodule
```

serv/servant/servant_mux.v

```
/* Arbitrates between dbus and ibus accesses.
 * Relies on the fact that not both masters are active at the same time
 */
module servant_arbiter
  (
   input wire [31:0]  i_wb_cpu_dbus_adr,
```

```
   input wire [31:0]  i_wb_cpu_dbus_dat,
   input wire [3:0]   i_wb_cpu_dbus_sel,
   input wire         i_wb_cpu_dbus_we,
   input wire         i_wb_cpu_dbus_cyc,
   output wire [31:0] o_wb_cpu_dbus_rdt,
   output wire        o_wb_cpu_dbus_ack,

   input wire [31:0]  i_wb_cpu_ibus_adr,
   input wire         i_wb_cpu_ibus_cyc,
   output wire [31:0] o_wb_cpu_ibus_rdt,
   output wire        o_wb_cpu_ibus_ack,

   output wire [31:0] o_wb_cpu_adr,
   output wire [31:0] o_wb_cpu_dat,
   output wire [3:0]  o_wb_cpu_sel,
   output wire        o_wb_cpu_we,
   output wire        o_wb_cpu_cyc,
   input wire [31:0]  i_wb_cpu_rdt,
   input wire         i_wb_cpu_ack);

   assign o_wb_cpu_dbus_rdt = i_wb_cpu_rdt;
   assign o_wb_cpu_dbus_ack = i_wb_cpu_ack & !i_wb_cpu_ibus_cyc;

   assign o_wb_cpu_ibus_rdt = i_wb_cpu_rdt;
   assign o_wb_cpu_ibus_ack = i_wb_cpu_ack & i_wb_cpu_ibus_cyc;

   assign o_wb_cpu_adr = i_wb_cpu_ibus_cyc ? i_wb_cpu_ibus_adr : i_wb_cpu_dbus_adr;
   assign o_wb_cpu_dat = i_wb_cpu_dbus_dat;
   assign o_wb_cpu_sel = i_wb_cpu_dbus_sel;
   assign o_wb_cpu_we  = i_wb_cpu_dbus_we & !i_wb_cpu_ibus_cyc;
   assign o_wb_cpu_cyc = i_wb_cpu_ibus_cyc | i_wb_cpu_dbus_cyc;

endmodule
```

serv/servant/servant_ram.v

```
/* Arbitrates between dbus and ibus accesses.
 * Relies on the fact that not both masters are active at the same time
 */
module servant_arbiter
  (
   input wire [31:0]  i_wb_cpu_dbus_adr,
   input wire [31:0]  i_wb_cpu_dbus_dat,
   input wire [3:0]   i_wb_cpu_dbus_sel,
   input wire         i_wb_cpu_dbus_we,
   input wire         i_wb_cpu_dbus_cyc,
   output wire [31:0] o_wb_cpu_dbus_rdt,
   output wire        o_wb_cpu_dbus_ack,

   input wire [31:0]  i_wb_cpu_ibus_adr,
   input wire         i_wb_cpu_ibus_cyc,
   output wire [31:0] o_wb_cpu_ibus_rdt,
```

```
   output wire        o_wb_cpu_ibus_ack,

   output wire [31:0] o_wb_cpu_adr,
   output wire [31:0] o_wb_cpu_dat,
   output wire [3:0]  o_wb_cpu_sel,
   output wire        o_wb_cpu_we,
   output wire        o_wb_cpu_cyc,
   input wire [31:0]  i_wb_cpu_rdt,
   input wire         i_wb_cpu_ack);

   assign o_wb_cpu_dbus_rdt = i_wb_cpu_rdt;
   assign o_wb_cpu_dbus_ack = i_wb_cpu_ack & !i_wb_cpu_ibus_cyc;

   assign o_wb_cpu_ibus_rdt = i_wb_cpu_rdt;
   assign o_wb_cpu_ibus_ack = i_wb_cpu_ack & i_wb_cpu_ibus_cyc;

   assign o_wb_cpu_adr = i_wb_cpu_ibus_cyc ? i_wb_cpu_ibus_adr : i_wb_cpu_dbus_adr;
   assign o_wb_cpu_dat = i_wb_cpu_dbus_dat;
   assign o_wb_cpu_sel = i_wb_cpu_dbus_sel;
   assign o_wb_cpu_we  = i_wb_cpu_dbus_we & !i_wb_cpu_ibus_cyc;
   assign o_wb_cpu_cyc = i_wb_cpu_ibus_cyc | i_wb_cpu_dbus_cyc;

endmodule
```

serv/servant/servant_gpio.v

```
module servant_gpio
  (input wire i_wb_clk,
   input wire i_wb_dat,
   input wire i_wb_we,
   input wire i_wb_cyc,
   output reg o_wb_rdt,
   output reg o_gpio);

   always @(posedge i_wb_clk) begin
      o_wb_rdt <= o_gpio;
      if (i_wb_cyc & i_wb_we)
          o_gpio <= i_wb_dat;
   end
endmodule
```