```
The spi-master currently on sends
VCD info: dumpfile dump.vcd opened for output.
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)
Sent out 0xC1, Received 0xc1
Sent out 0xBE, Received 0xbe
Sent out 0xEF, Received 0xef
```

https://www.fpga4student.com/2017/03/verilog-code-for-counter-with-testbench.html

```
// FPGA projects using Verilog/ VHDL
// fpga4student.com: FPGA projects, Verilog projects, VHDL projects
// Verilog code for up counter
module up_counter(input clk, reset, output[3:0] counter
    );
reg [3:0] counter_up;

// up counter
always @(posedge clk or posedge reset)
begin
if(reset)
 counter_up <= 4'd0;
else
 counter_up <= counter_up + 4'd1;
end
assign counter = counter_up;
endmodule
```

```
// FPGA projects using Verilog/ VHDL
// fpga4student.com: FPGA projects, Verilog projects, VHDL projects
// Verilog code for up counter with testbench
// Testbench Verilog code for up counter
module upcounter_testbench();
reg clk, reset;
wire [3:0] counter;

up_counter dut(clk, reset, counter);
initial begin
clk=0;
forever #5 clk=~clk;
end
initial begin
reset=1;
#20;
reset=0;
end
endmodule
```

devel@pi4-60:~/spi-master/Verilog/counter $ iverilog -o dsn upcounter_testbench.v counter_up.v
devel@pi4-60:~/spi-master/Verilog/counter $ vvp dsn
VCD info: dumpfile dump.vcd opened for output.