

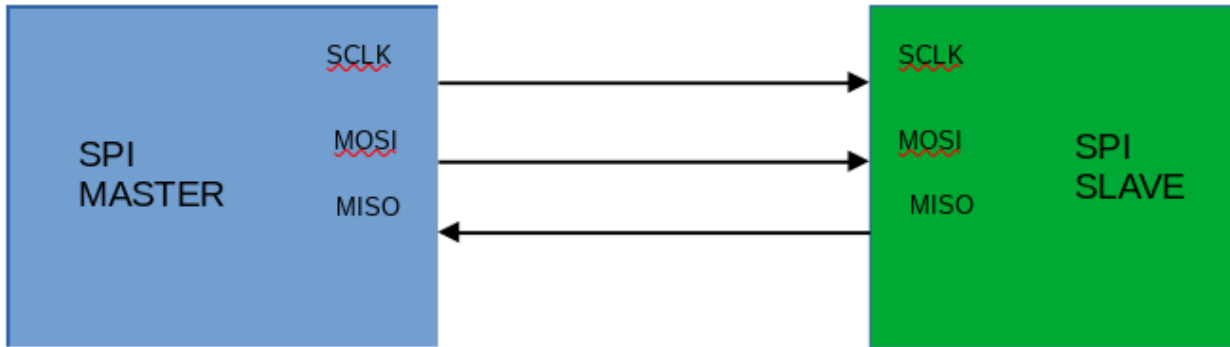
*****Draft*****

SPI-Master Written in SystemVerilog & SPI-Master with Single CS

10/14/23

*****Draft*****

Serial Peripheral Interface (SPI)



<https://youtu.be/ba0SQwjTQfw?> Youtube video

Forked <https://github.com/nandland/spi-master>

Iverilog required -g2005-sv and the file SPI_Master.v to obtain the dsn

```
devel@pi4-20:~$ git clone https://github.com/develone/spi-master.git -b dev
devel@pi4-20:~/spi-master/Verilog/sim $ iverilog -g2005-sv -o dsn SPI_Master_TB.sv
SPI_Master.v
```

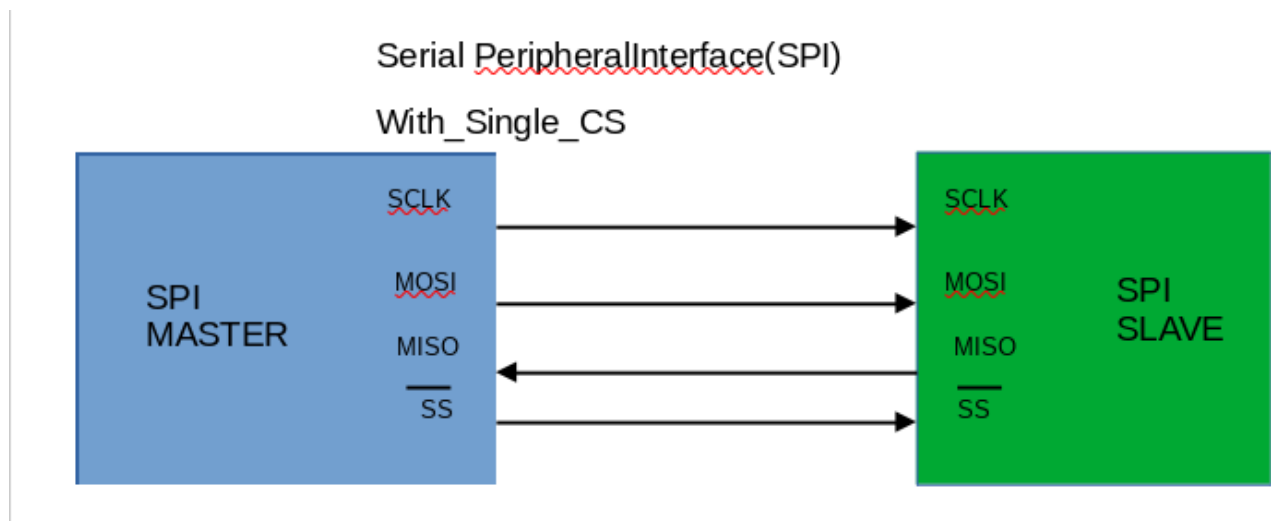
```
devel@pi4-20:~/spi-master/Verilog/sim $ vvp dsn
VCD info: dumpfile dump.vcd opened for output.
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)
Sent out 0xC1, Received 0xc1
Sent out 0xBE, Received 0xbe
Sent out 0xEF, Received 0xef
```

```
devel@pi4-20:~/spi-master/Verilog/sim $ gtkwave dump.vcd
```

GTKWave Analyzer v3.3.104 (w)1999-2020 BSI

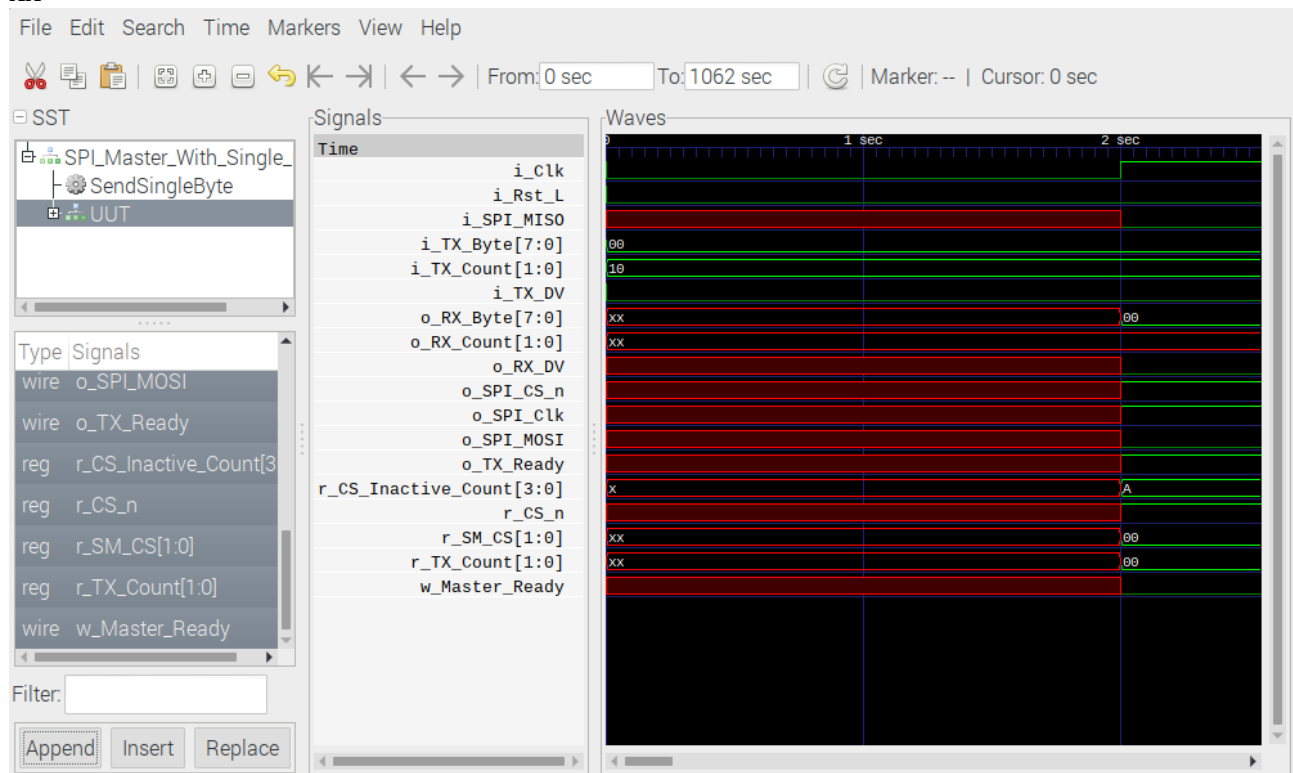
[0] start time.
[922] end time.

Sent out 0xC1, Received 0xc1
Sent out 0xC2, Received 0xc2
XX



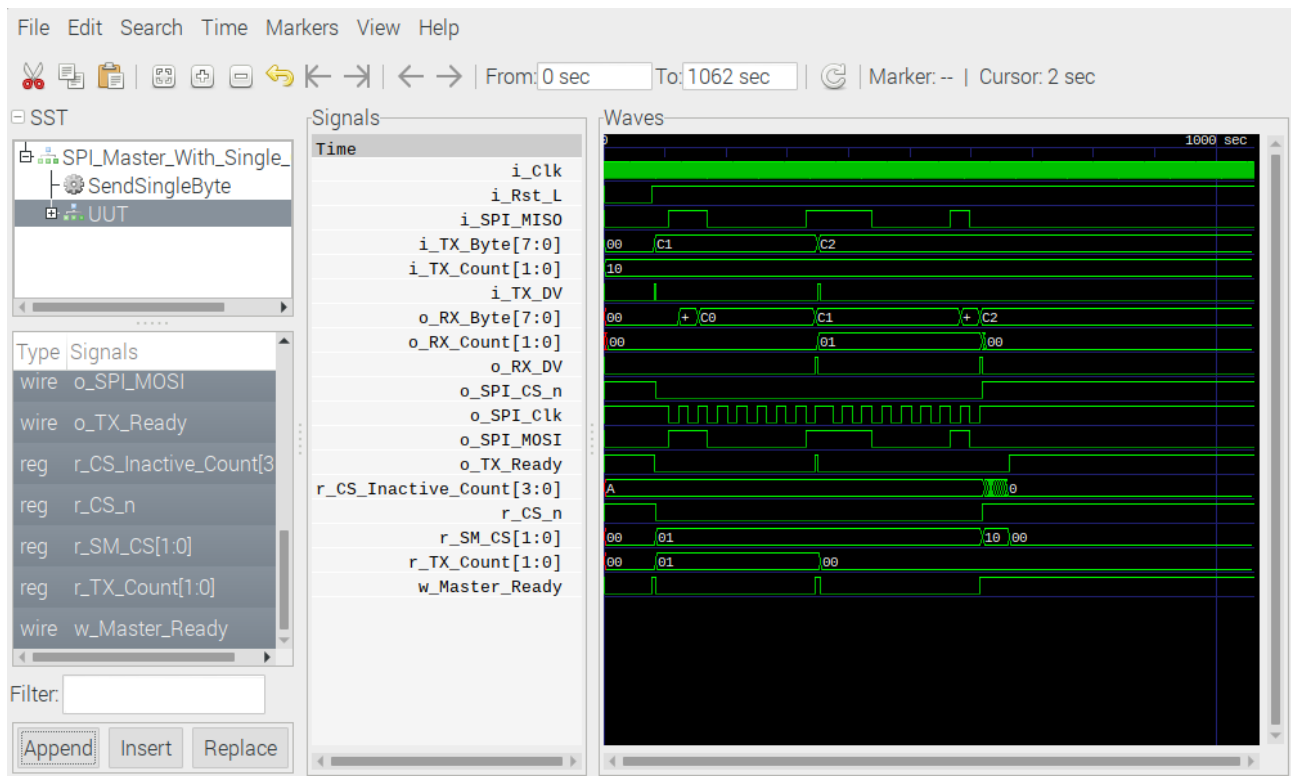
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Note: In the center of the image below the signal o_SPI_CS_n.



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