**********Draft**********
SPI-Master Written in SystemVerilog

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Forked https://github.com/nandland/spi-master

Iverilog required -g2005-sv and the file SPI_Master.v to obtain the dsn

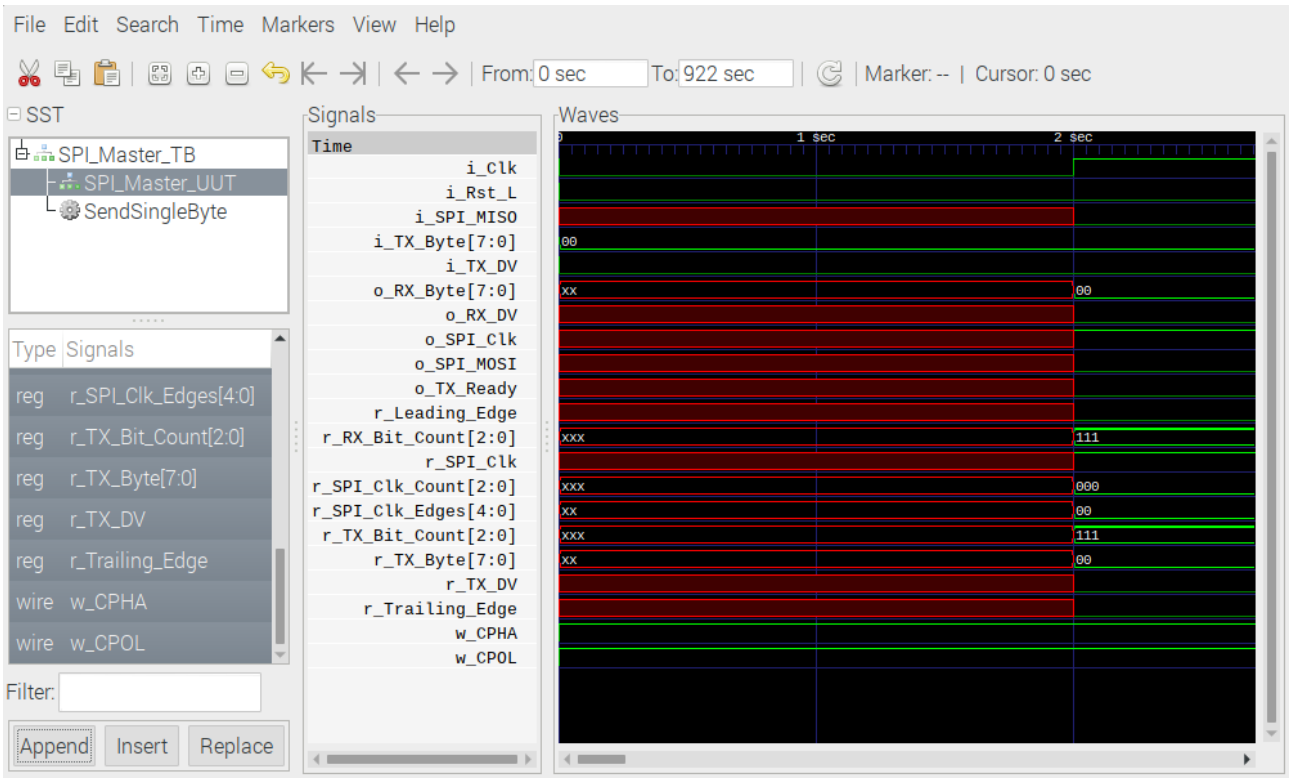
devel@pi4-20:git clone https://github.com/develone/spi-master.git -b dev
devel@pi4-20:~/spi-master/Verilog/sim $ iverilog -g2005-sv -o dsn SPI_Master_TB.sv SPI_Master.v

devel@pi4-20:~/spi-master/Verilog/sim $ vvp dsn
VCD info: dumpfile dump.vcd opened for output.
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)
Sent out 0xC1, Received 0xc1
Sent out 0xBE, Received 0xbe
Sent out 0xEF, Received 0xef

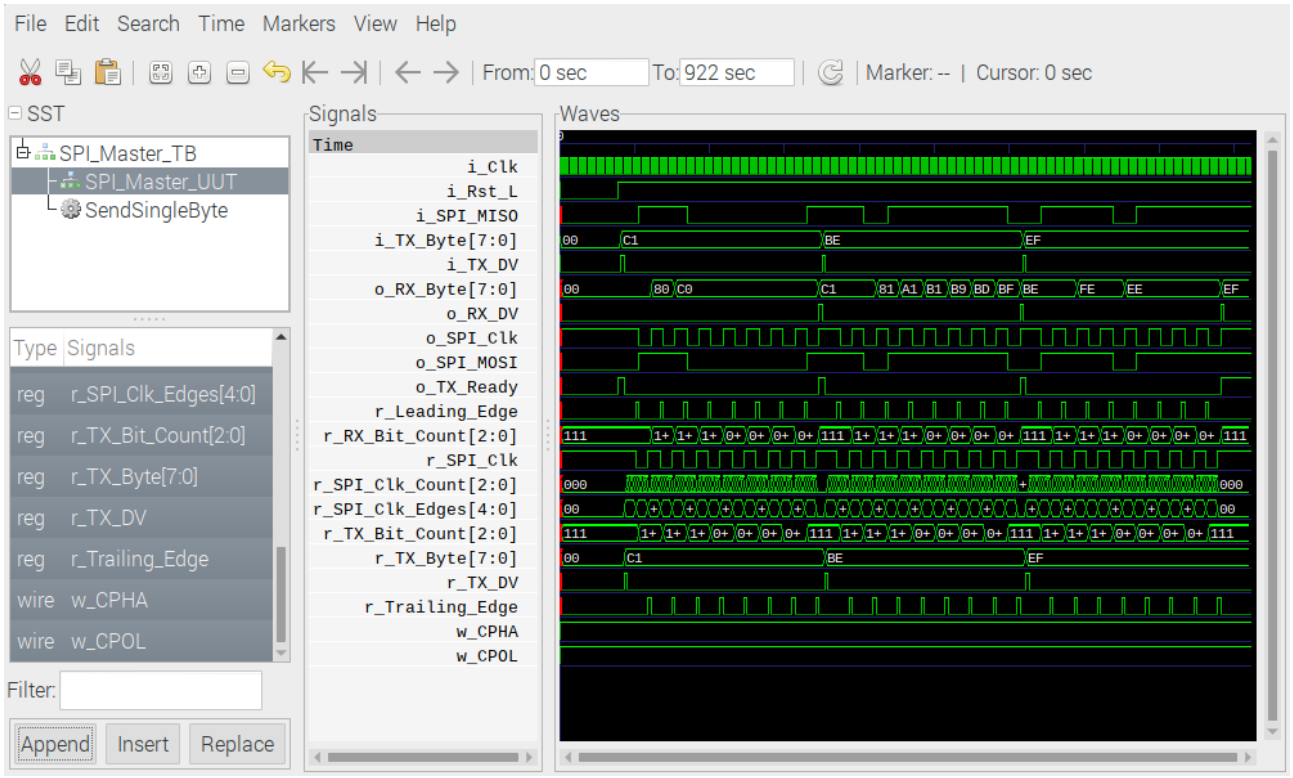
devel@pi4-20:~/spi-master/Verilog/sim $ gtkwave dump.vcd

GTKWave Analyzer v3.3.104 (w)1999-2020 BSI

[0] start time.
[922] end time.



Xx


File Edit Search Time Markers View Help
From: 0 sec
To: 922 sec
Marker: -- | Cursor: 0 sec
SST
SPI_Master_TB
SPI_Master_UUT
SendSingleByte
Type Signals
reg r_SPI_Clk_Edges[4:0]
reg r_TX_Bit_Count[2:0]
reg r_TX_Byte[7:0]
reg r_TX_DV
reg r_Trailing_Edge
wire w_CPHA
wire w_CPOL
Filter:
Append
Insert
Replace
Signals
Time
i_Clk
i_Rst_L
i_SPI_MISO
i_TX_Byte[7:0]
i_TX_DV
o_RX_Byte[7:0]
o_RX_DV
o_SPI_Clk
o_SPI_MOSI
o_TX_Ready
r_Leading_Edge
r_RX_Bit_Count[2:0]
r_SPI_Clk
r_SPI_Clk_Count[2:0]
r_SPI_Clk_Edges[4:0]
r_TX_Bit_Count[2:0]
r_TX_Byte[7:0]
r_TX_DV
r_Trailing_Edge
w_CPHA
w_CPOL
Waves

XX