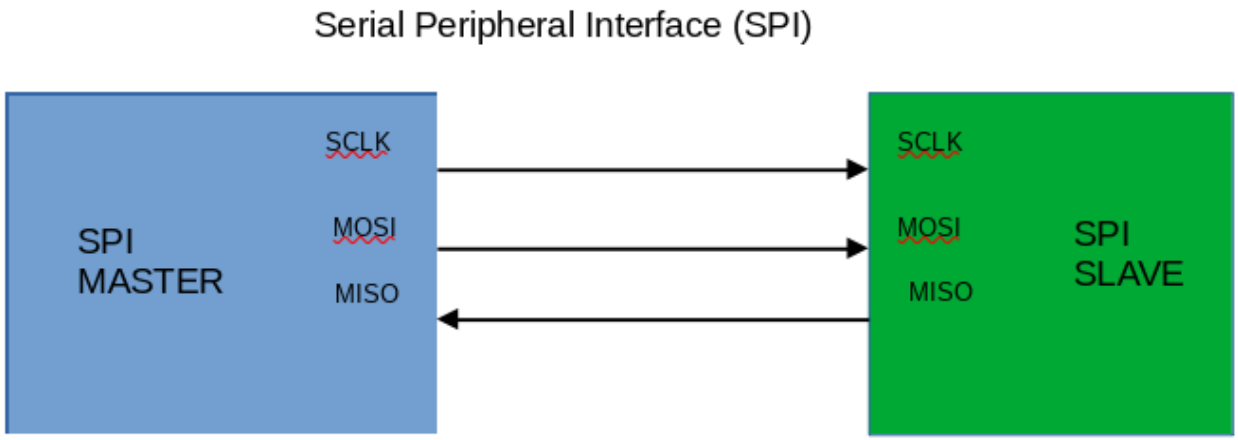
**********Draft**********

SPI-Master Written in SystemVerilog & SPI-Master with Single CS

10/27/23

**********Draft**********



https://youtu.be/ba0SQwjTQfw? Youtube video

Forked https://github.com/nandland/spi-master

Iverilog required -g2005-sv and the file SPI_Master.v to obtain the dsn

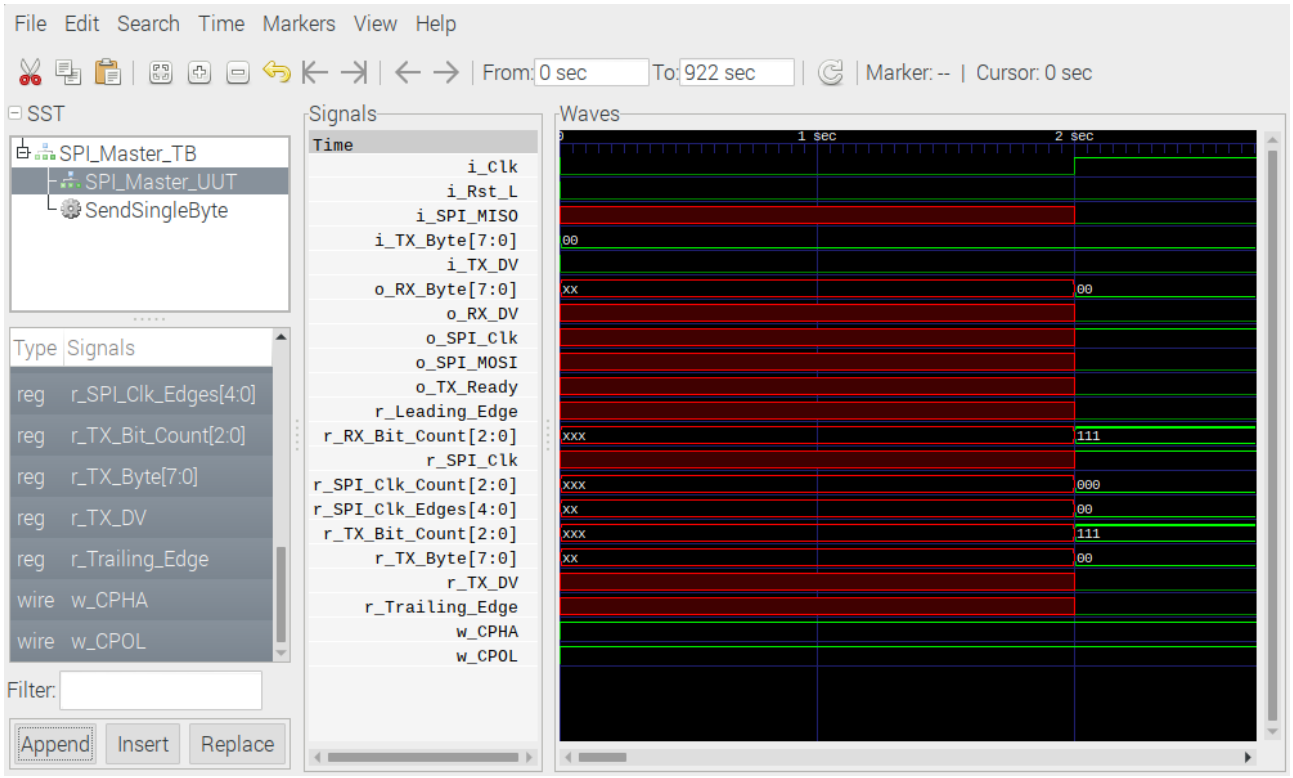
devel@pi4-20:git clone https://github.com/develone/spi-master.git -b dev
devel@pi4-20:~/spi-master/Verilog/sim $ iverilog -g2005-sv -o dsn SPI_Master_TB.sv SPI_Master.v

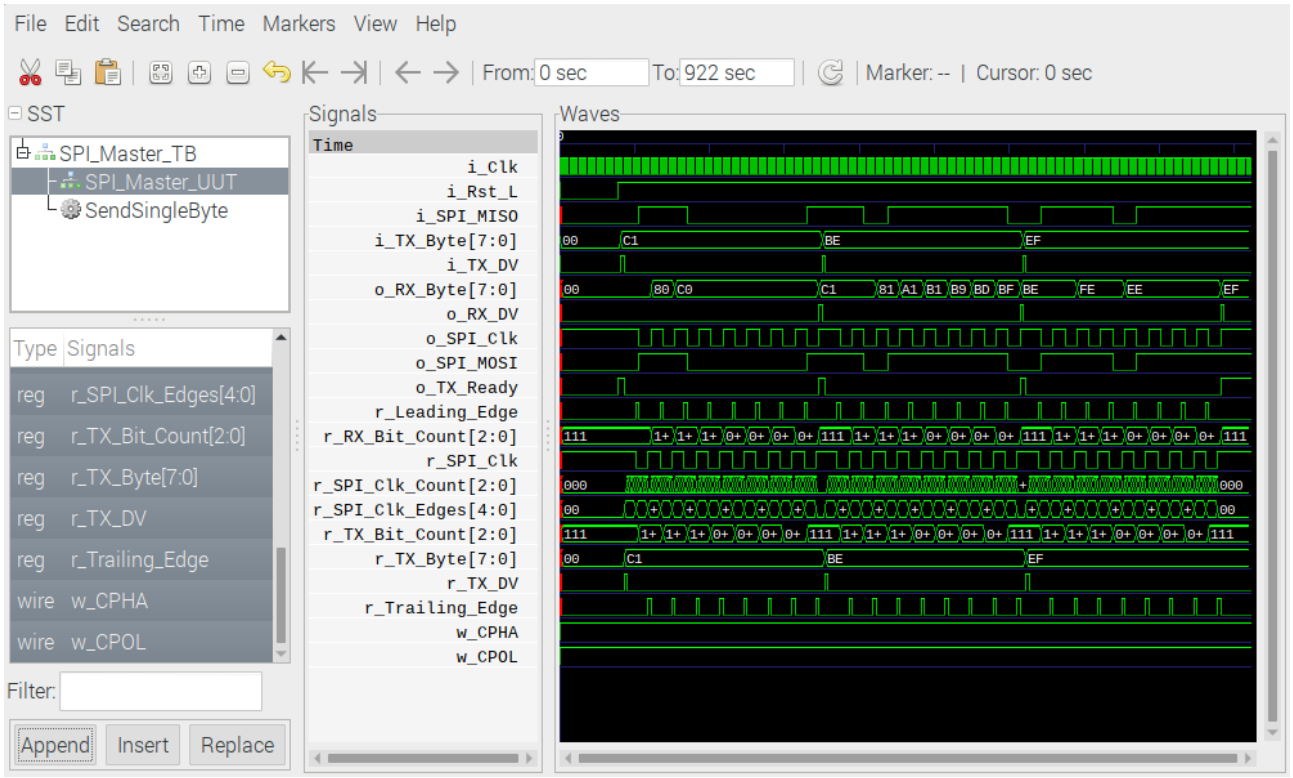
devel@pi4-20:~/spi-master/Verilog/sim $ vvp dsn
VCD info: dumpfile dump.vcd opened for output.
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)
Sent out 0xC1, Received 0xc1
Sent out 0xBE, Received 0xbe
Sent out 0xEF, Received 0xef

devel@pi4-20:~/spi-master/Verilog/sim $ gtkwave dump.vcd

GTKWave Analyzer v3.3.104 (w)1999-2020 BSI

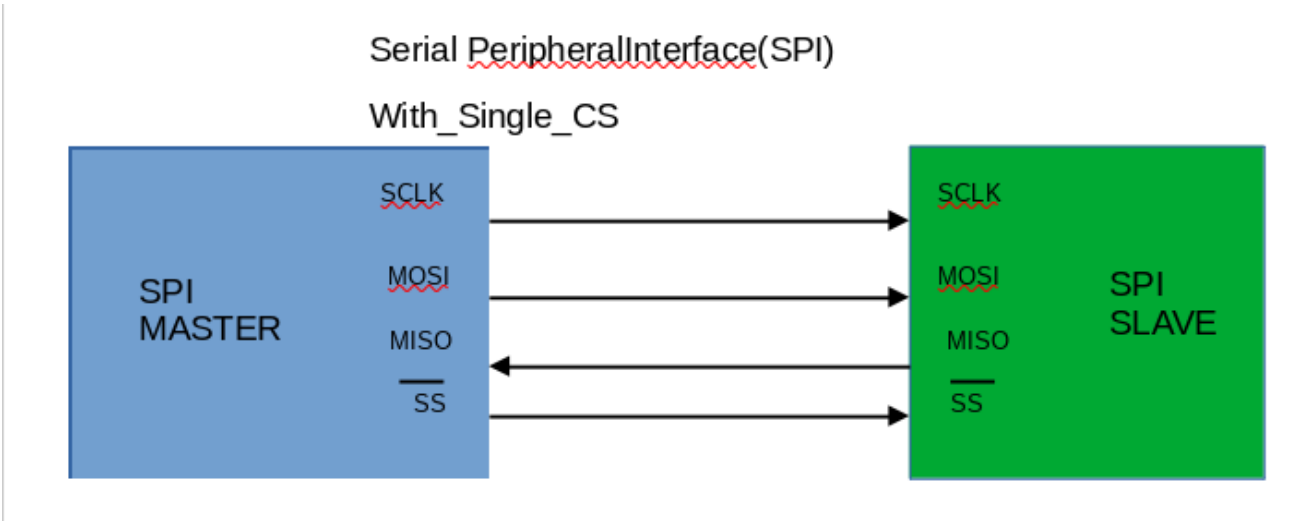
[0] start time.
[922] end time.



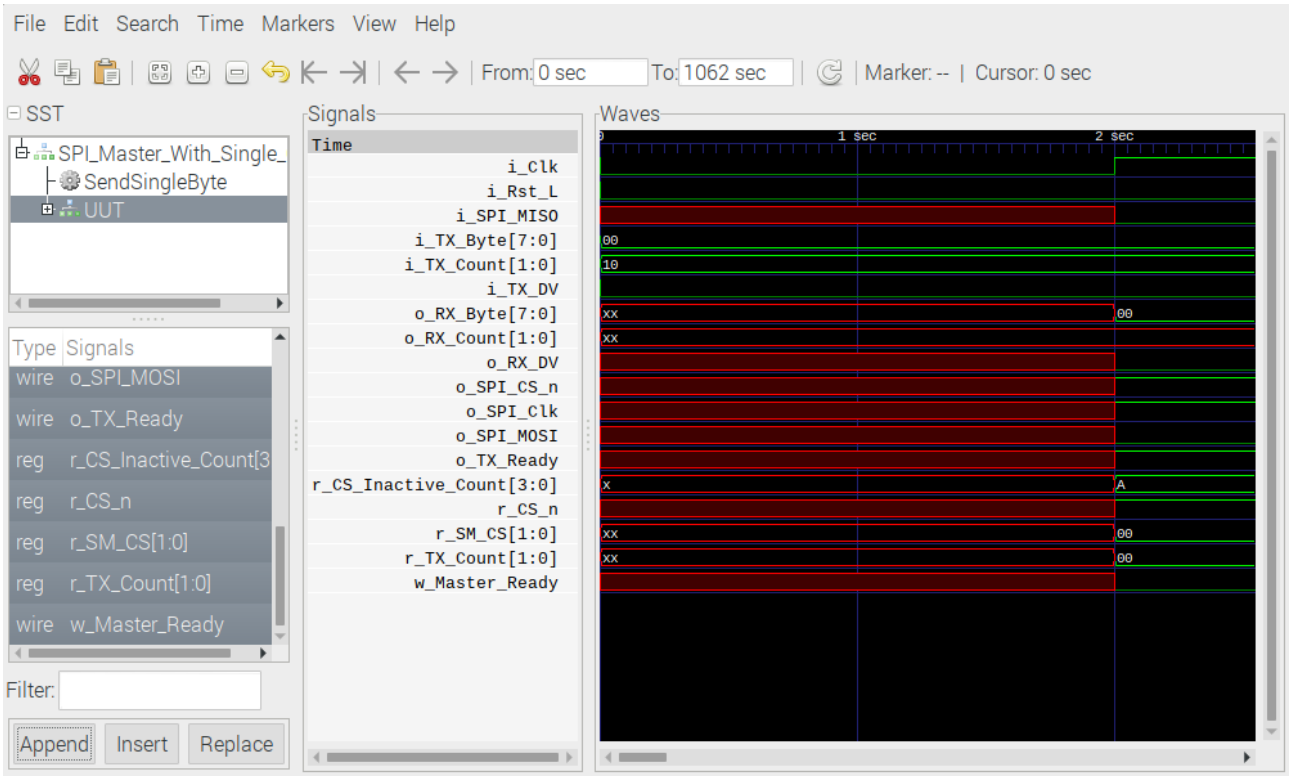


devel@pi4-20:~/spi-master/Verilog/sim $ iverilog -o dsn1 -g2005-sv SPI_Master_With_Single_CS_TB.sv ../source/SPI_Master_With_Single_CS.v
devel@pi4-20:~/spi-master/Verilog/sim $ vvp dsn1
VCD info: dumpfile dump.vcd opened for output.
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)

Sent out 0xC1, Received 0xc1
Sent out 0xC2, Received 0xc2
xx

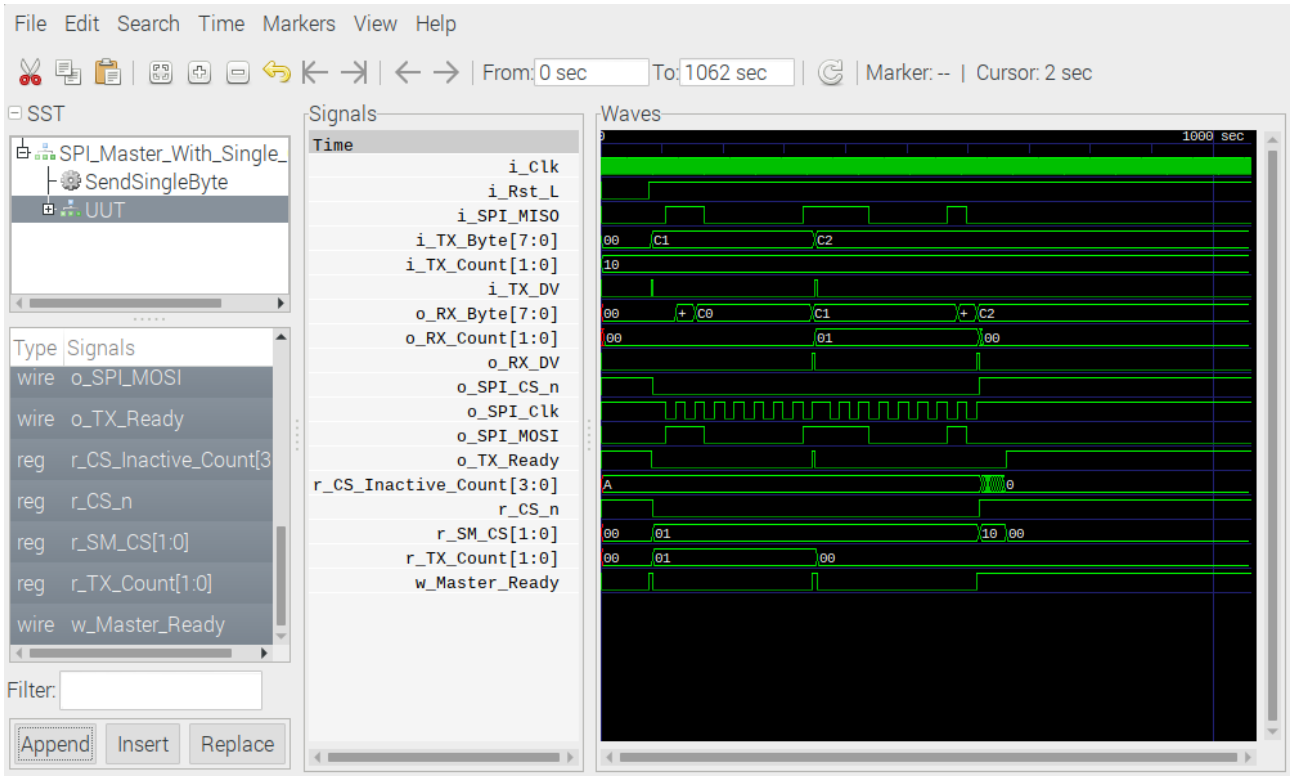


xx
xx



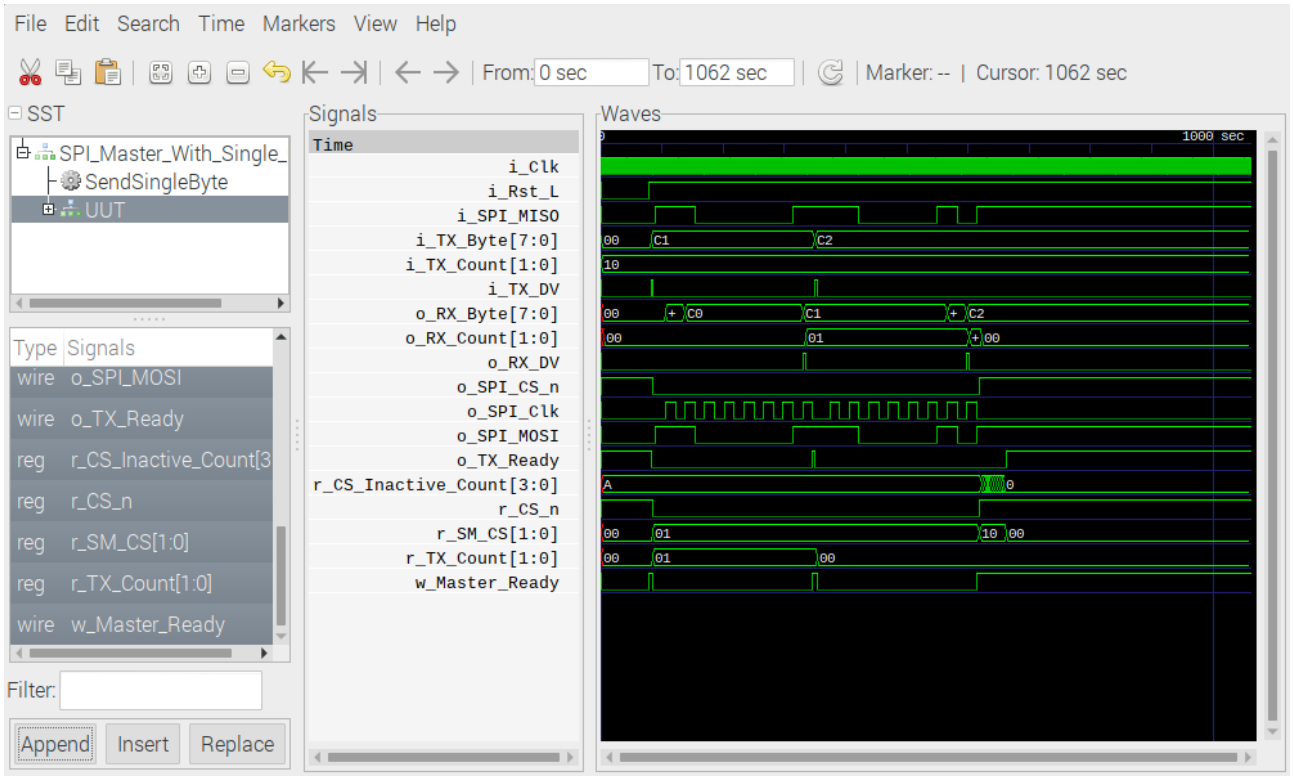
xx

Note: In the center of the image below the signal o_SPI_CS_n.

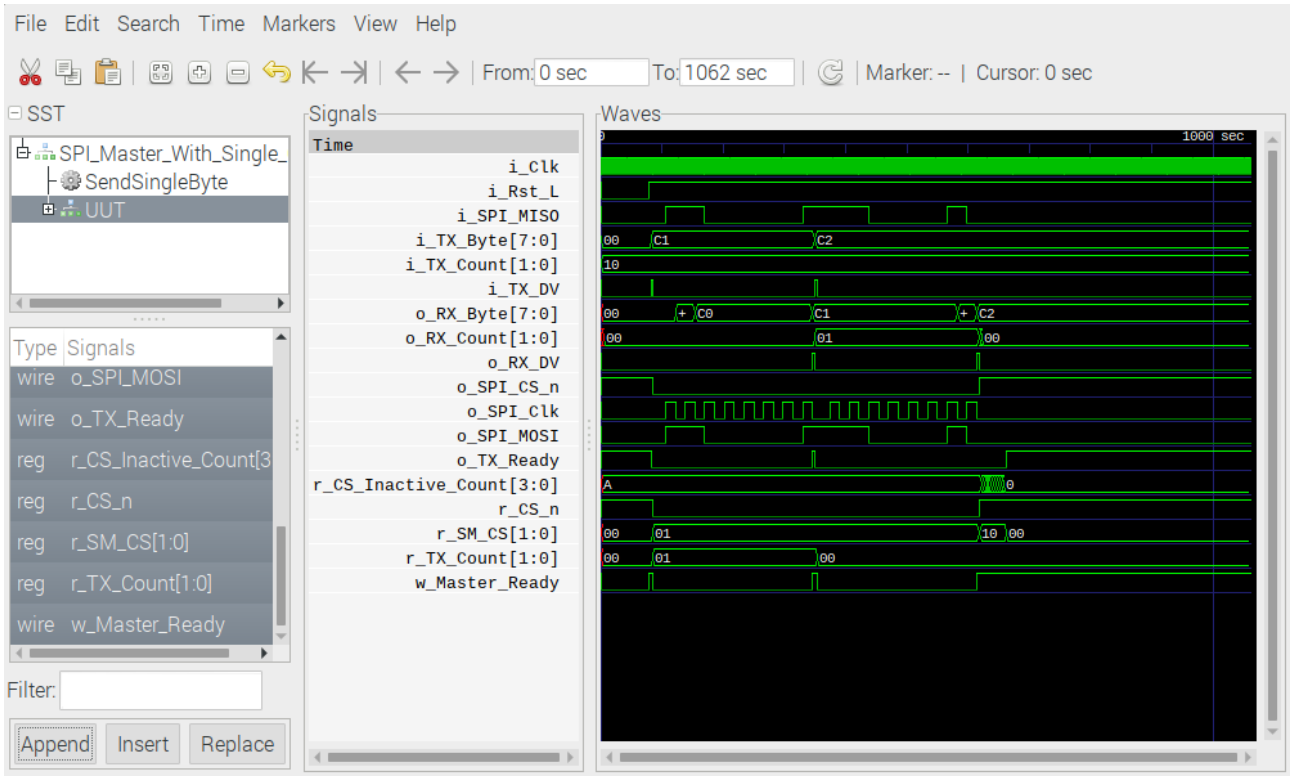



```
//              Mode | Clock Polarity (CPOL/CKP) | Clock Phase (CPHA)
//               0   |             0             |        0
//               1   |             0             |        1
//               2   |             1             |        0
//               3   |             1             |        1
  localparam IDLE        = 2'b00;
  localparam TRANSFER    = 2'b01;
  localparam CS_INACTIVE = 2'b10;
```

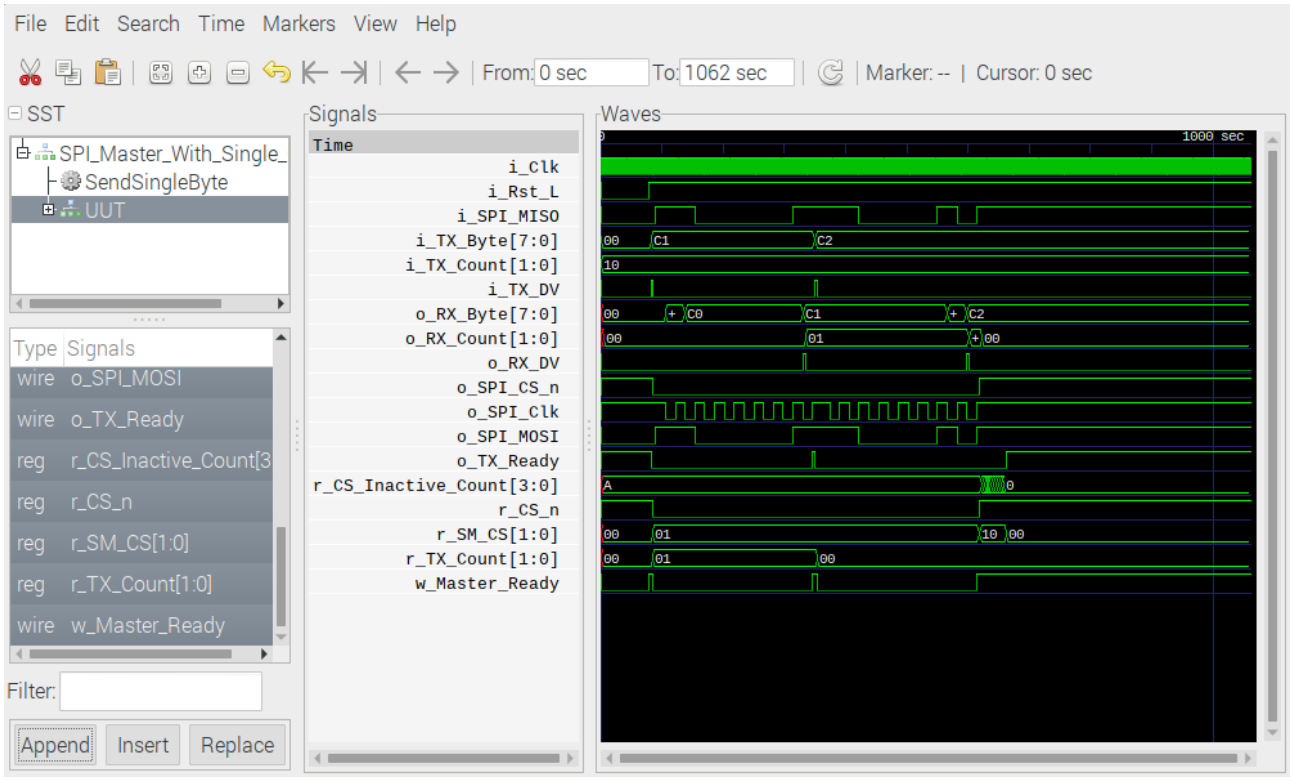
Mode0 clk idle lo positive edge.
iverilog -o dsnmode0 -g2005-sv SPI_Master_With_Single_CS_TB.sv
../source/SPI_Master_With_Single_CS.v
parameter SPI_MODE = 0;   // CPOL = 0, CPHA = 0



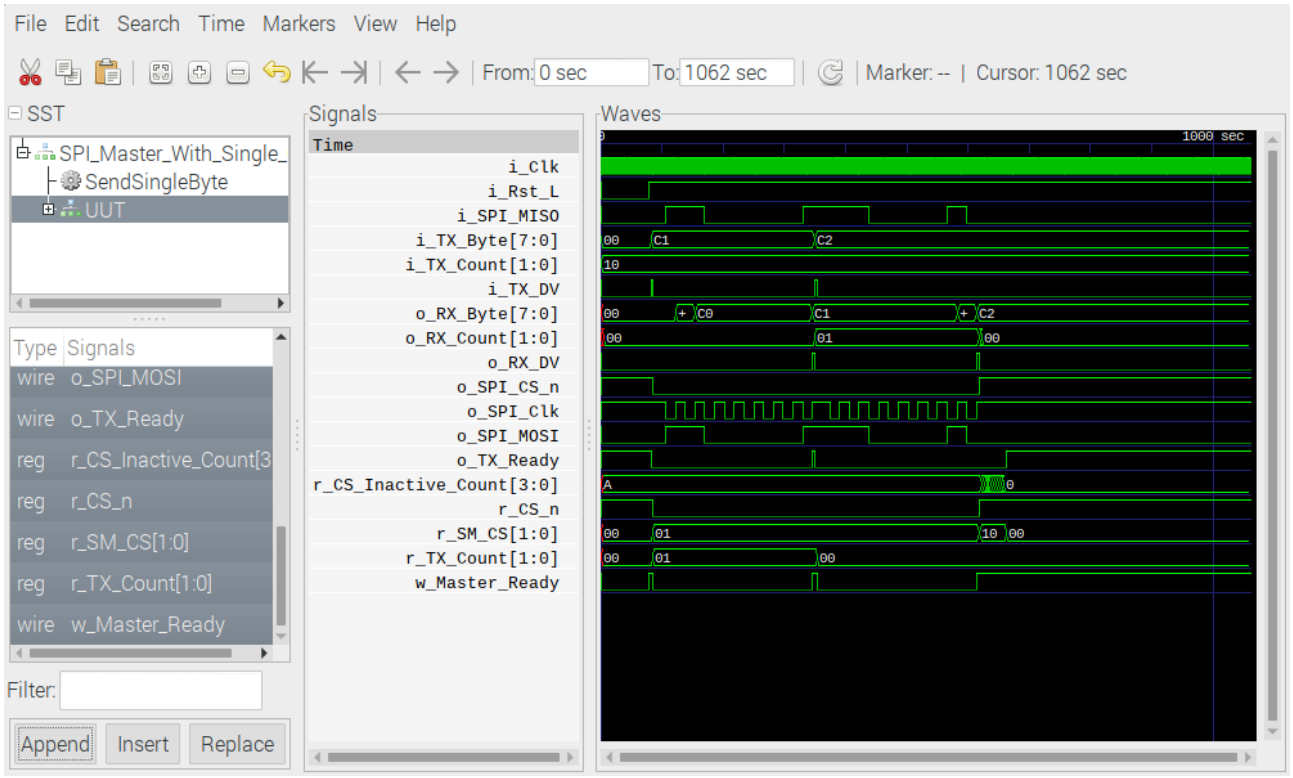
Mode1 clk idle lo negative edge
iverilog -o dsnmode1 -g2005-sv SPI_Master_With_Single_CS_TB.sv
../source/SPI_Master_With_Single_CS.v



Mode2 clk idle hi positive edge
iverilog -o dsnmode2 -g2005-sv SPI_Master_With_Single_CS_TB.sv
../source/SPI_Master_With_Single_CS.v
parameter SPI_MODE = 2; // CPOL = 1, CPHA = 0



Mode3 clk idle hi negative edge
iverilog -o dsnmode0 -g2005-sv SPI_Master_With_Single_CS_TB.sv
../source/SPI_Master_With_Single_CS.v
parameter SPI_MODE = 3; // CPOL = 1, CPHA = 1
verilog -o dsnmode2 -g2005-sv SPI_Master_With_Single_CS_TB.sv


File Edit Search Time Markers View Help
From: 0 sec
To: 1062 sec
Marker: -- | Cursor: 1062 sec
SST
SPI_Master_With_Single_
SendSingleByte
UUT
Type Signals
wire o_SPI_MOSI
wire o_TX_Ready
reg r_CS_Inactive_Count[3
reg r_CS_n
reg r_SM_CS[1:0]
reg r_TX_Count[1:0]
wire w_Master_Ready
Filter:
Append Insert Replace
Signals
Time
i_Clk
i_Rst_L
i_SPI_MISO
i_TX_Byte[7:0]
i_TX_Count[1:0]
i_TX_DV
o_RX_Byte[7:0]
o_RX_Count[1:0]
o_RX_DV
o_SPI_CS_n
o_SPI_Clk
o_SPI_MOSI
o_TX_Ready
r_CS_Inactive_Count[3:0]
r_CS_n
r_SM_CS[1:0]
r_TX_Count[1:0]
w_Master_Ready
Waves
1000 sec