```
The spi-master currently on sends
VCD info: dumpfile dump.vcd opened for output.
VCD warning: $dumpvars: Unsupported argument type (vpiPackage)
Sent out 0xC1, Received 0xc1
Sent out 0xBE, Received 0xbe
Sent out 0xEF, Received 0xef
```

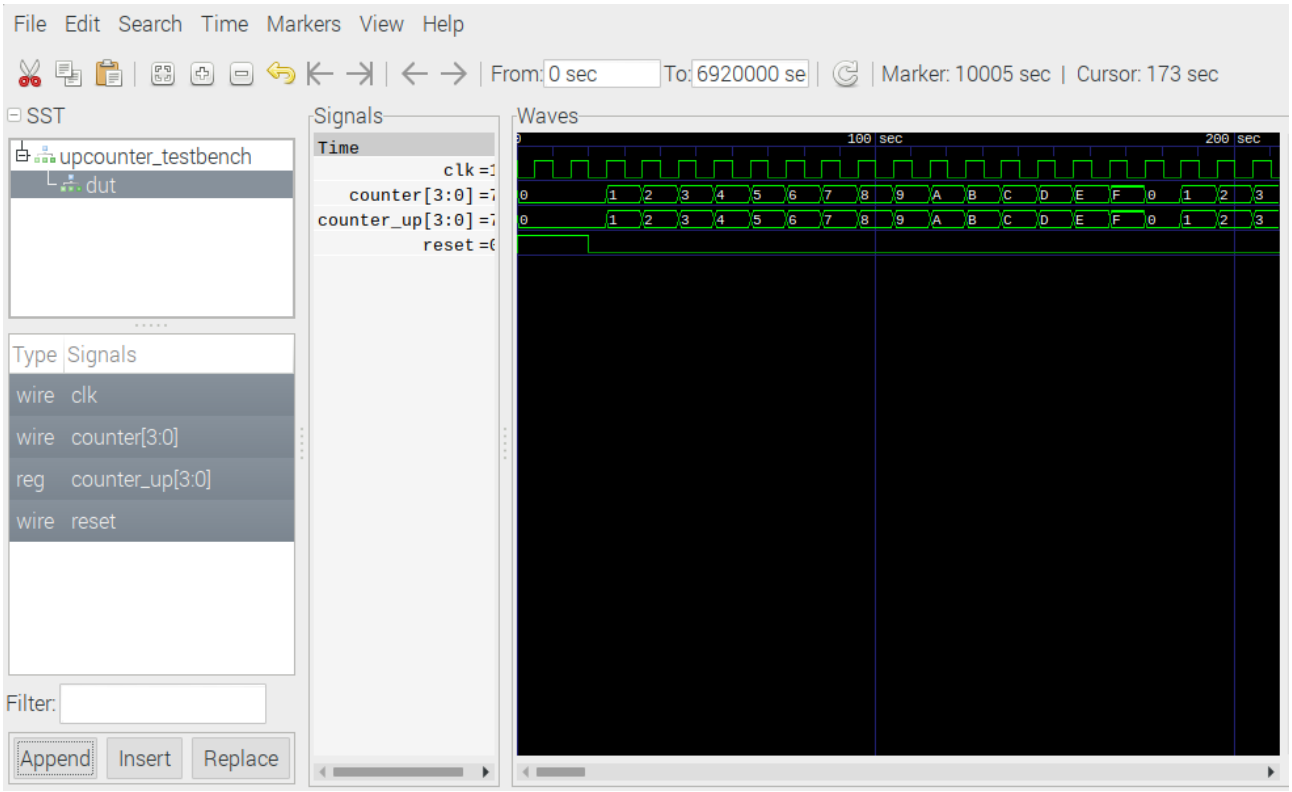
https://www.fpga4student.com/2017/03/verilog-code-for-counter-with-testbench.html

```
// FPGA projects using Verilog/ VHDL
// fpga4student.com: FPGA projects, Verilog projects, VHDL projects
// Verilog code for up counter
module up_counter(input clk, reset, output[3:0] counter
    );
reg [3:0] counter_up;

// up counter
always @(posedge clk or posedge reset)
begin
if(reset)
 counter_up <= 4'd0;
else
 counter_up <= counter_up + 4'd1;
end
assign counter = counter_up;
endmodule
```

```
// FPGA projects using Verilog/ VHDL
// fpga4student.com: FPGA projects, Verilog projects, VHDL projects
// Verilog code for up counter with testbench
// Testbench Verilog code for up counter
module upcounter_testbench();
reg clk, reset;
wire [3:0] counter;

up_counter dut(clk, reset, counter);
initial begin
clk=0;
forever #5 clk=~clk;
end
initial begin
reset=1;
#20;
reset=0;
end
endmodule
```

devel@pi4-60:~/spi-master/Verilog/counter $ iverilog -o dsn upcounter_testbench.v counter_up.v
devel@pi4-60:~/spi-master/Verilog/counter $ vvp dsn
VCD info: dumpfile dump.vcd opened for output.

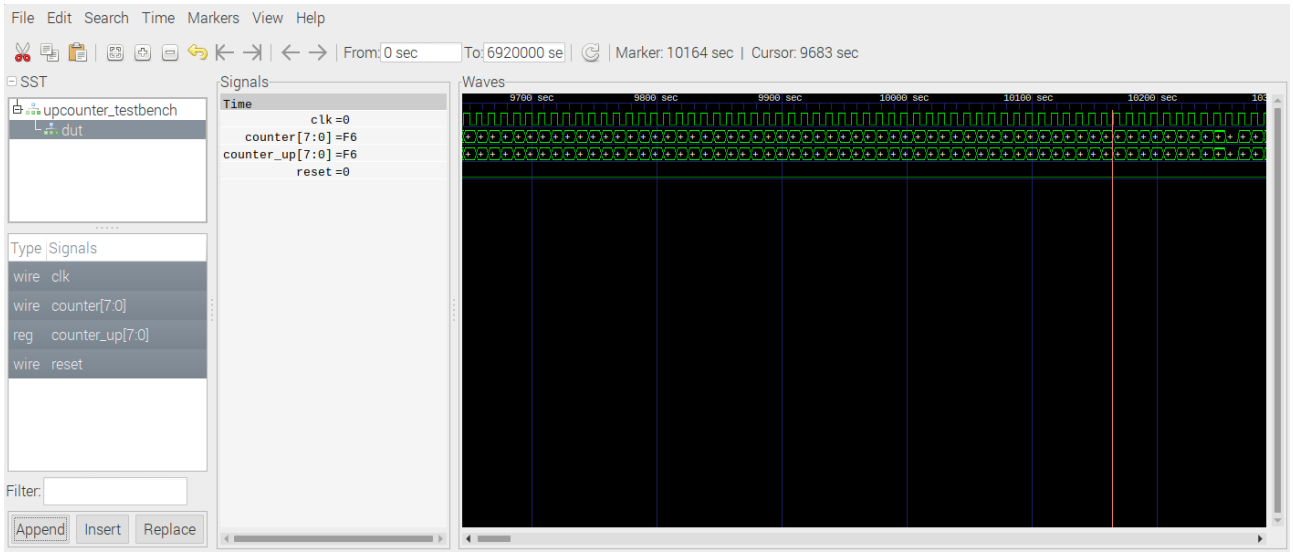
devel@pi4-60:~/spi-master/Verilog/counter $ gtkwave dump.vcd



Converting the 4 bit counter to 8 bit counter.

```
diff --git a/Verilog/counter/counter_up.v b/Verilog/counter/counter_up.v
index 38d9833..850dd59 100644
--- a/Verilog/counter/counter_up.v
+++ b/Verilog/counter/counter_up.v
@@ -1,18 +1,17 @@
 // FPGA projects using Verilog/ VHDL
 // fpga4student.com: FPGA projects, Verilog projects, VHDL projects
 // Verilog code for up counter
-module up_counter(input clk, reset, output[3:0] counter
+module up_counter(input clk, reset, output[7:0] counter
     );
-reg [3:0] counter_up;
+reg [7:0] counter_up;

 // up counter
 always @(posedge clk or posedge reset)
 begin
 if(reset)
- counter_up <= 4'd0;
+ counter_up <= 8'd0;
```

```
 else
- counter_up <= counter_up + 4'd1;
+ counter_up <= counter_up + 8'd1;
 end
 assign counter = counter_up;
-endmodule
-
+endmodule
\ No newline at end of file

git diff upcounter_testbench.v
diff --git a/Verilog/counter/upcounter_testbench.v b/Verilog/counter/upcounter_testbench.v
index 7734158..5b7a421 100644
--- a/Verilog/counter/upcounter_testbench.v
+++ b/Verilog/counter/upcounter_testbench.v
@@ -4,7 +4,7 @@
 // Testbench Verilog code for up counter
 module upcounter_testbench();
 reg clk, reset;
-wire [3:0] counter;
+wire [7:0] counter;

 up_counter dut(clk, reset, counter);
 initial begin
@@ -16,4 +16,18 @@ reset=1;
 #20;
 reset=0;
 end
-endmodule
\ No newline at end of file
+
+initial
+begin
+#6920000
+$finish();
+end
+
+ initial
+    begin
+      // Required to dump signals to EPWave
+      $dumpfile("dump.vcd");
+      $dumpvars(0);
+    end
+
+endmodule
\ No newline at end of file

devel@pi4-60:~/spi-master/Verilog/counter $ gtkwave dump.vcd
```


File Edit Search Time Markers View Help
From: 0 sec
To: 6920000 se
Marker: 10164 sec | Cursor: 9683 sec
SST
upcounter_testbench
dut
Type Signals
wire clk
wire counter[7:0]
reg counter_up[7:0]
wire reset
Filter:
Append Insert Replace
Signals
Time
clk =0
counter[7:0] =F6
counter_up[7:0] =F6
reset =0
Waves
9700 sec
9800 sec
9900 sec
10000 sec
10100 sec
10200 sec