

04/26/18

Thu Apr 19 2018

Initial code was download from

<https://www.edaplayground.com/x/Pgf>

<http://www.nandland.com>

Command to create **testuart** from **UART_TB.v** **UART_RX.v** **UART_TB/v** includes **UART_TX.v**

iverilog -o testuart UART_TB.v UART_RX.v

vvp testuart

VCD info: dumpfile dump.vcd opened for output.

Test Passed - Correct Byte Received

This code was created

```
// Testbench uses a 25 MHz clock
// Want to interface to 115200 baud UART
// 25000000 / 115200 = 217 Clocks Per Bit.
parameter c_CLOCK_PERIOD_NS = 40;
```

Both the UART_TX and UART_RX are a case statement

IDLE, TX_START_BIT, TX_DATA_BITS, TX_STOP_BIT, and C:EANUP.

IDLE, RX_START_BIT, RX_DATA_BITS, RX_STOP_BIT, and C:EANUP.

In MyHDL the case statement was written for uart_tx.

if(r_SM_Main==IDLE):

.

.

elif (r_SM_Main==TX_START_BIT):

.

.

elif (r_SM_Main==TX_DATA_BITS):

.

.

elif (r_SM_Main==TX_STOP_BIT):

.

.

else:

.

.

and the uart_rx was similar

if(r_SM_Main==IDLE):

.

.

elif (r_SM_Main==RX_START_BIT):

.

.

elif (r_SM_Main==RX_DATA_BITS):

```

        .
        .
    elif (r_SM_Main==RX_STOP_BIT):
        .
        .
    else:
        .
        .

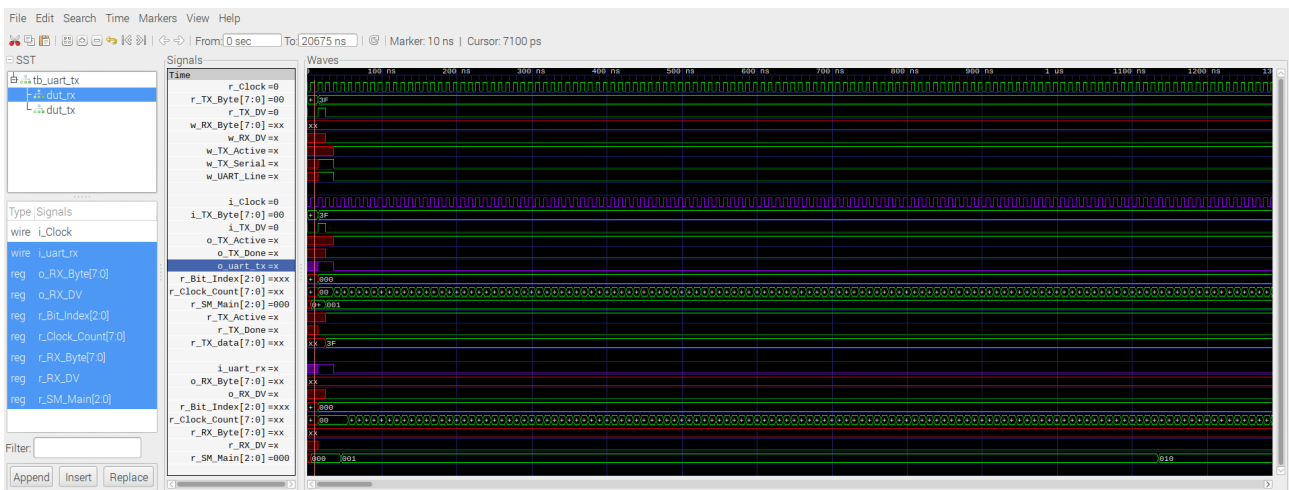
```

In the simulation the r_TX_BYTE is set to byte to be transmitted and a 1 clock wide r_TX_DV.

```

r_TX_DV  <= 1'b1;
r_TX_Byte <= 8'h3A;
@(posedge r_Clock);
r_TX_DV <= 1'b0;

```



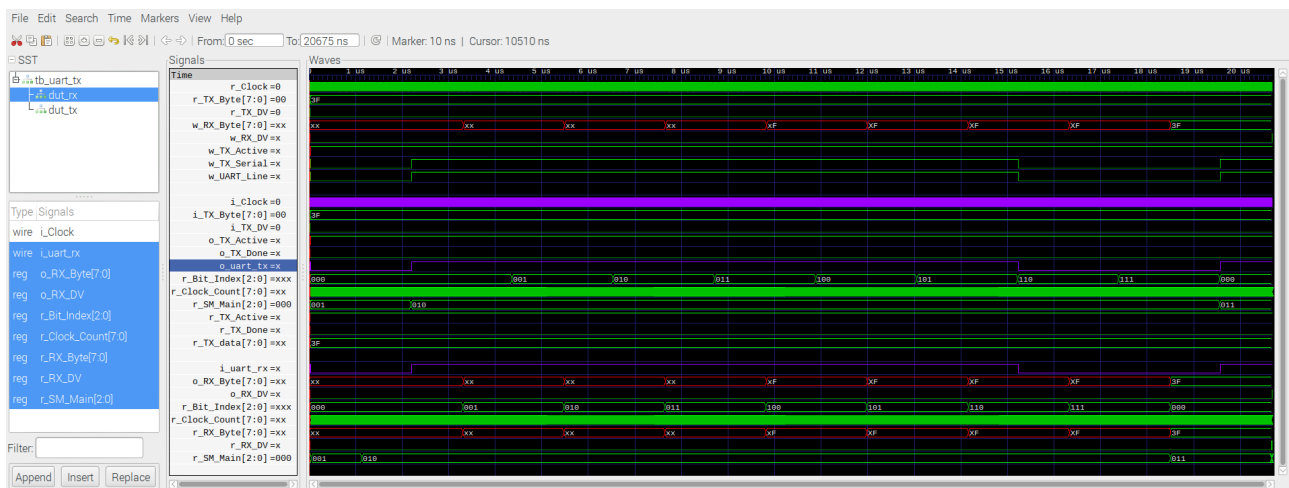
Testing at 100 MHz appears okay
Using MyHDL to create **uart_rx.v** with **uart_rx.py**
& **uart_tx.v** with **uart_tx.py**

iverilog -o testuart tb_dut_uart_txrx.v uart_rx.v

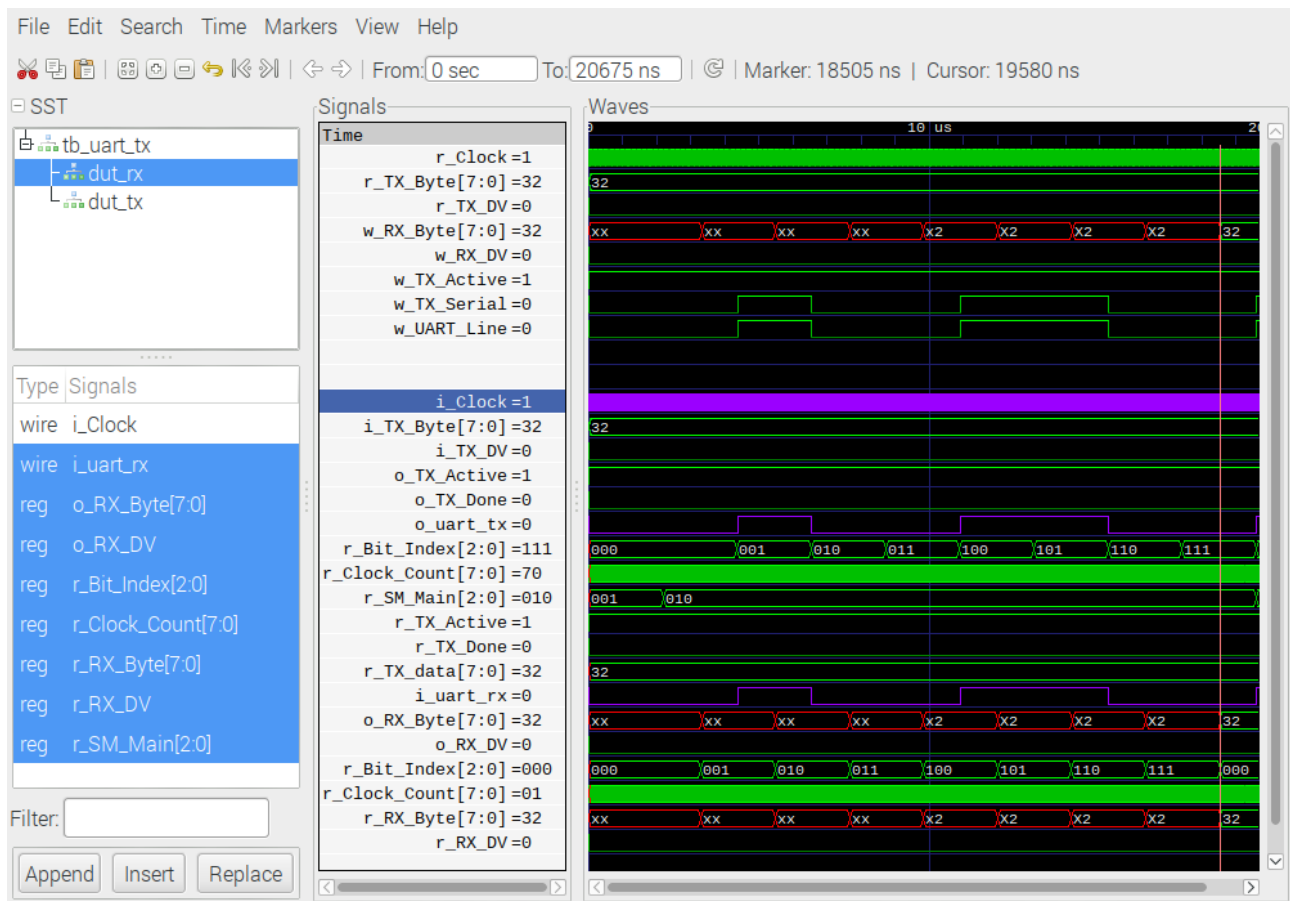
vvp testuart

VCD info: dumpfile dump.vcd opened for output.
Test Passed - Correct Byte Received

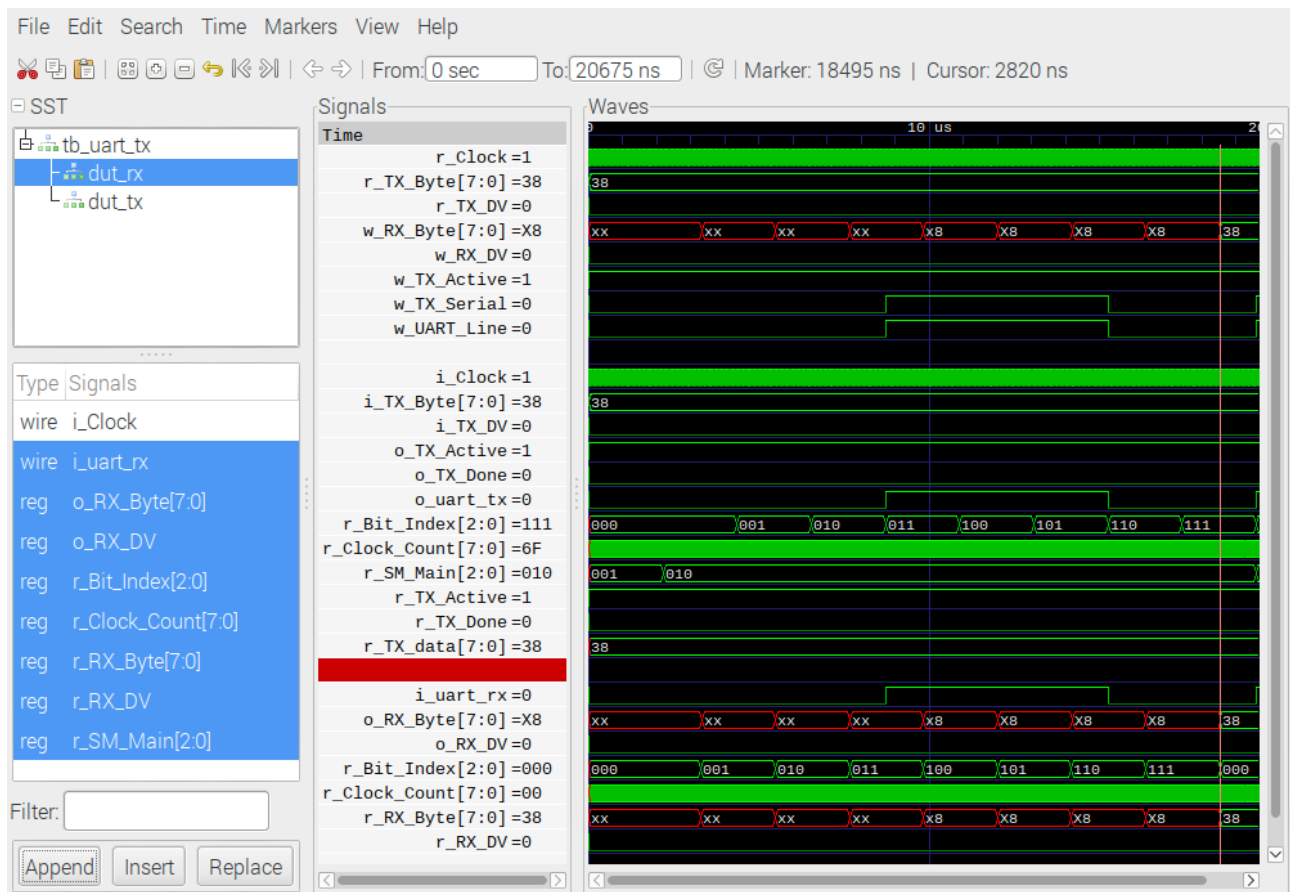
Several simulations were tested 0x3F, 0x32, 0x38, 0x3A, 0x41.
3F transmitted & received



00111111
32 transmitted & received
00110010

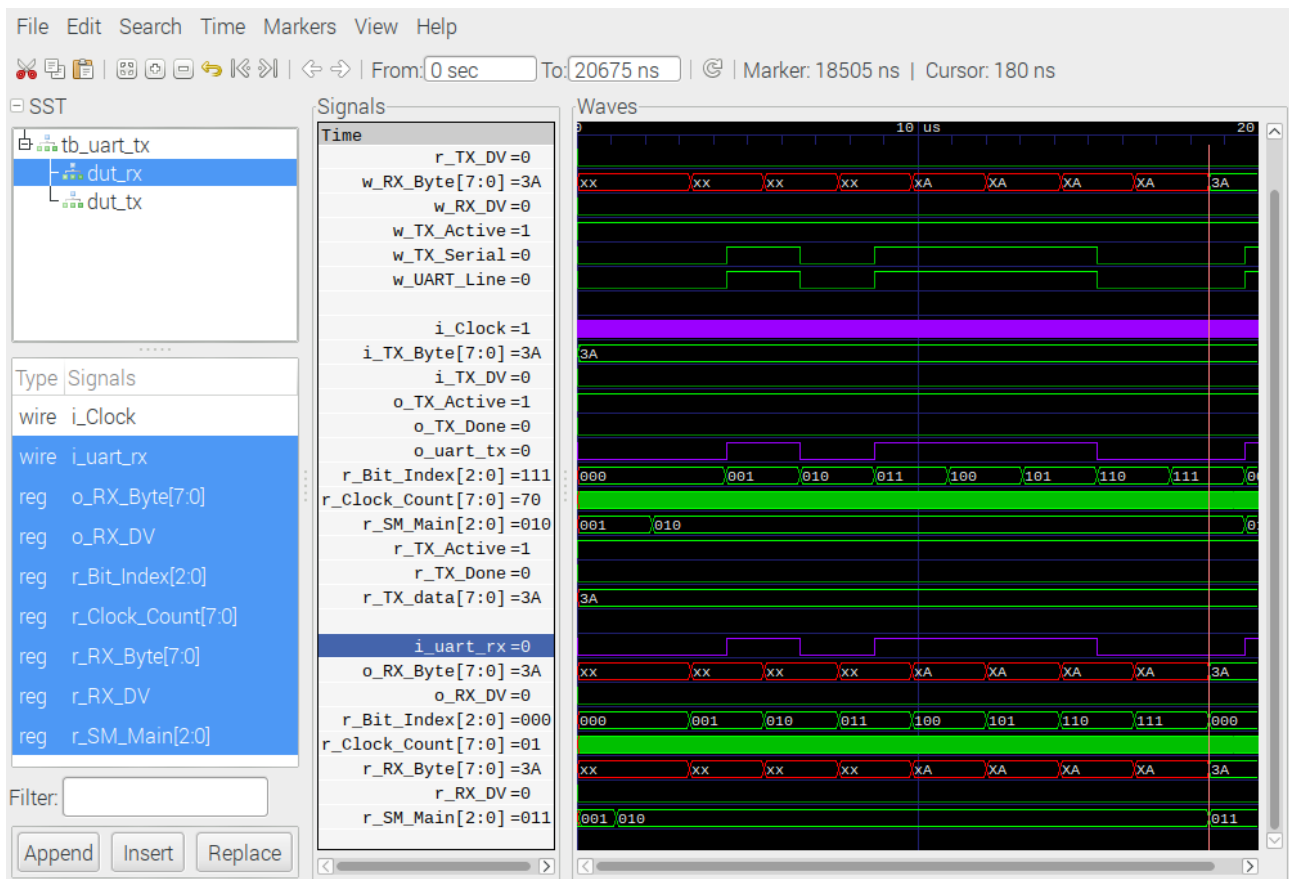


38 transmitted & recived



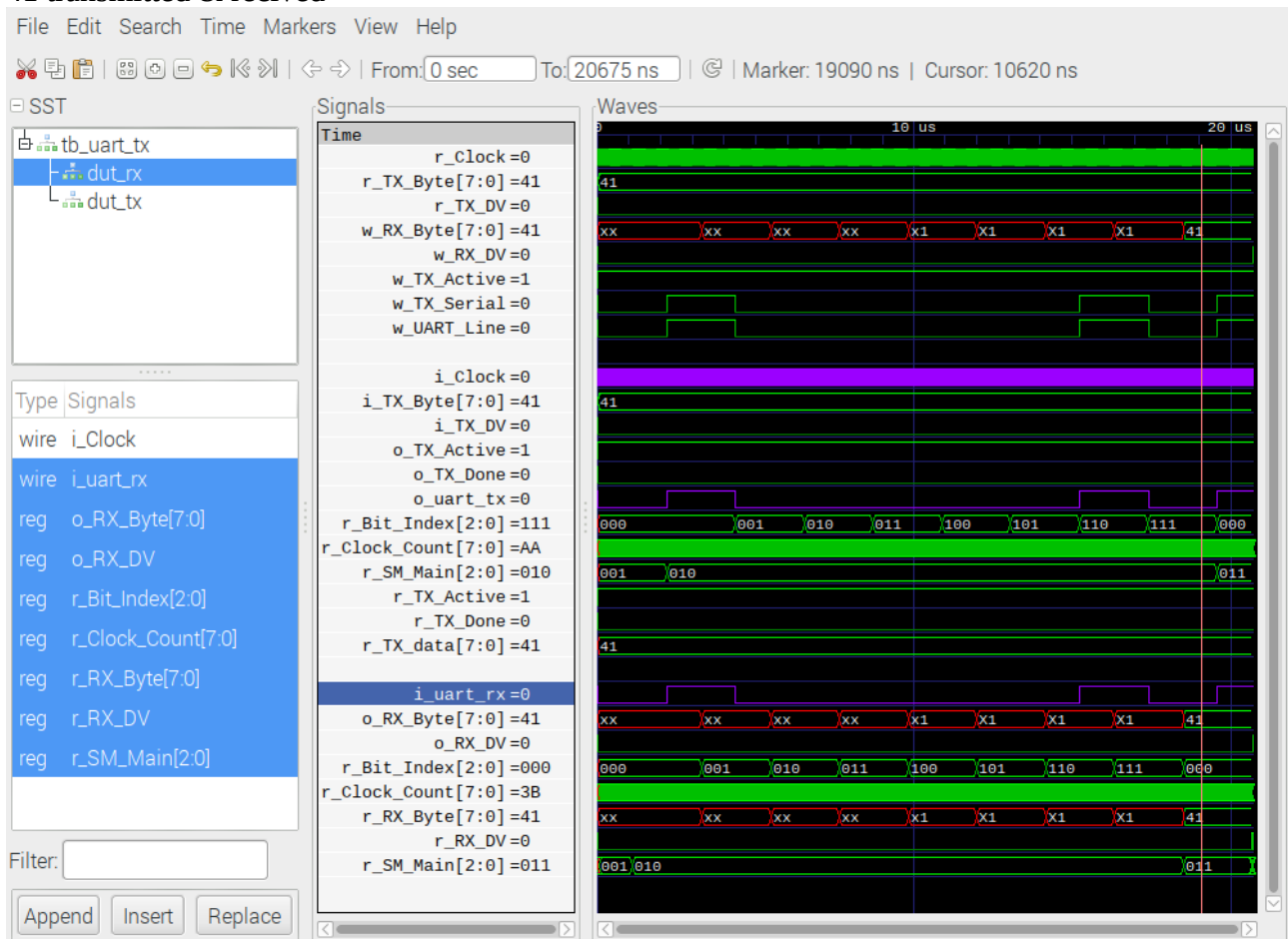
00111000

3A transmitted & recived



00111010

41 transmitted & received



0100001