

\*\*\*\*\***DRAFT**\*\*\*\*\*

**Testing MyHDL created `uart_tx.v` & `uart_rx.v`  
for the CATBOARD**

**based `UART_RX.v` & `UART_TX.v`**

**On a RPi2B**

**05/01/18**

\*\*\*\*\***DRAFT**\*\*\*\*\*

1.0)

**`"cd uart_txrx/catboard"`**

2.0)

**`"./build-Prog-cat.sh 3"`**

This invokes several scripts. The first creates the **`"catboard.blif"`**. The 2<sup>nd</sup> creates the **`"catboard.txt"`**. The 3<sup>rd</sup> creates the **`"catboard.bin"`**. If these files were created the last script programs the FPGA,

**`"catboard.sh"`**

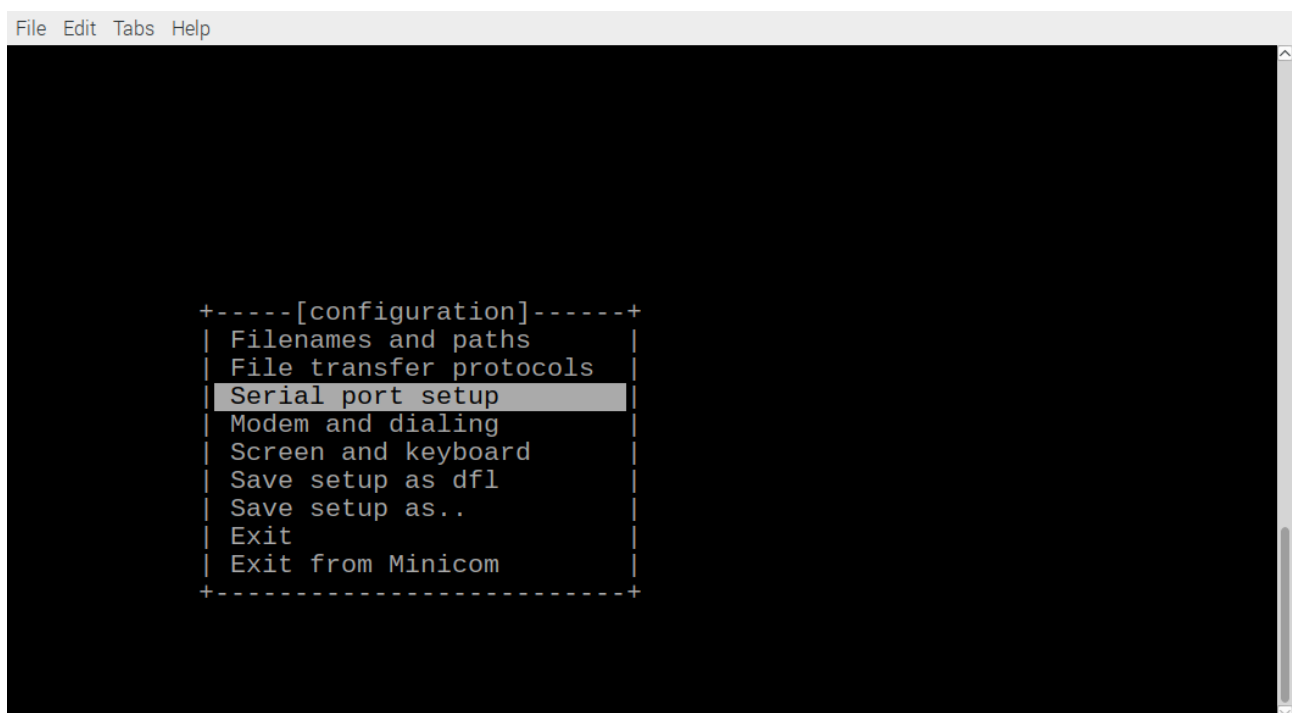
**`"catboard_pnr.sh"`**

**`"catboard_bin.sh"`**

**`"sudo ~/catboard_yosys/config_cat catboard.bin"`**

3.0)

**`"sudo minicom -s"`**



The screenshot shows a terminal window with a menu titled "[configuration]". The menu options are: "Filenames and paths", "File transfer protocols", "Serial port setup" (which is highlighted), "Modem and dialing", "Screen and keyboard", "Save setup as dfl", "Save setup as..", "Exit", and "Exit from Minicom". The terminal window has a menu bar with "File", "Edit", "Tabs", and "Help".

Depressing **`"Enter"`** brings up a new screen

```
File Edit Tabs Help

+-----+
| A -   Serial Device       : /dev/ttyAMA0 |
| B - Lockfile Location    : /var/lock     |
| C -   Callin Program      :              |
| D -   Callout Program     :              |
| E -   Bps/Par/Bits        : 115200 8N1   |
| F - Hardware Flow Control : No           |
| G - Software Flow Control : No           |
|                                     |
|   Change which setting? █             |
+-----+

| Screen and keyboard |
| Save setup as dfl   |
| Save setup as..     |
| Exit                |
| Exit from Minicom   |
+-----+
```

*If the onboard Rpi is used /dev/ttyAMA0 is used as above.  
If the pmodusbuart is connected to pm2-A /dev/ttyUSB0 is used as below.*

*This requires that catboard.pcf be modified*

*The GoBoard codes*

*catboard.pcf.rpi*

*set\_io i\_UART\_RX T15*

*set\_io o\_UART\_TX T14*

*catboard.pcf.pm2-A*

*set\_io i\_UART\_RX B5*

*et\_io o\_UART\_TX B3*

*The MyHDL code*

*uart\_loopback.pcf.rpi*

*set\_io i\_UART\_RX T15*

*set\_io o\_UART\_TX T14*

*uart\_loopback.pcf.pm2-A*

*set\_io i\_UART\_RX B5*

*et\_io o\_UART\_TX B3*

```
File Edit Tabs Help

+-----+
| A -   Serial Device       : /dev/ttyUSB0 |
| B - Lockfile Location    : /var/lock     |
| C -   Callin Program      :              |
| D -   Callout Program     :              |
| E -   Bps/Par/Bits        : 115200 8N1   |
| F - Hardware Flow Control : No           |
| G - Software Flow Control : No           |
|                                         |
|   Change which setting?                 |
+-----+
| Screen and keyboard |
| Save setup as dfl   |
| Save setup as..     |
| Exit                |
| Exit from Minicom   |
+-----+
```

Depressing ***“Enter”*** and scrolling down to ***“Exit”***.

```
File Edit Tabs Help

Welcome to minicom 2.7

OPTIONS: I18n
Compiled on Apr 22 2017, 09:14:19.
Port /dev/ttyAMA0, 15:05:52

Press CTRL-A Z for help on special keys

1234567890!@#$%^&*()-_+=, .<>/?abcdefghijklmnopqrstuvwxyzABCDEFGHIJKLMNOPQRSTUVWXYZ
XYZ█
```

Typing characters get echoed. The programmed FPGA is transmitting the received characters correctly

Thu Apr 19 2018

Initial code was download from  
<https://www.edaplayground.com/x/Pgf>

<http://www.nandland.com>

Command to create **testuart** from **UART\_TB.v** **UART\_RX.v** **UART\_TB/v** includes **UART\_TX.v**

**iverilog -o testuart UART\_TB.v UART\_RX.v**

**vvp testuart**

**VCD info: dumpfile dump.vcd opened for output.**

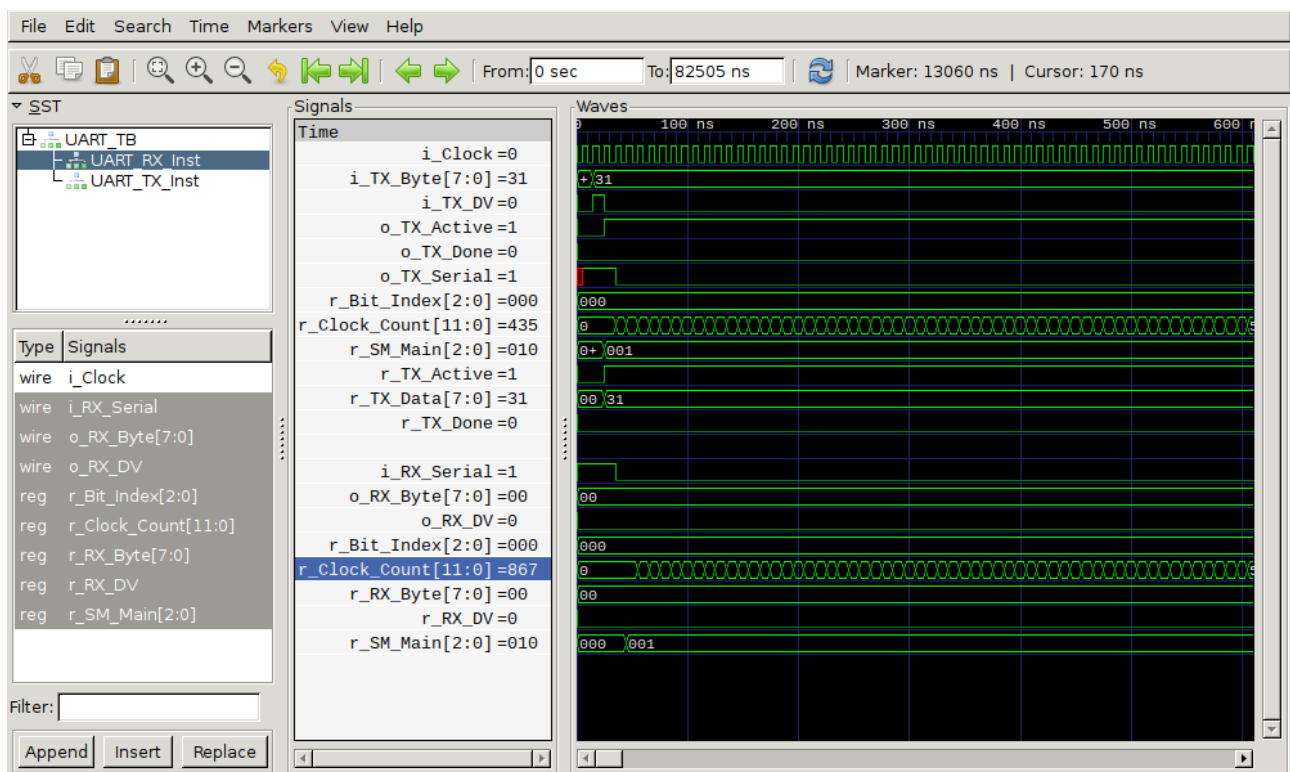
**Test Passed - Correct Byte Received**

This code was created

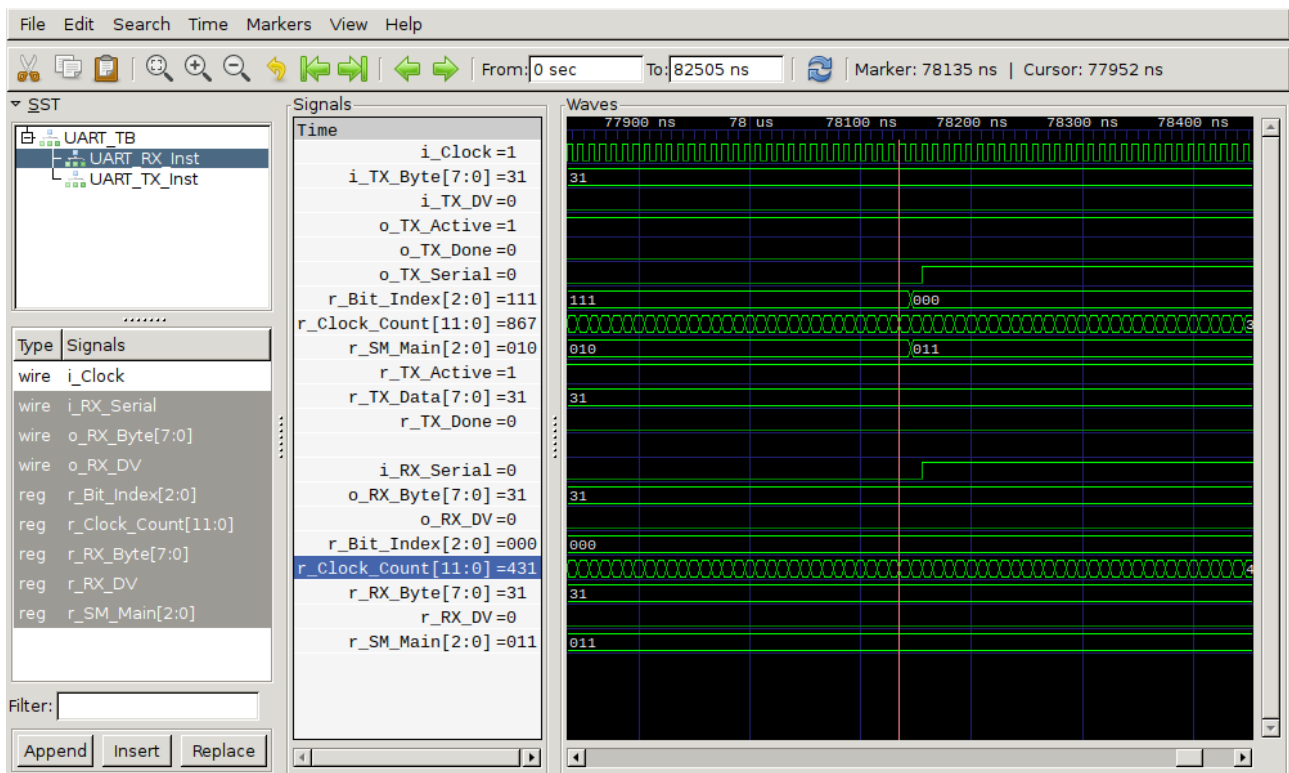
```
// Testbench uses a 25 MHz clock
// Want to interface to 115200 baud UART
// 25000000 / 115200 = 217 Clocks Per Bit.
parameter c_CLOCK_PERIOD_NS = 40;
At 100MHz the parameter c_CLKS_PER_BIT = 868; is required.
```

**Note: This does not fit in 8 bits which required a change in both UART\_TX.v and UART\_RX.v  
reg [7:0] r\_Clock\_Count = 0; → reg [11:0] r\_Clock\_Count = 0;**

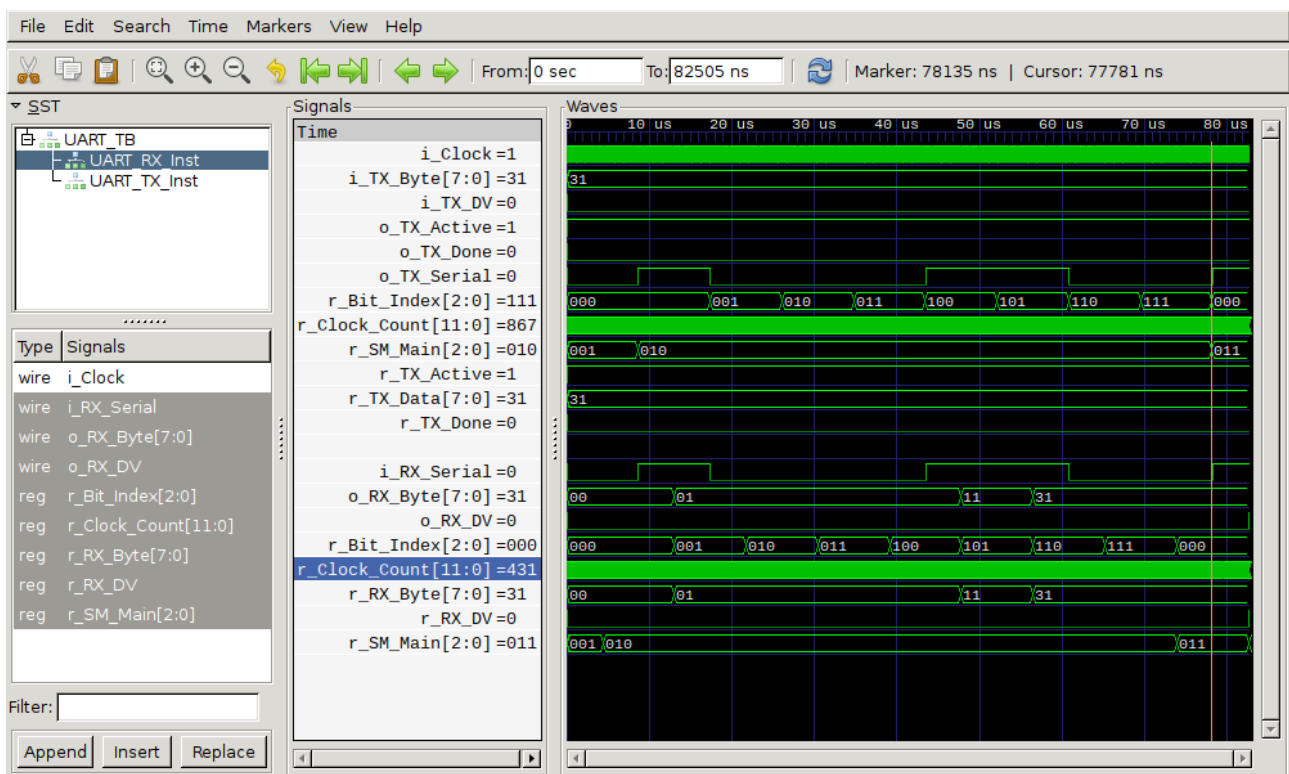
**In UART\_TB.v parameter c\_CLKS\_PER\_BIT = 217 → parameter c\_CLKS\_PER\_BIT = 868;**



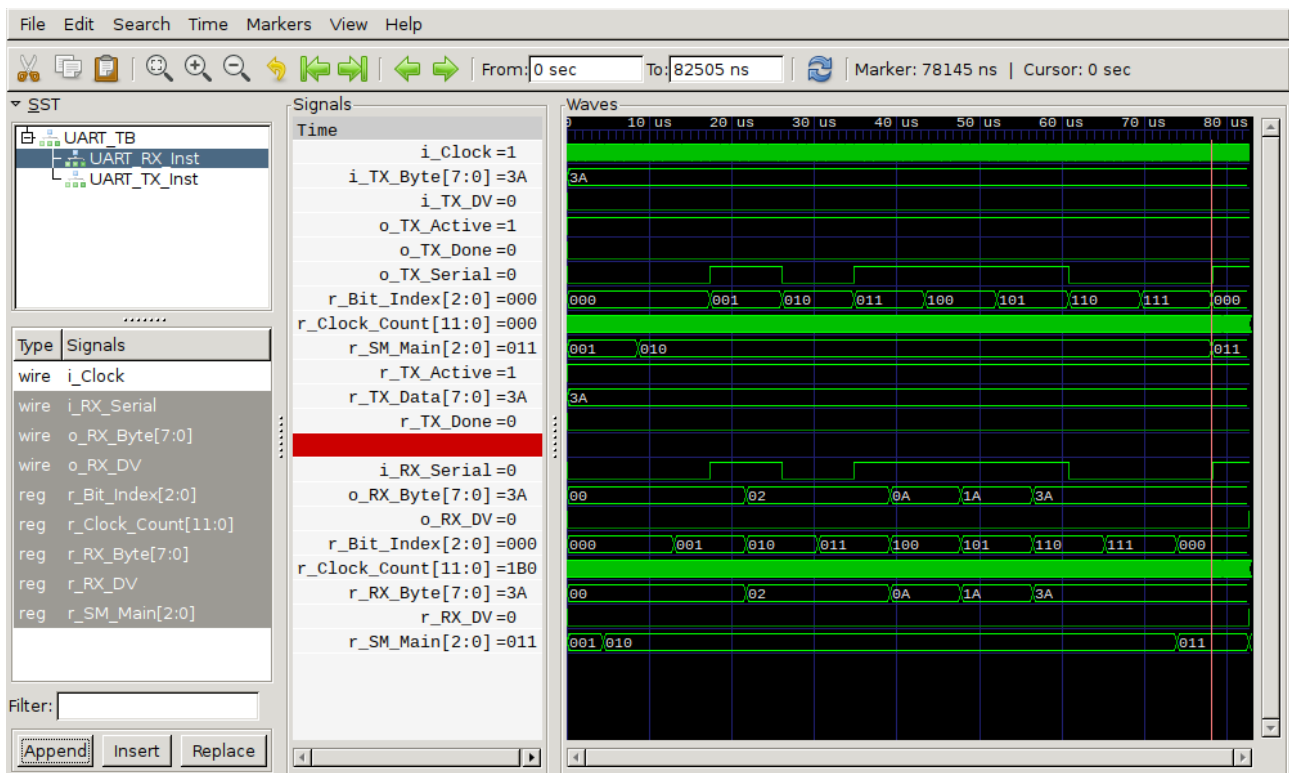
Checking that r\_Clock\_Count does not overflow with 868.



Simulation of 00110001 being transmitted and received.



Simulation of 00110101 being transmitted and received.



Both the UART\_TX and UART\_RX are a case statement  
 IDLE, TX\_START\_BIT, TX\_DATA\_BITS, TX\_STOP\_BIT, and C:EANUP.  
 IDLE, RX\_START\_BIT, RX\_DATA\_BITS, RX\_STOP\_BIT, and C:EANUP.  
 In MyHDL the case statement was written for uart\_tx.

***if(r\_SM\_Main==IDLE):***

•  
•

***elif (r\_SM\_Main==TX\_START\_BIT):***

•

```

        .
    elif (r_SM_Main==TX_DATA_BITS):
        .
        .
    elif (r_SM_Main==TX_STOP_BIT):
        .
        .
    else:
        .
        .
and the uart_rx was similar
if(r_SM_Main==IDLE):
    .
    .
    elif (r_SM_Main==RX_START_BIT):
        .
        .
    elif (r_SM_Main==RX_DATA_BITS):
        .
        .
    elif (r_SM_Main==RX_STOP_BIT):
        .
        .
    else:
        .
        .

```

In the simulation the r\_TX\_BYTE is set to byte to be transmitted and a 1 clock wide r\_TX\_DV.

```

r_TX_DV  <= 1'b1;
r_TX_Byte <= 8'h3A;
@(posedge r_Clock);
r_TX_DV <= 1'b0;

```

Testing at 100 MHz appears okay  
Using MyHDL to create *uart\_rx.v* with *uart\_rx.py*  
& *uart\_tx.v* with *uart\_tx.py*

***iverilog -o testuart tb\_dut\_uart\_txx.v uart\_rx.v***

***vvp testuart***  
***VCD info: dumpfile dump.vcd opened for output.***  
***Test Passed - Correct Byte Received***

Several simulations were tested 0x3F, 0x32, 0x38, 0x3A, 0x41.  
3F transmitted & received

00111111  
32 transmitted & received  
00110010

38 transmitted & received

00111000  
3A transmitted & received

00111010  
41 transmitted & received

01000001

uart\_txx.sh            catboard.sh

uart\_txx\_pnr.sh       catboard\_pnr.sh  
uart\_loopback.pcf     catboard.pcf



```
uart_txrx_bin.sh      catboard_bin.sh
```

```
/home/pi/uart_rxtx/MyHDL  
sudo ~/catboard_yosys/config_cat uart_loopback.bin
```

```
/home/pi/uart_rxtx/catboard  
sudo ~/catboard_yosys/config_cat catboard.bin
```

```
.
```