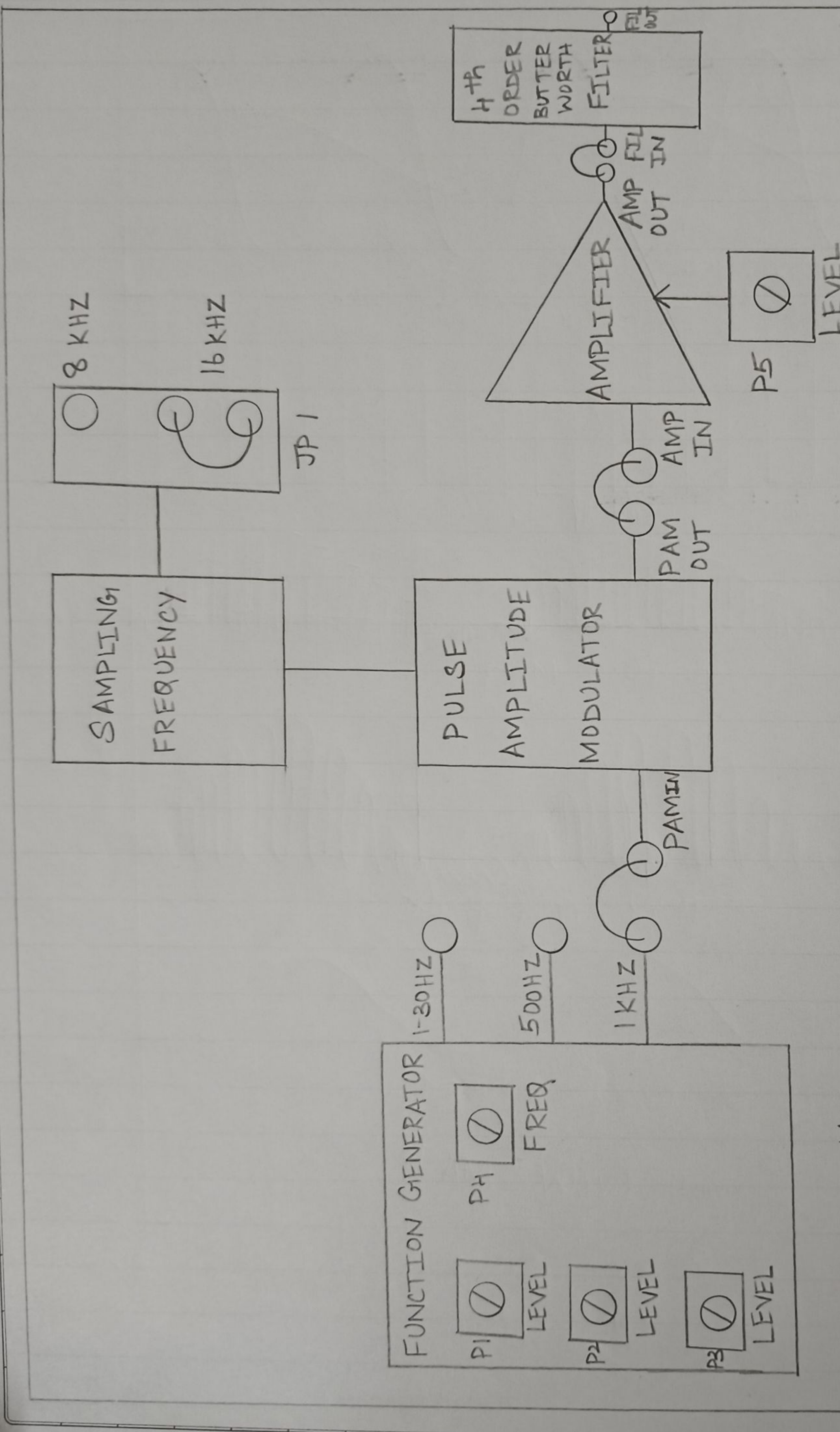
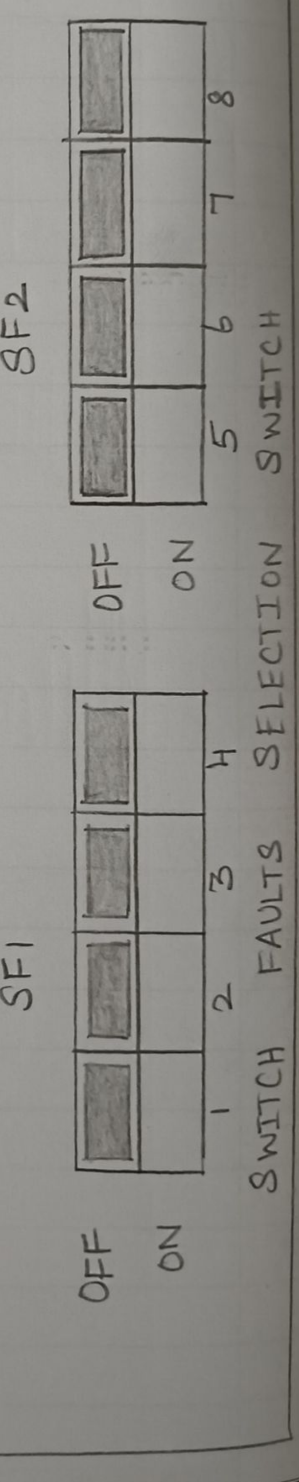
BLOCK DIAGRAM:



BLOCK DIAGRAM FOR PULSE AMPLITUDE MODULATION AND DEMODULATION



Date

Expt. No. 1) A)

Page No.

PULSE AMPLITUDE MODULATION

AIM:

TO Conduct an experiment to generate PAM Signal and also design a circuit to demodulate the Obtained PAM Signal and Verify Sampling theorem. Plot the Relevant Waveform.

COMPONENTS REQUIRED:

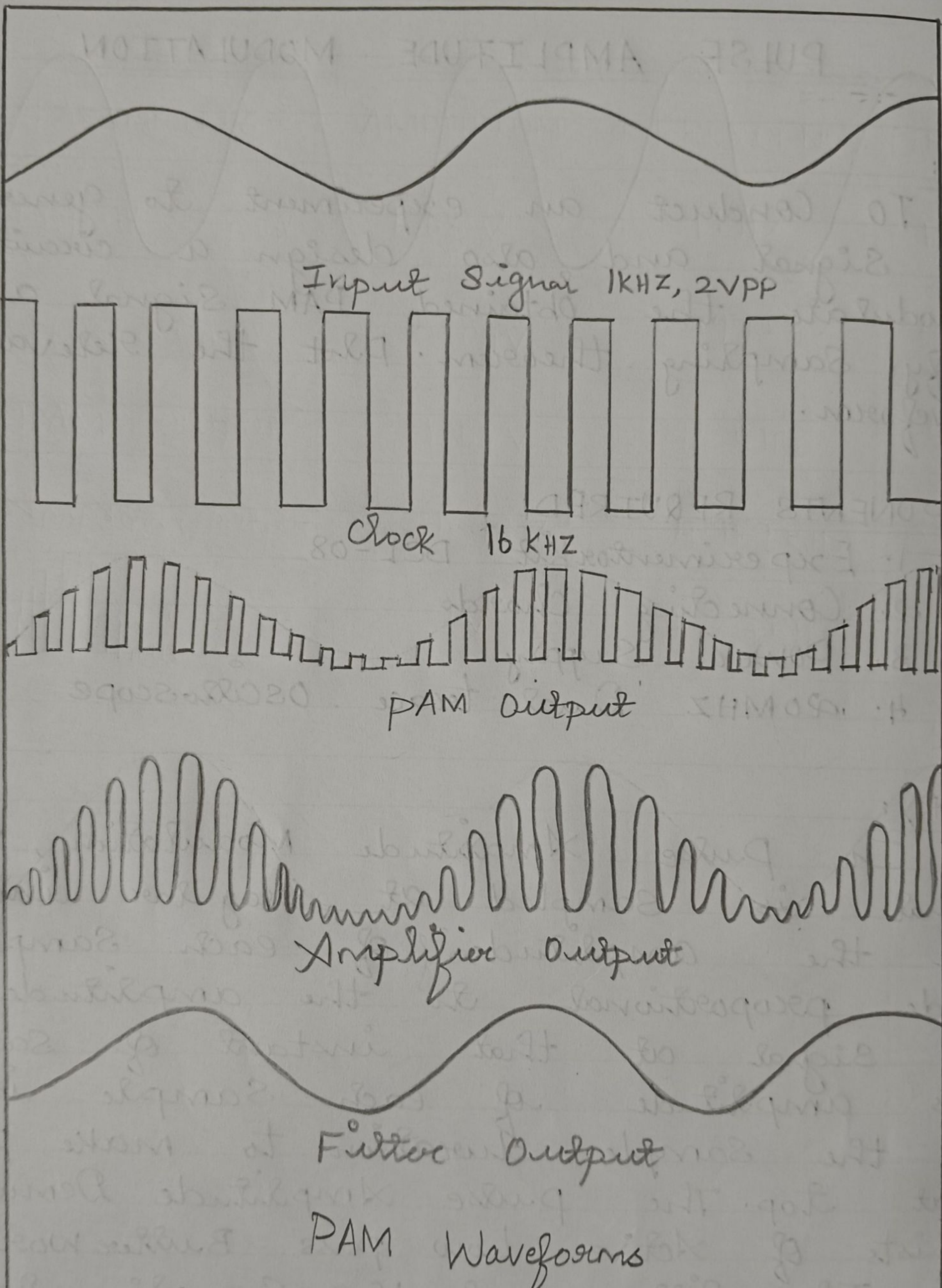
1. Experimentor Kit DCL-08
2. Connecting Chords
3. Power Supply
4. 20MHZ Dual trace OSCilloscope

THEORY:

In Pulse Amplitude Modulation, the Signal is sampled at regular intervals and the amplitude of each Sample is Made proportional to the amplitude of the signal at that instant of Sampling. This amplitude of each Sample is hold for the sample duration to make pulses flat top. The pulse Amplitude Demodulator Consists of Active Low pass Butter worth filter. It filters out the Sampling frequency and their harmonics from the Modulated Signal and recovers the base band by integrated action.

Teacher's Signature

MODEL GRAPH:



PAM Waveforms

PROCEDURE:

1. Refer to the block diagram and carry out the following connections and switch settings.

2. Connect the power supply with proper polarity to the kit DCL-08 and switch it on.

3. Select 16 KHZ sampling frequency by jumper JP1.

4. Connect the 1KHZ, 2V P-P sine wave signal generated onboard to PAM IN post.

5. Observe the pulse Amplitude Modulation output at PAM OUT post.

6. Short the following posts with the connecting chords provided as shown in block diagram.

PAM OUT and AMP IN
AMP OUT and FIL IN

7. Keep the amplifier gain control potentiometer P5 to maximum completely clockwise.

8. Observe the pulse Amplitude Demodulated signal at FIL OUT, which is same as the input signal.

9. Repeat the experiment for different input signal and sampling frequencies.

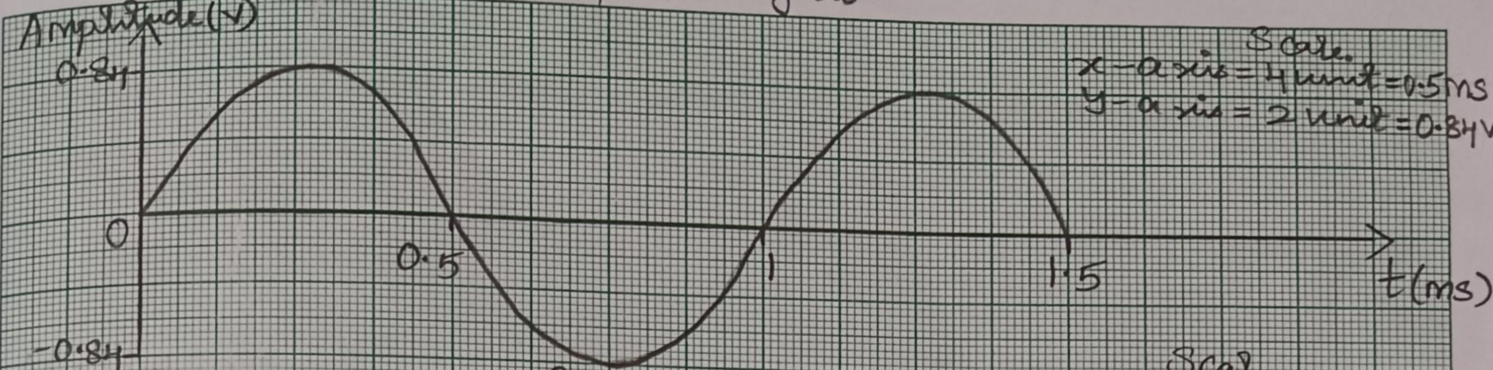
TABULATION:

S.No	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input signal	1.68 V	1 KHZ	1 ms
2.	Clock signal	5.04 V	15.97 KHZ	62.61 μs
3.	PAM Output	1.56 V	16 KHZ	62.5 μs
4.	Amplifier output	1.78 V	4.119 KHZ	242.7 μs
5.	Filter Output	1 V	1.003 KHZ	1 ms

Pulse Amplitude Modulation

Input Signal

Scale
x-axis = 4 unit = 0.5ms
y-axis = 2 unit = 0.84V

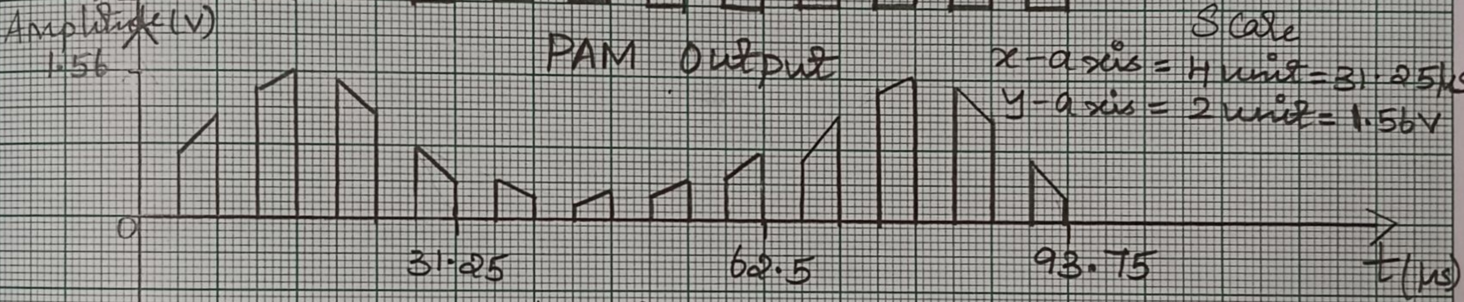


Clock Signal

Scale
x-axis = 62.61 μs
y-axis = 2 unit = 2.52V

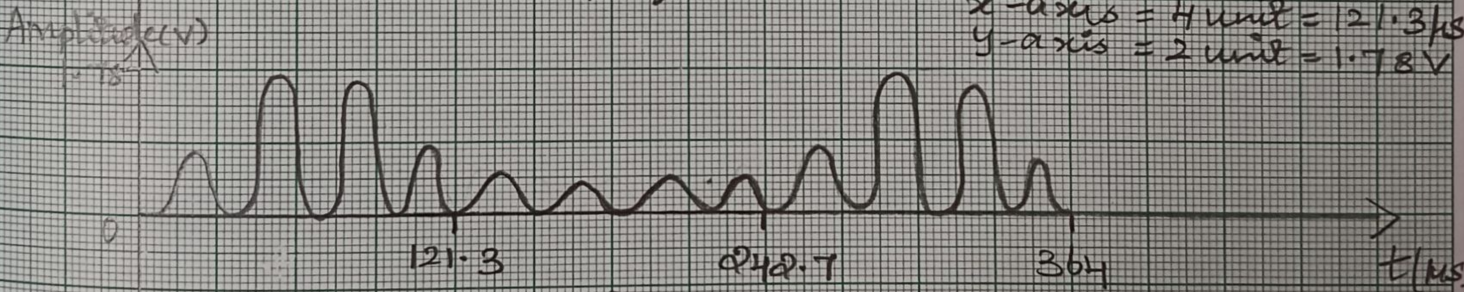
PAM output

Scale
x-axis = 4 unit = 31.25μs
y-axis = 2 unit = 1.56V



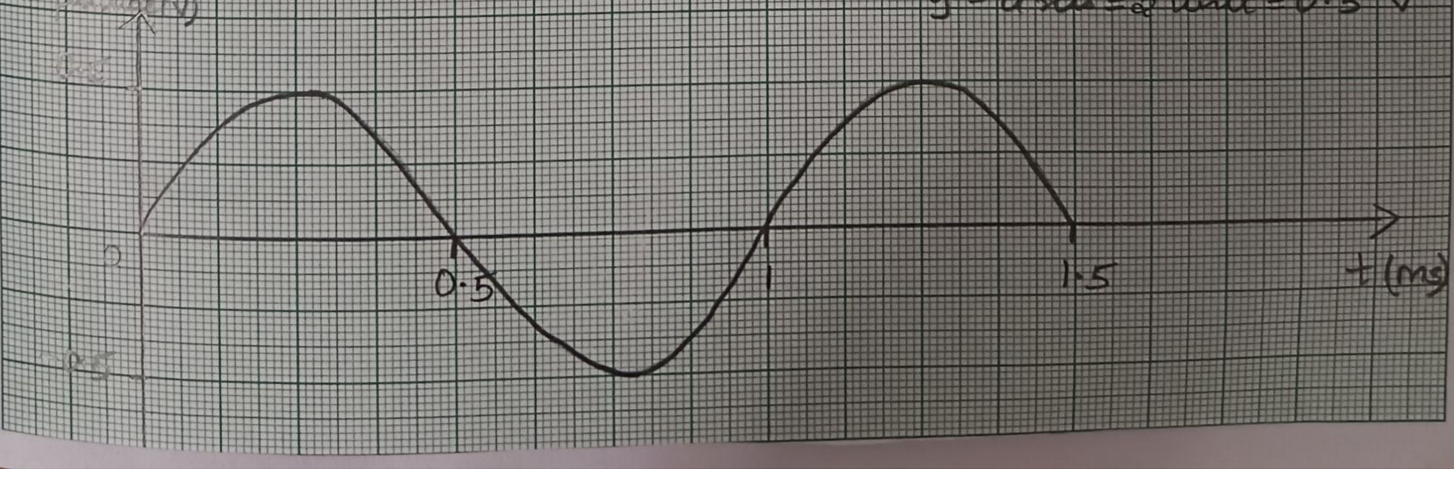
Amplifier output

Scale
x-axis = 4 unit = 121.3μs
y-axis = 2 unit = 1.78V



Filter output

Scale
x-axis = 4 unit = 0.5ms
y-axis = 2 unit = 0.5 V



Expt. No. ______ Date ______

Page No. ______

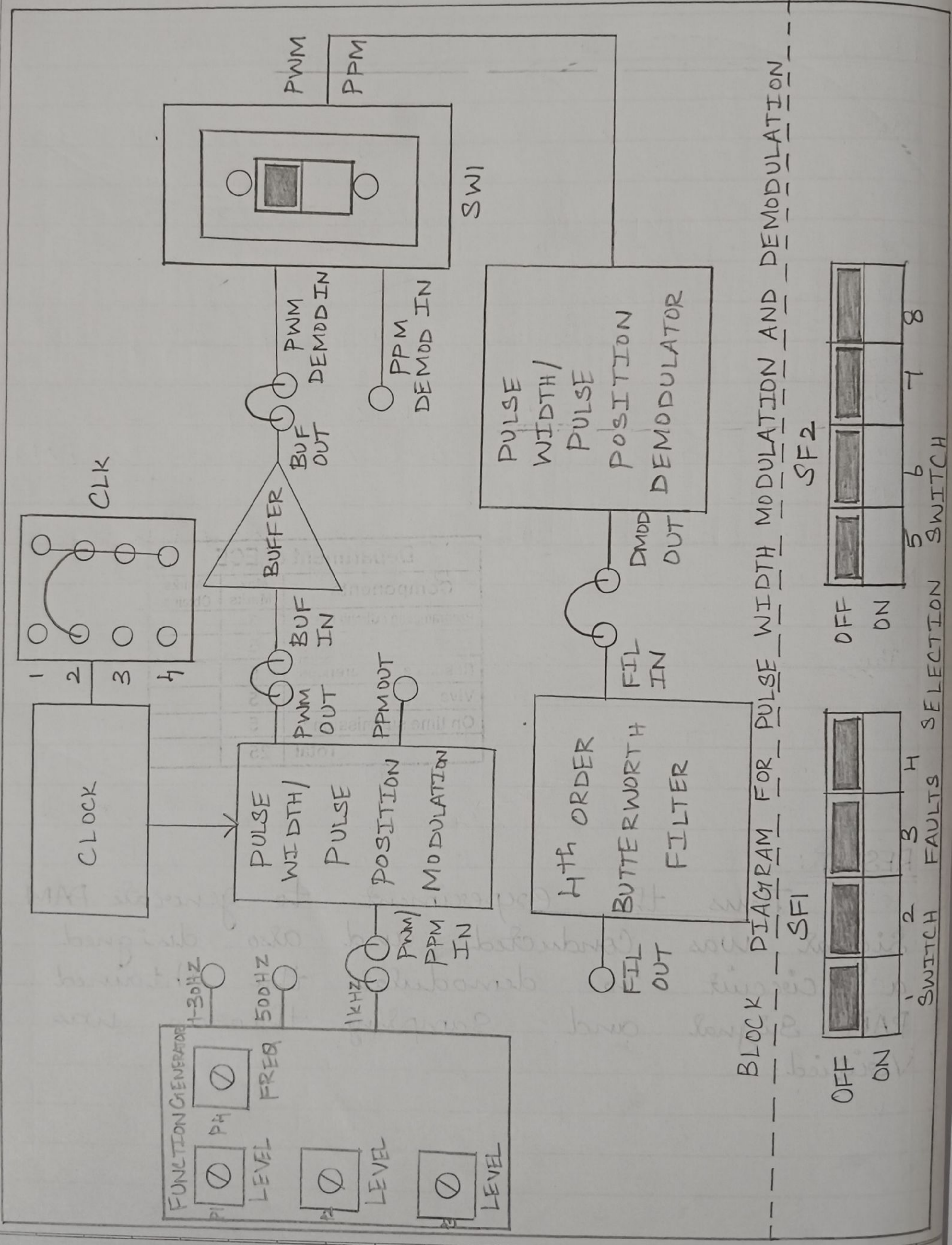
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT :

Thus the experiment to generate PAM Signal was Conducted and also designed a circuit to demodulate the Obtained PAM Signal and Sampling theorem was Verified.

Teacher's Signature ______

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR PULSE WIDTH MODULATION AND DEMODULATION

Date

Expt. No. 1) B)

Page No.

PULSE WIDTH MODULATION

AIM:

TO Conduct an experiment to generate PWM Signal and also design a circuit to demodulate the obtained PWM Signal and Verify Sampling theorem. plot the relevant waveforms.

COMPONENTS REQUIRED:

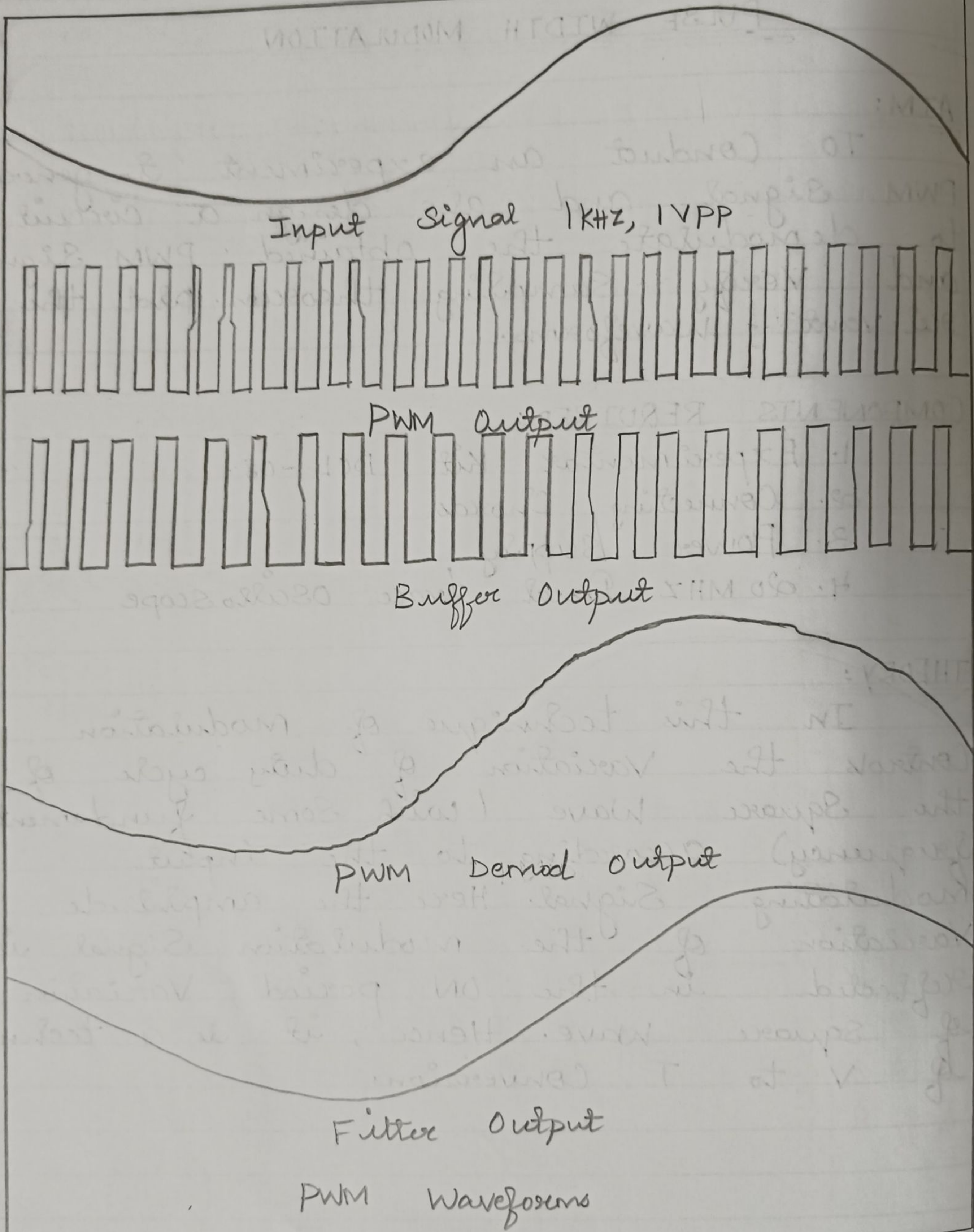
1. Experimentar Kit DCL-08.
2. Connecting Chords
3. Power Supply
4. 20 MHZ Dual trace oscilloscope

THEORY:

In this technique of modulation controls the Variation of duty cycle of the Square Wave (with Some fundamental frequency) according to the input modulating Signal. Here the amplitude Variation of the modulation Signal is reflected in the ON period Variation of square wave. Hence, it is a technique of V to T conversion.

Teacher's Signature

MODEL GRAPH:



PWM Waveforms

Date
Expt. No.
Page No.

PROCEDURE :

1. Refer to the block diagram and carry out the following connections and switch settings.

2. Connect the power supply with proper polarity to the kit DCL-08 and switch it on.

3. Put jumper JP3 to 2nd position.

4. Select 1KHZ 1V-pp Sine Wave Signal generated onboard.

5. Connect this signal to PWM/PPM IN.

6. observe the pulse width modulated output at PWM OUT post. Note that since the sampling frequency is high, only blurred band in waveform will be observed due to persistence of vision. In absence of input signal only square wave of fundamental frequency and fixed on time will be observed and no width variation are present. To observe the variation in pulse width, apply 1-30 HZ Sine wave signal to PWM/PPM IN post. Vary the frequency from 1-30 HZ.

7. Short the following posts with the connecting chords provided as shown in block diagram for demodulation section.

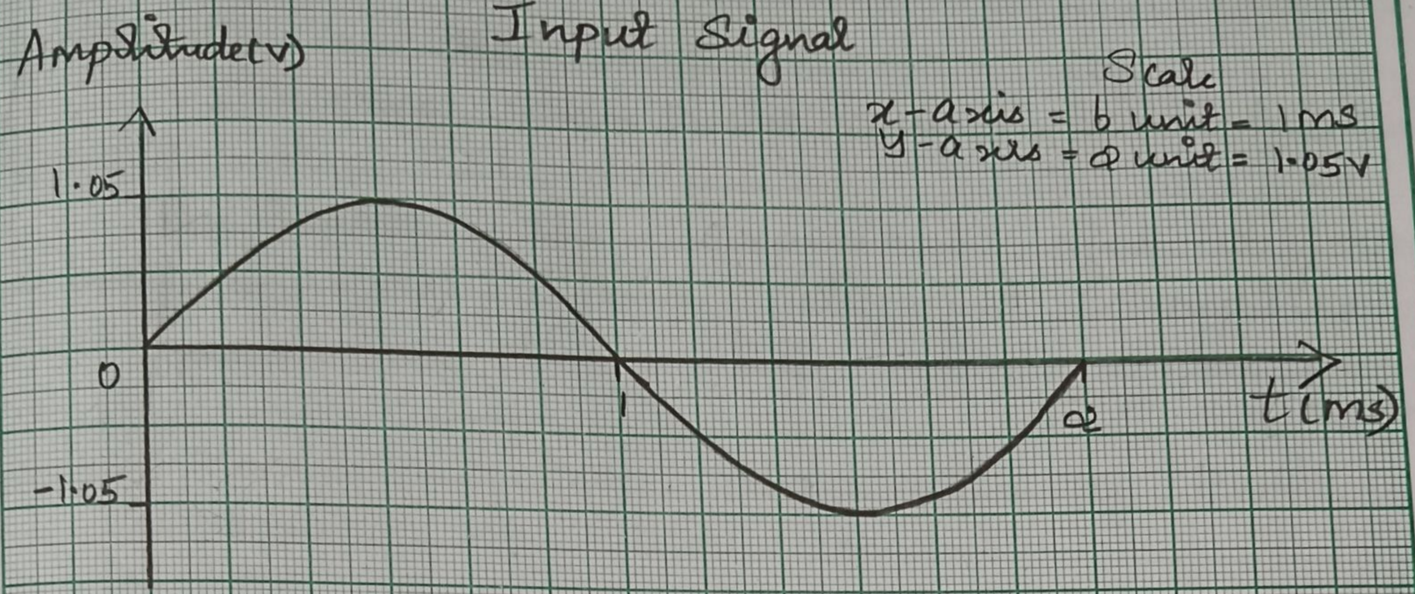
PWM OUT and BUF IN
BUF OUT and PWM DMOD IN

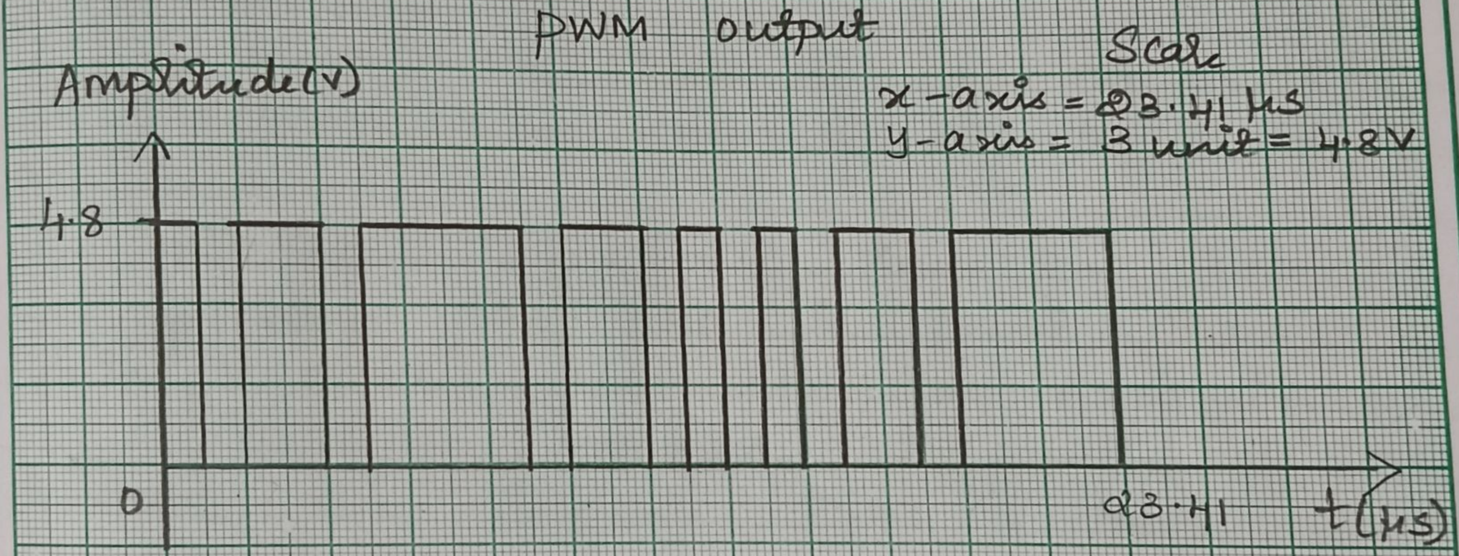
Teacher's Signature

TABULATION:

S.NO	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input Signal	2.10V	498.8 HZ	2ms
2.	PWM Output	4.8 V	42.70 KHZ	23.41 μs

Pulse Width Modulation





DMOD OUT and FIL IN.

8. Observe the pulse width Demodulated output at FIL OUT.

9. Repeat the experiment for different input Signal and different sampling Clocks with the help of jumper JP3.

Note: procedure For observation of PWM Output in DUAL mode:

1. Keep CH1 Knob of CRO on 1 volt/div ac
2. Keep CH2 Knob of CRO on 2 Volts/div ac
3. Keep Times/div Knob on 1 msec.
4. Keep the CRO in Dual Channel (Auto/TV mode). Use X10 for expansion.
5. After proper triggering of CRO, observe the Signals PWM IN and PWM OUT Simultaneously.

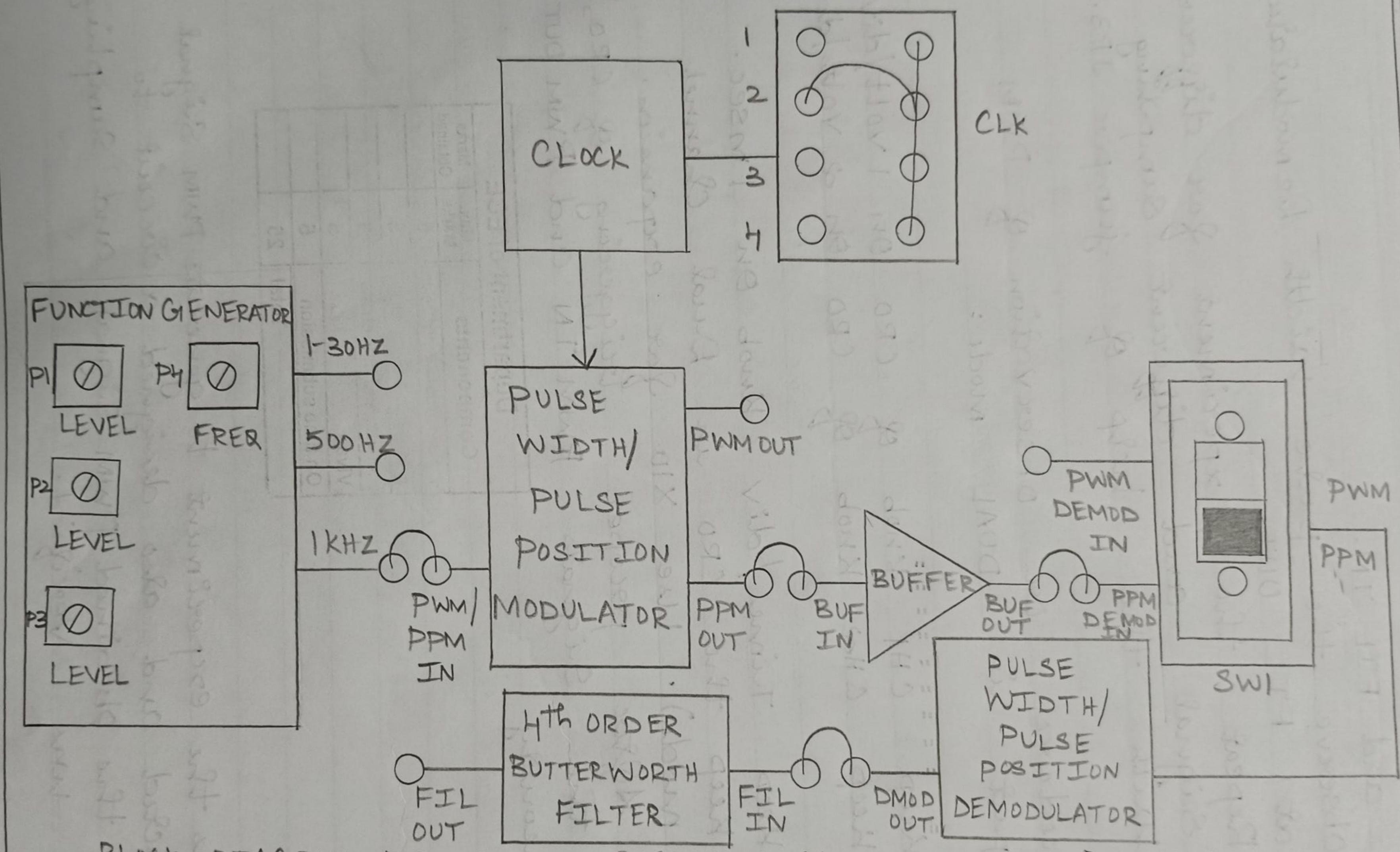
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

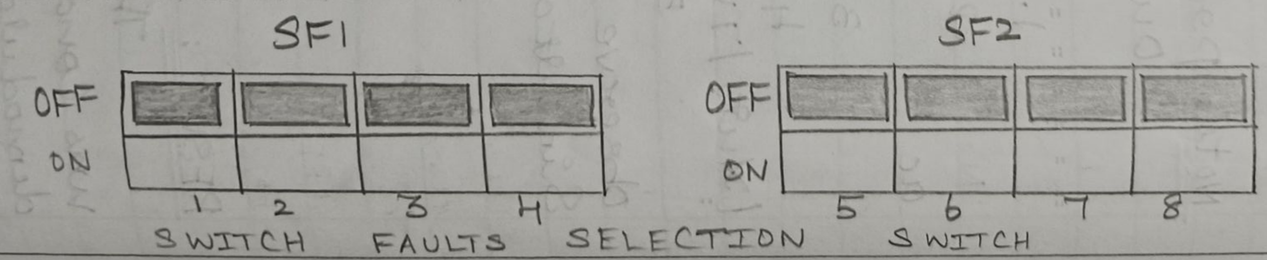
Thus the experiment to generate PWM Signal was conducted and also designed a circuit to demodulate the obtained PWM Signal and Sampling theorem was Verified.

Teacher's Signature

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR PULSE POSITION MODULATION AND DEMODULATION



Expt. No. 1) c)

Date

Page No.

PULSE POSITION MODULATION

AIM:

TO Conduct an experiment to generate PPM Signal and also design a circuit to demodulate the obtained PPM Signal and Verify Sampling theorem. Plot the relevant Waveforms.

COMPONENTS REQUIRED:

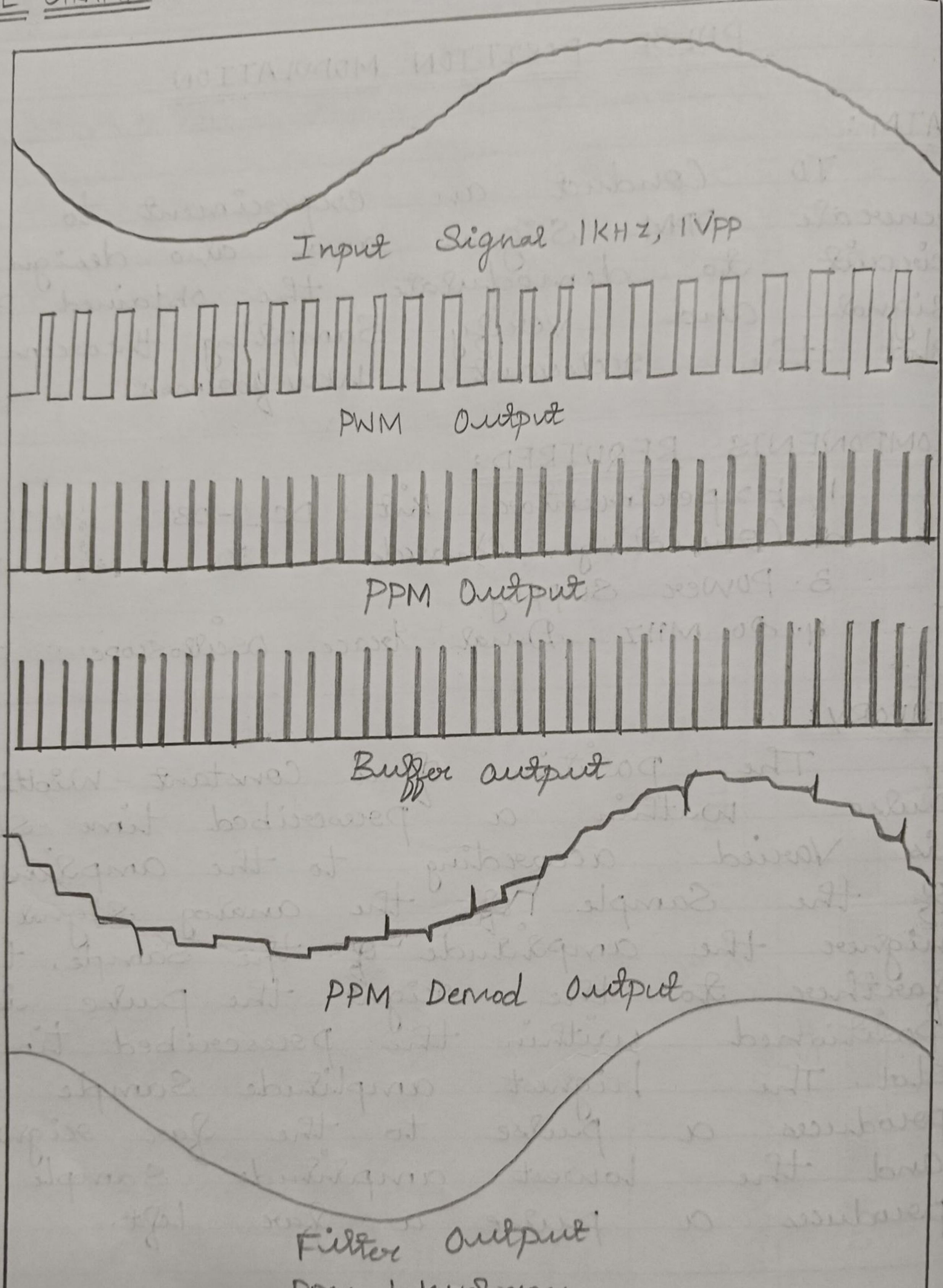
1. Experimentor Kit DCL-08
2. Connecting Chords
3. Power Supply
4. 20 MHZ Dual trace oscilloscope

THEORY:

The position of a Constant-Width pulse within a prescribed time slot is Varied according to the amplitude of the Sample of the analog signal. The higher the amplitude of the Sample, the farther to the right the pulse is positioned within the prescribed time slot. The highest amplitude Sample produces a pulse to the far right, and the lowest amplitude Sample produces a pulse a far left.

Teacher's Signature

MODEL GRAPH:



PPM Waveforms

Expt. No. ____________ Date ____________ Page No. ____________

PROCEDURE :

1. Refer to the block diagram and carry out the following connections and switch settings.

2. Connect the power supply with proper polarity to the kit DCL-08 and switch it on.

3. put jumper JP3 to 2nd position.

4. Select 1KHZ, 1V-PP sine wave signal generated onboard.

5. Connect the selected signal to the PWM/PPM IN.

6. Observe the pulse position Modulated Output at PPM OUT post with shifted position on time scale. Please note amplitude and width of pulse are same and there is shift in position which is proportional to input Analog signal.

7. To observe the variation in pulse positions, apply 1-30HZ sine wave signal to PWM/PPM IN post vary the frequency from 1-30 HZ and observe the signal on oscilloscope in dual for posts PPM OUT and PWM OUT simultaneously.

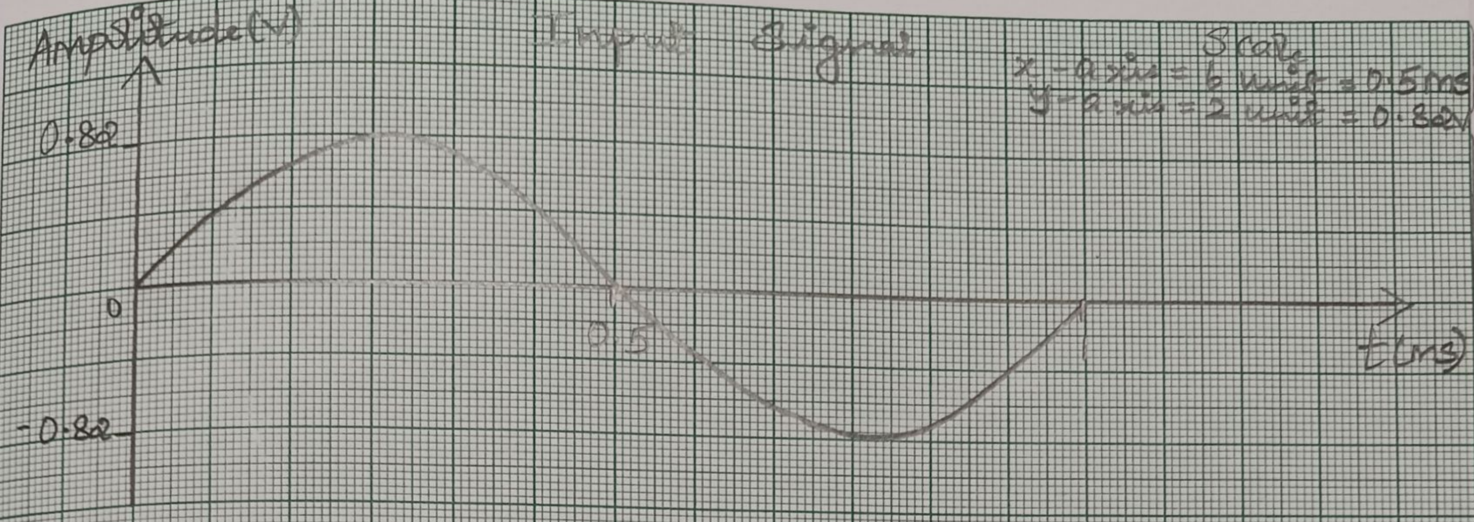
8. Then short the following posts with the link provided as shown in block diagram for Demodulation Section.
PPM OUT and BUFIN

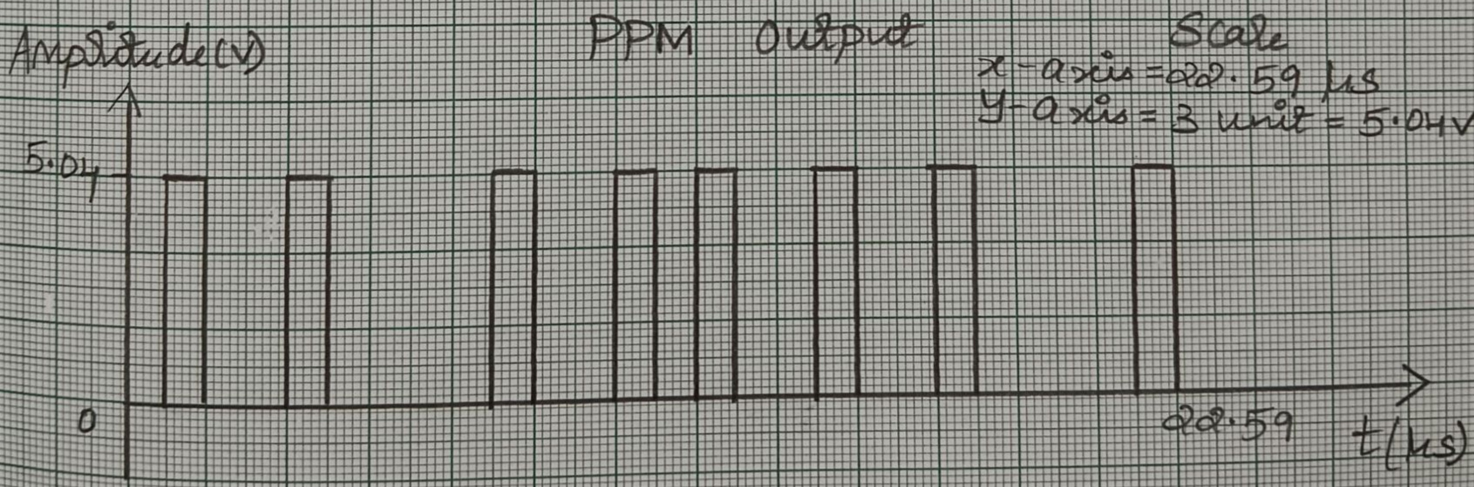
Teacher's Signature ____________

TABULATION:

S.NO	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input Signal	1.64 V	995.4 HZ	1 mS
2.	PWM Output	4.8V	44.44 KHZ	22.5μs
3.	PPM Output	5.04V	44.26 KHZ	22.59μs

Pulse position Modulation





Expt. No. ______ Date ______

Page No. ______

BUFOUT and PPM DMOD IN
DMOD OUT and FIL IN

9. Observe the pulse position Demodulated signal at FIL OUT.

10. Repeat the experiment at different input signal and different sampling frequencies.

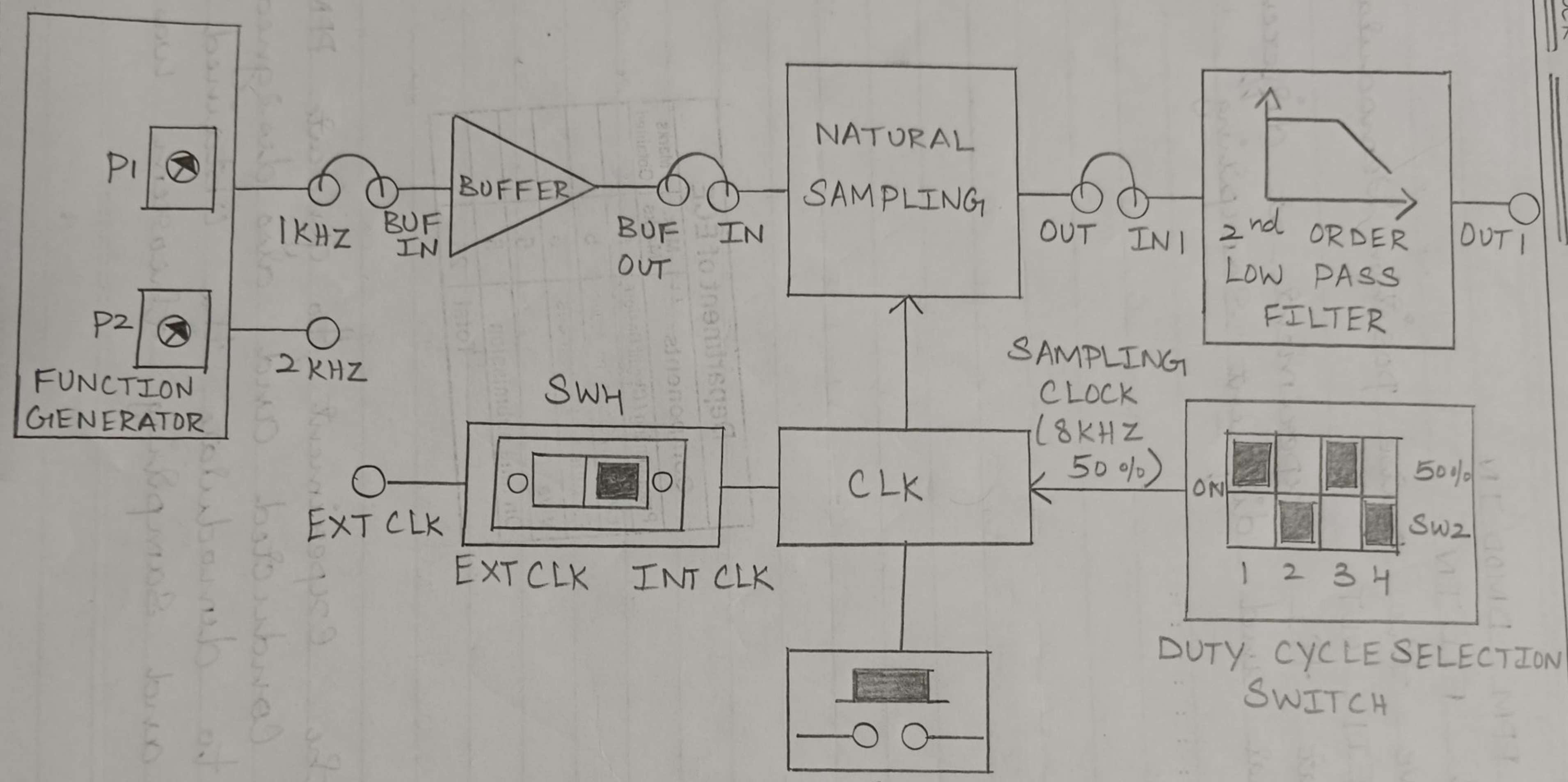
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

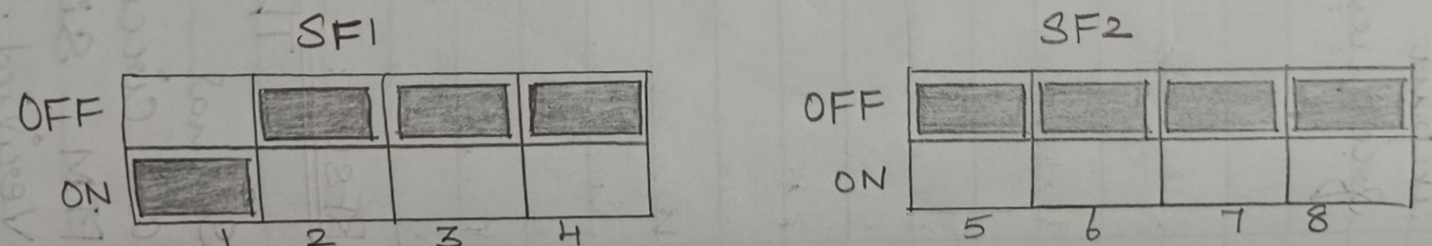
Thus the experiment to generate PPM signal was conducted and also designed a circuit to demodulate the Obtained PPM signal and sampling theorem was verified.

Teacher's Signature ______

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR NATURAL SAMPLING



SWITCH FAULTS SELECTION SWITCH

Expt. No. 2) A)

Date

Page No.

NATURAL SAMPLING

AIM:

To Study the Natural sampling signals and its reconstruction.

COMPONENTS REQUIRED:

1. Experimentor Kit DCL-01
2. Connecting Chords
3. Power Supply
4. 20 MHZ Dual Trace oscilloscope

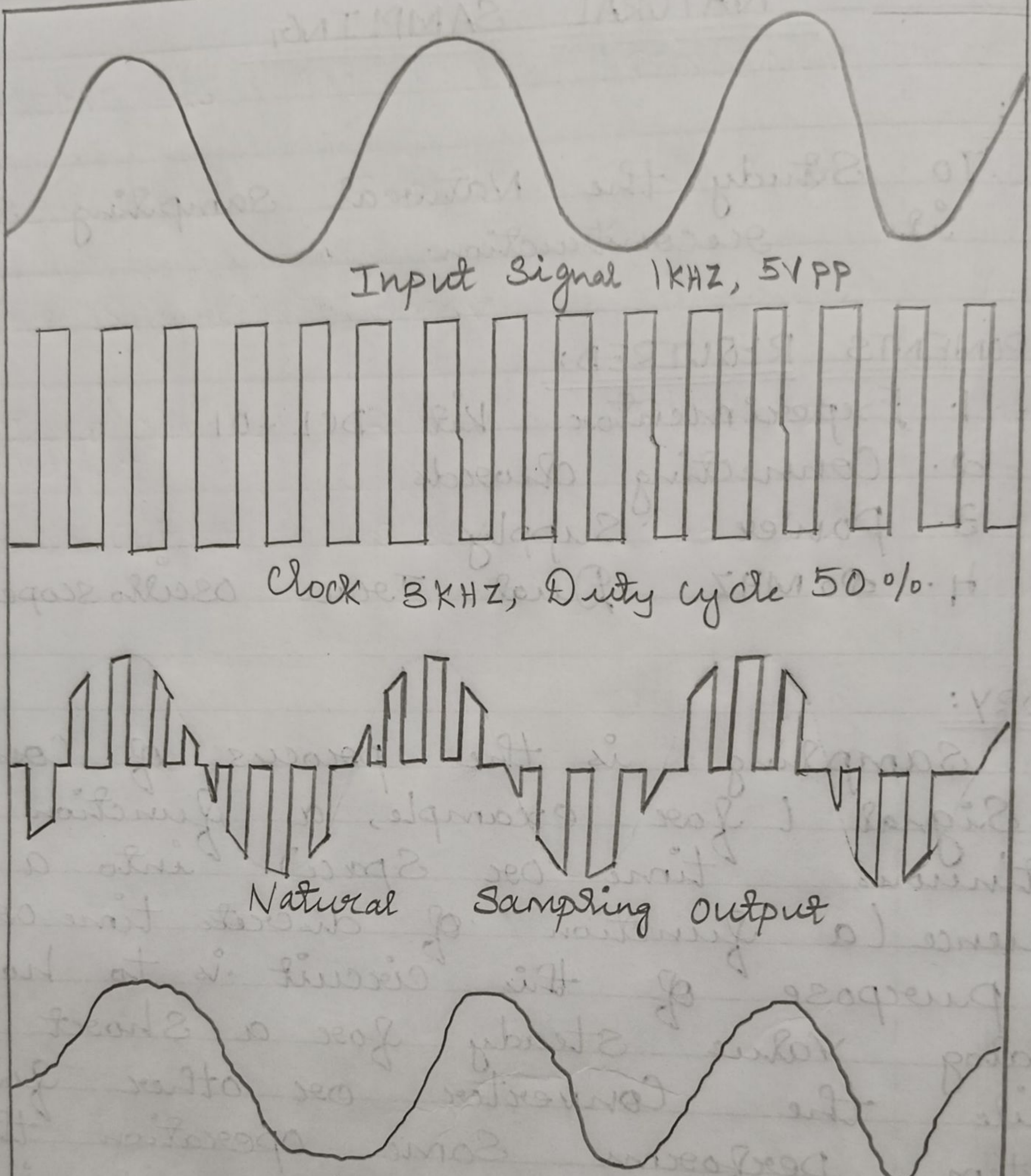
THEORY:

Sampling is the process of converting a signal (for example, a function of continuous time or space) into a numeric sequence (a function of discrete time or space). The purpose of this circuit is to hold the analog value steady for a short time while the converter or other following system performs some operation that takes a little time. Here, capacitor is used to store the analog voltage and an electronic switch or gate is used to alternately connect and disconnect the capacitor from the analog input. The rate at which this switch is operated is the sampling rate of the system.

$$f_s \geq 2f_m$$

Teacher's Signature

MODEL GRAPH:



Waveforms Natural Sampling

Expt. No. ______ Date ______ Page No. ______

PROCEDURE:

1. Refer to the Block diagram carry out the following connections and switch settings.

2. Connect power supply in proper polarity to the kit DCL-01 & Switch it on.

3. Connect the 1KHZ, 5VPP Sine Wave signal, generated onboard, to the BUFIN post of the BUFFER and BUF OUT post of the BUFFER to the IN post of the Natural Sampling block by means of the connecting chords provided.

4. Connect the Sampling frequency clock in the internal mode INT CLK using Switch (SW4).

5. Using clock selector switch (S1) Select 8KHZ Sampling frequency.

6. Using Switch SW2 Select 50% duty cycle.

7. Connect the OUT post of the Natural sampling block to the input IN1 post of the 2nd Order Low pass Butterworth Filter and take necessary Observation as mentioned below.

8. Repeat the procedure for the 2KHZ sine wave signal as input.

Teacher's Signature ______

TABULATION:

S.NO	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input Signal	3.24 V	956.9 HZ	1.04 ms
2.	Clock Signal	9.20V	61.42 KHZ	16.28 μs
3.	Natural Sampling Output	3.80V	916.6 HZ	1.09 ms
4.	Filter Output	2.36V	955.7HZ	1.04ms

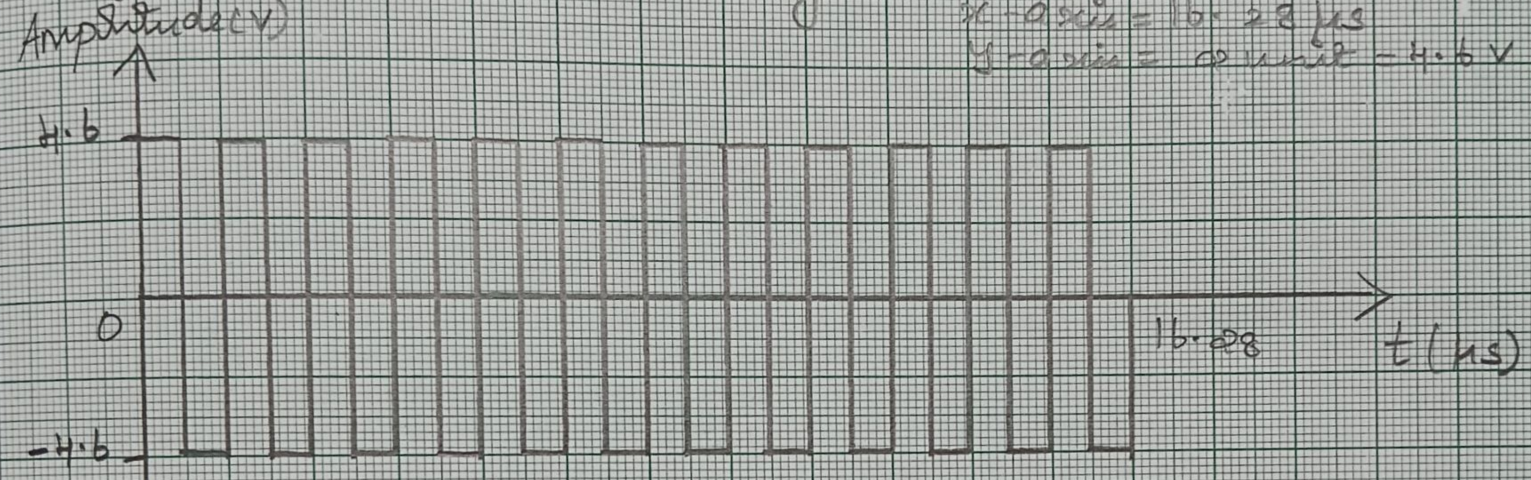
Natural Sampling

Input Signal

Scale
x-axis = 4 unit = 0.52 ms
y-axis = 2 unit = 1.62 V

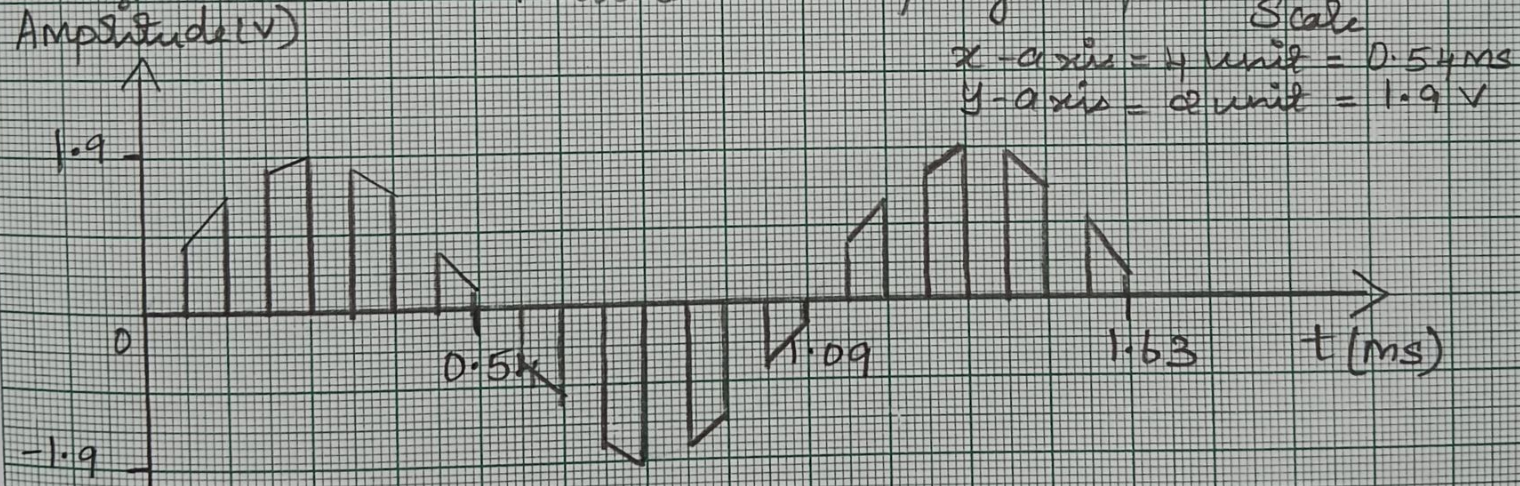
Clock Signal

Scale
x-axis = 16.28 μs
y-axis = 2 unit = 4.6 V



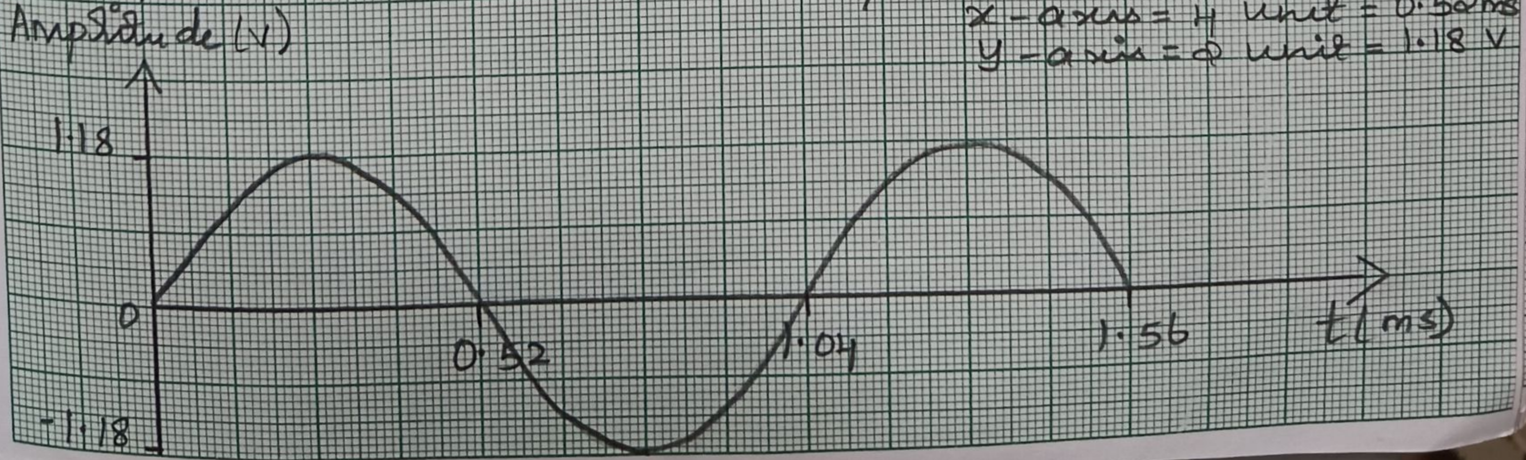
Natural Sampling output

Scale
x-axis = 4 unit = 0.54 ms
y-axis = 2 unit = 1.9 V



Filter output

Scale
x-axis = 4 unit = 0.52 ms
y-axis = 2 unit = 1.18 V



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Page No. ______

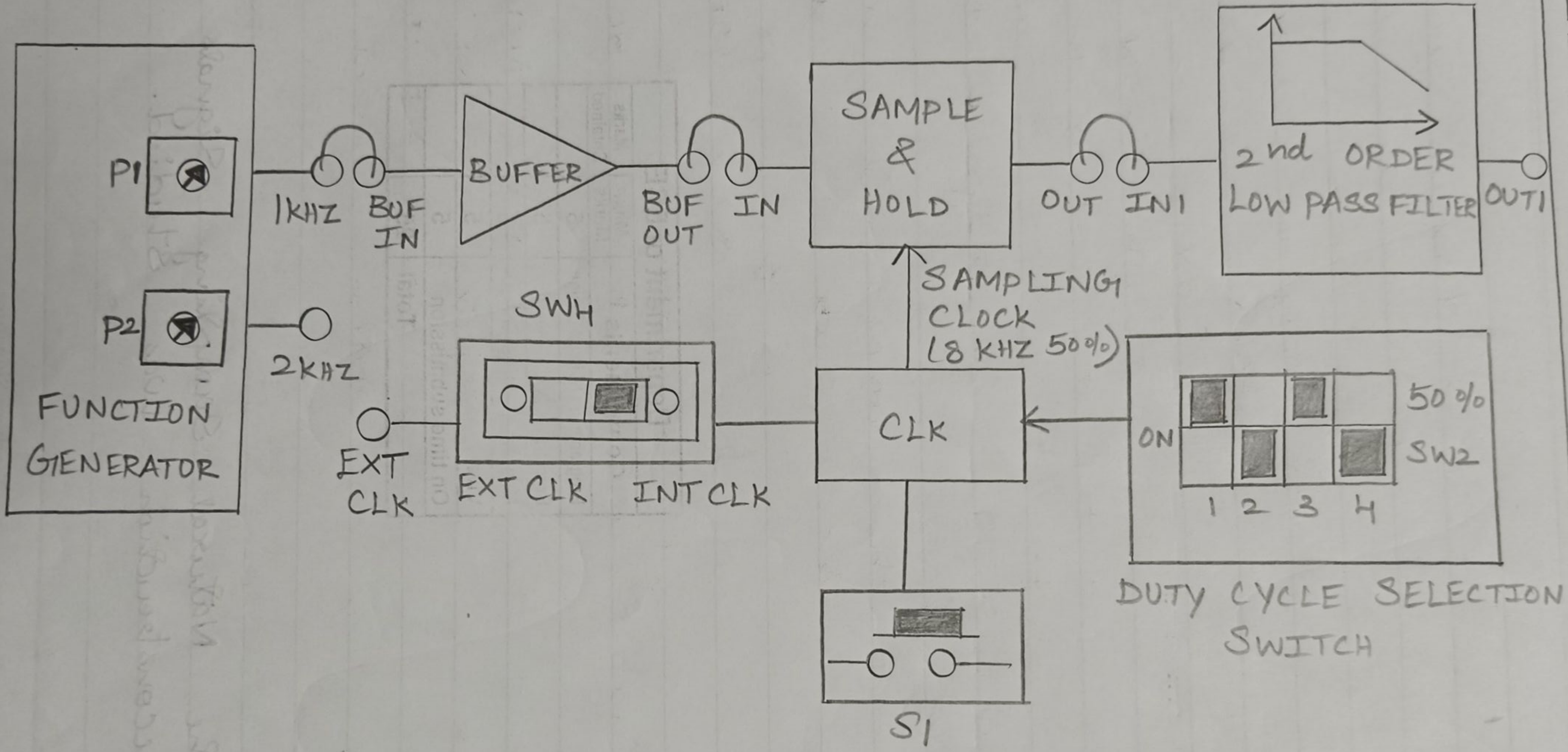
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

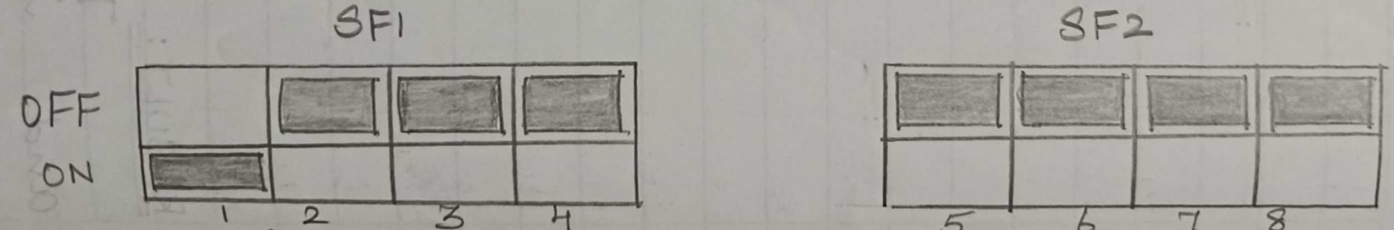
Thus the Natural Sampling Signals and its reconstruction was Studied.

Teacher's Signature ______

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR SAMPLE & HOLD



SWITCH FAULTS SELECTION SWITCH

Expt. No. 2) B)

Date

Page No.

SAMPLE AND HOLD

AIM:

TO Study the Sample and hold Signals and its reconstruction.

COMPONENTS REQUIRED:

1. Experimentor kit DCL-01
2. Connecting Chords
3. Power Supply
4. 20MHZ Dual Trace Oscilloscope

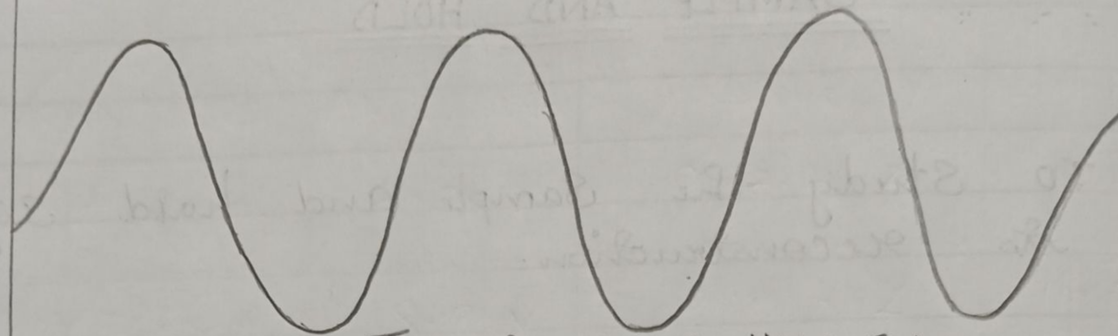
THEORY:

Sampling is the process of converting a Signal (for example, a function of Continuous time or Space) into a numeric Sequence (a function of discrete time or Space). The purpose of this circuit is to hold the analog value Steady for a short time while the Converter or other following System performs Some Operation that takes a Little time. The Nyquist rate is the minimum sampling rate required to avoid aliasing, at least equal to twice the highest frequency contained within the Signal.

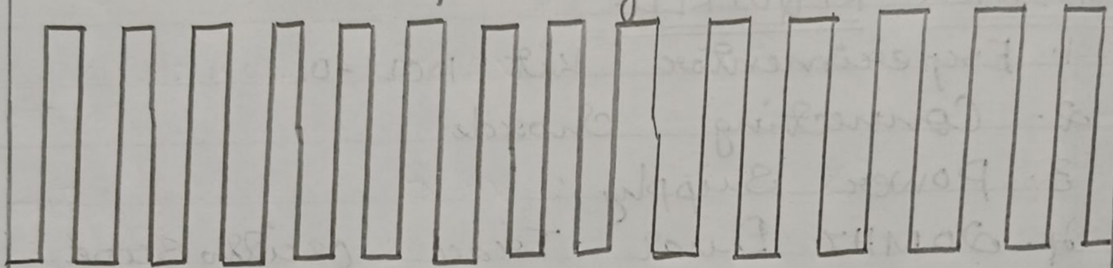
$$f \geq 2f_m$$

Teacher's Signature

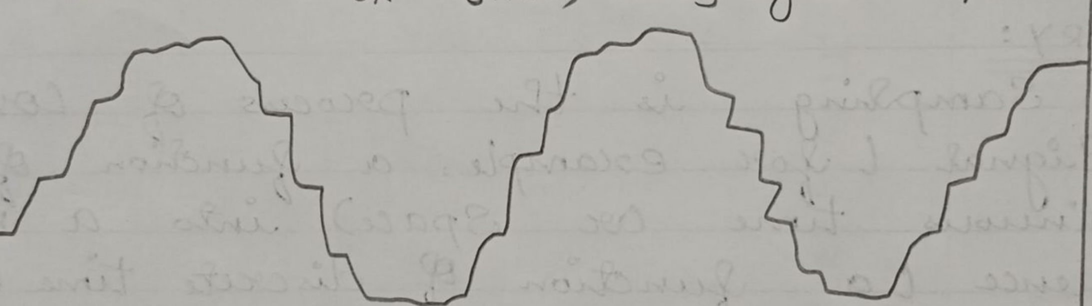
MODEL GRAPH:



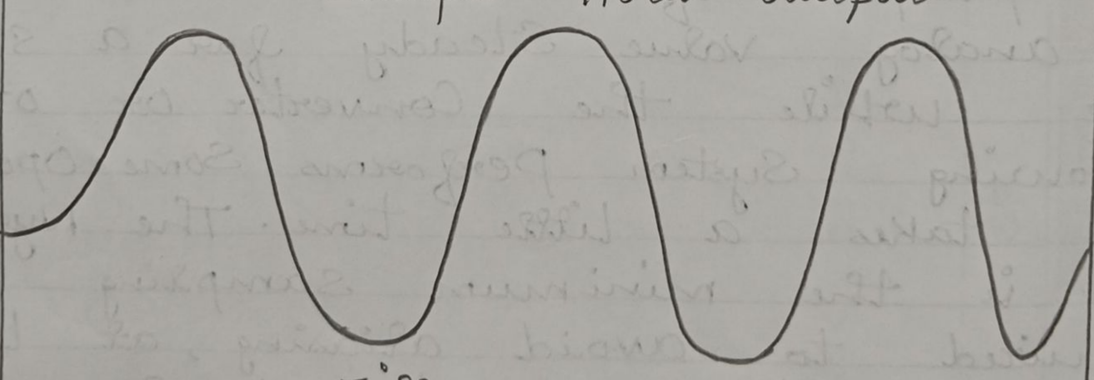
Input Signal 1KHZ, 5VPP



Clock 8KHZ, Duty cycle 50%



Sample Hold Output



Filter Output OUT1

Waveforms Sample Hold

Expt. No. ____________ Date ____________

Page No. ____________

PROCEDURE:

1. Refer to the Block Diagram carry out the following connections and switch settings.

2. Connect power supply in proper polarity to the kit DCL-01 & Switch it on.

3. Connect the 1KHZ, 5VPP Sine wave Signal, generated onboard, to the BUF IN post of the BUFFER and the BUF OUT post of the BUFFER to the IN post of the Sample and hold block by means of the connecting chords provided.

4. Connect the sampling frequency clock in the internal mode INT CLK using switch (SW4).

5. Using clock selector switch select 8 KHZ sampling frequency.

6. Using Switch SW2 select 50% duty cycle.

7. Connect the OUT post of the Sample and Hold block to the input IN1 post of the 2nd order Low pass Butterworth Filter and take necessary Observation as mentioned below.

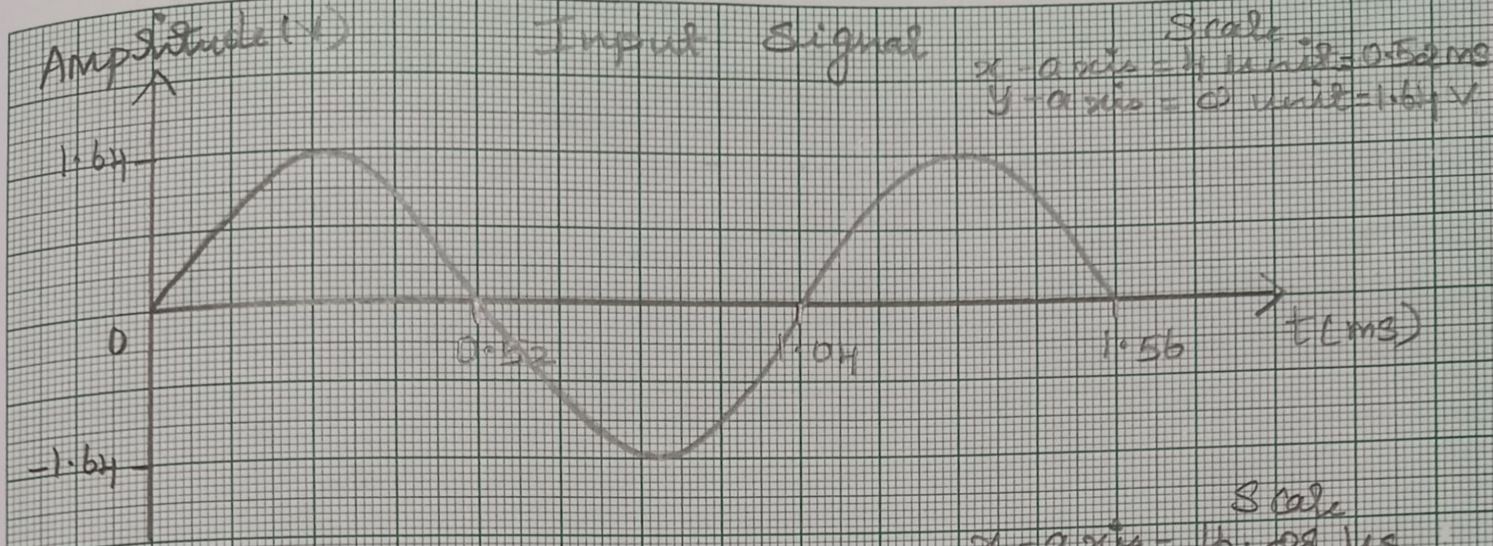
8. Repeat the procedure for the 2 KHZ Sine Wave Signal as input.

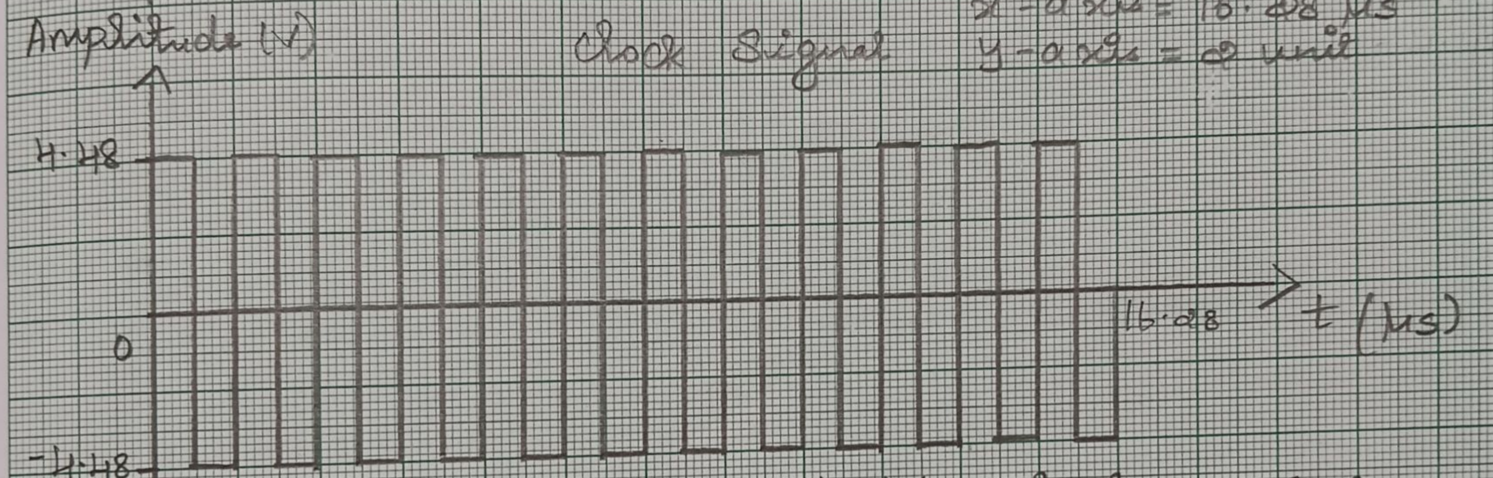
Teacher's Signature ____________

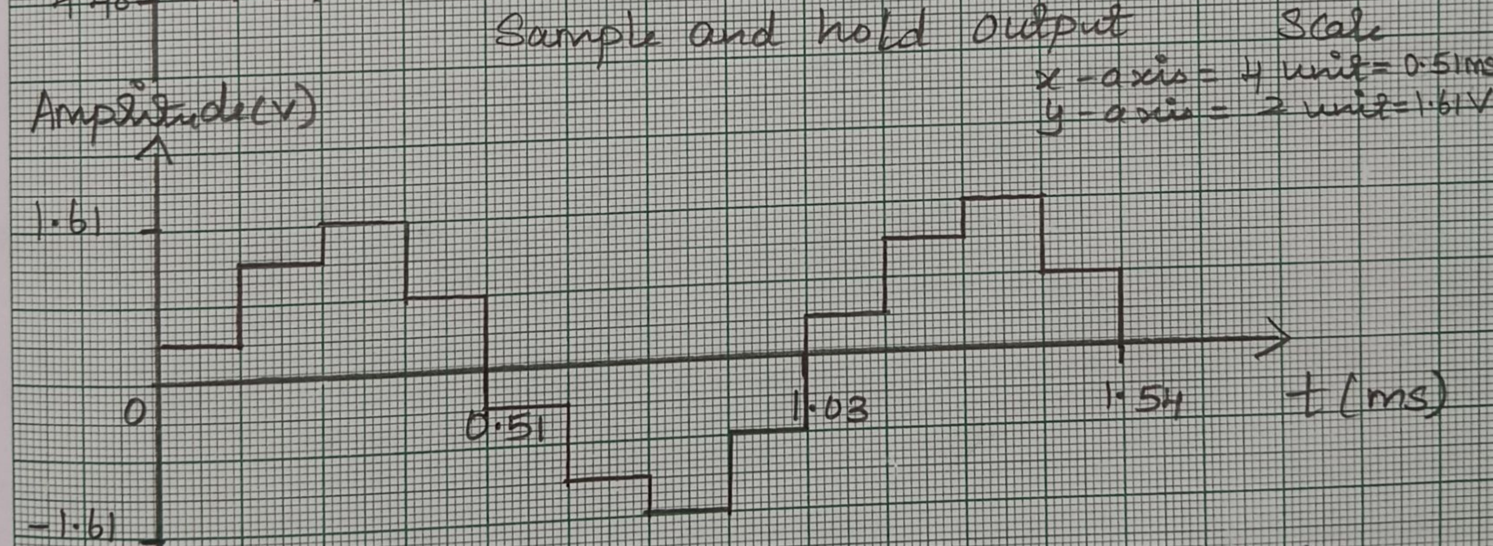
TABULATION:

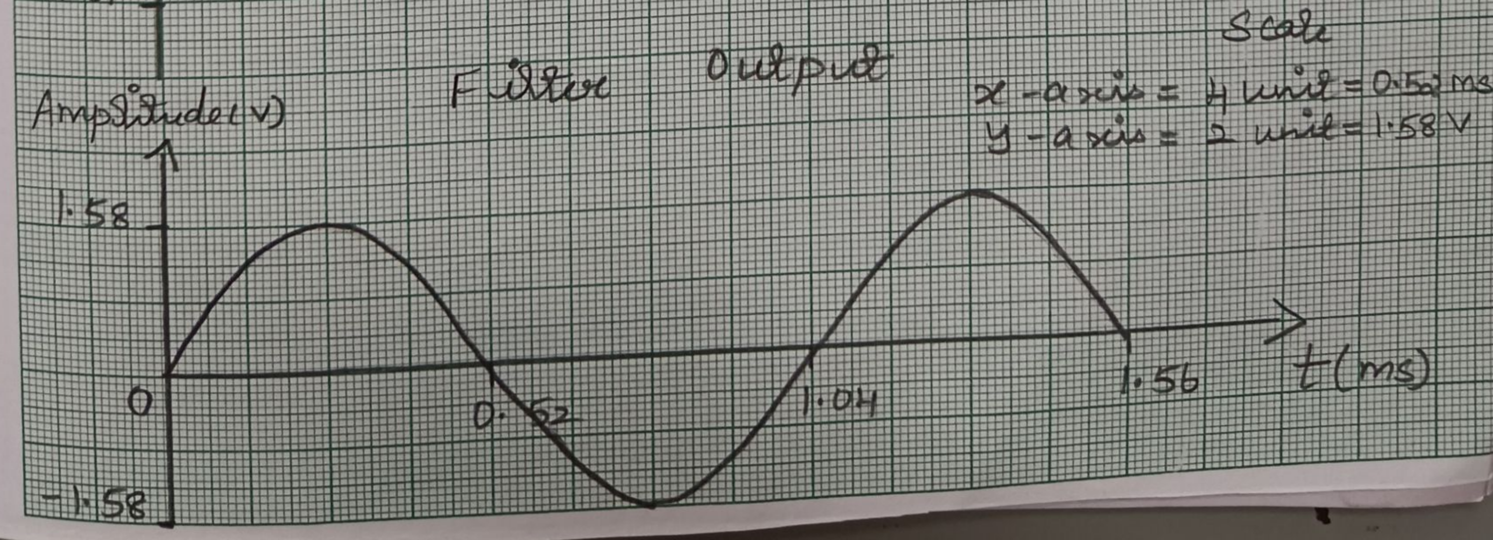
S.NO	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input Signal	3.28 V	953.4 HZ	1.04 ms
2.	Clock Signal	8.96 V	61.41 KHZ	16.28 μs
3.	Sample and hold Output	3.22 V	963.7 HZ	1.03 ms
4.	Filter output	3.16 V	960 HZ	1.04 ms

Sample and Hold









Expt. No. ______ Date ______

Page No. ______

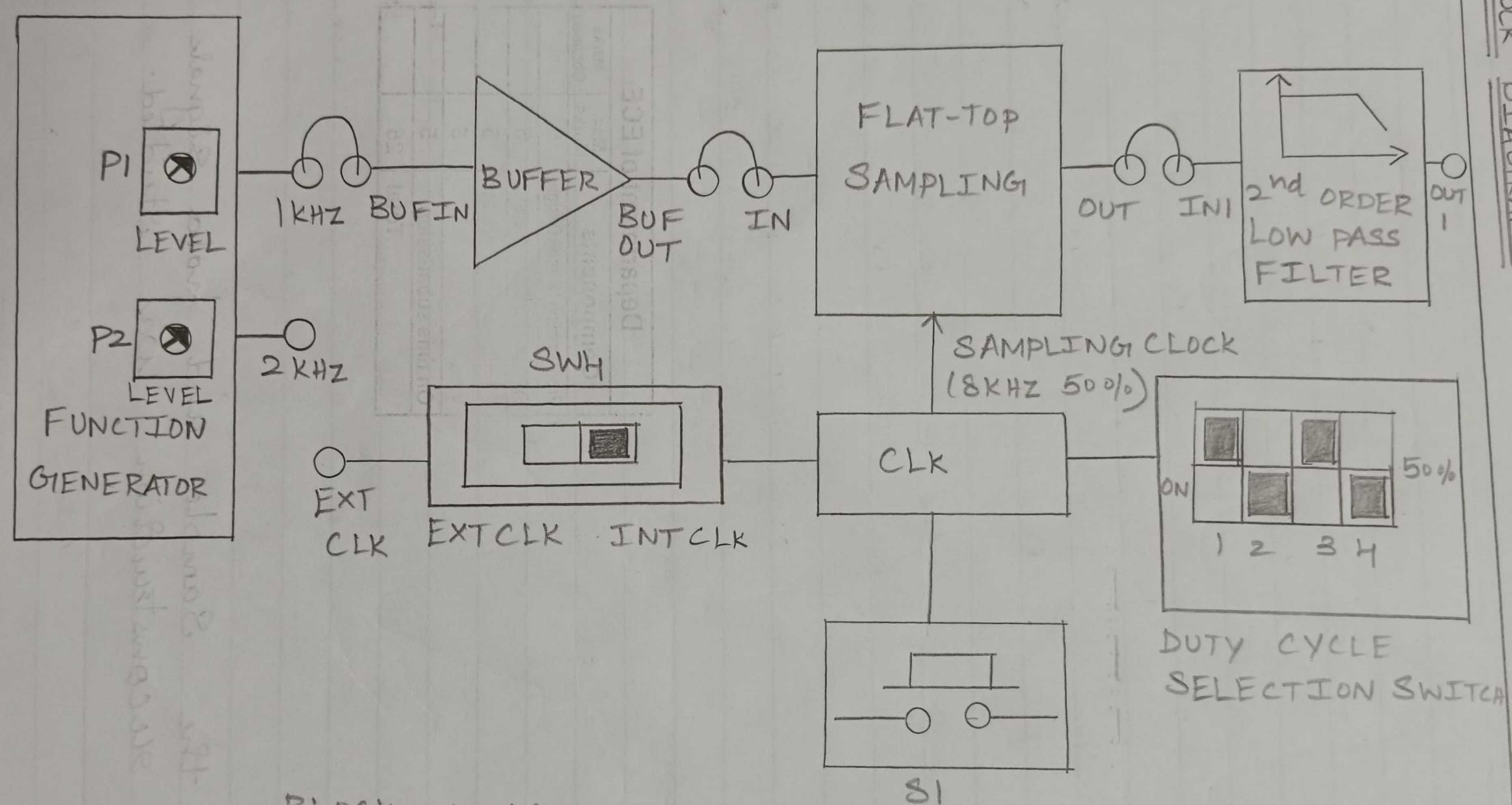
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

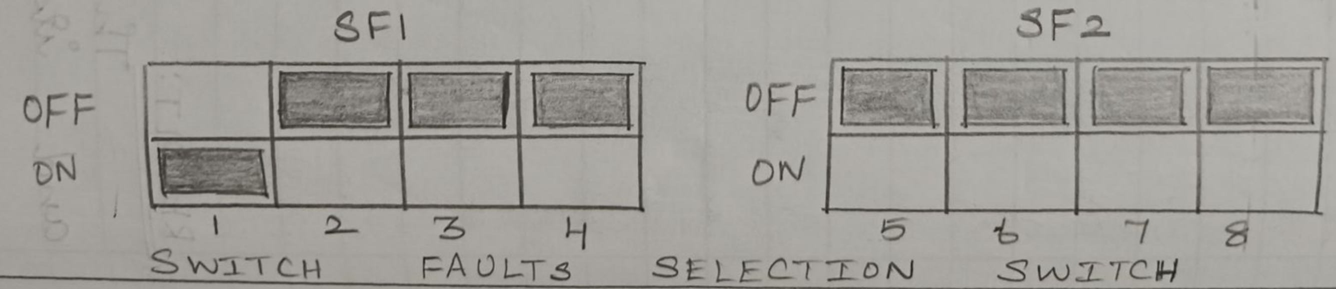
Thus the Sample and hold signals and its reconstruction was Studied.

Teacher's Signature ______

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR FLAT-TOP SAMPLING



Expt. No. 2) c)

Date

Page No.

FLAT - TOP

AIM:

TO study the Flat-TOP Sampling Signals and its reconstruction

COMPONENTS REQUIRED:

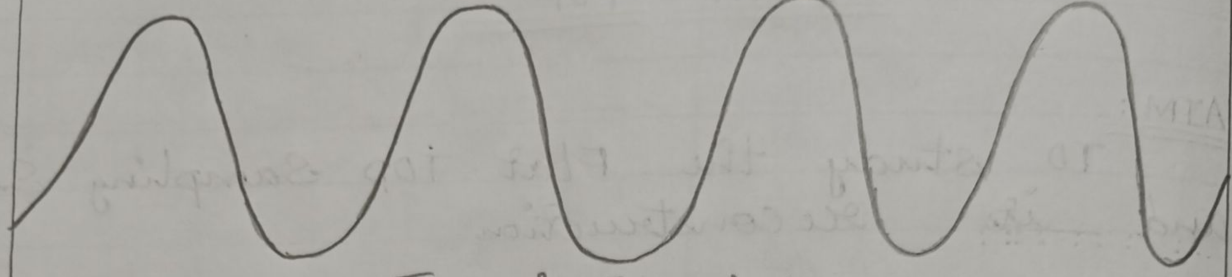
1. Experimentor Kit DCL - 01
2. Connecting Chords
3. Power Supply
4. 20MHZ Dual Trace oscilloscope

THEORY:

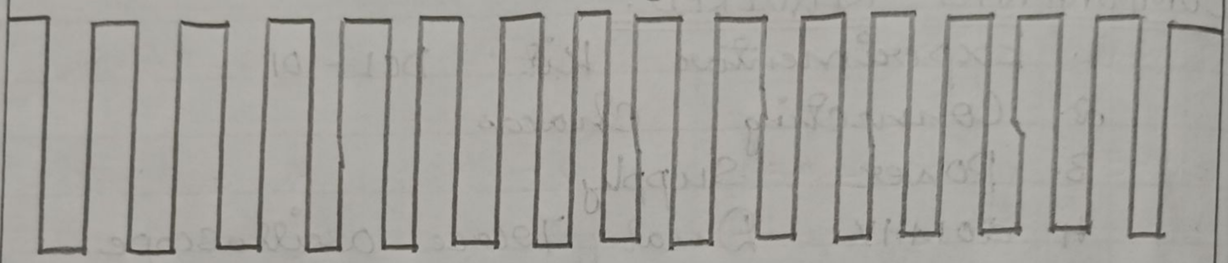
Sampling is the process of converting a signal (for example, a function of continuous time or space) into a numeric sequence (a function of discrete time or space). The purpose of this circuit is to hold the analog value steady for a short time while the converter or other following system performs some operation that takes a little time. Here, capacitor is used to store the analog voltage and an electronic switch or gate is used to alternately connect and disconnect the capacitor from the analog input. The Nyquist rate is the minimum sampling rate required to avoid aliasing, at least equal to twice the highest frequency contained within the signal.

Teacher's Signature

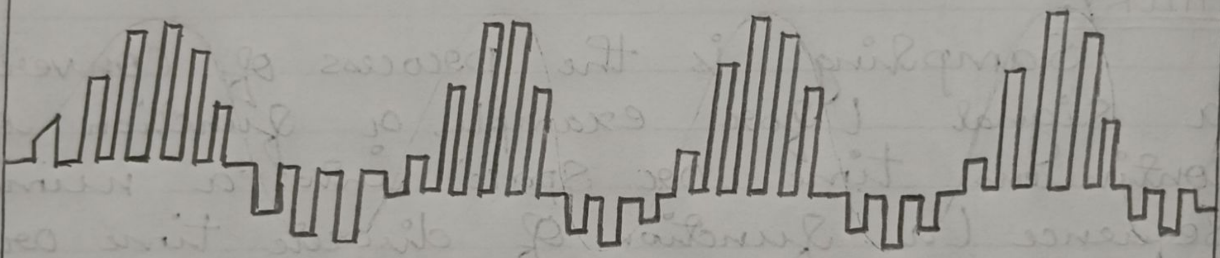
MODEL GRAPH:



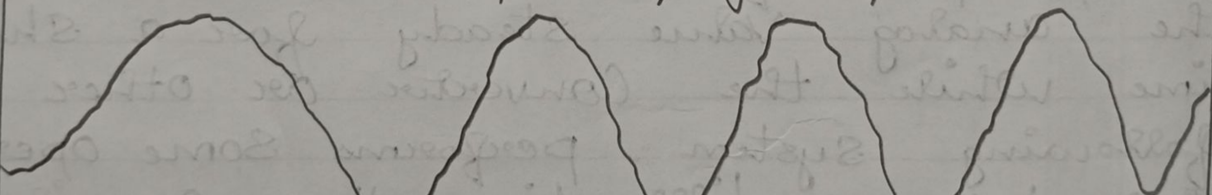
Input Signal 1KHZ, 5VPP



Clock 8KHZ, Duty cycle 50%



Flat-Top Sampling Output



Filter Output OUT 1

Waveform FLAT-TOP Sampling

Date

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$$f \geq 2f_m$$

where is the highest frequency at which the signal can have non zero energy.

PROCEDURE:

1. Refer to the Block Diagram carry out the following connections and switch settings.

2. Connect power supply in proper polarity to the kit DCL-018 switch it on.

3. Connect the 1KHZ, 5Vpp Sine Wave signal, generated onboard to the BUF IN post of the Buffer and the BUF OUT post of the Buffer to the IN post of the Flat Top Sampling block by means of the connecting chords provided.

4. Connect the sampling frequency clock in the internal mode INT CLK using switch (SW4).

5. Using clock selector switch S1 select 8KHZ sampling frequency.

6. Using switch SW2 select 50% duty cycle.

7. Connect the OUT post of the Flat top sampling block to the input IN1 of the 2nd Order Low pass Butterworth Filter and take necessary observation as mentioned below.

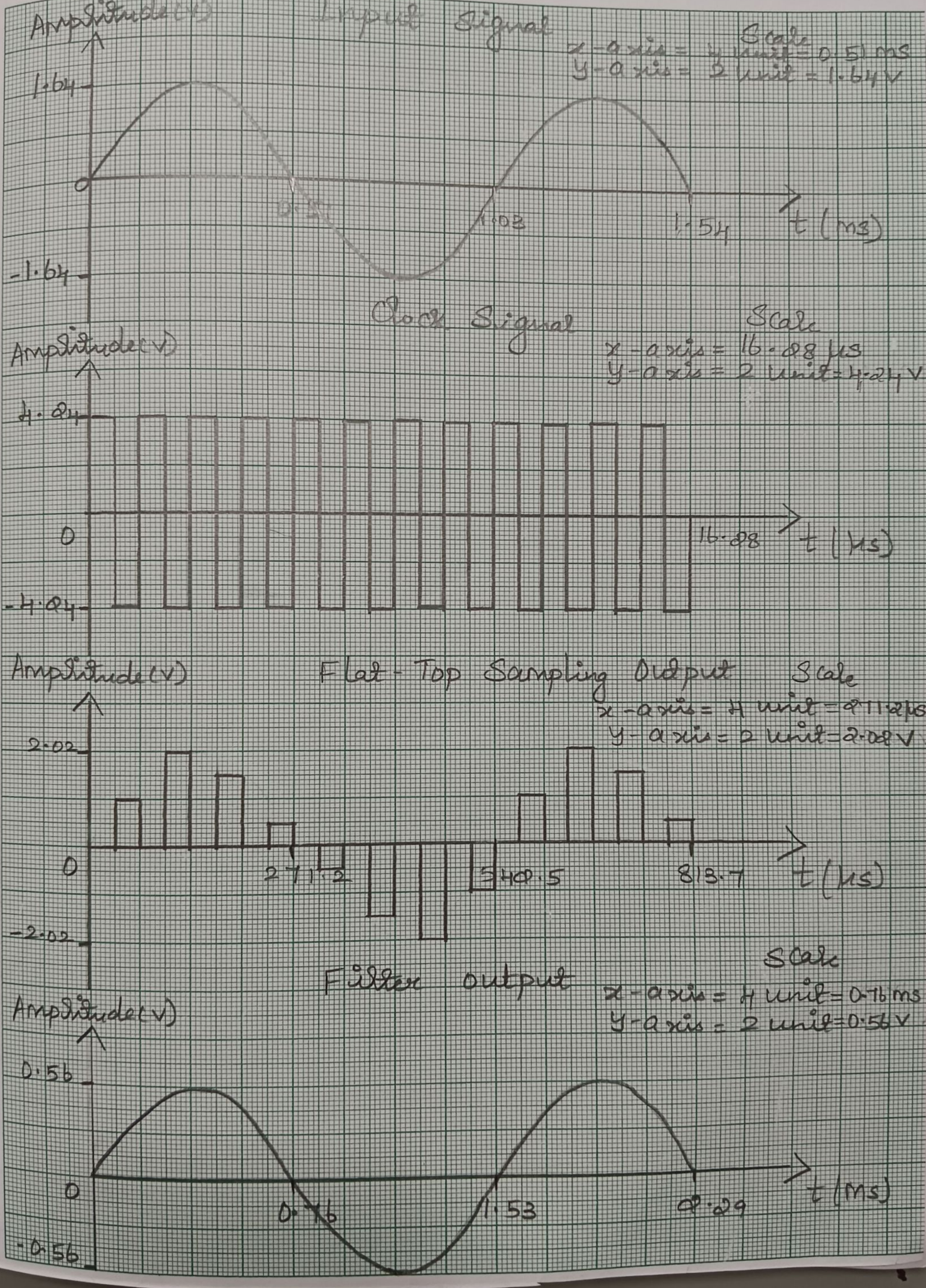
8. Repeat the procedure for the 2KHZ Sine Wave signal as input.

Teacher's Signature

TABULATION:

S.NO	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input Signal	3.28V	964 HZ	1.03 ms
2.	Clock Signal	8.48 V	61.41 KHZ	16.28 μs
3.	Flat-Top Sampling Output	4.04 V	1.843 KHZ	542.5 μs
4.	Filter Output	1.12 V	652.3 HZ	1.53 ms

Flat-TOP Sampling



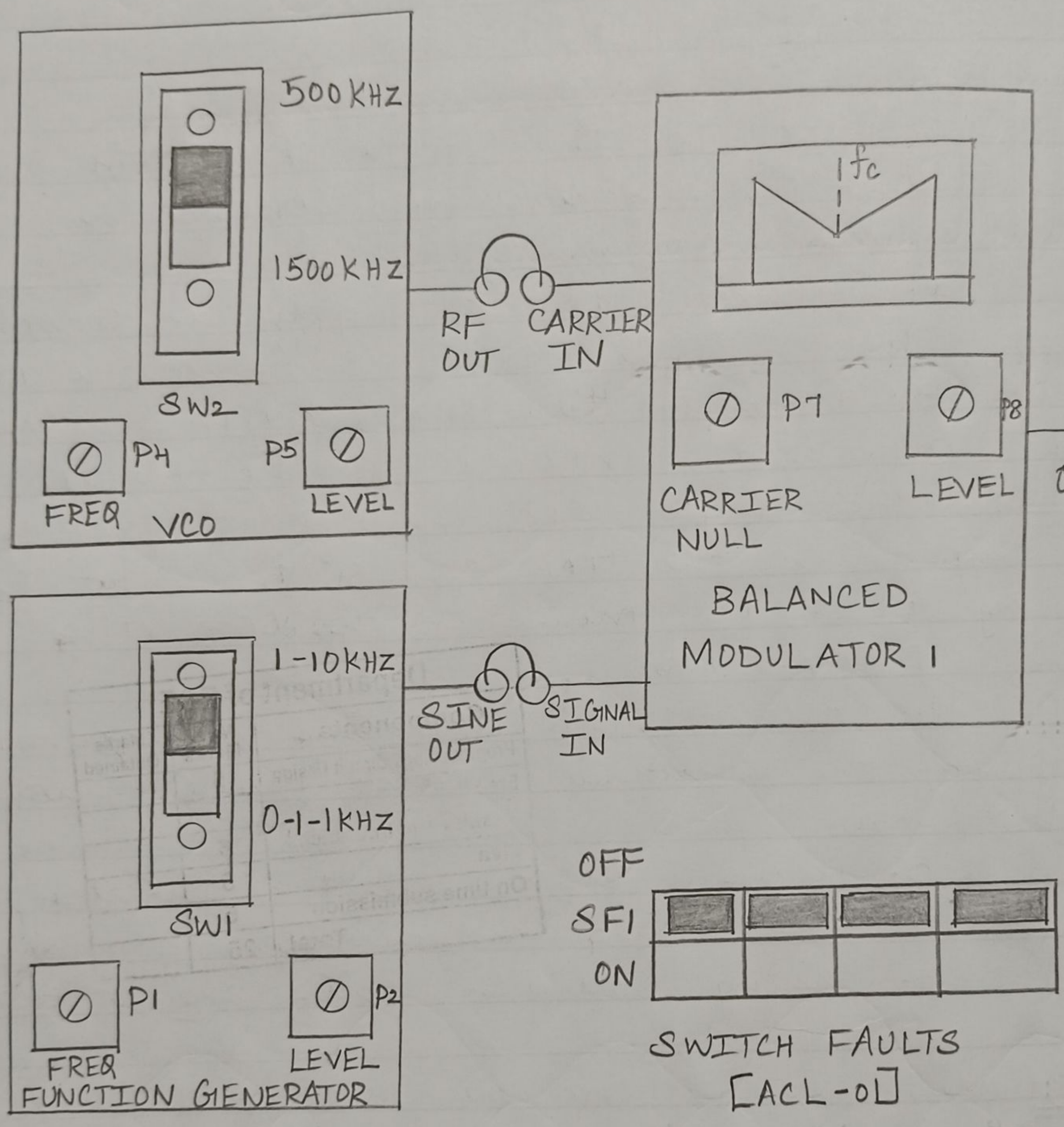
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

Thus the Flat-TOP Sampling Signals and its reconstruction was studied.

Teacher's Signature

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR STUDY OF DSB AM GENERATION

Expt. No. 3

Date

Page No.

AMPLITUDE MODULATION AND DEMODULATION

AIM:

TO conduct an experiment to generate an AM Signal using Collector modulation for an fc = KHZ and fm = HZ. plot the Variation of modulating Signal amplitude v/s modulation index.

COMPONENTS REQUIRED:

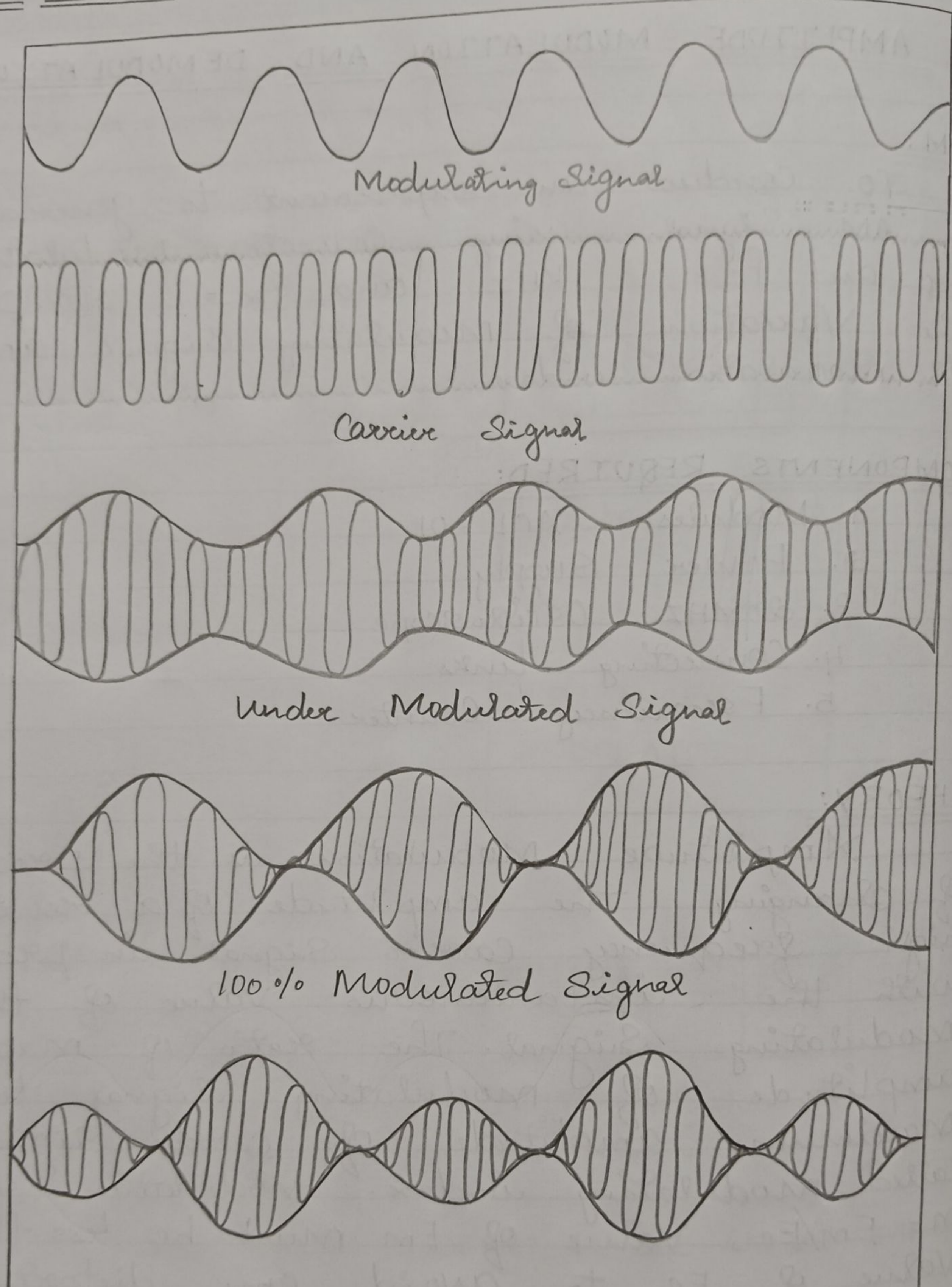
1. Modules ACL -01
2. Power Supply
3. 20MHZ Oscilloscope
4. Connecting links
5. Frequency Counter

THEORY:

Amplitude Modulation is the process of changing the amplitude of a relatively high frequency carrier Signal in proportion with the instantaneous Value of the modulating Signal. The ratio of maximum amplitude of modulating Signal to maximum amplitude of carrier Signal is called modulating index. Modulation index, $m = Em/Ec$, Value of Em must be less than Value of Ec to avoid any distortion in the modulated Signal. AM demodulation is the reverse process of AM modulation.

Teacher's Signature

MODEL GRAPH:


Modulating Signal
Carrier Signal
Under Modulated Signal
100% Modulated Signal

It is the process of Separating message signal from the modulated carrier Signal.

PROCEDURE:

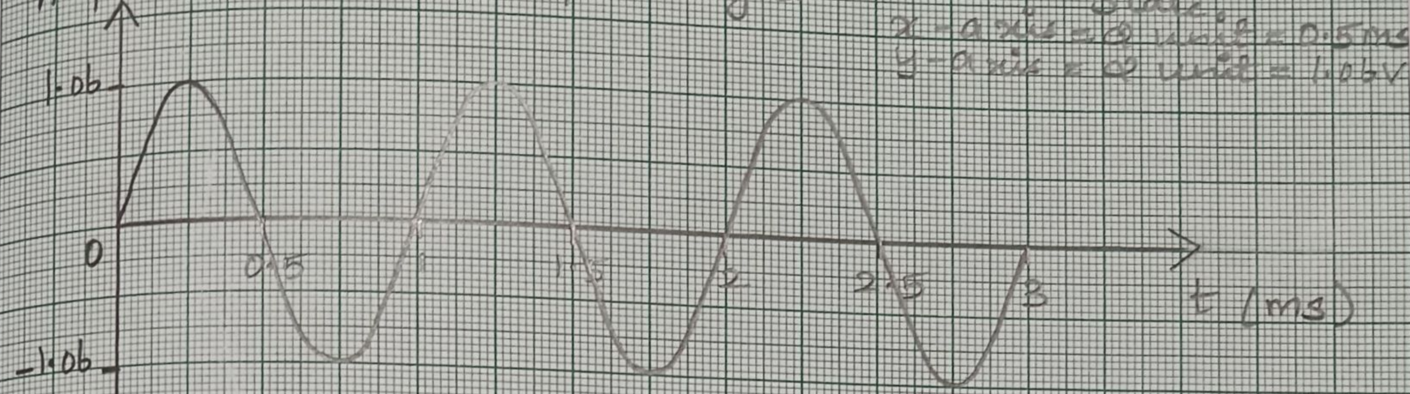
1. Refer to the fig & carry out the following connections.
2. Connect o/p of VCO (ACL-01) RF OUT post to the input of Balance modulator 1 CARRIER IN post (ACL-01).
3. Connect the power supply with proper polarity to the kit ACL-01 & ACL-02, while connecting this; ensure that the power supply is OFF.
4. Switch on the power supply and carry out the following presetting:
FUNCTION GENERATOR: LEVEL about 0.5VPP; FREQ about 1KHZ.
* VCO: LEVEL about 1VPP; FREQ about 450KHZ, switch on 500KHZ.
* BALANCED MODULATOR 1: CARRIER NULL completely rotated
* clockwise or counter clockwise, so as to "unbalance" the modulator and to obtain an AM signal with the not suppressed carrier across the output; OUT LEVEL in fully clockwise.
5. Connect the oscilloscope to the inputs of the modulator post (SIG and CAR) and detect the modulating signal and

TABULATION:

S.NO	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input Signal	2.12 V	991.72 HZ	1 ms
2.	Carrier Signal	2.14 V	11 KHZ	90.9 μs
3.	Under Modulated Signal	2.12 V	11 KHZ	90.9 μs

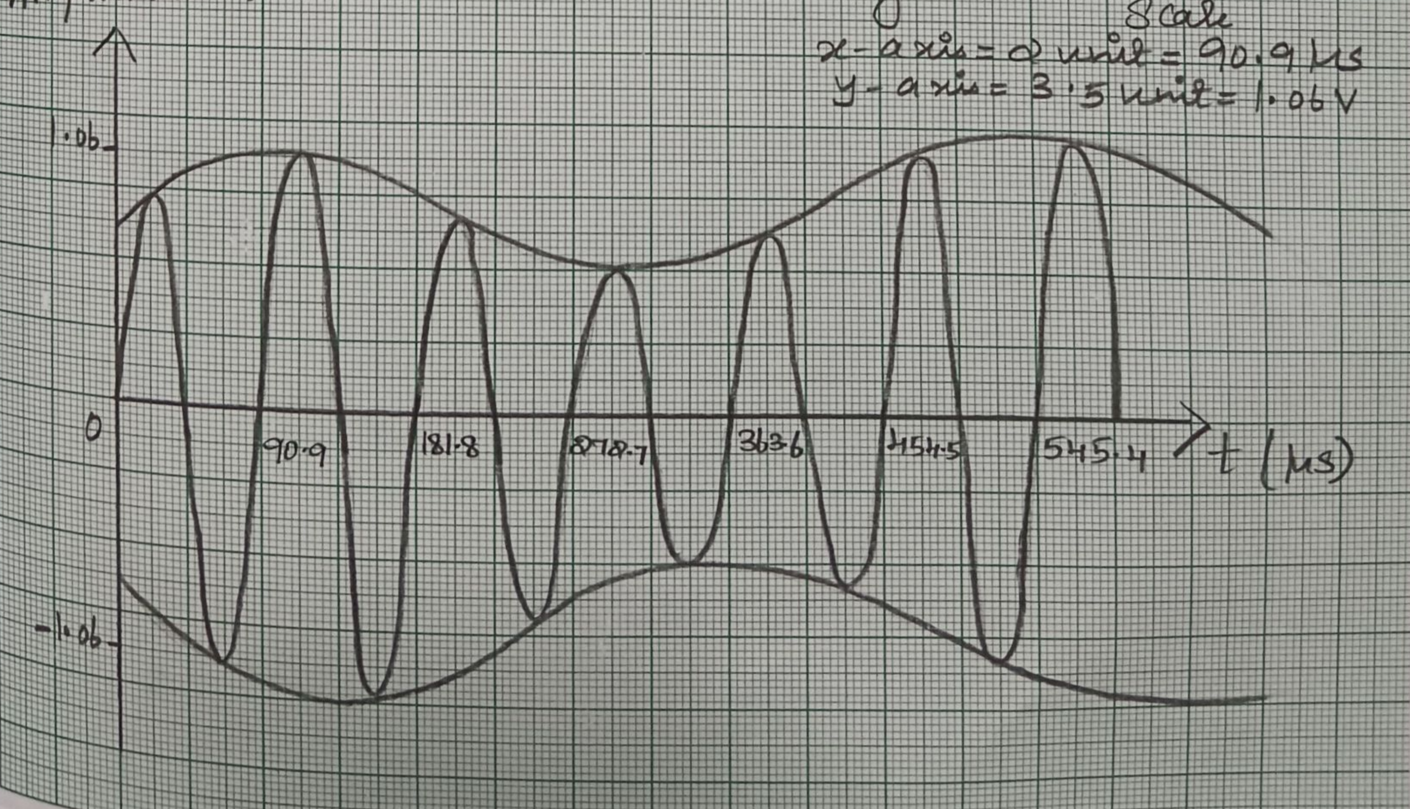
Amplitude Modulation

Input Signal



Carrier Signal

Under Modulated Signal



the Carrier Signal

6. Move the probe from post SIG to post OUT (output of the modulator), where Signal Modulated in amplitude is detected. Note that the modulated Signal envelope Corresponds to the Wave form of the DSB AM modulating Signal.

7. Vary the amplitude of the modulating Signal and Check the 3 following conditions: Modulation percentage lower than the 100 %, equal to the 100 %, superior to 100 %.

8. Vary the frequency and amplitude of the modulating Signal, and Check the Corresponding Variations of the modulated Signal.

9. Vary the amplitude of the modulating Signal and note that the modulated signal can result Saturation or over modulation.

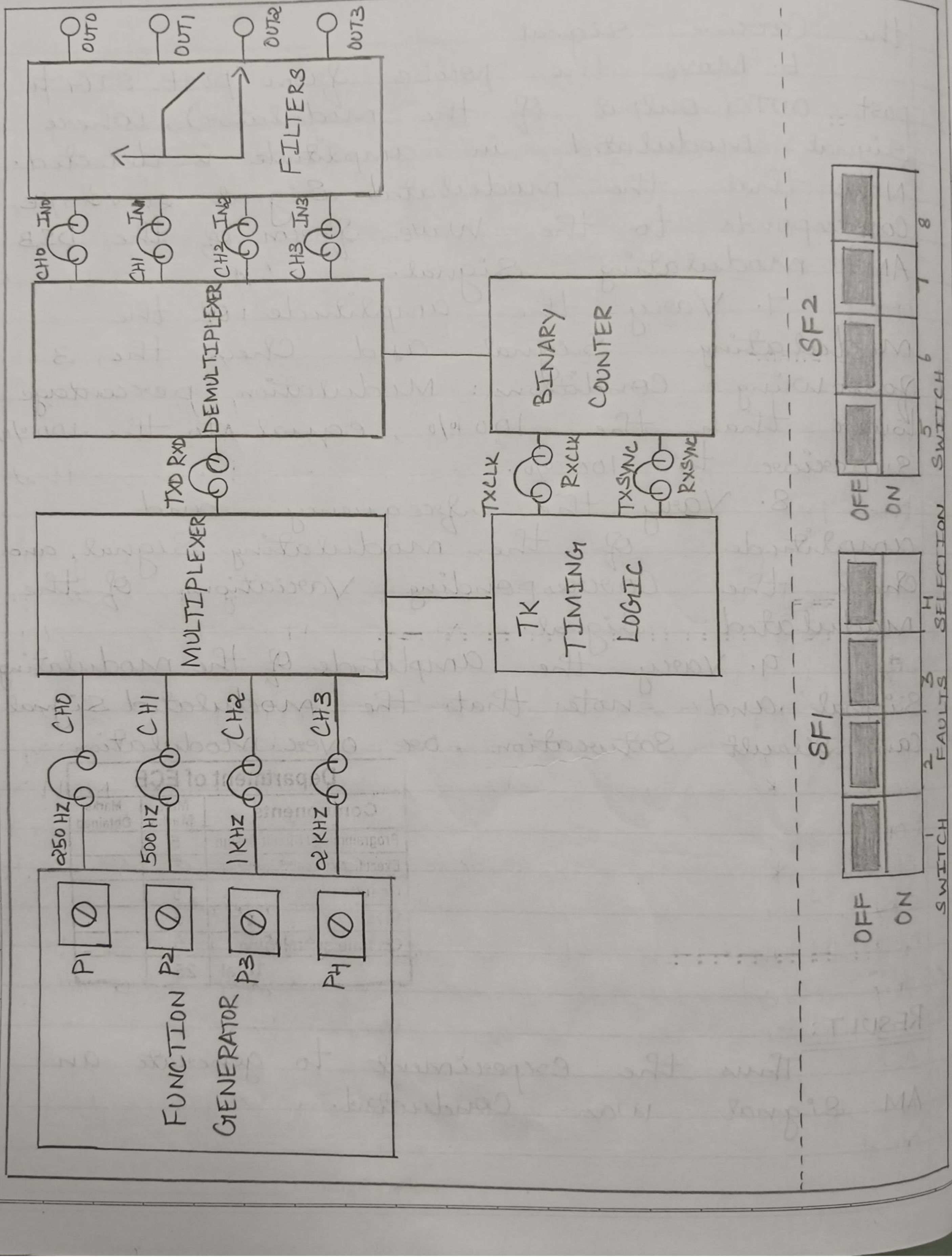
Department of ECE

Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

Thus the experiment to generate an AM Signal was Conducted.

BLOCK DIAGRAM:



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AIM:

Conduct an experiment to generate TDM Signal and also design a circuit to demodulate the obtained TDM Signal and Verify Sampling theorem.

COMPONENTS REQUIRED:

1. Experimentor Kit DCL-02
2. Connecting Chords
3. Power Supply
4. 20 MHZ Dual Trace Oscilloscope.

THEORY:

ONBOARD FUNCTION GENERATOR:

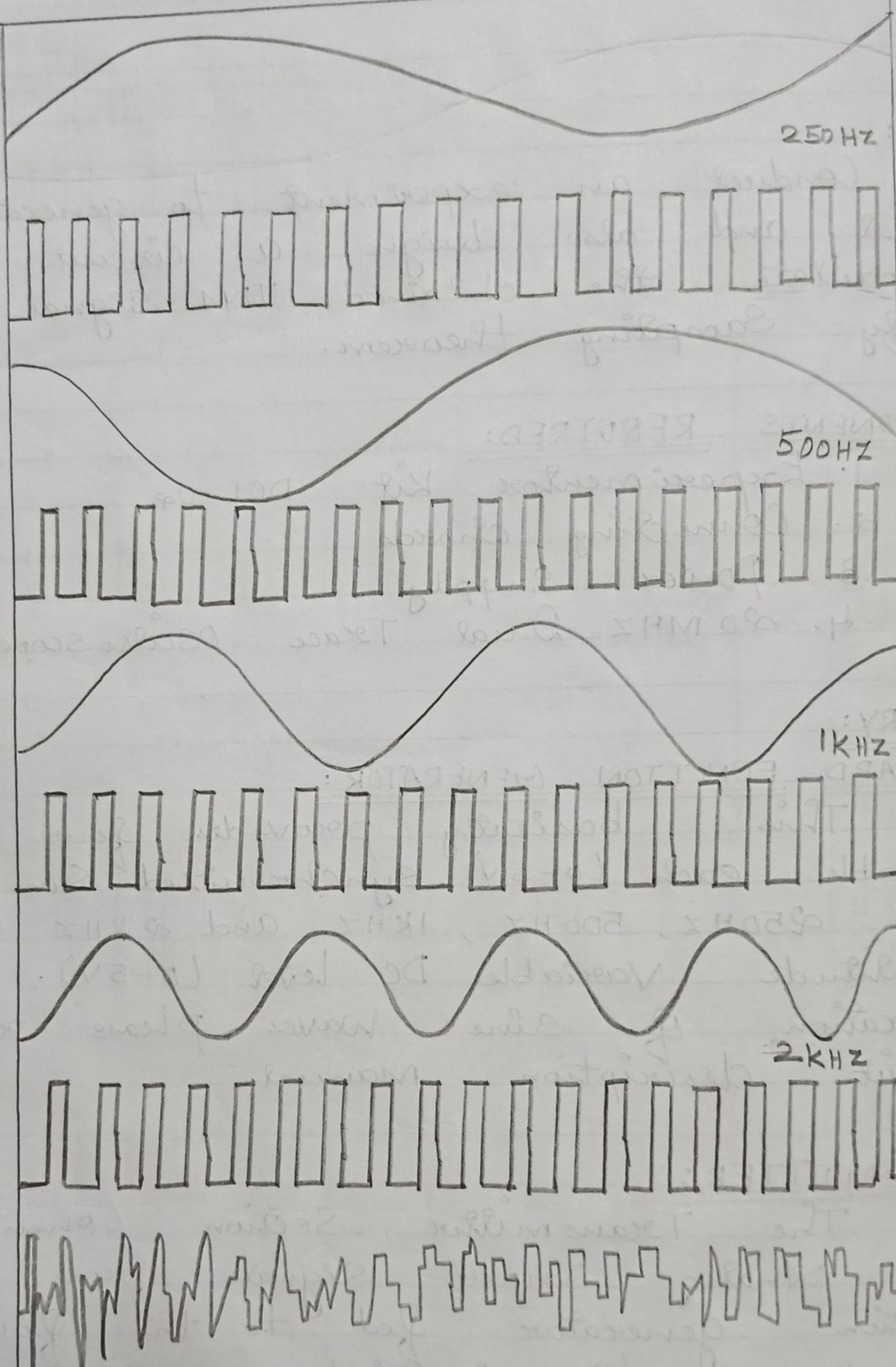
This basically provides four Amplitude Variable each (0-5V) synchronized Sine Waves, each 250 HZ, 500 HZ, 1KHZ and 2KHZ and an amplitude Variable DC level (0-5V). For the generation of Sine Waves please refer to circuit description Manual.

TRANSMITTER:

The Transmitter Section Consists of four Analog Input Signals from the Function generator fed to the four Channels of the Multiplexer where the Signals fed are Time Division Multiplexed

Teacher's Signature

MODEL GRAPH:



WAVEFORM TDM TRANSMITTER

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Date
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after undergoing the sampling. The sampling process makes the signals pulse Amplitude Modulated. The frequencies for sampling are given from the decoder.

RECEIVER:

The Receiver Section Consists of a Demultiplexer that demultiplexes the four Time Division Multiplexed Signals, which it receives from the transmitter. This Demultiplexed Signals are then fed to the reconstruction circuit, which is the filter section.

The Receiver timing logic is very Similar to the transmitter timing logic. This demultiplexer based on the control Signals C0, C1, C2, C3 assigns the information to the corresponding Channels.

PROCEDURE:

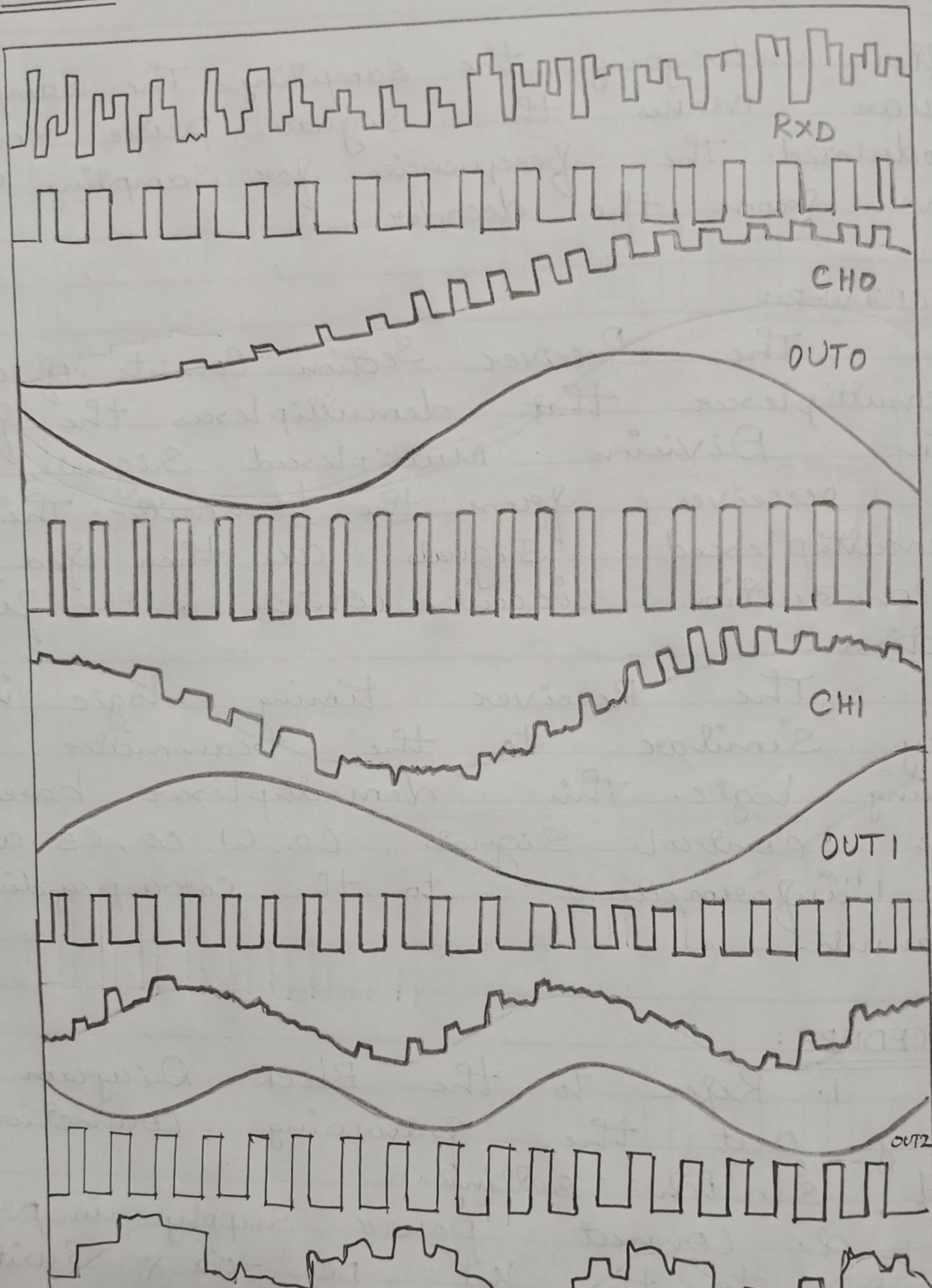
1. Refer to the Block Diagram & Carry out the following Connections and Switch settings.

2. Connect power supply in proper polarity to the kit DCL-02 & Switch it on.

3. Connect 250HZ, 500HZ, 1KHZ and 2KHZ Sine Wave Signal from the

Teacher's Signature

MODEL GRAPH:



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Function Generator to the multiplexer input channel CH0, CH1, CH2, CH3 by means of the connecting chords provided.

4. Connect the multiplexer output TXD of the transmitter section to the demultiplexer input RXD of the receiver section.

5. Connect the output of the receiver section CH0, CH1, CH2, CH3 to the IN0, IN1, IN2, IN3 of the filter section.

6. Connect the sampling clock TX CLK and channel Identification clock TXSYNC of the transmitter section to the corresponding RX CLK and RX SYNC of the receiver section respectively.

7. Set the amplitude of the input sine wave as desired.

8. Take observations as mentioned below.

Teacher's Signature ____________

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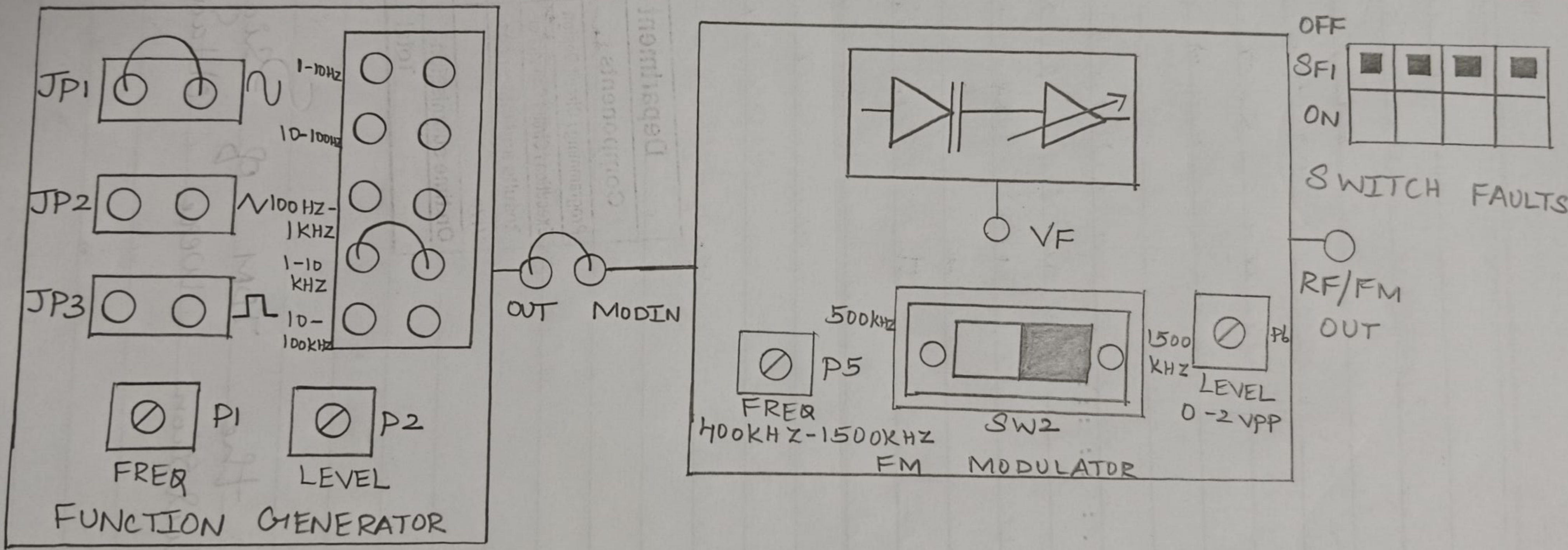
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

Thus the TDM of Signals and its demodulation were obtained and Studied.

Teacher's Signature ______

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR STUDY OF VARACTOR MODULATOR

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Page No.

FREQUENCY MODULATION AND DEMODULATION

AIM:

Conduct a Suitable experiment to generate an FM Wave. Display the various Waveforms.

COMPONENTS REQUIRED:

1. Experimentor kit ACL - 03
2. Connecting Chords
3. Power Supply
4. 20MHZ Dual Trace oscilloscope.

THEORY:

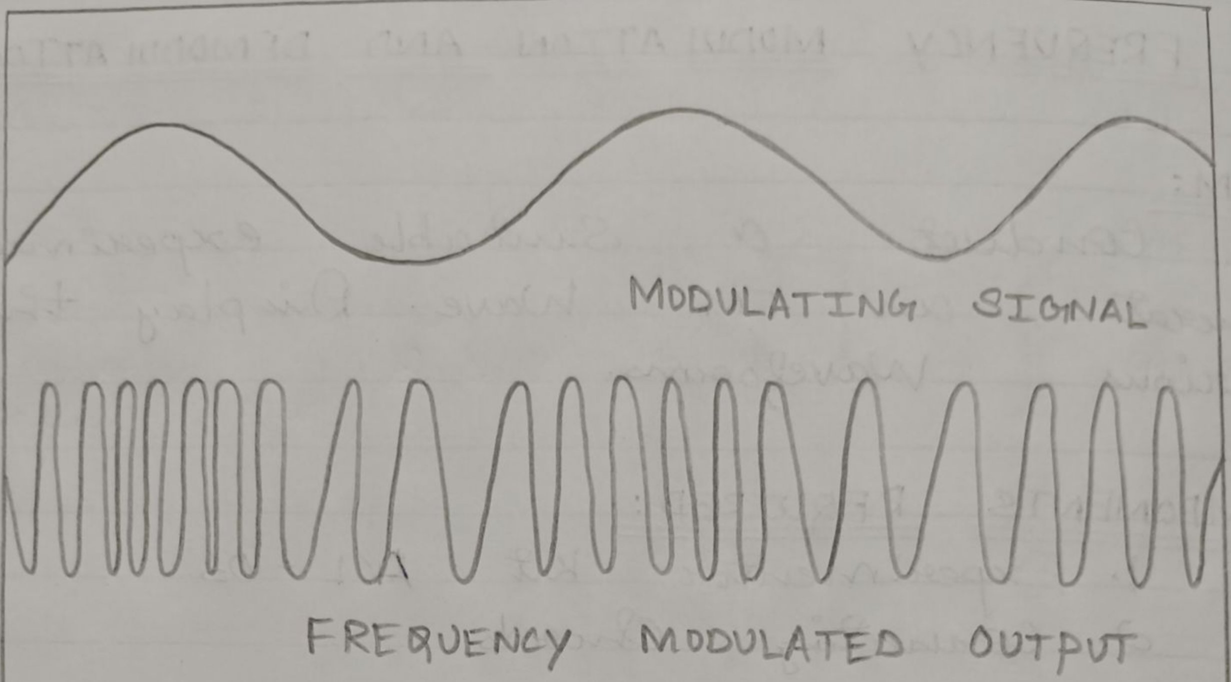
Frequency modulation is defined as change in frequency of carrier signal with respect to change in amplitude of modulating signal. The maximum frequency deviation is produced during positive half cycle of the message signal. Similarly minimum deviation is produced during negative half cycle of message signal.

PROCEDURE:

1. Refer to the figure & carry out the following connections.
2. Connect the power supply with proper polarity to the kit

Teacher's Signature

MODEL GRAPH:



FREQUENCY MODULATION

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ACL-03 While Connecting this; ensure that the power Supply is OFF.

3. Connect the output of function generator OUT post to the modulation IN of Frequency Modulator MOD IN post.

4. Switch ON the power Supply and carry out the following presetting:

* FUNCTION GENERATOR: Sine Wave (JP1); LEVEL about 100mV; FREQ about 1KHZ.

* FREQUENCY MODULATOR LEVEL about 2VPP; FREQ On the center; Switch On 1500KHZ.

5. Connect the oscilloscope to the Output of the modulator FM/RF OUT. You obtain a waveform Similar to the One of Figure.

6. The frequency deviation ΔF can be Calculated as follows:

* From the oscilloscope evaluate FM and Fm, detecting the periods of the respective Sine Waves.

* The frequency deviation ΔF is defined as: $\Delta F = (FM - Fm)/2$.

7. The Value of the modulation index Mf is calculated by the relation.

$Mf = \Delta F/f$, Where f is the frequency of the modulating Signal.

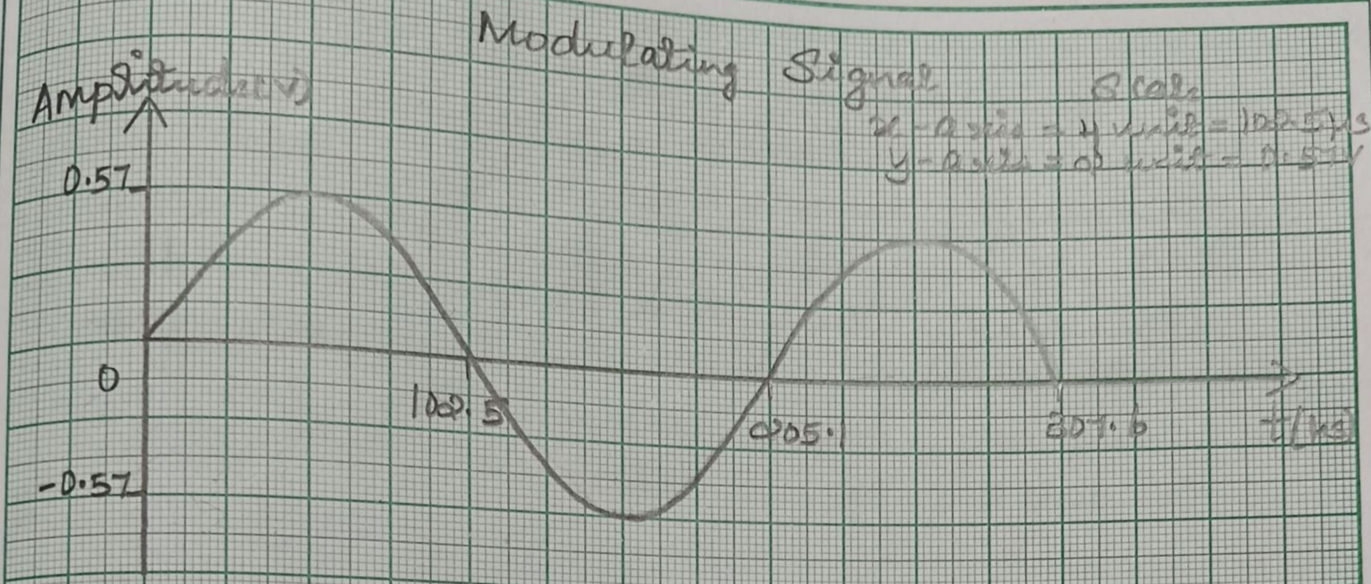
8. Then Observe the FM Signal as shown in Figure.

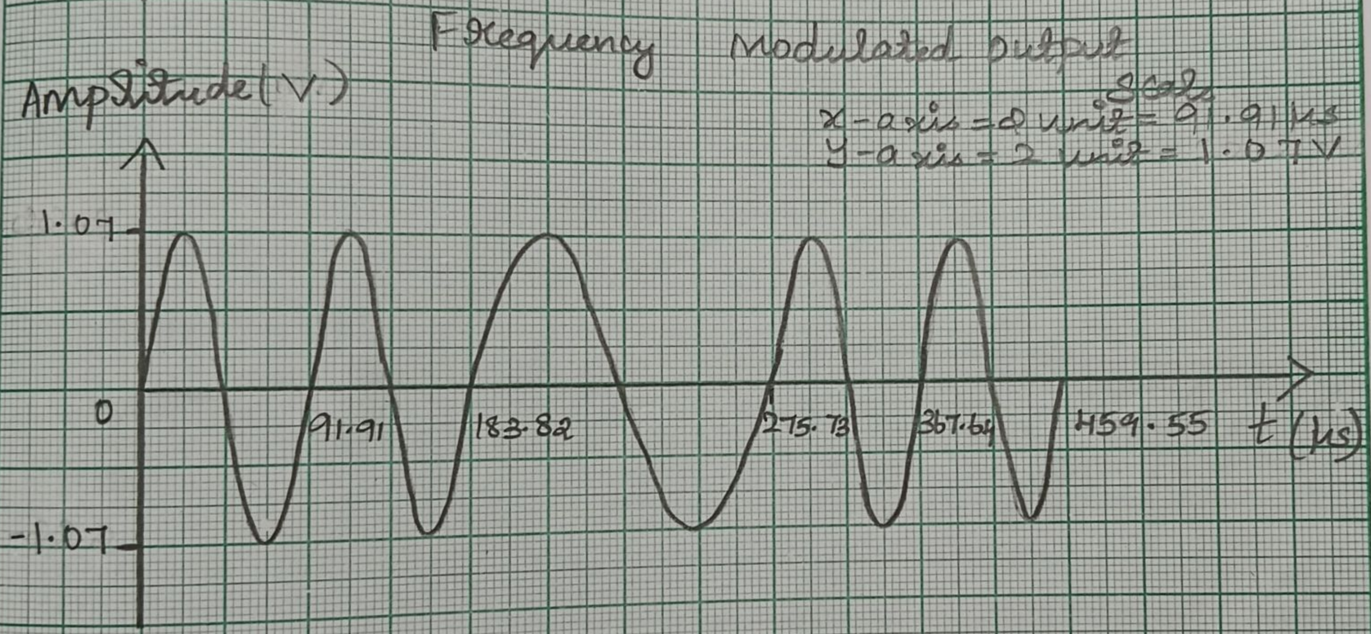
Teacher's Signature ______

TABULATION:

S.NO	PARAMETERS	AMPLITUDE	FREQUENCY	TIME PERIOD
1.	Input Signal	1.14 V	4.874 KHZ	205.1 μs
2.	Frequency Modulated Output	2.14 V	10.88 KHZ	91.91 μs

Frequency Modulation





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9. To observe the FM at lower frequencies apply sine Wave of 1KHZ and 1VPP from external function generator to MOD IN post of Onboard function Generator and keep JP4 at 10-100KHZ position and adjust the frequency at about 20-25 KHZ and output level of Function generator at 2VPP.

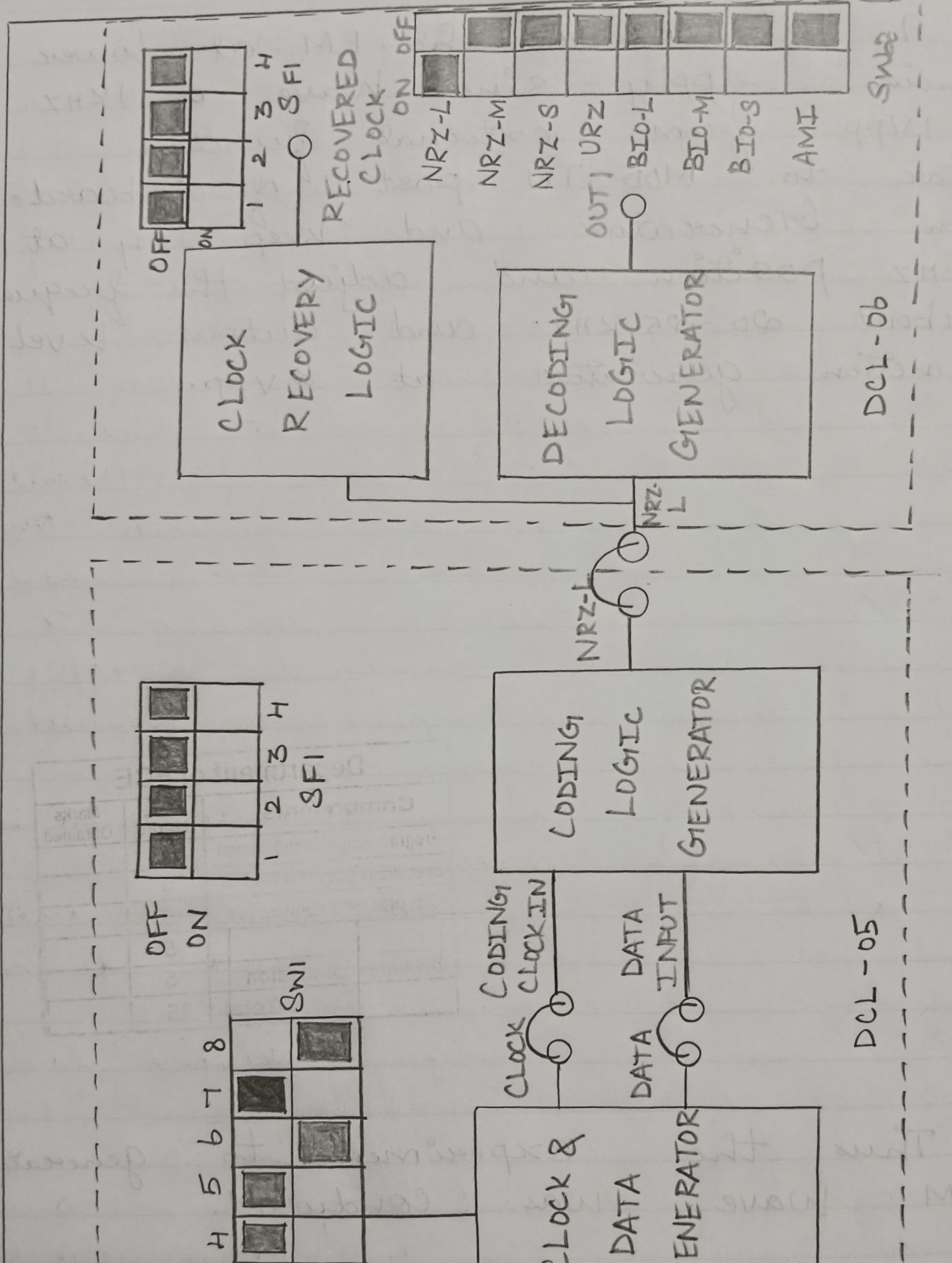
Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

Thus the experiment to generate an FM wave was conducted.

Teacher's Signature ______

BLOCK DIAGRAM:



BLOCK DIAGRAM FOR NON-RETURN TO ZERO-LEVEL CODING/DECODING TECHNIQUES

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Page No. ______

AIM:

TO study the Various line Coding Schemes

a) Non- Return -TO Zero (Level)
b) Non- Return -TO Zero (Mark)
c) Biphase (Manchester) Coding
d) Biphase (Mark) Coding
e) Alternate mark inversion (AMI) Coding

COMPONENTS REQUIRED:

1. DCL-05 & DCL-06
2. patch chords
3. power supply
4. DSO

THEORY:

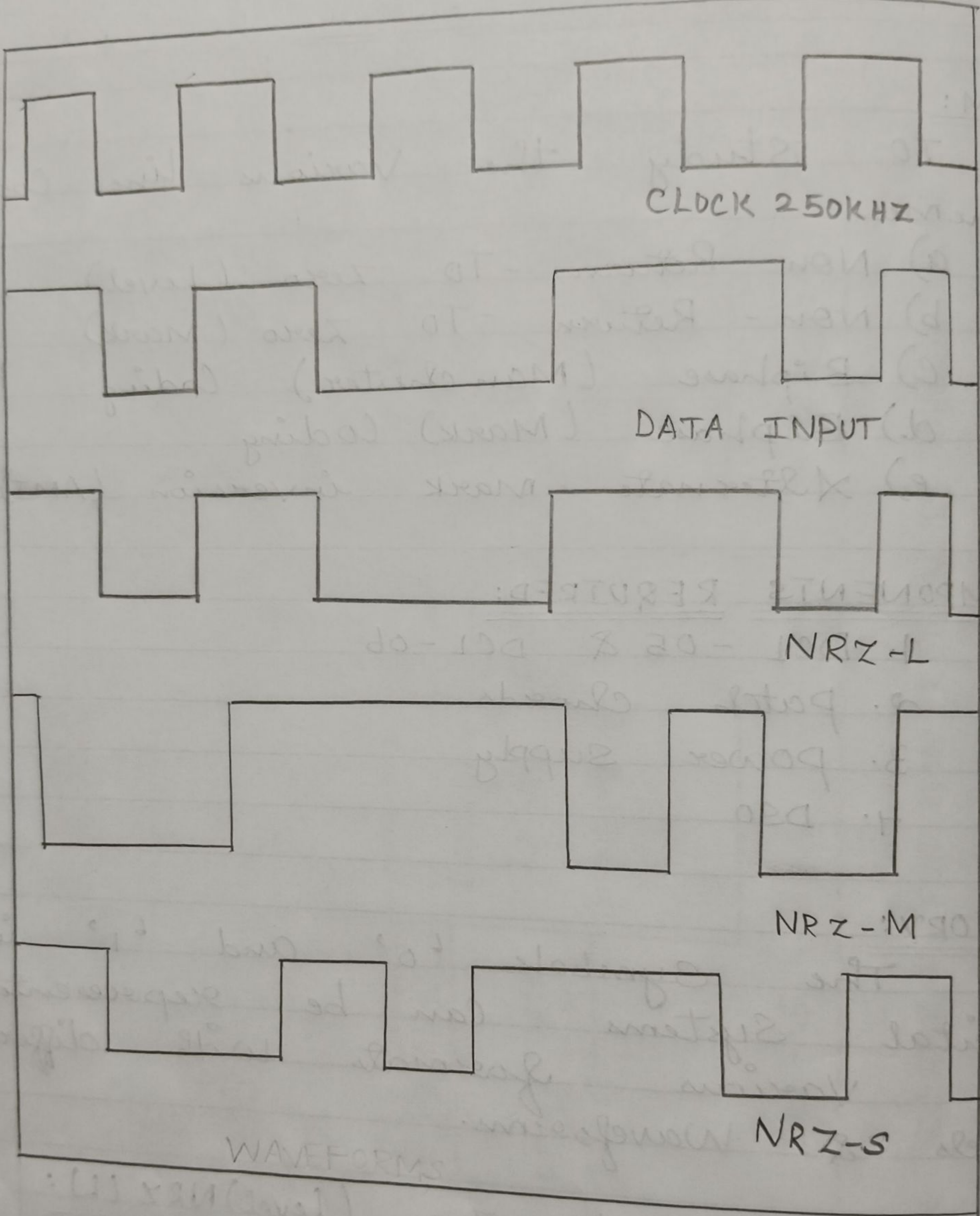
The symbols '0' and '1' in digital Systems can be represented in Various formats with different levels & Waveforms.

1. Non - Return to Zero (Level) NRZ (L):

It is the Simplest form of data representation. The NRZ (L) waveform Simply goes low for one bit time to represent a data '0' & high for one bit time to represent a data '1'.

Teacher's Signature ______

MODEL GRAPH:



2. Non- Return -To zero (Mark) : [NRZ(M)]

The NRZ(M) code is very much similar to the NRZ(L) code. Here if logic 1 is to be transmitted. The new level is inverse of the previous level. i.e. Change in level occurs.

Biphase (Manchester) Coding:

The encoding rules for biphase (Manchester) code are as follows. A data '0' is encoded as a low level during first half of the bit time and a high level during the second half.

Biphase (Mark):

The biphase (Mark) is yet another form of biphase formats. In this coding also, the data is coded as two levels in each bit time.

a) If a data '0' is to be transmitted, the sequence of the transmitted levels will remain same as for the previous bit interval.

b) If a data '1' is to be transmitted, the sequence of the transmitted levels will reverse i.e. phase reversal will occur.

PROCEDURE:

1. Refer to the block diagram and carry out the following connection and switch settings.

2. Connect power supply in proper polarity to the kits DCL-05 and DCL-06 and switch it on.

3. Connect CLOCK and DATA generated on DCL-05 to coding clock in and Data input respectively by means of the patch-chords provided.

4. Connect the coded data NRZ-L/ NRZ-M / NRZ-S/ URZ/ BIO-L / BIO-M/ BIO-S / AMI on DCL-06.

5. Keep the switch SW2 for NRZ-L to ON position for decoding logic as shown in the block diagram.

6. Observe the coded and decoded signal on the oscilloscope.

7. connect the coded data NRZ-M on DCL-05 to the corresponding DATA INPUT NRZ-M of the decoding logic on DCL-06.

8. Keep the switch SW2 for NRZ-M to ON position for decoding logic as shown in the block diagram.

9. observe the coded and decoded signal on the oscilloscope.

10. Connect the coded data NRZ-S

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On DCL-05 to the corresponding DATA INPUT NRZ-M of the decoding logic on DCL-06.

11. Keep the switch SW2 for NRZ-S to ON position for decoding logic as shown in the block diagram.

12. Observe the coded and decoded signal on the oscilloscope.

13. Connect the coded data URZ on DCL-05 to the corresponding DATA INPUT URZ of the decoding logic on DCL-06.

14. Keep the switch SW2 for URZ to ON position for decoding logic as shown in the block diagram.

15. Observe the coded and decoded signal on the oscilloscope.

16. Connect the coded data BIO-L on DCL-05 to the corresponding DATA INPUT BIO-L of the decoding logic on DCL-06.

17. Keep the switch SW2 for BIO-L to ON position for decoding logic as shown in the block diagram.

18. Observe the coded and decoded signal on the oscilloscope.

19. Connect the coded data BIO-M on DCL-05 to the corresponding DATA INPUT BIO-M of the decoding logic on DCL-06.

Teacher's Signature ______

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20. Keep the Switch SW2 for BIO-M to ON position for decoding logic as shown in the block diagram.

21. Observe the coded and decoded signal on the oscilloscope.

22. Connect the coded data AMI on DCL-05 to the corresponding DATA INPUT AMI of the decoding logic on DCL-06.

23. Keep the switch SW2 for AMI to ON position for decoding logic as shown in the block diagram.

24. Observe the coded and decoded signal on the oscilloscope.

25. Use RESET switch for clear data observation if necessary.

26. Unipolar to Bipolar / Bipolar to Unipolar:

a) Connect NRZ-L signal from DCL-05 to the input post IN of Unipolar to Bipolar and Observe the Bipolar Output at post OUT.

b) Then connect bipolar output signal to the input post IN of Bipolar to unipolar and observe unipolar output at post OUT.

Teacher's Signature ______

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Department of ECE		
Components	Max. Marks	Marks Obtained
Programming / Circuit Design	5	
Execution / Circuit Connection	5	
Results and Inferences	5	
Viva	5	
On time submission	5	
Total	25	

RESULT:

Thus the Various line coding Schemes were Studied.

Teacher's Signature ______