Indian Institute of Technology Bombay
Department of Electrical Engineering
EE-309: Microprocessors

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Test 6 (Open Book)

MM: 10 marks **Aug 30, 2018** **Time: 20 Min**

Questions 1 [5]: Which statements are true for 8051

(a) All programmable interrupts can be masked ○ (Yes disable EA)

(b) A port can be partially used as input port and partially as output port

(c) Serial interrupt can get the highest priority among the programmable interrupts

(d) Disabling interrupt will also disable the reset ×

(e) Timers can be used to count an event on the external interface using T0/T1

Question 2 [5]: Instructor of course EE-309 asked you to develop a monitor program to match the fingerprint (One byte data) to allow students to enter into Institute Auditorium during cultural fest. You have decided to develop 8051-based system for this purpose as you have already learnt how to use this device in your laboratory practice and a similar kind of program is discussed in the class. After testing the chip, 8051, you figured out that register bank RB0 and RB1 are not functional. One of your friends mentioned you that you can still use this chip as you have availability of other register banks. However (s)he warned you to be careful while programming stacks etc. You also feel that 4KB memory is not sufficient for future uses, therefore you bought additional ROM for program (16 KB) and decided to use that only (i.e., decided not to use the internal ROM). You have also bought data ROM (16 kB) as well as data RAM (16 kB). → Till here same

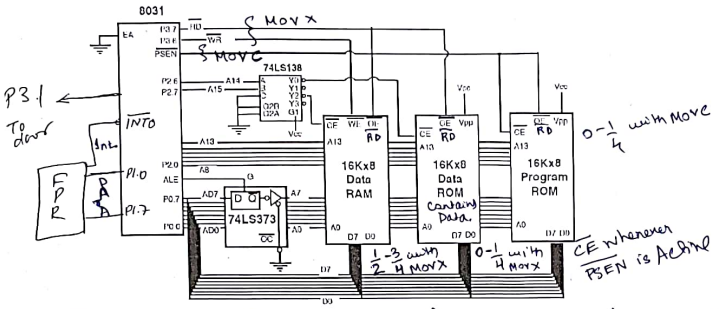
RB0 ✗ RB1 ✗

→ Matching Data there in ext. Data ROM

The size of fingerprint is one byte. Assume fingerprints of all the students are available to you (you have stored them in external data ROM). You are expected to read fingerprint (one byte data) of the student entering into Auditorium using port 1 (fingerprint scanning device should be connected to P1). The moment FPR detect the finger it will generate one bit signal with high to low transition which can stay low upto 12 cycles (about one microsecond). This input is connected to pin P3.2 (INT0). The system should provide ONE BIT output to port 3 (P3.1), which activates the door lock (opens door) when set high on matching fingerprint. You have decided to interface using interrupts. If you think this device is usable, please write a program. If you think it is not usable then explain the reasons.

→ The Chip 74138 is a 3 → 8 Decoder
• We are using it like a 2 → 4 Decoder

→ No it is not possible to use given Arrangement.
Reasons → Overlap .....



→ Since $\overline{EA} = 0$, we always read from external memory.

→ At power up, 8031 will Implicitly attempt to read the Instruction in 0000h of external memory

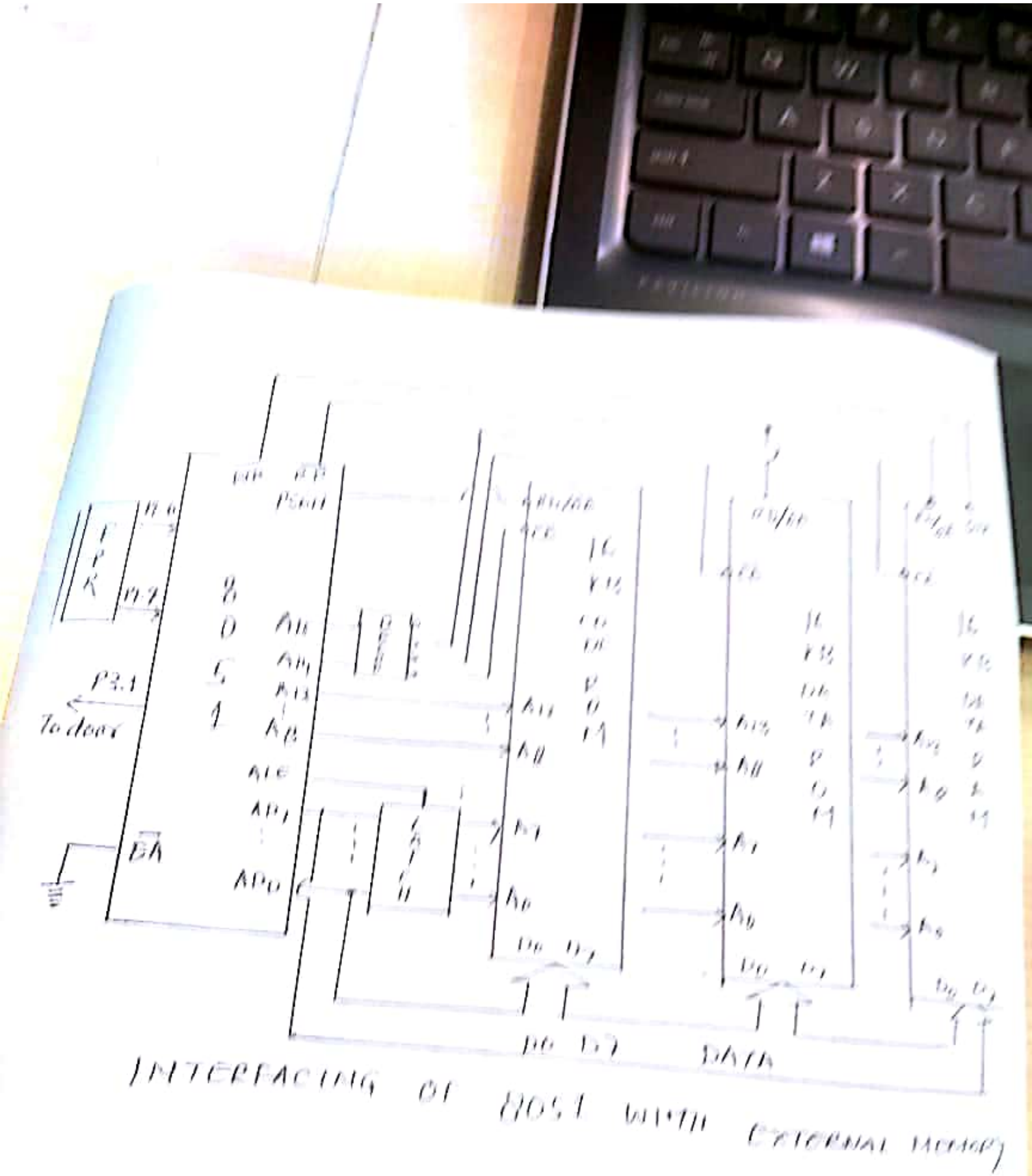
→ The Data ROM Chip will be Enabled since its $\overline{CE}$ is such that 0000h to 3FFFh

→ Both the Data ROM Chip and Program ROM Chip will simultaneously be Enabled at Startup

→ But since $\overline{PSEN}$ is connected to $\overline{RD}$ of Pgy. ROM it will read Instruction from there (0000h start)

→ later when we want to use Data ROM, we must use MOVX ~~to~~ since MOVC can only read from Program ROM

→ The Main ISSUE is that when we write ISR for $\overline{INT0}$ at 03h, then ~~later~~ inside it if we use MOVX, then we will attempt to Read ISR from the wrong chip (Data Chip) & Return to the memory location on wrong chip



INTERFACING OF 8051 WITH EXTERNAL MEMORY

Indian Institute of Technology Bombay
Department of Electrical Engineering
EE-309: Microprocessors

Name: ID

Test 5 (Open Book)

MM: 10 marks | Aug 23, 2018 | Time: 20 Min

Question 1 [3]: Which statements are true for 8051

(a) Execution of RET is superset of execution of RET instruction

(b) ANL P1, #50 instruction always perform ANDing of data of P1 pins with #50

(c) You can always use instruction SETB EA to use external ROM

Question 2 [7]: Instructor of course EE-309 asked you to develop a monitor program to match the fingerprint (One byte data) to allow students to enter into Institute Auditorium during cultural fest. You have decided to develop 8051 based system for this purpose as you have already learnt how to use this device in your laboratory practice and a similar kind of program is discussed in the class. After testing the chip, 8051, you figured out that register bank RB0 and RB1 are not functional. One of your friends mentioned you that you can still use this chip as you have availability of other register banks. However (s)he warned you to be careful while programming stacks etc. You also feel that 4KB memory is not sufficient for future uses, therefore you bought additional ROM for program (32 kB) and decided to use that. You have also bought data ROM (16 kB) as well as data RAM (16 kB). Memory is interfaced in the following way as taught in the class (shown in figure below). Further, your friend noticed that $\overline{PSEN}$ and $\overline{RD}$ signals connected to data ROM and program ROM have been swapped while interfacing, which makes you worried. However, (s)he figured out that both are ROMs, therefore it does not matter. You believe your friend always think through before making any comment. Are you convinced with your friend's argument? Justify your answer. If you are convinced with his(her) argument then write a program to match the fingerprint of about 250 students residing on campus. The size of fingerprint is one byte. Assume fingerprints of all the students are available to you (you can store either in external data ROM or program ROM). You are expected to read fingerprint (one byte data) of the student entering into Auditorium using port 1 (fingerprint scanning device should be connected to P1). The system should provide ONE BIT output to port 3 (P3.1), which activates the door lock (opens door) when set high on matching fingerprint. If you are not convinced then explain the reason.

Indian Institute of Technology Bombay
Department of Electrical Engineering
EE-309: Microprocessors

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Test 7 (Open Book)

MM: 10 marks **Sep 06, 2018** **Time: 15 Min**

Question 1 [4]: 8051 transmits 750 characters per second (character is 8 bit) in serial communication mode. Compute the data rate and baud rate.

Data Rate:

Baud Rate:

Question 2 [6]: You are serving as a leading architect at Smart Computer System (SCS) Inc., which designs a low-end processor called *Little-Bombay* for embedded controller market. As a first task being an architect, you are working on instruction set architecture and decided to build a 12-bit RISC type machine, i.e. instruction length is 12 bits. The machine uses fixed instruction length and can use any suitable coding scheme. You have decided to use 32 general purpose 12-bit registers to reduce memory traffic and memory is indirectly addressable. You have surveyed most common operations to be implemented and figured out that you need to at least implement 3 two-address instructions and 25 zero address instructions. Your friend, Unmesh, suggests you some useful common one-address instruction which may be very effective in getting high performance, however he would like to know maximum how many one-number of one address instruction your processor support. Compute the maximum number of one-address instructions your processor? Sketch out possible encoding.