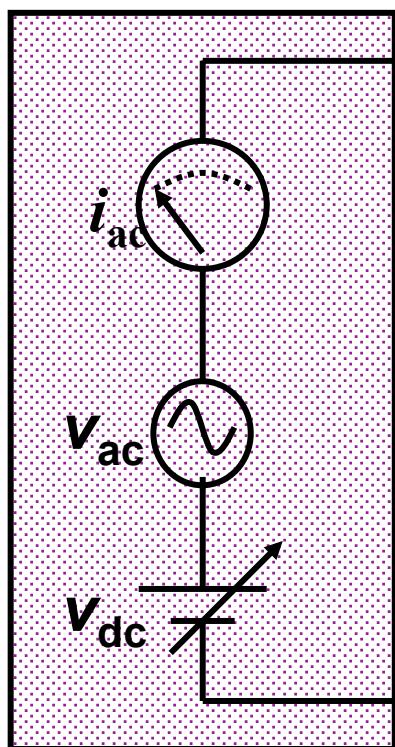


MOS CV Measurement Method

Small signal AC
superposed on DC



C-V Meter

V_G (DC) is scanned

Capacitive current due to
 v_{ac} is measured

$$i_{ac} = C \frac{dv_{ac}}{dt}$$

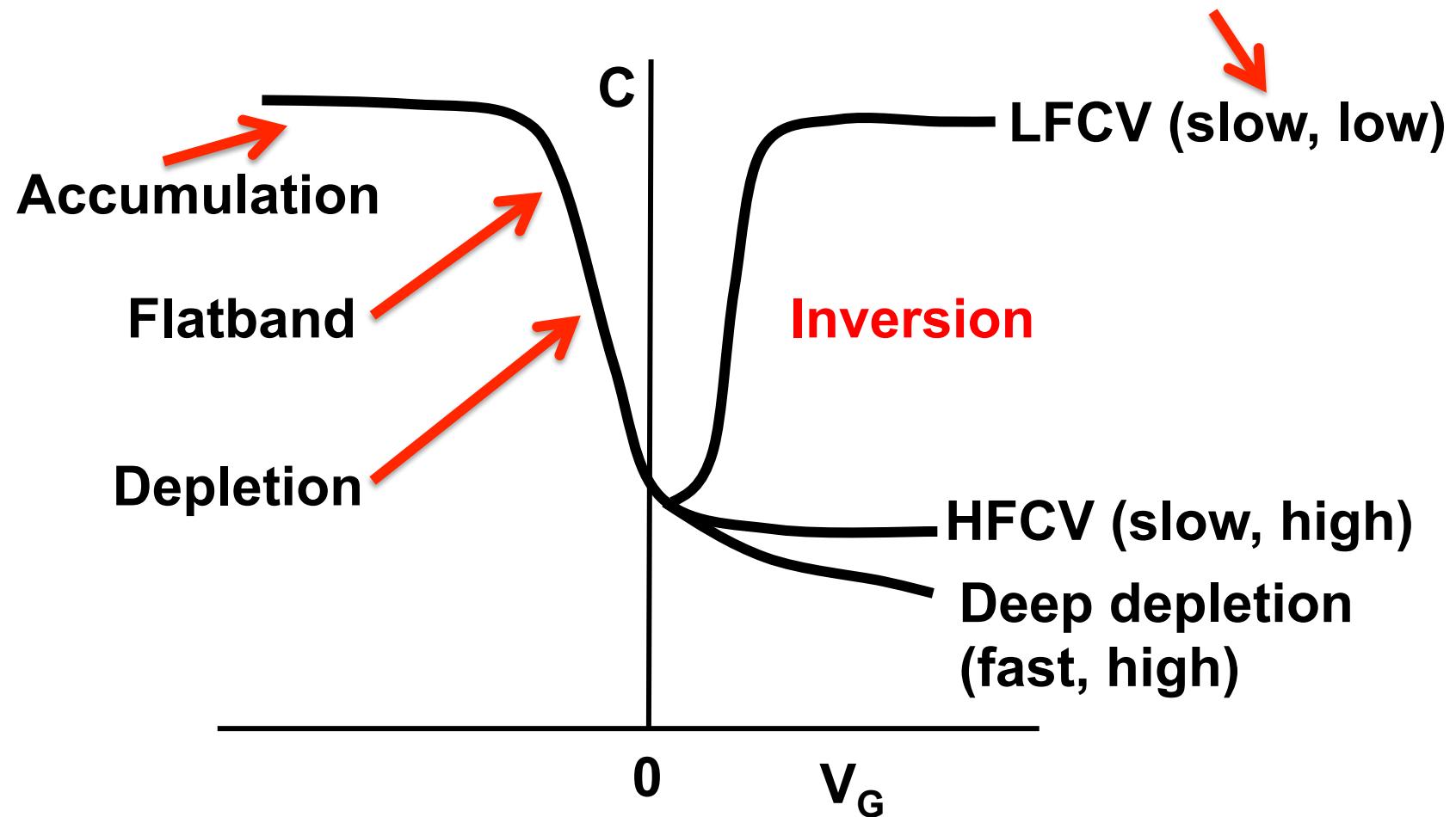
$$C = \frac{dQ_m}{dV_G} = -\frac{dQ_s}{dV_G}$$

DC ramp rate
AC frequency

MOS CV Characteristics (NMOS)

N+ poly-Si gate / P-type substrate

Ramp rate, frequency



MOS CV Inversion Charge Response

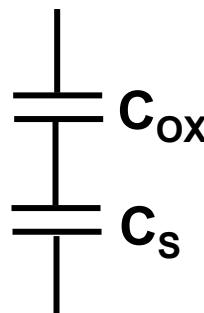
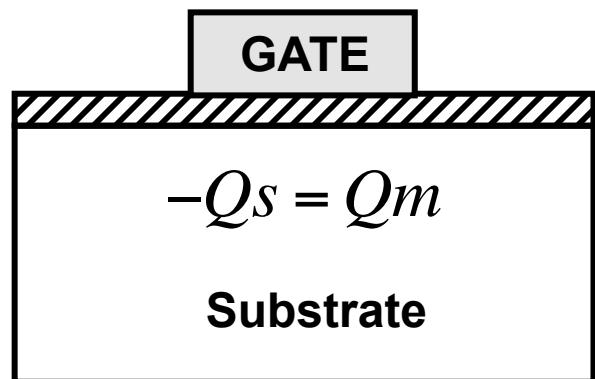
NMOS: Minority carriers (electrons) from thermal G-R

M	DC Ramp	AC freq.	Response
o	Slow	Slow	Both DC and small signal variation
s	Slow	Fast	DC variation, not small signal variation
	Fast	Fast	None

Response of minority electrons to DC and AC signals determines CV behavior in inversion

As in the graph

MOS CV Basics (NMOS)



$$C = \frac{dQ_m}{dV_G} = -\frac{dQ_s}{dV_G}, C_s = -\frac{dQ_s}{d\psi_s}$$

$$-Q_s = C_{ox}(V_G - V_{FB} - \psi_s)$$

$$V_G = V_{FB} + \psi_s - \frac{Q_s}{C_{ox}}$$

$$\frac{dV_G}{dQ_s} = \frac{d\psi_s}{dQ_s} - \frac{1}{C_{ox}}$$

$$\frac{1}{C} = \frac{1}{C_s} + \frac{1}{C_{ox}}$$

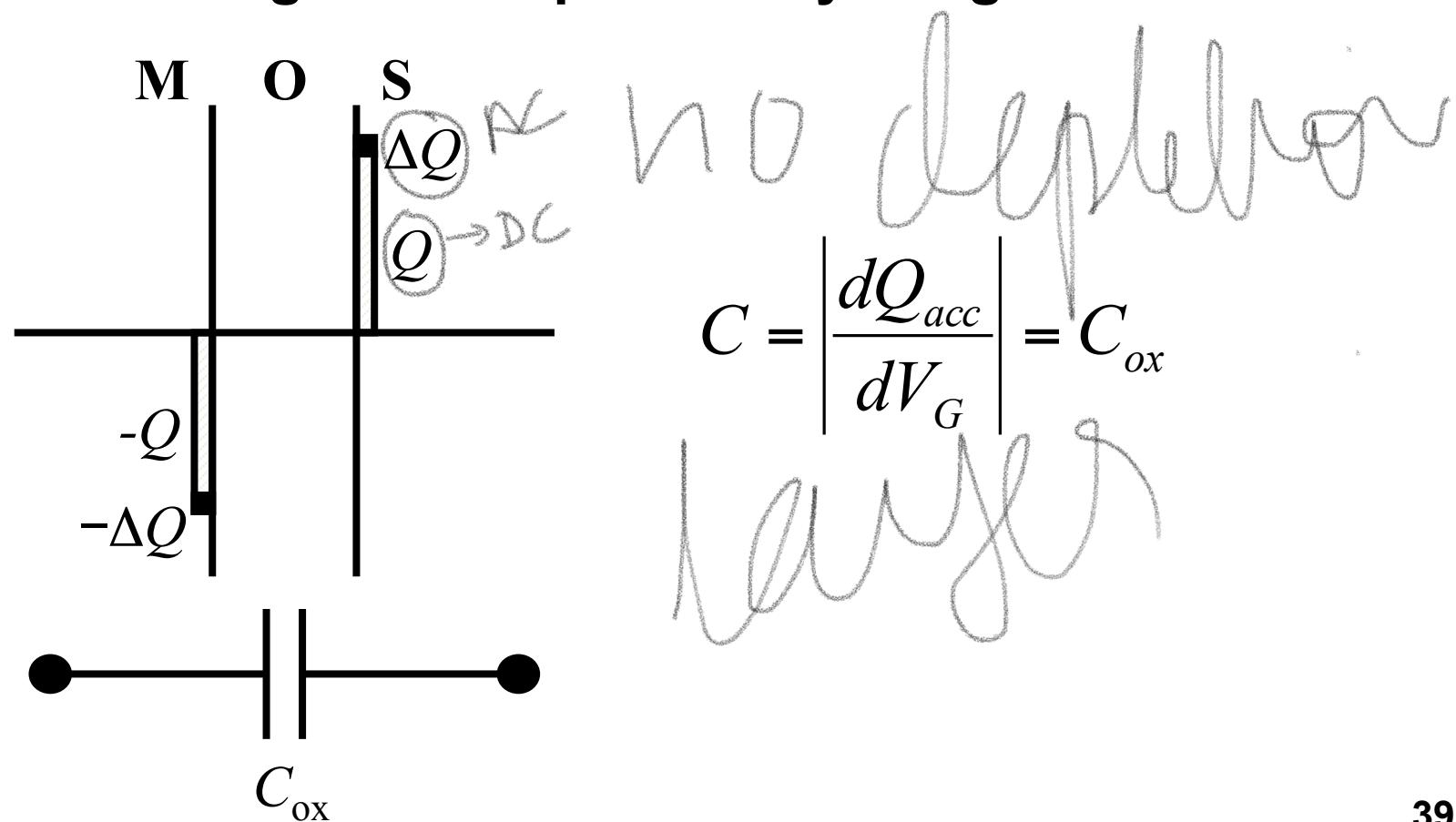
Total capacitance is a series combination of oxide and substrate capacitance

V_G is w.r.t V_{FB} for non ideal MOS

Capacitance in Accumulation (p-type Si)

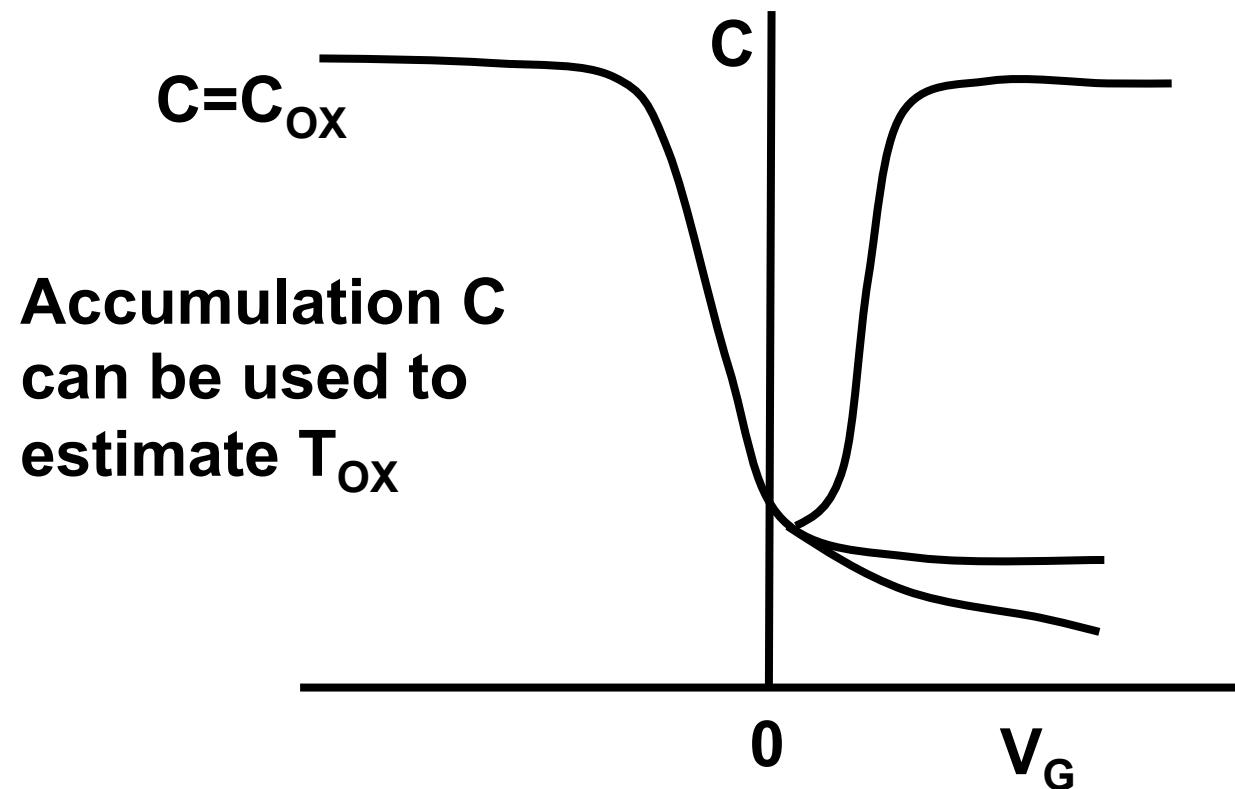
As gate voltage is varied, incremental charges are added/subtracted to/from the gate and substrate.

Incremental charges are separated by the gate oxide.



MOS CV Characteristics (NMOS)

N+ poly-Si gate / P-type substrate



Flat-Band Capacitance

At the flat-band condition, variations in V_G give rise to the addition/subtraction of incremental charges in the substrate, at a depth L_D



The diagram shows a parallel plate capacitor with two dielectrics. The left plate is connected to ground. The right plate is connected to a voltage source. The left dielectric is labeled C_{ox} and the right dielectric is labeled C_{Debye} .

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{L_D}{\epsilon_{Si}}$$

From here we can find V_{fb}

*independent
of d_{it} &
oxide chargl*

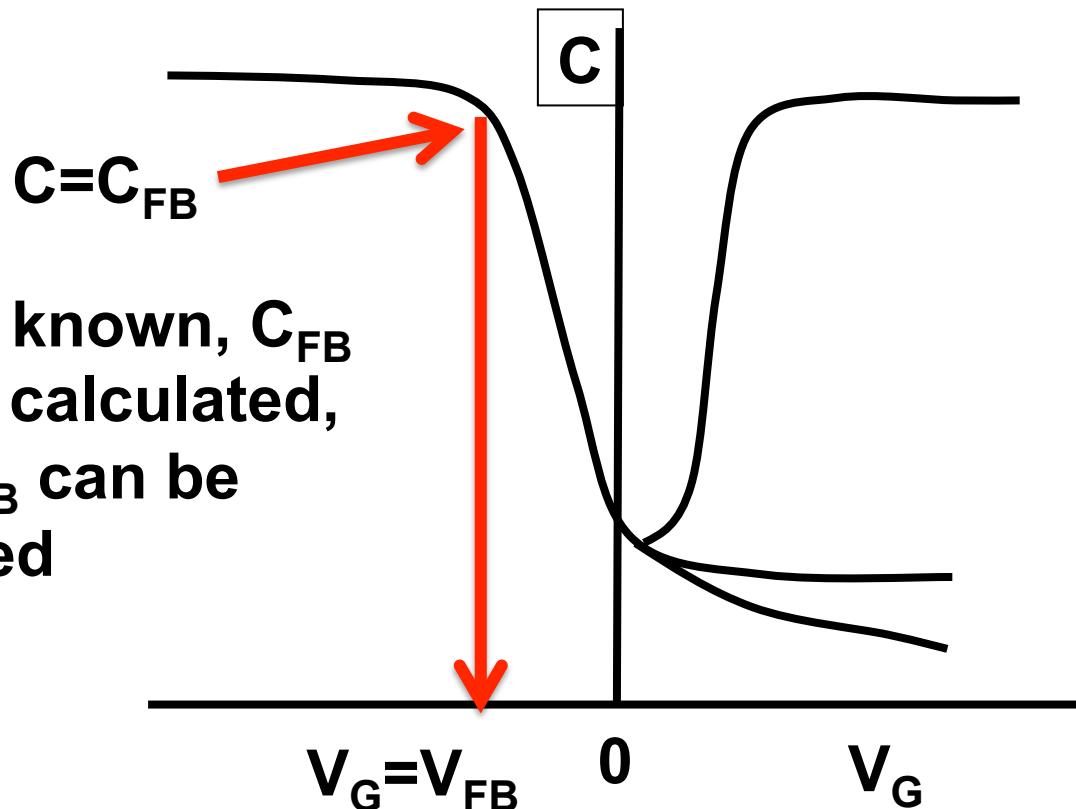
L_D is “extrinsic Debye Length” → characteristic shielding distance, or the distance where the electric field emanating from a perturbing charge falls off by a factor of $1/e$

$$L_D = \sqrt{\frac{\epsilon_{Si} kT}{q^2 N_A}}$$

MOS CV Characteristics (NMOS)

N+ poly-Si gate / P-type substrate

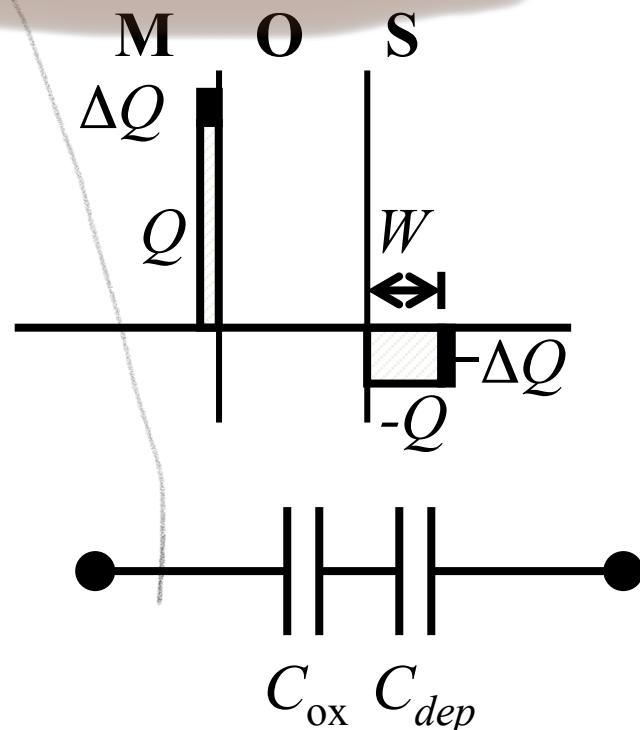
If N_A is known, C_{FB} can be calculated, and V_{FB} can be obtained



Capacitance in Depletion (NMOS)

As the gate voltage is varied, the width of the depletion region varies.

Incremental charge is effectively added/subtracted at a depth W in the substrate.



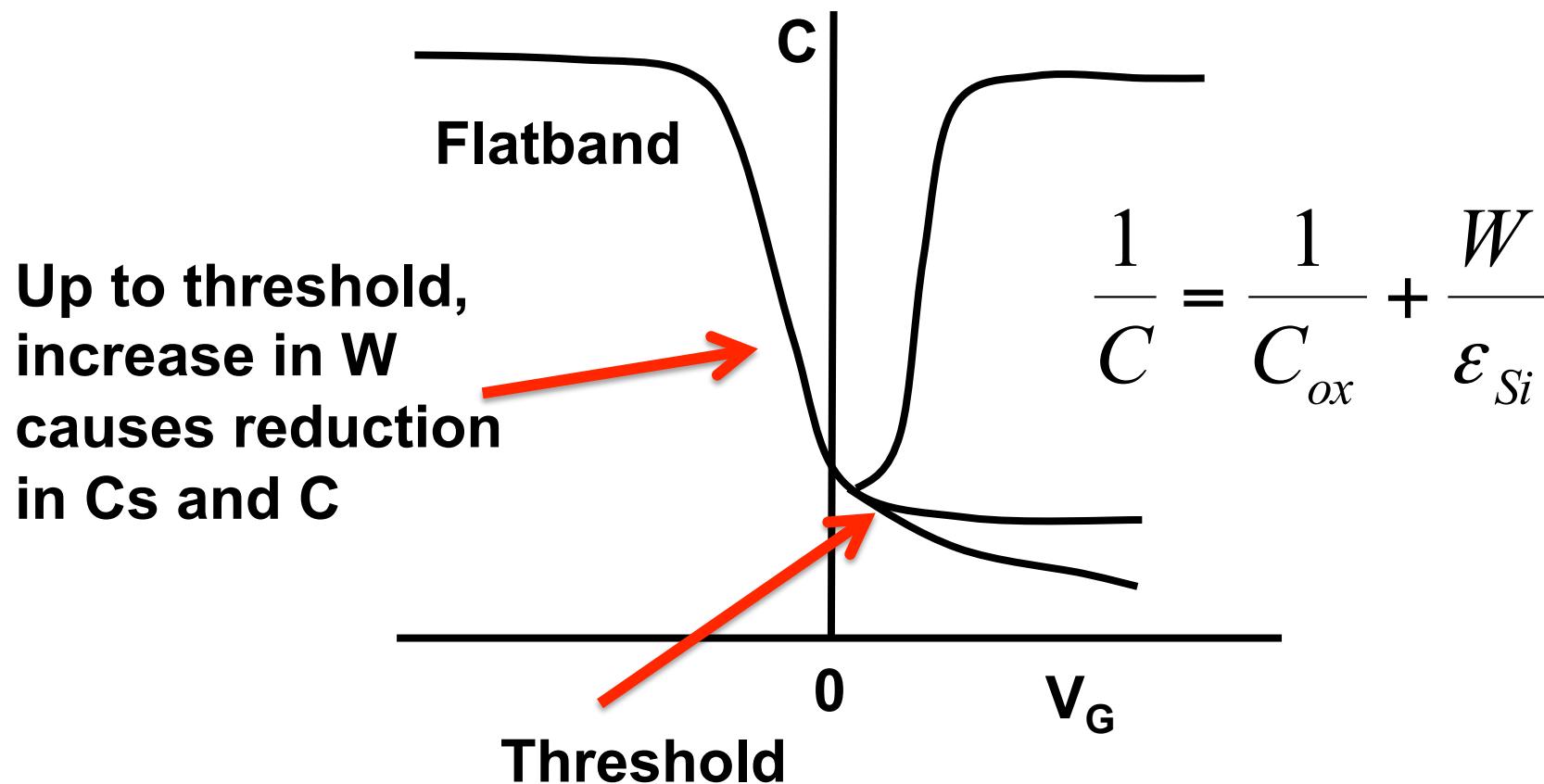
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{W}{\epsilon_{Si}}$$

$$\Rightarrow W = \sqrt{\frac{2\epsilon_{Si}\psi_S}{qN_A}}$$

(Recall one-sided PN junction)

MOS CV Characteristics (NMOS)

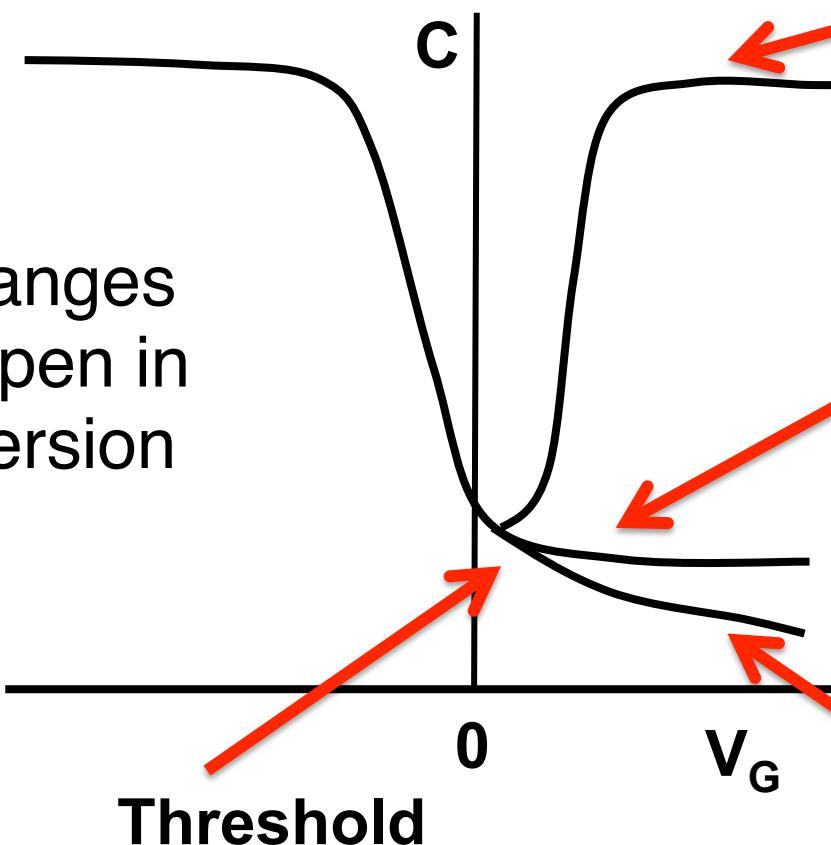
N+ poly-Si gate / P-type substrate



MOS CV Characteristics (NMOS)

N+ poly-Si gate / P-type substrate

Changes happen in inversion



LFCV: Low dc ramp rate, low ac frequency → Inversion layer responds to dc and ac

HFCV: Low dc ramp rate, high ac frequency → Inversion layer responds to dc but not to ac

changes remain at end of depletion layer

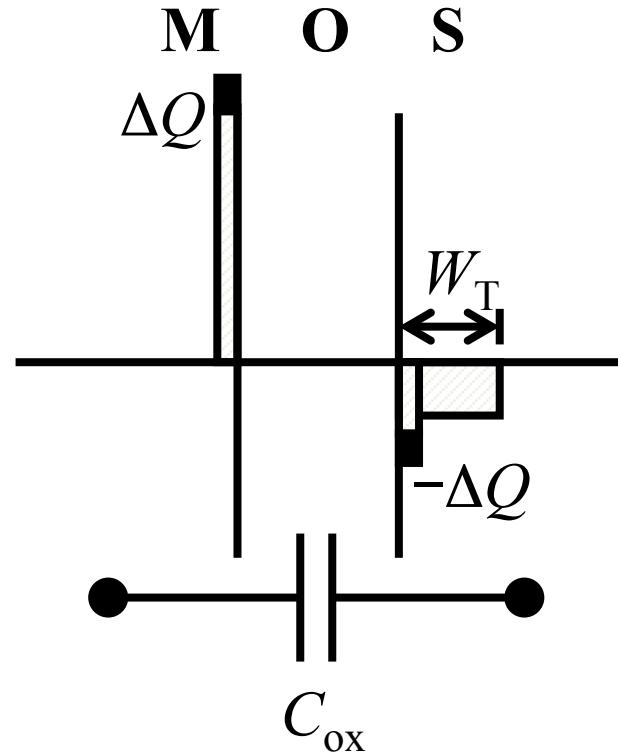
DD: High dc ramp rate, high ac frequency → Inversion layer does not respond to dc and ac, increase in W , reduction in C

hole

Ramp voltage is quasi static

Capacitance in Inversion (NMOS)

LFCV: Inversion-layer charge *can* be supplied/removed quickly enough to respond to changes in the gate voltage. Incremental charge is effectively added/subtracted at the surface of the substrate.

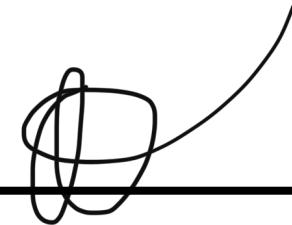


$$C = \left| \frac{dQ_{inv}}{dV_G} \right| = C_{ox}$$

Time required to build inversion-layer charge?

As majority carriers have less generation time so mos characteristic have only one curve in acc but in inversion charges are minority and they have more generation time so there are two curves

Minority Carrier Response Time



Recombination current density (recall PN diode):

$$J_R = q \cdot n_i \cdot W_D / 2\tau; \text{ where } \tau \text{ is minority lifetime}$$

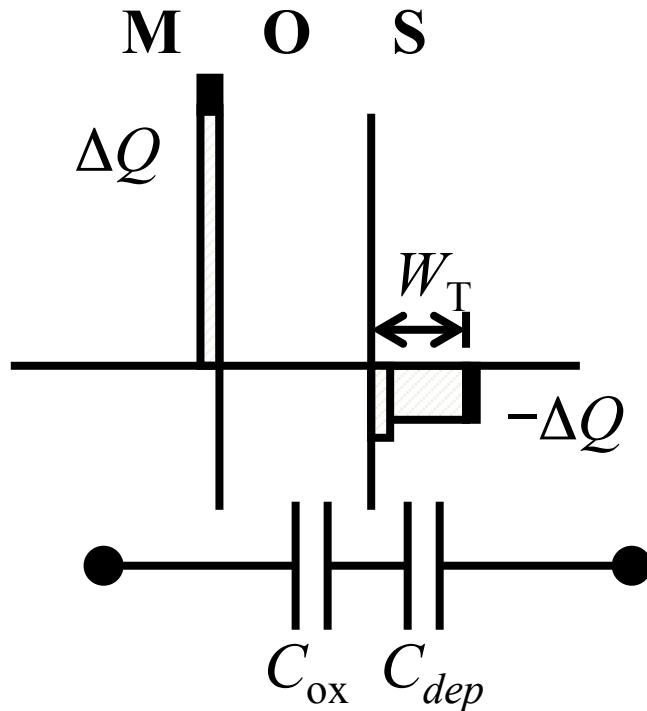
Depletion charge: $Q_d = q \cdot N_A \cdot W_D$

Time taken to replenish inversion layer:

$$Q_d / J_R = 2(N_A / n_i) \cdot \tau$$

Capacitance in Inversion (NMOS)

HFCV: Inversion-layer charge *cannot* be supplied/removed quickly enough to respond to changes in the gate voltage. Incremental charge is effectively added/subtracted at a depth W_T in the substrate.



$$\begin{aligned}\frac{1}{C} &= \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \\ &= \frac{1}{C_{ox}} + \frac{W_T}{\epsilon_{Si}} \\ &= \frac{1}{C_{ox}} + \sqrt{\frac{2(2\phi_F)}{qN_A\epsilon_{Si}}} \equiv \frac{1}{C_{\min}}\end{aligned}$$

If C_{ox} is known, C_{\min} can be used to determine N_A

Parameter Extraction Summary

Determine T_{ox} from C_{max} in accumulation

Determine N_A from C_{min} in inversion HFCV

Determine C_{FB} , and find V_{FB}

- What can we find from V_{FB} ?

from graph

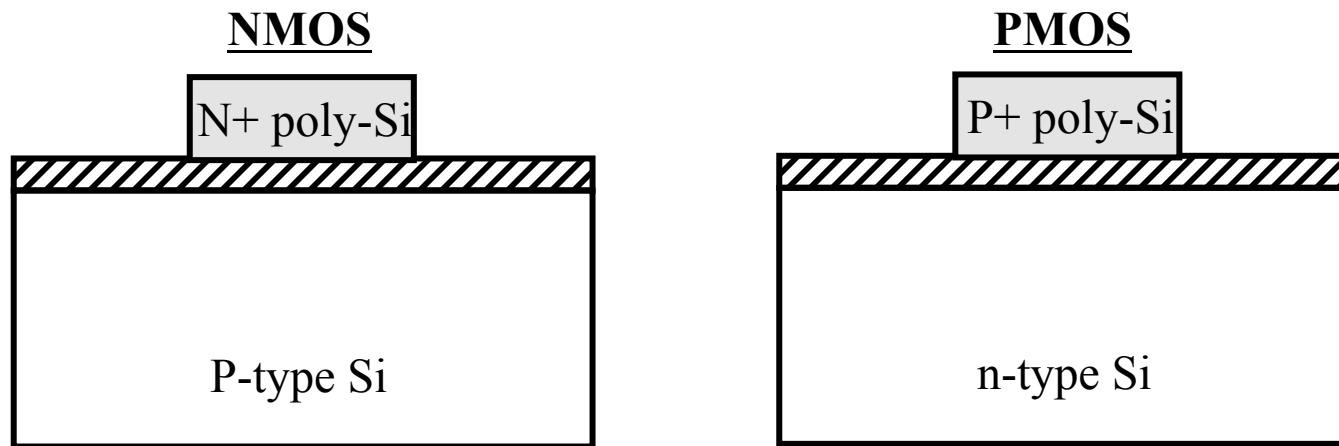
metal work function

Can you find C_{MG} and V_{MG} (midgap, for $\psi_s = \phi_F$)

yes depletion

Poly-Si Gate Depletion

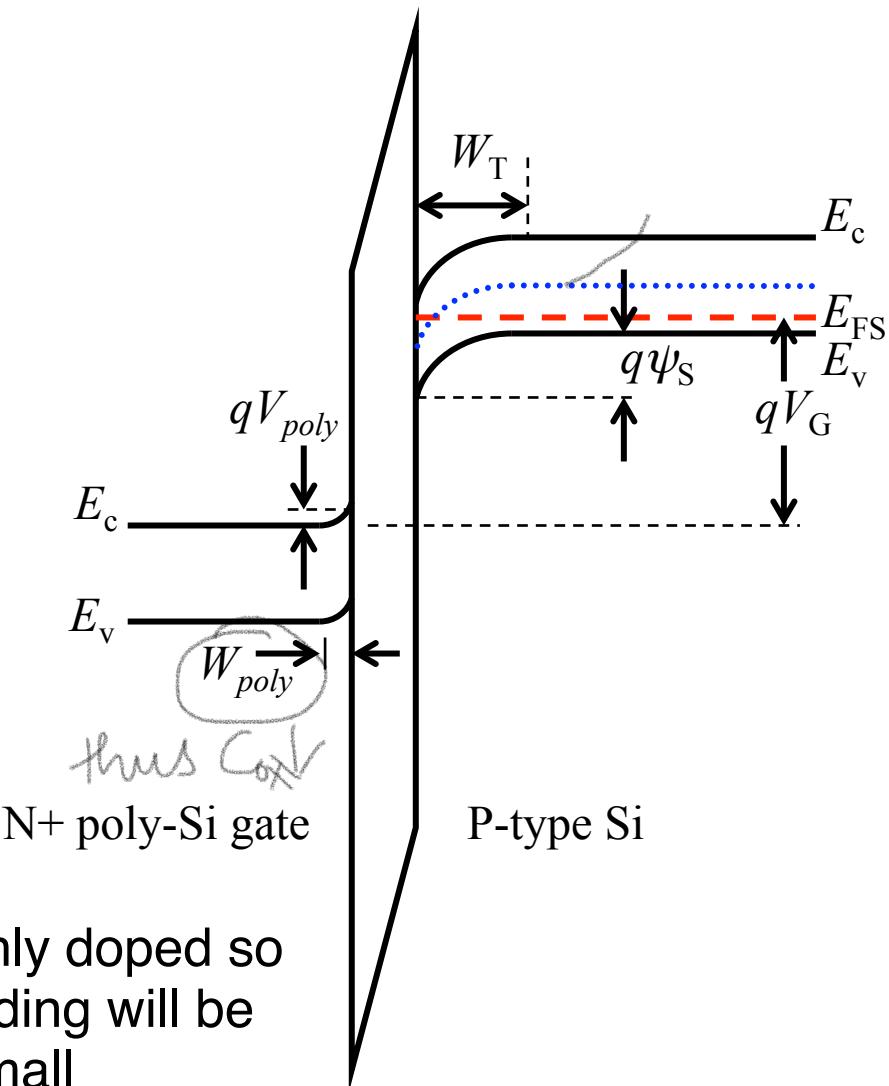
- Heavily doped film of polycrystalline silicon (poly-Si) is typically employed as the gate-electrode material in modern MOS devices.



- There are practical limits to the electrically active dopant concentration
- The gate must be considered as a semiconductor, rather than a metal

MOS Band Diagram with Gate Depletion

NMOS (p-type Si) biased to inversion:



V_G is effectively reduced:

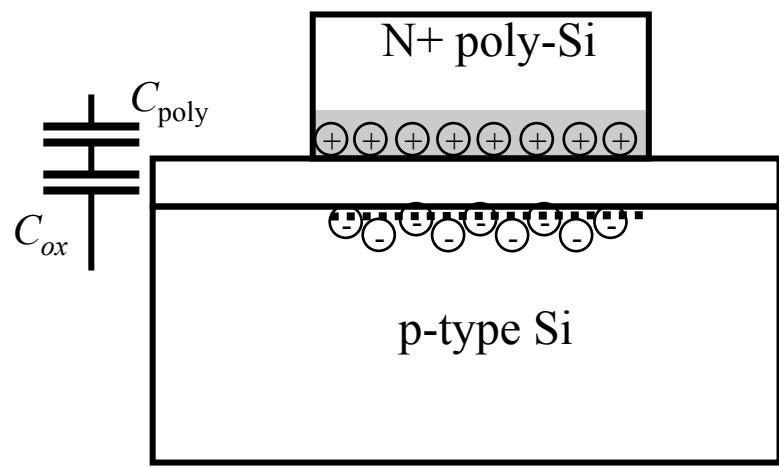
$$Q_{inv} = C_{ox}(V_G - V_{poly} - V_T)$$

$$W_{poly} = \sqrt{\frac{2\epsilon_{Si}V_{poly}}{qN_{poly}}}$$

How can gate depletion
be minimized?

Gate Depletion Effect

T_{ox} is effectively increased:

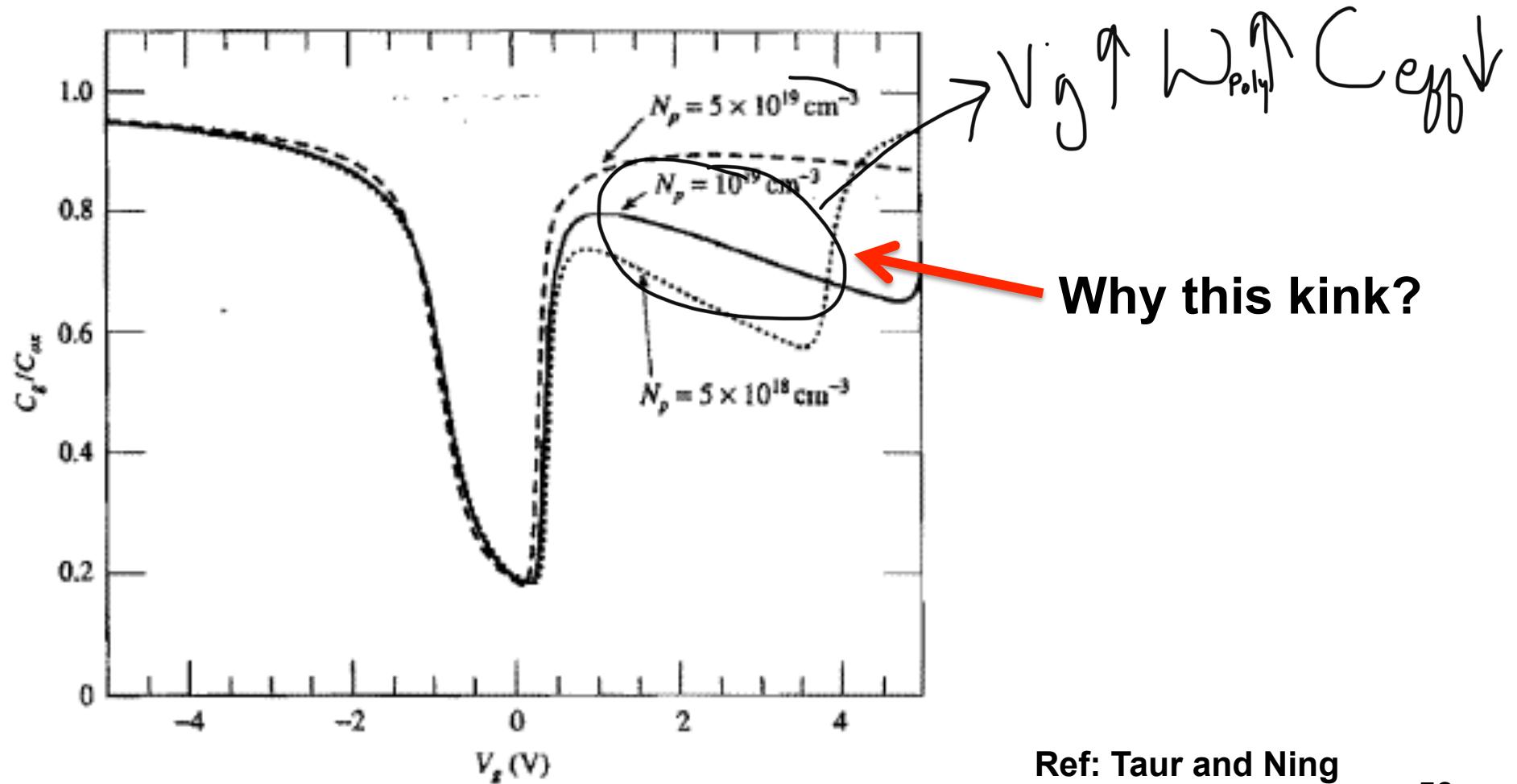


$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{poly}} \right)^{-1} = \left(\frac{T_{ox}}{\epsilon_{ox}} + \frac{W_{poly}}{\epsilon_{Si}} \right)^{-1}$$
$$= \frac{\epsilon_{ox}}{T_{ox} + (W_{poly}/3)}$$

$$Q_{inv} = (V_G - V_T) \cdot \frac{\epsilon_{ox}}{T_{ox} + (W_{poly}/3)}$$

Impact on CV Characteristics

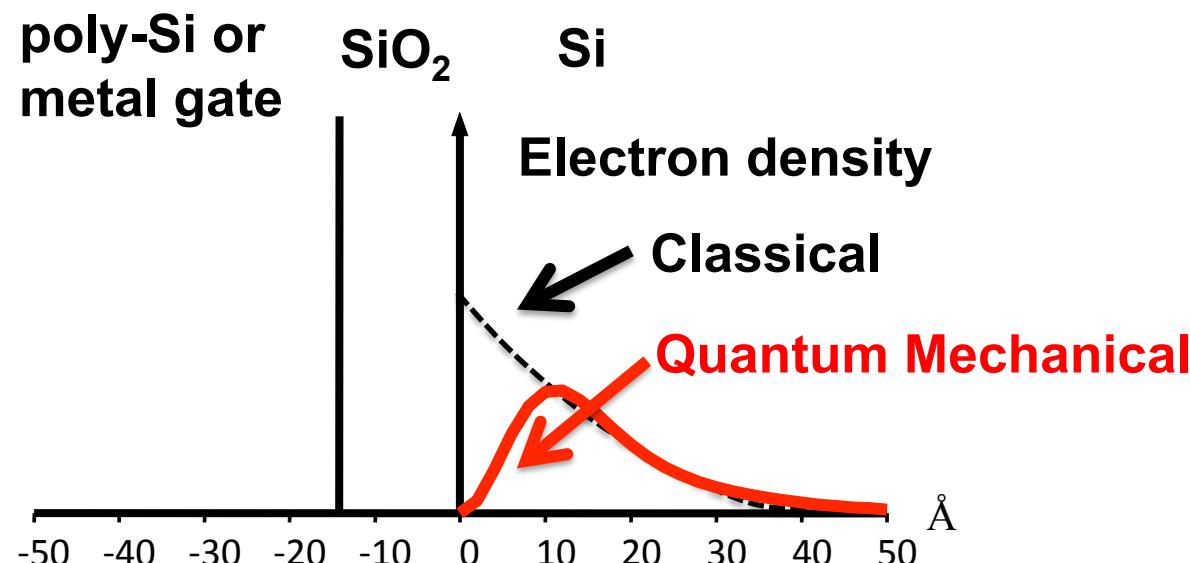
Reduction in inversion, more for lower poly doping



Ref: Taur and Ning

Inversion-Layer Quantization

The average inversion-layer location is below the Si/SiO₂ interface, adds extra “oxide thickness”.

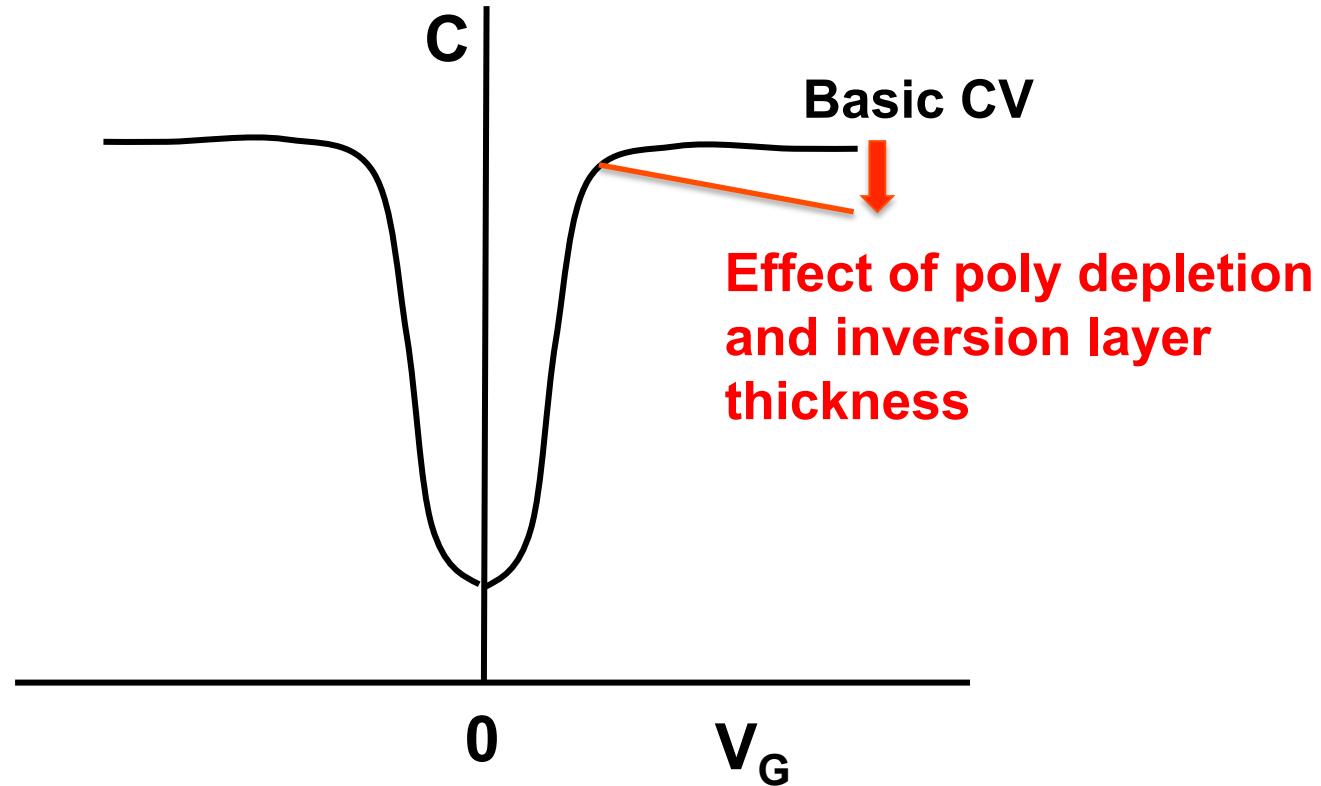


According to classical physics the inversion charge should be at the interface but as the substrate and oxide interface behaves as an quantum well there fore there is a maxima at few angstrom from the interface

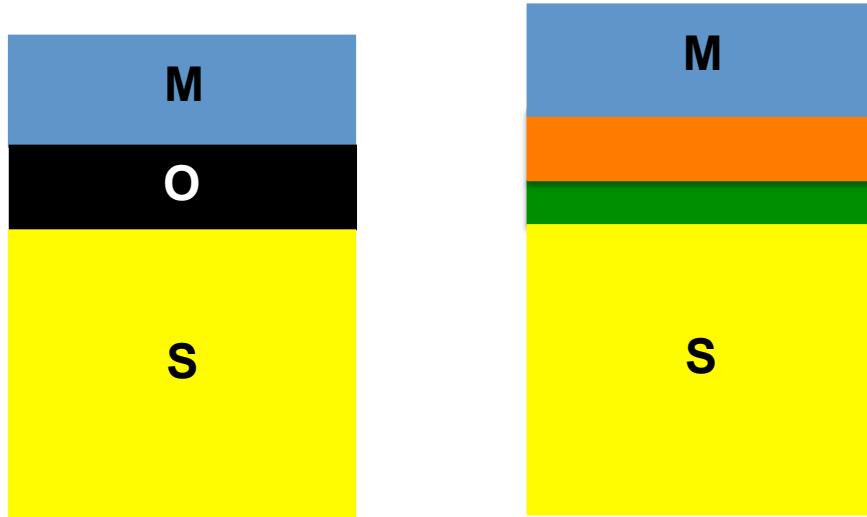
Effective Oxide Capacitance, C_{oxe}

$$T_{oxe} = T_{ox} + W_{poly}/3 + T_{inv}/3$$

$$Q_{inv} = \frac{\epsilon_{ox}}{T_{oxe}} (V_G - V_T) = C_{oxe} (V_G - V_T)$$



Dual Layer Gate Stacks (High-K Metal Gate)



HK: High-K (HfO_2), $k \sim 20$

IL: Interlayer ($\sim \text{SiO}_2$), $k \sim 4$

Capacitance
Equivalent
Thickness

$$C_{OX} = \frac{\epsilon_{SiO_2}}{EOT} = \left[\frac{T_{IL}}{\epsilon_{IL}} + \frac{T_{HK}}{\epsilon_{HK}} \right]^{-1};$$

Equivalent
Oxide
Thickness

$$CET \approx EOT + 0.3\text{nm}$$

due to polygate