Assignment-3

Due Date - 06/03/2019

1. Write a code to find out the drain current (I_D) of n-channel MOSFET as a function of drain voltage (V_{DS}) keeping gate voltage at threshold ($V_G = V_{Th} = 2*(kT/q)*\ln(N_a/n_i)$. Use Brews and Pao-Sah double integral method for the above calculation and coding. ……...[10]

2. Compare the I_D-V_{DS} curves you get from Brews and Pao-Sah double integral model with Piecewise I_D-V_{DS} model for identical device parameters. If you see any mismatch (error) between the curves then explain the reason for that….....….[10]

3. Plot the I_D-V_{DS} curves you get from Brews and Pao-Sah double integral model for different V_G ($V_G = V_{Th}$; $V_G = V_{Th} + 5*kT/q$; $V_G = V_{Th} + 10*kT/q$; $V_G = V_{Th} + 15*kT/q$). Compare the plots and if you see any increasing or decreasing trend of mismatch (error), then explain the reason……...[15]

Note:

Assume $N_a = 5x10^{15}$ cm^{-3}; V_{FB} = - 0.2 Volt; u_{eff} = 800 $cm^2V^{-1}s^{-1}$, W/L = 40; T_{SiO2} = 5 nm.

You may have to find out the surface potential for question number (3) for different gate voltages using the following equation:

$$V_G = V_{FB} + \psi_S - \frac{Q_S}{C_{OX}}$$

For reference you may look into **Section-3.1.1** from the book "**Fundamentals of Modern VLSI Devices**" by **Yuan Taur and Tak H. Ning**.