

Scaling problem

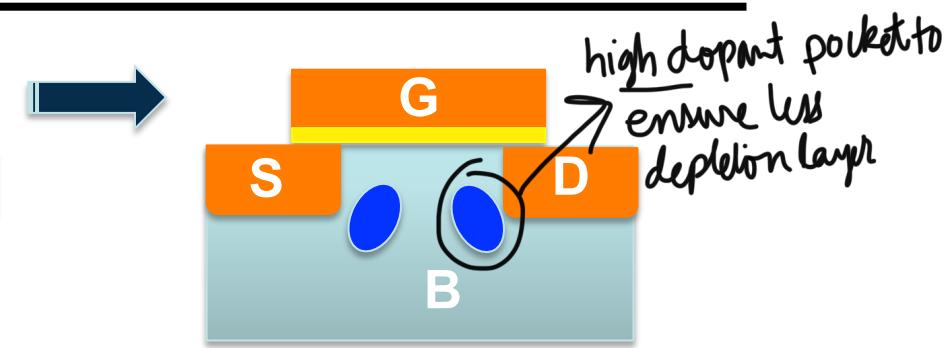
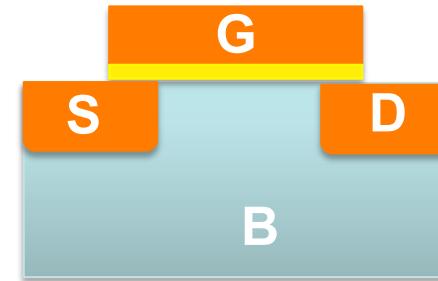
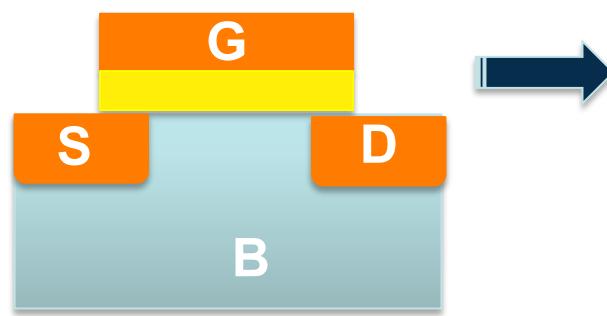
Increase in active power

Alarming increase in standby power due to channel subthreshold leakage and gate leakage (tunneling)

Increase in electric field

- Reduction in mobility (velocity saturation)**
- Reliability**

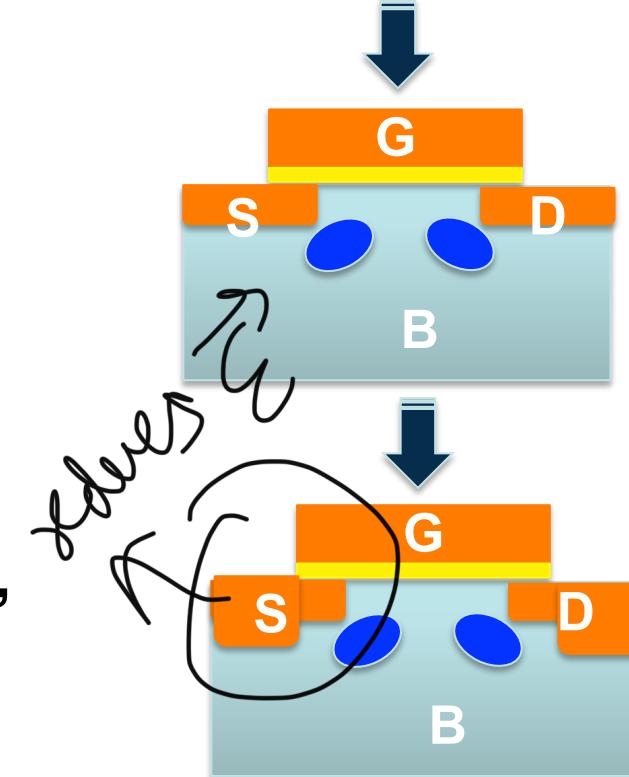
Scaling – Traditional Solutions



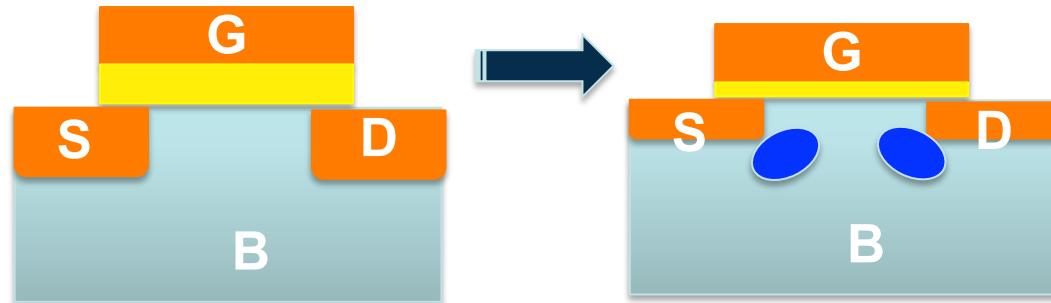
**Reduce oxide thickness –
Increase Gate control**

**Increase channel doping –
Increase “electrical” S/D distance**

**Reduce S/D junction thickness –
cutoff conduction away from surface,
but need LDD/HDD to manage
electric field / series resistance**



Limitations of Gate Oxide Scaling

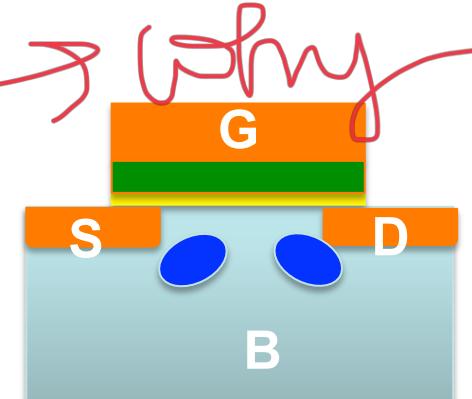
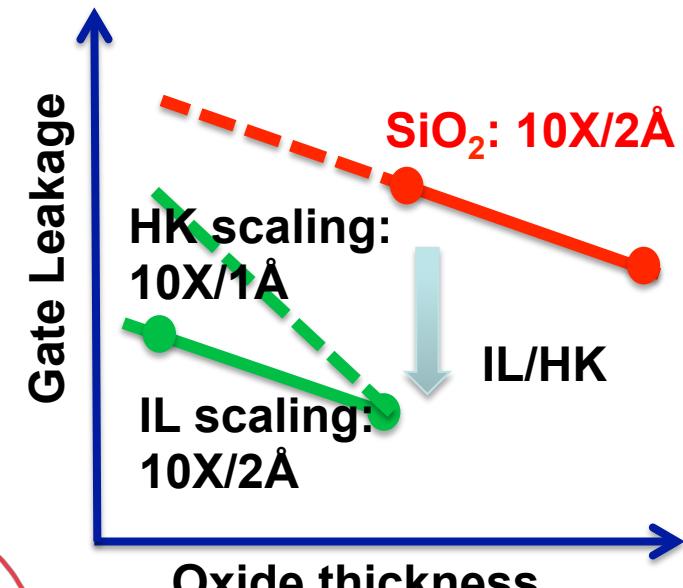


Increase in gate leakage, static power consumption *as we lower top*

Use of high-k gate dielectric (higher physical thickness, lower electrical thickness)
ensure less tunneling *more gate control*

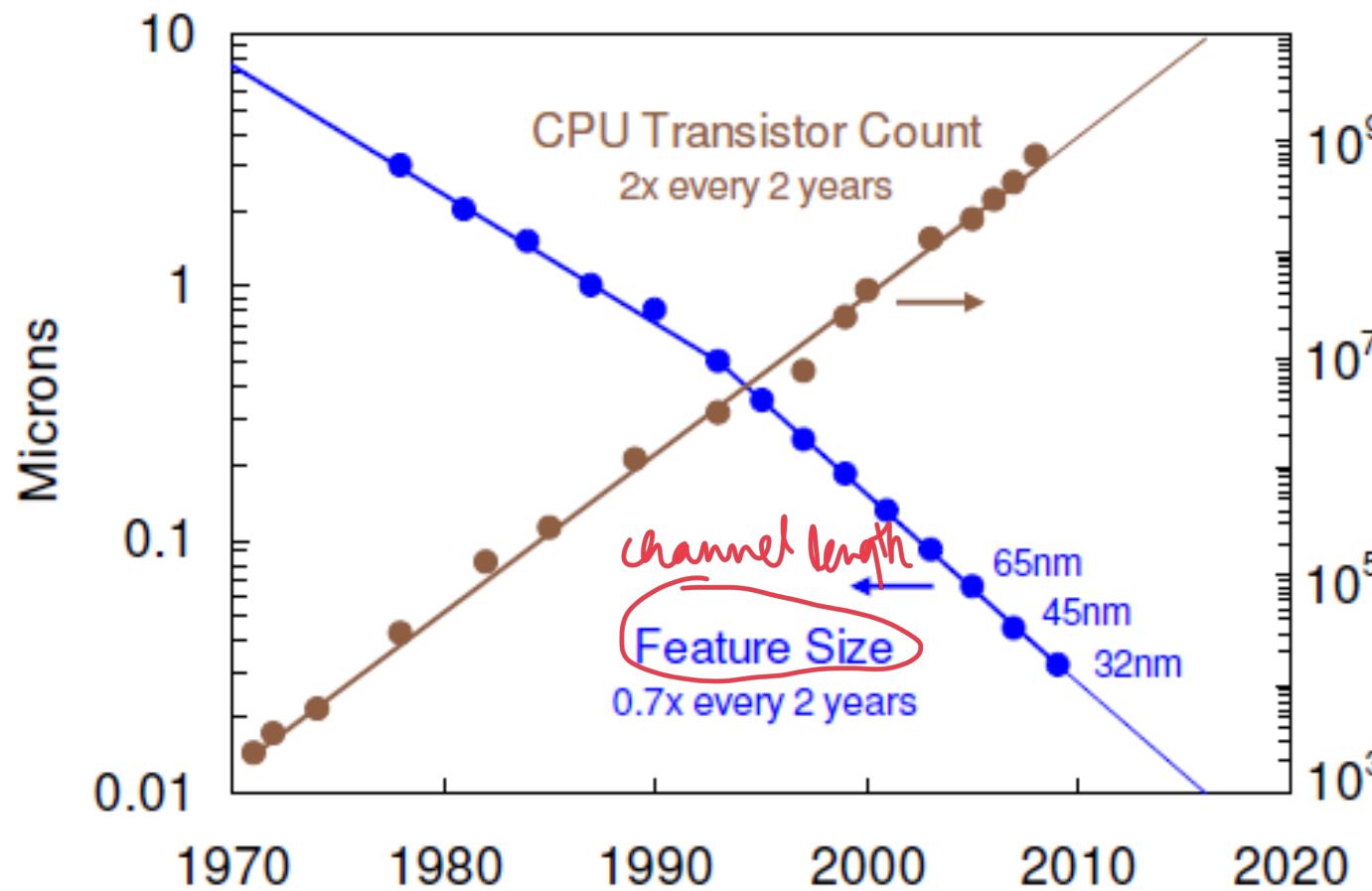
If only HK is used
Poor quality, need SiO_2 interlayer (IL), limits thickness scaling

HKMG: Thickness scaling can only be achieved by IL scaling

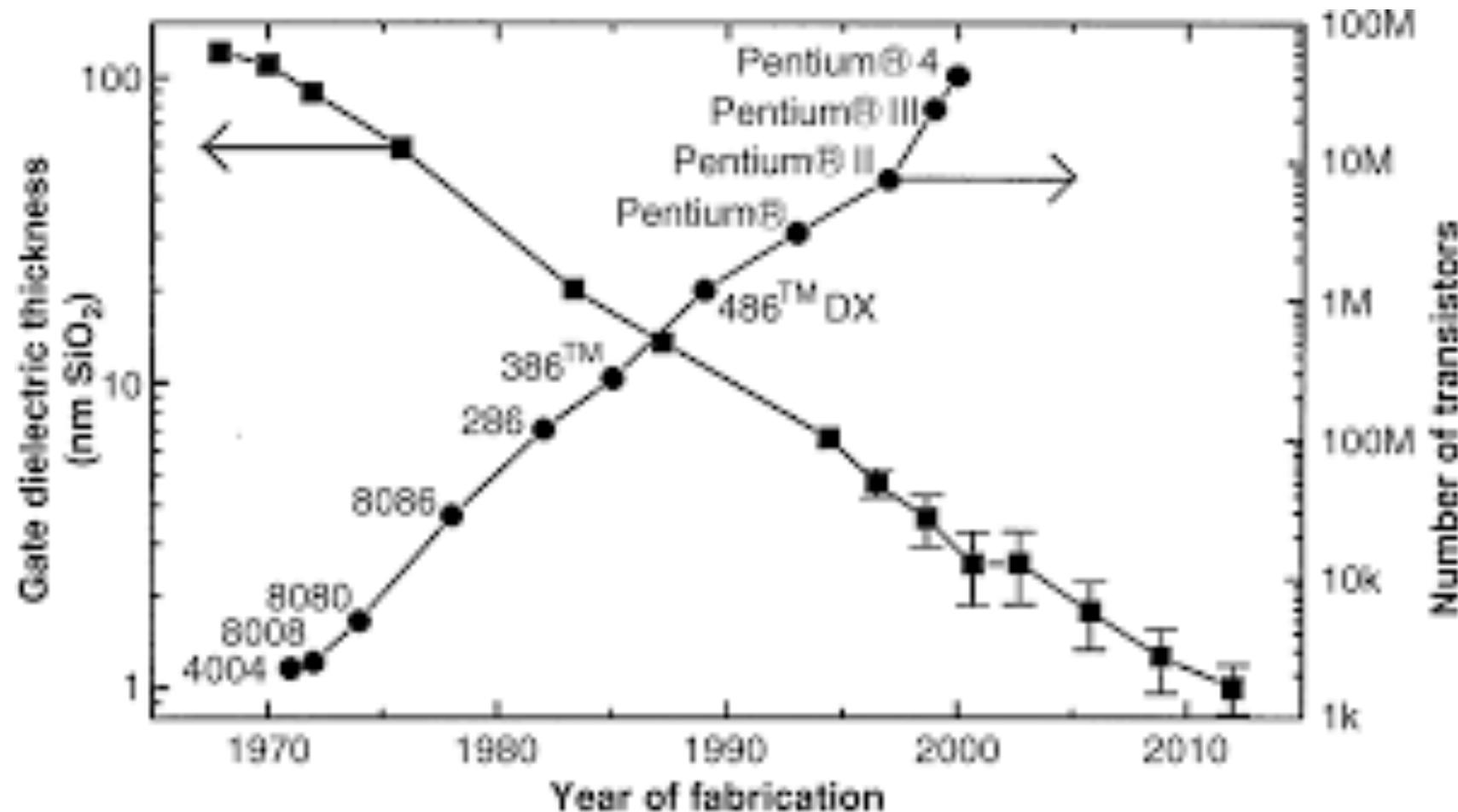


Recap: Channel Length Scaling

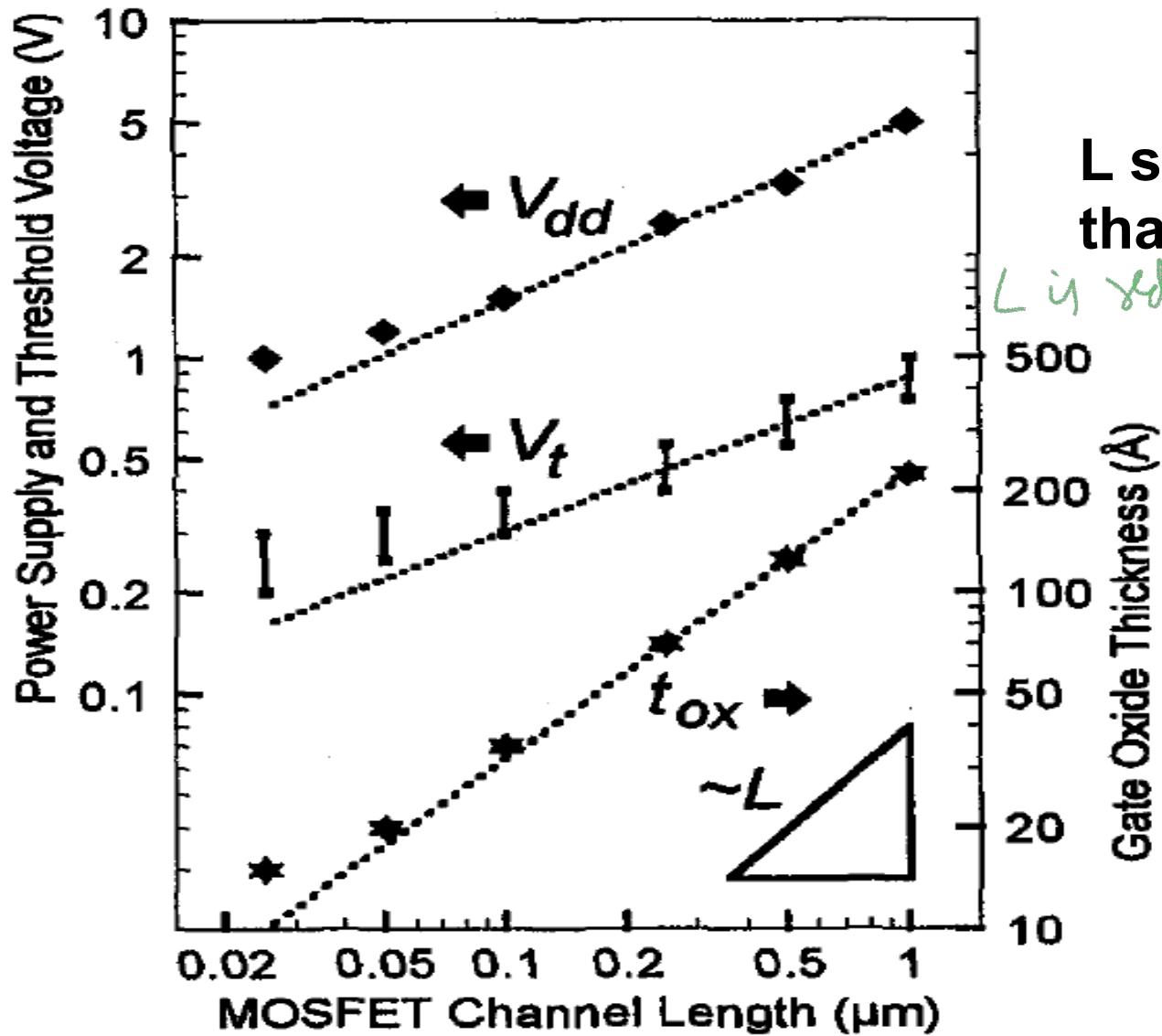
Exponential increase over the last ~40 years



Gate Oxide Scaling



Scaling of Dimensions and Biases



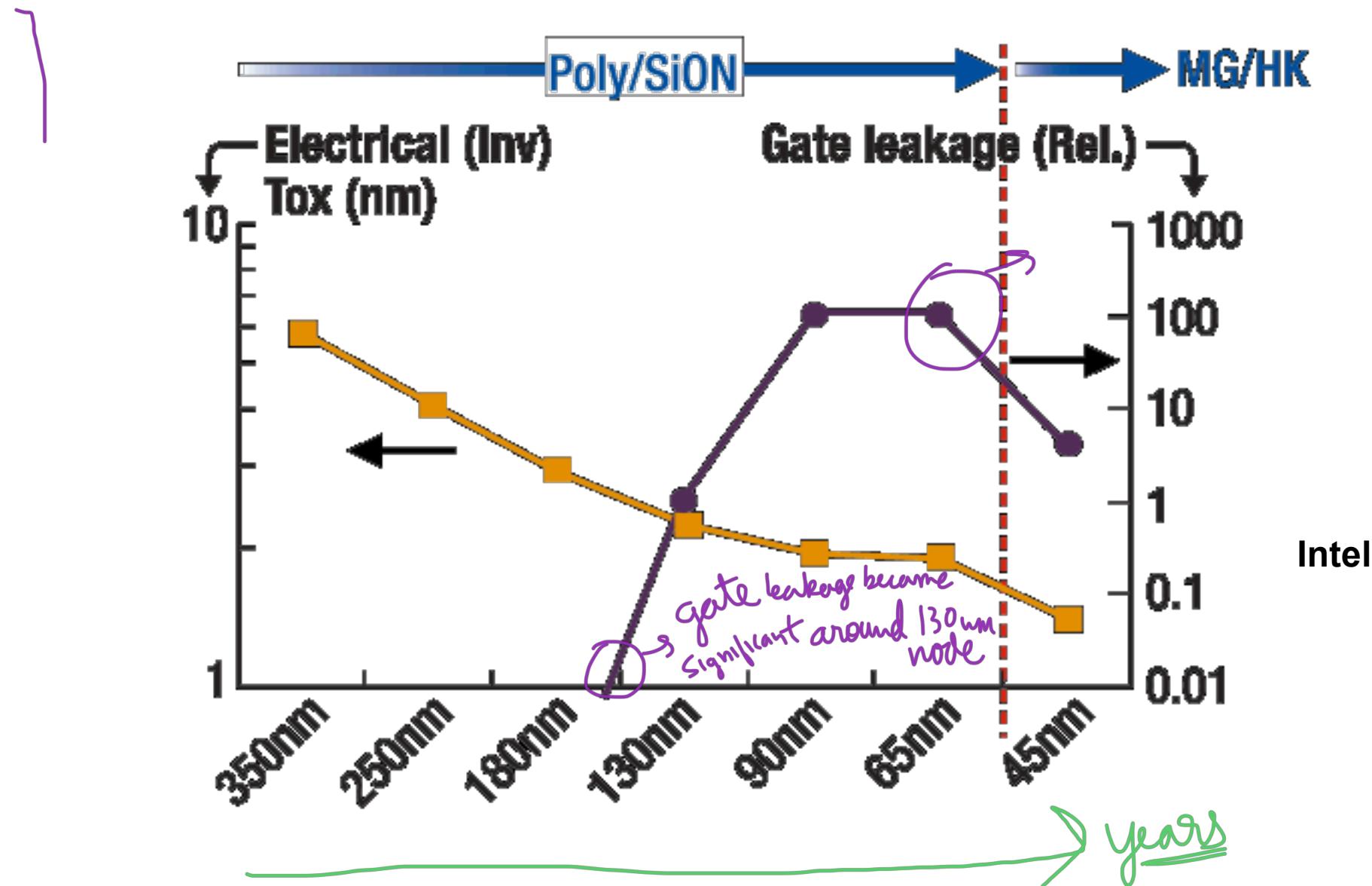
L scales much more than other quantities

L is scaled by 50 while period is constant.

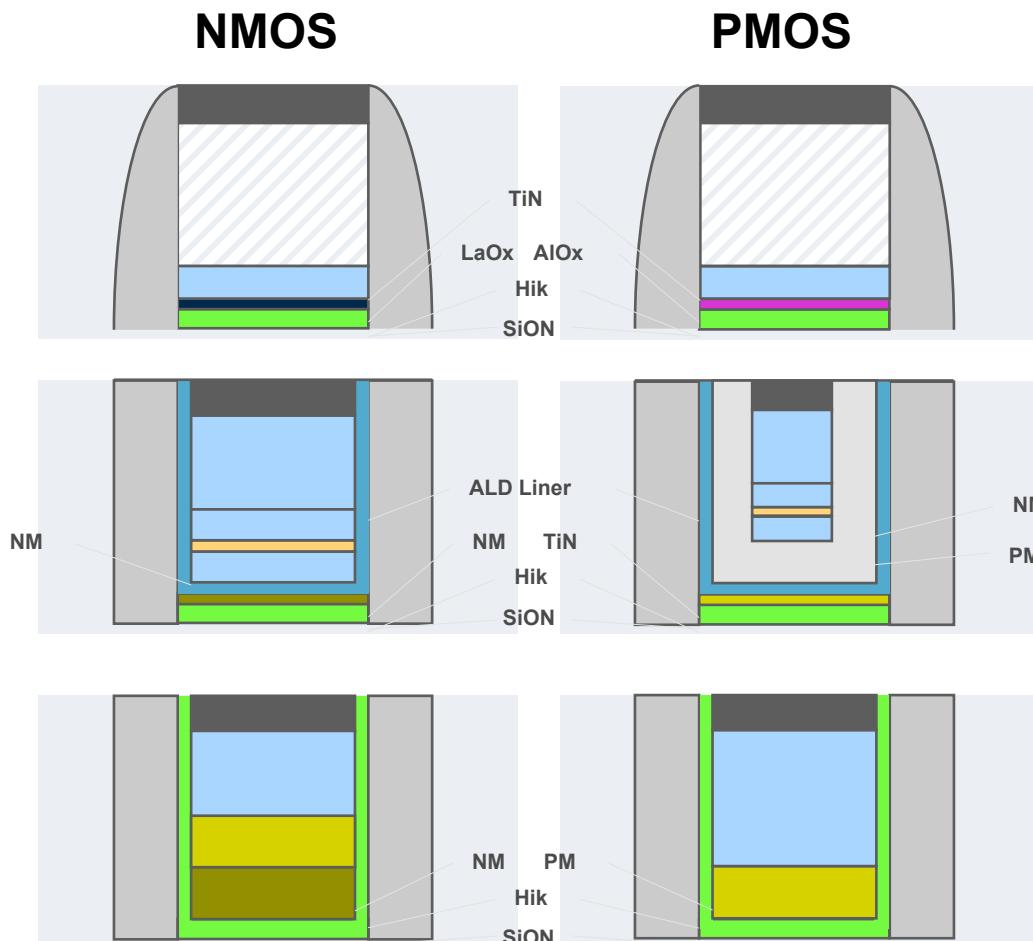
$$\begin{aligned}V_{dd} &\rightarrow \frac{1}{5} \\V_t &\rightarrow \frac{1}{2.5} \\t_{ox} &= \frac{15}{200} \approx\end{aligned}$$

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Gate Oxide Scaling and Leakage



HKMG Gate Insulator Stack

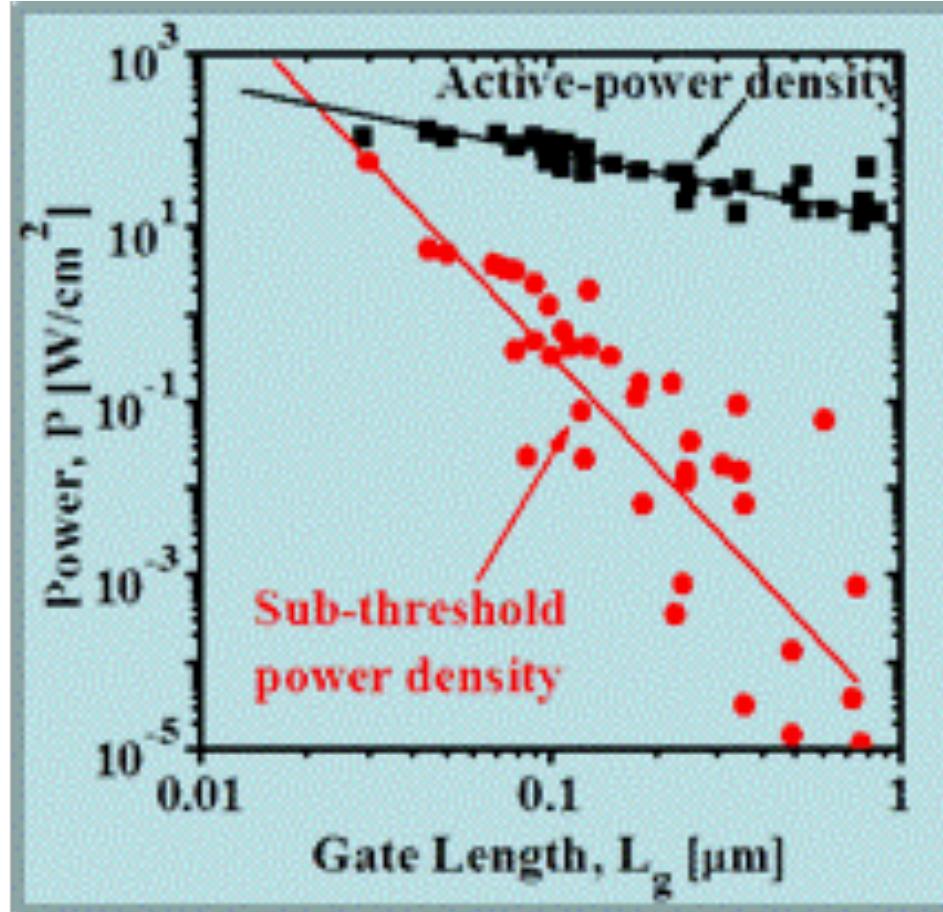


Gate First, S/D afterwards

**Gate oxide first, S/D then,
Gate Metal afterwards**

**S/D first, full
gate stack afterwards**

Scaling – The Power Problem

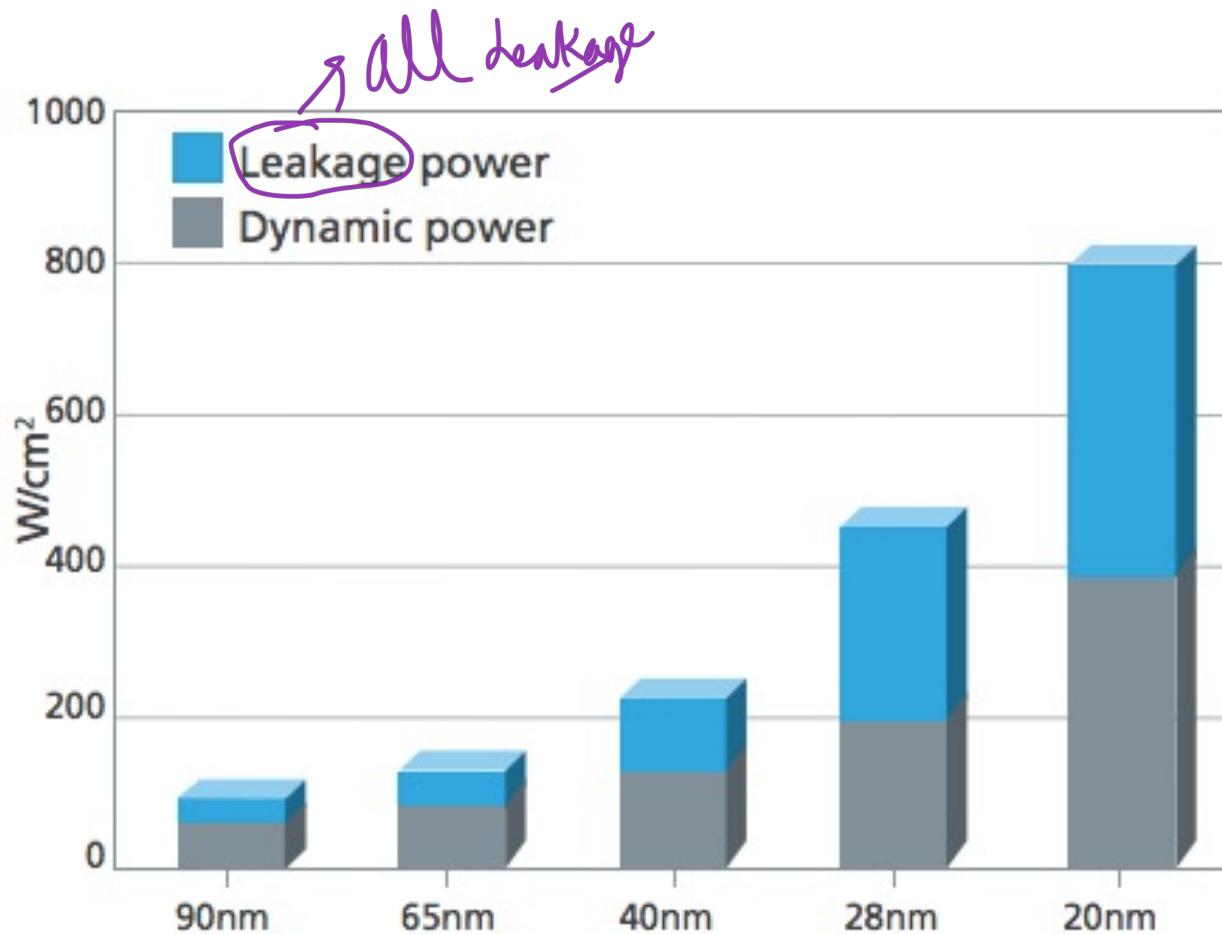


Intel

Leakage (idle) power becoming equal to dynamic (active) power with technology scaling

not good

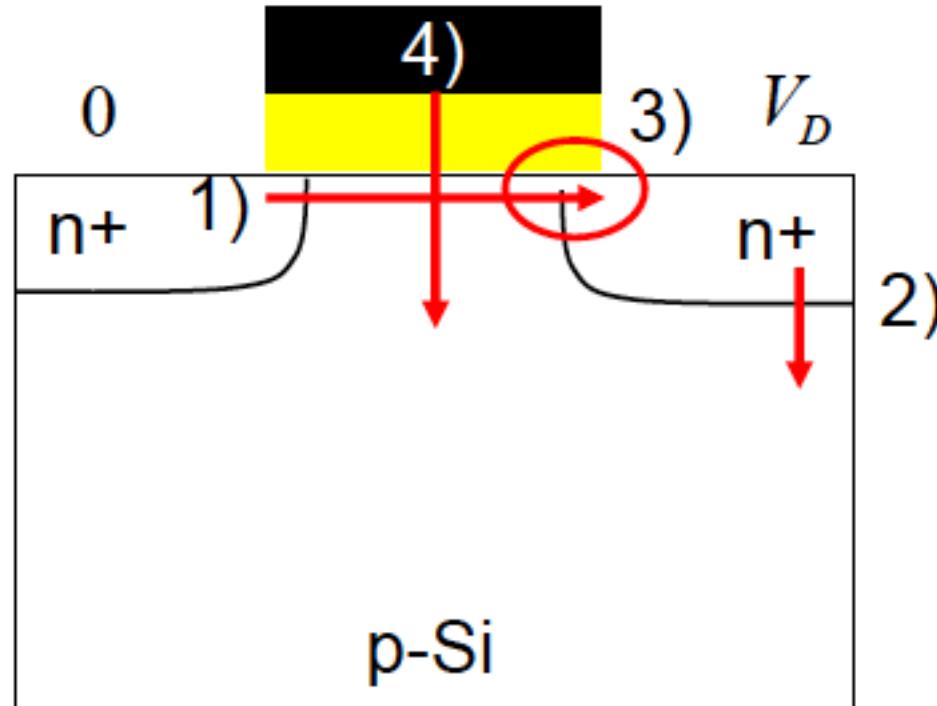
Scaling – The Power Problem



Source: IBS

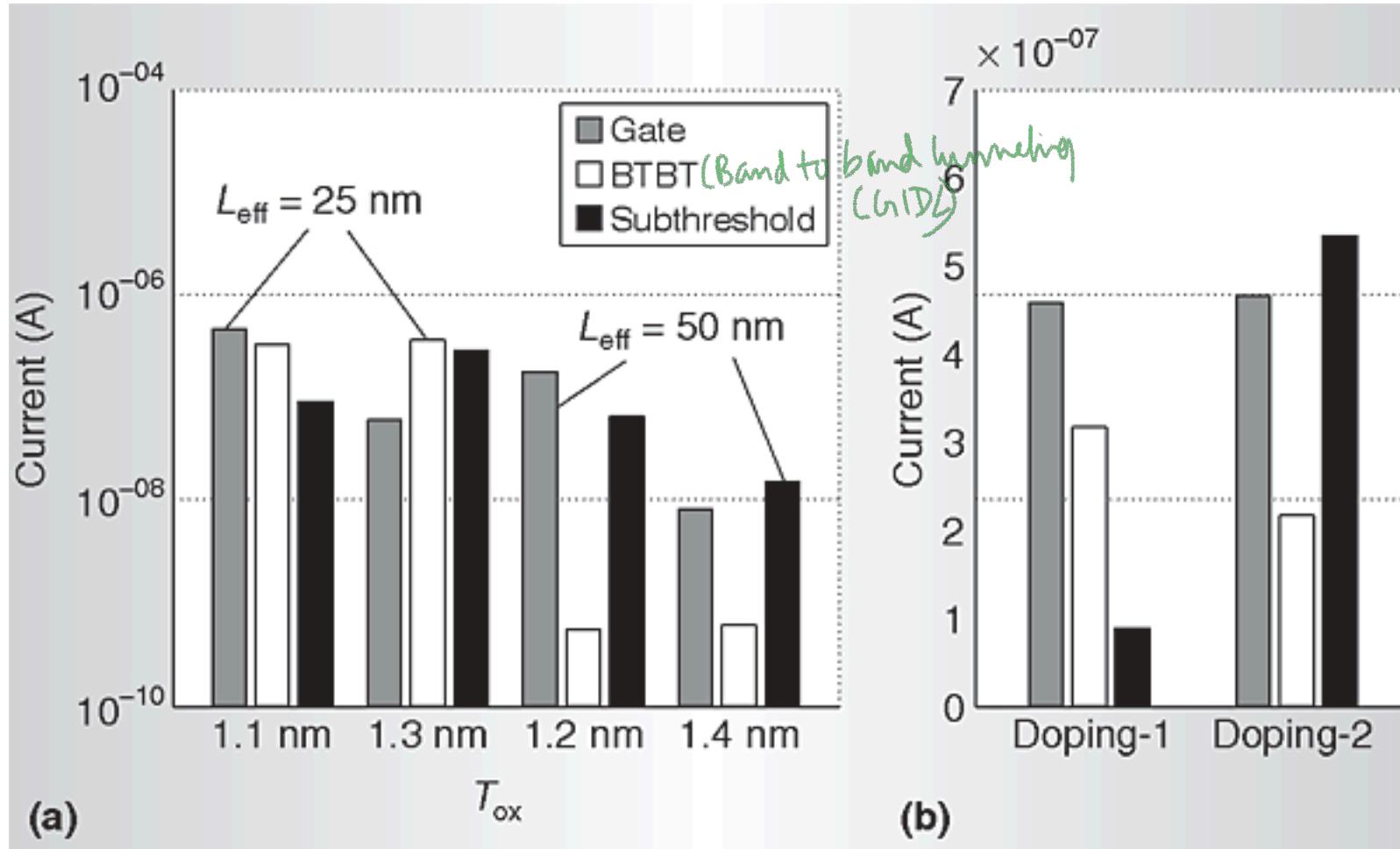
Leakage (idle) power becoming equal to dynamic (active) power with technology scaling

Different Leakage Mechanisms



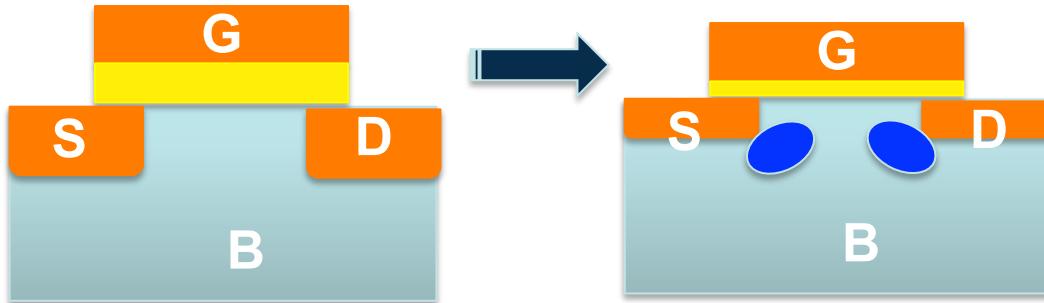
- 1) subthreshold current
- 2) junction leakage
- 3) gate-induced drain leakage (GIDL)
- 4) gate-leakage

Different Leakage Mechanisms



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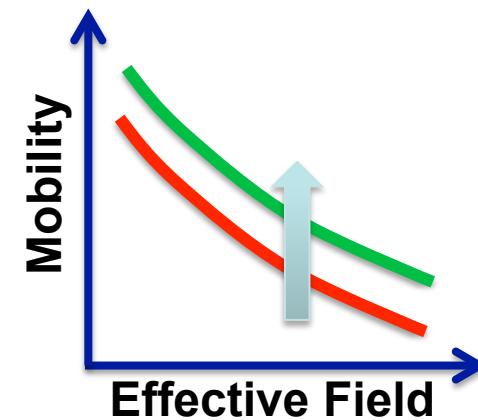
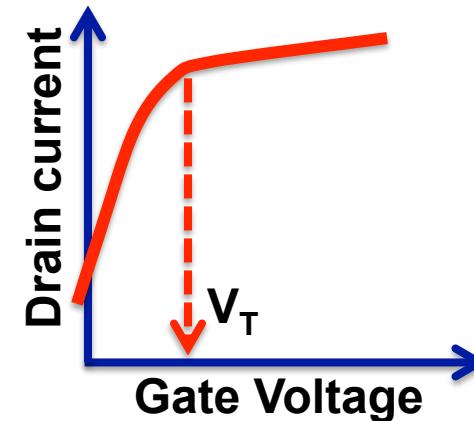
Limitations of Traditional Scaling



**Sub V_T leakage do not scale:
Difficult to reduce V_T with scaling L**

**Supply V_{DD} does not scale to
maintain overdrive ($V_G - V_T$)**

**Increase in lateral field ($\sim V_D/L$),
vertical field ($\sim V_G/L$), reduction in
mobility (μ) – ON current suffers**



**Use strain to
boost mobility**

Drain Current – Impact of Stress

Scaling → increase in E field → reduction in mobility → reduction in I_D

Stress → increase in mobility → increase in I_D

