

MOS Transistor Reliability (Front End)

- A) Overview
- B) Negative Bias Temperature Instability
- C) Positive Bias Temperature Instability
- D) Substrate and Gate current
- E) Hot Carrier Degradation (HCD)
- F) Stress Induced Leakage Current (SILC)
- G) Time Dependent Dielectric Breakdown (TDDB)
- H) Variability and stochastic effects
- I) Characterization methods

Reliability and Failure

Reliability: Ability to perform a given task at a given performance level over a given period of time

Failure: When the above is not met!

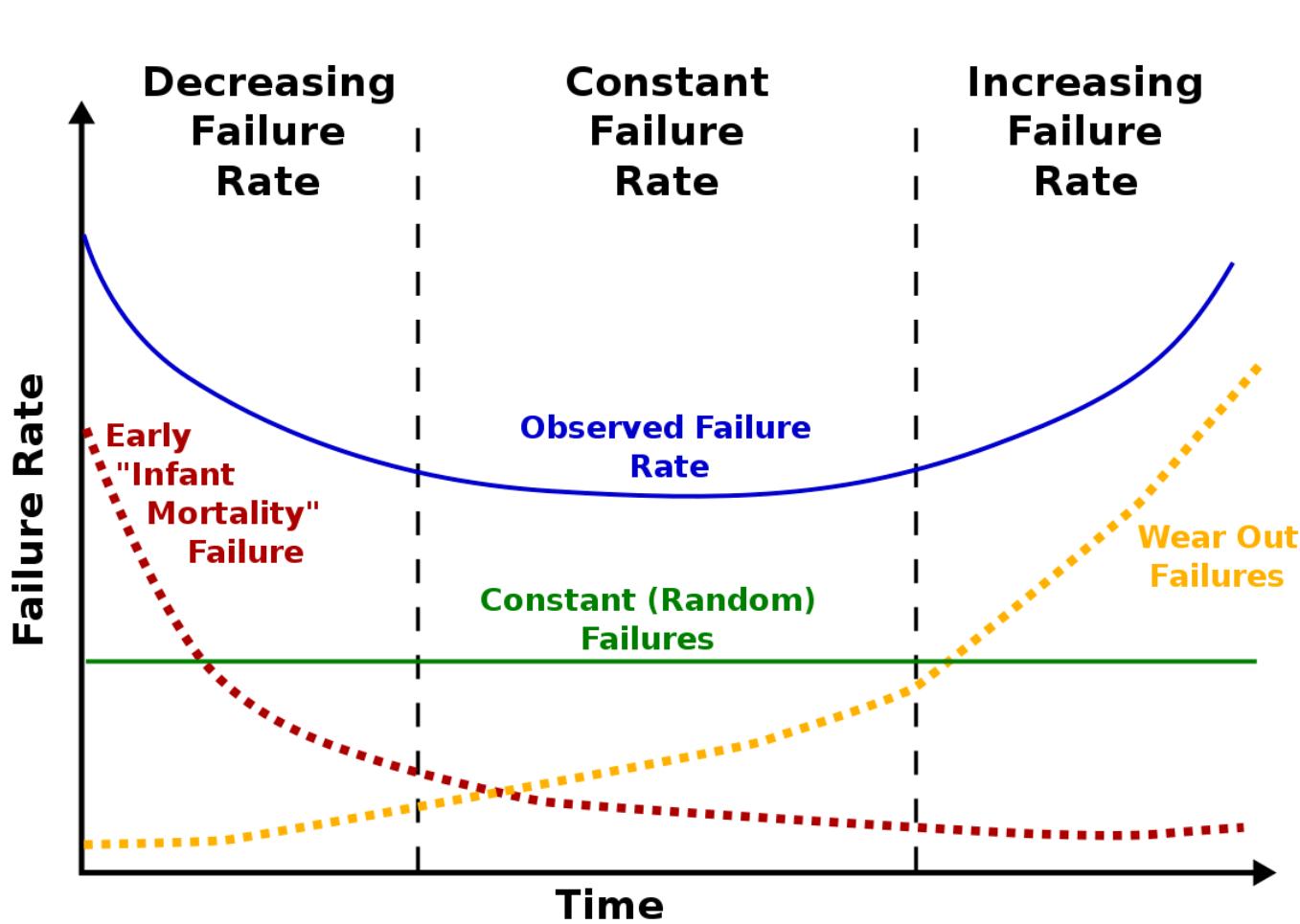
Example:



**Electronics
chips /
systems can
go anywhere,
so better be
safe than
sorry!**

Reliability Bathtub Curve

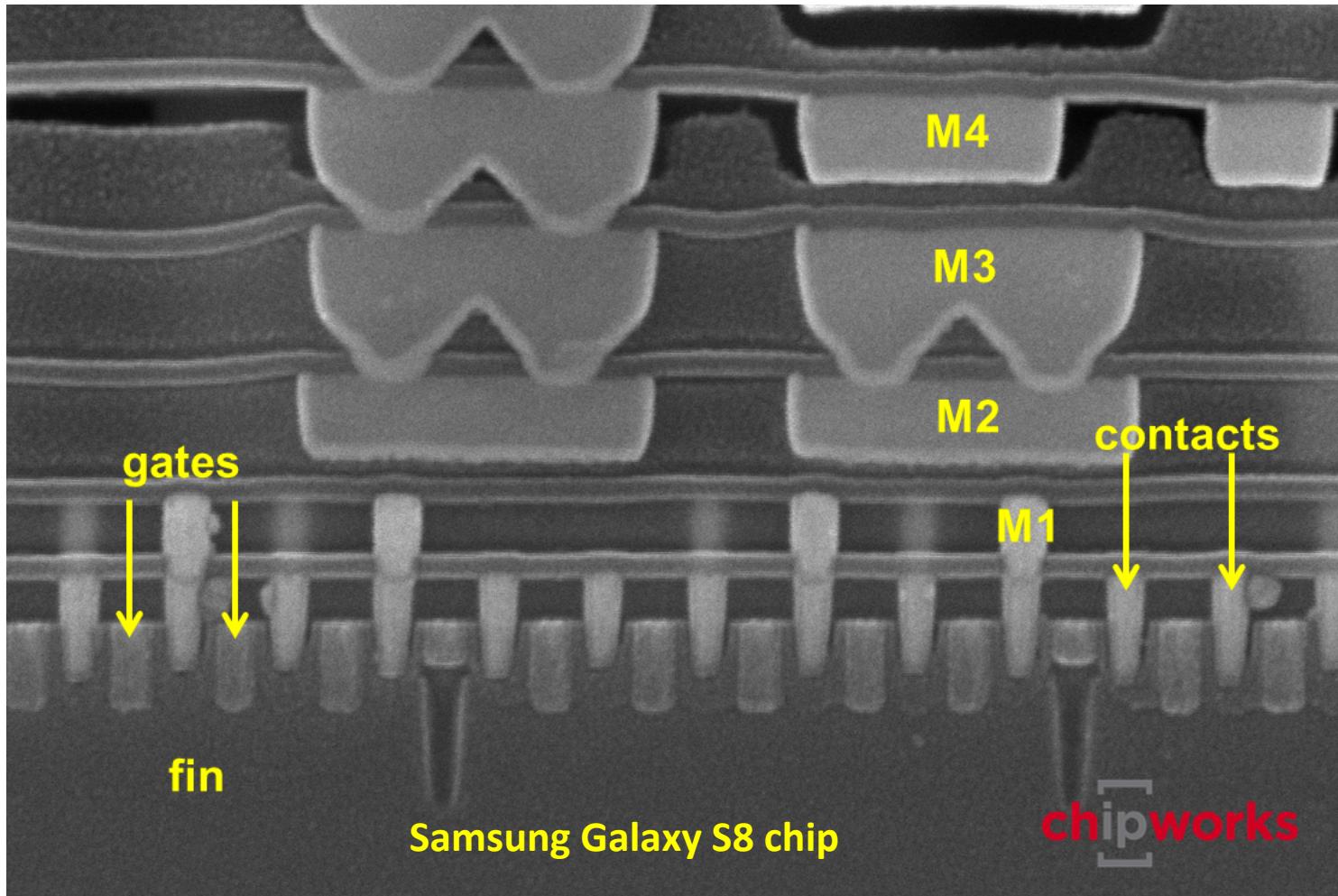
Different processes impact reliability / failure



Wiki

CMOS Chip

Any one can fail: Front End, Middle End, Back End



Role of a “Reliability” Engineer

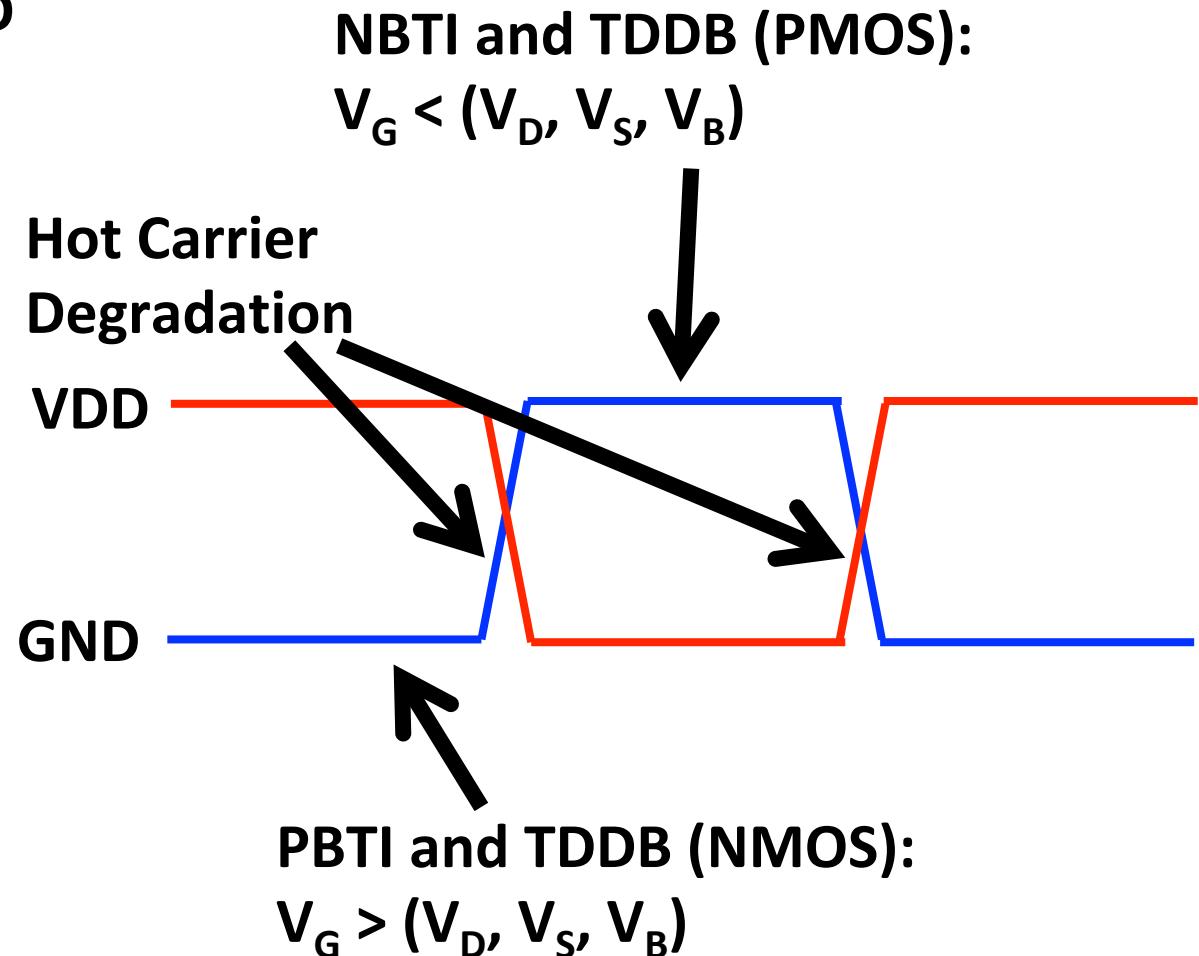
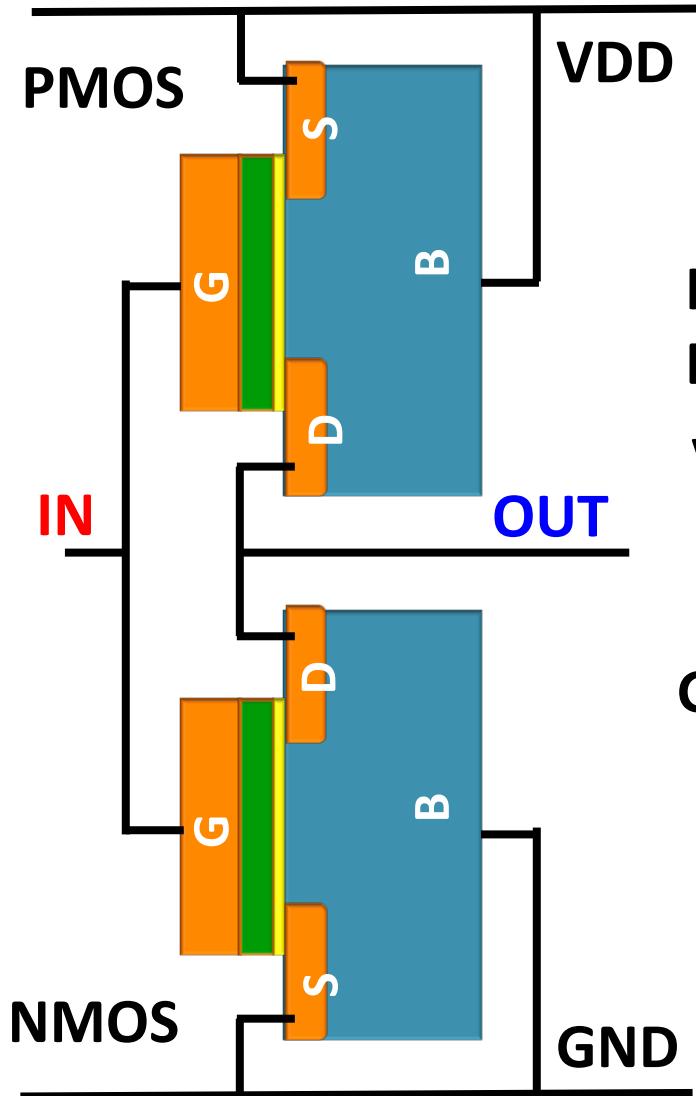
Identify “worst case ageing / failure” mode

Accelerate “degradation” and test “impact”

Make sure “no other unwanted modes” get into play by virtue of acceleration

Build models / methods to project → End of life, use profile

Degradation Modes



Historical Timeline

~1970 → First observation of NBTI (PMOS only circuits)

~1980 → NMOS only circuit, no NBTI, HCD became important

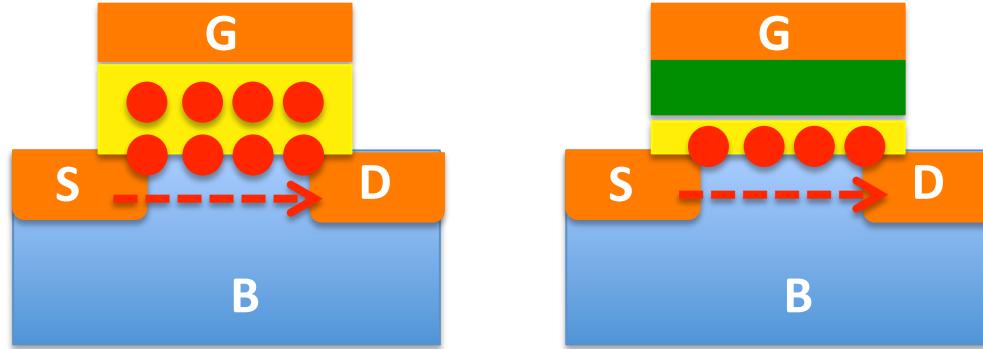
~1990 → CMOS, voltage scaled, drain profile changed (LDD), HCD reduces, TDDB became important

~2000 → Voltage scaled, SiON technology, NBTI became important, TDDB became less of an issue

~2005 → HKMG, both NBTI and PBTI became important, but subsequently PBTI issue went away (now)

~2012 → FinFET, NBTI an issue, HCD became important, Self Heating Effect

Negative Bias Temperature Instability



Degradation of
drain current

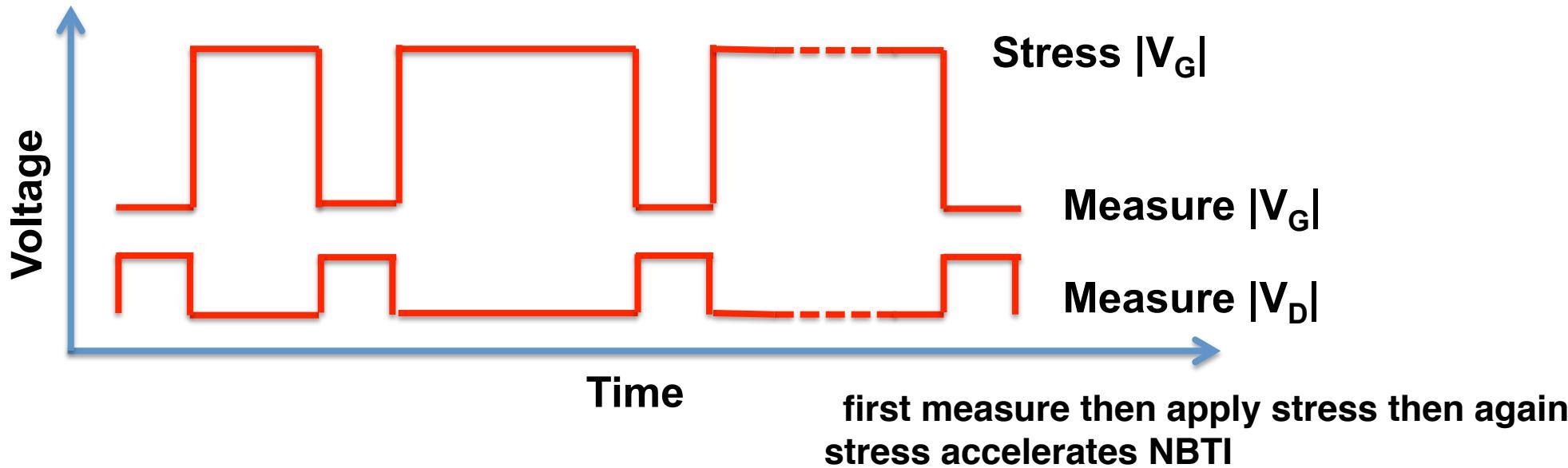
Uniform degradation, observed for SiO_2 (less), SiON and HKMG (SiON/HfO₂) gate stacks

Positive charges at channel/oxide interface and oxide bulk
(SiO_2 / SiON interlayer for HKMG) \rightarrow Negative V_T shift

Presence of transconductance (g_m) degradation

Nbt shows Gm degradation

NBTI Measurement (MSM Method)



Measure – Stress – Measure method

Stress at higher (than nominal) V_G to accelerate NBTI

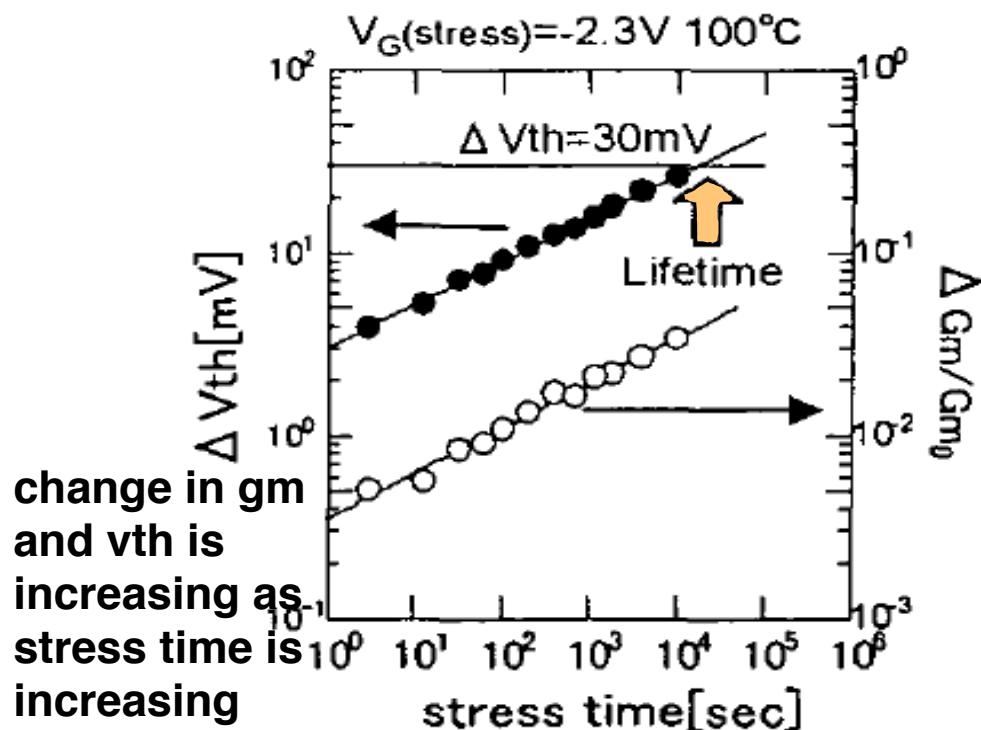
Interrupt stress (in log-uniform intervals) to measure drain current (one V_G , or I_D versus V_G sweep)

NBTI Measurement

ss subthreshold slope

Find parameter (e.g. V_T , gm , SS) from I-V measurements before and after stress (during interruptions)

Calculate parametric shift = Post – Pre; Plot versus time



Usually plotted in a log-log scale, power law time dependence

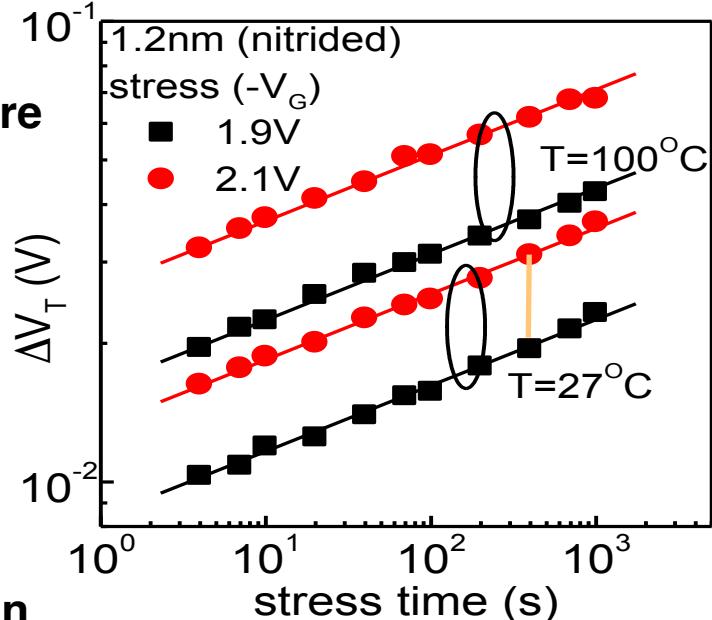
Lifetime = Time to reach a particular value

more stress more shift and we cant accomodate for too drastic change in vth

Kimizuka, VLSI'00

Parametric Shift

see the vt is higher at higher temperature



the change in delta vth has also increased(y axis is in log scale)

Varghese, IEDM'05

Shift increases with bias (more negative) and temperature

Time: Power-law Exponent n

Pre-factor (~ quality)

$$\Delta V_T = A * V_G^\Gamma * e^{-E_A/kT} * t^n$$

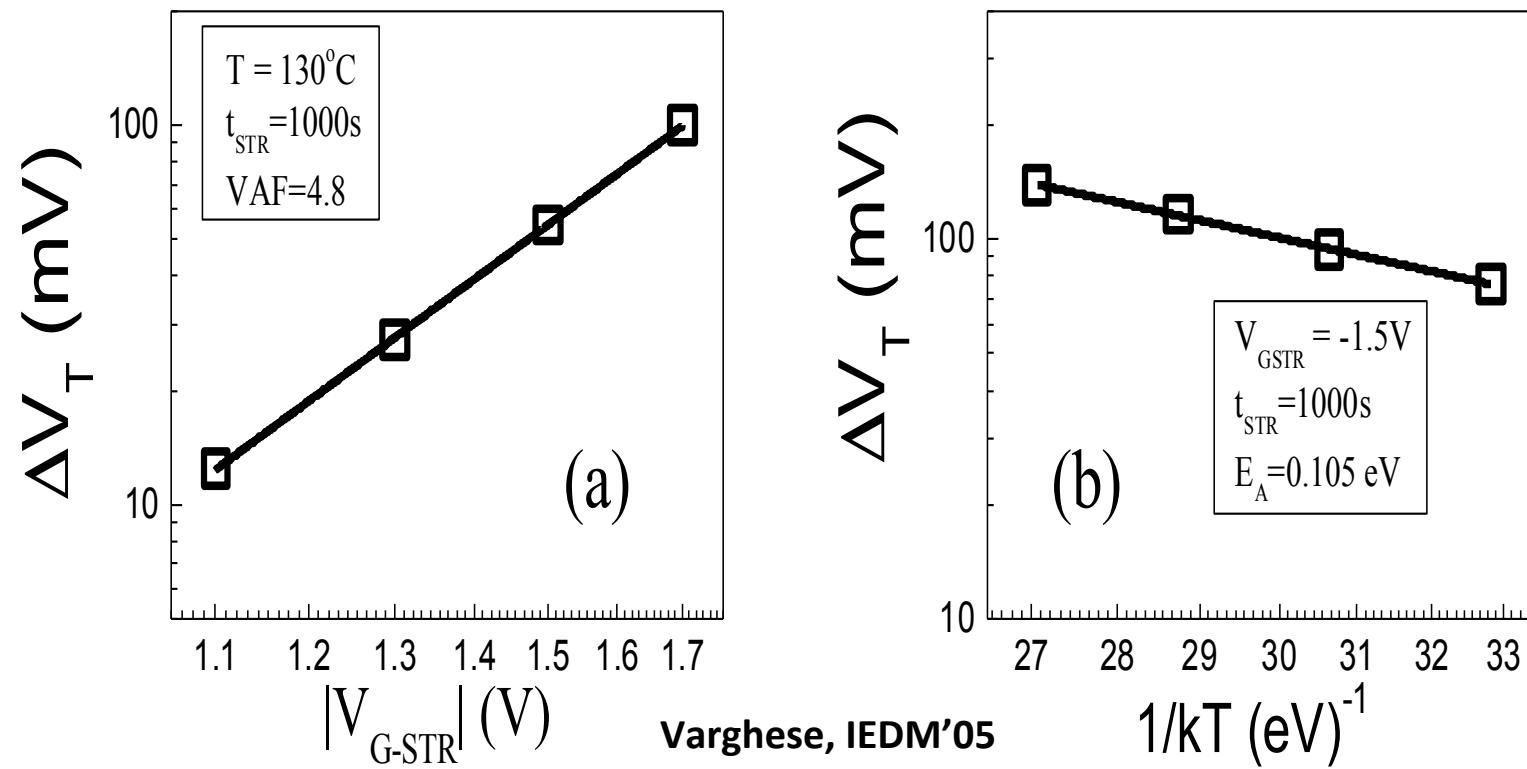
Voltage: Power-law Voltage Acceleration Factor (VAF)

Temperature: Arrhenius Activation, Energy E_A

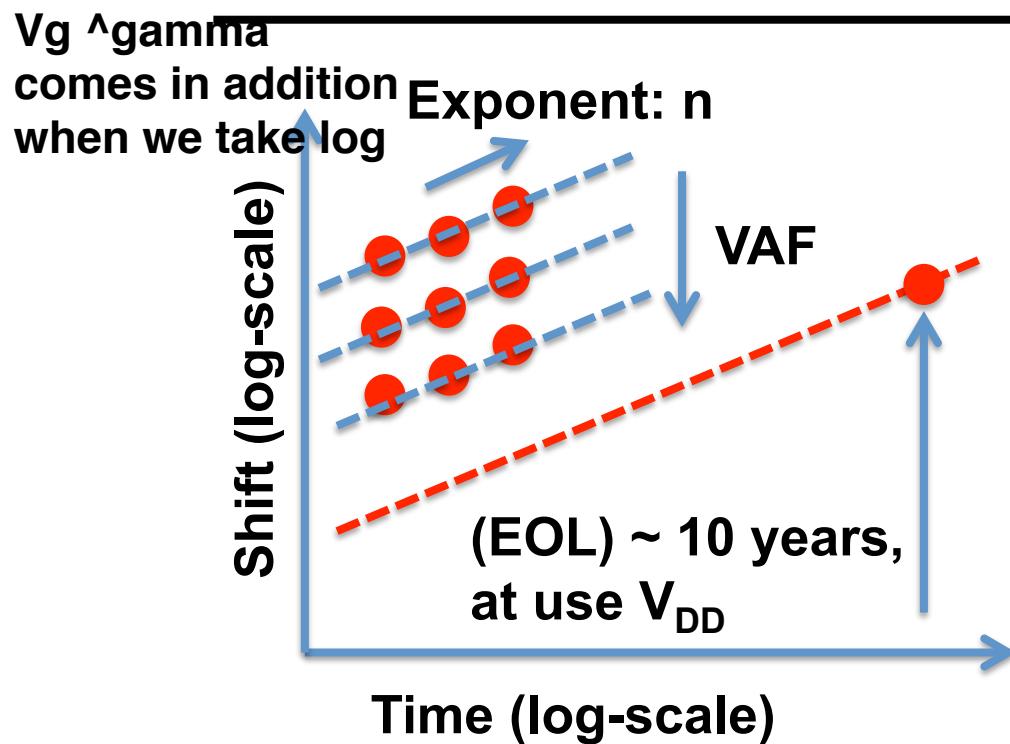
Voltage and Temperature Dependence

Power law plot of fixed time degradation versus stress voltage at a fixed T → Slope is VAF

Arrhenius T dependence → Activation energy (E_A)



Lifetime Determination



** varies,
~ hours (wafer)
~ weeks / months (package)

Fix Temperature

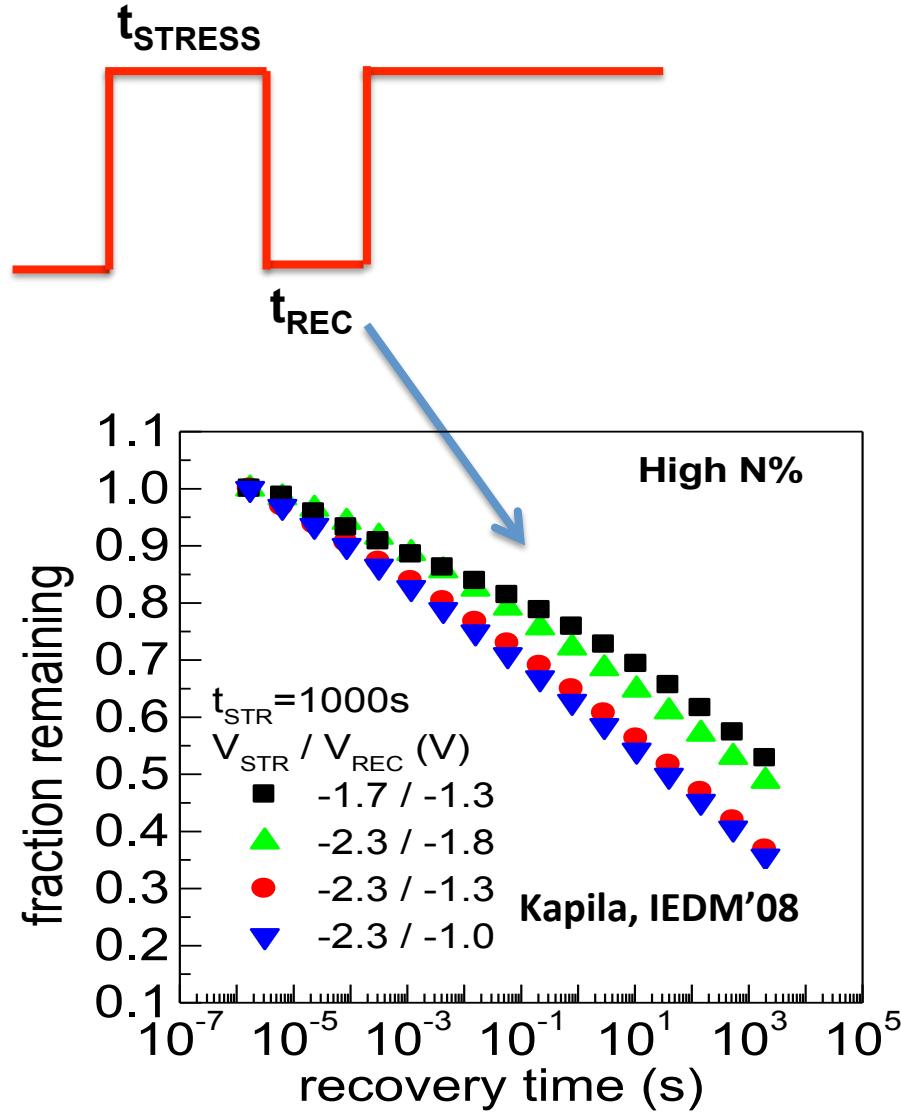
Measure degradation at
accelerated V_G stress, shorter
time**

Repeat for several stress V_G

Extrapolate to use V_G and end
of life (EOL) → use parameters
 Γ and n

Repeat at different
temperature, if needed

NBTI Recovery



Recovery of degradation after stress

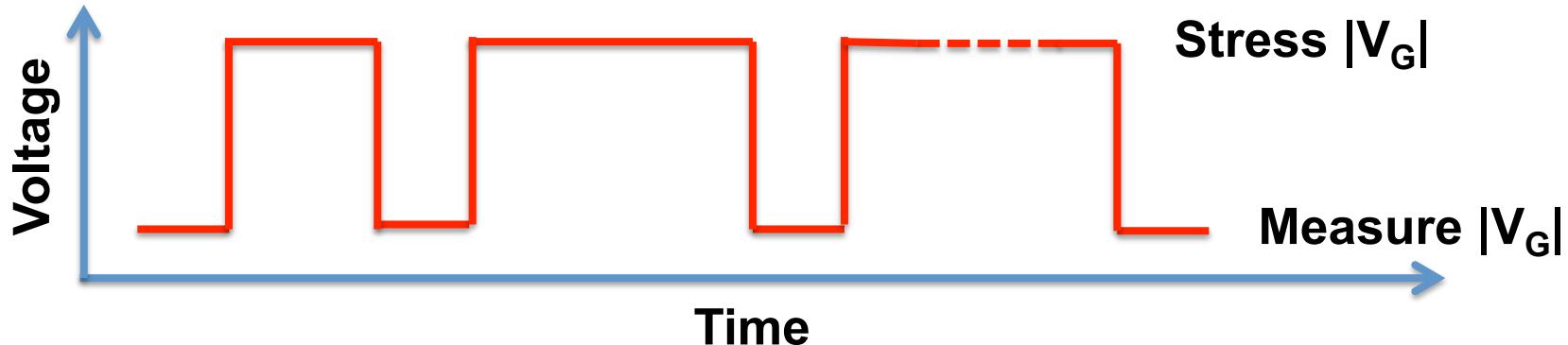
Amount of recovery depends on time, and difference between stress and recovery bias

$$\Delta V_T = \frac{\Delta V_T (EOS)}{1 + k \left(\frac{t_{REC}}{t_{STRESS}} \right)^m}$$

Alam, IEDM'03

Grasser, IRPS'07

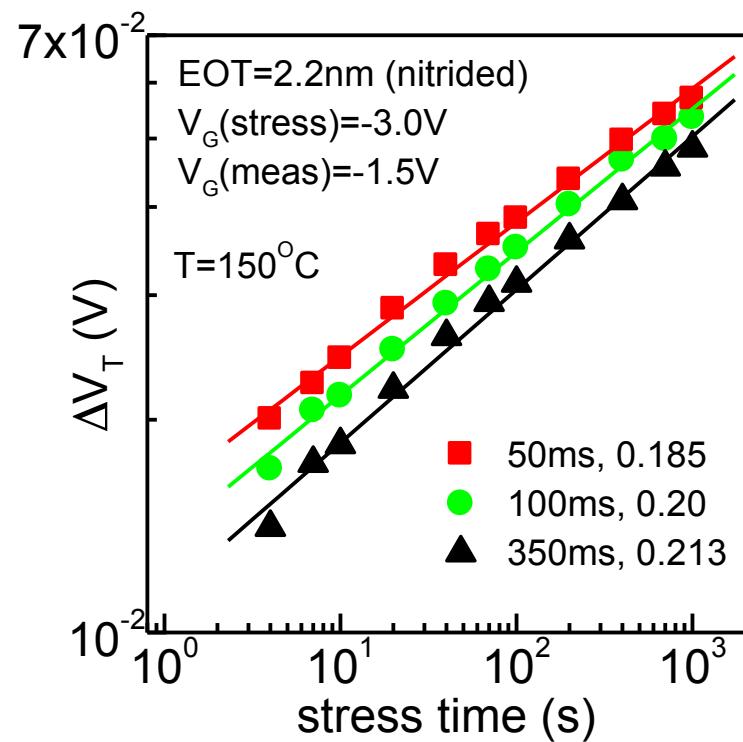
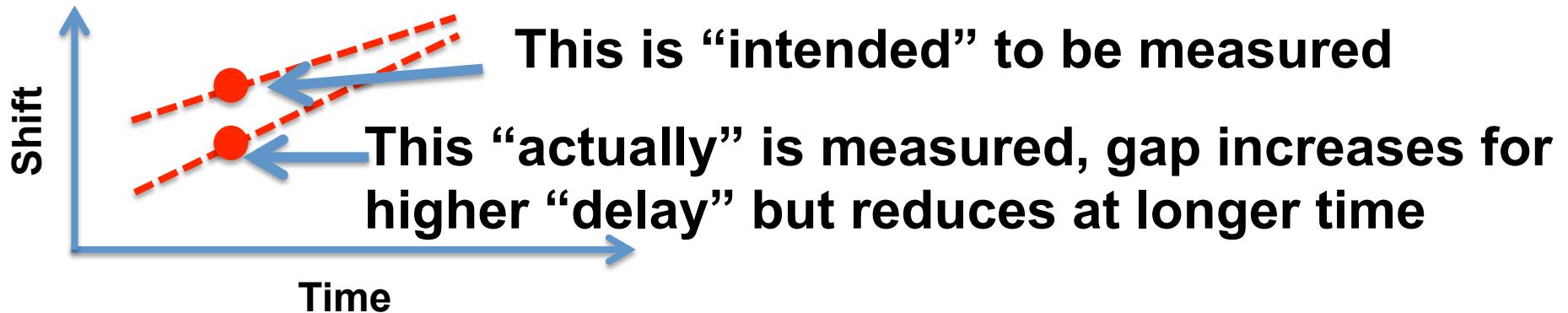
Impact of Recovery (Measurement Delay)



Measurement duration is fixed, stress duration increases exponentially at longer time

Impact of recovery is larger at shorter stress time (high recovery / stress time ratio)

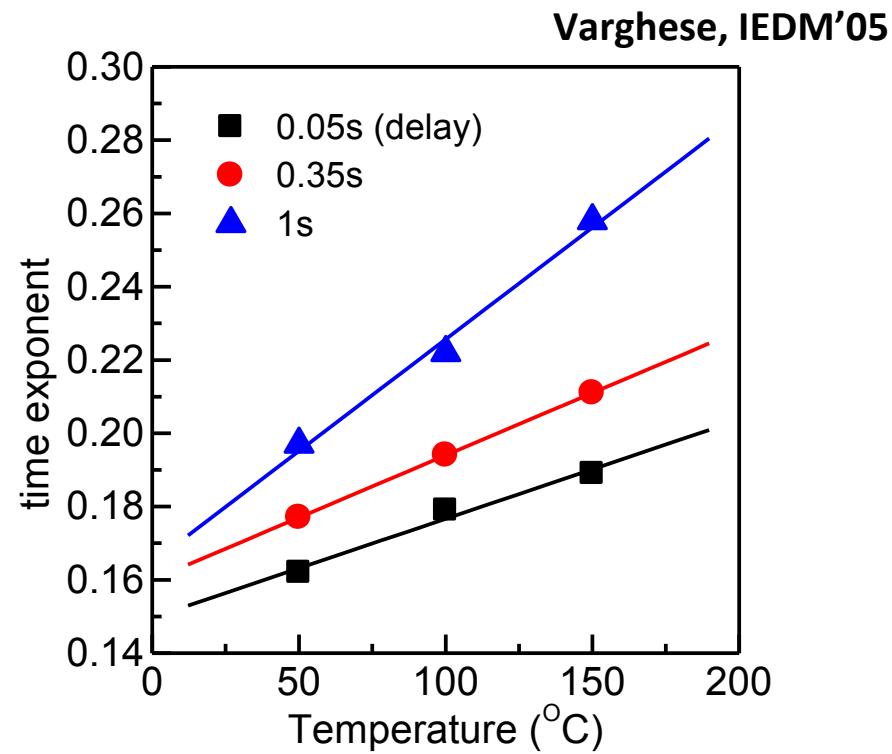
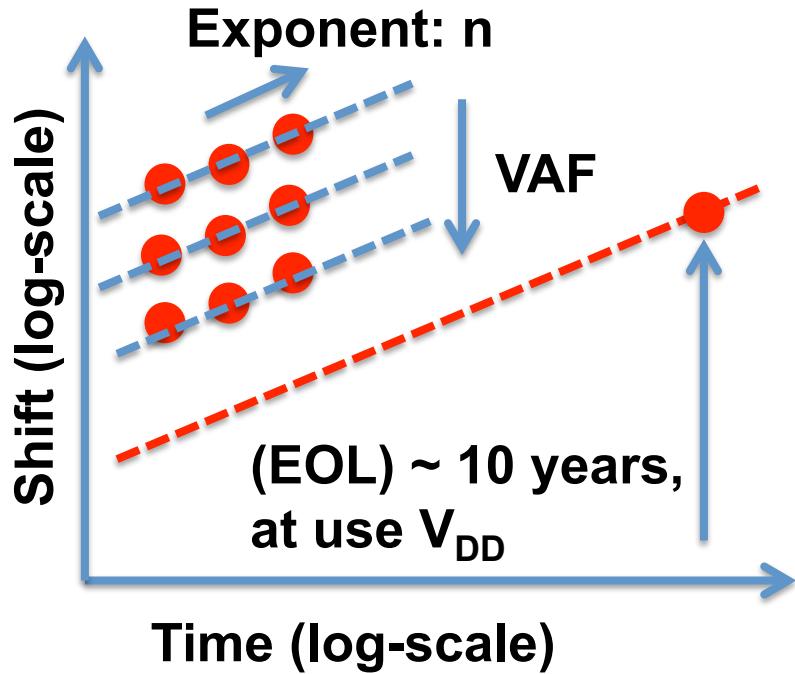
Impact of Recovery (Measurement Delay)



Lower degradation magnitude and higher time exponent (n) due to delay

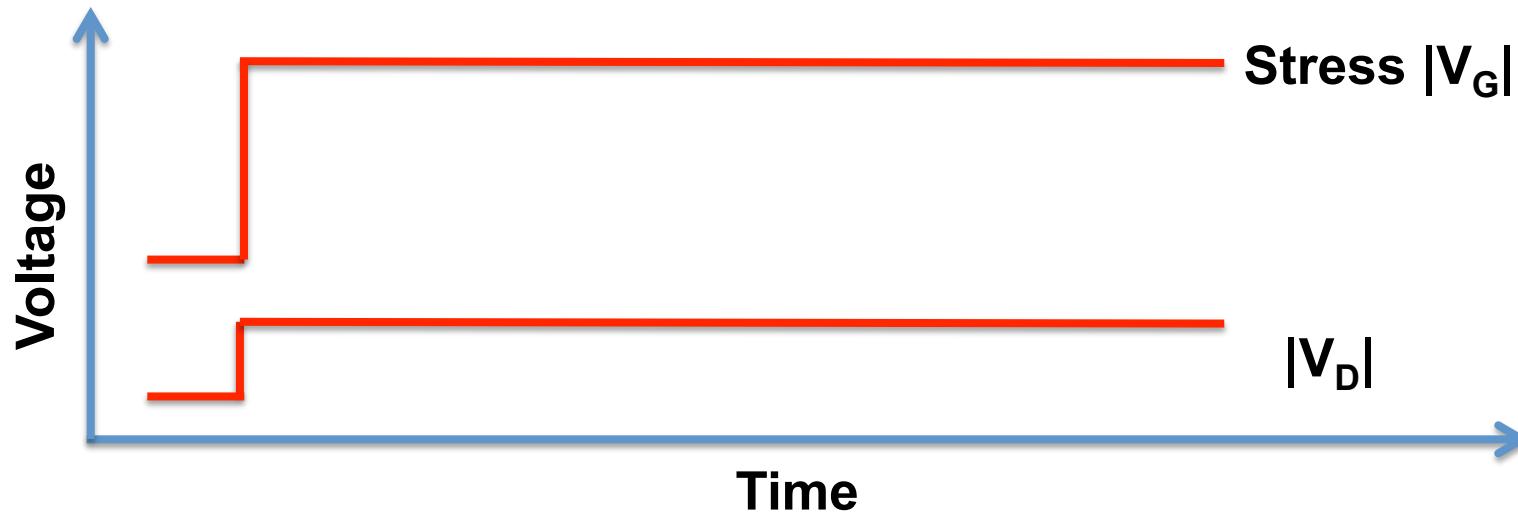
Varghese, IEDM'05

Importance of Measurement Delay



Extrapolation from shorter time stress to end of life depends on time exponent (n), which varies with delay and temperature → Error in extrapolated ΔV_T

NBTI Measurement (OTF Method)

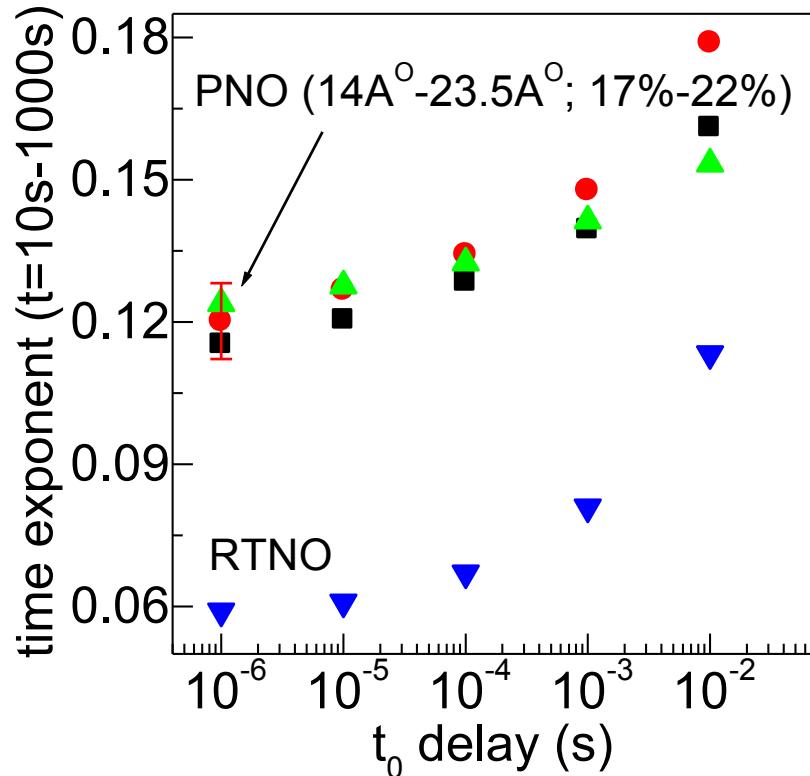


On-The-Fly method

Stress at higher (than nominal) V_G to accelerate NBTI

Do not interrupt for measurement, monitor drain current,
assume first data point as un-stressed (~ measurement
delay)

How Fast is Good Enough?



In MSM the graph of time exponent and to delay was straight line

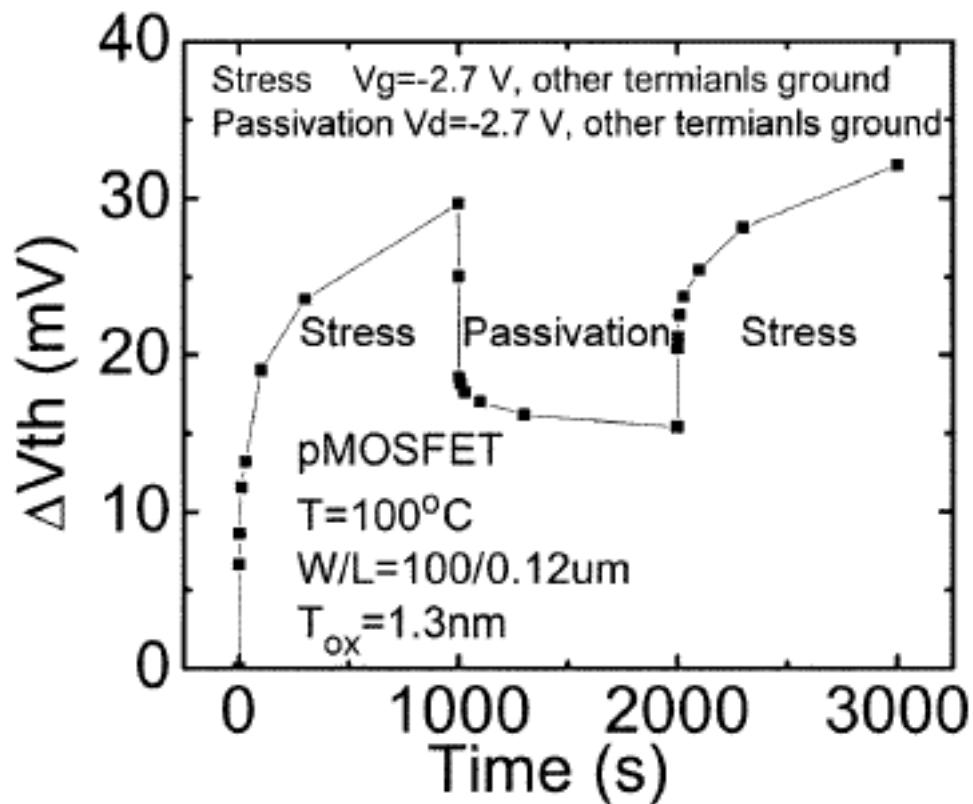
OTF method: slope reduces at lower delay (less impact), ~ $10\mu s$ or lower delay is good enough

Different process shows different slope (explained later)

initially the slope looks constant as it in on the fly method the stress is being continuously applied so it will take some time to show its result

Dynamic (AC) NBTI

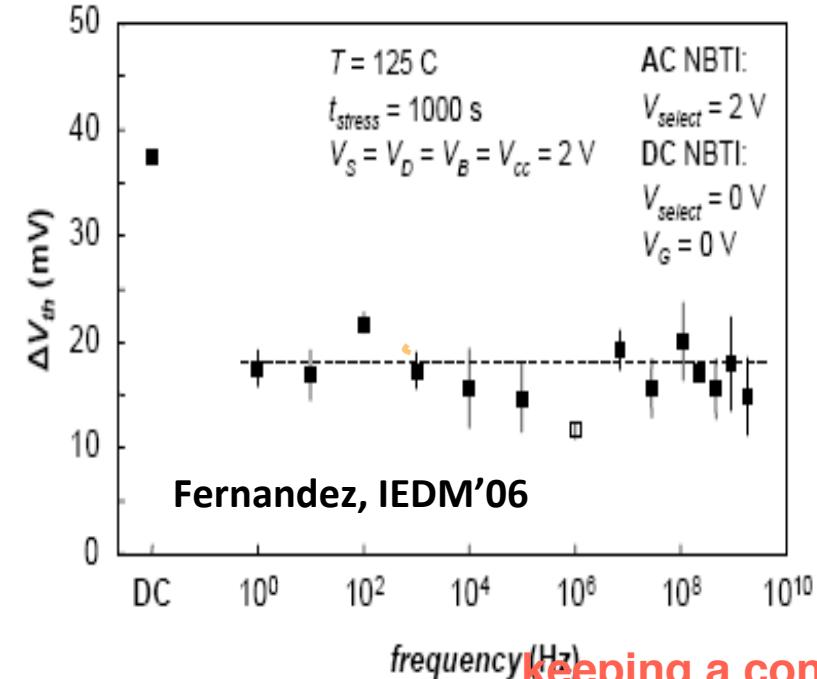
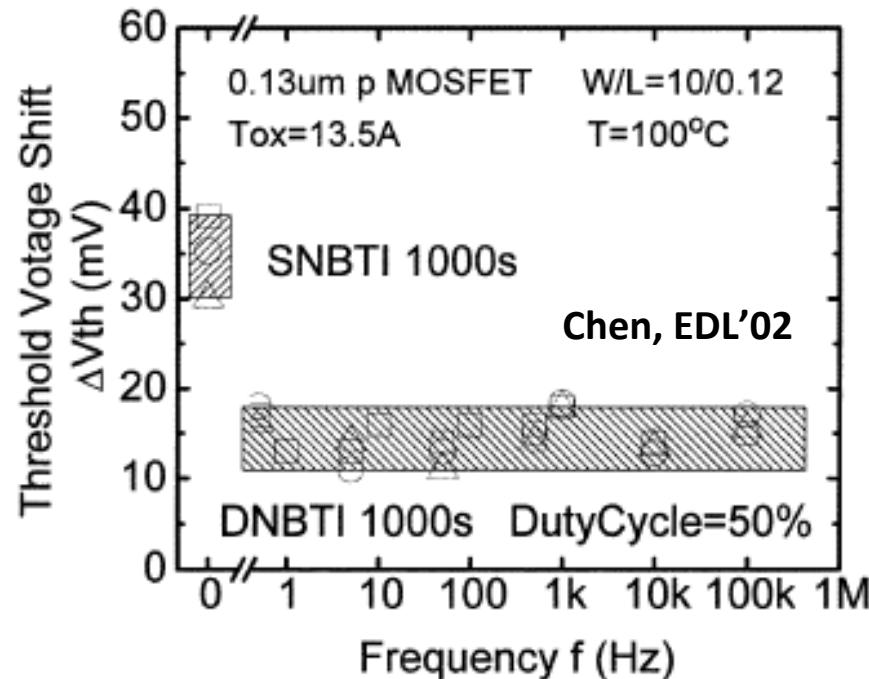
Digital circuits operate under AC → Reduction in ΔV_T



Stress: $V_G = 0$,
 $(V_D, V_B, V_S) = V_{DD}$
Hence: $V_G < 0$, others
grounded

Passivation: $V_D = 0$,
 $(V_G, V_B, V_S) = V_{DD}$
Hence $V_D < 0$, others
grounded

NBTI Frequency Independence



Device level data at lower frequency

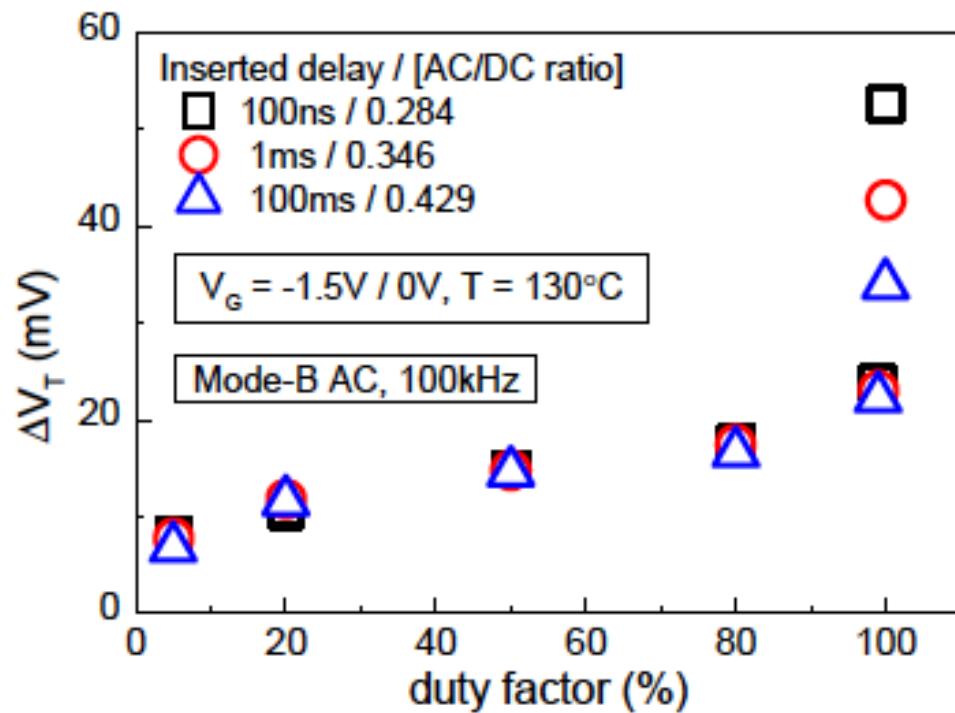
Keeping a constant duty cycle there is no impact on delta vth

Circuit (ring oscillator) data at higher frequency

AC/DC ratio ~ 0.5 (duty cycle=50%), no impact of frequency

NBTI Duty Cycle Dependence

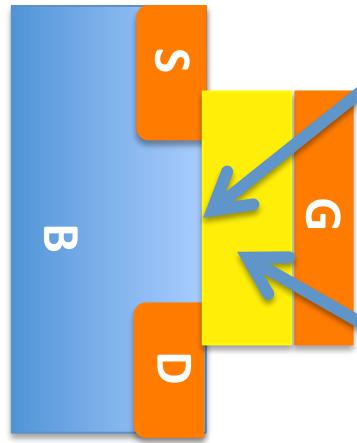
“S” shaped, AC not impacted by (reasonable) delay



Goel, MR'14

$$\Delta V_T = A * (PDC)^k * V_G^\Gamma * e^{-E_A/kT} * t^n$$

The “Physics” of Time Exponent



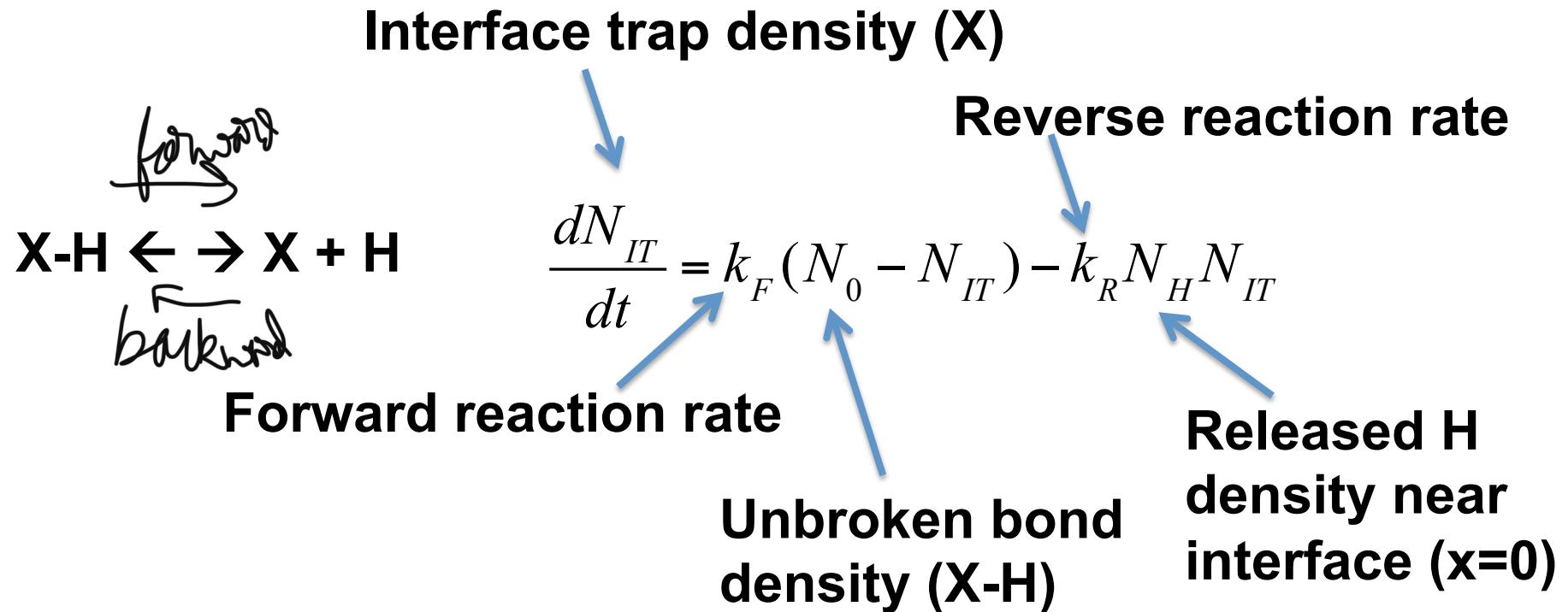
Inversion layer hole, oxide electric field and T assisted breaking of X-H bonds at Si/SiO₂ interface (1): $X\text{-H} \rightarrow X + H$

Diffusion of H, formation of H₂ by reaction with other X-H bonds (2): $Y\text{-H} + H \rightarrow Y + H_2$

X and Y are generated traps (when charged cause device parameter shift), diffusion of H₂ controls long-time slope

Recovery: Back diffusion of H₂, reverse reaction of (2), back diffusion of H, reverse reaction of (1)

Analytical Solution



Principle of detailed balance,
and $N_0 \gg N_{IT}$

$$\frac{dN_{IT}}{dt} \sim 0$$

$$N_H(x=0)N_{IT} = \frac{k_F}{k_R} N_0$$

Details: Alam,
IRPS'05 (Tutorial)

Analytical Solution (..contd.)

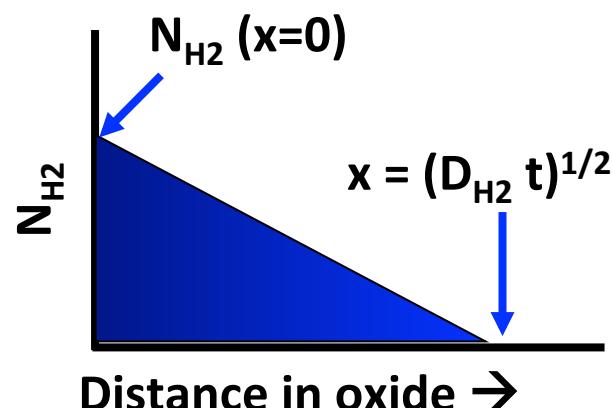
Transformation of $H \rightarrow H_2$: $H + H = H_2$

$$N_H^2(x=0) = N_{H2}(x=0) = \text{Constant.}$$

$$N_{IT}^2 = \left(\frac{k_F}{k_R} \frac{N_0}{N_H(x=0)} \right)^2 = \left(\frac{k_F}{k_R} N_0 \right)^2 \frac{1}{N_{H2}(x=0)}$$

Diffusion of H_2 (Fick's law)

$$\frac{dN_{H2}}{dt} = D_{H2} \frac{d^2 N_{H2}}{dx^2}$$
$$x = \sqrt{D_{H2} t}$$



Analytical Solution (..contd.)

Total no. of traps = 2 x Generated H₂ molecules

$$N_{IT} = 2 * \frac{1}{2} N_{H2}(x=0) \cdot (D_{H2} t)^{1/2}$$

**Area under the curve
for a triangle**

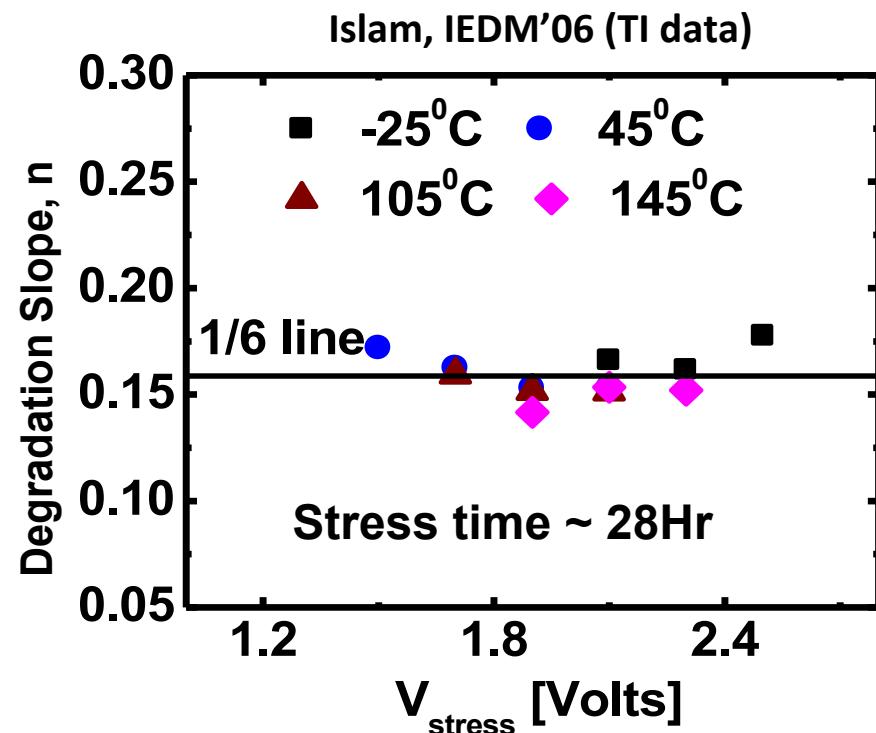
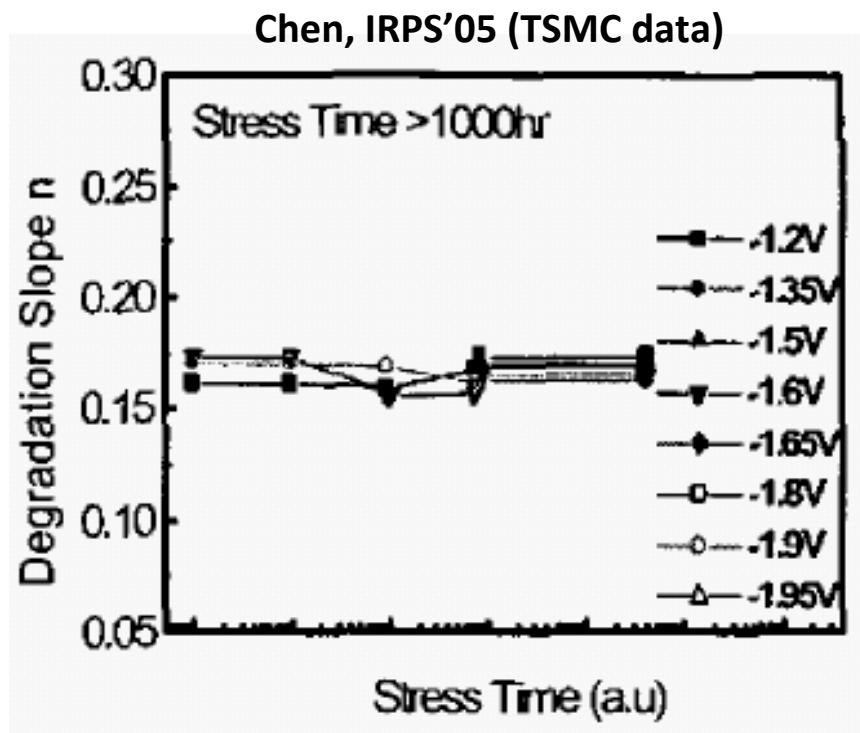
$$N_{IT}^2 = \left(\frac{k_F}{k_R} N_0 \right)^2 \frac{1}{N_{H2}(x=0)}$$

$$N_{IT} = \left(\frac{k_F}{k_R} N_0 \right)^{2/3} (D_{H2} t)^{1/6}$$

**Power-law time
dependence with
exponent n=1/6**

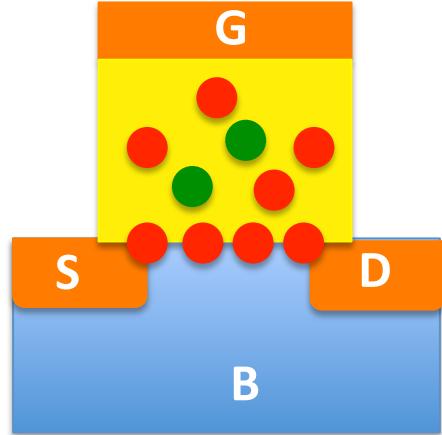
Experimental Proof

Very long time degradation in production quality devices



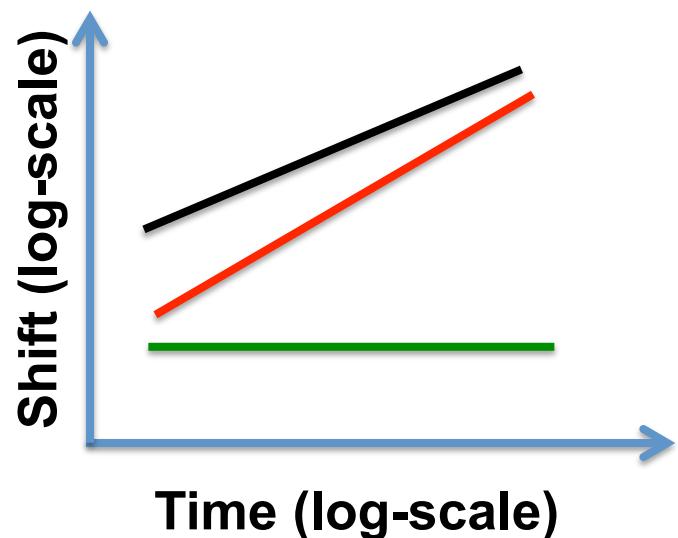
Power law time exponent (n) $\sim 1/6$

The “Physics” of Time Exponent (..contd.)



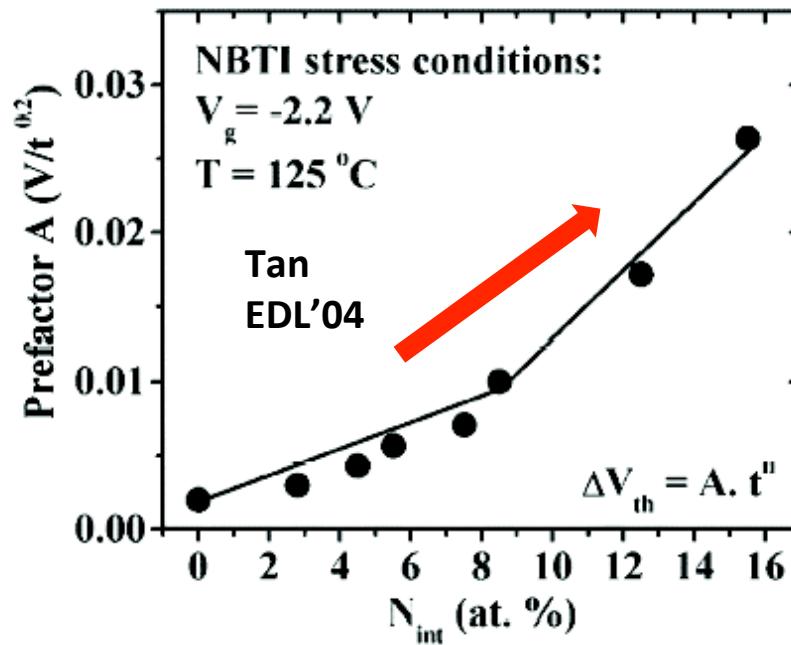
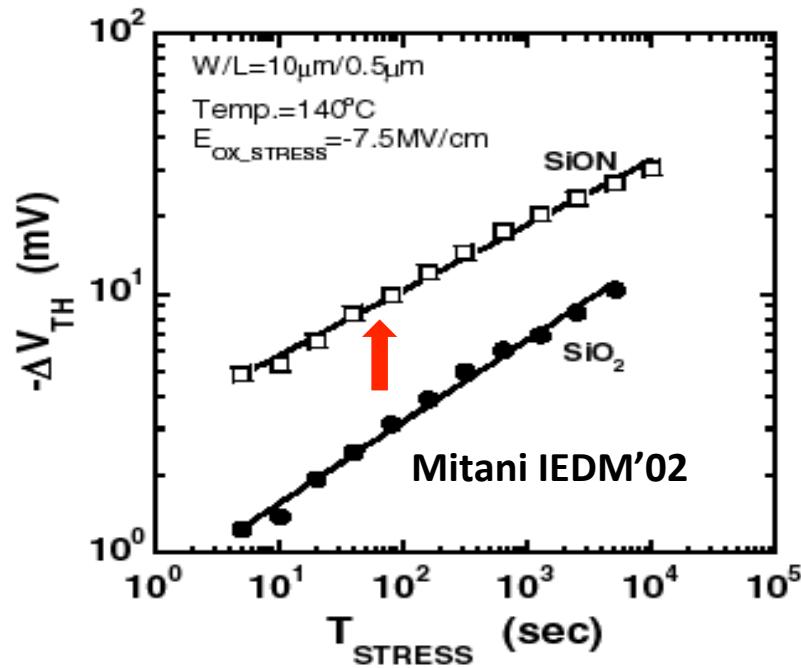
Power law exponent ($n \sim 1/6$) due to generation of X and Y defects (H related, red dots) \rightarrow Slow process

Process related pre-existing traps (green dots) additionally capture holes (when significant) \rightarrow Fast process



Total degradation (black) has higher magnitude and lower slope (n), addition of trap generation (red) and hole trapping (green)

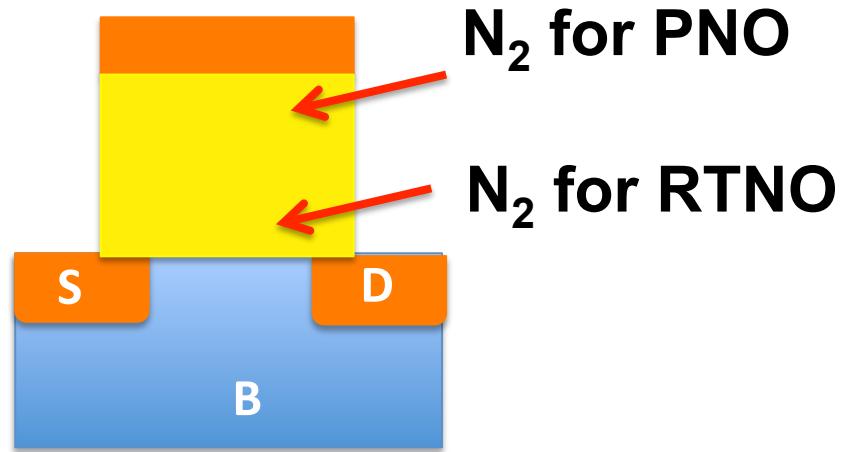
Impact of Gate Insulator Process (Nitrogen)



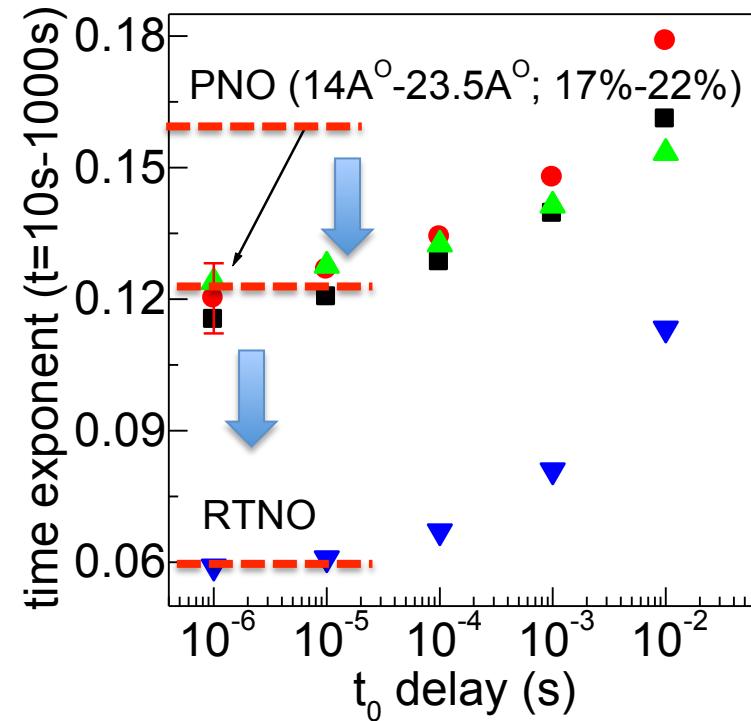
Higher degradation magnitude and lower time exponent when Nitrogen is present in the gate oxide

Total Shift (Interface Traps, Trapping)

$$\Delta V_T = A_{IT} * V_G^{\Gamma_{IT}} * e^{-E_{AIT}/kT} * t^{1/6} + A_{HT} * V_G^{\Gamma_{HT}} * e^{-E_{AHT}/kT} * t^0$$



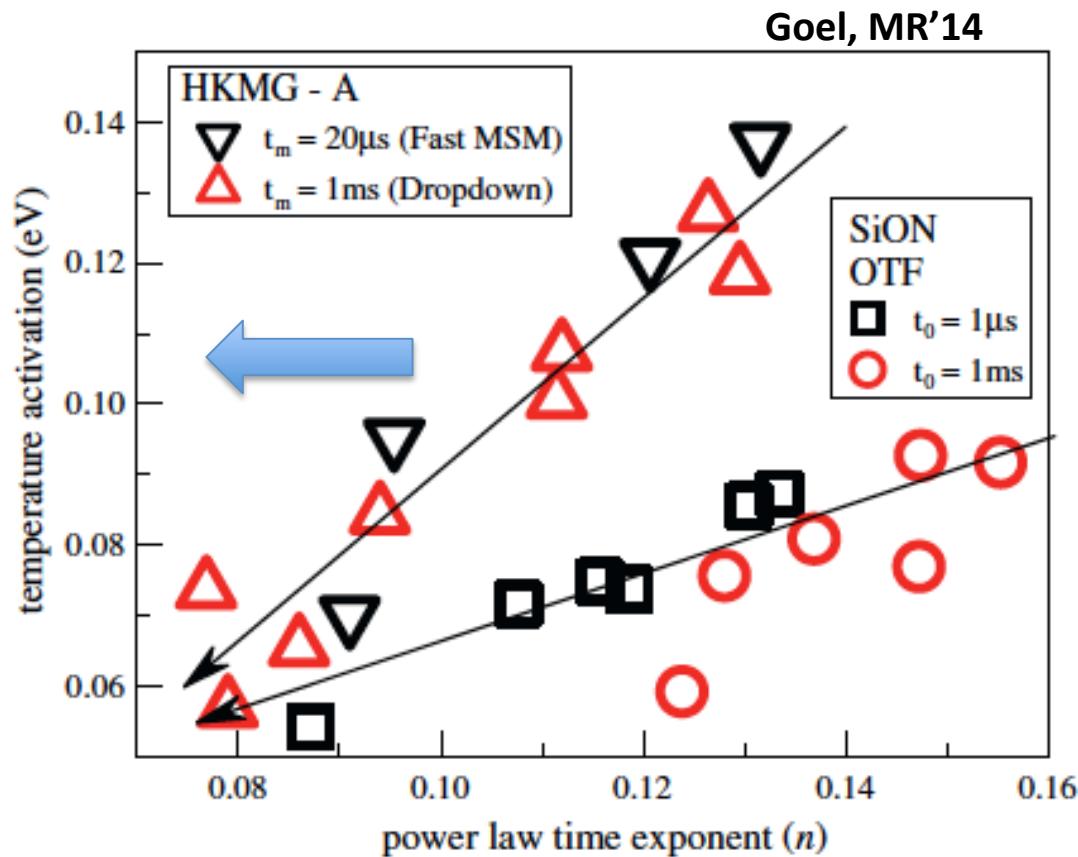
Kumar, IEDM'07



Higher hole trapping for RTNO (Rapid Thermal Nitrided Oxide) than PNO (Plasma Nitrided Oxide), determined by location of Nitrogen

Temperature Activation

Higher hole trapping reduces time exponent (n)



Hole trapping has lower E_A

Uncorrelated trap generation and trapping

Higher hole trapping reduces E_A of overall NBTI

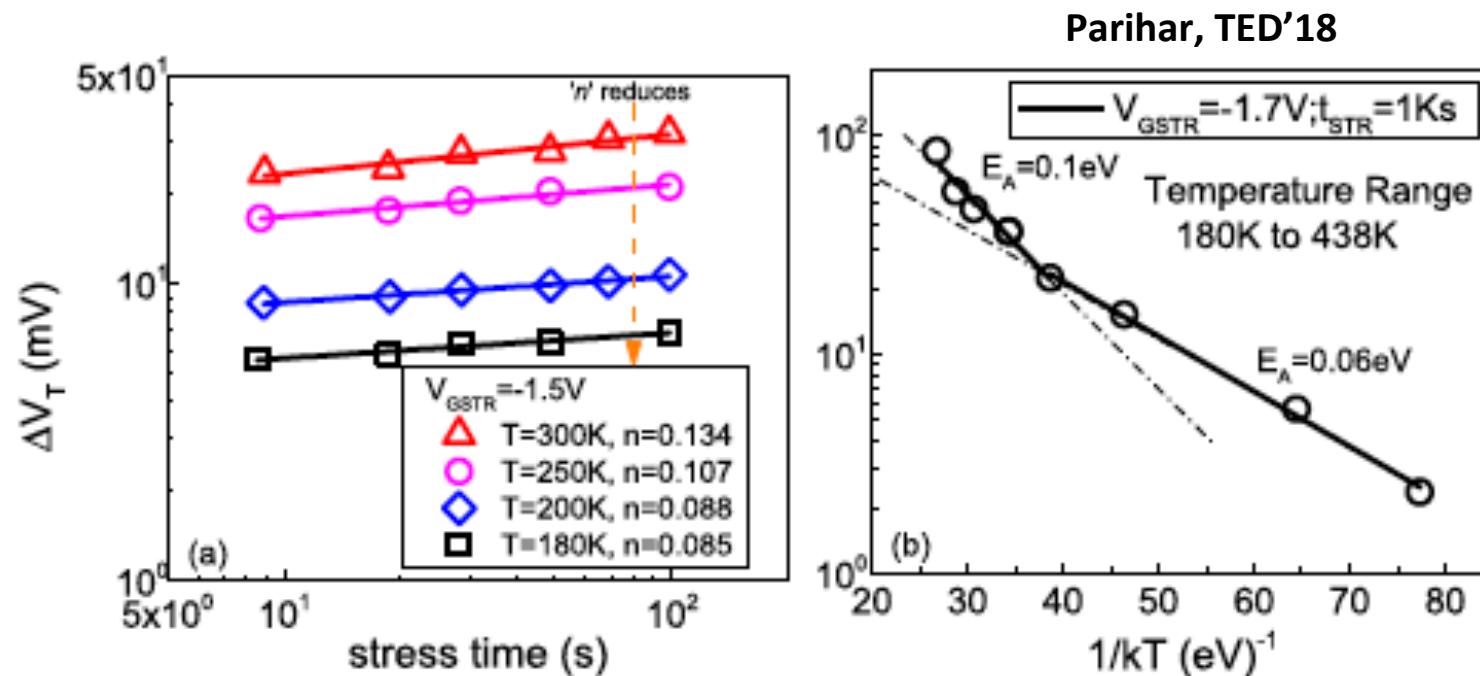
Universality across different SiON and HKMG processes

Further Proof: Low Temperature

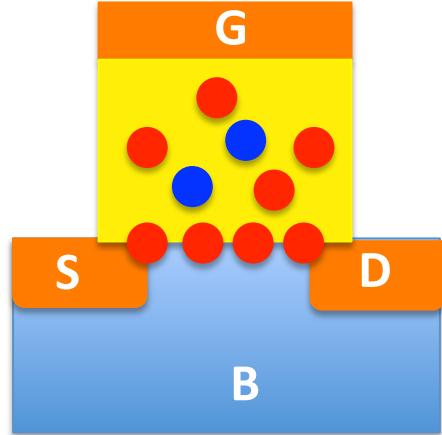
Trapping → Saturation, lower T activation

Trap generation → Power law ($n \sim 1/6$), higher T activation

Trapping has more influence at lower T → Slope reduces

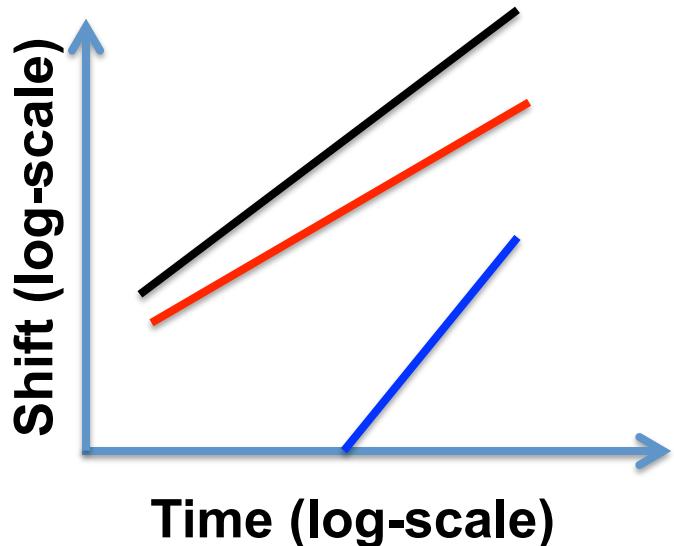


The “Physics” of Time Exponent (..contd.)



Generation of bulk oxide defects due to broken Si-O bonds under high stress bias and temperature (blue dots) → Slow process

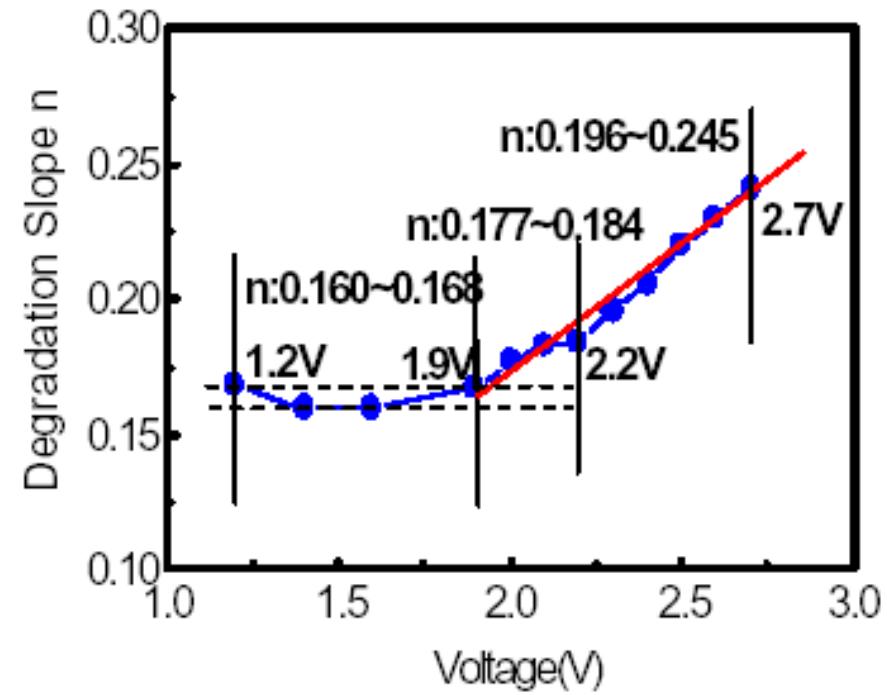
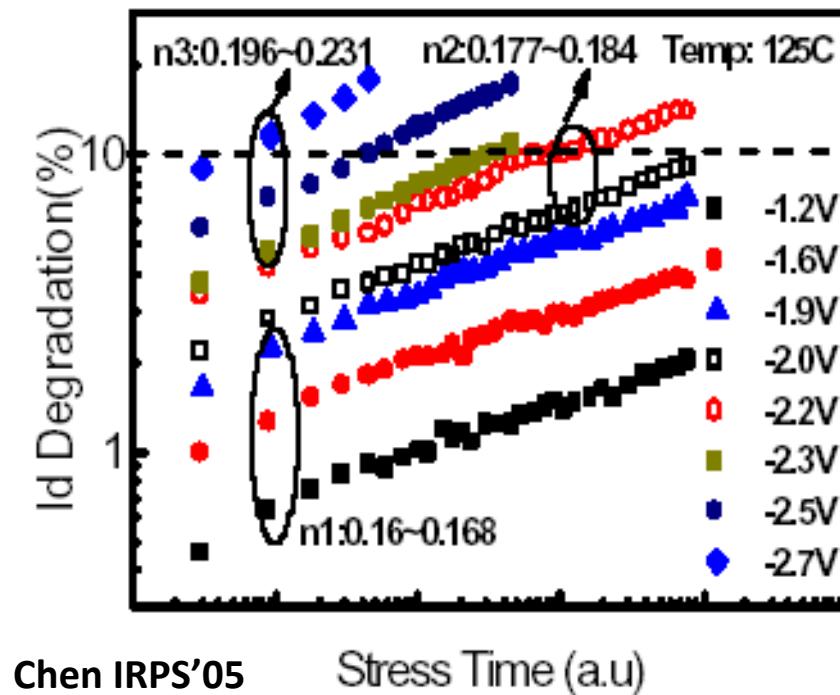
Power law time exponent ($n \sim 0.25 - 0.35$), mechanism not fully understood



Total degradation (black) has higher magnitude and higher slope (n), addition of trap generation due to X-H (Y-H) and Si-O broken bonds

Total Shift (Interface Traps, Bulk Traps)

$$\Delta V_T = A_{IT} * V_G^{\Gamma_{IT}} * e^{-E_{AIT}/kT} * t^{1/6} + A_{OT} * V_G^{\Gamma_{OT}} * e^{-E_{AOT}/kT} * t^{1/4}$$



Increase in degradation magnitude and slope at longer stress time and higher stress bias → Careful choice of maximum stress bias needed to minimize this effect

Final (Total) Degradation

Uncorrelated contribution from all 3 subcomponents

$$\begin{aligned}\Delta V_T &= A * V_G^{\Gamma} * e^{-E_A/kT} * t^n && \textbf{Total shift} \\&= A_{IT} * V_G^{\Gamma_{IT}} * e^{-E_{AIT}/kT} * t^{1/6} && \textbf{Interface traps} \\&+ A_{HT} * V_G^{\Gamma_{HT}} * e^{-E_{AHT}/kT} * t^0 && \textbf{Hole trapping *} \\&+ A_{OT} * V_G^{\Gamma_{OT}} * e^{-E_{AOT}/kT} * t^{1/4} && \textbf{Bulk traps **}\end{aligned}$$

* Higher N, ** Higher V_G / T

Independent verification?