MOS Capacitor

A) Overview
B) MOS electrostatics
C) MOS CV and parameter extraction
D) CV in realistic devices
E) Oxide and interface charges – impact on CV
F) Interface traps from CV (HFCV, HFLFCV)
G) Interface traps from conductance method
H) Leakage through gate oxide (FN and direct tunneling)

Refs: Books by Sze, Taur and Ning, Pierret

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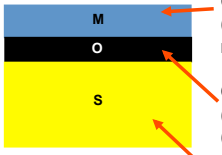
MOS Capacitor

MOS: Metal – Oxide – Semiconductor



Gate: Al (earlier), Poly-Si (earlier), TiN and other metals (now)

Oxide: SiO_2 (earlier), SiON (earlier), Dual layers of SiO_2 (or SiON) and HfO_2 (now)

Substrate: p-type Si (N-MOS) & n-type Si (P-MOS)

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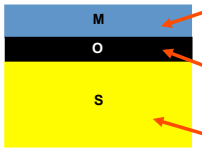
MOS Parameters



Workfunction of Gate

Oxide thickness

Substrate doping (N_A or N_D)

How do we determine MOS parameters?

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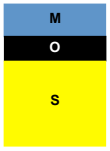
MOS: Ideal vs. Real System



	Ideal system	Real system
Gate	Same workfunction as substrate	N-type for NMOS, P-type for PMOS
Oxide	No conduction	Tunnel conduction (Fowler Nordheim or Direct)
Charges	Only in Gate and Substrate	Also Substrate/ Oxide interface and Oxide bulk

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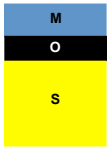
Charges in MOS System (NMOS)



Mode	Gate Charge	Substrate Charge
Accumulation	Negative ($V_G < 0$)	Positive
Depletion	Positive ($V_G > 0$)	Negative
Inversion	Positive ($V_G >> 0$)	Negative

** Opposite for PMOS

Ideal MOS: Gate charge = Substrate charge
Source of substrate charges?

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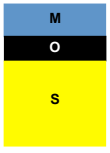
Charges in MOS System (NMOS)



Gate bias	Substrate Charge	Source
$V_G < 0$	Positive	Holes (majority carriers)
$V_G > 0$	Negative	Ionized acceptors (N_A), few electrons (minority carriers)
$V_G >> 0$	Negative	More electrons

Source of majority and minority carriers?

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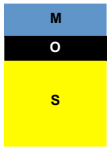
Charges in MOS System (NMOS)



Gate bias	Substrate Charge	Source
$V_G < 0$	Holes	Substrate contact
$V_G > 0$	Electrons	Thermal generation

Response time of majority and minority carriers?

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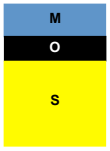
Charges in MOS System (NMOS)



Gate bias	Substrate Charge	Response time
$V_G < 0$	Holes	Fast (dielectric relaxation time)
$V_G > 0$	Electrons	Slow, thermal generation-recombination

Carrier response time impacts MOS CV

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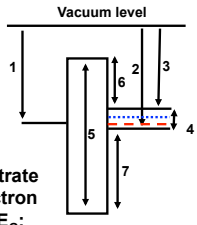
MOS: Energy Band Diagram

Equilibrium (V_G=0), Ideal NMOS



(1) Gate work function, ϕ_m; (2) Substrate work function, ϕ_s; (3) Substrate electron affinity, χ_s; (4) Substrate band gap, E_G; (5) Oxide band gap, E_O; (6) Conduction band offset, ΔE_C; (7) Valence band offset, ΔE_V

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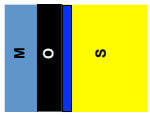
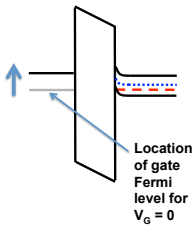
MOS: Energy Band Diagram

Accumulation (V_G<0), Ideal NMOS





Negative charges in gate metal

Positive charges in substrate – accumulation of holes

Where are the holes coming from?

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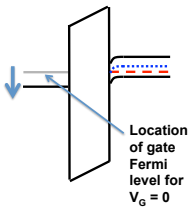
MOS: Energy Band Diagram

Depletion (V_G>0), Ideal NMOS



Positive charges in gate metal

Negative charges in substrate – depletion of holes – "un-covering" of ionized acceptors

Where are the holes going to?

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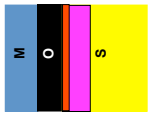
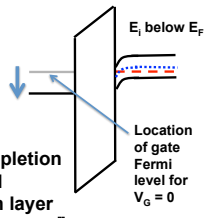
MOS: Energy Band Diagram

Inversion (V_G>>0), Ideal NMOS





Positive charges in gate metal

Negative charges in substrate – depletion of holes – "un-covering" of ionized acceptors + Formation of inversion layer by electrons → Surface becomes "n-type"

Where are the electrons coming from?

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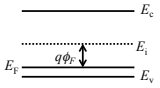
Bulk Semiconductor Potential

$$q\phi_F \equiv E_i(bulk) - E_F$$

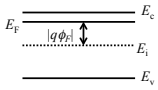
- **p-type Si (n-MOS):**

$$\phi_F = \frac{kT}{q}\ln(N_A / n_i) > 0$$



- **n-type Si (p-MOS):**

$$\phi_F = -\frac{kT}{q}\ln(N_D / n_i) < 0$$



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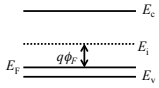
Semiconductor Workfunction

Electron affinity → $q\chi_s$ (vacuum level – C.B.)

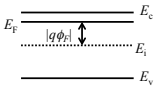
- **p-type Si (n-MOS):**

$\phi_s = \chi_s + E_G/2q + \phi_F$



- **n-type Si (p-MOS):**

$\phi_s = \chi_s + E_G/2q - \phi_F$



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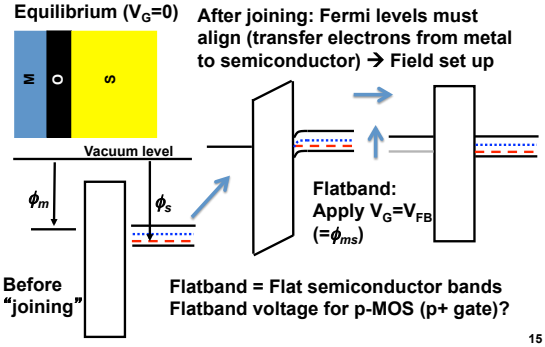
Non-ideal Gate Workfunction (NMOS)

Equilibrium (V_G=0)

After joining: Fermi levels must align (transfer electrons from metal to semiconductor) → Field set up



Flatband = Flat semiconductor bands
Flatband voltage for p-MOS (p+ gate)?

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