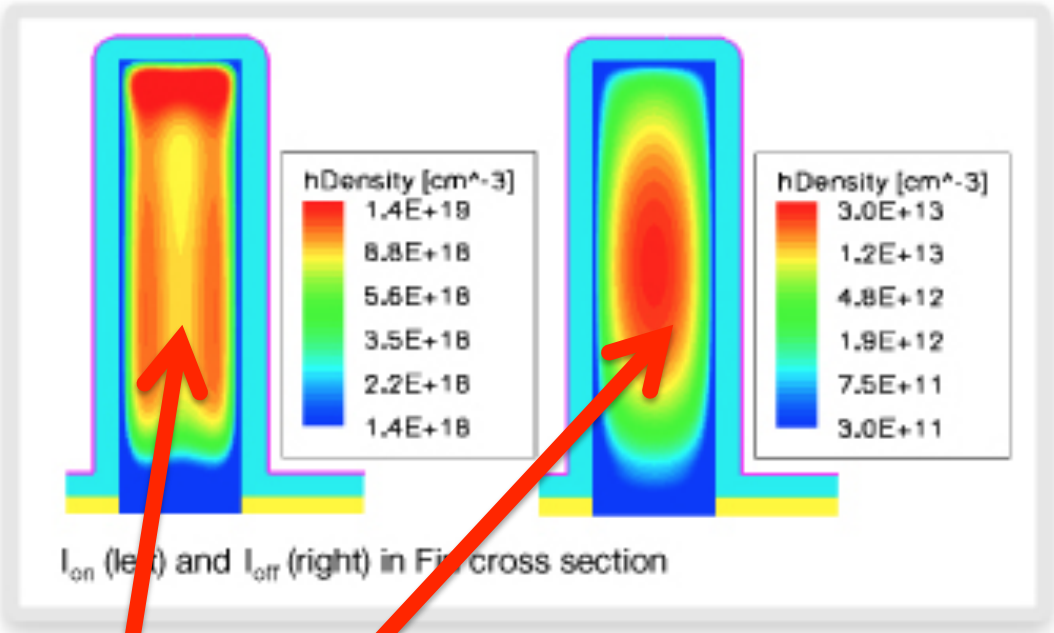
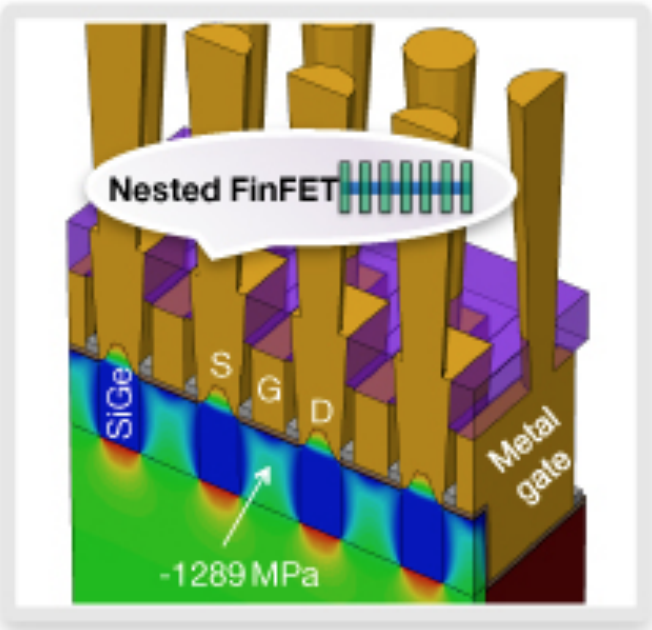
FinFET – Current Conduction



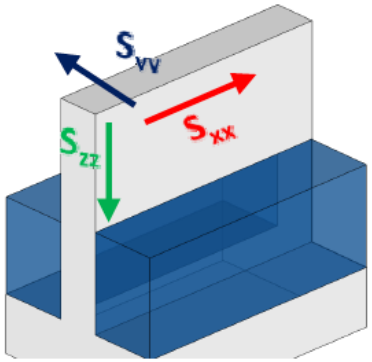
I_{on} (left) and I_{off} (right) in Fin cross section



ON: Surface conduction dominates

OFF: Volume conduction dominates (away from gate, difficult to turn off) → Thinner fins

FinFET – Stress Effects

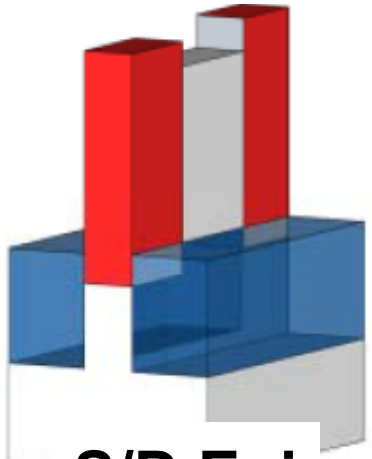


T = Tensile (**+ve**); **C** = Compressive (**-ve**)

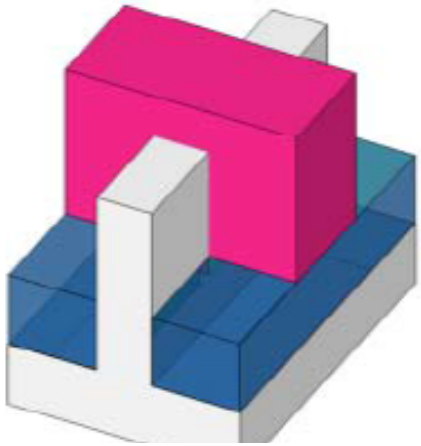
Stress (1 Gpa)	NMOS	PMOS
S_{xx} Longitudinal	T (65%)	C (63%)
S_{yy} Transverse	T (19%)	T (22%)
S_{zz} Vertical	C (60%)	T (26.5%)

Stress options:

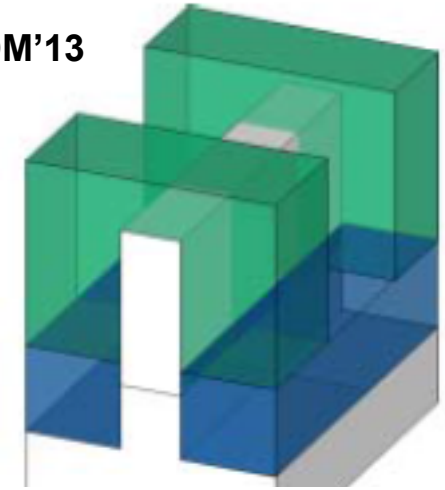
Nainani, IEDM'13



S/D Epi



RMG Gate Fill

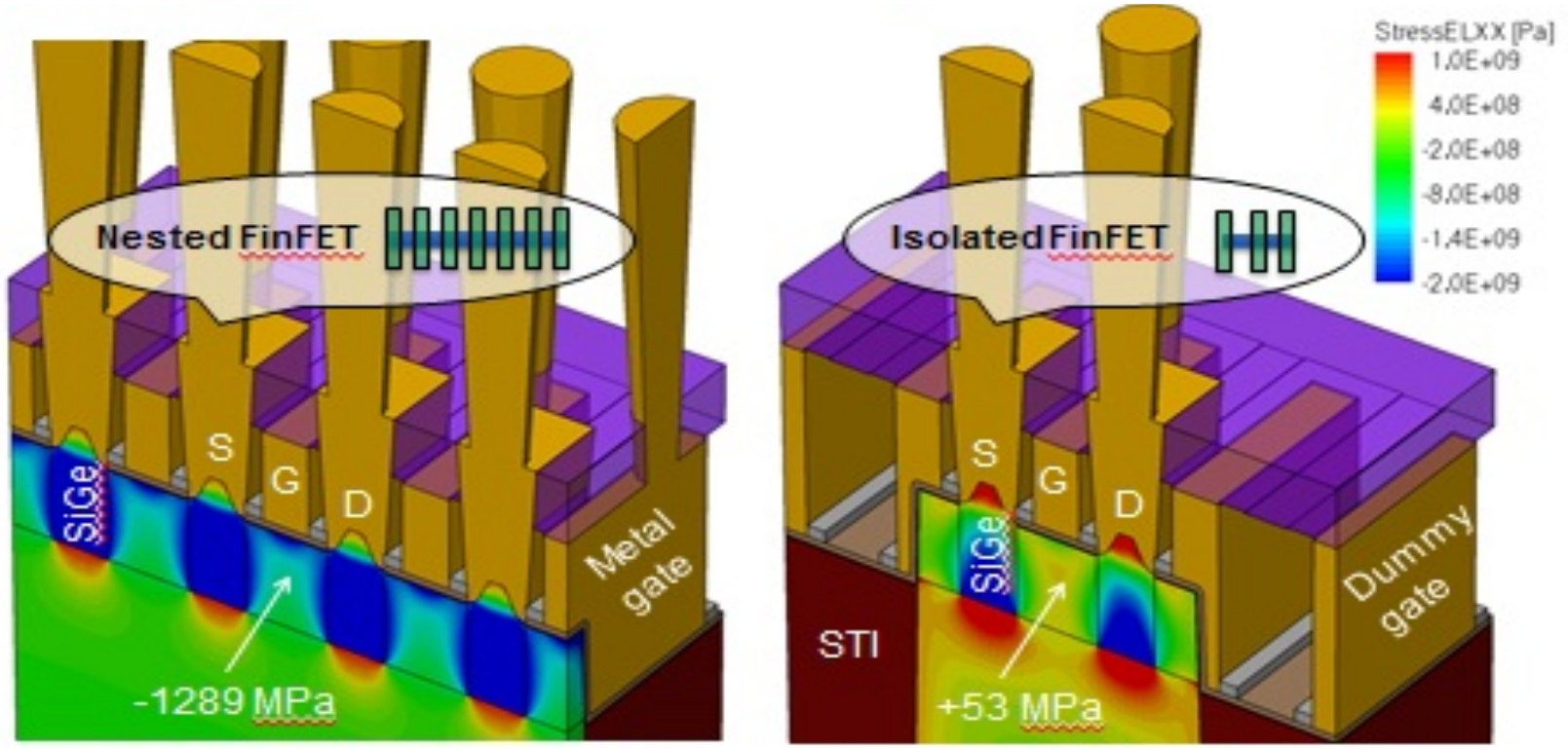


S/D Contact Fill

Stress liners (e.g. planar) no longer effective

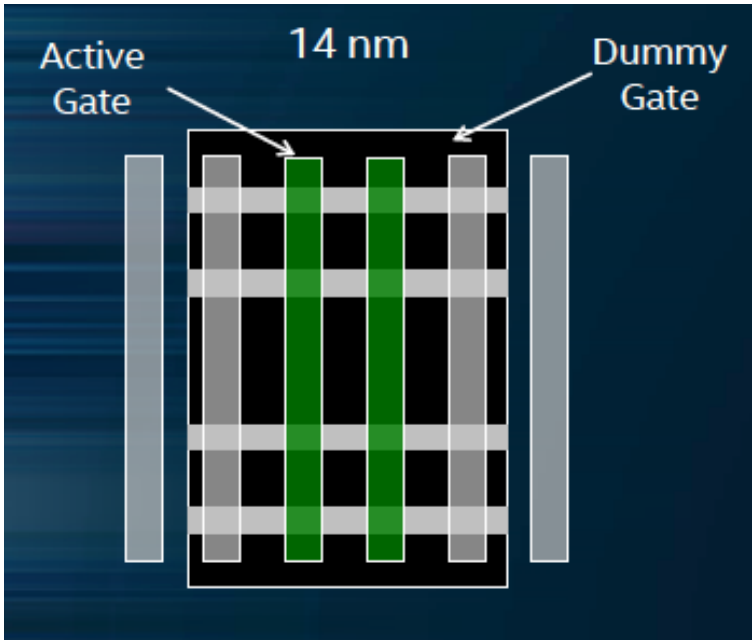
FinFET Stress Proximity Effect

Stress simulation in multiple fin versus single fin device

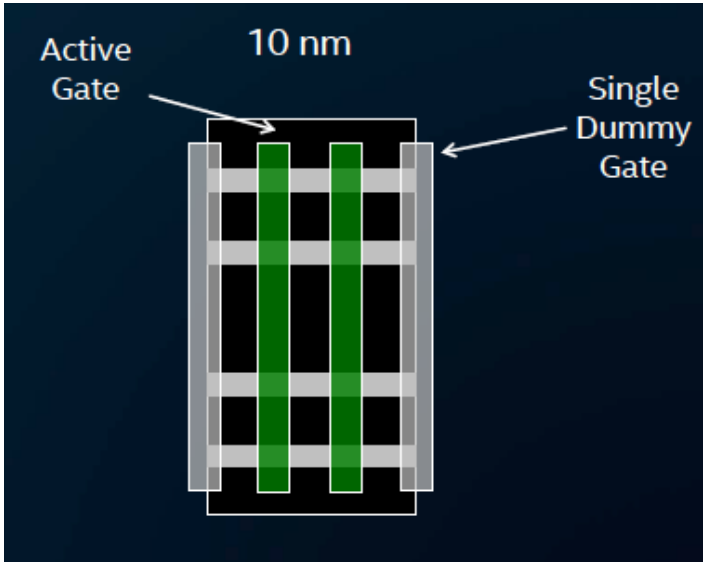


Stress relaxation in single fin device – reduction in I_D

FinFET Stress Proximity Effect

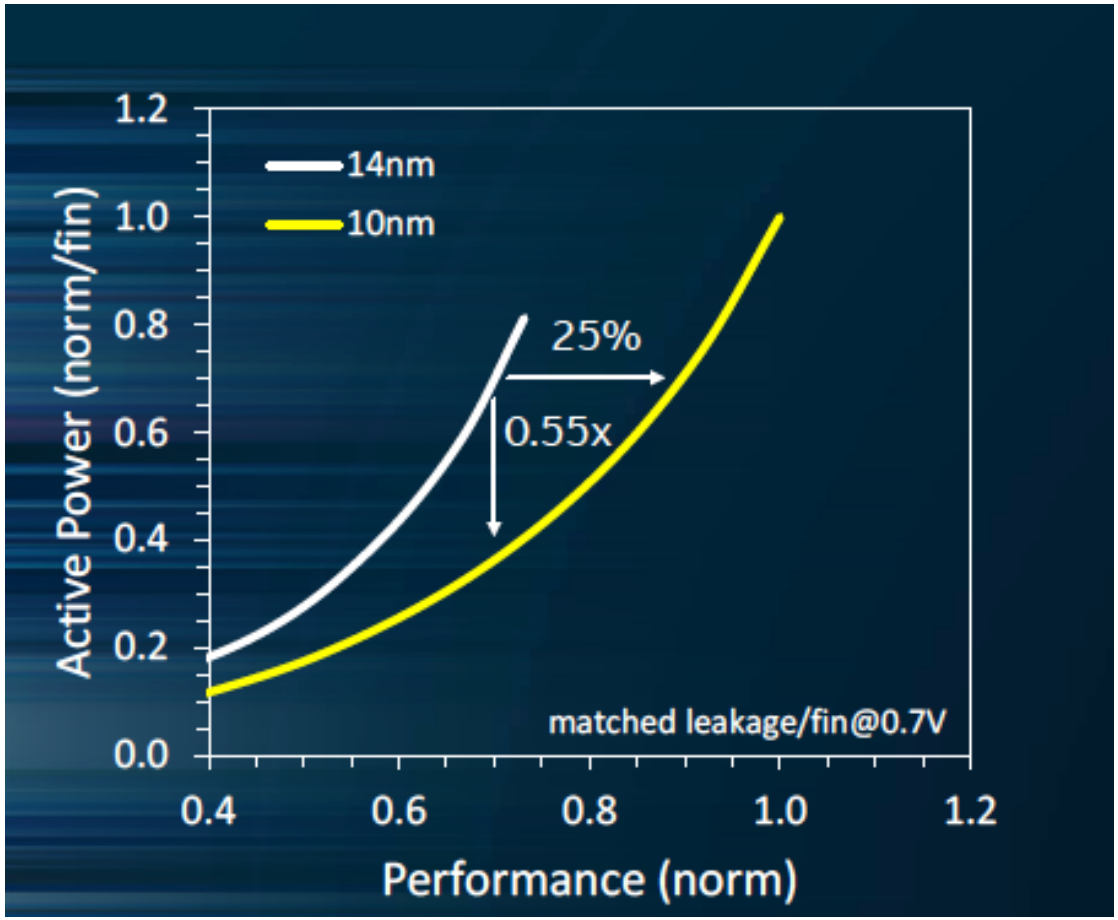


Need dummy gates



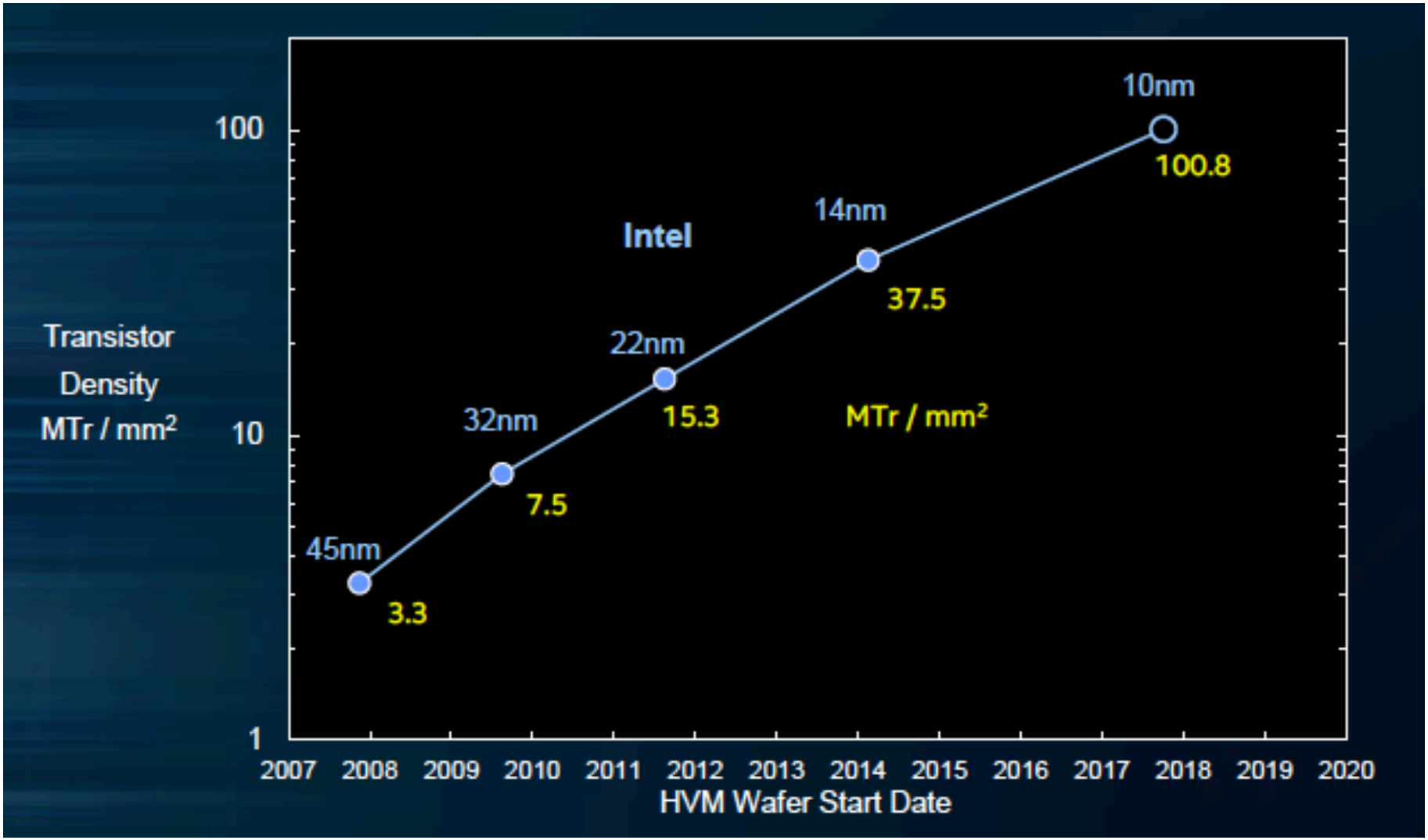
Intel

FinFET Scaling → Power vs. Performance



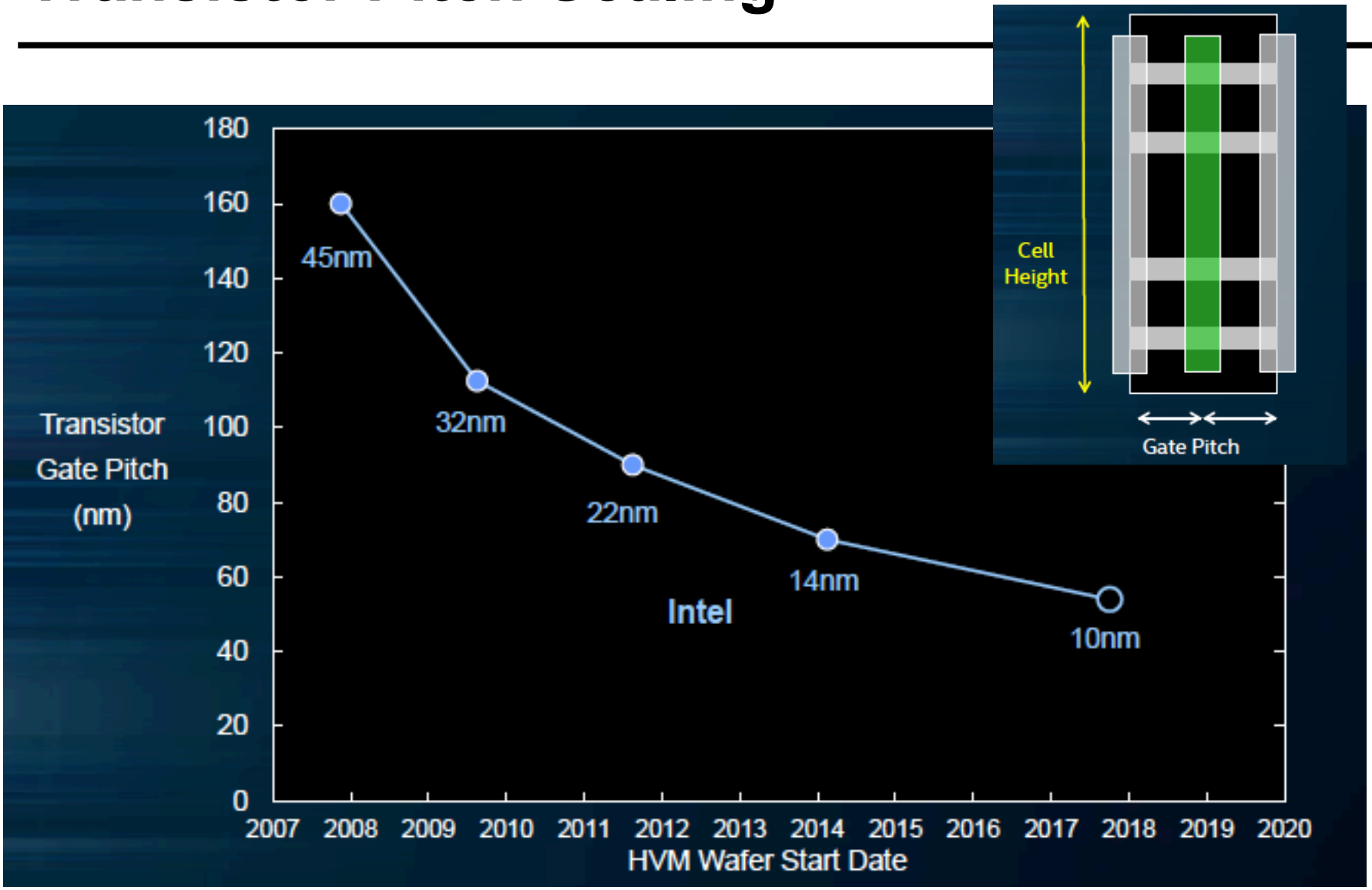
Intel

Logic Transistor Density



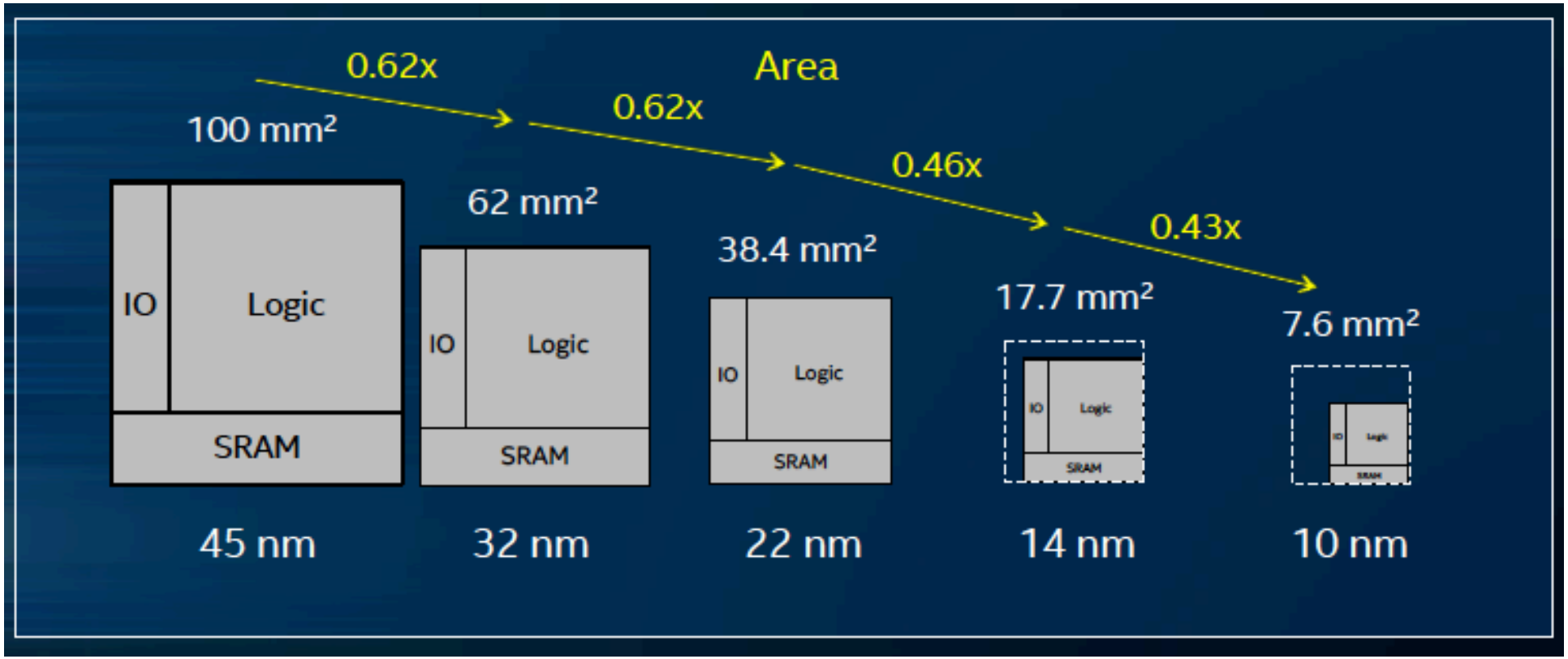
Intel

Transistor Pitch Scaling



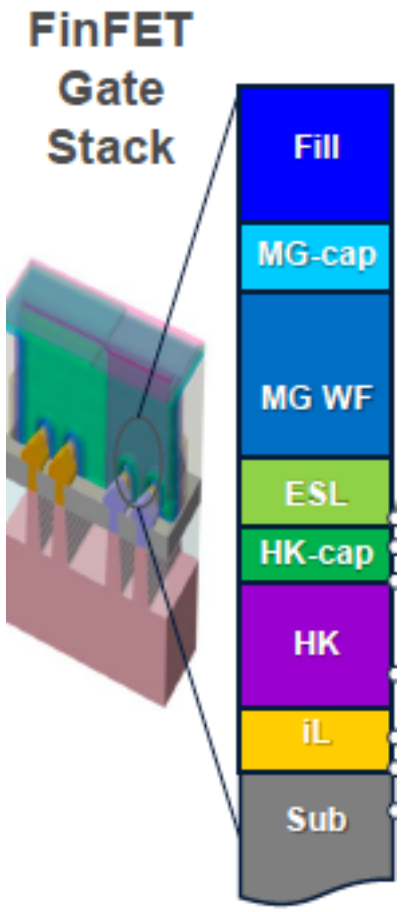
Intel

Microprocessor Area Scaling

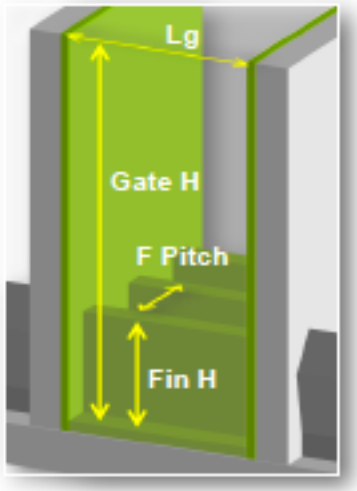


Intel

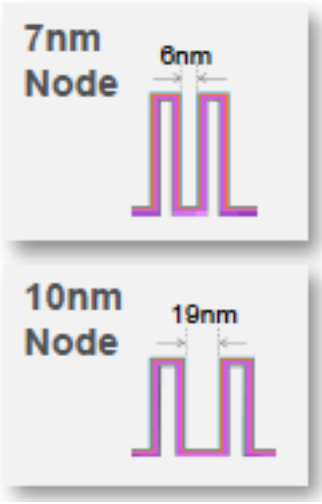
Scaling Challenges: Gate Stack (1)

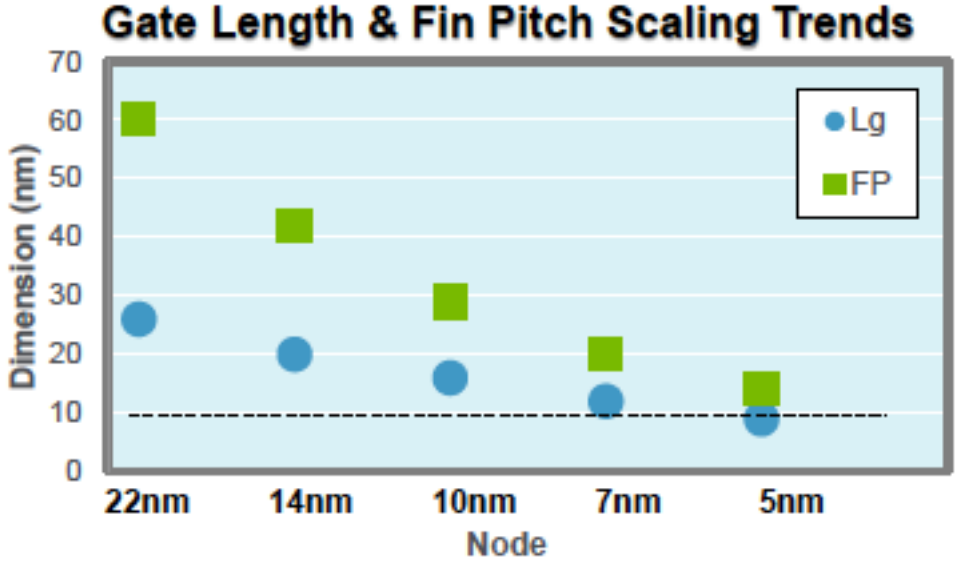


FinFET Gate Trench



Post HK-cap Fin Profile





Diminishing volume for gate stack → Thinner layers → Loss of bulk properties

PMOS SiGe channel (mobility boost) → Integration

Si / SiGe GAA → Lower volume, strong quantum effects, new transport physics

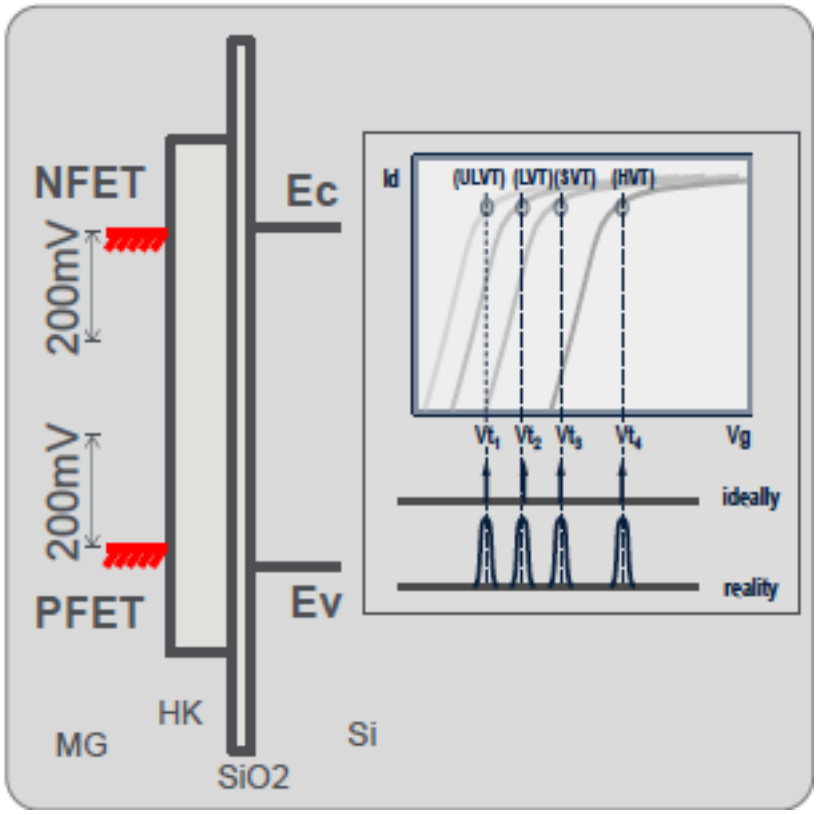
Steven H. (AMAT)

Scaling Challenges: Gate Stack (2)

Need FETs with multiple V_T for SoC applications

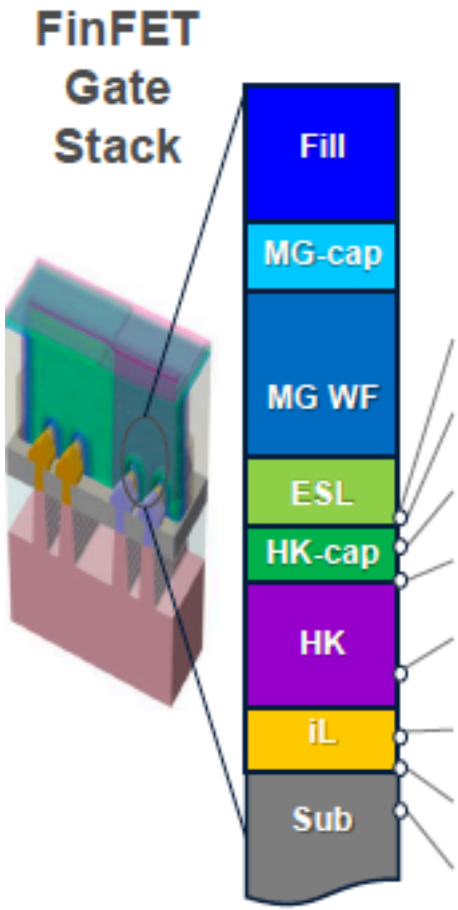
Composition and thickness

Insertion of dipole or trace elements



Steven H. (AMAT)

Scaling Challenges: Gate Stack (3)

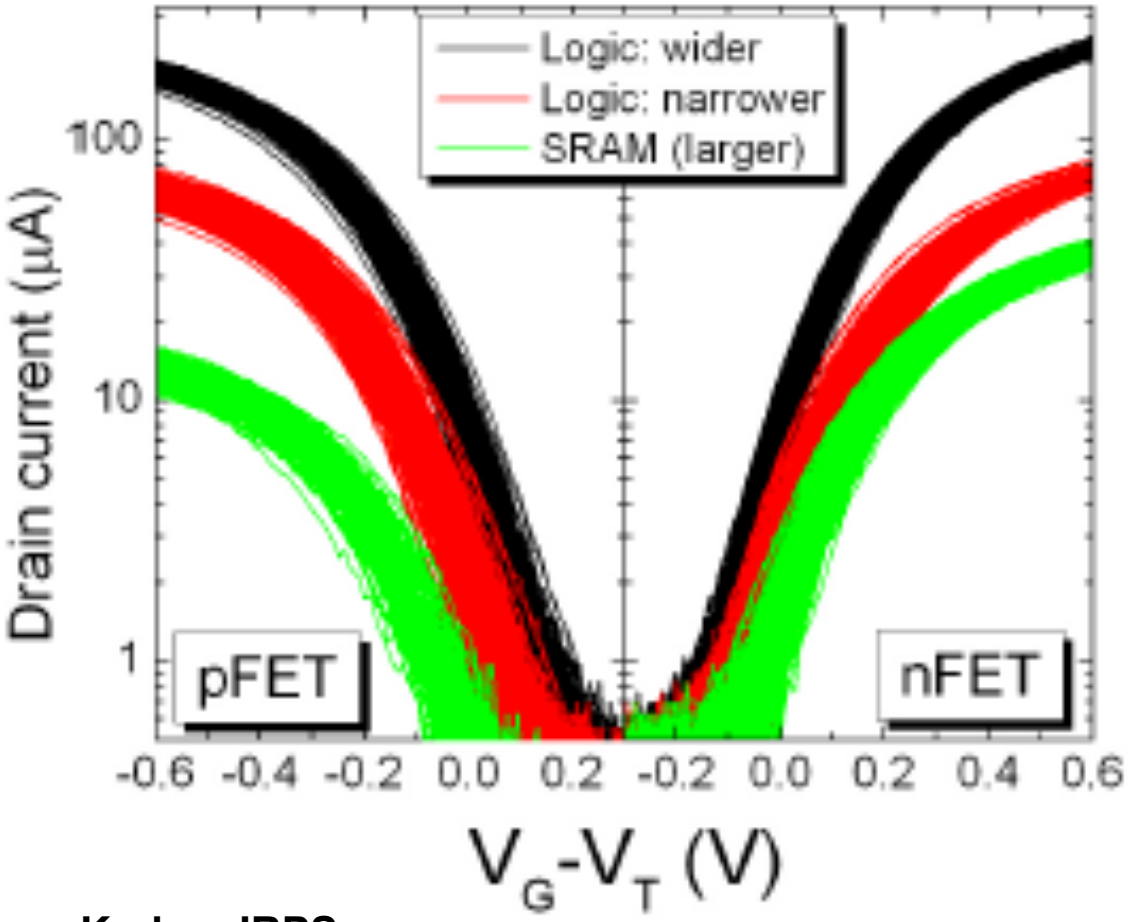


Layers	Functions	Effects on Device						
		Tinv	Jinv	Vt	μ	NBTI	PBTI	TDDB
WF MG / cap	Establish WF for N and P FETs	✓	✓	✓			✓	✓
a-Si + Anneal	Reliability, EOT and Vt control	✓	✓			✓	✓	✓
Post cap Anneal	Densification of HK cap	✓	✓	✓				✓
HK cap	Phy/Chem barrier for HfOx	✓		✓				✓
HK passivation	Suppress Vacancy & Defects	✓	✓	✓		✓	✓	✓
HK	Gate Leakage Suppression	✓	✓	✓			✓	✓
iL formation	Performance & Reliability	✓	✓	✓	✓	✓		✓
Pre-clean	Interface Quality				✓	✓		
Channel implt	Dopant & Profile			✓	✓	✓		

Processes → Impact on performance & reliability

Steven H. (AMAT)

Variability



Kerber, IRPS 2013

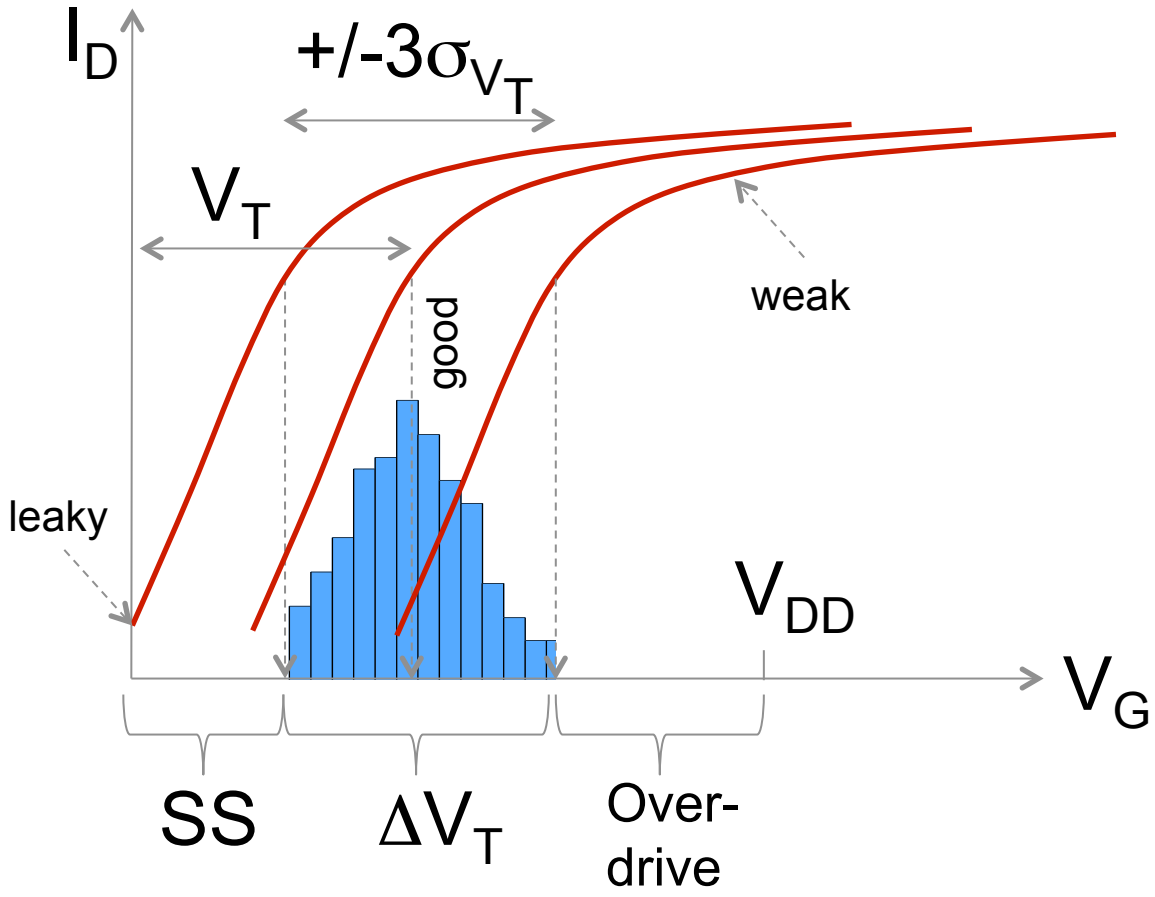
Variation in current across devices

Systematic (process) variability and stochastic effects

Random Dopant Fluctuation (RDF), Line Edge Roughness (LER), Metal Grain Granularity (MGG)

Consequences of Variability

V_T distribution is normal (mean, variance)



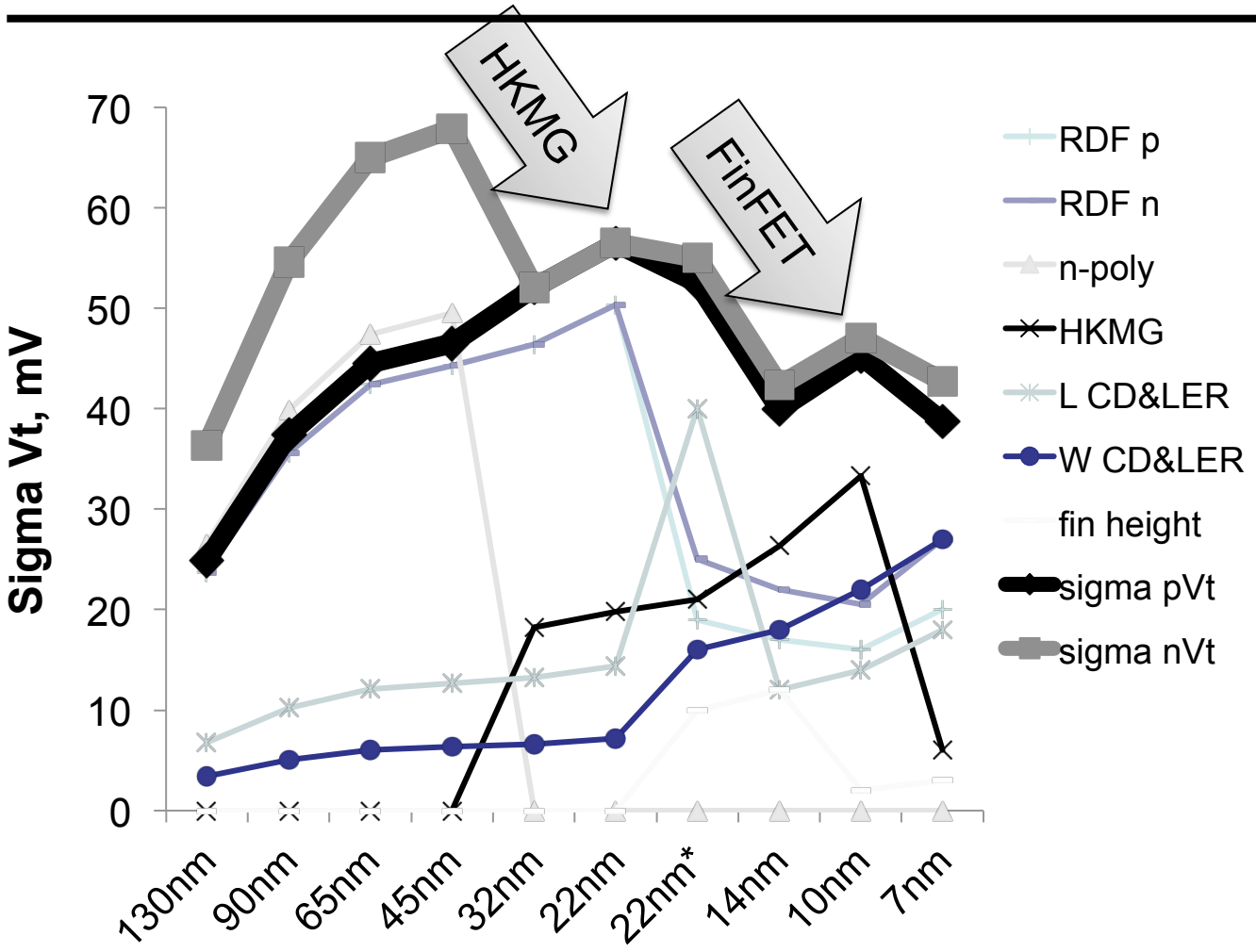
Puts limit on V_{DD} scaling

Dynamic power ~ V_{DD}^2

How to reduce static and dynamic power?

How to achieve voltage scaling?

Variability and Scaling: HKMG, FinFET



The data is for the L_{min} W_{min} transistor

Planar → RDF domination

FinFET → Dimension domination

Overall reduction due to better dimension control

V. Moroz (Synopsys)