

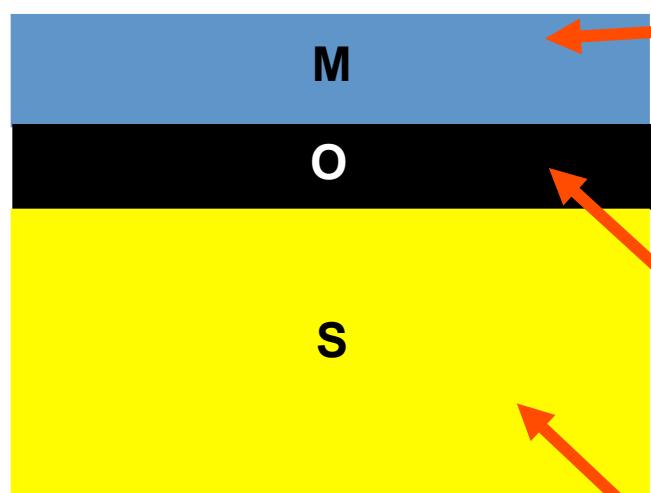
MOS Capacitor

- A) Overview
- B) MOS electrostatics
- C) MOS CV and parameter extraction
- D) CV in realistic devices
- E) Oxide and interface charges – impact on CV
- F) Interface traps from CV (HFCV, HFLFCV)
- G) Interface traps from conductance method
- H) Leakage through gate oxide (FN and direct tunneling)

Refs: Books by Sze, Taur and Ning, Pierret

MOS Capacitor

MOS: Metal – Oxide – Semiconductor

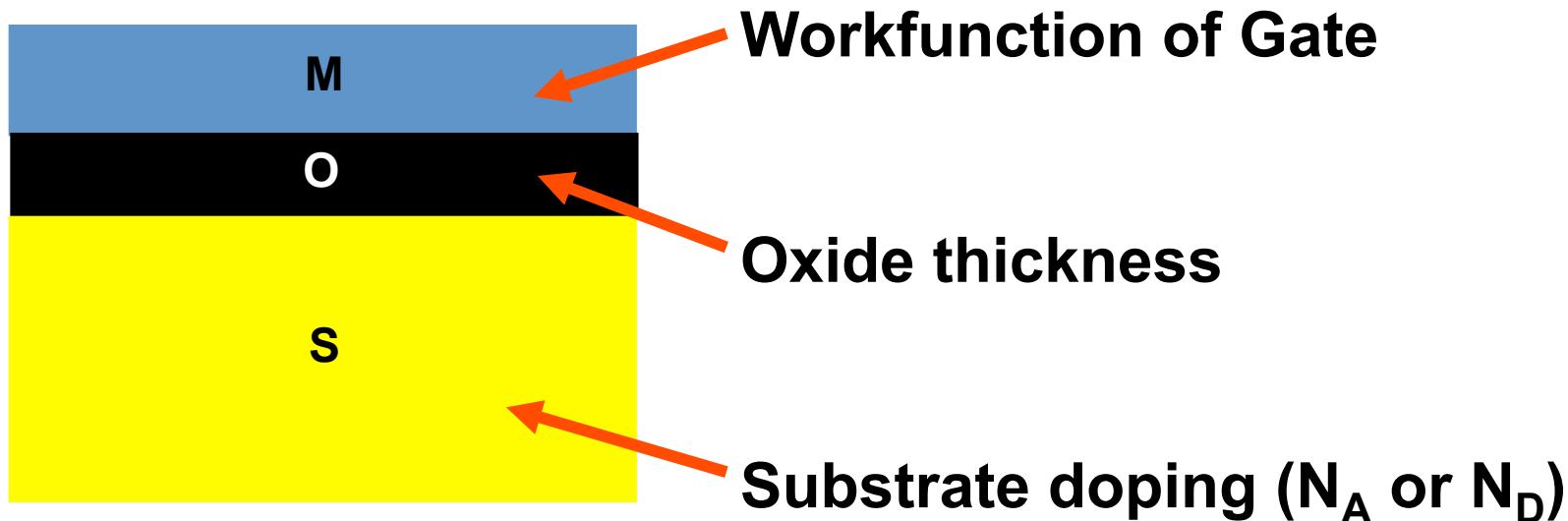


Gate: Al (earlier), Poly-Si (earlier), TiN and other metals (now)

Oxide: SiO₂ (earlier), SiON (earlier), Dual layers of SiO₂ (or SiON) and HfO₂ (now)

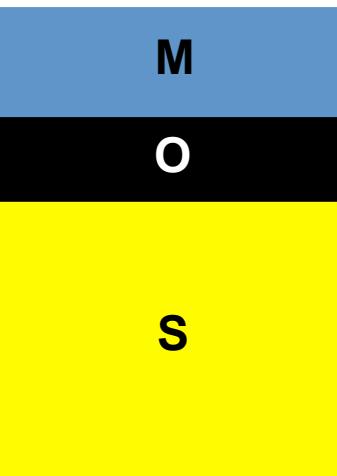
Substrate: p-type Si (N-MOS) & n-type Si (P-MOS)

MOS Parameters



How do we determine MOS parameters?

MOS: Ideal vs. Real System

		Ideal system	Real system
 <p>M O S</p> The diagram shows a cross-section of an MOS stack. It consists of three horizontal layers: a top blue layer labeled 'M' (Metal), a middle black layer labeled 'O' (Oxide), and a bottom yellow layer labeled 'S' (Substrate).	Gate	Same workfunction as substrate	N-type for NMOS, P-type for PMOS
	Oxide	No conduction	Tunnel conduction (Fowler Nordheim or Direct)
	Charges	Only in Gate and Substrate	Also Substrate/Oxide interface and Oxide bulk

Charges in MOS System (NMOS)

M	Mode	Gate Charge	Substrate Charge
O	Accumulation	Negative ($V_G < 0$)	Positive
	Depletion	Positive ($V_G > 0$)	Negative
	Inversion	Positive ($V_G \gg 0$)	Negative

** Opposite for PMOS

Ideal MOS: Gate charge = Substrate charge
Source of substrate charges?

Charges in MOS System (NMOS)

M	Gate bias	Substrate Charge	Source
o	$V_G < 0$	Positive	Holes (majority carriers)
s	$V_G > 0$	Negative	Ionized acceptors (N_A), few electrons (minority carriers)
	$V_G \gg 0$	Negative	More electrons

Source of majority and minority carriers?

Charges in MOS System (NMOS)

M	Gate bias	Substrate Charge	Source
O	$V_G < 0$	Holes	Substrate contact
S	$V_G > 0$	Electrons	Thermal generation

Response time of majority and minority carriers?

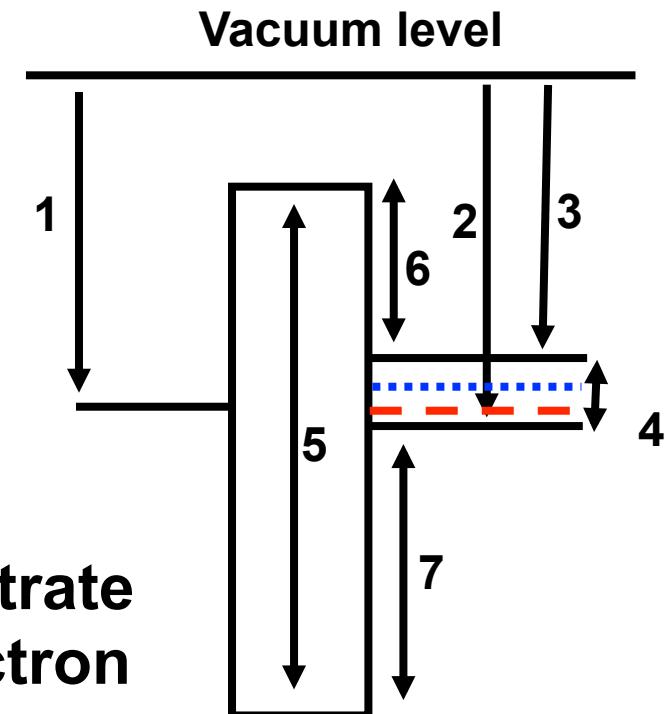
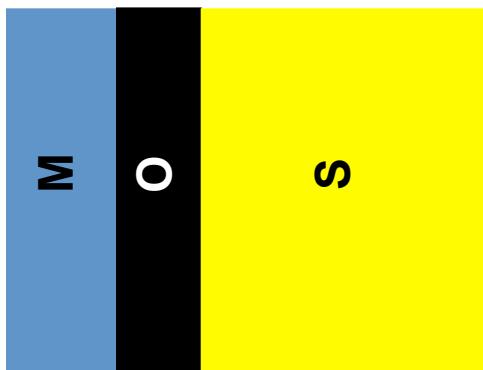
Charges in MOS System (NMOS)

M	Gate bias	Substrate Charge	Response time
O	$V_G < 0$	Holes	Fast (dielectric relaxation time)
	$V_G > 0$	Electrons	Slow, thermal generation-recombination

Carrier response time impacts MOS CV

MOS: Energy Band Diagram

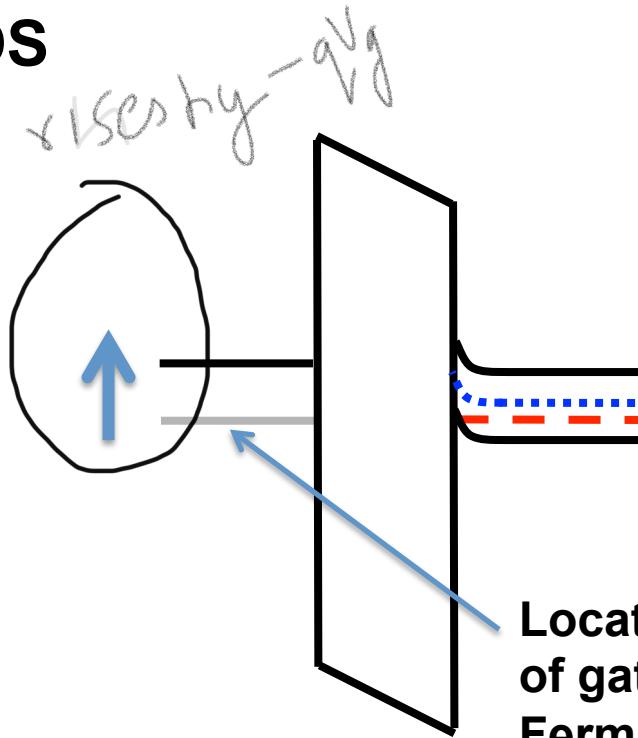
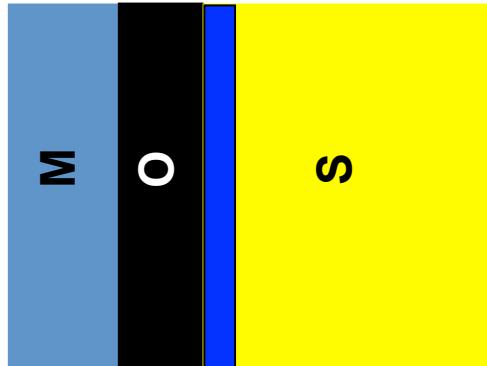
Equilibrium ($V_G=0$), Ideal NMOS



- (1) Gate work function, ϕ_m ; (2) Substrate work function, ϕ_s ; (3) Substrate electron affinity, χ_s ; (4) Substrate band gap, E_G ; (5) Oxide band gap, E_O ; (6) Conduction band offset, ΔE_C ; (7) Valence band offset, ΔE_V

MOS: Energy Band Diagram

Accumulation ($V_G < 0$), Ideal NMOS



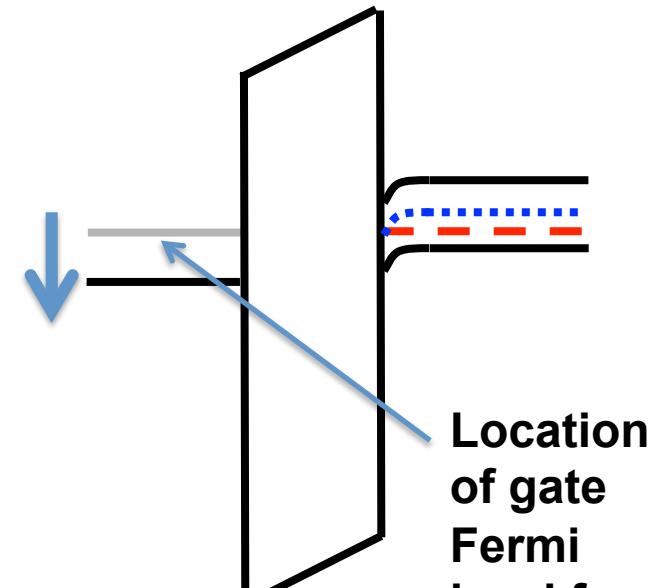
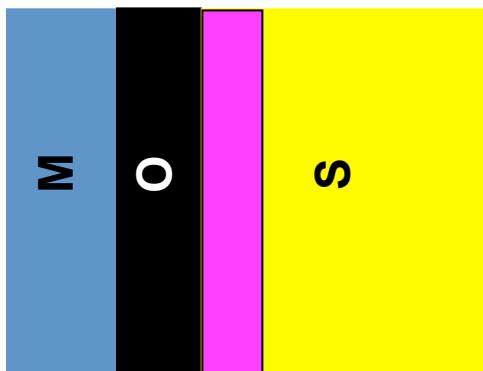
Negative charges in gate metal

Positive charges in substrate –
accumulation of holes

Where are the holes coming from?

MOS: Energy Band Diagram

Depletion ($V_G > 0$), Ideal NMOS



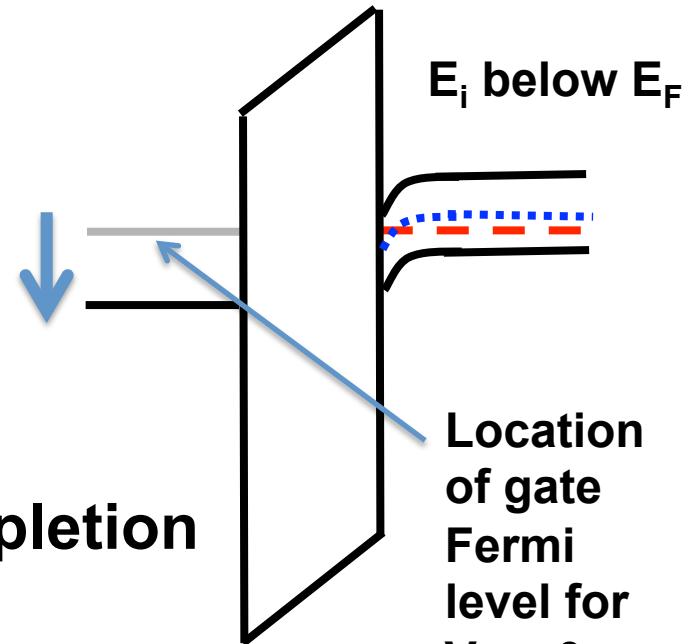
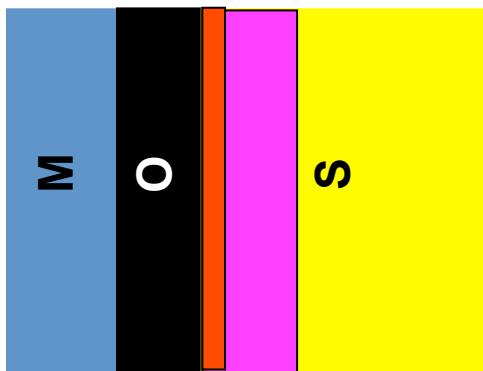
Positive charges in gate metal

Negative charges in substrate –
depletion of holes – “un-covering”
of ionized acceptors

Where are the holes going to?

MOS: Energy Band Diagram

Inversion ($V_G \gg 0$), Ideal NMOS



Positive charges in gate metal

Negative charges in substrate – depletion of holes – “un-covering” of ionized acceptors + Formation of inversion layer by electrons → Surface becomes “n-type”

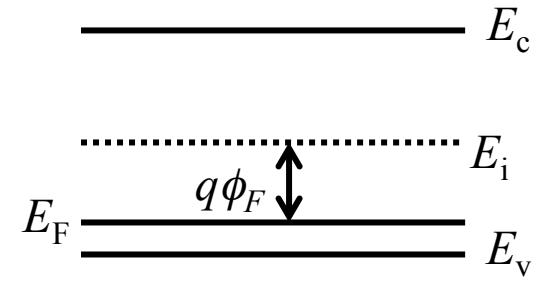
Where are the electrons coming from?

Bulk Semiconductor Potential

$$q\phi_F \equiv E_i(\text{bulk}) - E_F$$

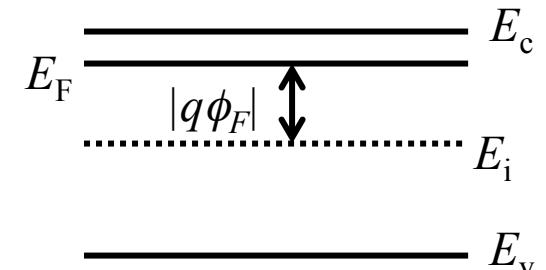
- **p-type Si (n-MOS):**

$$\phi_F = \frac{kT}{q} \ln(N_A / n_i) > 0$$



- **n-type Si (p-MOS):**

$$\phi_F = -\frac{kT}{q} \ln(N_D / n_i) < 0$$

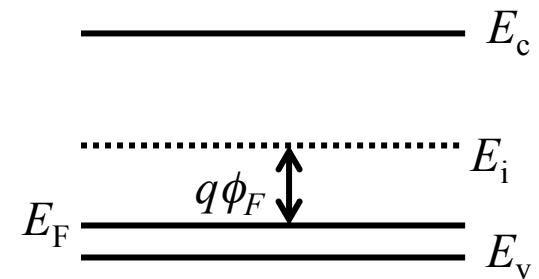


Semiconductor Workfunction

Electron affinity $\rightarrow q \cdot \chi_s$ (vacuum level – C.B.)

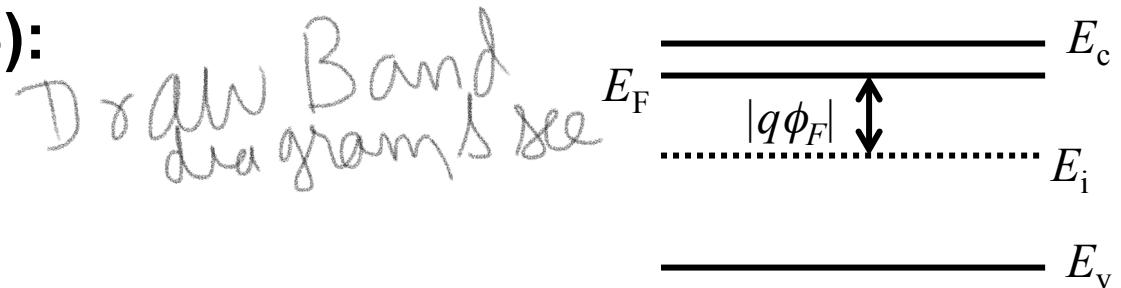
- p-type Si (n-MOS):

$$\phi_s = \chi_s + E_G/2q + \phi_F$$



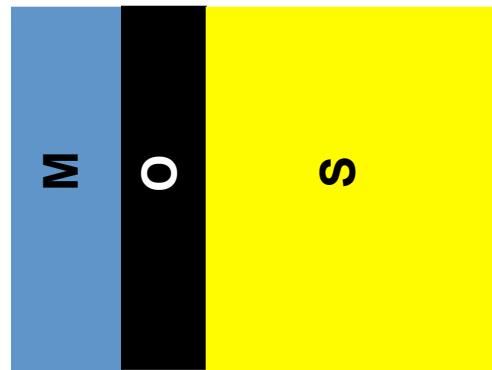
- n-type Si (p-MOS):

$$\phi_s = \chi_s + E_G/2q - \phi_F$$

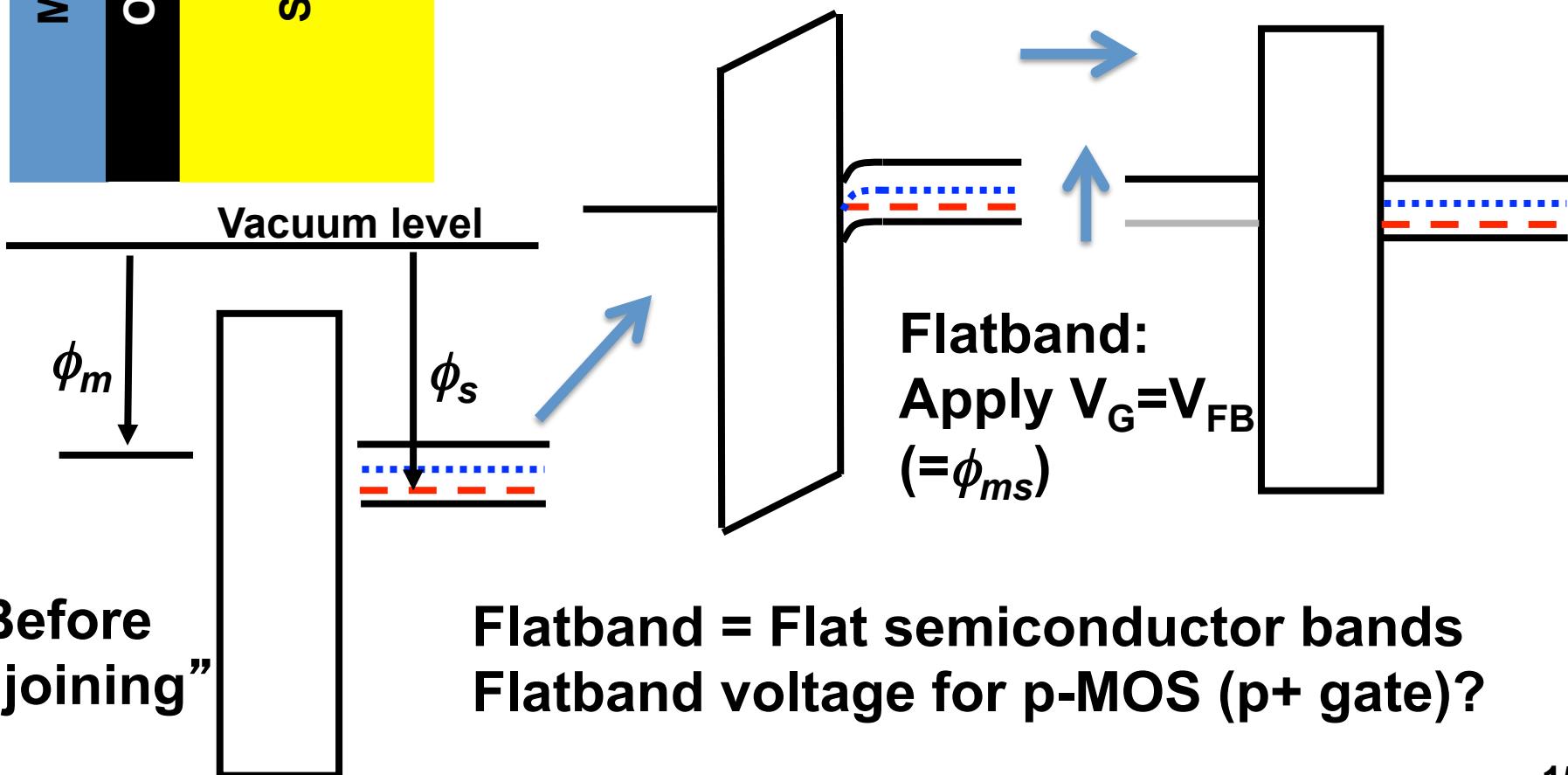


Non-ideal Gate Workfunction (NMOS)

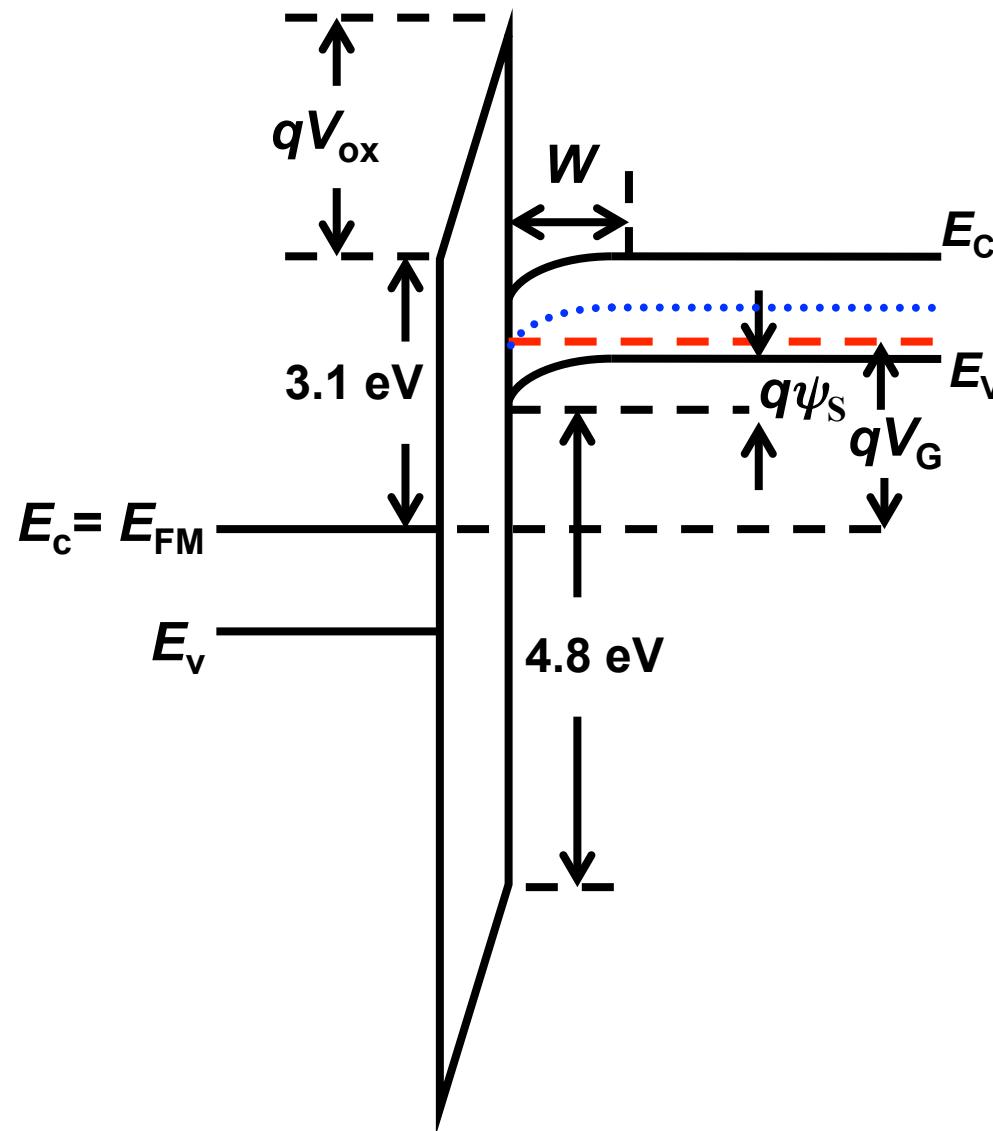
Equilibrium ($V_G=0$)



After joining: Fermi levels must align (transfer electrons from metal to semiconductor) \rightarrow Field set up



MOS Electrostatics (NMOS)



MOS Electrostatics (NMOS)

Solution of Poisson equation

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\epsilon_{si}} [p - n + N_D - N_A]$$

$$p = N_A e^{-q\psi/kT}, \quad n = \frac{n_i^2}{N_A} e^{q\psi/kT}$$

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\epsilon_{si}} [N_A (e^{-q\psi/kT} - 1)]$$

$$-\frac{n_i^2}{N_A} (e^{q\psi/kT} - 1)]$$

**Ψ and $-d\Psi/dx$ are
band bending and
electric field at any
 x inside substrate**

**Multiply both sides by $(d\Psi/dx)dx$
and integrate from bulk towards
the surface**



MOS Electrostatics (NMOS)

MOS

$$\int_0^{d\psi/dx} \frac{d\psi}{dx} d\left(\frac{d\psi}{dx}\right) = -\frac{q}{\epsilon_{si}} \int_0^\psi [N_A (e^{-q\psi/kT} - 1) - \frac{n_i^2}{N_A} (e^{q\psi/kT} - 1)] d\psi$$

$$\left(\frac{d\psi}{dx}\right)^2 = \frac{2kTN_A}{\epsilon_{si}} \left[(e^{-q\psi/kT} + \frac{q\psi}{kT} - 1) + \frac{n_i^2}{N_A^2} (e^{q\psi/kT} - \frac{q\psi}{kT} - 1) \right]$$

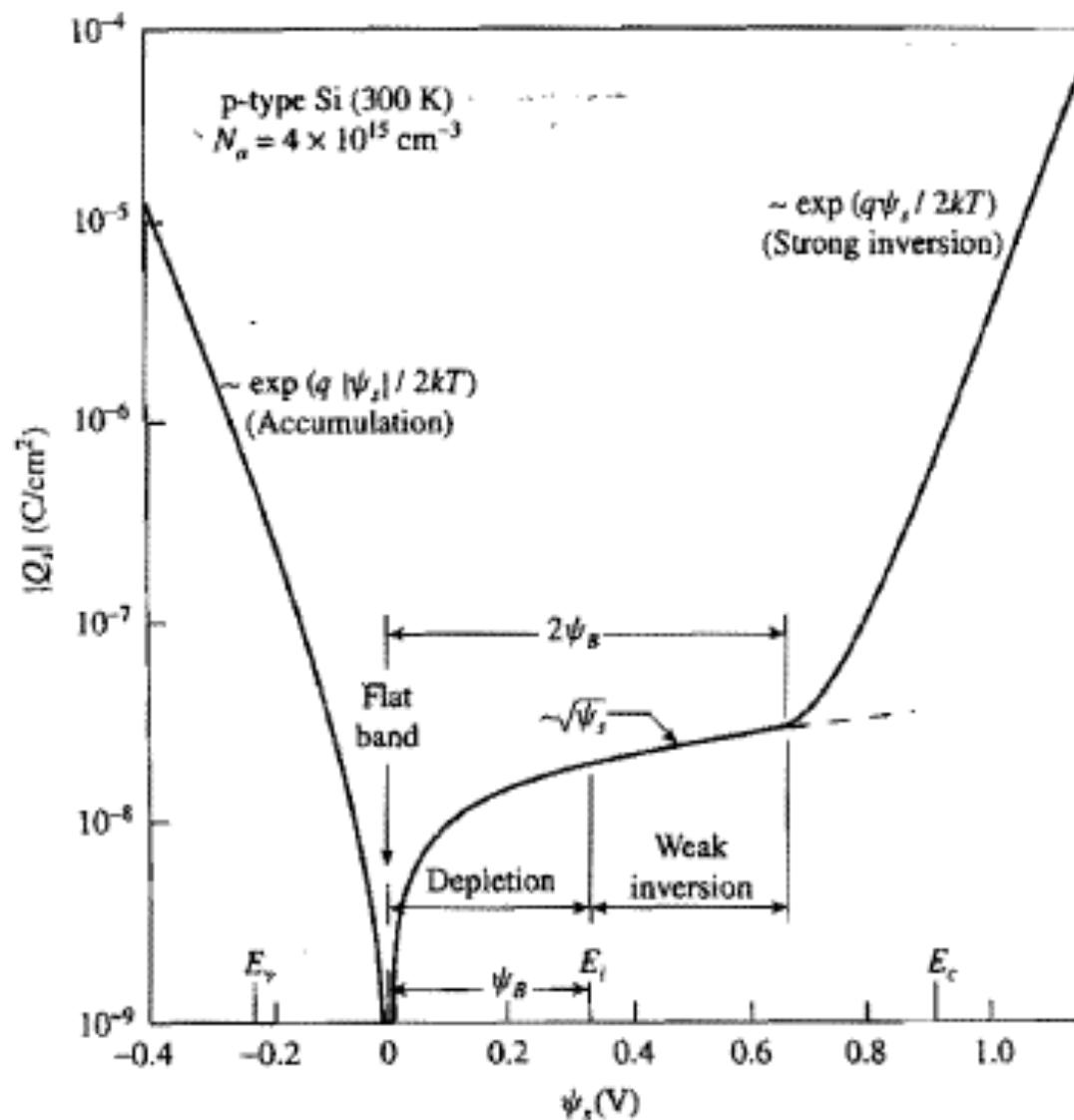
Applying Gauss law for total substrate charge

$$Q = -\epsilon_{si} \left(-\frac{d\psi_s}{dx} \right) = \pm \sqrt{2\epsilon_{si} kTN_A} \left[(e^{-q\psi_s/kT} + \frac{q\psi_s}{kT} - 1) \right.$$

$$\left. + \frac{n_i^2}{N_A^2} (e^{q\psi_s/kT} - \frac{q\psi_s}{kT} - 1) \right]^{1/2}$$

Ψ_s and $-d\Psi_s/dx$ are band bending and electric field at oxide/semiconductor interface

NMOS Channel Charge vs. Surface Potential



Ref: Sze

NMOS Channel Charge vs. Gate Bias

Need numerical solution

$$V_G - V_{FB} - \psi_s = \frac{-Q}{C_{OX}}; \quad V_{FB} = \phi_{MS}$$

$$Q = \pm \sqrt{2\epsilon_{si} kT N_A} \left[\left(e^{-q\psi_s/kT} + \frac{q\psi_s}{kT} - 1 \right) \right.$$

$$\left. + \frac{n_i^2}{N_A^2} \left(e^{q\psi_s/kT} - \frac{q\psi_s}{kT} - 1 \right) \right]^{1/2}$$

in accumulation band bending is negative

**Strong
inversion**

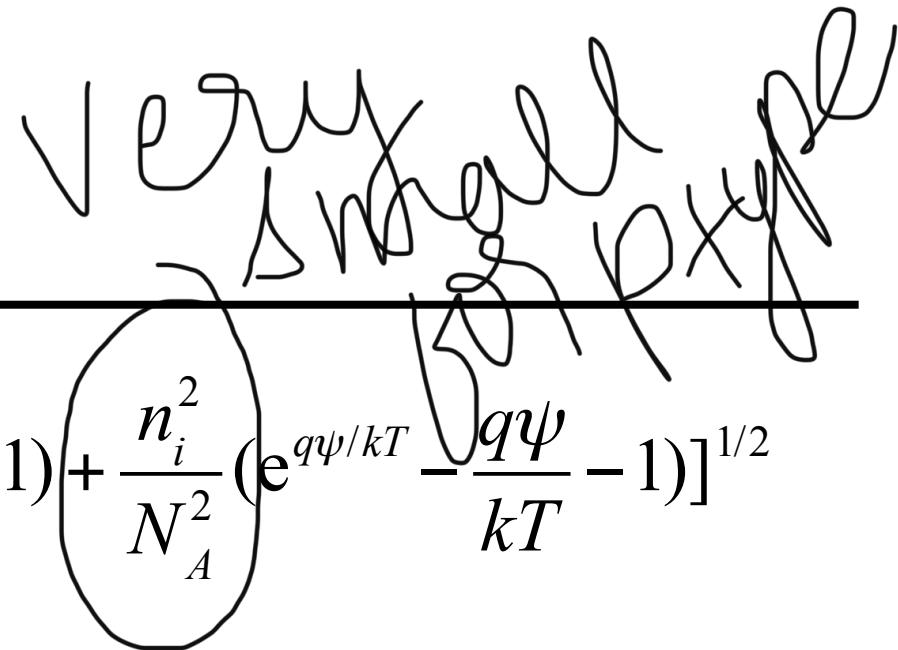
Accumulation

As when ψ is - then it is exp

Depletion

ψ $\rightarrow +ve$

Regime Wise Equations



$$\frac{d\psi}{dx} = \pm \sqrt{\frac{2kT N_A}{\varepsilon_{si}}} \left[\left(e^{-q\psi/kT} + \frac{q\psi}{kT} - 1 \right) + \frac{n_i^2}{N_A^2} \left(e^{q\psi/kT} - \frac{q\psi}{kT} - 1 \right) \right]^{1/2}$$

$$\frac{d\psi}{dx} = + \sqrt{\frac{2kT N_A}{\varepsilon_{si}}} [e^{-q\psi/kT}]^{1/2}$$

Accumulation

$$\frac{d\psi}{dx} = - \sqrt{\frac{2kT N_A}{\varepsilon_{si}}} \left[\frac{q\psi}{kT} - 1 \right]^{1/2} \approx - \sqrt{\frac{2q N_A \psi}{\varepsilon_{si}}}$$

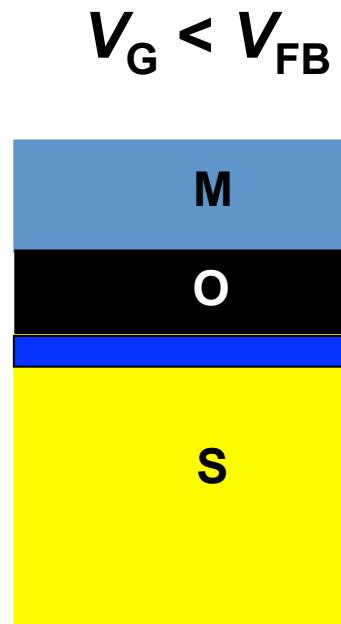
Depletion

$$\frac{d\psi}{dx} = - \sqrt{\frac{2kT N_A}{\varepsilon_{si}}} \left[\frac{q\psi}{kT} + \frac{n_i^2}{N_A^2} e^{q\psi/kT} \right]^{1/2}$$

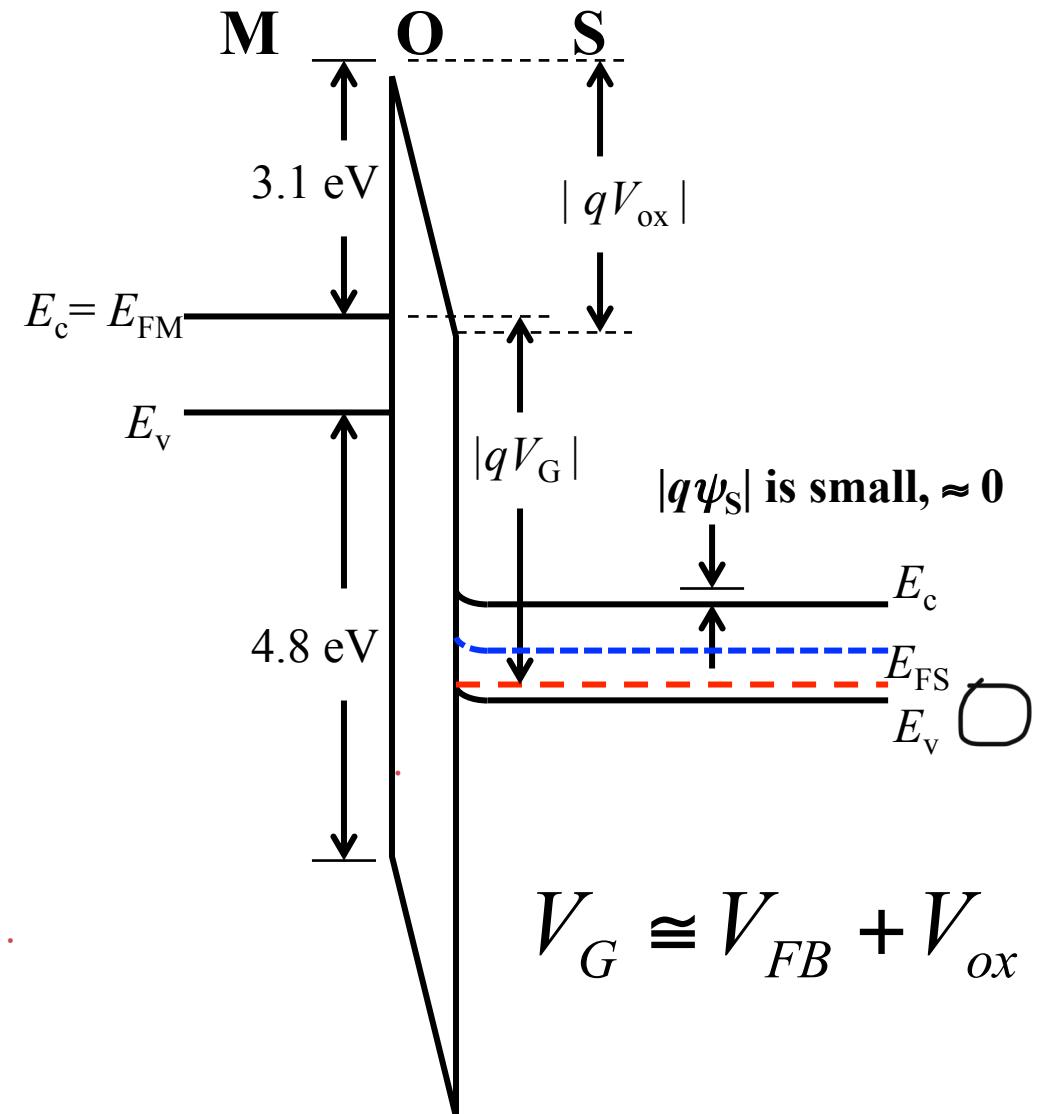
Inversion

As ψ is positive highly

Accumulation (NMOS, N+ Poly-Si Gate)



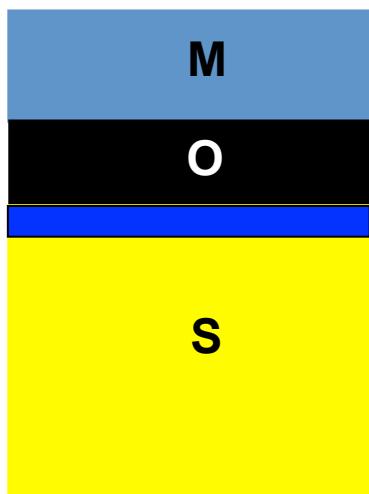
Hole accumulation



In flat band condition the density of carrier at the junction = density at bulk²²

Accumulation Layer Charge Density (NMOS)

$$V_G < V_{FB}$$



$$V_{ox} \cong V_G - V_{FB}$$

From Gauss' Law:

$$E_{ox} = -Q_{acc} / \epsilon_{ox}$$

$$V_{ox} = E_{ox} * T_{ox} = -Q_{acc} / C_{ox}$$

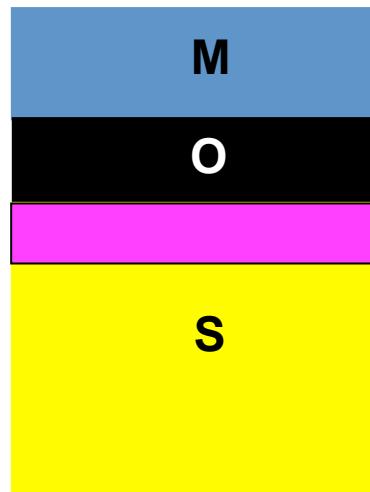
$$C_{ox} = \epsilon_{ox} / T_{ox} \quad (\text{units: F/cm}^2)$$

Hole accumulation

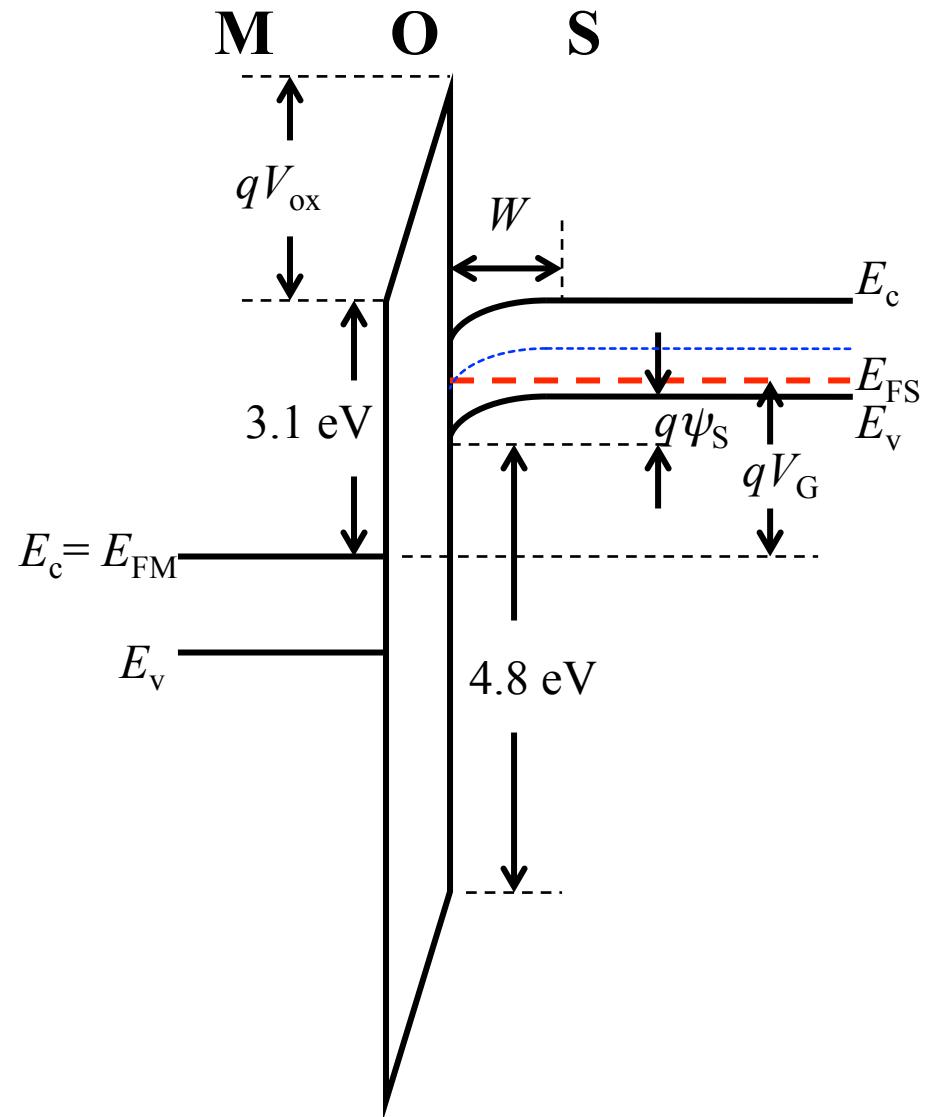
$$\Rightarrow Q_{acc} = -C_{ox}(V_G - V_{FB}) > 0$$

Depletion (NMOS, N+ Poly-Si Gate)

$$V_T > V_G > V_{FB}$$



**Si surface is depleted of mobile carriers (holes)
And surface charge is due to ionized acceptors**



Calculation of Depletion Width

Depletion Approximation: Si surface is depleted of mobile carriers to a depth W .

The charge density within the depletion region is

$$\rho \approx -qN_A \quad (0 \leq x \leq W)$$

Poisson's equation: $\frac{dE}{dx} = \frac{\rho}{\epsilon_{Si}} \approx -\frac{qN_A}{\epsilon_{Si}} \quad (0 \leq x \leq W)$

$$E = \frac{qN_A}{2\epsilon_{Si}} x^2$$

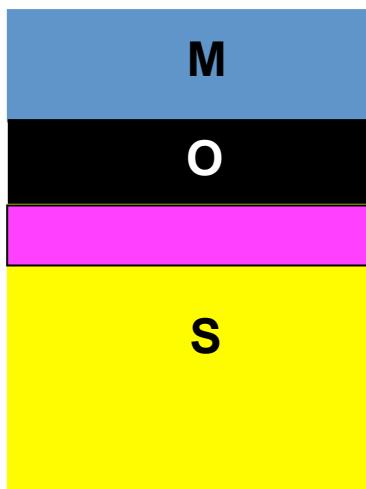
Integrate twice, use $\psi(0) = \psi_s$ and $\psi(W) = 0$

$$\psi_s = \frac{qN_A}{2\epsilon_{Si}} W^2 \Rightarrow W = \sqrt{\frac{2\epsilon_{Si}\psi_s}{qN_A}}$$

How to find ψ_s ?

Voltage Drop in Depletion

$$V_T > V_G > V_{FB}$$



From Gauss' Law:

$$E_{ox} = -Q_{dep} / \epsilon_{ox}$$

$$V_{ox} = E_{ox} * T_{ox} = -Q_{dep} / C_{ox}$$

$Q_{dep} \rightarrow$ integrated Si charge density

$$Q_{dep} = -qN_A W = -\sqrt{2qN_A \epsilon_{Si} \psi_S}$$

$$V_G = V_{FB} + \psi_S + V_{ox} = V_{FB} + \psi_S + \frac{\sqrt{2qN_A \epsilon_{Si} \psi_S}}{C_{ox}}$$

Surface Potential in Depletion

$$V_G = V_{FB} + \psi_S + \frac{\sqrt{2qN_A\epsilon_{si}\psi_S}}{C_{ox}}$$

Solving for ψ_S :

$$\sqrt{\psi_S} = \frac{\sqrt{qN_A\epsilon_{si}}}{\sqrt{2C_{ox}}} \left[\sqrt{1 + \frac{2C_{ox}^2(V_G - V_{FB})}{qN_A\epsilon_{si}}} - 1 \right]$$

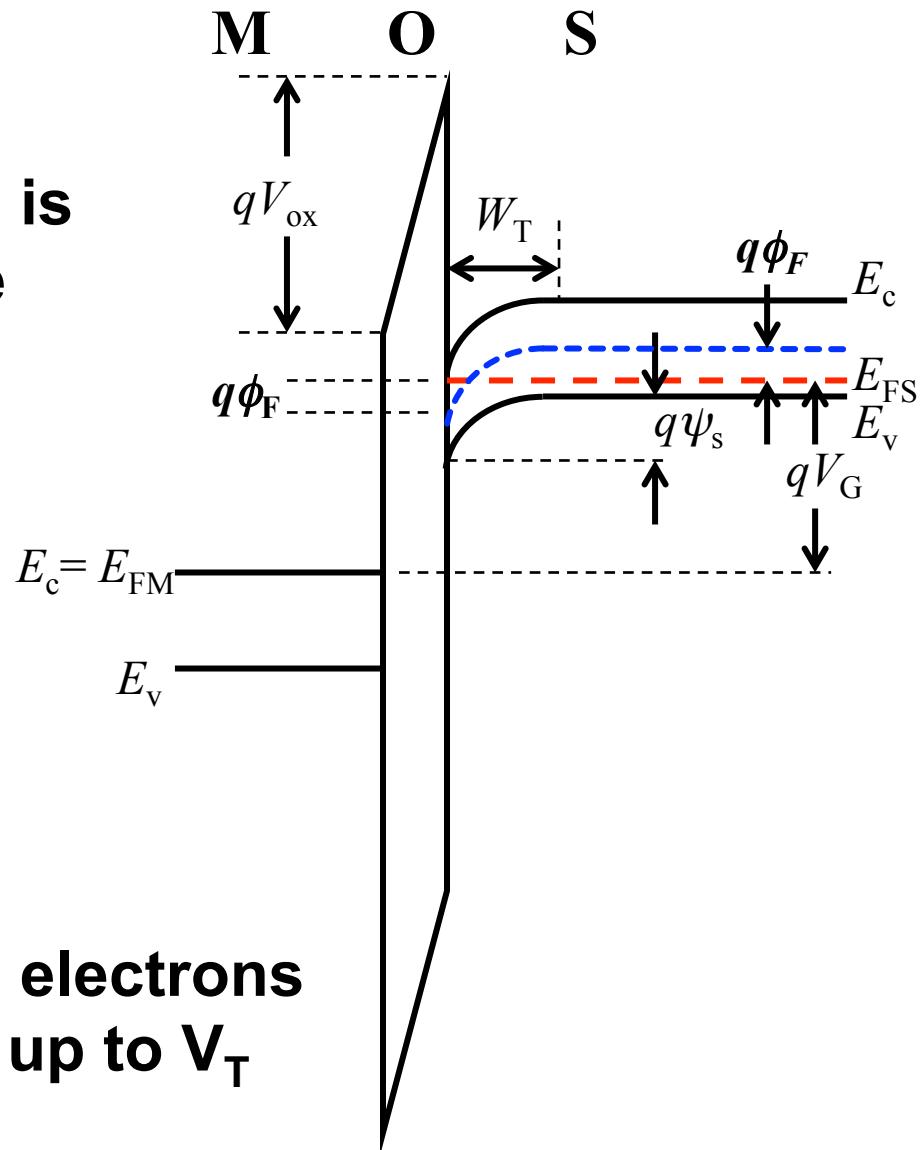
$$\psi_S = \frac{qN_A\epsilon_{si}}{2C_{ox}^2} \left[\sqrt{1 + \frac{2C_{ox}^2(V_G - V_{FB})}{qN_A\epsilon_{si}}} - 1 \right]^2$$

Definition of Threshold

When $V_G = V_T$ (threshold voltage), surface band bending $\psi_s = 2\phi_F \rightarrow$ surface is as much n-type as it were p-type

$$\psi_s = 2\phi_F = 2 \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right)$$

$$W = W_T = \sqrt{\frac{2\epsilon_{Si}(2\phi_F)}{qN_A}}$$



Approximation: No mobile electrons (inversion charges) for V_G up to V_T

Threshold Voltage

- For p-type Si (NMOS):

$$V_G = V_{FB} + \psi_S + V_{ox} = V_{FB} + \psi_S + \frac{\sqrt{2qN_A\epsilon_{si}\psi_S}}{C_{ox}}$$

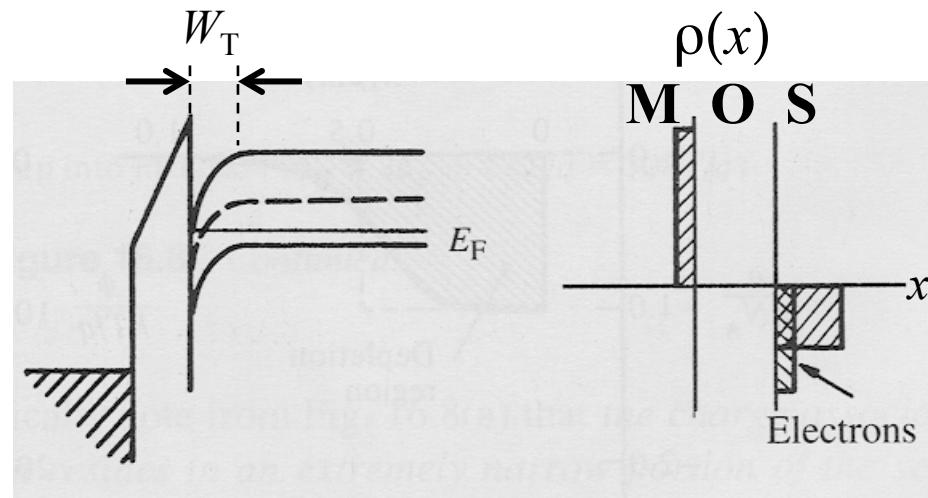
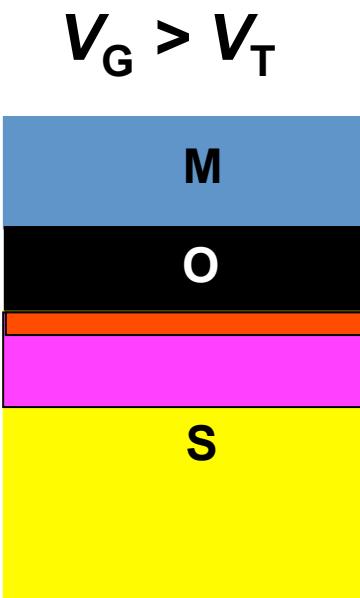
$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\epsilon_{Si}(2\phi_F)}}{C_{ox}}$$

- For n-type Si (PMOS):

$$V_T = V_{FB} + 2\phi_F - \frac{\sqrt{2qN_D\epsilon_{Si}|2\phi_F|}}{C_{ox}}$$

Strong Inversion (NMOS, N+ Poly-Si Gate)

As V_G is increased above V_T , negative charge in the Si is increased by adding mobile electrons (rather than by depleting the Si more deeply), so the depletion width remains \sim constant at $W = W_T$



$$\psi_S \approx 2\phi_F$$

Band-bending gets locked-in

$$W \approx W_T = \sqrt{\frac{2\epsilon_{si}(2\phi_F)}{qN_A}}$$

Inversion Layer Charge Density (NMOS)

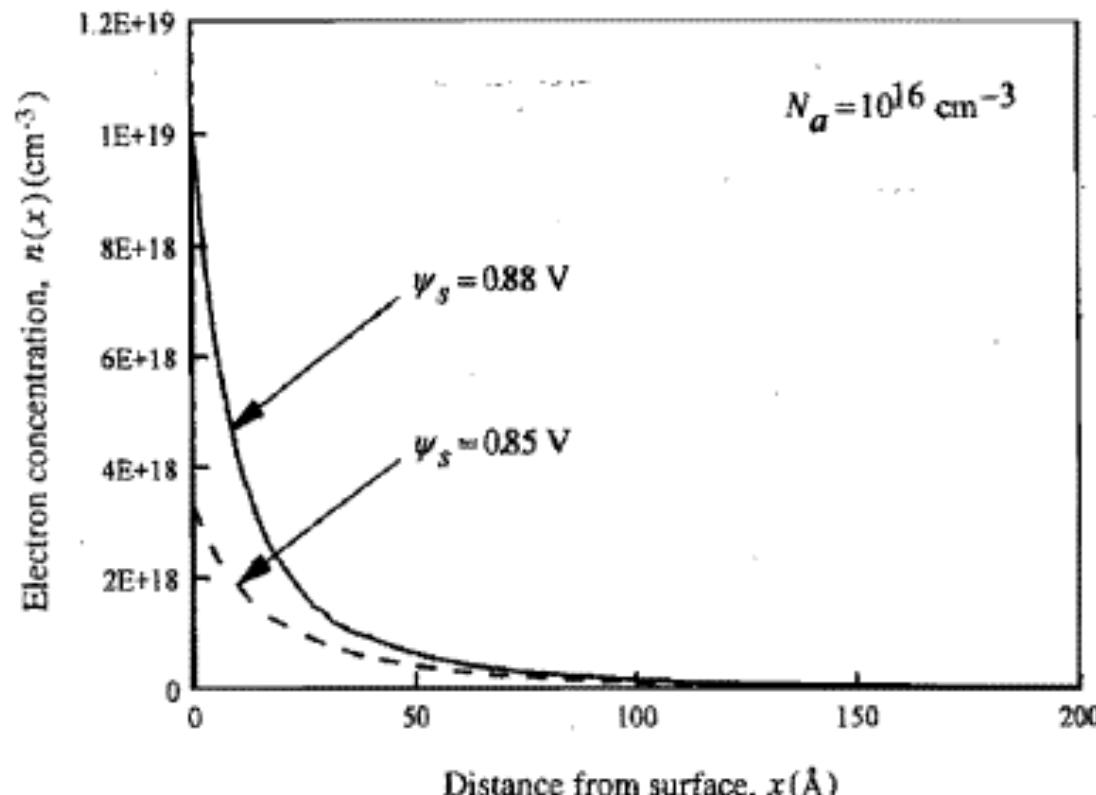
$$\begin{aligned}V_G &= V_{FB} + \psi_S + V_{ox} \\&= V_{FB} + 2\phi_F - \frac{(Q_{dep} + Q_{inv})}{C_{ox}} \\&= V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\epsilon_s(2\phi_F)}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} \\&= V_T - \frac{Q_{inv}}{C_{ox}}\end{aligned}$$

$$\therefore Q_{inv} = -C_{ox}(V_G - V_T)$$

Inversion Layer Thickness

$$\frac{d\psi}{dx} = -\sqrt{\frac{2kTN_A}{\epsilon_{si}}}\left[\frac{q\psi}{kT} + \frac{n_i^2}{N_A^2}e^{q\psi/kT}\right]^{1/2}$$

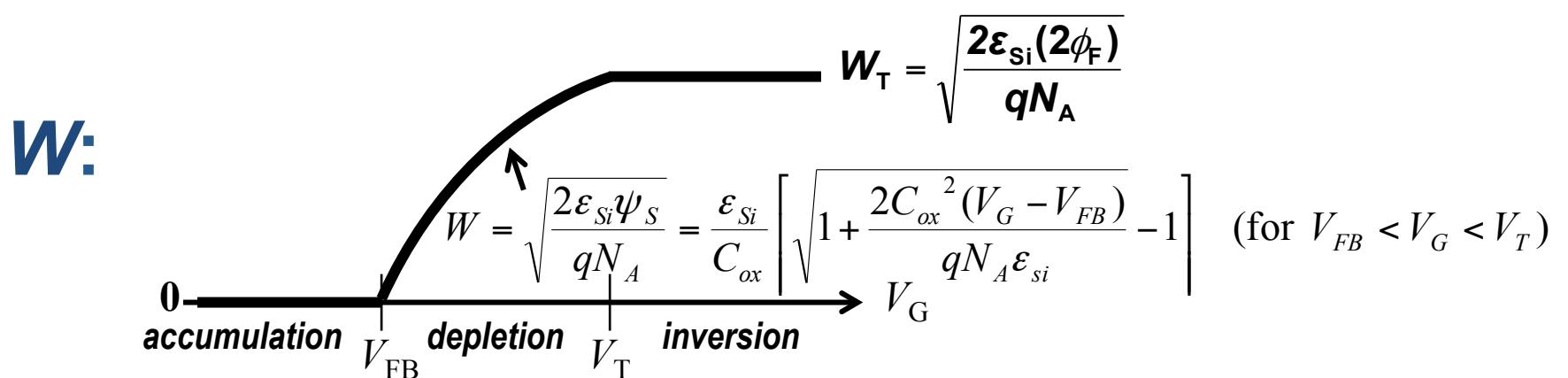
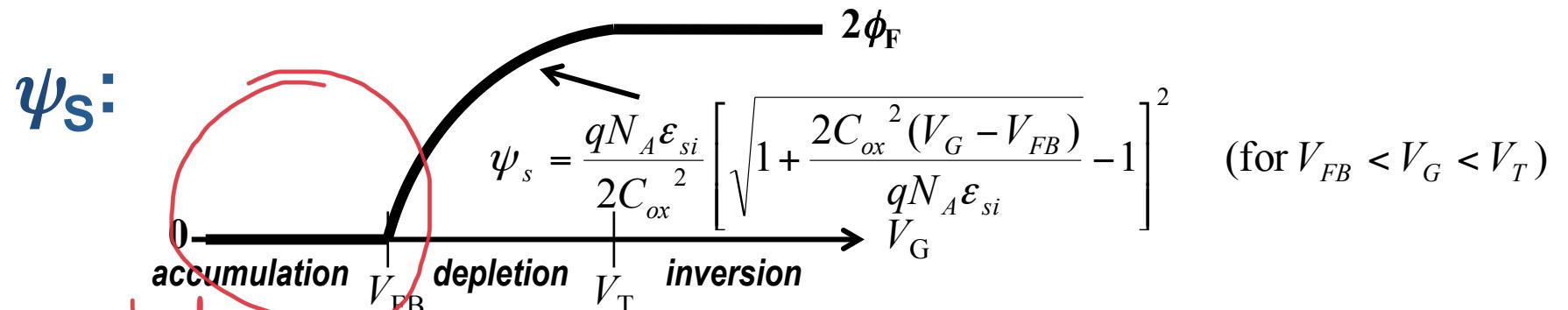
Numerical solution



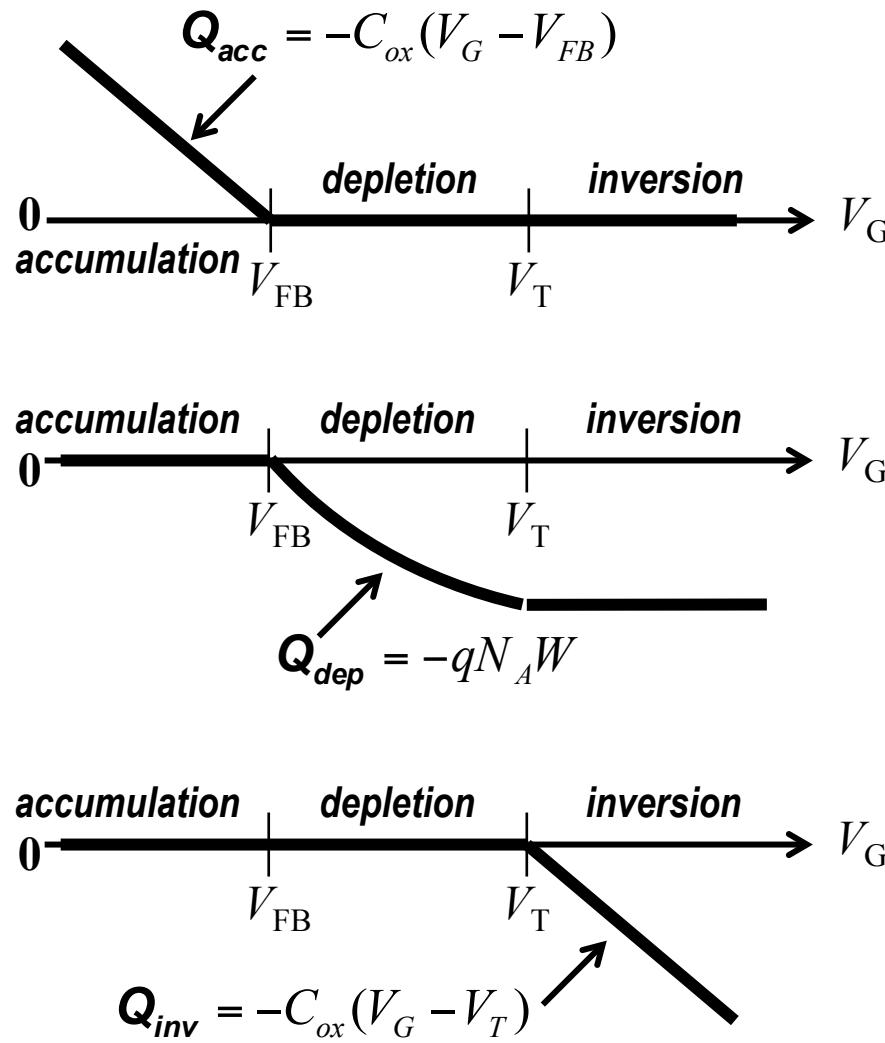
Inversion layer thickness $\sim 50\text{\AA}$, can be approximated as a sheet of charge

Ref: Taur and Ning

Variation of ψ_s and W (NMOS)



Variation of Charge Density (NMOS)



$$Q_s = Q_{acc} + Q_{dep} + Q_{inv}$$

