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EFFECTS OF DIFFUSION CURRENT ON CHARACTERISTICS OF METAL–OXIDE (INSULATOR)–SEMICONDUCTOR TRANSISTORS*

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Abstract—A qualitative discussion of the device operation is first given using three-dimensional energy band diagrams to show the significance of the diffusion current. The theoretical static I–V characteristics are then computed including both the diffusion and the drift currents, based on the one-dimensional and gradual channel model. Drain current saturation phenomena are evident in these exact solutions which are in good agreement with the calculations based on the bulk charge approximation and with the experimental data for the entire non-saturating and saturated ranges. The relative importance of the two current components along the length of the channel is illustrated. The effects of the diffusion current on the three more important low-frequency dynamic characteristics (the short-circuit gate capacitance, the transconductance, and the drain conductance) are discussed. The surface potential, the quasi-Fermi potential, the surface electric field and the surface carrier concentration along the channel are examined. The complete one-dimensional gradual channel model is inadequate to account for the large drain conductance observed in the saturation range, and it is shown that the electric field longitudinal to the channel current flow must be taken into account near the drain junction where it is larger than the transverse field due to the voltage applied to the gate electrode.

Résumé—Une discussion qualitative de l'opération du dispositif est donnée tout d'abord en employant les schémas d'energie de bande à trois dimensions. Les caractéristiques théoriques statiques courant-tension sont ensuite calculées, en comprenant les courants d'apport et d'épuisement, basées sur le modèle à voie graduelle et à une dimension. Les phenomènes de saturation de courant d'épuisement sont évidents dans ces solutions exactes qui sont en accord avec les calculs basés sur une approximation de la charge de base et avec les données expérimentales des gammes complètes saturées et non-saturées. L'importance relative des deux composantes du courant le long de la voie est illustrée. Les effets du courant de diffusion sur les trois plus importantes caractéristiques dynamiques à basse fréquence (la capacité de porte à court-circuit, la transconductance et la conductance d'épuisement) sont discutés. La surface de potentiel, le potentiel quasi-Fermi, le champ électrique de surface et la concentration de porteurs à la surface le long de la voie sont examinés. Le modèle à voie graduelle complet à une dimension n'est pas suffisant pour expliquer la conductance d'épuisement élevée observée dans la gamme de saturation, et on démontre que le champ électrique longitudinal à l'écoulement du courant de voie doit être pris en considération près de la jonction d'épuisement ou il est plus grand que le champ transversal grâce à la tension appliquée à l'électrode de porte.

Zusammenfassung—Zuerst wird die Wirkungsweise der Anordnung qualitativ erklärt. Das geschieht an Hand von dreidimensionalen Energiebanddiagrammen, welche die Bedeutung des Diffusionsstromes aufzeigen sollen. Dann werden die statischen I–V-Kennlinien auf der Grundlage des eindimensionalen gradual channel Modells berechnet. Dabei finden sowohl der Drift- als auch der Diffusionsstrom Berücksichtigung. Die exakten theoretischen Kurven lassen nicht nur die Sättigung des Saugstromes erkennen. Sie stehen auch in guter Übereinstimmung mit Rechnungen

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nach der bulk charge Näherung und experimentellen Resultaten. Das gilt im ganzen Spannungsbereich, d.h. vor und in der Sättigung. Das Verhältnis der beiden Stromanteile über der channel-Länge wird dargestellt. Die Auswirkungen des Diffusionsstromes auf die drei wichtigeren Niederfrequenzkenngrössen werden besprochen. Es sind dies die Kapazität der Steuerelektrode gegen die kurzgeschlossenen Quell- und Saugelektroden, die Steilheit und die channel-Leitfähigkeit. Ferner wird der Verlauf folgender Grossen längs des channel geprüft: Oberflächenpotential, Quasiferminiveau, elektrisches Feld an der Oberfläche, Oberflächenkonzentration der Ladungsträger. Das nur eindimensionale gradual channel Modell kann der beobachteten grossen channel-Leitfähigkeit in der Sättigung nicht gerecht werden. Wie gezeigt wird muss das elektrische Feld in Richtung des channel-Stromes in der Nähe der Saugelektrode in Betracht gezogen werden, wo es grösser ist als das Querfeld, welches von der Steuerelektrode ausgeht.

1. INTRODUCTION

RECENT DEVELOPMENTS in the insulated-gate type of field-effect transistors[1-3] have created some rather interesting and promising device capabilities and potentials. However, some details of the device characteristics are still not well understood especially in the saturation mode. They are more or less in the same state of clarity as Shockley's classical theory[4] although several authors have recently shed some additional light to the current saturation behavior of the insulated-gate type.[5-8]

Whether in the junction type or the insulated-gate type, it has been customary to assume that the drift component of the channel current is the only dominant term. Such an assumption is valid as long as the transistor is not operating in saturation. At saturation or beyond, difficulties arise in this drift model due to depletion of carriers in the pinch-off region, necessitating a rapid increase of the electric field along the channel towards the drain junction in order to maintain a constant saturation drain current observed experimentally. GROSVALET *et al.*[9] have suggested that the saturation current in the junction-gate type is due to the limiting drift velocity effect in the pinch-off region. This is a plausible interpretation only for short channels whose width is greater than the length, but it cannot account for the current saturation effect in the long and thin channel structure. A similar limiting velocity treatment has been carried out by ROOT and VADASZ[10] for the MOS structure, but their calculated I–V characteristics deviate widely from those observed experimentally. A detailed analysis of the effect of surface scattering which extends Schrieffer's model[11] to include the exact transverse field, and the multi-valley band structure shows that our data can be accounted for by complete diffused scattering. A more quantitative theory which shows current saturation was proposed by WRIGHT[8,12] who asserted that the channel current in the pinch-off region is carrier space-charge-limited. Wright's model is applicable mainly for dielectric channel or for semiconducting channels which are essentially intrinsic. More recently GEURST[13] derived a single equation to describe the channel based on Wright's model. Experimental evidences, however, have shown that the pinch-off region is essentially depleted of carriers for extrinsic semiconductor channels.[6] As PRIM and SHOCKLEY[14] have pointed out, when the depletion region extends out into the channel, a two dimensional potential model has to be taken into account. The solution to the two-dimensional Poisson equation was shown to be rather complicated. Furthermore, it actually depicts only the continuity of the electric field by arbitrarily fixing a set of boundary conditions, but fail to account for the current continuity or the "intrinsic" saturation behavior. In this paper, the general solution including the diffusion current predicts the current saturation phenomenon in the metal–insulator–semiconductor (MIS) transistor. The physical model for this saturation effect is considered in detail.

2. QUALITATIVE ANALYSIS OF DEVICE OPERATION[15]

Let us first examine the different modes of operation of an MOS transistor by means of three-dimensional energy band diagrams. Figure 1(b) shows the equilibrium case. A flat band condition is assumed, i.e. the influence of the surface states and the work function differences are neglected. The Fermi level lies very close to the conduction band edge in the N^+ regions (below for an impurity concentration of 10^{19} cm^{-3} and above for 10^{20} cm^{-3}), but crosses midway between the

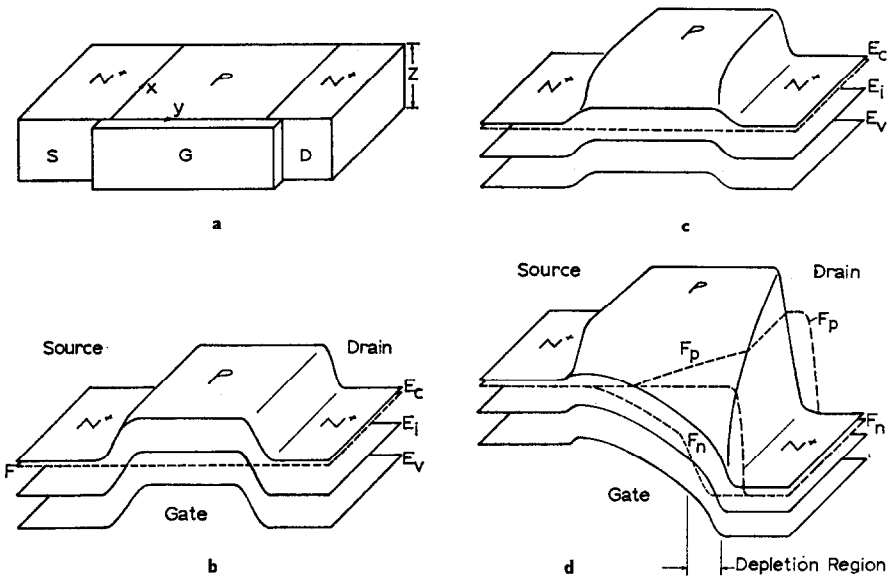


FIG. 1(*a*). A sketch of the physical structure of an *N*-channel MOS transistor. (*b–d*) Three-dimensional energy band diagrams depicting (*b*) the flat-band zero-bias equilibrium condition, (*c*) the equilibrium condition under a gate bias and (*d*) the equilibrium condition under both drain and gate biases.

intrinsic Fermi level and the valence band edge in the *P* region. When a positive voltage is applied at the gate electrode, the energy band at the surface is bent down or the Fermi level surface is raised. Depending on the gate bias and the substrate impurity concentration, the surface band bending may be such that the Fermi level at the surface crosses the intrinsic Fermi level as illustrated in Fig. 1(c), and a channel is formed. The Fermi level is still flat across the device because there is no current flow. When a positive bias is applied to the drain electrode, the energy level at the drain junction is pulled down. With current flow, quasi-Fermi levels are used to express the electron and hole concentrations. The hole quasi-Fermi level is essentially unperturbed* in the channel and drops rapidly towards F_n in the drain region while the electron quasi-Fermi level is almost in parallel to the band edges or the intrinsic Fermi level, however, as it approaches the pinch-off region, it falls very rapidly below the intrinsic Fermi level, such as that shown in Fig. 1(d) for a saturated case.

Let us examine the current continuity along the channel when the device is operating in saturation. At the source end, the channel is still open and the drift component is the dominant term. As we get closer to the drain junction electron concentration decreases. At the drain junction, the carriers are almost completely depleted. Unless there is an extremely large field ($> 10^6$ V/cm) the drift current alone cannot sustain the observed saturation current. It is at this "bottleneck" of the channel that diffusion current component becomes significant and cannot be neglected. The carrier concentration may be small but the gradient of the concentration is extremely large. The saturation current going through this depletion pinch-off point is governed by the bulk impurity concentration, the oxide thickness and the channel mobility. With these parameters known, one can easily predict the saturation current. Beyond the pinch-off point there exists a depletion region which is

* The constancy of the hole quasi-Fermi level, F_p, has been discussed in detail[15] based on zero recombination. For finite recombination and hence finite hole current, F_p must still be essentially constant in the channel since the hole current is negligible compared with the electron current. The finite recombination case is similar to the situation in the base region of a bipolar transistor.

really an extension of the reverse biased drain junction. When the carriers diffuse across the pinch-off point, it is immediately swept across the depletion region, a situation similar to the collector junction of a conventional transistor. Thus, the current continuity is achieved as follows: the carriers are injected from the source junction; drift down the open channel until they reach the depletion region; and are then swept away into the drain junction. This model will now be demonstrated quantitatively.

3. DRAIN CURRENT

The drain current is the most important device parameter of the field-effect device. It may be obtained by integrating the total current density over the cross-sectional area of the channel.[15]

$$I_D = \int_0^{x_i} J(x, y) z \, dx \tag{1}$$

where x_i is the intrinsic point beyond which the electron concentration is negligible and the total current density $J(x, y)$ of an N-Channel device comes essentially from the electron current density:

$$J(x, y) = J_n + J_p \cong J_n = q\mu_n n E_y + qD_n \nabla n = -qD_n n \nabla \xi \tag{2}$$

where ξ is the electron quasi-Fermi level measured from the bulk Fermi level and normalized to kT/q. The total drain current is then

$$I_D = \frac{1}{L} \int_0^L D_n q Z \left(\frac{d\xi}{dy}\right) \int_0^{x_i} n(x, y) dx dy$$

$$= \left(\frac{kT}{q}\right)^2 \left(\frac{C_0 Z}{2L}\right) \gamma \mu_n \int_0^{U_D} \int_{U_F}^{U_s} \frac{e^{U-\xi-U_F}}{F(U, \xi, U_F)} dU d\xi \tag{3}$$

Here $\gamma = U_s/|U_s|(C_D/C_0)$, $C_D = K_s \epsilon_0 / L_D$, $L_D =$ intrinsic Debye length, $Z =$ channel width, $L =$ channel length, $\mu_n =$ carrier mobility. U, U_s, ξ, and U_F are the electrostatic potential, the surface potential, the electron quasi-Fermi potential and the equilibrium Fermi potential in the bulk, all normalized to kT/q. U_D is the drain voltage also in units of kT/q. The $F(U, \xi, U_F)$ function is the normalized electric field obtained from the solution of Poisson equation worked out in the Appendix. The gate voltage in units of kT/q is U_G and is related to the surface potential U_s through the Kirchoff voltage law.

$$U_G' = (q/kT)(V_G - \phi_{MS'} + Q_{ss}/C_0) = U_s + \gamma F(U_s, \xi, U_F) \tag{4}$$

For a particular device, equation (4) may be calculated numerically. The input data are: the bulk impurity concentration N_A, the physical dimensions of the device and the constant effective carrier

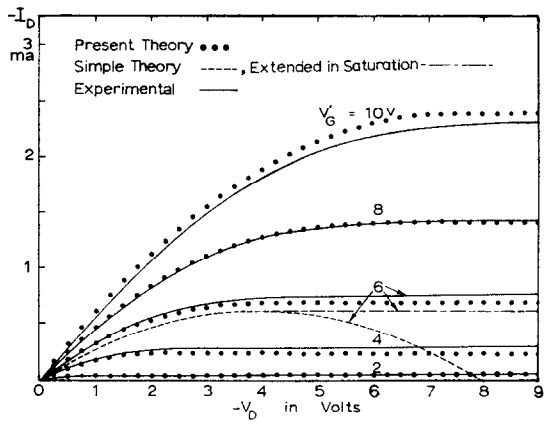


FIG. 2. The theoretical and experimental drain characteristics of a P-channel MOS transistor having $x_0 = 0{\cdot}2\ \mu$; $N_D = 4{\cdot}6 \times 10^{14}\ \text{cm}^{-3}$; $\mu_p = 256\ \text{cm}^2/\text{V-sec}$ and area $= 8{\cdot}4 \times 10^{-4}\ \text{cm}^2$.

mobility obtained experimentally from a straight-line approximation of the drain-conductance vs. gate voltage curve. A typical result is illustrated in Fig. 2. It demonstrates the current saturation phenomena very well. Unlike most of the previous published theories, in which the solutions have had to be cut-off at the pinch-off point, this solution is valid for the entire range of drain voltage. For comparison, the experimental data and the simple theory are plotted on the same graph. They match each other closely in the non-saturating region, but beyond the pinch-off point the simple theory breaks down. However, the bulk charge approximation[16] gives characteristics almost identical to the results presented here. A simple example is given in Fig. 3. The slight deviation between the results

calculated from the present theory and the experimental values shown in Fig. 2 are believed to come from the transverse and longitudinal field-dependent surface mobility since the MOS capacitance–voltage curve shows only a small surface state charge effect.

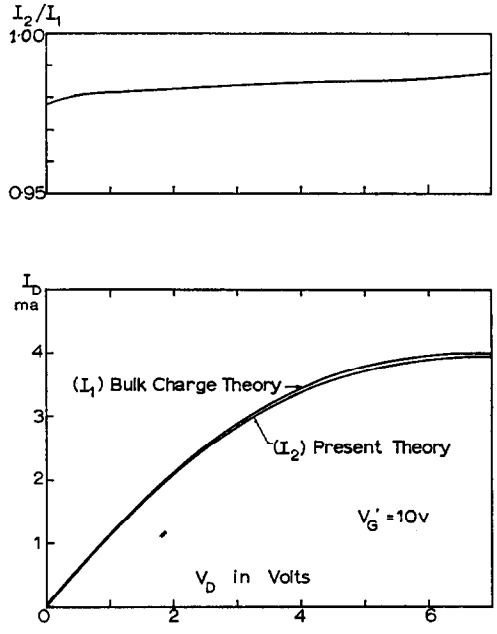


FIG. 3. Comparison of the drain current calculated from the bulk charge method and the present method.

The relative importance of the two components can be easily illustrated from the ratio

$$\begin{aligned} D_n(\mathrm{d}n/\mathrm{d}y)/\mu_n n E_y &= (\mathrm{d}n/\mathrm{d}\xi)(\mathrm{d}\xi/\mathrm{d}y)/n(\mathrm{d}U_s/\mathrm{d}y) \\ &= (1-\mathrm{d}U_s/\mathrm{d}\xi)/(\mathrm{d}U_s/\mathrm{d}\xi) \\ &= (N_A-p_s)/n_s \end{aligned} \tag{5}$$

where N_A is the impurity concentration in the P-type substrate, p_s and n_s are the carrier concentrations at the semiconductor surface. Near the source junction in the channel, $n_s \gg N_A$, and the diffusion current component can be neglected while in the depletion region, $n_s \ll N_A$ so that the diffusion component must be taken into account.

Very often, in the narrow channel devices ($< 10\,\mu$) the saturation current does not level-off as that illustrated in Fig. 2. This is due to the space charge region widening effect[5,6] which shortens the effective length of the channel. For those cases, the channel length L must be replaced by an effective channel length, depending on the impurity concentration gradient of the drain junction.

4. OTHER DEVICE PARAMETERS

Several important device parameters are computed in this section. In our previous paper,[16] we had to use three different solutions to calculate these characteristics, one each to describe the different modes of operation. The addition of the diffusion component, however, gives us a complete solution without the use of the three-voltage-range approximation.

The analytical expression for C_{GS} may be obtained from $C_{GS} = (\partial Q_G/\partial V_G)V_D$, where Q_G is the total charge on the metal gate electrode for a given bias condition. Making use of the charge neutrality condition, we have

$$Q_G = Q_s + (Q_{ss} + Q_0)$$

or

$$Z\int K_0\epsilon_0 E_0\,\mathrm{d}y = Z\int K_s\epsilon_0 E_s\mathrm{d}y + (Q_{ss}+Q_0) \tag{6}$$

where $(Q_{ss}+Q_0)$ is the charge in the interface surface states and the oxide, and Q_s is that in the semiconductor. From equations (A-11) and (1), one can formulate the expression for Q_G.

$$Q_G = \frac{C_D}{I_D'}\left(\frac{kT}{q}\right)\int_0^{U_D}\int_{U_F}^{U_s} F(U_s, \xi, U_F) \times \frac{e^{U-\xi-U_F}}{F(U,\xi,U_F)}\,\mathrm{d}U\mathrm{d}\xi \tag{7}$$

where I_D' is the normalized drain current. The short circuit gate capacitance normalized to the

oxide capacitance C_0 is:

$$\frac{C_{Gs}}{C_0} = 1 - \frac{1}{I_D'}\int_0^{U_D} \frac{F(U_s,\xi\ U_F)\left(\int_{U_F}^{U_s} \frac{e^{U-\xi-U_F}}{F(U,\xi,U_F)}dU\right)d\xi}{F(U_s,\xi,U_F)+(\gamma/2)(e^{U_s-\xi-U_F}-e^{U_F-U_s}+e^{U_F}-e^{-U_F})}$$

$$+\frac{\gamma}{I_D'}\int_0^{U_D} e^{U_s-\xi-U_F}\left(\frac{F(U_s,\xi,U_F)}{F(U_s,\xi,U_F)+(\gamma/2)(e^{U_s-\xi-U_F}-e^{U_F-U_s}+e^{U_F}-e^{-U_F})}\right)d\xi$$

$$-\frac{\gamma}{I_D'^2}\left[\int_0^{U_D} F(U_s,\xi,U_F)\int_{U_F}^{U_s}\frac{e^{U-\xi-U_F}}{F(U,\xi,U_F)}dU d\xi\right].$$

$$\left[\int_0^{U_D}\frac{e^{U_s-\xi-U_F}\,d\xi}{F(U_s,\xi,U_F)+(\gamma/2)(e^{U_s-\xi-U_F}-e^{U_F-U_s}+e^{U_F}-e^{-U_F})}\right] \tag{8}$$

Here we have assumed that Q_{ss} is a constant, independent of the applied voltages. For a given device, with the device geometry and the bulk impurity concentration known, one can evaluate C_{GS} for any bias condition. However, a considerable amount of computer time was required to do the numerical integration especially in the saturation and the cut-off regions. The solutions of equation (8) not only show all the detailed multi-extrema structure of the capacitance in the three voltage ranges, but also agree remarkably well with the experimental data as evident in the typical example for an N-channel device illustrated in Fig. 4. Because of the complexity of equation (8), it is difficult to isolate or distinguish the individual influence of the diffusion current in each part of the capacitance characteristics, but qualitatively the inclusion of the diffusion current provides us with a non-diverging electric field at saturation so that the input capacitance has no singularities at these points.

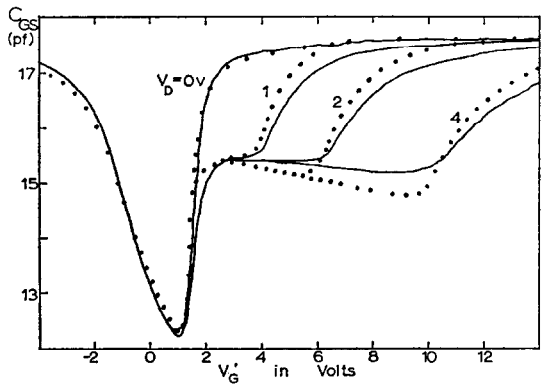


FIG. 4. The theoretical and experimental short circuit gate capacitance characteristics of an N-channel MOS transistor having $x_0 = 0{\cdot}17\ \mu$; $N_A = 1{\cdot}57\times10^{16}\ \text{cm}^{-3}$; and area $= 8{\cdot}4\times10^{-4}\ \text{cm}^2$.

The transconductance, g_m, may be readily derived from equations (3) and (4).

$$J_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D} = \left(\frac{\partial I_D}{\partial U_s}\right)_{V_D}\cdot\left(\frac{\partial U_s}{\partial V_G}\right)_{V_D}$$

$$= \frac{\mu_n C_0 Z}{L}\left(\frac{kT}{q}\right)\left(\frac{\gamma}{2}\right)\int_0^{U_D}\frac{e^{U_s-\xi-U_F}}{F(U_s,\xi,U_F)+(\gamma/2)(e^{U_s-\xi-U_F}-e^{U_F-U_s}+e^{U_F}-e^{-U_F})} \tag{9}$$

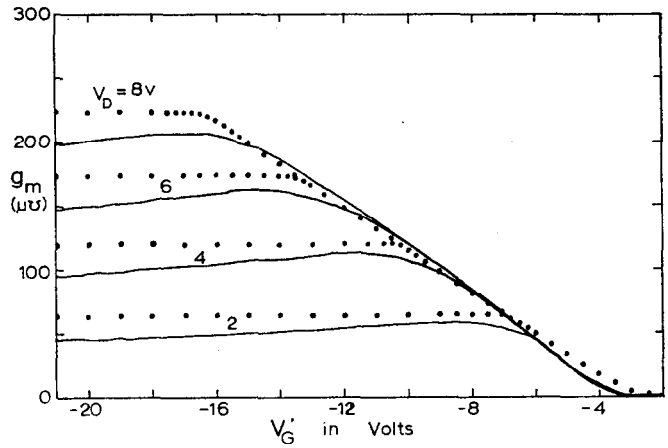


FIG. 5. The theoretical and experimental transconductance characteristics of a *P*-channel MOS transistor having $x_0 = 0{\cdot}62\ \mu$; $N_D = 6{\cdot}43 \times 10^{14}$ cm^{-3}; $\mu_p = 326$ cm^2/V-sec and area $= 8{\cdot}4 \times 10^{-4}$ cm^2.

To calculate equation (9) for a given set of V_D and V_G, it is necessary to evaluate first the U_s through the Kirchoff voltage relationship of equation (4). The theoretical and experimental g_m curves are compared in Fig. 5. The rounding off at the saturation points is clearly displayed. For very high gate voltage, the observed discrepancy is believed to be mostly due to the field dependent carrier mobility. Here again, the same solution for the entire range of voltage is used.

Let's examine the transconductance in terms of the surface potential as shown in equation (9). With the sustained drain saturation current provided by the diffusion component, one finds that the surface potential varies in the same manner as the drain current, which means that the term $(\partial I_D/\partial U_s)_{V_D}$ is essentially a constant throughout. However, the variation of U_s with respect to V_G is very large, it starts from zero at the flat-band case ($U_s = 0$, $V_G = 0$) and increases rapidly until the device goes out of saturation. After that it gradually levels off. In other words, the transconductance is essentially a measure of the change of surface potential with respect to the gate voltage. Only with the inclusion of the diffusion component can one establish the relationship where the surface potential and the drain current have the same positional dependence along the channel.

The drain conductance g_d may be obtained either from the definition $g_d = (\partial I_D/\partial V_D)_{V_G}$ or from the total mobile charge Q_n evaluated at the drain terminal.[15]

$$g_d = \frac{\mu_n c_0 Z}{L}\left(\frac{kT}{q}\right)\frac{\gamma}{2}\int_{U_F}^{U_s(U_D)} \frac{e^{U-U_D-U_F}}{F(U,U_D,U_F)}\,dU \tag{10}$$

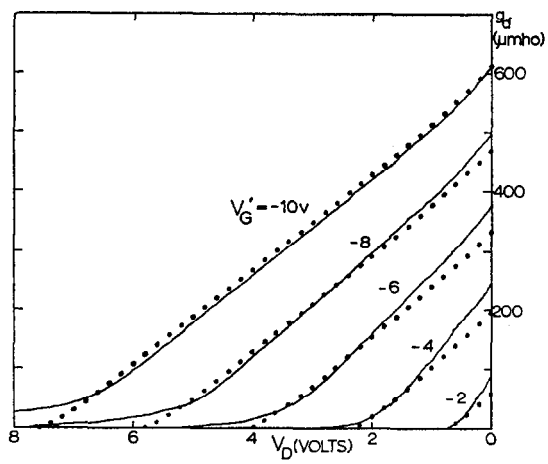


FIG. 6. The theoretical and experimental drain conductance of a *P*-channel MOS transistor having $x_0 = 0{\cdot}21\ \mu$; $N_D = 1{\cdot}56 \times 10^{15}$ cm^{-3}; $\mu_p = 343$ cm^2/V-sec and area $= 8{\cdot}4 \times 10^{-4}$ cm^2.

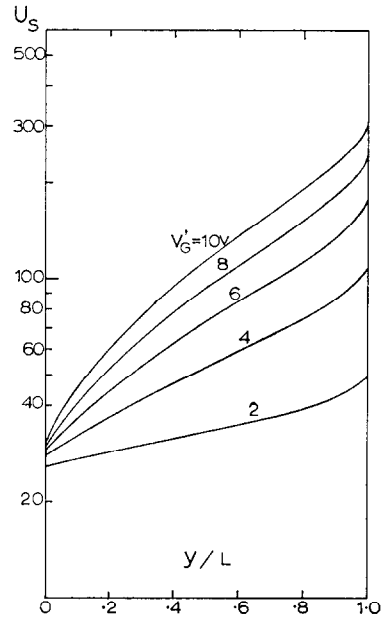


FIG. 7. The normalized surface potential U_s along the channel with the transistor operating just in saturation. (Curves in Figs. 7–10 are calculated using the same set of device parameters: $x_0 = 0{\cdot}2\ \mu$; $N_D = 4{\cdot}6 \times 10^{14}$ cm^{-3}; $L = 70\ \mu$; $Z = 1200\ \mu$).

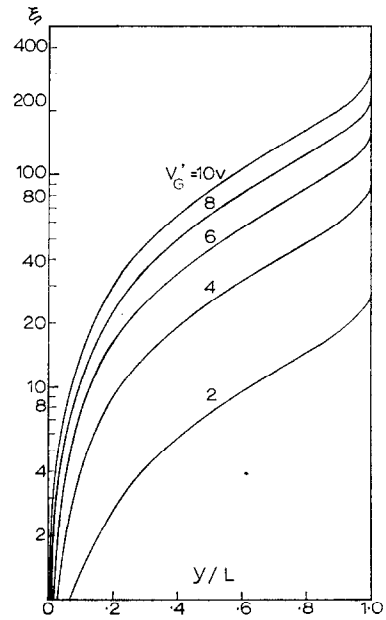


FIG. 8. The normalized quasi-fermi level ξ along the channel with the MOS transistor operating just in saturation.

Note that the drain conductance is given by the conductance evaluated at the drain junction where the diffusion current becomes important at saturation. For drain voltage beyond the saturation point, the diffusion-current-limited region (the bottleneck) would move towards the source as the depletion region extends into the channel. Figure 6 shows a typical drain conductance characteristics of the P-channel device, having g_d plotted as a function of V_D with V_G as a parameter. The residual drain conductance which is the major discrepancy between the theoretical curves calculated from equation (10) and the experimental curves is mainly due to the shrinkage of the effective channel length, which provides a finite drain conductance beyond saturation. Other factors like the inhomogeneity in the impurity concentration and oxide thickness in the channel, soft drain junction, surface states, etc. may all contribute to the observed finite conductance. Of course, if the device is driven way into saturation, hot electron effects may also be important.

5. SOME ELECTROSTATIC PROPERTIES

There are several electrostatic properties of the channel whose variation along the channel is of considerable interest. These are the surface potential, U_s, the quasi Fermi potential, ξ, the surface electric field, $F(U_s, \xi, U_F)$, and the surface carrier concentration n_s. By integrating equation (1) with respect to ξ and setting an arbitrary limit to ξ, the normalized distance along the channel measured from the source, y/L, may be related to ξ.

$$\frac{y}{L} = \frac{1}{I_D'} \int_0^{\xi} \int_{U_F}^{U_s} \frac{e^{U-\xi-U_F}}{F(U, \xi, U_F)} \, dU d\xi = \frac{I_D'(\xi)}{I_D'(U_D)} \tag{11}$$

Note that y/L is the dependent variable and it is also the ratio of the total current components up to the point ξ over the total current components in the entire open channel. Thus, this relationship is not valid in the pinch-off region. In Fig. 7, the normalized surface potential U_s is plotted for fixed gate voltages while the drain is maintained saturated in all the cases. The drain voltage is

mainly responsible for the large change in U_s along the channel. The gate voltage can only lower the surface potential up to near the bulk Fermi level of the N^+ regions. Further increase would result in a spill-over of electrons to the drain or source islands. In the illustration shown, U_s increases steadily as one goes from the source to the drain, with the change being the fastest near the drain end. In Fig. 8, a similar plot is given for the electron quasi Fermi level. Let's compare the two figures for a particular V_G, say 10 V. At the source point, i.e. $y/L = 0$, the difference is about 30 units of kT/q. U_s can be taken as the bottom of the potential well and ξ the top of the channel. Even at $y/L = 0{\cdot}8$ the difference is still about 28 units of kT/q. It is only beyond $y/L = 0{\cdot}9$ that the carriers rapidly decrease towards the intrinsic concentration or F_n approaches E_i. Another way of showing this behavior is the plot of surface electron concentration given in Fig. 9. The expression for the concentration is:

$$n_s = n_i \exp[U_s - \xi - U_F] \qquad (12)$$

These all lead to further verification of the existence of the diffusion current.

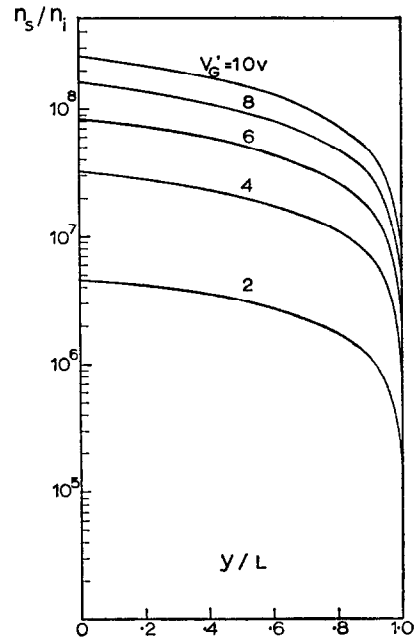
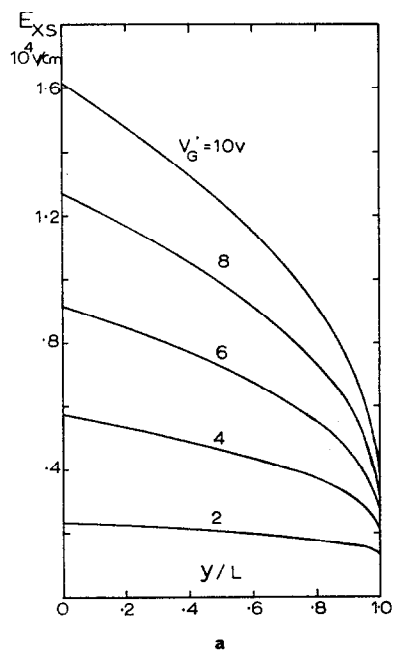


FIG. 9. The surface electron concentration along the channel with the MOS transistor operating just in saturation.



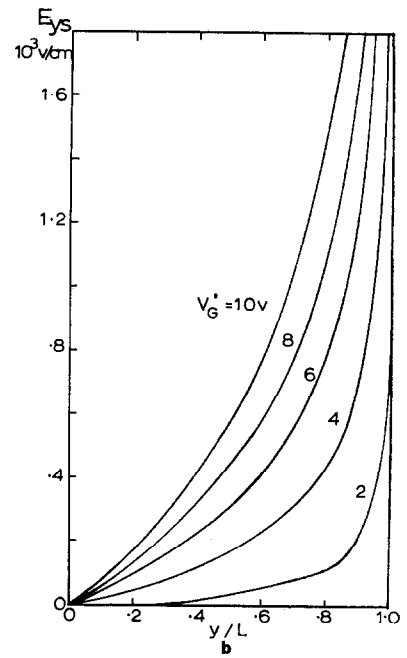


FIG. 10. The (*a*) transverse and (*b*) longitudinal electric field at the surface along the channel with the MOS transistor operating just in saturation.

The variation of the electric field, E_{xs} [expression derived in the Appendix] along the channel is plotted in Fig. 10(a). It is interesting to note that the field decreases as it goes towards the drain. If one examines the energy band diagram of Fig. 1(c) closely, it becomes evident for a cross-section near the source, the band-bending is narrow and very sharp whereas for one near the drain, the band-bending extends further into the semiconductor, resulting in a lower electric field. Of course, this gradual band-bending is also responsible for the pinch-off of the channel. The longitudinal electric field E_y, as one would predict, increases as it approaches the drain. The expression may be derived with the aid of equations (3) and (4) as shown in the Appendix. Figure 10(b) illustrates the variation of E_y along the channel. The scale of Fig. 10(a) is one order of magnitude greater than that of Fig. 10(b). It is evident that E_y is much smaller than E_x along most part of the channel. However, once it gets near the pinch-off point, it is no longer negligible. From that point on, one can either assume it to be the same as that in the depletion layer of an p–n junction or solve the two-dimensional Poisson equation as suggested by SHOCKLEY[4] and demonstrated by GUERST[13] for a case in which the bulk impurity concentration is assumed zero. The latter approach has the disadvantage of being rather complicated and involved.

In Fig. 11, the ratio of the longitudinal field to the transverse field normalized with respect to $(x_0/2L)(K_s/K_0)$ is plotted for different bulk impurity concentrations. This points out that the higher the concentration, the harder it is to pinch-off the channel. It also shows explicitly that for devices with small values of the ratio $(x_0/2L)$, this one-dimensional approximation should be valid for most of the possible bias conditions.

6. CONCLUSION

The inclusion of the diffusion current component has provided not only the current continuity along the channel but also the current saturation phenomenon, making the solution valid for the entire range of operation, from the cut-off mode through saturation to the non-saturating mode. These are the main features of adding the diffusion current. For very short channel devices, the channel length shrinkage effect is still the dominating factor that produces the finite resistance beyond saturation.

The results given here have been compared with those obtained using the voltage-dependent bulk change approximation method.[16] Almost identical numerical results are found although in the bulk charge case the solutions must be calculated in three bias ranges and then piece-mealed together. Nevertheless it indicates that the bulk charge model is a good approximation to the more exact solution presented here. Since an extensive quantitative theory–experiment comparison has been treated in our previous paper,[16] only typical examples have been given here. For device design purpose, it is much simpler and more economical to use expressions derived from the bulk charge method.

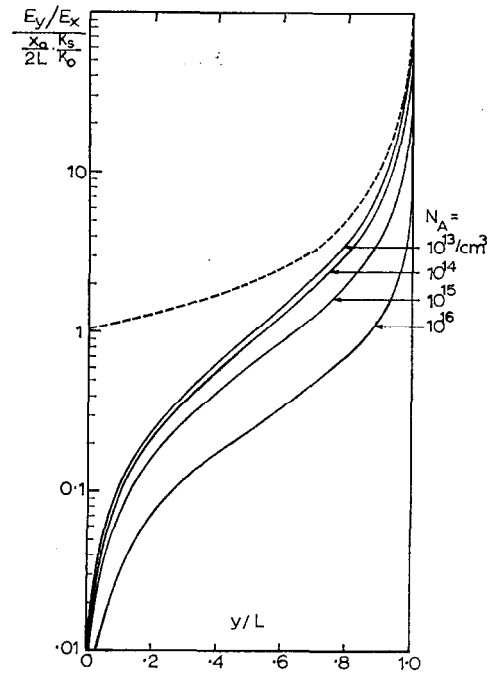


FIG. 11. The ratio of electric fields along the channel with the MOS transistor operating just in saturation for different impurity concentrations.
– – – – simple theory.[15]

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APPENDIX A

The Poisson equation for the channel may be written as:

$$\frac{d^2\psi}{dx^2} = -\rho$$

$$= -\frac{q}{K_s\epsilon_0}[p - n + N_D - N_A] \quad \text{(A-1)}$$

where

$$p = n_i\, e^{U_F - U} = n_i e^{U_F - U} \quad \text{(A-2)}$$

$$n = n_i e^{U - U_n} = e^{U - \xi - U_F} \quad \text{(A-3)}$$

$$N_A - N_D = n_i(e^{U_F} - e^{-U_F}) \quad \text{(A-4)}$$

The boundary conditions are:

$$\psi(x) \to 0 \quad \text{as} \quad x \to \infty \quad \text{(A-5)}$$

$$\frac{d\psi(x)}{dx} \to 0 \quad \text{as} \quad x \to \infty \quad \text{(A-6)}$$

In units of electrostatic potential

$$\frac{d^2U}{dx^2} = \frac{q^2}{kT}\frac{n_i}{K_s\epsilon_0} \times [e^{U - \xi - U_F} - e^{U_F - U} + e^{U_F} - e^{-U_F}]$$

$$= \frac{1}{L_D{}^2}[e^{-(\xi/2)} \sinh(U - (\xi/2) - U_F) + \sinh U_F] \quad \text{(A-7)}$$

Take the integration with respect to U and set limits from zero to any arbitrary value

$$\int_0^{(dU/dx)} \left(\frac{dU}{dx}\right) d\left(\frac{dU}{dx}\right) = \frac{1}{2L_D{}^2}\int_0^U [e^{U - \xi - U_F} - e^{U_F - U} + e^{U_F} - e^{-U_F}]\, dU$$

$$\left(\frac{dU}{dx}\right)^2 = \frac{1}{L_D{}^2}[e^{U - \xi - U_F} + e^{U_F - U} + (U-1)e^{U_F} - (U + e^{-\xi})e^{-U_F}] \quad \text{(A-8)}$$

$$\therefore \left(\frac{dU}{dx}\right) = \frac{1}{L_D} \cdot \frac{U}{|U|} F(U, \xi, U_F) \quad \text{(A-9)}$$

where

$$F(U, \xi, U_F) = \sqrt{[e^{U - \xi - U_F} + e^{U_F - U} + (U-1)e^{U_F} - (U + e^{-\xi})e^{-U_F}]} \quad \text{(A-10)}$$

At the surface, $x = 0$, $U = U_s$, the electric field is

$$E_s = \left(\frac{kT}{q}\right)\left(\frac{dU}{dx}\right)_{x=0} = \frac{U_s}{|U_s|}\left(\frac{kT}{q}\right)\frac{F(U_s, \xi, U_F)}{L_D} \quad \text{(A-11)}$$

To select the physically meaningful sign for the square-root, the factor $U_s/|U_s|$ is added.