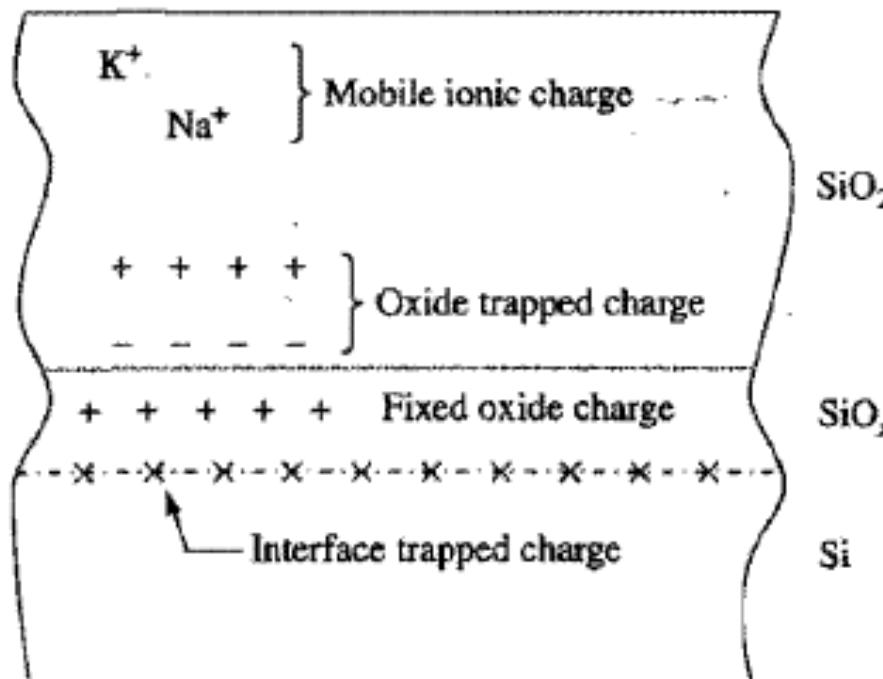
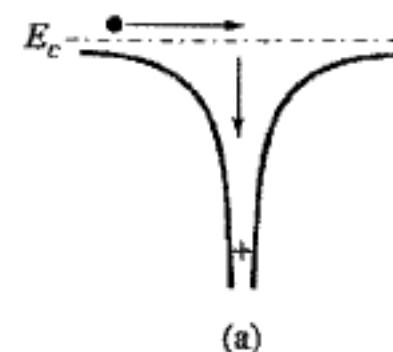


Oxide and Interface Traps / Charges

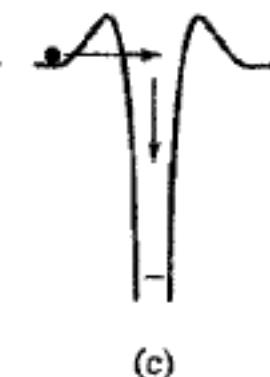
Different sources of oxide charges (mobile ions, traps)



Coulomb
attractive

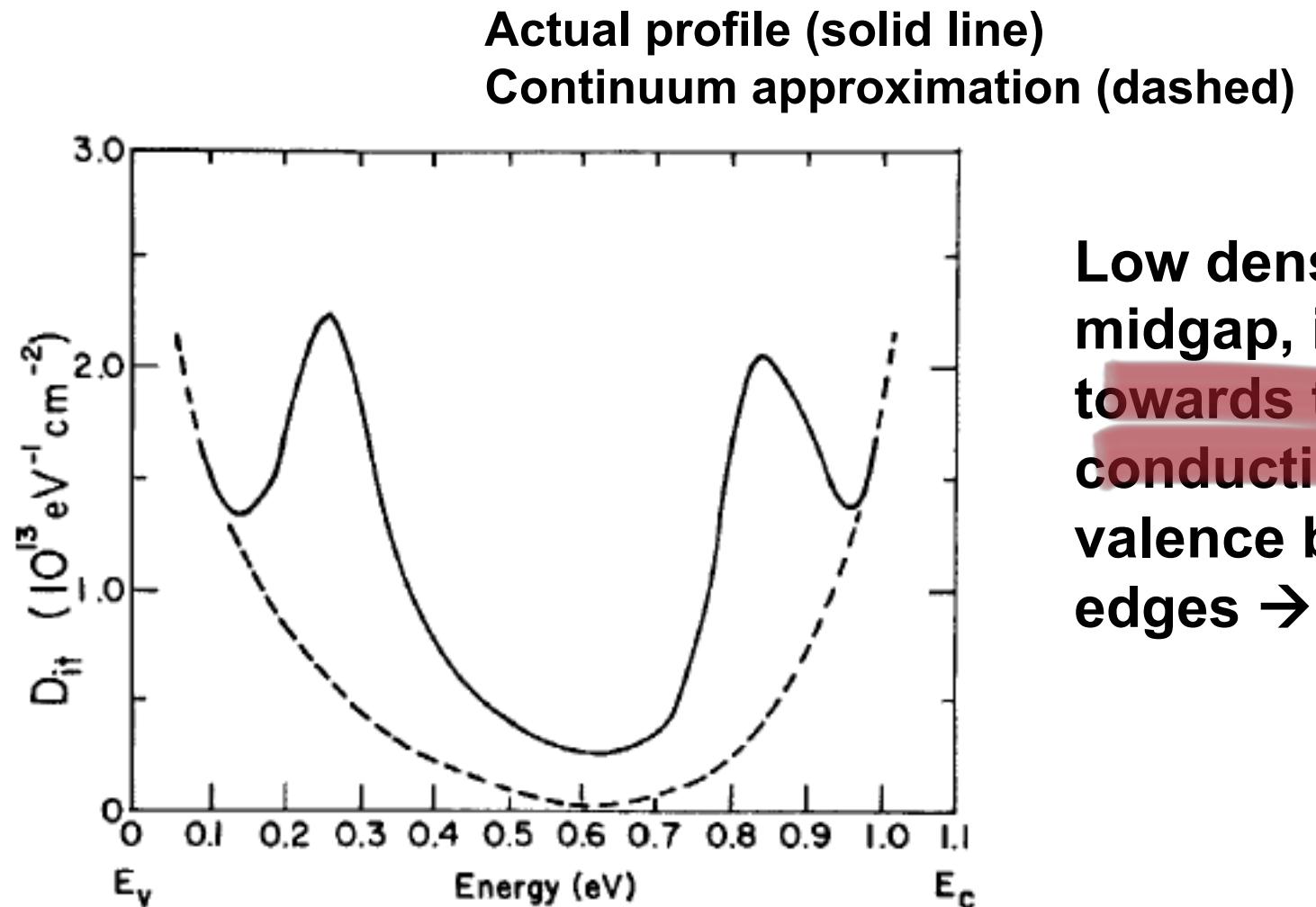


Coulomb
repulsive



Coulomb
neutral

Si/SiO₂ Interface Trap Distribution

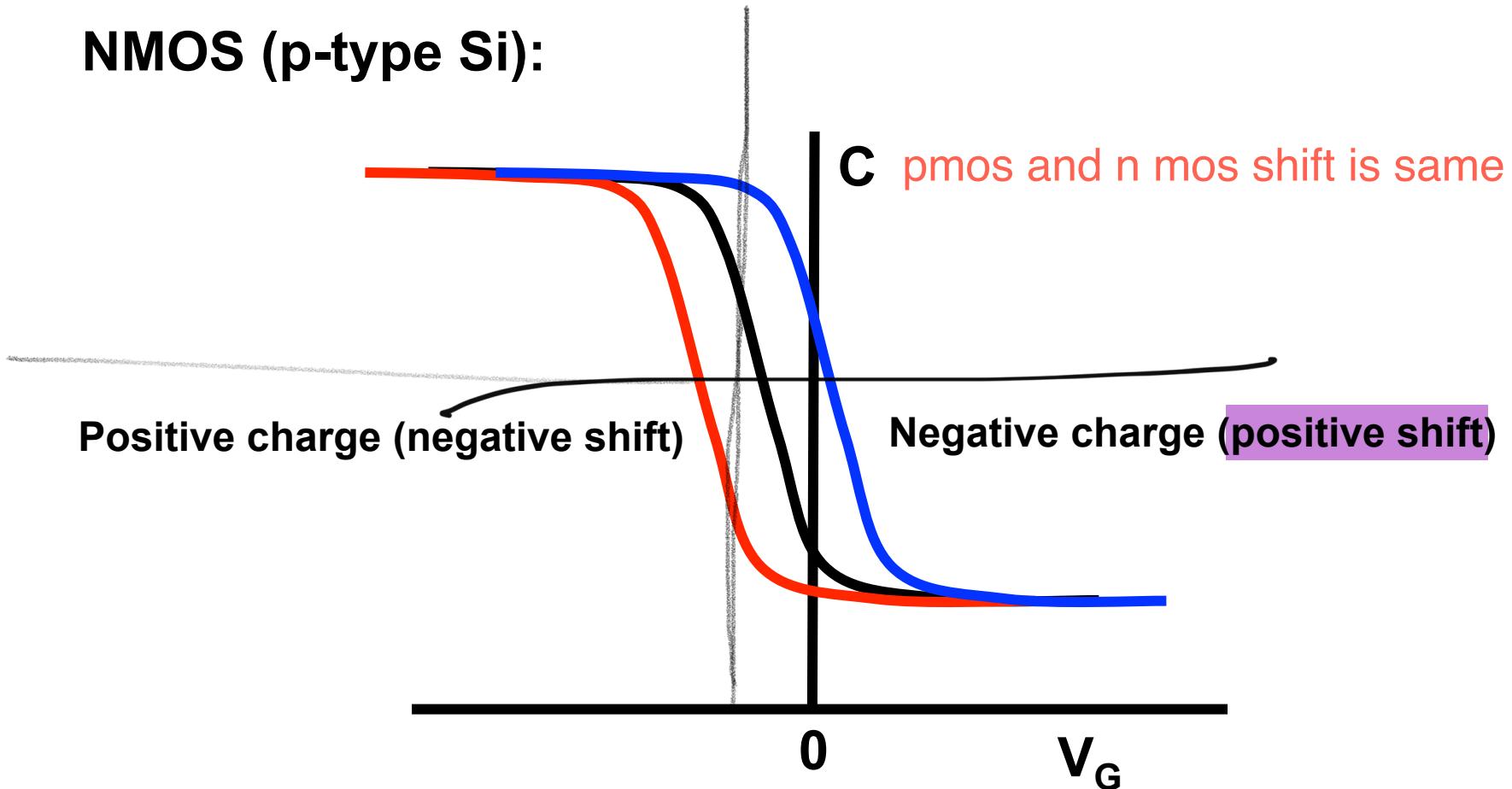


Low density in midgap, increases towards the conduction and valence band edges → U profile

Poindexter, JAP 1984

Impact of Fixed Charges on C-V curve (HFCV)

NMOS (p-type Si):

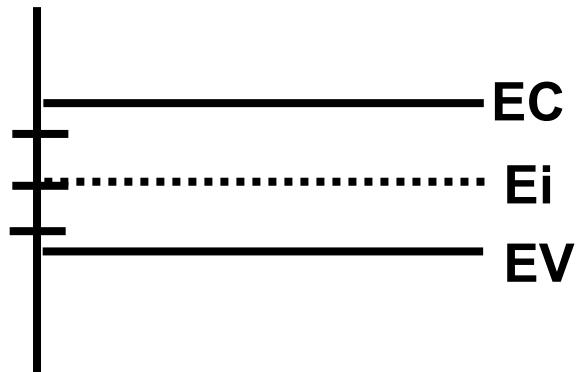


Parallel shift in C-V curve due to oxide charges

Properties of Interface Traps

Upper half (EC to Ei) → Acceptor like traps

Negatively charged (filled with electron), Zero charge (empty)



**Traps below Fermi level
are filled with electrons**

Text

**Traps above Fermi
level are empty**

Lower half (Ei to EV) → Donor like traps

Zero charge (filled with electron), Positively charged (empty)

Calculation of Interface Trap Charges (NMOS)

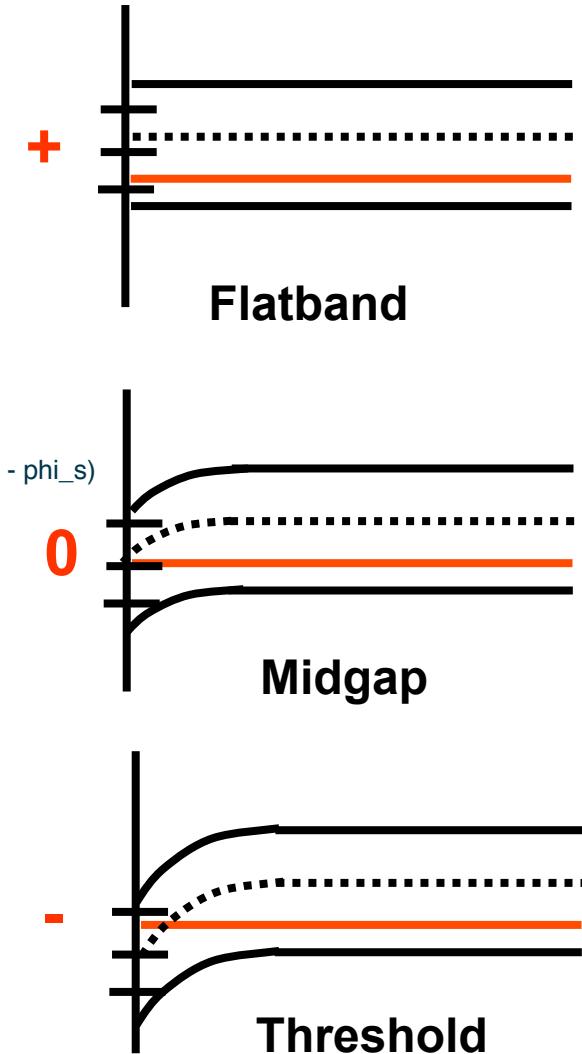
Interface trap density $\rightarrow D_{IT}$ (no. of traps / eV of band gap / cm² of capacitor area)

Flatband: $Q_{IT} = q \cdot \langle D_{IT} \rangle \cdot \phi_F$

Midgap: $Q_{IT} = 0$

Threshold: $Q_{IT} = -q \cdot \langle D_{IT} \rangle \cdot \phi_F$

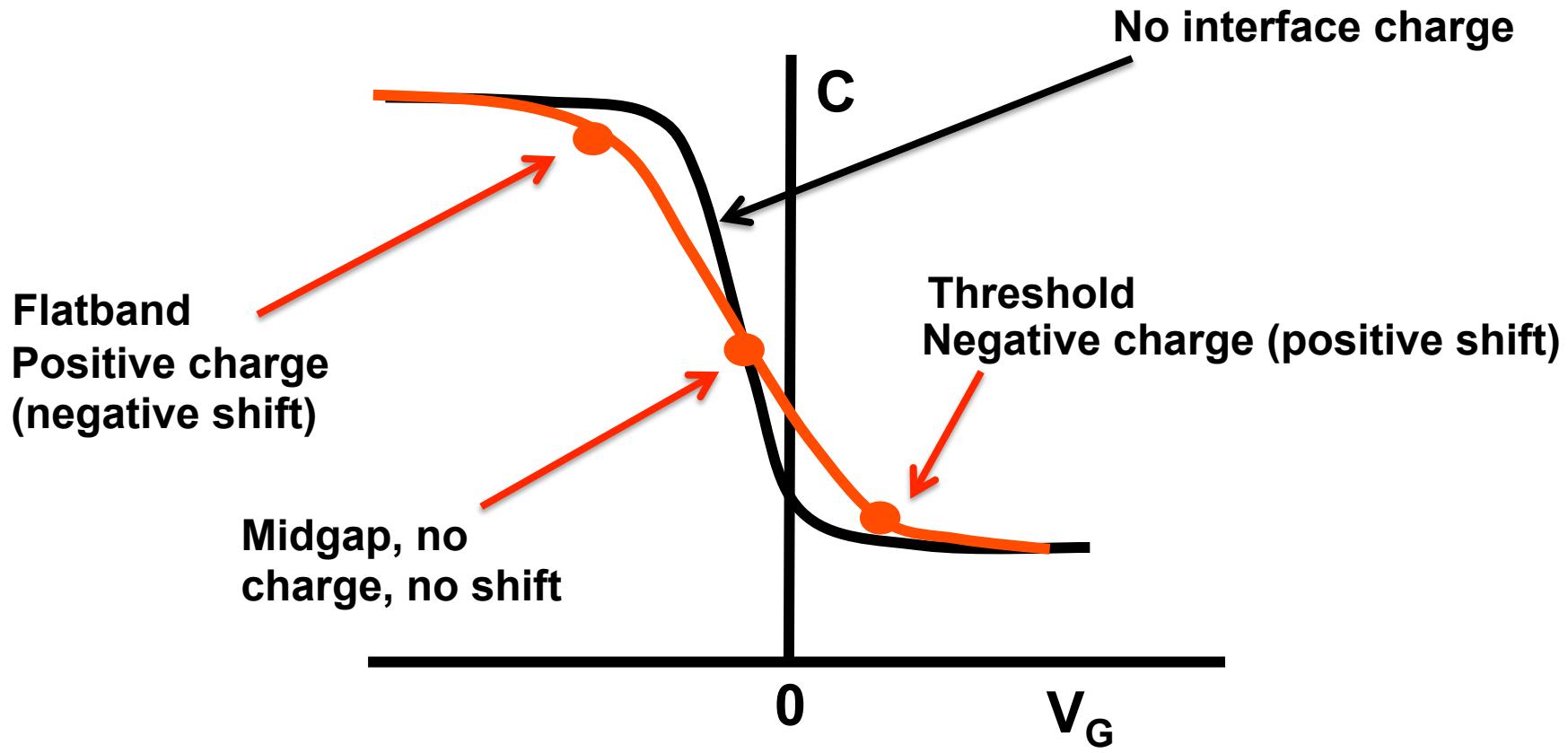
for any condition $q_{IT} = +q \langle D_{IT} \rangle (\phi_F - \phi_s)$



Magnitude and sign of interface trap charges change with band bending

Impact of D_{IT} on C-V curve (NMOS, HFCV)

Interface charge



Skew in C-V curve due to interface trap charges

Determination of Oxide / Interface Charges

Calculate reference CV, determine C_{MG} and V_{MG}

Check difference of real and reference V_{MG} ,
calculate Q_{ox}

$$Q_{ox} = \frac{1}{T_{ox}} \int_0^{T_{ox}} x \cdot \rho(x) dx = C_{ox} \cdot \Delta V_{MG}$$

Charge density in oxide at location x
 $\rho(x)$ is mostly taken cont and is given

Check difference of real and reference V_{FB} ,
calculate $Q_{ox} + Q_{IT}$ (hence D_{IT})

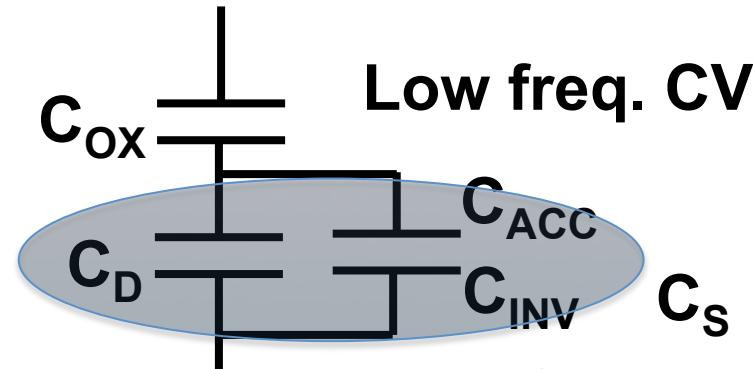
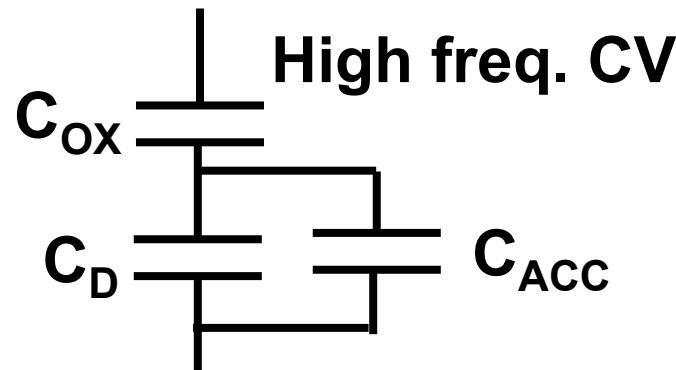
$$Q_{ox} + q \cdot \langle D_{IT} \rangle \cdot \phi_F = C_{ox} \cdot \Delta V_{FB}$$

impact of thinner oxide is less when interface charge as
 $\Delta V_{FB} = Q/C_{ox}$

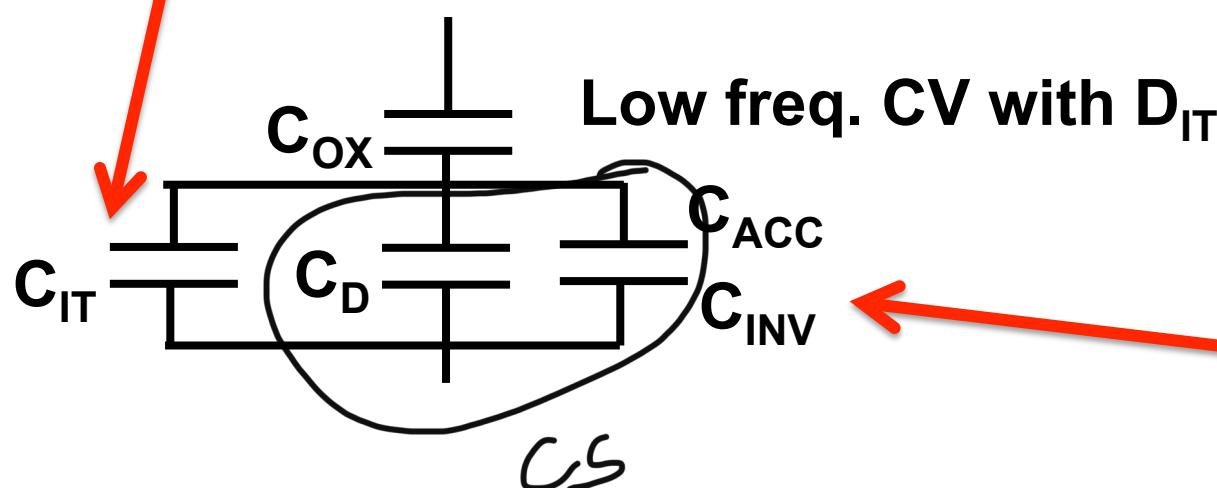
Q_{ox} is the oxide trapped charge

Can repeat for different V_G values to get D_{IT} distribution in the bandgap (need to link V_G to band bending)

Capacitance in MOS System

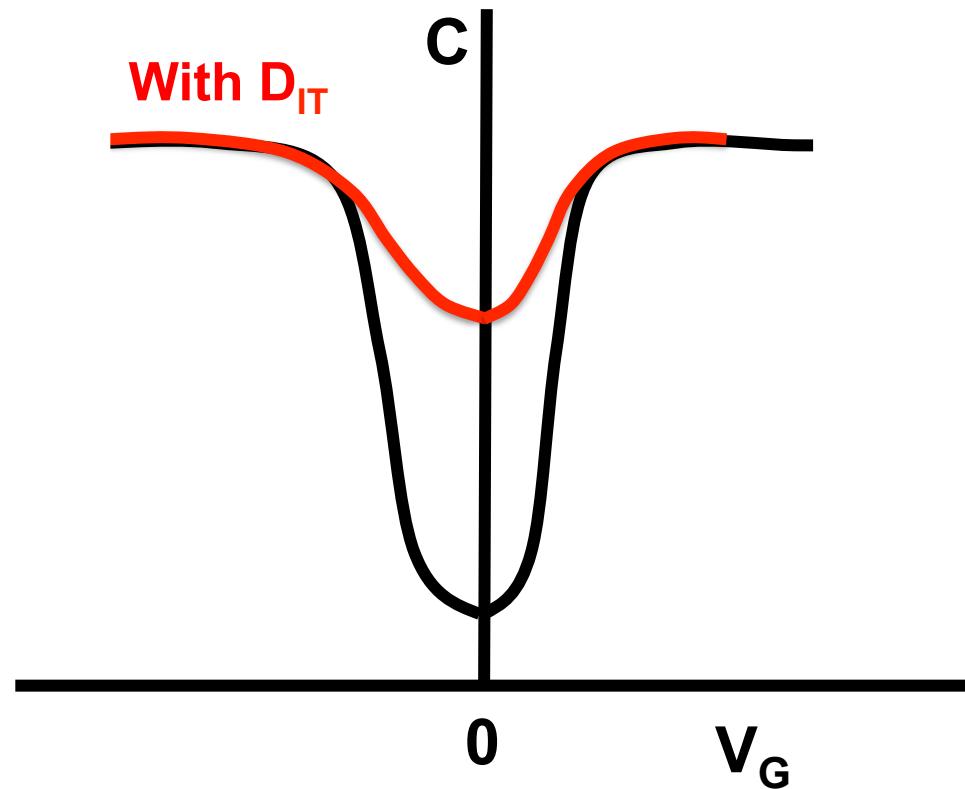


Interface traps respond at lower freq.



Added only in
inversion

Impact of D_{IT} on C-V curve (NMOS, LFCV)



Stretching due to DC charge (same as HFCV)

Higher capacitance due to contribution from interface traps
AC response

Close to accumulation and inversion,
substrate capacitance dominates

Determination of Interface Charges

HFCV:

$$\frac{1}{C_{HF}} = \frac{1}{C_{OX}} + \frac{1}{C_S}$$

Evaluate in depletion, not valid for V_G closer to accumulation or inversion

$$C_S = \left[\frac{1}{C_{HF}} - \frac{1}{C_{OX}} \right]^{-1}$$

LFCV:

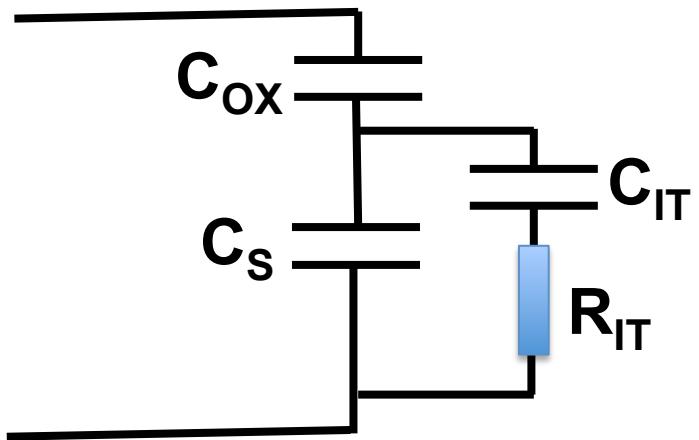
$$\frac{1}{C_{LF}} = \frac{1}{C_{OX}} + \frac{1}{C_S + C_{IT}}; \text{ where } C_{IT} = q. \langle D_{IT} \rangle$$

D_{IT}:

$$C_{IT} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{OX}} \right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{OX}} \right]^{-1}$$

Can repeat for different V_G values to get D_{IT} distribution in the bandgap (need to link V_G to band bending)

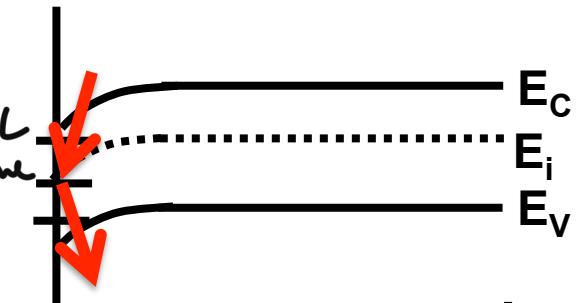
MOS Conductance and Capacitance



Capture-emission of electrons (CB to VB) via interface traps is a loss process → Conductance

Trap time constant: τ_{IT}

$$\tau_{IT} = C_{IT} \cdot R_{IT}$$



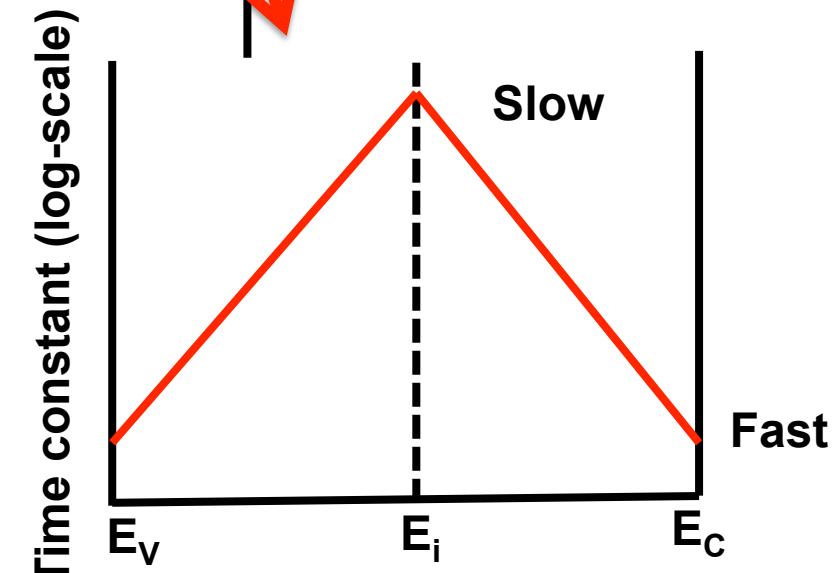
Capture c.s

Thermal velocity

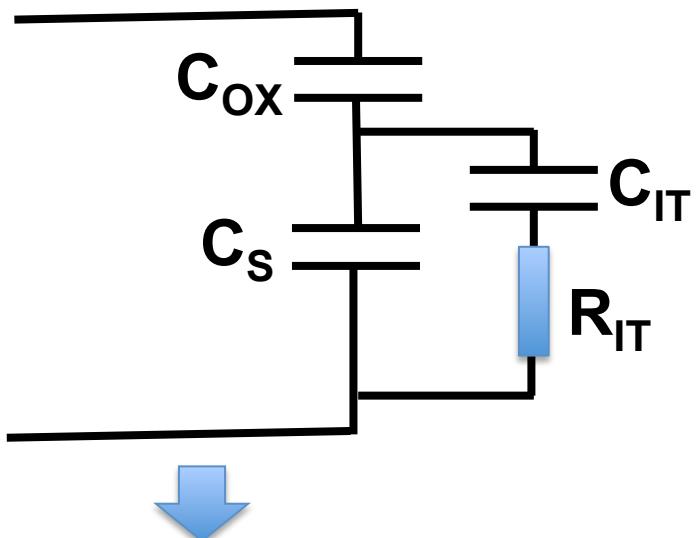
$$\tau_{IT} = \frac{1}{\sigma_{n,p} n_i v_{th}} e^{-(|E - E_i|)/kT}$$

*Proof nahi
dya*

Intrinsic carrier density

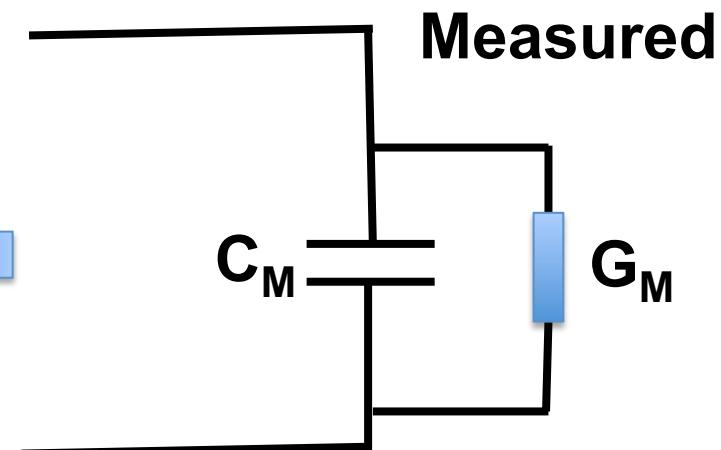
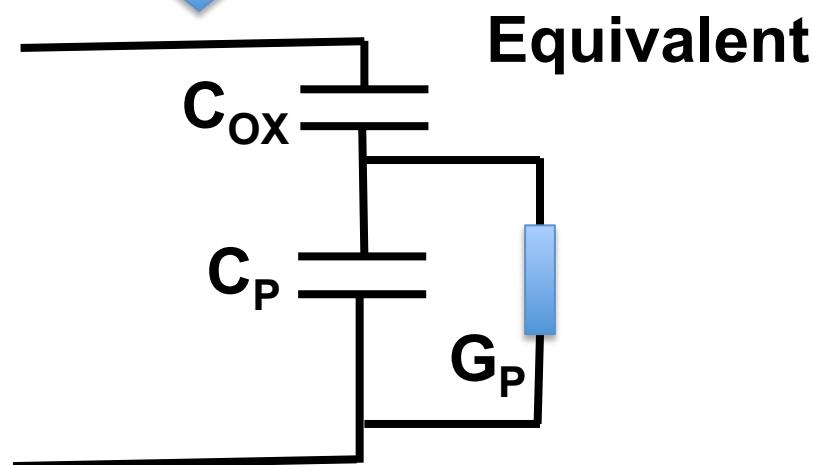


MOS Conductance and Capacitance

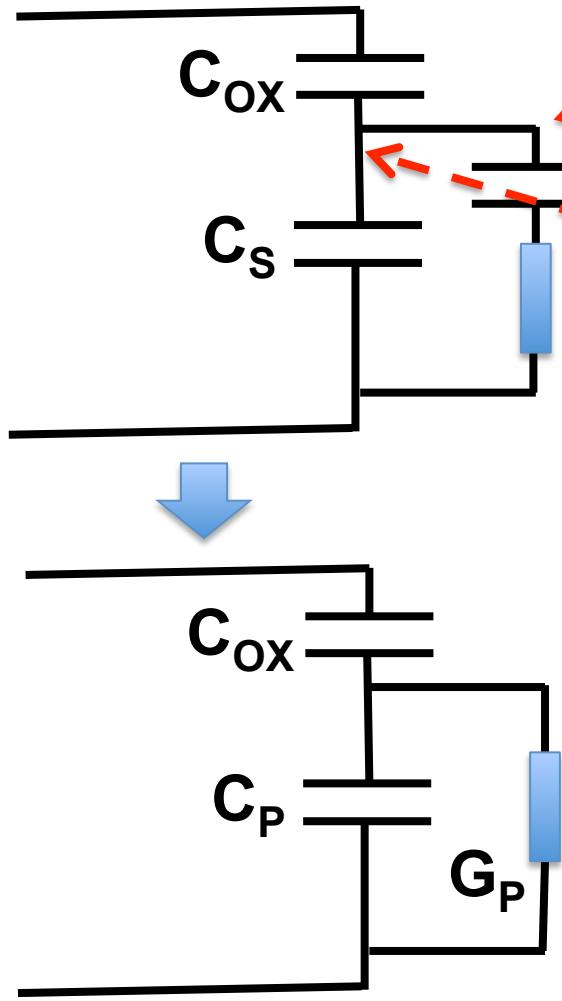


Convert actual network to equivalent network

Impedance measurement in parallel mode



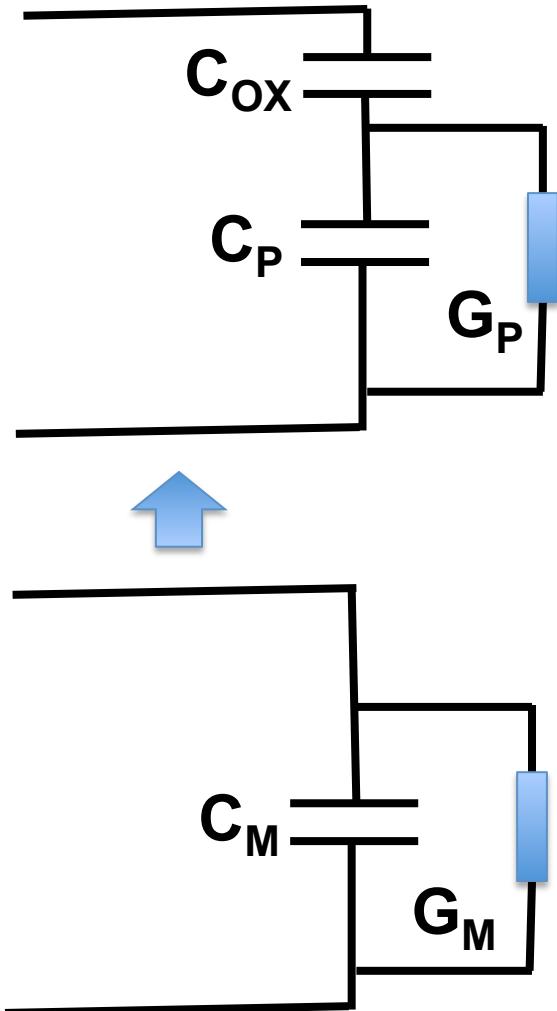
MOS Conductance and Capacitance



$$\begin{aligned}
 Z_{IT} &= R_{IT} + \frac{1}{j\omega C_{IT}} = \frac{1 + j\omega\tau_{IT}}{j\omega C_{IT}} \\
 Y_S &= j\omega C_S + \frac{j\omega C_{IT}}{1 + j\omega\tau_{IT}} \\
 &= \frac{\omega^2 C_{IT} \tau_{IT}}{1 + (\omega\tau_{IT})^2} + j\omega \left[C_S + \frac{C_{IT}}{1 + (\omega\tau_{IT})^2} \right] \\
 &= G_P + j\omega C_P
 \end{aligned}$$

$$\frac{G_P}{\omega} = \frac{qD_{IT}\omega\tau_{IT}}{1 + (\omega\tau_{IT})^2} \text{ and } C_P = C_S + \frac{C_{IT}}{1 + (\omega\tau_{IT})^2}$$

MOS Conductance and Capacitance



$$\frac{1}{j\omega C_{ox}} + \frac{1}{G_P + j\omega C_P} = \frac{1}{G_M + j\omega C_M}$$
$$G_P + j\omega C_P = \left[\frac{1}{G_M + j\omega C_M} - \frac{1}{j\omega C_{ox}} \right]^{-1}$$
$$\frac{G_P}{\omega} = \frac{\omega G_M C_{ox}^2}{G_M^2 + \omega^2 (C_{ox} - C_M)^2}$$

Fix $V_G \rightarrow$ Measure C_M and G_M as freq. is varied \rightarrow Set another V_G and repeat

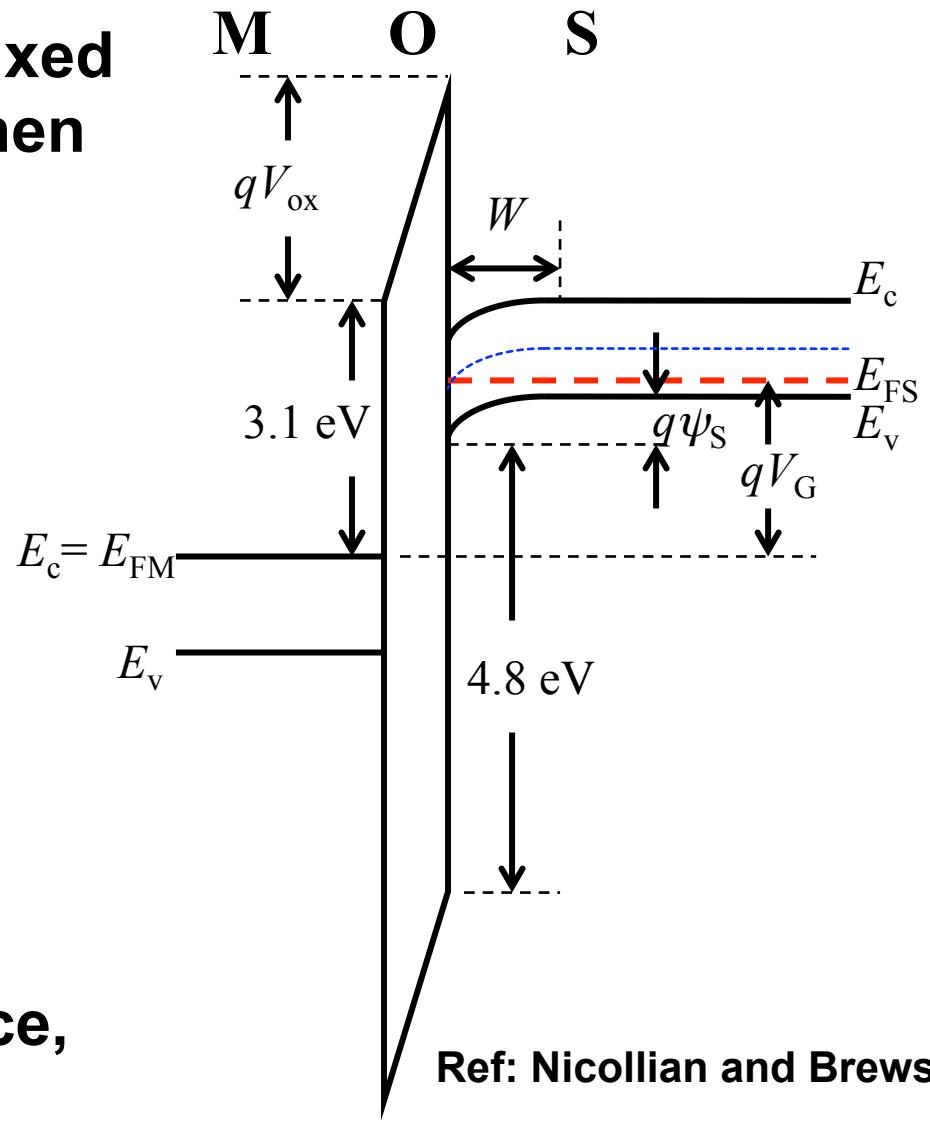
MOS Conductance Measurement

Band bending is fixed for a fixed $V_G \rightarrow$ Conductance peaks when freq. matches with trap time constant: $\omega\tau_{IT} = 1$

$$\frac{G_P}{\omega} = \frac{qD_{IT}\omega\tau_{IT}}{1 + (\omega\tau_{IT})^2} \Rightarrow D_{IT} = \frac{2G_P}{q\omega}$$

Repeat at different V_G (band bending) to get trap profile

Need modifications for non uniform traps, spatial non-uniformities, series resistance, gate leakage etc.



MOS Conductance Measurement

Band bending is fixed for a fixed $V_G \rightarrow$ Conductance peaks when freq. matches with trap time constant: $\omega\tau_{IT} = 1$

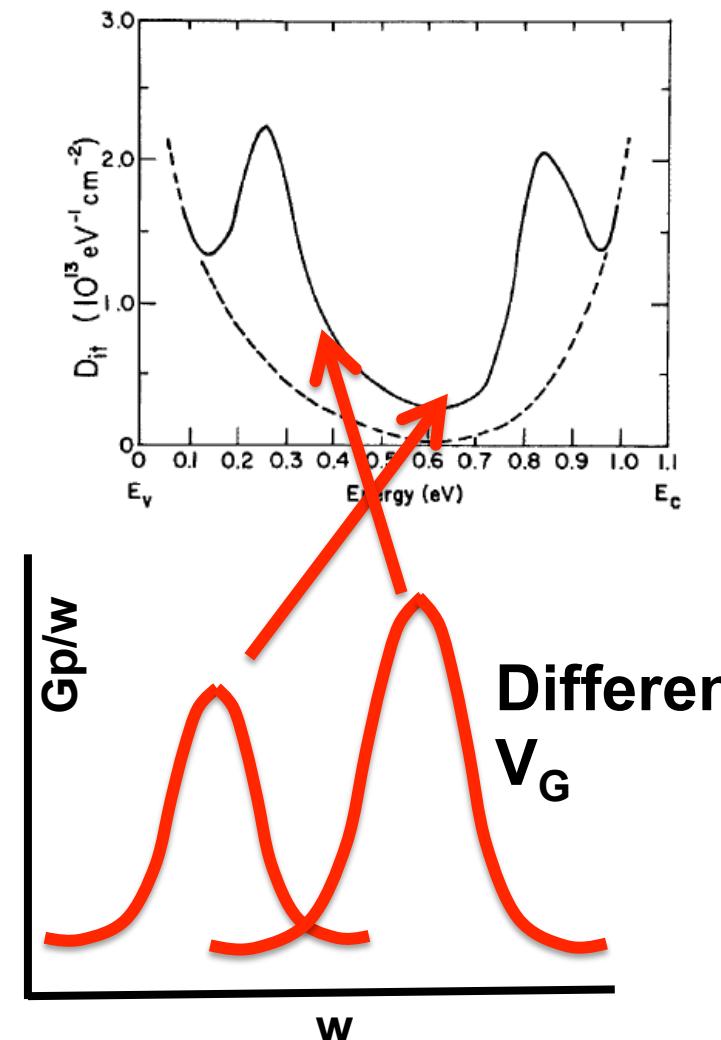
$$\frac{G_P}{\omega} = \frac{qD_{IT}\omega\tau_{IT}}{1 + (\omega\tau_{IT})^2} \Rightarrow D_{IT} = \frac{2G_P}{q\omega}$$

Peak magnitude \rightarrow Trap density

Frequency of peak \rightarrow Capture c.s

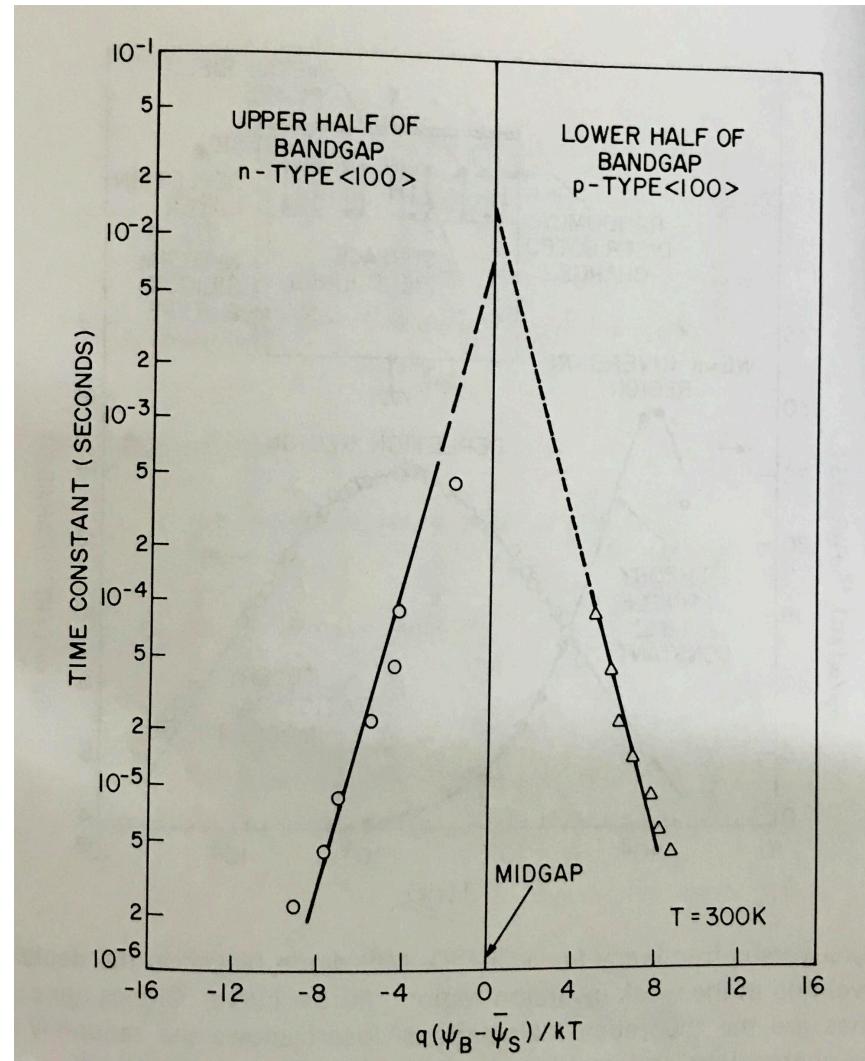
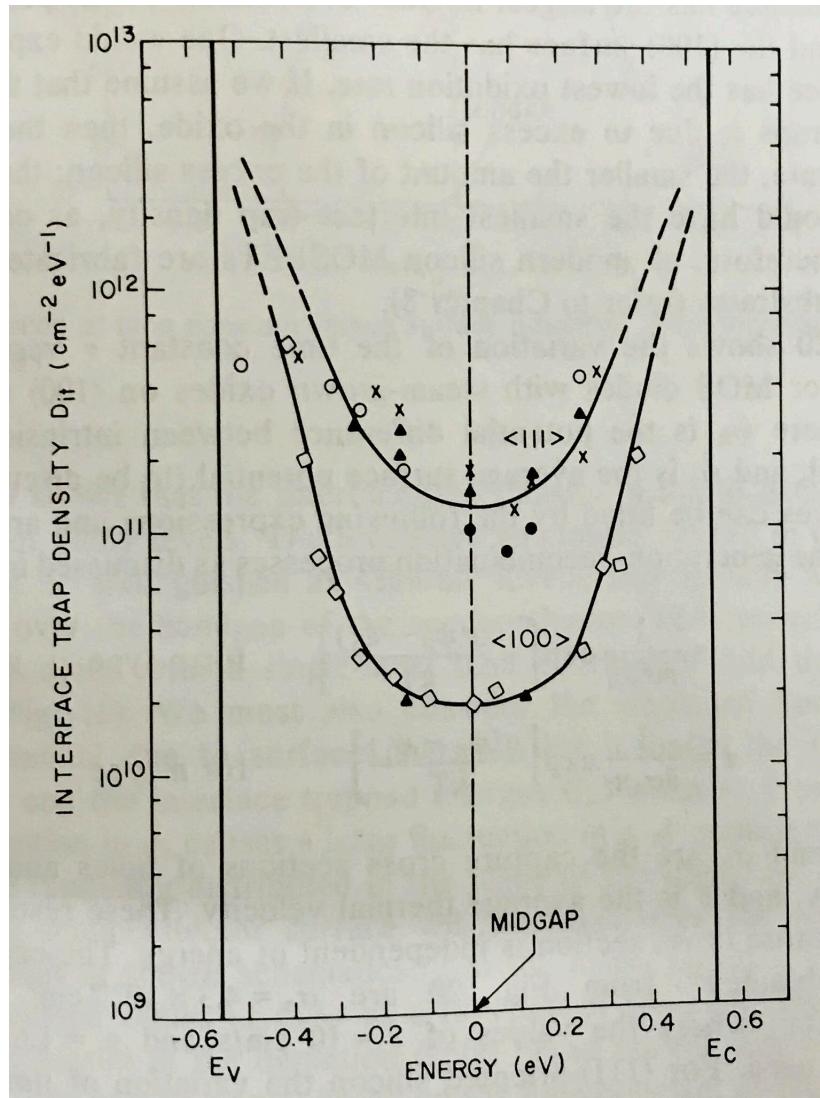
$$\frac{2G_P}{\omega} = qD_{IT}$$

Higher G_P will correspond to higher D_{IT}

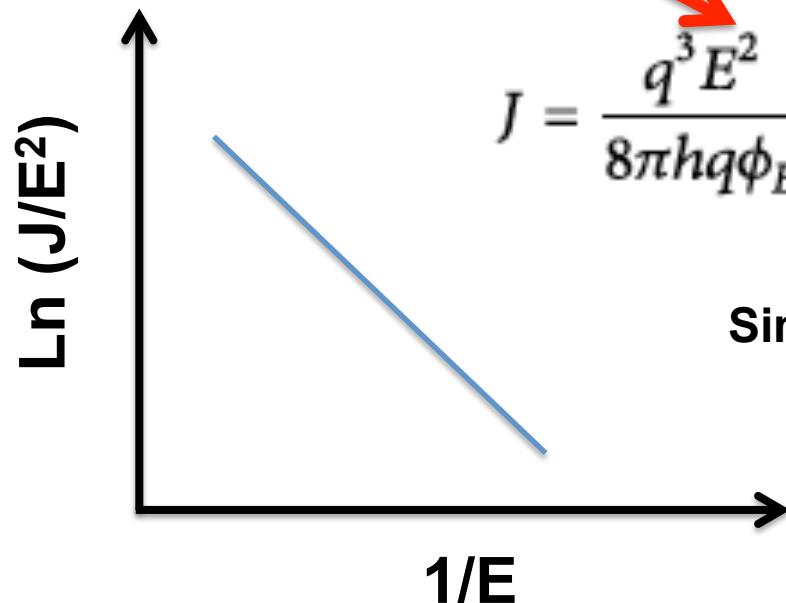
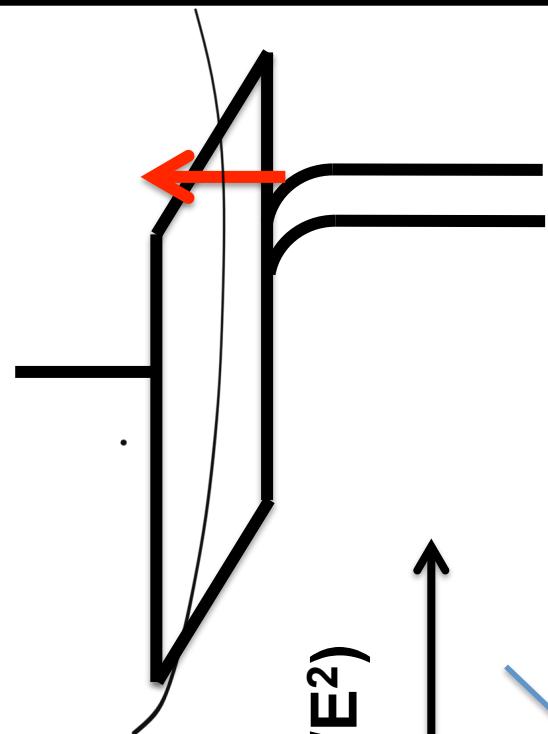


Ref: Nicollian and Brews

Trap Density and Capture Cross Section



Gate Leakage: Fowler Nordheim Tunneling



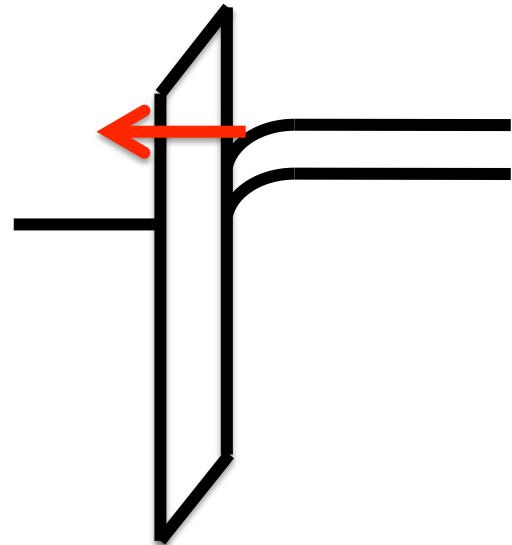
For relatively thicker gate insulator and high electric field

Tunneling via triangular barrier

$$J = \frac{q^3 E^2}{8\pi h q \phi_B} \exp \left[\frac{-8\pi(2qm_T^*)^{1/2}}{3hE} \phi_B^{3/2} \right]$$

Simplified analytical expression

Gate Leakage: Direct Tunneling



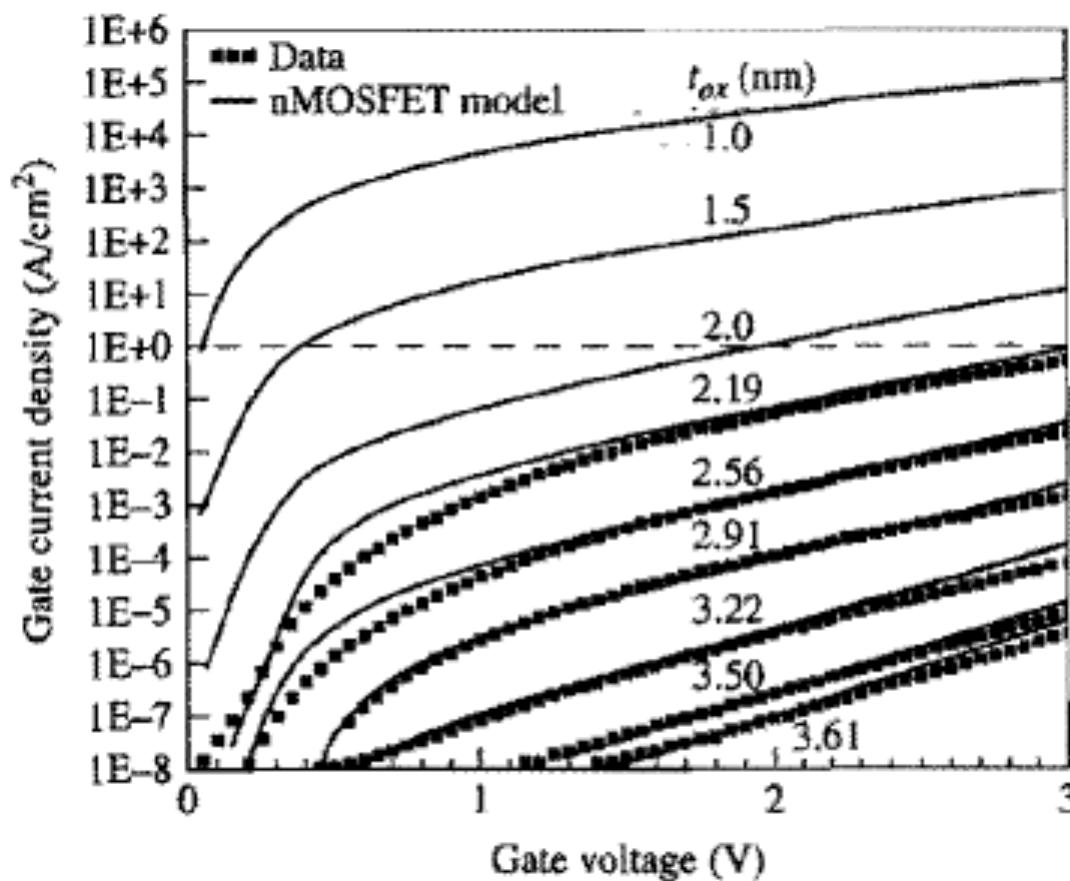
Tunneling via rectangular potential barrier

**Thinner dielectric, lower electric field
(relative to FN) → For SiO_2 become
relevant for $T_{\text{ox}} < 3\text{nm}$**

**Need numerical solution, not easy to
derive closed form**

Gate Leakage: Direct Tunneling

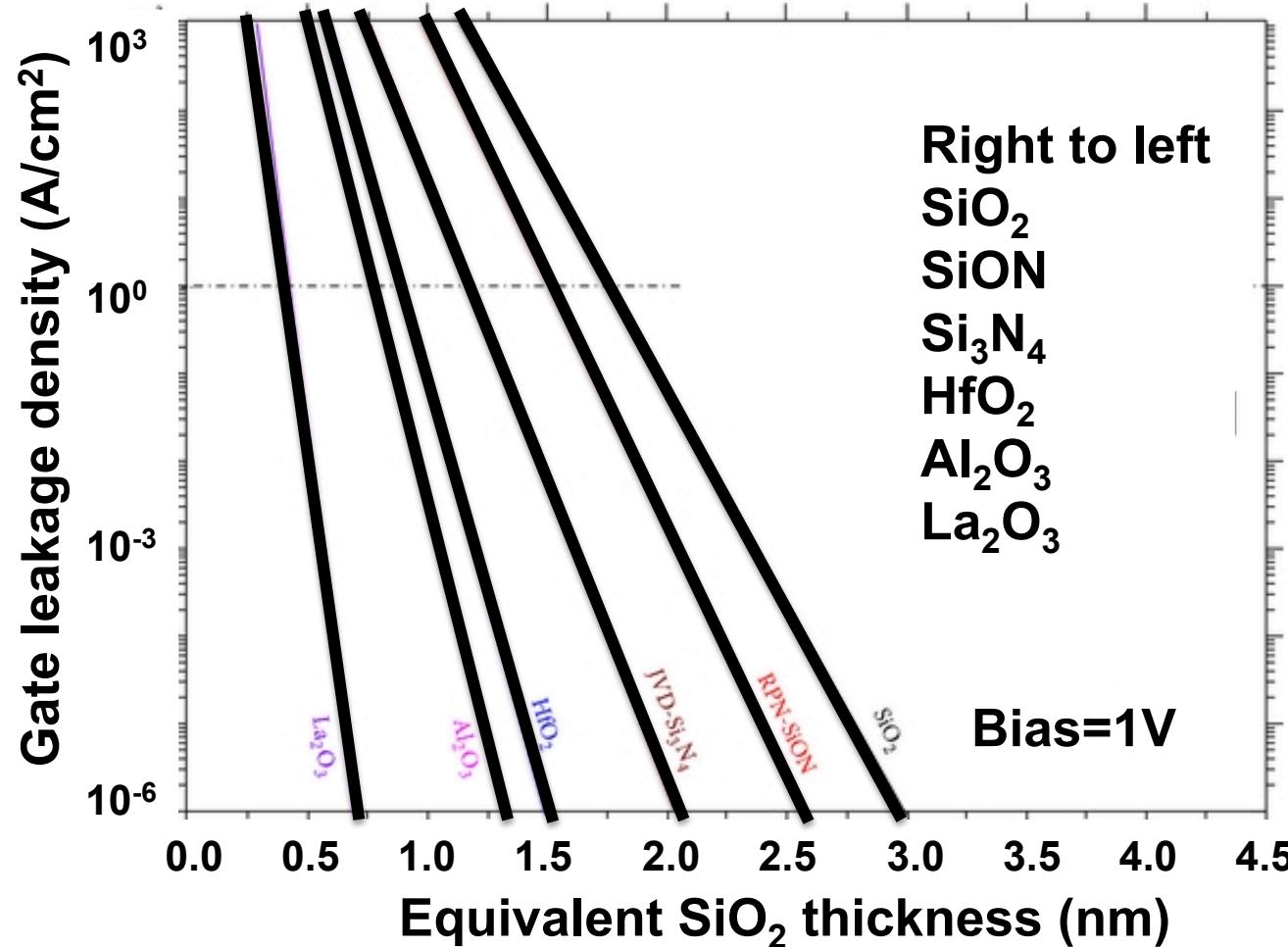
Direct tunneling current vs. voltage characteristics for different gate insulator thickness



Ref: Taur and Ning

Gate Leakage: Direct Tunneling

Direct tunneling current for different gate insulator



Increase in
gate leakage

SiO_2 : 10X/2Å

HfO_2 : 10X/1Å

Ref: Taur and Ning