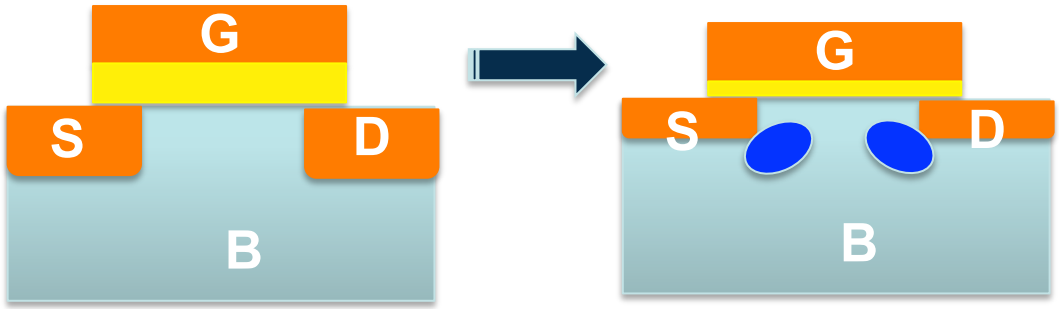
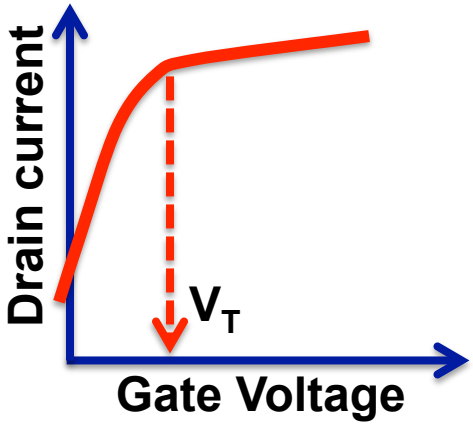
Limitations of Traditional Scaling

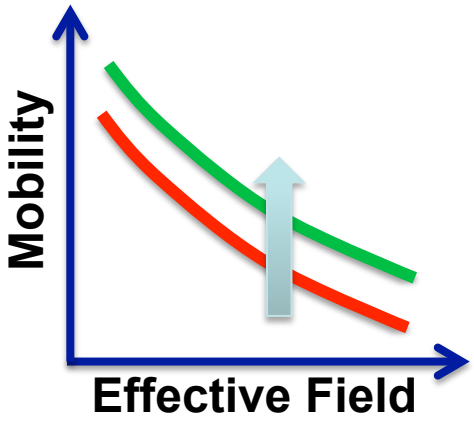




Sub V_T leakage do not scale: Difficult to reduce V_T with scaling L

Supply V_{DD} does not scale to maintain overdrive ($V_G - V_T$)

Increase in lateral field (~V_D/L), vertical field (~V_G/L), reduction in mobility (μ) – ON current suffers

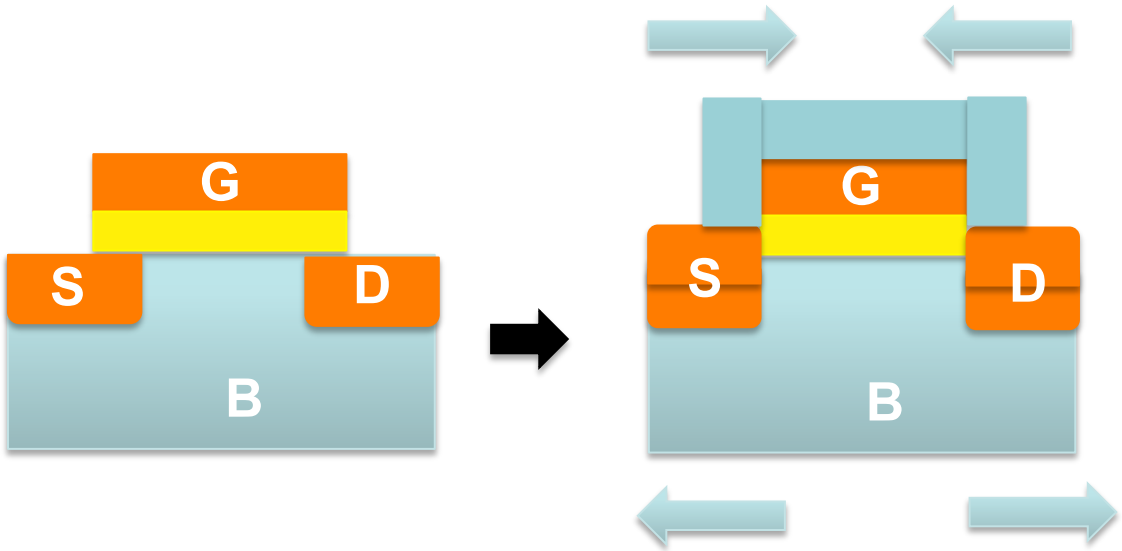


Use strain to boost mobility

Drain Current – Impact of Stress

Scaling → increase in E field→ reduction in mobility → reduction in I_D

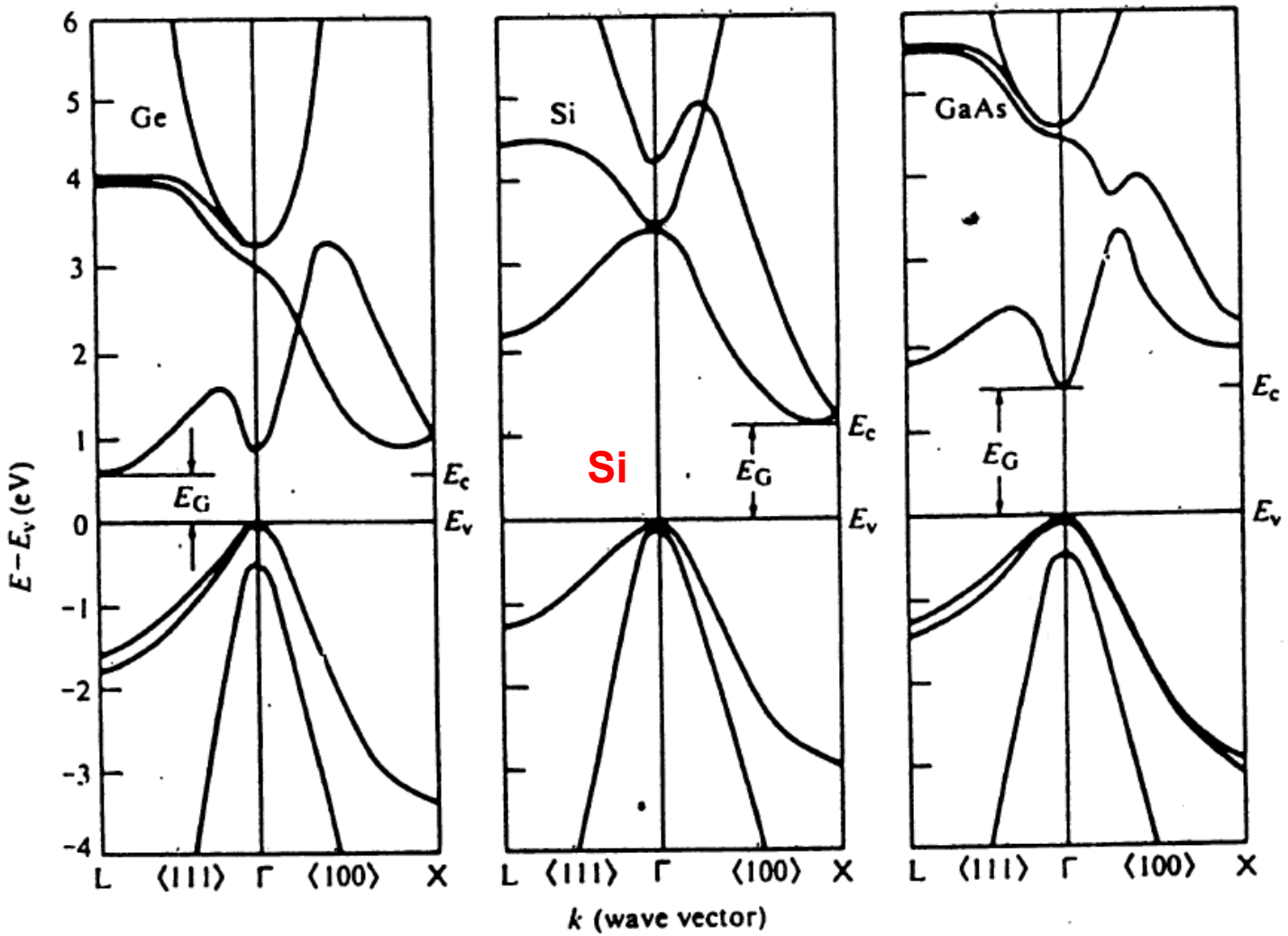
Stress → increase in mobility → increase in I_D



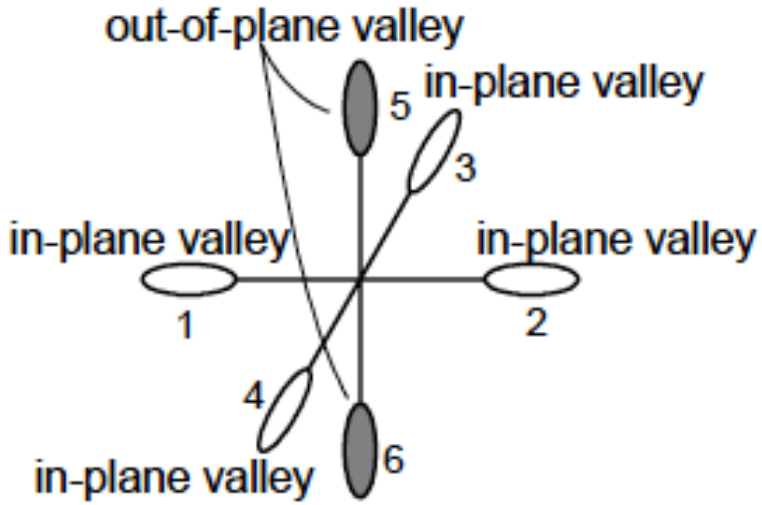
PMOS:
Compressive Liner
SiGe S/D

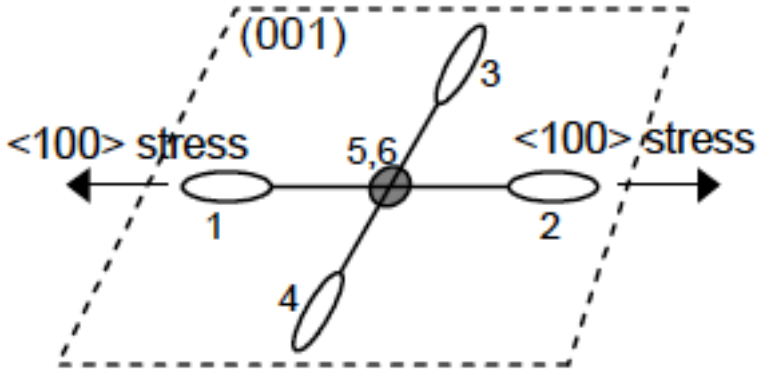
NMOS:
Tensile Liner
SiC S/D

Recap – Energy Bands (E-K plots)



Physics of Strain (NMOS)





Electrons in conduction band: 4 in plane and 2 out of plane valleys

Projection of out of plane valleys

Mobility depends on valley occupancy

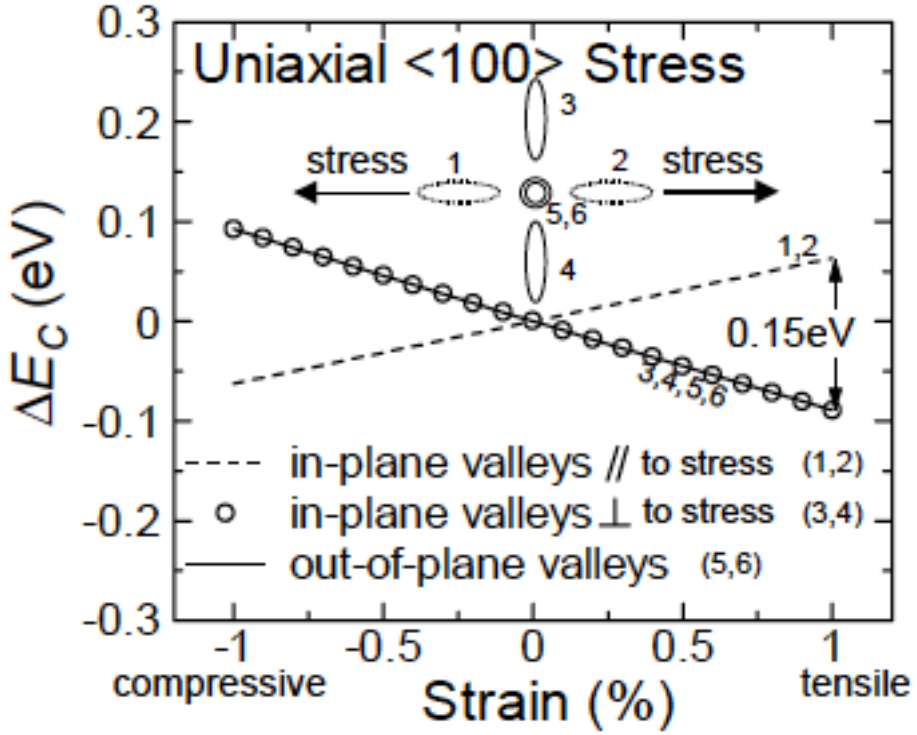
$$\mu = \frac{q < \tau > \left(\frac{n_{1,2}}{m_L} + \frac{n_{3,4}}{m_T} + \frac{n_{5,6}}{m_T}\right)}{\left(n_{1,2} + n_{3,4} + n_{5,6}\right)}$$

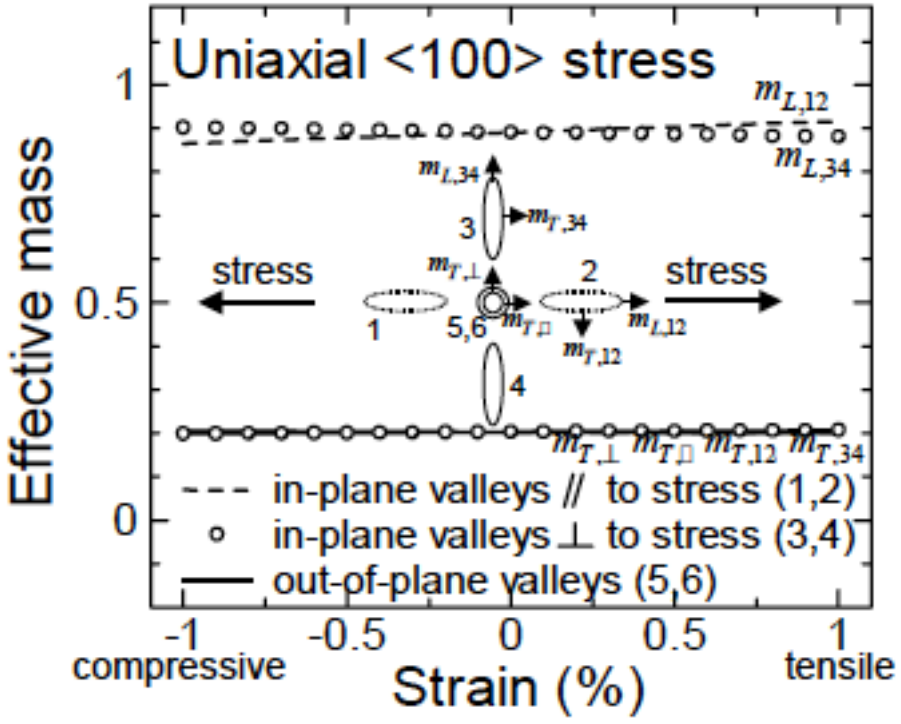
Uchida, IEDM'05

Physics of Strain (NMOS)

Strain → Splitting of energy levels → change in population

Higher m_L for in-plane; lower m_T for out of plane → Lower overall m* due to population of out of plane valleys

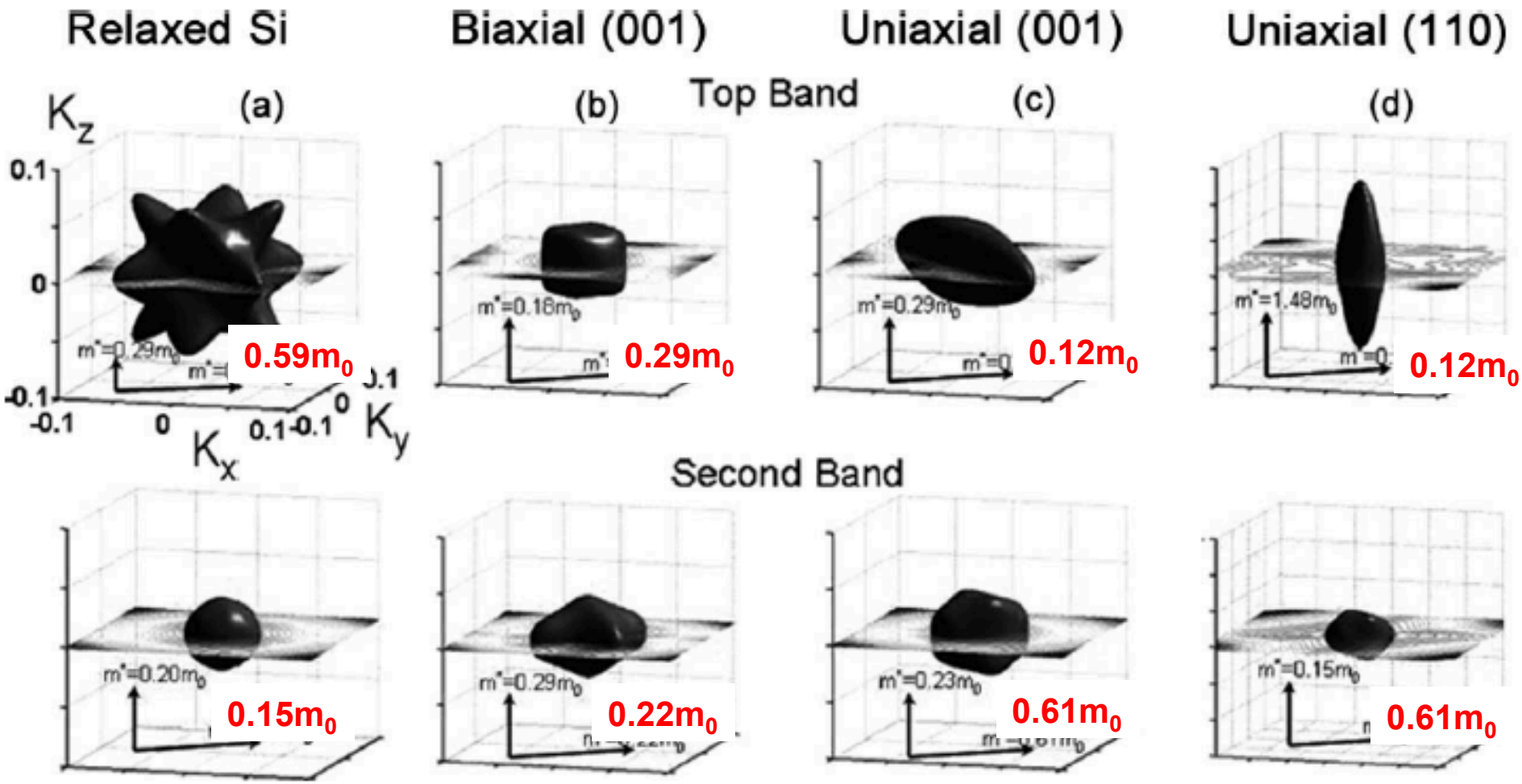




Uchida, IEDM'05

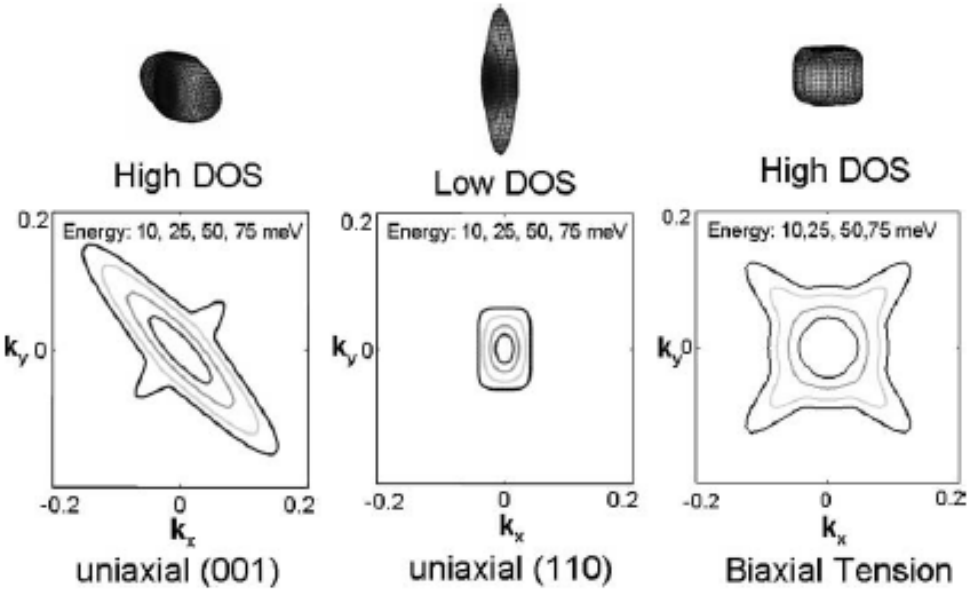
Physics of Strain (PMOS)

Strain → Lowering of transport effective mass (top band)



Thomson, TED'06

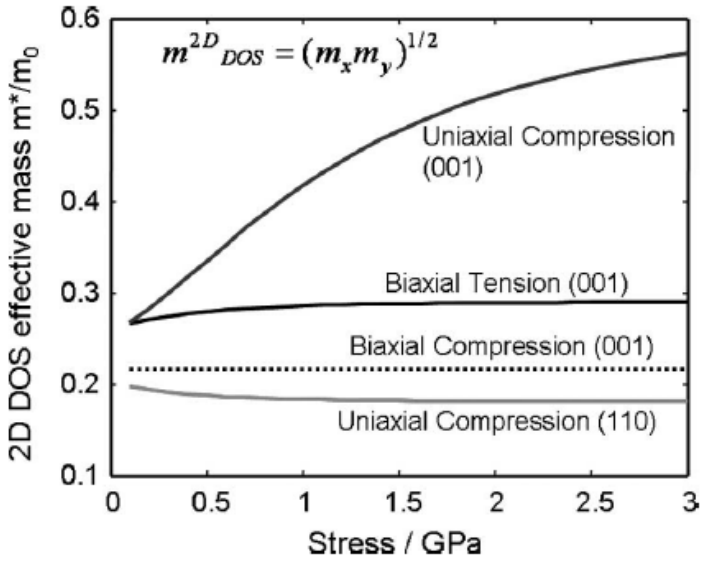
Physics of Strain (PMOS)

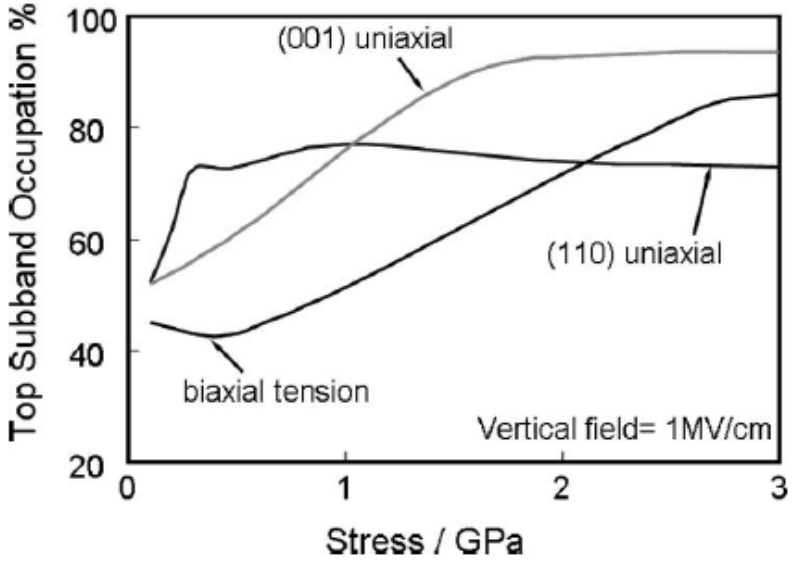


Strain → Increase in DOS effective mass

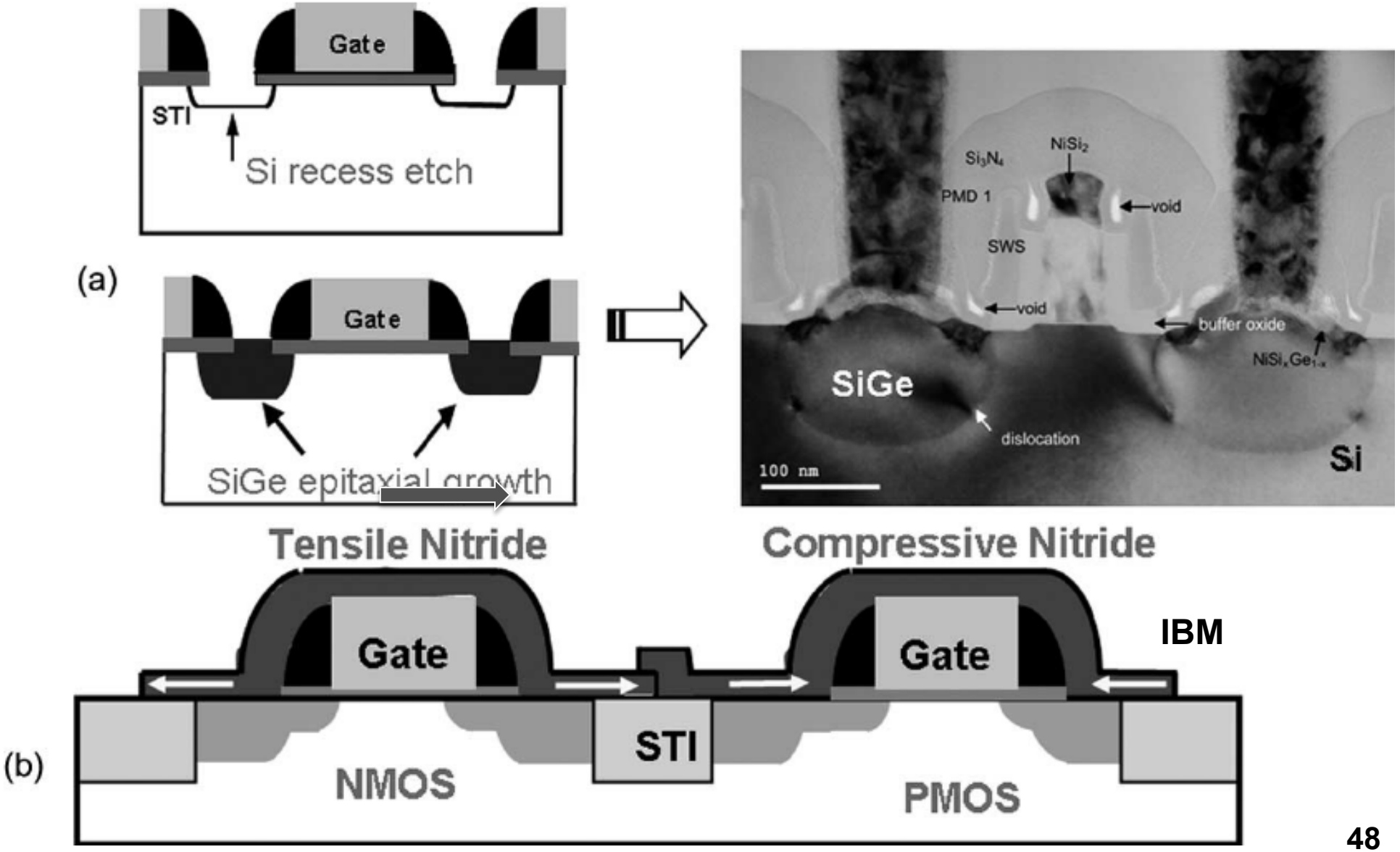
Increased occupancy of top band

Thomson, TED'06

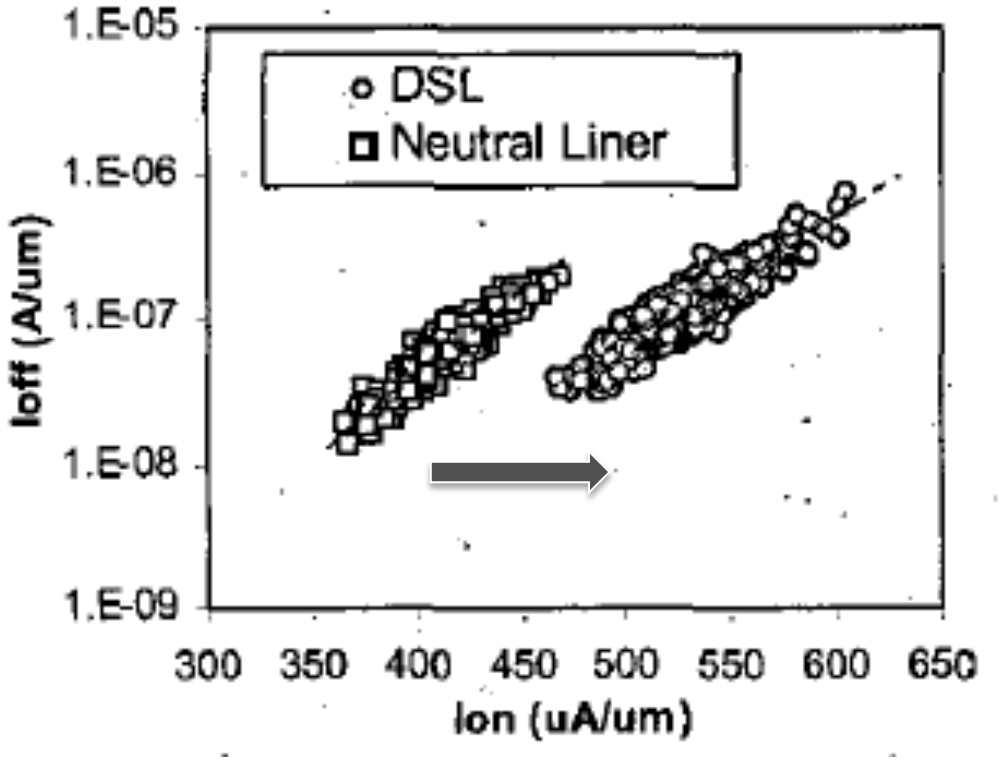




Stressor Technology

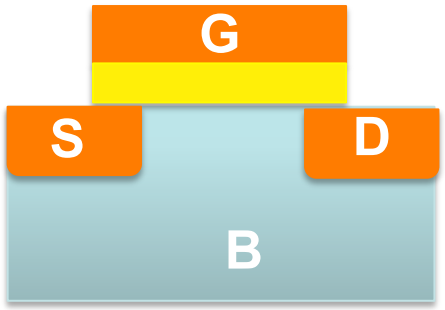


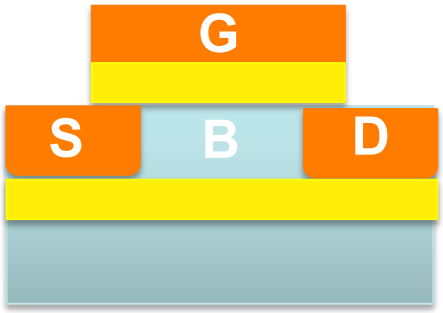
Stressor Technology

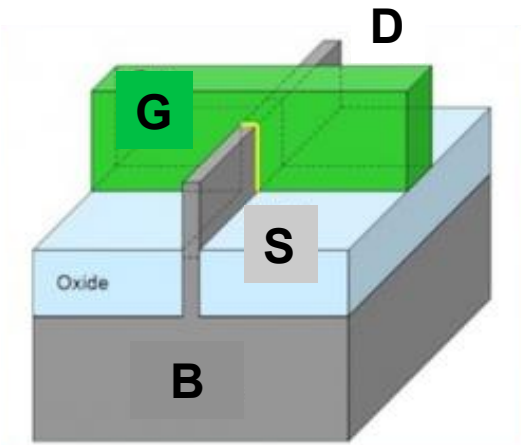


IBM

Scaling – Advanced Solutions





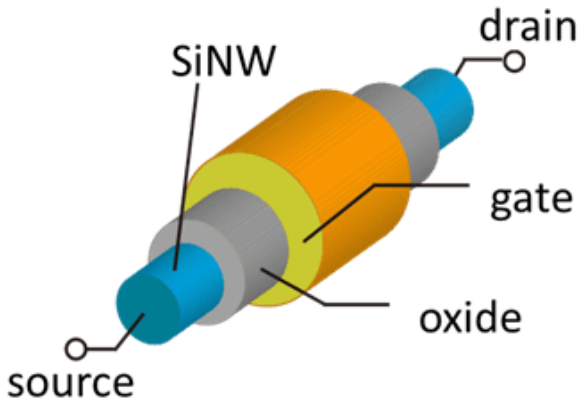


Successful scaling → control short L effect (OFF current)

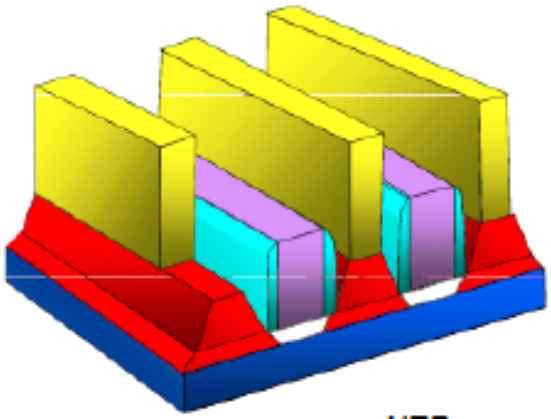
UTB-SOI: Reduce body thickness (Silicon On Insulator)

FinFET: Wrap Gate around Channel

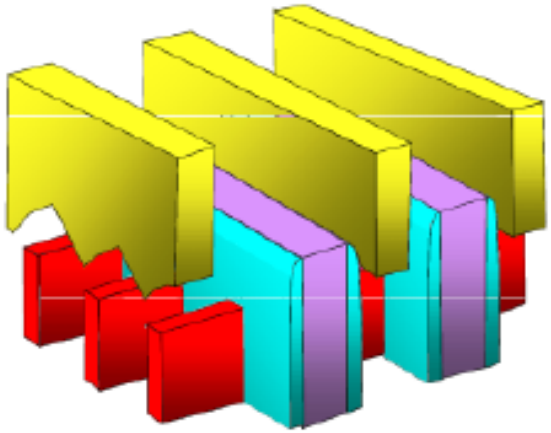
Nanowire FET: Full Gate wrapping



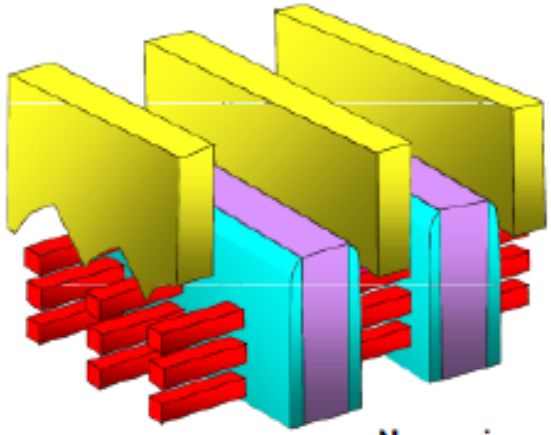
Scaling – Advanced Solutions



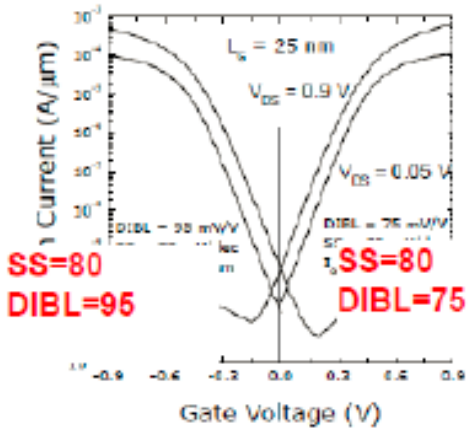
UTB



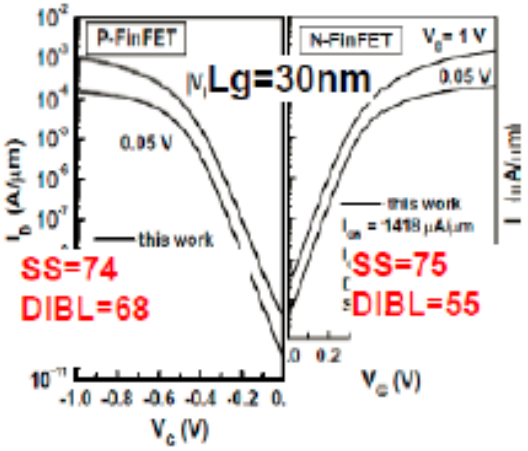
FinFET/Trigate



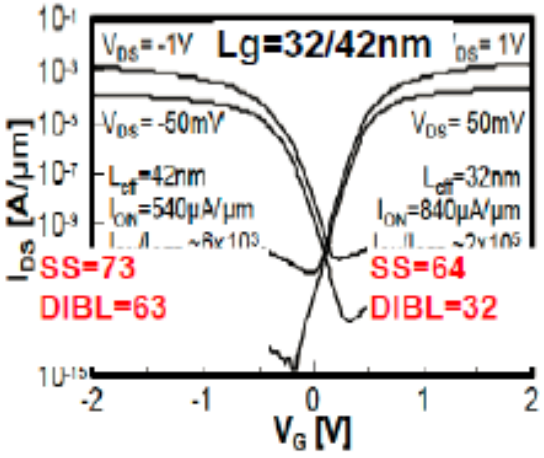
Nanowire



Cheng – IEDM 2009 (IBM)



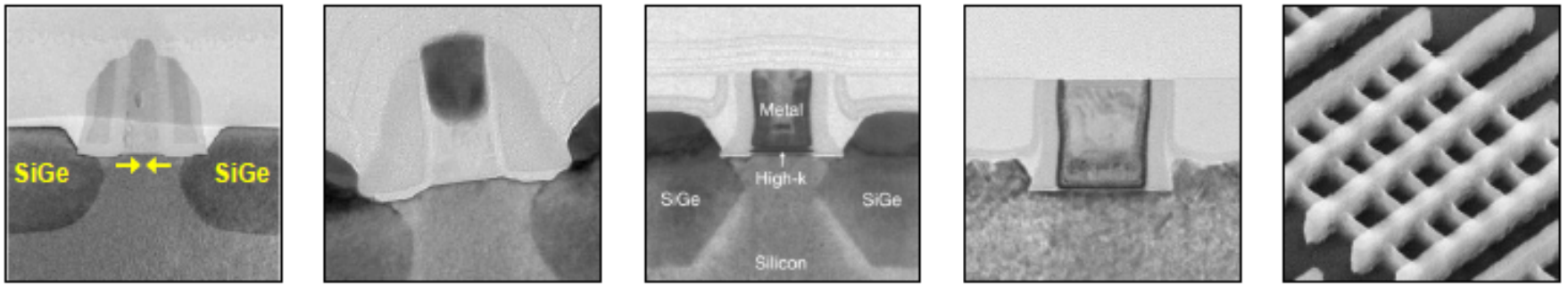
Yeh – IEDM 2010 (TSMC)



Tachi – IEDM 2010 (CEA-LETI)

Real Life Scaling Examples

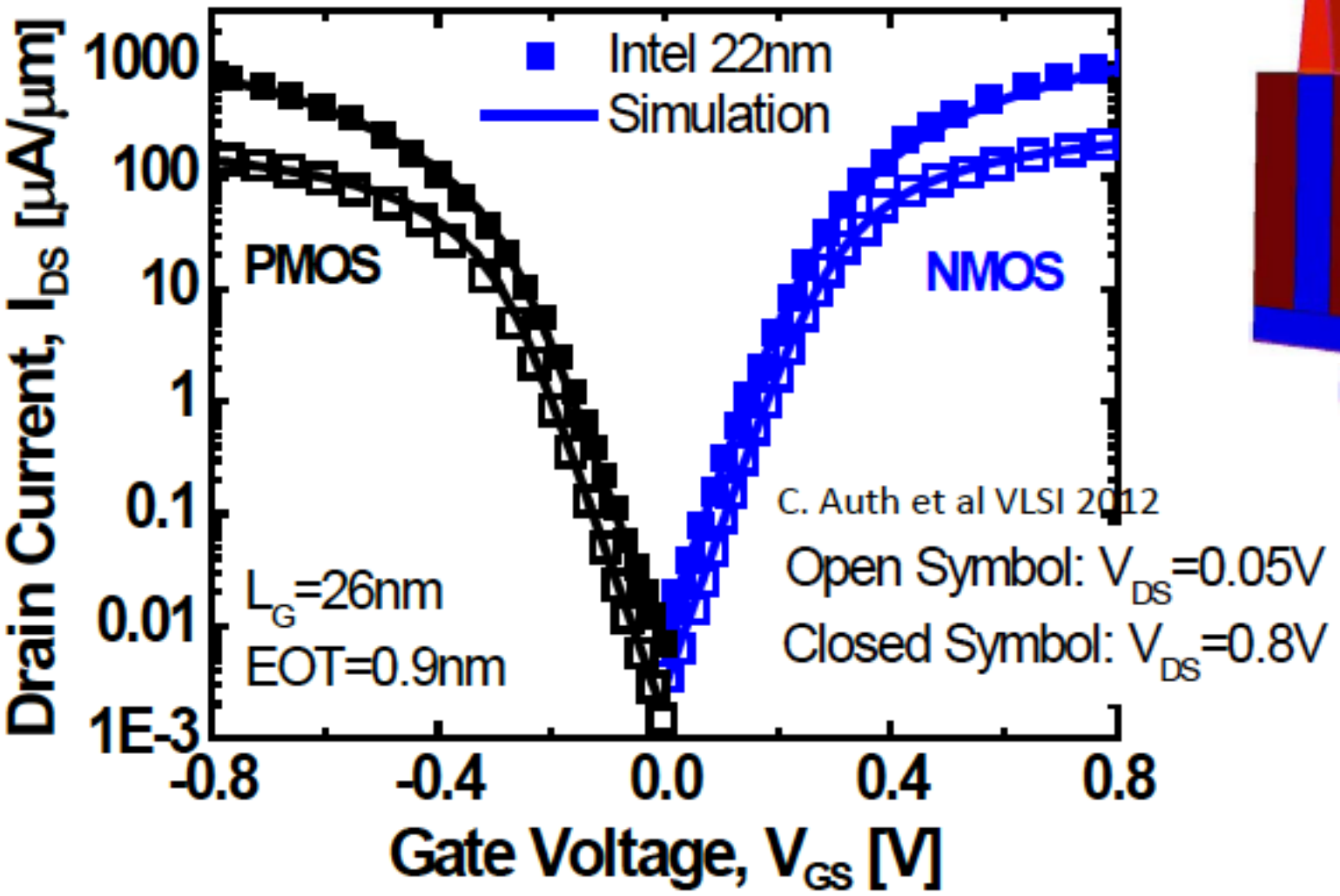
2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm

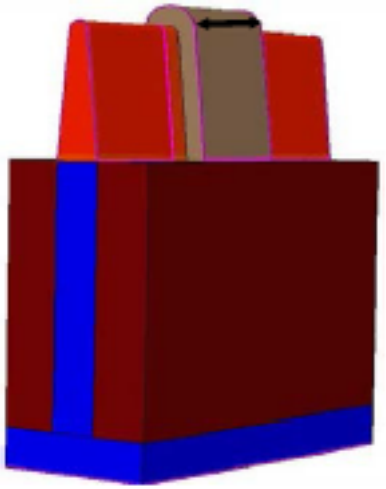


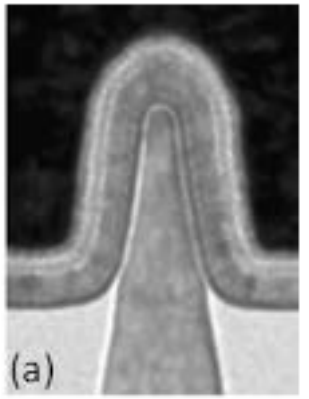
Strain - mobility **HKMG - leakage** **FinFET - SCE**

Intel

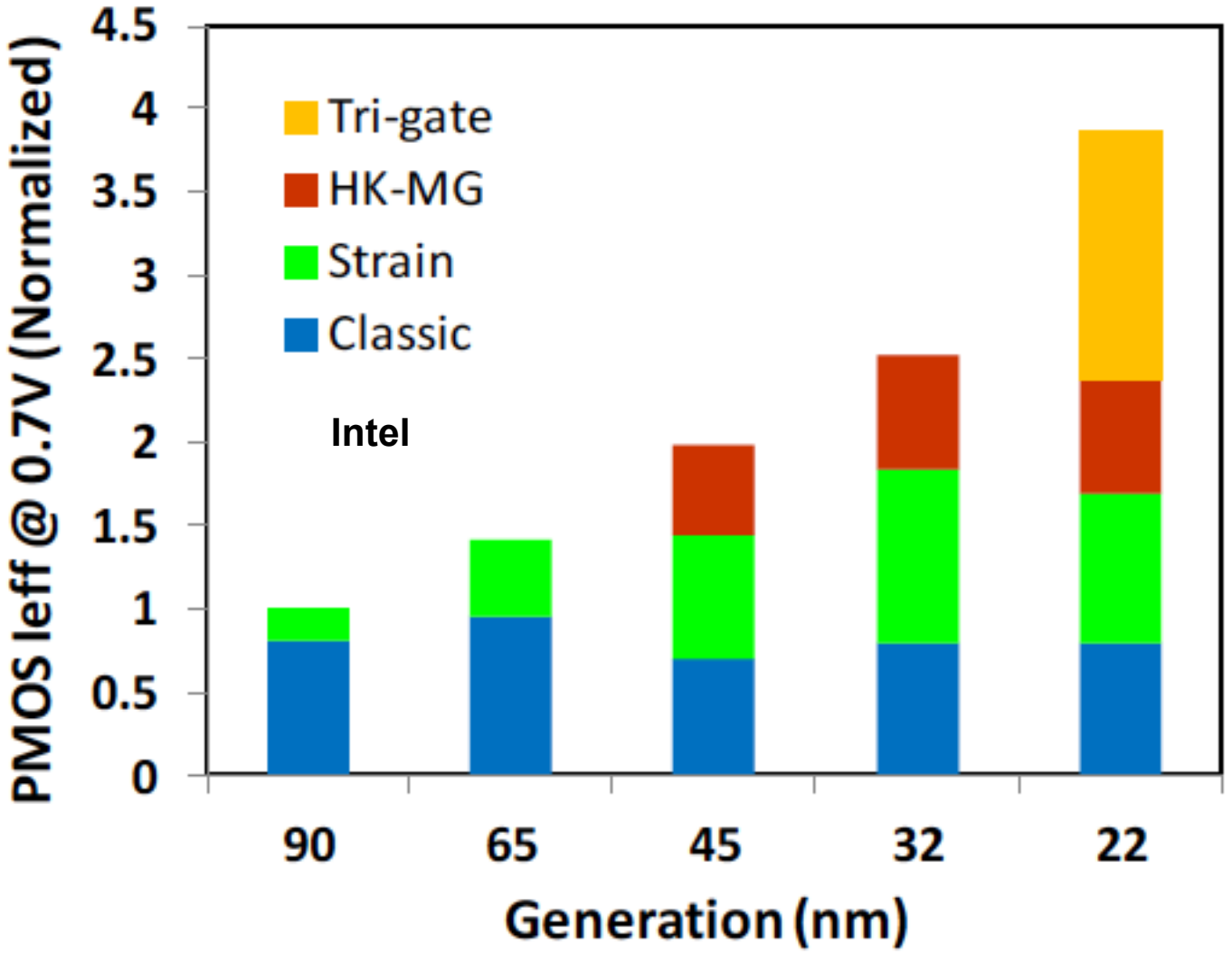
Intel 22nm FinFET



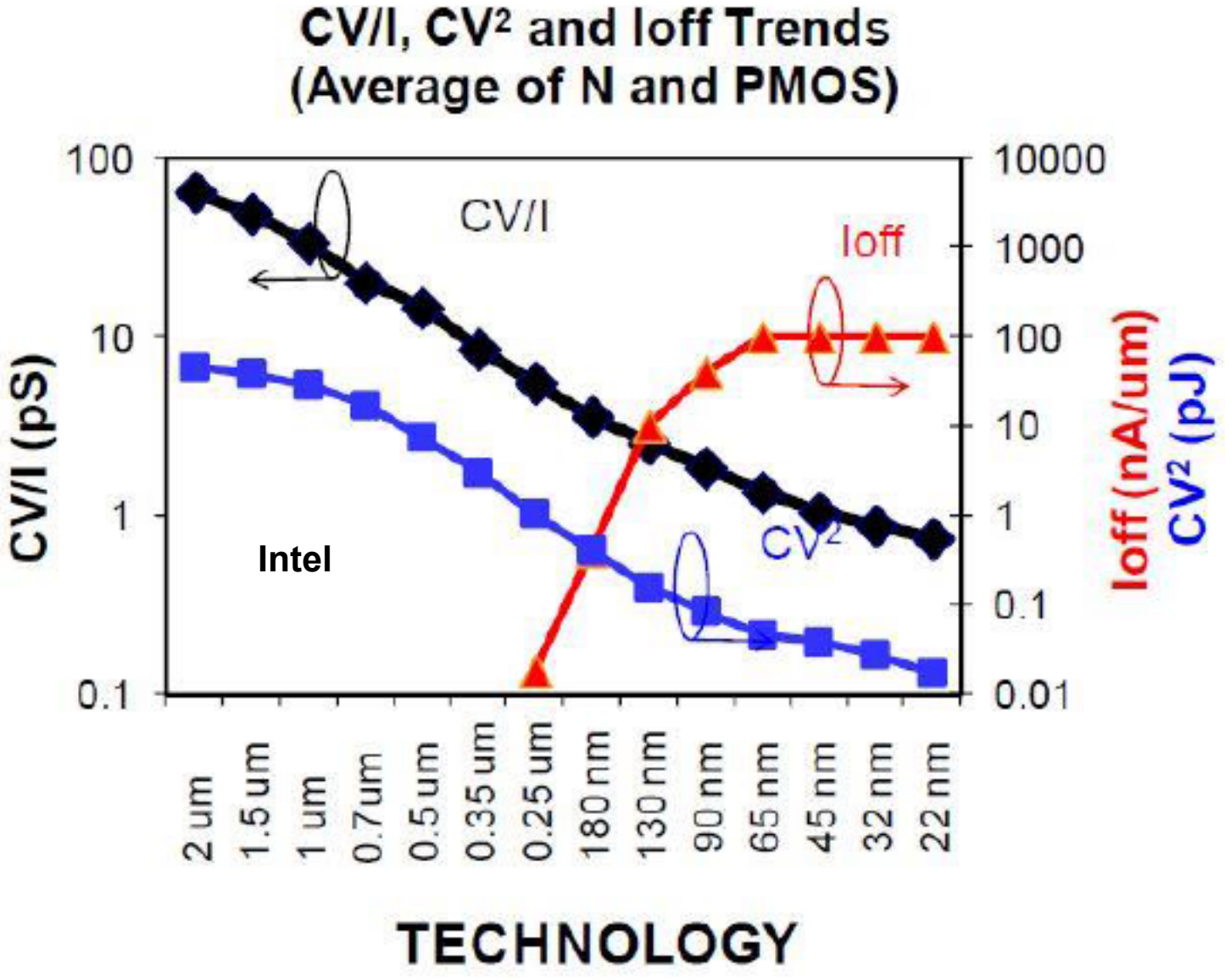




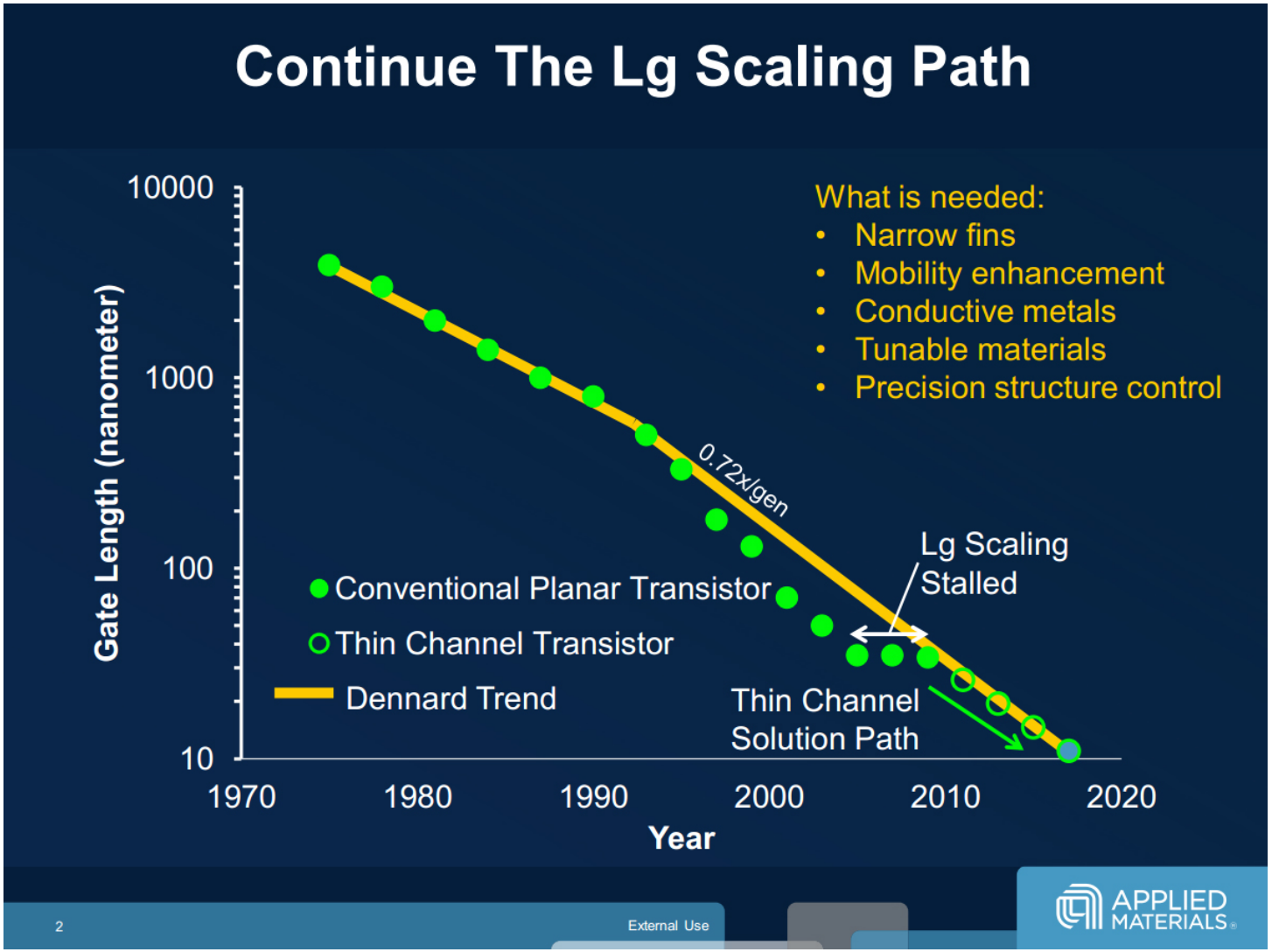
Different Performance Boosters



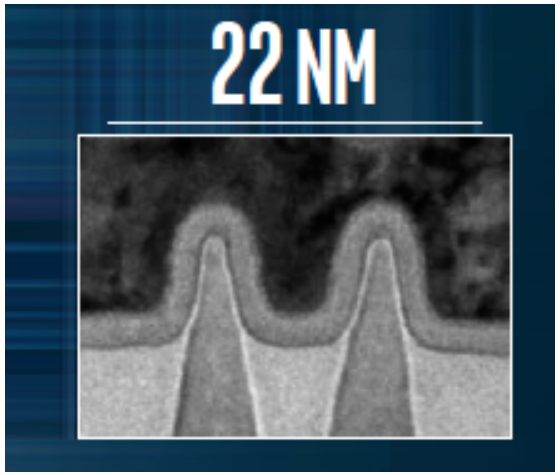
Scaling Trends → Performance Metrics



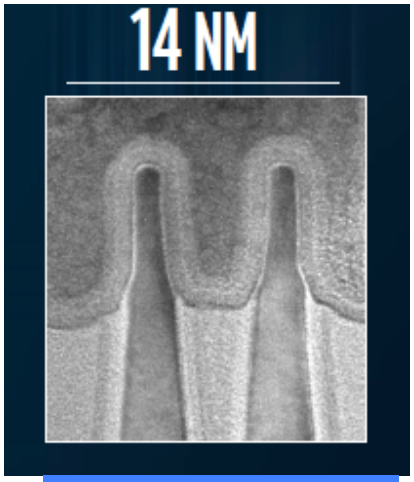
Thinner Channel Enables L Scaling



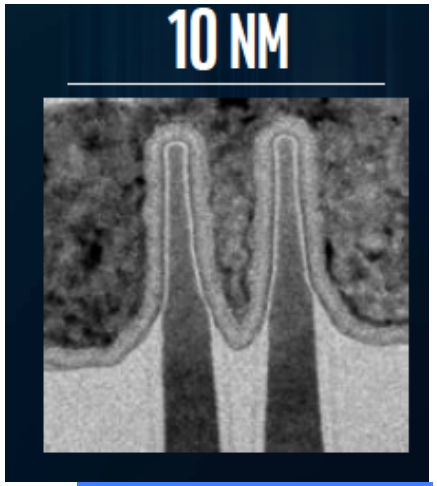
FinFET Scaling



2011 (Intel)
L=26nm
W=10nm (avg.)
H=34nm



2014 (Intel)
L=20nm
W=8nm (avg.)
H=42nm



2018 (Intel)
L=18nm
W=7nm (avg.)
H=50nm

Tall and skinny fins → Mechanical stability

Scaling: Node and Channel Lenth