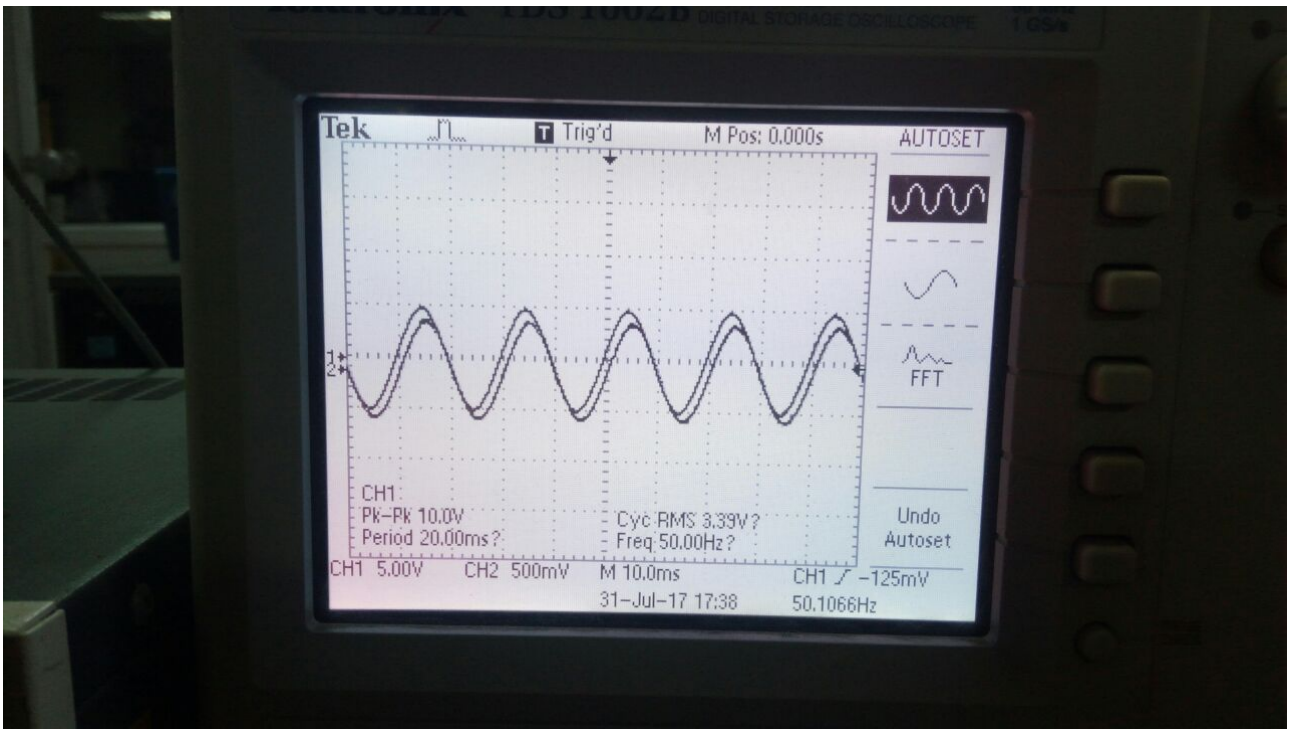
Experiment 1

Name : Devesh Kumar **Roll No:16d070044**
Batch:Monday **Table No:20**
Exp Date:
Name of TA/RA : Arindam Sardar

Part 1: RC circuits

1. Input and output waveforms for R=1k, C=1uF, V_{in} = 10 V_{p-p}, 50Hz sinusoidal signal.



There is phase shift between vin (ch1)and vc(ch2

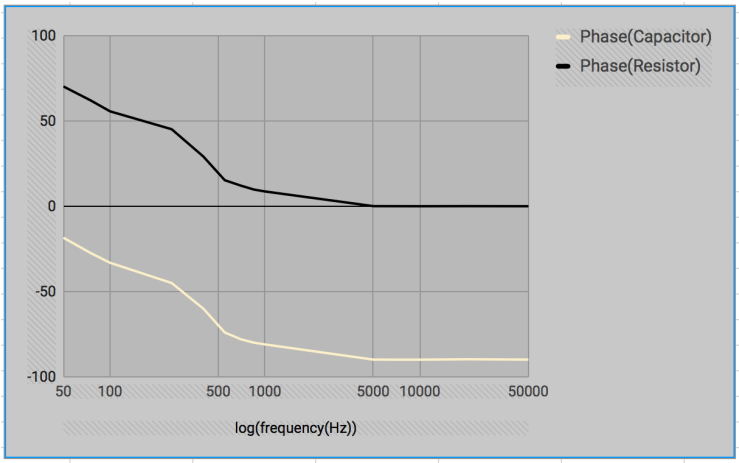
2. Frequency response

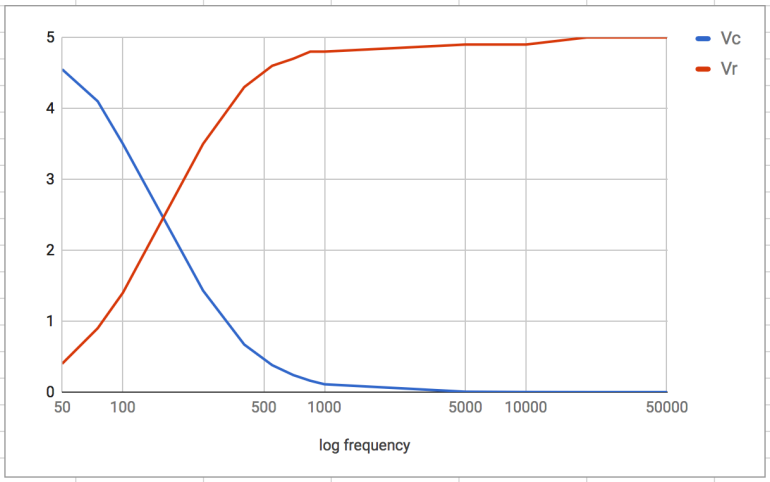
dB v/s log frequency plot

Φ v/s log frequency plot

Indicate the axes and scales properly
Show the cut-off frequency

Frequency	Vc	Vr	Phase(Capacitor)	Phase(Resistor)
50	4.55	0.4	-18.4	70.3
75	4.1	0.9	-27.4	62.1
100	3.5	1.4	-33.1	55.7
250	1.43	3.5	-45	45.2
400	0.67	4.3	-60	29.2
550	0.38	4.6	-74	15.3
700	0.24	4.7	-78	12.1
850	0.16	4.8	-80	9.8
1000	0.11	4.8	-81	8.7
5000	0.005	4.9	-89.9	0.1
10000	0.001	4.9	-89.95	0.05
20000	0	5	-89.7	0.1
50000	0	5	-89.9	0.05





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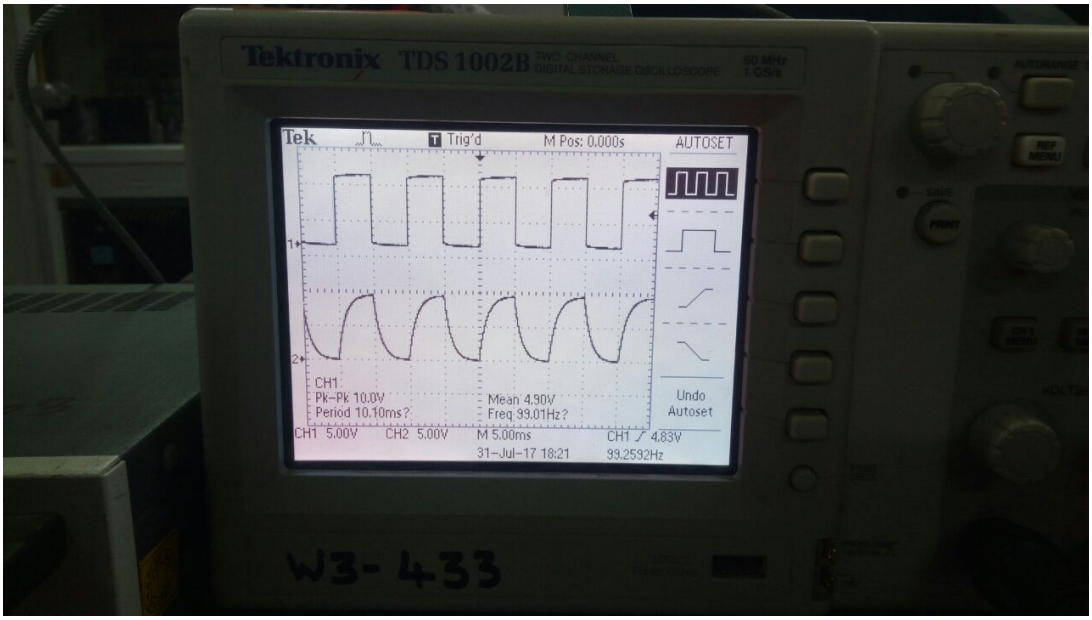
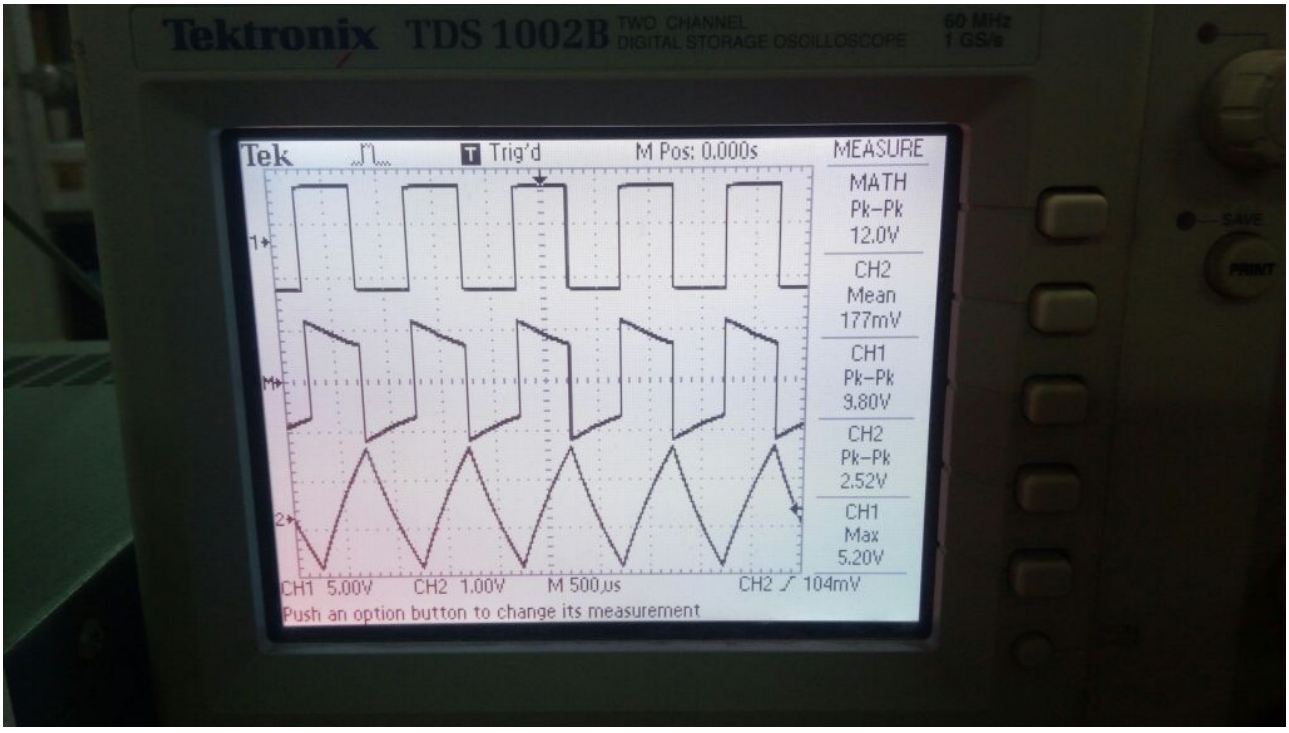
3.Comment on the plots:
Vp decreases with increase in frequency in both the cases . Thus the sign of vp in resistor is opposite to that of vp in capacitor
Vdp is directly proportional to frequency in case of resister. It only allows wave with high frequency to pass through. Vdp is inversely promotional to frequency in case of capacitor.

4. Response of RC circuit to square wave input: <<Specify R,C and input signal amplitude, and frequency clearly>



5. Effect of varying frequency on the output voltage :



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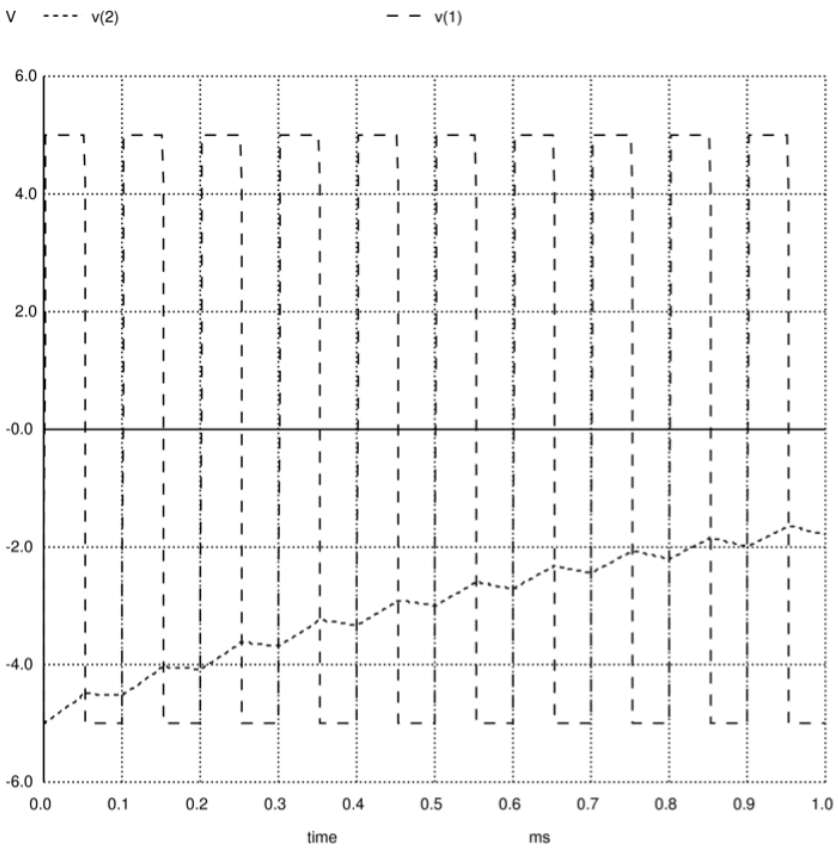
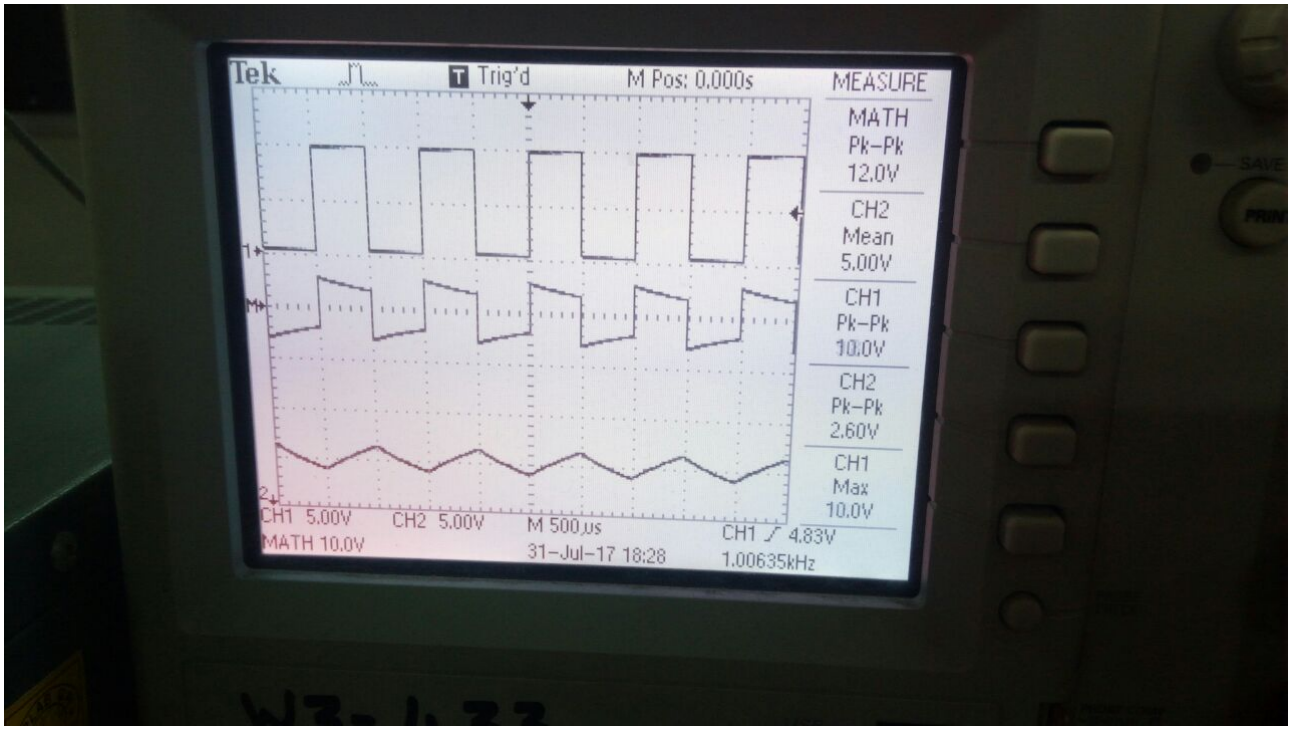


V out through capacitor (f 1000hz).as frequency increases capacitor gets less time accumulate charge so it takes more time to reach vin .If frequency is low then capacitor to is max value .

6. Response of RC circuit to square wave input with DC offset: <<Specify R,C and input signal amplitude, offset, and frequency clearly>>



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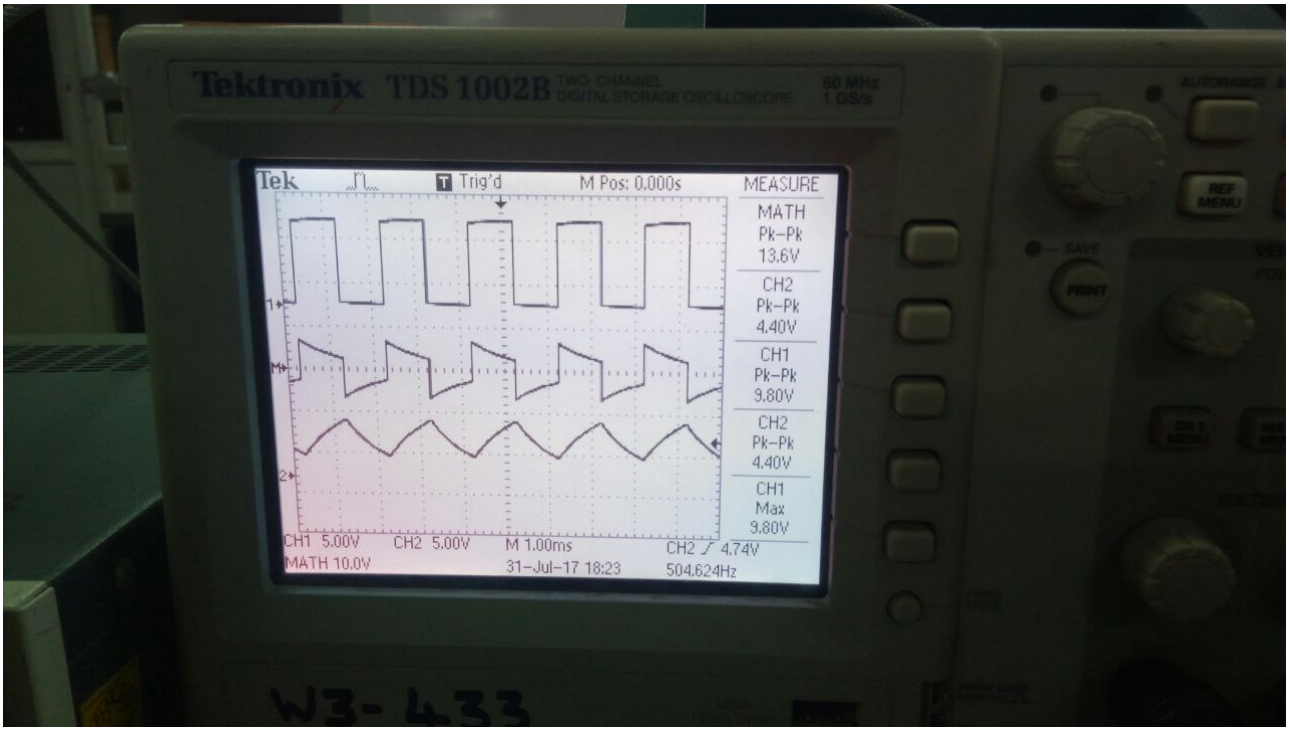
8.Effect of varying frequency on the output voltage



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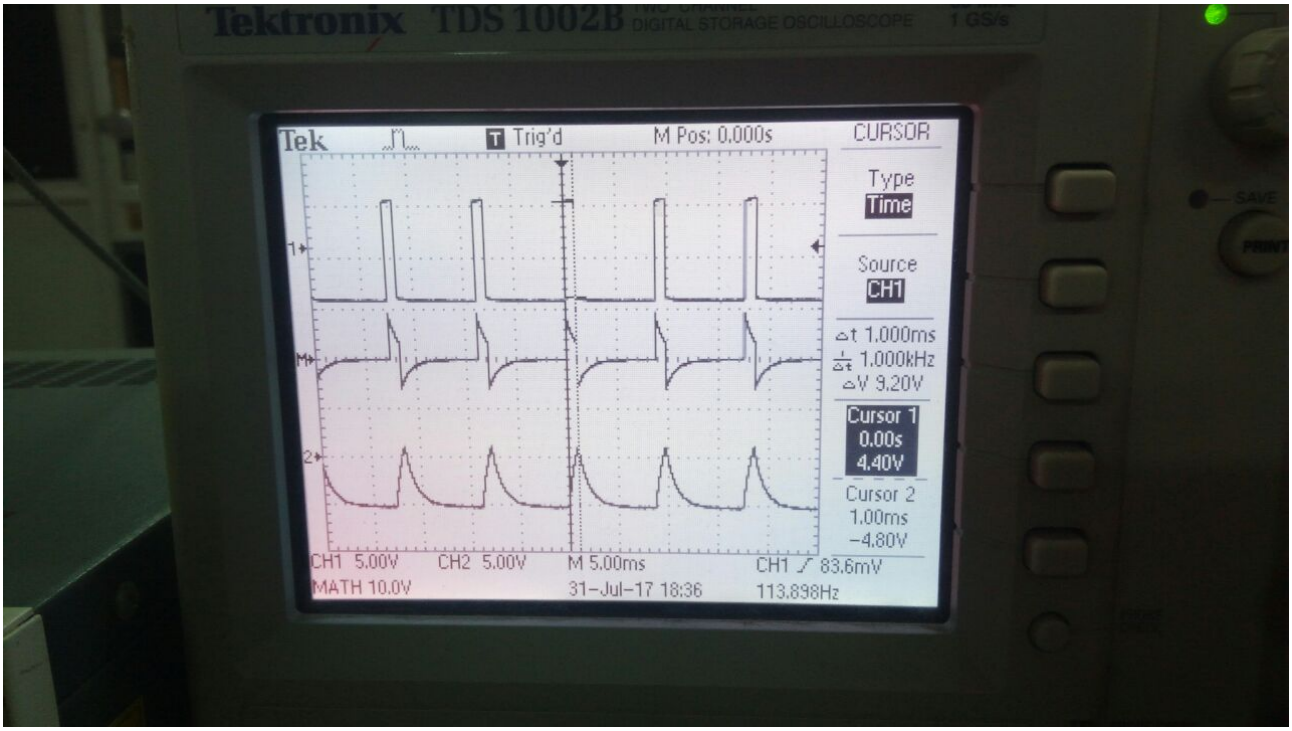
9. Change the duty cycle of the input voltage to 10 % and observe the input output waveforms.



In all the graph ch1 is vin, ch 2 is v across capacitor, m=Vin-Vc i.e voltage across resistor

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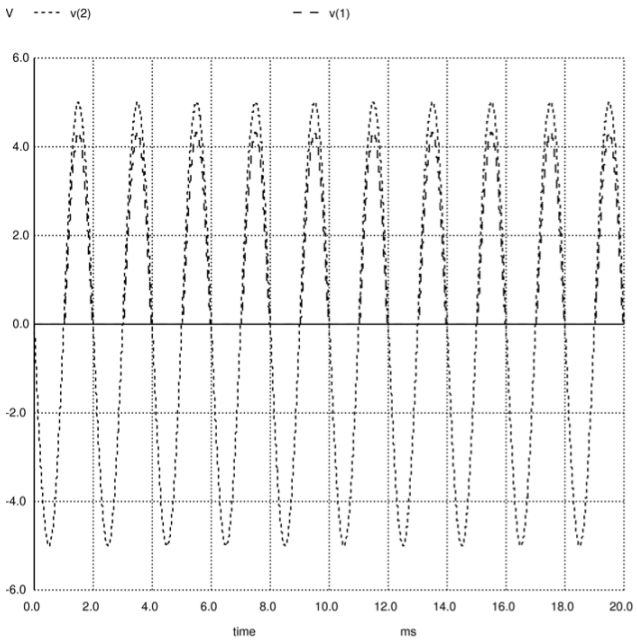
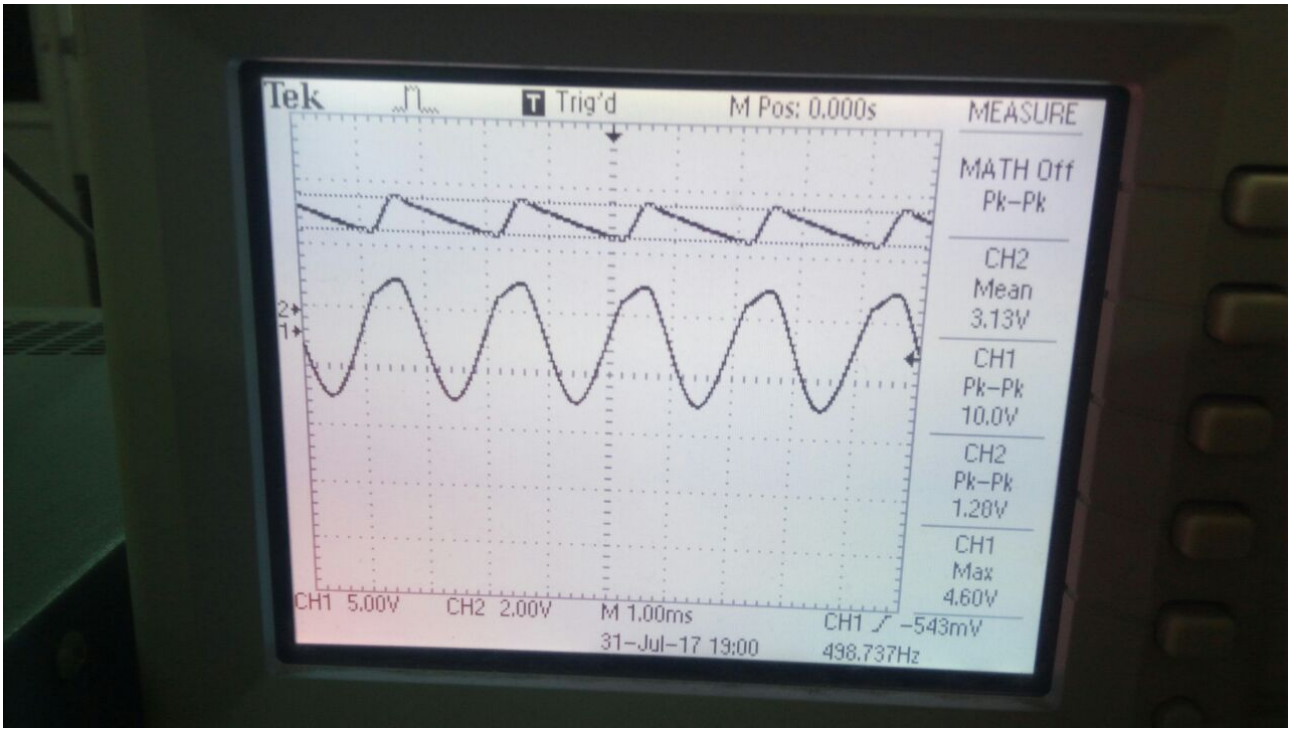
PART 2: RECTIFIER

1. Connect the half wave rectifier circuit shown in Fig.1. Observe the input and output waveforms for Vs = 10Vpp, 500Hz sinusoidal signal, R_L=1K and for 1N914 diode.



2.Now connect a capacitor of 4.7 µF across the load resistor R_L. Observe the input and output voltage waveform.



3.Comment on these waveforms.

When vin is positive ,diode conducts in normal way.as vin decrease the capacitor must discharge with time constant =rc. Thus it discharge slowly as we increase r or c.

When vout equal to vin then conduction happen again and capacitor charges

4.Vary the value of capacitor to 10μF, 4vin 7μF, and 100μF and observe the effect. Repeat for R_L=10K. Tabulate the readings in each case to estimate the ripple factor in Table 1 below.
Note: V_{R-PP} is peak-to-peak value of ripple voltage.

Rl	C	Vrpp	vdc	r
1	4.7	1.28	2.8	0.1344537815
1	10	0.72	2.98	0.07106198184
1	47	0.16	3	0.01568627451
10	4.7	0.4	3.93	0.02993563838
10	10	0.16	3.94	0.01194386384

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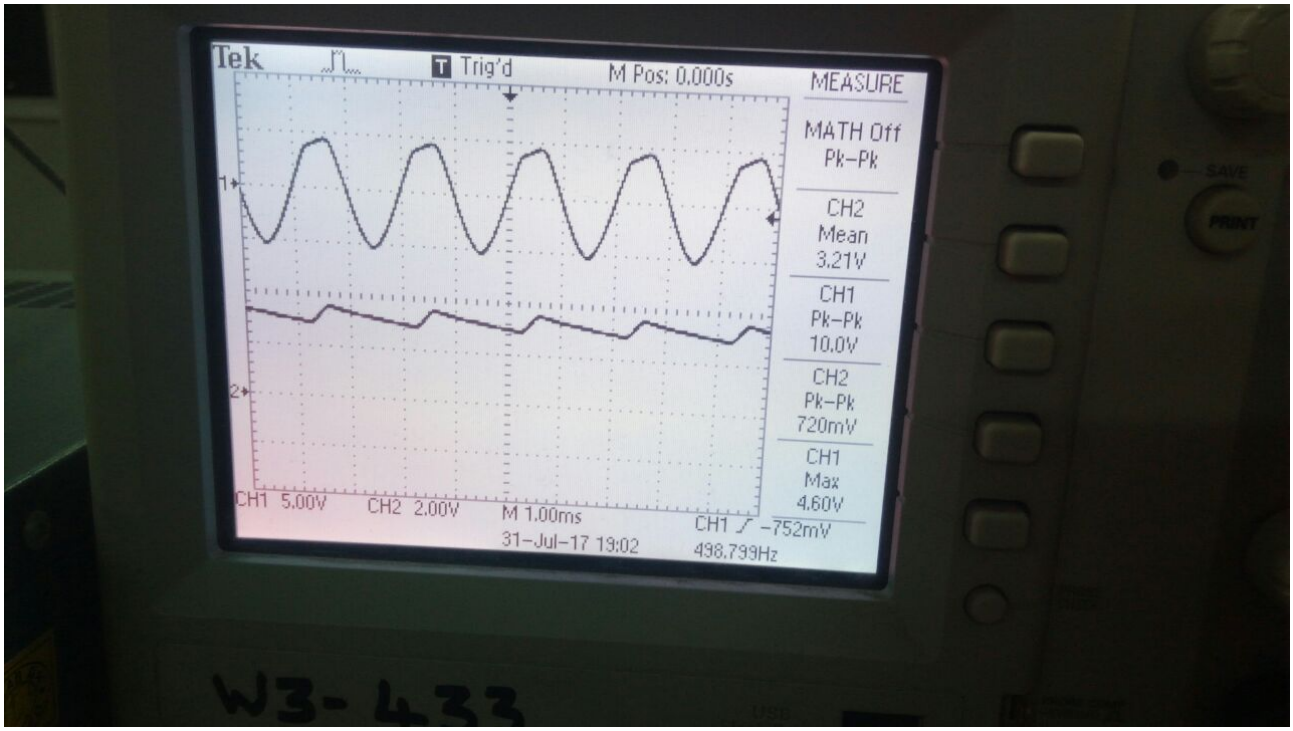

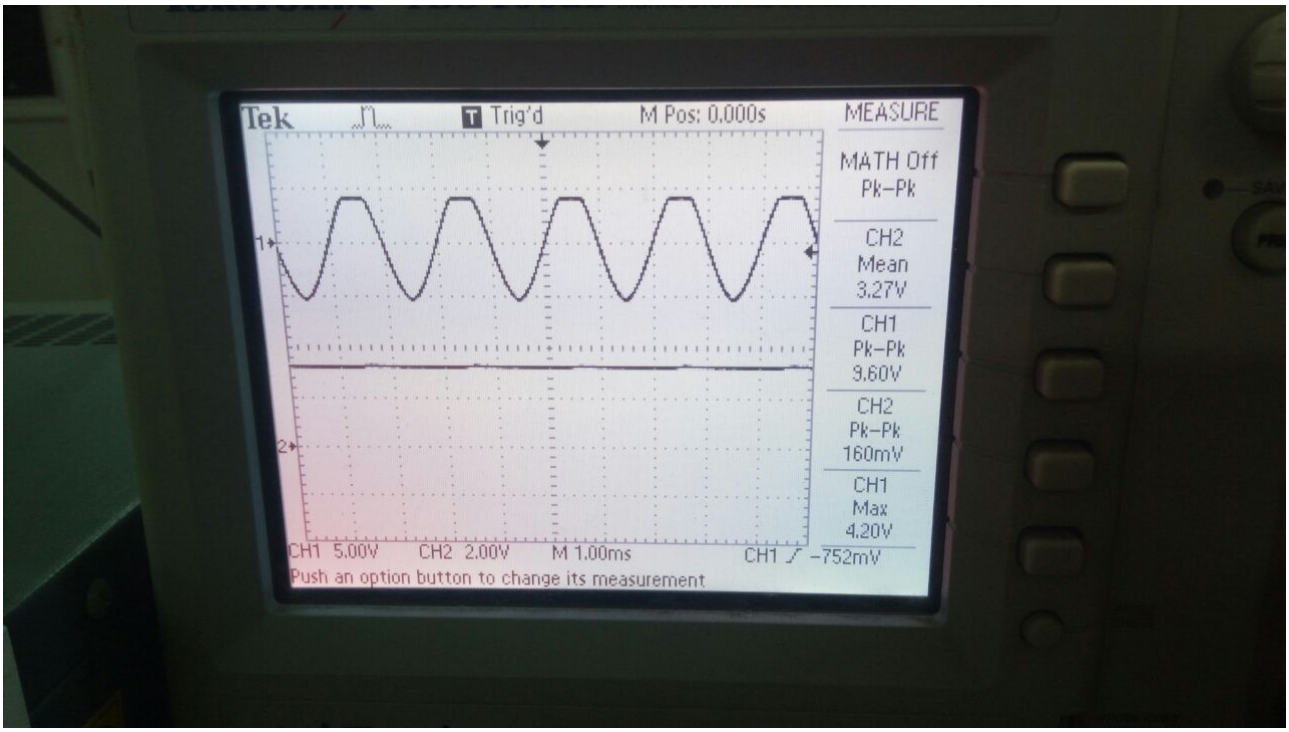

PART 3:CE AMPLIFIER

1. Wire up the circuit. Make sure that C_B, C_C, C_E are sufficiently large for the signal frequency of 5 kHz to be in the mid-band region.

Re = 2k ohm Rc = 3k ohm R1 = 27k ohm

2 Wire up the circuit. Make sure that C_B, C_C, C_E are sufficiently large for the signal frequency of 5 kHz to be in the mid-band region.

Cb = Cc = Ce = 47uF

3. Calculate A_{VL}, A_{V0}, R_i, R_o for your design

Avl = -gm (Rc || Rl) = -30
Avo = -gm (Rc) = -120
Rin = r pi || R1 || R2 = 4.6k ohm
Rout = Rc || Rl = 750 ohm

4 Check your calculations against measurements made with a signal frequency of 5 kHz (use oscilloscope, not multi-meter). Keep the input voltage sufficiently small so as to give an undistorted output. A voltage divider (with 1 kΩ and 47 Ω, for example) may be used.

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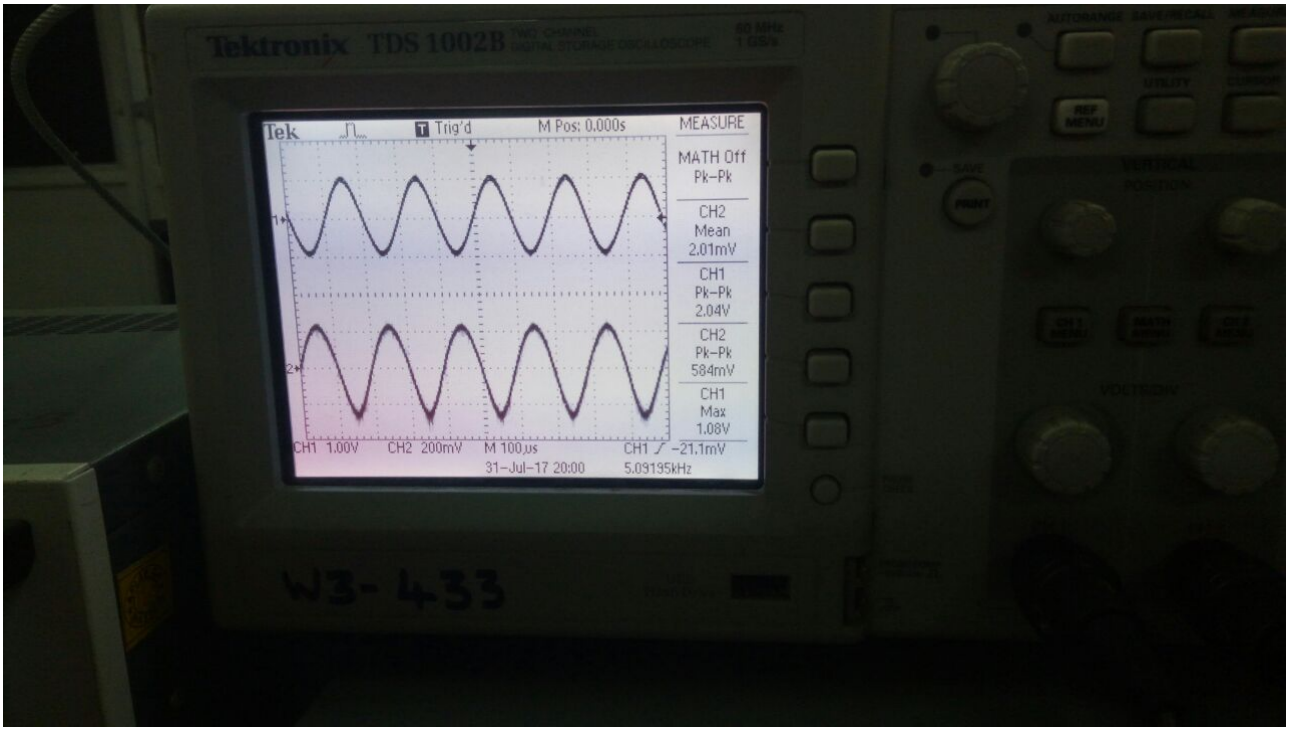
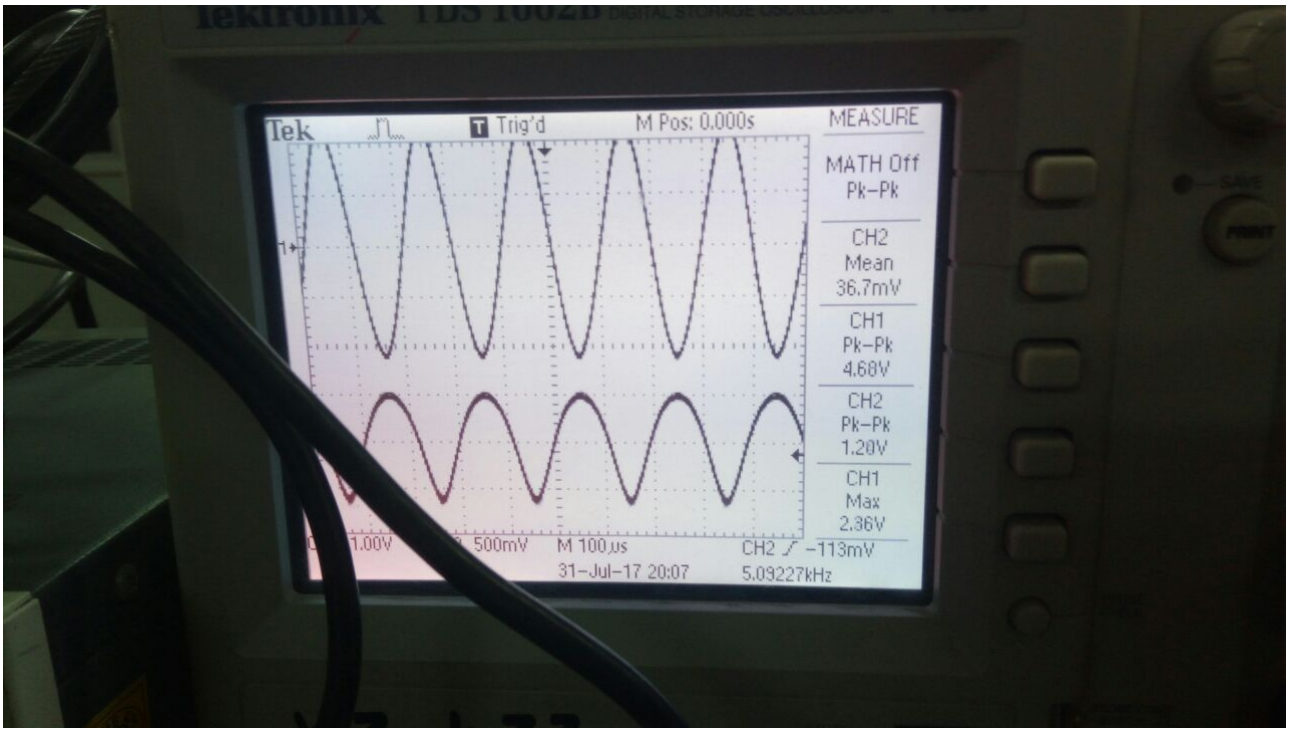


5 Increase the input amplitude to a point where you begin to see some distortion at the output. Note this amplitude.



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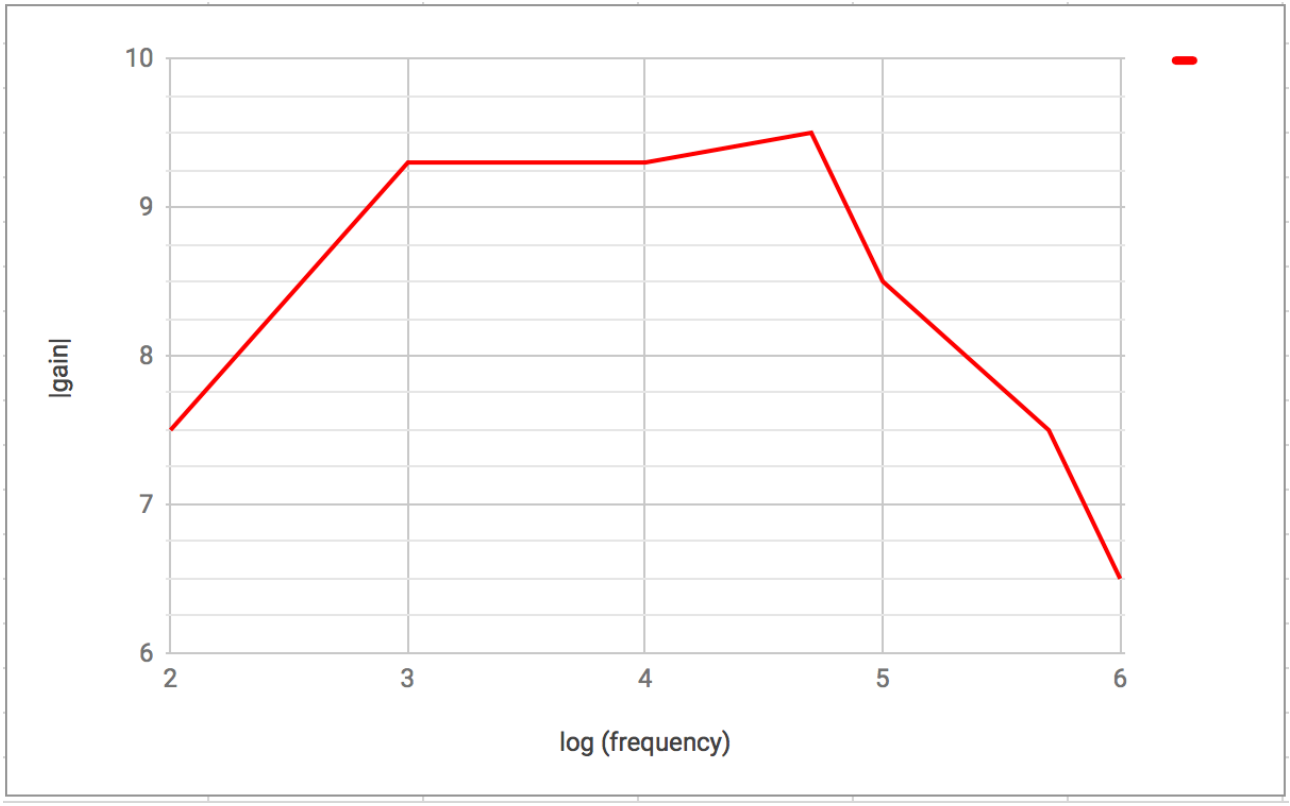
6.

frequency	log(frequency)	Vin(p-p) in mV	Vout(p-p) in mV	|gain|	vdb
100	2	20	250	12.5	-12.04119983
1000	3	20	500	25	-6.020599913
5000	3.698970004	20	520	26	-5.679933127
10000	4	20	515	25.75	-5.763855419
50000	4.698970004	20	520	26	-5.679933127
100000	5	20	520	26	-5.679933127
500000	5.698970004	20	360	18	-8.873949985
700000	5.84509804	20	300	15	-10.45757491
1000000	6	20	280	14	-11.05683937



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7 Partially bypassed R_E: Replace R_E with R_{E1} and R_{E2} (see figure), keeping the other component values the same as before. Select R_{E1} and R_{E2} to obtain approximately the same bias point (as the CE amplifier) and a gain of about 10.

R_{E1}=40 ohm and R_{E2} = 1.5k ohm

8 Calculate $A_{V\,L}$, $A_{V\,0}$, R_i, R_o for your design.

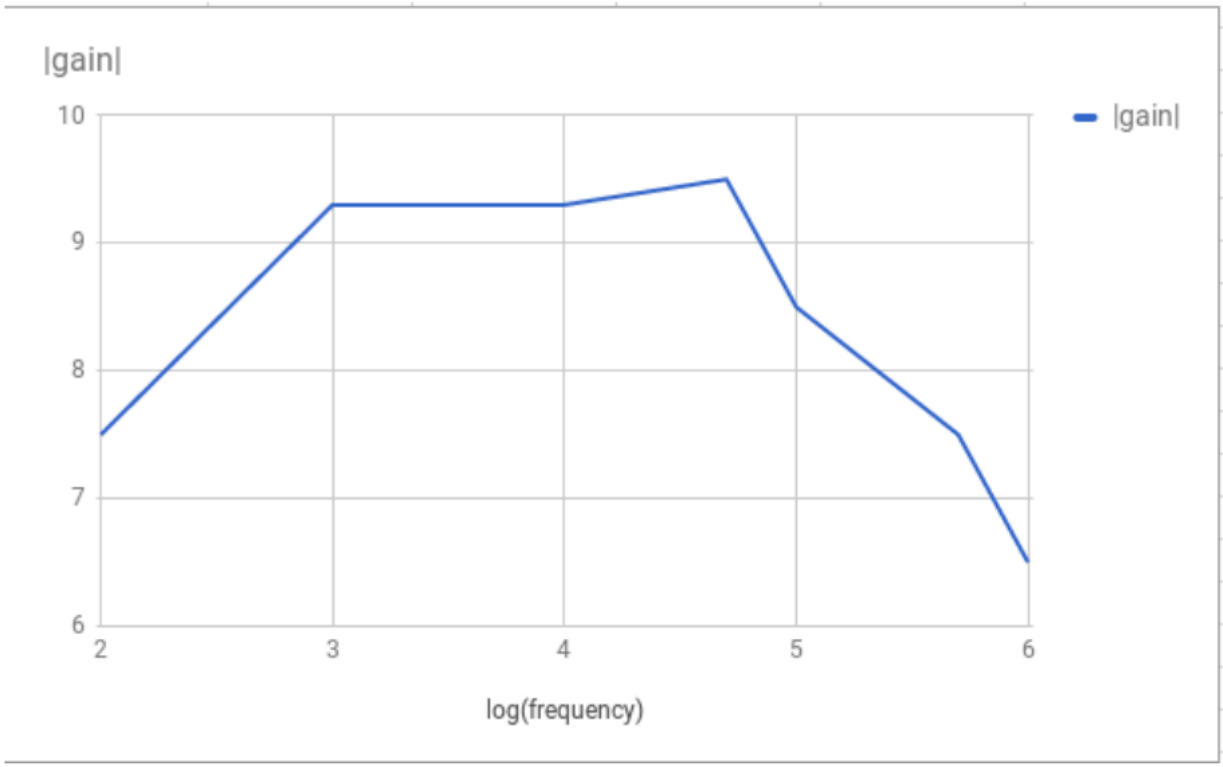
Avl = 10.1 Avo = 64 Ri = 36k Ro = 3k

9 Wire up the amplifier and repeat the measurements you made for the CE amplifier.

Gain in Partial bypass CE-Amplifier is less

10. Plot the frequency response of the two amplifiers on the same graph (log-log plot) and comment on the salient features you observe.

frequency	log(frequency)	Vin(p-p) in mV	Vout(p-p) in mV	|gain|	vdb
100	2	20	150	7.5	-16.47817482
1000	3	20	186	9.3	-14.60974112
5000	3.698970004	20	186	9.3	-14.60974112
10000	4	20	186	9.3	-14.60974112
50000	4.698970004	20	190	9.5	-14.42492798
100000	5	20	170	8.5	-15.39102157
500000	5.698970004	20	150	7.5	-16.47817482
1000000	6	20	130	6.5	-17.72113295


|gain|
10
9
8
7
6
2
3
4
5
6
log(frequency)
|gain|

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