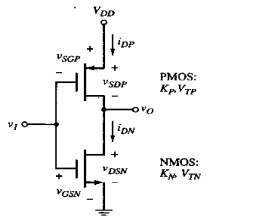
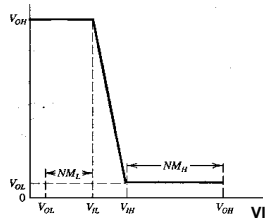
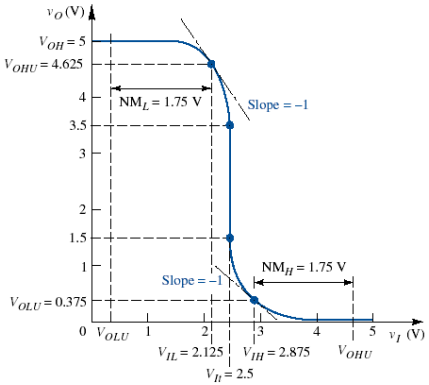
Concept of Noise Margins







NM_L=V_{IL}-V_{OL} (noise margin for low input)
NMH=V_{OH}-V_{IH} (noise margin for high input)

NM_L=V_{IL}-V_{OLU} (noise margin for low input)
NMH=V_{OHU} - V_{IH} (noise margin for high input)

Noise Margins equations

At point V_{IL} the NMOS is biased in the saturation region and PMOS is biased in the nonsaturation region

$$K_N[v_I - V_{TN}]^2 = K_P[2(V_{DD} - v_I + V_{TP})(V_{DD} - v_O) - (V_{DD} - v_O)^2] \quad (1)$$

Taking derivative with respect to V_I yields

$$2K_N[v_I - V_{TN}] = K_P\left[-2(V_{DD} - v_O) - 2(V_{DD} - v_I + V_{TP})\frac{dv_O}{dv_I} - 2(V_{DD} - v_O)\left(-\frac{dv_O}{dv_I}\right)\right] \quad (2)$$

At V_{IL} $\quad \frac{dv_O}{dv_I} = -1$

$$K_N[v_I - V_{TN}] = -K_P[(V_{DD} - v_O) - (V_{DD} - v_I + V_{TP}) + (V_{DD} - v_O)] \quad (3)$$

$\Rightarrow$ Solving for v_O produces

$$v_O = V_{OHU} = \frac{1}{2}\left\{\left(1 + \frac{K_N}{K_P}\right)v_I + V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}\right\} \quad (4)$$

Assume CMOS is symmetrical i. e. K_N=K_P

$$\Rightarrow \quad v_O = V_{OHU(K_N=K_P)} = \tfrac{1}{2}\{2v_I + V_{DD} - V_{TN} - V_{TP}\} \quad (5)$$

Substituting (5) into (1) $\Rightarrow$

$$v_I = V_{IL(K_N=K_P)} = V_{TN} + \tfrac{3}{8}(V_{DD} + V_{TP} - V_{TN}) \quad (6)$$

Noise Margins equations (cont.)

At point V_{IH} the NMOS is biased in the nonsaturation region and PMOS is biased in the saturation region

$$K_N[2(v_I - V_{TN})v_O - v_O^2] = K_P(V_{DD} - v_I + V_{TP})^2 \quad (6)$$

Taking derivative with respect to V_I yields

$$K_N\left[2(v_I - V_{TN})\frac{dv_O}{dv_I} + 2v_O - 2v_O\frac{dv_O}{dv_I}\right] = 2K_P(V_{DD} - v_I + V_{TP})(-1) \quad (7)$$

Setting the derivative equal to -1, we find that

$$K_N[-(v_I - V_{TN}) + v_O + v_O] = -K_P[V_{DD} - v_I + V_{TP}] \quad (8)$$

The output voltage v_O is then

$$v_O = V_{OLU} = \frac{v_I\left(1 + \frac{K_N}{K_P}\right) - V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}}{2\left(\frac{K_N}{K_P}\right)} \quad (9)$$

Assume CMOS is symmetrical i. e. K_N=K_P

$$v_O = V_{OLU(K_N=K_P)} = \tfrac{1}{2}\{2v_I - V_{DD} - V_{TN} - V_{TP}\} \quad (10)$$

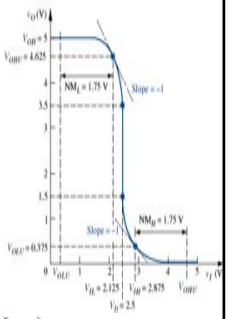
Substituting (10) into (6) $\Rightarrow$

$$v_I = V_{IH(K_N=K_P)} = V_{TN} + \tfrac{5}{8}(V_{DD} + V_{TP} - V_{TN})$$

Summary of the noise margin of a symmetrical CMOS inverter

$NM_L = V_{IL} - V_{OLU}$ (noise margin for low input)

$NMH = V_{OHU} - V_{IH}$ (noise margin for high input)



$$v_I = V_{IL(K_N=K_P)} = V_{TN} + \tfrac{3}{8}(V_{DD} + V_{TP} - V_{TN})$$

$$v_O = V_{OLU(K_N=K_P)} = \tfrac{1}{2}\{2v_I - V_{DD} - V_{TN} - V_{TP}\}$$

$$v_O = V_{OHU(K_N=K_P)} = \tfrac{1}{2}\{2v_I + V_{DD} - V_{TN} - V_{TP}\}$$

$$v_I = V_{IH(K_N=K_P)} = V_{TN} + \tfrac{5}{8}(V_{DD} + V_{TP} - V_{TN})$$

Summary of the noise margin of asymmetrical CMOS inverter

$NM_L = V_{IL} - V_{OLU}$ (noise margin for low input)

$NMH = V_{OHU} - V_{IH}$ (noise margin for high input)

$$v_I = V_{IL} = V_{TN} + \frac{(V_{DD} + V_{TP} - V_{TN})}{\left(\frac{K_N}{K_P} - 1\right)}\left[2\sqrt{\frac{\frac{K_N}{K_P}}{\frac{K_N}{K_P} + 3}} - 1\right]$$

$$v_O = V_{OLU} = \frac{v_I\left(1 + \frac{K_N}{K_P}\right) - V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}}{2\left(\frac{K_N}{K_P}\right)}$$

$$v_O = V_{OHU} = \frac{1}{2}\left\{\left(1 + \frac{K_N}{K_P}\right)v_I + V_{DD} - \left(\frac{K_N}{K_P}\right)V_{TN} - V_{TP}\right\}$$

$$v_I = V_{IH} = V_{TN} + \frac{(V_{DD} + V_{TP} - V_{TN})}{\left(\frac{K_N}{K_P} - 1\right)}\left[\frac{2\frac{K_N}{K_P}}{\sqrt{3\frac{K_N}{K_P} + 1}} - 1\right]$$

Example 16.11 **Objective:** Determine the noise margins of a CMOS inverter.

Consider a CMOS inverter biased at $V_{DD} = 5$ V. Assume the transistors are matched with $K_N = K_P$ and $V_{TN} = -V_{TP} = 1$ V.

Solution: From Equation (16.57), the input voltage at the transition points, or the inverter switching point, is 2.5 V. Since $K_N = K_P$, V_{IL} is, from Equation (16.73)

$$V_{IL} = V_{TN} + \frac{1}{8}(V_{DD} + V_{TP} - V_{TN}) = 1 + \frac{1}{8}(5 - 1 - 1) = 2.125\text{ V}$$

Point V_{IH} is, from Equation (16.79)

$$V_{IH} = V_{TN} + \frac{3}{8}(V_{DD} + V_{TP} - V_{TN}) = 1 + \frac{3}{8}(5 - 1 - 1) = 2.875\text{ V}$$

The output voltages at points V_{IL} and V_{IH} are determined from Equations (16.72) and (16.78), respectively. They are

$$V_{OHU} = \frac{1}{2}[2V_{IL} + V_{DD} - V_{TN} - V_{TP}]$$
$$= \frac{1}{2}[2(2.125) + 5 - 1 + 1] = 4.625\text{ V}$$

and

$$V_{OLU} = \frac{1}{2}[2V_{IH} - V_{DD} - V_{TN} - V_{TP}]$$
$$= \frac{1}{2}[2(2.875) - 5 - 1 + 1] = 0.375\text{ V}$$

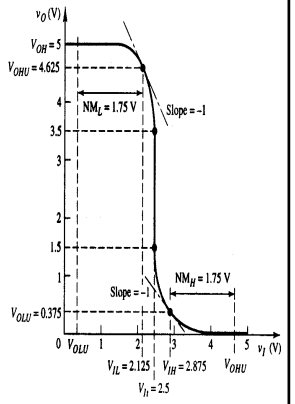
The noise margins are therefore

$$NM_L = V_{IL} - V_{OLU} = 2.125 - 0.375 = 1.75\text{ V}$$

and

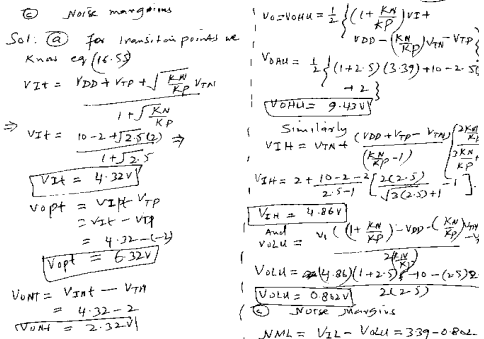
$$NM_H = V_{OHU} - V_{IH} = 4.625 - 2.875 = 1.75\text{ V}$$

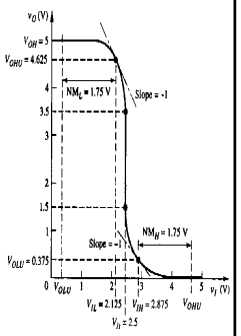
Comment: The results of this example are shown in Figure 16.43. Since the two transistors are electrically identical, the voltage transfer curve and the resulting critical voltages are symmetrical. Also, $(V_{OH} - V_{OHU}) = 0.375$ V, which is less than $|V_{TP}|$, and $(V_{OLU} - V_{OL}) = 0.375$ V, which is less than V_{TN}. As long as the input voltage remains within the limits of the noise margins, no logic error will be transmitted through the digital system.



Test Your Understanding

***16.16** A CMOS inverter is biased at $V_{DD} = 10$ V. The transistor parameters are: $V_{TN} = 2$ V, $V_{TP} = -2$ V, $K_N = 200\,\mu A/V^2$, and $K_P = 80\,\mu A/V^2$. (a) Sketch the voltage transfer curve. (b) Determine the critical voltages V_{IL} and V_{IH}, and the corresponding output voltages. (c) Calculate the noise margins NM_L and NM_H. (Ans. (b) $V_{IL} = 3.39$ V, $V_{IH} = 4.86$ V (c) $NM_L = 2.59$ V, $NM_H = 4.57$ V)



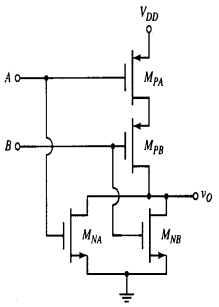


CMOS Logic Circuits

Large scale integrated CMOS logic circuits such as watched, calculators, and microprocessors are constructed by using basic CMOS NOR and NAND gates. Therefore, understanding of these basic gates is very important for the designing of very large scale integrated (VLSI) logic circuits.

CMOS NOR gate

CMOS NOR gate can be constructed by using two parallel NMOS devices and two series PMOS transistors as shown in the figure. In the CMOS NOR gate the output is at logic 1 when all inputs are low. For all other possible inputs, output is low or at logic 0.



A	B	v_O
0	0	V_{DD}
V_{DD}	0	0
0	V_{DD}	0
V_{DD}	V_{DD}	0

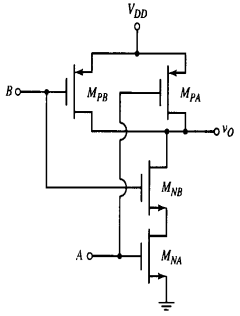
(a) (b)

Figure 16.44 (a) Two-input CMOS NOR logic circuit and (b) truth table

CMOS NAND gate

In CMOS NAND gate the output is at logic 0 when all inputs are high.

For all other possible inputs, output is high or at logic 1.



A	B	v_O
0	0	V_{DD}
V_{DD}	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

(a) (b)

Figure 16.45 (a) Two-input CMOS NAND logic circuit and (b) truth table

How can we design CMOS NOR symmetrical gate?

- In order to obtained symmetrical switching times for the high-to-low and low-to-high output transitions, the **effective** conduction (design) parameters of the **composite** PMOS and **composite** NMOS device must be equal. For the CMOS NOR gate we can write as,

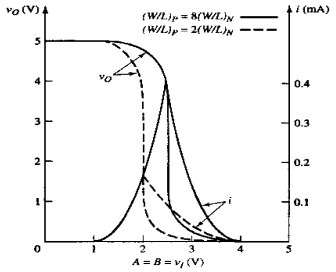
$K_{CN}=K_{CP}$

By recalling effective channel width and effective channel length concept, the effective conduction parameter for NMOS and PMOS for a CMOS NOR can be written as,

Since $K'_n \sim 2K'_p$ $\quad \frac{K_n'}{2}\left(\frac{2W}{L}\right)_N = \frac{K_p'}{2}\left(\frac{W}{2L}\right)_p$

$2\left(\frac{2W}{L}\right)_N = \left(\frac{W}{2L}\right)_p$ or $\left(\frac{W}{L}\right)_P = 8\left(\frac{W}{L}\right)_N$

For asymmetrical case switching time is longer

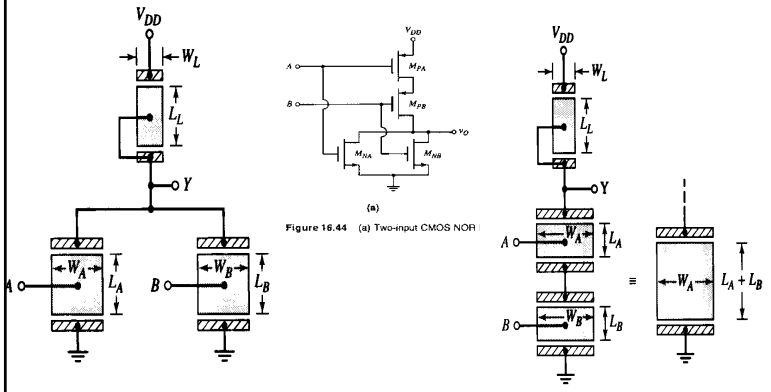


This implies that in order to get the symmetrical switching properties , the width to length ratio of PMOS transistor must be approximately eight times that of the NMOS device.

Concept of effective width to length ratios

Parallel combination

Series combination



(a)

Figure 16.44 (a) Two-input CMOS NOR

D16.19 In the two-input CMOS NAND gate in Figure 16.45(a), determine the relationship between the (W/L) ratios of the n-channel and p-channel transistors such that the composite conduction parameters of the PMOS and NMOS devices are equal. (Ans. $(W/L)_N = 2(W/L)_P$)

D16.20 Design a three-input CMOS NOR logic gate such that the effective conduction parameters of the composite PMOS and NMOS transistors are equal. Determine $(W/L)_P/(W/L)_N$, where (W/L) is the width-to-length ratio of the individual PMOS and NMOS transistors. (Ans. $(W/L)_P = 18(W/L)_N$)

D16.19 on page 1051

Reference: 2 input CMOS NAND gate.

Determine relationship b/w the n-channel and p-channel transistors, such that composite conduction parameters of the PMOS and NMOS devices are equal.

ie $K_{N,eff} = K_{P,eff}$

Sol: Inspection of figure 16.45a shows that the effective channel width of the parallel P MOS device is twice the individual width and effective channel length of the series NMOS Transistors is twice the individual length. i.e.

$$\left(\frac{K_n'}{2}\right)\left(\frac{W}{2L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{2W}{L}\right)_P$$

Since $K_n' \simeq 2K_P'$

$$\Rightarrow \left(\frac{2K_P'}{2}\right)\left(\frac{W}{2L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{2W}{L}\right)_P$$

$$\Rightarrow \frac{1}{2}\left(\frac{W}{L}\right)_N = K_P'\left(\frac{W}{L}\right)_P$$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_P}$$

16.20 on page 1051

Design a three input CMOS NOR logic gate such that $K_{N,eff} = K_{P,eff}$

Determine $(W/L)_P/(W/L)_N$

Sol: In case of the input CMOS NOR gate we have three NMOS parallel transistors three PMOS series Transistor

$$\Rightarrow \left(\frac{K_n'}{2}\right)\left(\frac{3W}{L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{3W}{3L}\right)$$

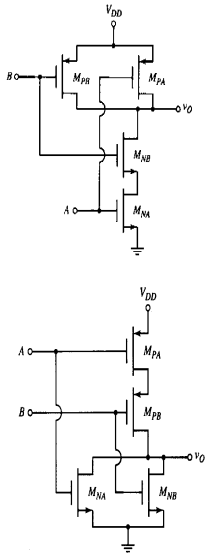
Since $K_n' \simeq 2K_P'$

$$\left(\frac{2K_P'}{2}\right)\left(\frac{3W}{L}\right)_N = \left(\frac{K_P'}{2}\right)\left(\frac{3W}{3L}\right)$$

$$3\left(\frac{W}{L}\right)_N = \frac{1}{6}\left(\frac{W}{L}\right)_P$$

$$\Rightarrow \boxed{\frac{(W/L)_P}{(W/L)_N} = 18}$$

one n mos added in II and 1 pmos in series

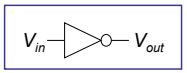


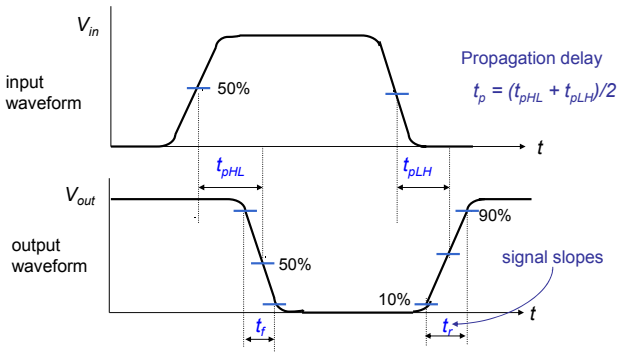
Fan-In and Fan-Out

- The Fan-in of a gate is the number of its inputs. Thus a four input NOR gate has a fan-In of 4.
- Similarly, Fan-Out is the maximum number of similar gates that a gate can drive while remaining within guaranteed specifications.

Propagation Delay Definitions

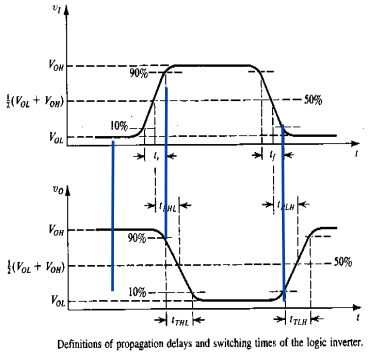
The propagation delay t_p of a gate defines how quickly it responds to a change at its input(s).





Switching Time and Propagation Delay Time

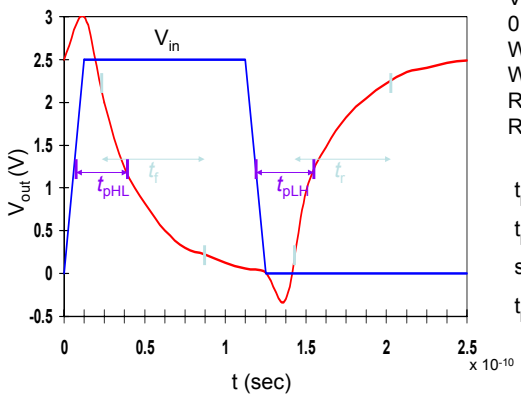
- The dynamic performance of a logic circuit family is characterized by propagation delay of its basic inverter. The propagation delay time is define as the *average of low-to-high propagation delay time and the high-to-low propagation delay time.*
- The propagation delay time is directly proportional to the **switching time** and increases as the Fan-out increases. Therefore, the maximum Fan-out is limited by the maximum acceptable propagation delay time.



Definitions of propagation delays and switching times of the logic inverter.

Each additional load gate increases the load capacitance their must be charge and discharge as the driver gate changes state. This place a practical limit on the maximum allowable number of load gates.

Inverter Transient Response (input step pulse)



V_{DD}=2.5V
0.25µm
W/L_n = 1.5
W/L_p = 4.5
R_{eqn}= 13 kΩ (÷ 1.5)
R_{eqp}= 31 kΩ (÷ 4.5)

t_{pHL} = 36 psec

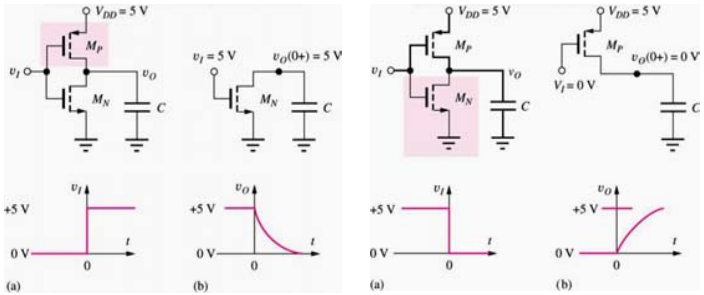
t_{pLH} = 29 psec

so

t_p = 32.5 psec

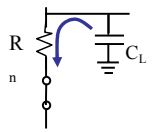
From simulation: t_{pHL} = 39.9 psec and t_{pLH} = 31.7 psec

Propagation Delay Estimate



- The two modes of capacitive charging/discharging that contribute to propagation delay

Switch-level model



Delay estimation using switch-level model (for general RC circuit):

$$I = C\frac{dV}{dt} \quad \rightarrow \quad dt = \frac{C}{I}dV$$

$$I = \frac{V}{R} \quad \rightarrow \quad dt = \frac{RC}{V}dV$$

$$t_1 - t_0 = t_p = \int_{V_0}^{V_1} \frac{RC}{V}dV$$

$$t_p = RC\left[\ln(V_1) - \ln(V_0)\right] = RC\ln\left(\frac{V_1}{V_0}\right)$$

Switch-level model

- For fall delay t_{phl}, $V_0=V_{cc}$, $V_1=V_{cc}/2$

$$t_p = RC\ln\left(\frac{V_1}{V_0}\right) = RC\ln\left(\frac{\frac{1}{2}V_{CC}}{V_{CC}}\right)$$

$$t_p = RC\ln(0.5)$$

$$t_{phl} = 0.69R_nC_L$$

$$t_{plh} = 0.69R_pC_L$$

← Standard RC-delay equations