NON-IDEAL EFFECTS IN MOS.

We discussed the I-V relation of an ideal MOS in three different regimes - Subthreshold, linear & Saturation. Here we will see how non-idealities affect the MOS characteristics. For this we consider the following.

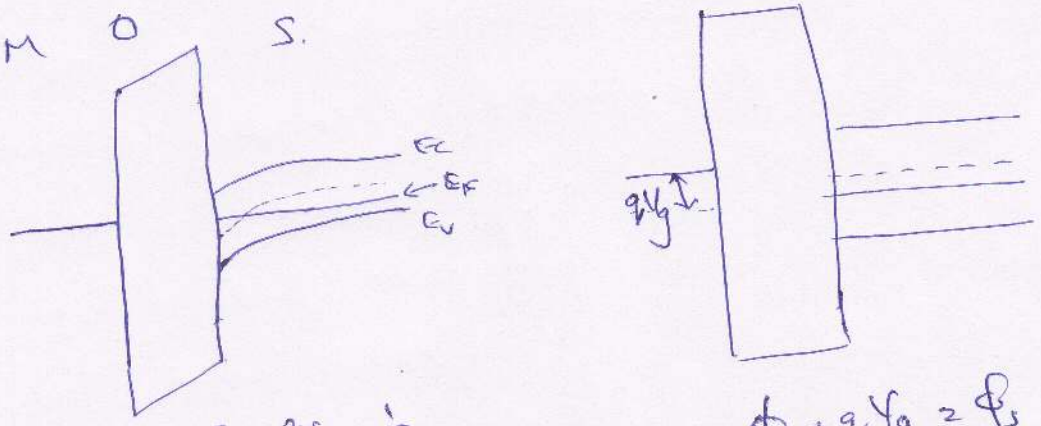
(*) Metal - Semiconductor work function differences
(*) Trapped Charges in the oxide.
(*) Trapped charges at oxide/silicon interface.
(*) Interface states at oxide/silicon interface
(*) Field dependent mobility.
(*) Effect of body bias.
(*) Short channel effects.
(*) Quantum-Effects.
(*) Reliability

For most of the above, an easy way to quantify the effects would be identify how the flat band voltage changes. ~~due to the presence~~ This is a valid approach as the current through a MOS is uniquely dependent on the amount of band-bending (with respect to the substrate & source, as we will discuss later). For similar band bending, if other parameters kept constant, you would get similar currents.

⊛ Metal - Semiconductor Work function difference

$$\phi_{MS} = \phi_M - \phi_S.$$

For an ideal MOS, we assumed $\phi_{MS} = 0$ such that at $V_{gs} = 0$, the semiconductor is in flat band condition. If $\phi_{MS} \neq 0$, then on applying a voltage of $qV_g = +\phi_{MS}$, the semiconductor band bending can be ~~made~~ reduced to zero.



$\phi_M \neq 0$, Equilibrium

$\phi_M + qV_g = \phi_S$ for flat band.

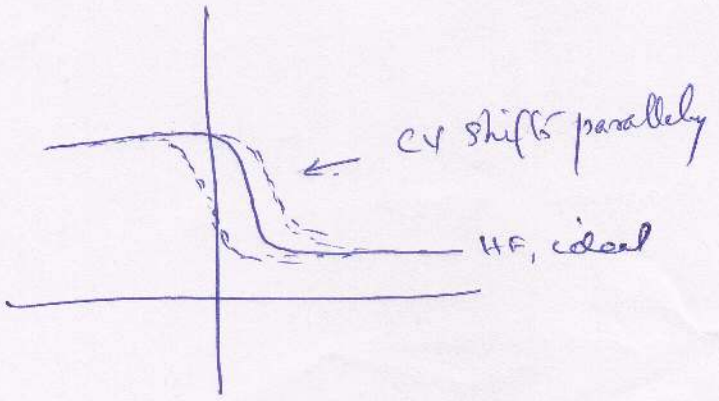
$\Rightarrow V_g = (\phi_M - \phi_S)/q$.

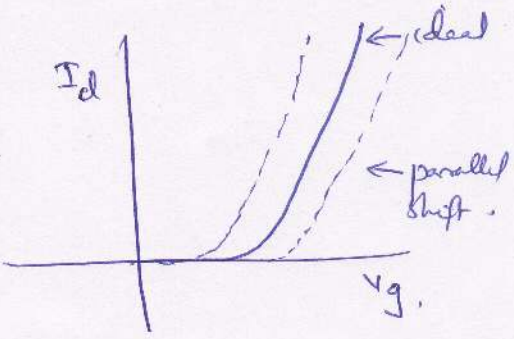
$\Rightarrow$ Due to the above, V_T of a MOS changes by

$$V_{T,new} = V_{T,ideal} + V_{FB}.$$

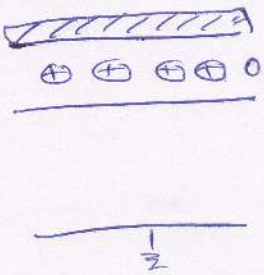
V_{FB} is the flat band voltage, as shown above

The effects on CV & IV are



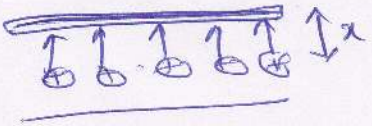


④ Trapped charges in Oxide (Bulk charges).



Bulk charges in oxide can change the flat band condition. For example presence of +ve charges as shown in figure could induce some band bending in Si thus reducing the threshold voltage.

The flat band voltage change can be estimated easily as follows. With an applied voltage, the field lines due to the trapped charges should terminate on the gate metal instead of that in Si. Under such condition the Silicon will be in flat band condition.



The required voltage in such a case would be.

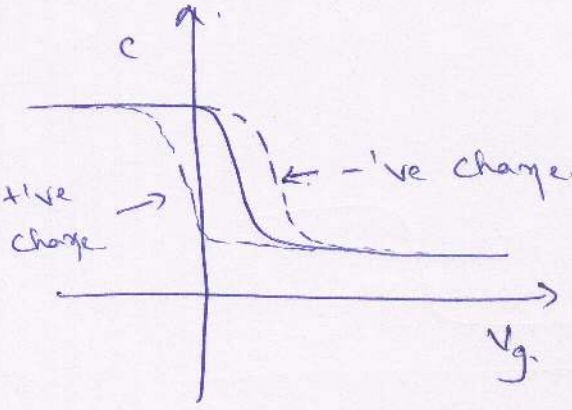
$$\Delta V_g = -\frac{Q_{ox} \times x \cdot dx}{\varepsilon_{ox}\ t_{ox}}$$

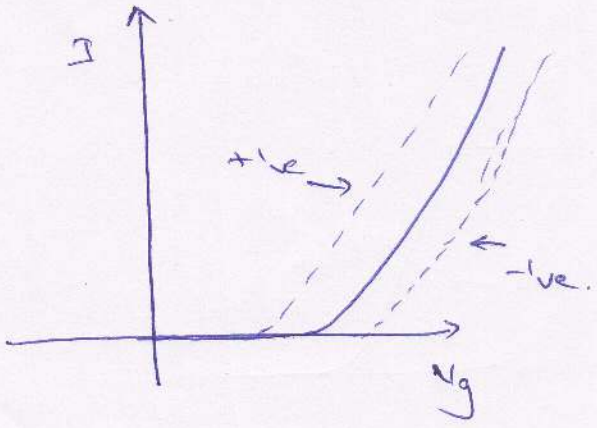
Here the $V_{fb} = -\int_0 \frac{Q_{ox}}{\varepsilon_{ox}} x\, dx.$

Q_{ox} – charge density in C/cm^3.

t_{ox} – oxide thickness

The effect on CV & IV are as shown below.



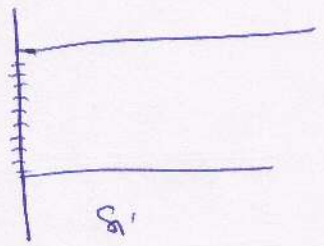


Note that the shift in CV & IV are parallel to the original.

⊛ Trapped charges & interface states at oxide/Si interface.

Trapped charges at oxide/Si. interface act in a similar way as the bulk charges in oxide, as discussed before (except that trapped charges at oxide/Si interface would be like a sheet of charge, instead of a volume density.)

Interface states are more complex. At oxide/Si interface, ~~the~~ all the bonds of Si are not satisfied and hence there are many "dangling" bonds. These result in energetically distributed localized states at Si/ox interface as shown. Accordingly we have



Donor state : +ve charge when empty
zero charge when filled.

Acceptor state : ~~⊛~~ Zero charge when empty
-ve charge when filled.

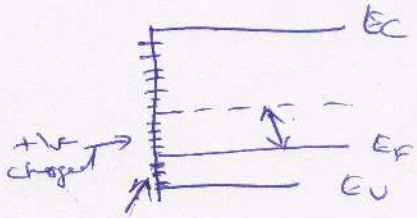
(It is typically assumed that the states closer to Ec are acceptor and those closer to Ev are donor type. [Also supported by experiments].

Note: There is no connection between the above Donor/Acceptor traps to Donor/Acceptor dopants.

It is evident that the flat band condition and the threshold voltage will now depend on the type of traps. Further, the amount of charge on the interface due to these traps would vary with band bending.

Let us assume that we have acceptor type traps (ie from $\frac{E_V + E_C}{2}$ E_C) & donor type traps (E_V to $\frac{E_C + E_V}{2}$) and the density is uniform/constant D_{it} ($\#cm^{-2}/eV$). For a flat band condition in semiconductor, the net interface charge is then given by

$$Q_{IT} = qD_{it} \times (E_F - E_i) = qD_{it}\psi_F$$



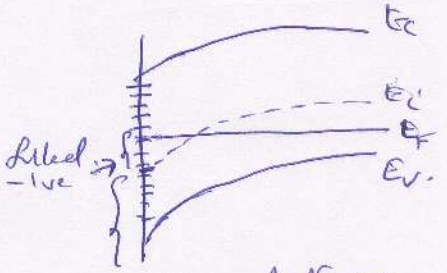
Hence the $V_{FB} = -\frac{Q_{IT} \times t_{ox}}{\varepsilon_{ox}}$ (A)

~~Empty~~ filled and hence zero charge.

At inversion, we have the following scenario.

$$Q_{IT} = -qD_{it}(E_F - E_i)\Big|_{\text{at interface}}$$

$$= -qD_{it}\psi_F$$



All donor states are filled & hence zero charge

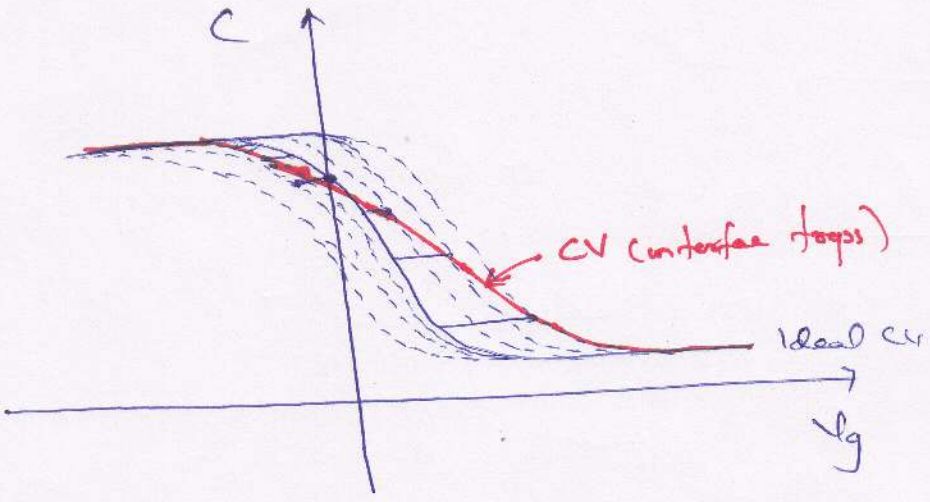
the V_g will have to account for this charge at inversion.

Hence $\Delta V_T = \frac{-Q_{IT}}{C_{ox}}$

$$= \frac{qD_{it}\psi_F}{C_{ox}} \quad (B)$$

From (A) & (B), we have an extended scenario. Once the band bending increases, such that $\psi_s > 2\psi_F$, the net charge on the interface due to traps is -ve (acceptor type ie filled). For $\psi_s < \psi_F$, the net charge is +ve (due to donors).

Further as the bias increases, ($\psi_s > \psi_F$), the net interface charge also increases. Hence the CV will be stretched out in comparison to the ideal CV.



The effect on I-V is two fold. There will be an increase in V_T as discussed before. Further there will be significant changes in the sub-threshold characteristics as well.

We have.

$$V_g = \psi_s + \frac{Q_s + Q_{IT}}{C_{ox}} = \psi_s + \frac{Q_D + Q_{IT}}{C_{ox}}$$

$$V_g = \psi_s + \frac{\sqrt{2\varepsilon_s q N_a \psi_s} + q D_{it} \psi_s}{C_{ox}} \rightarrow (A)$$

$Q_D = \left[2\varepsilon_s q N_a \psi_s\right]^{1/2}$

$Q_{IT} = q D_{it} \psi_s$

$$V_T = 2\psi_F + \frac{\sqrt{2\varepsilon_s q N_a 2\psi_F} + q D_{it} 2\psi_F}{C_{ox}} \rightarrow (B)$$

If we solve of ψ_s from (A) & (B). under the condition $|\psi_s - 2\psi_F| \ll 2\psi_F$, (as done in lectures for the analysis of sub-threshold slope)

$$(V_g - V_t) = m(\psi_s - 2\psi_F).$$

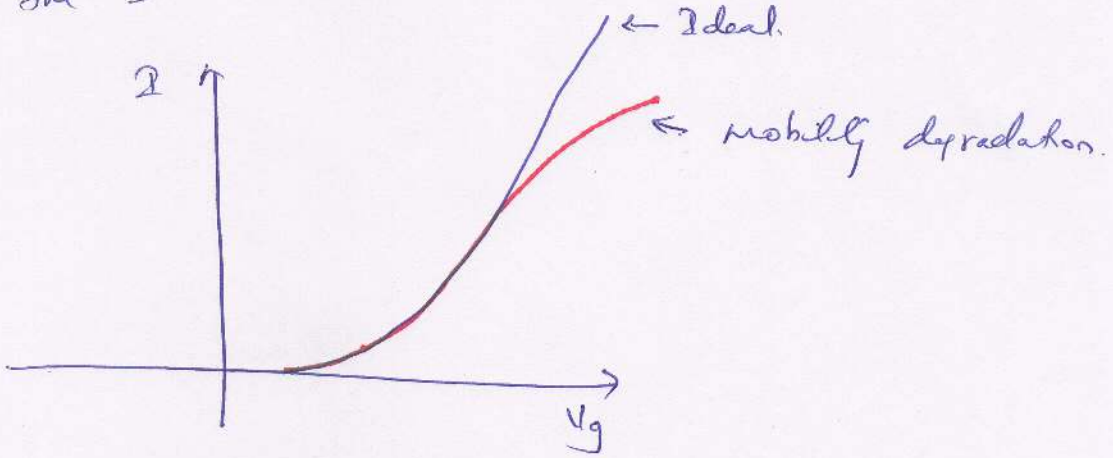
where $m = 1 + \left(\frac{\varepsilon_s N_a}{4\psi_F}\right)^{1/2} \frac{1}{C_{ox}} + \frac{qD_{it}}{C_{ox}}$

Since the sub-threshold current $\propto e^{q\psi_s/kT}$, we find that the sub-threshold slope changes with D_{it}.

Note: The above changes in V_{FB}, V_T, & ψ_B allows one to quantify the D_{it}. (in simple terms) however there are other characterization techniques as well.

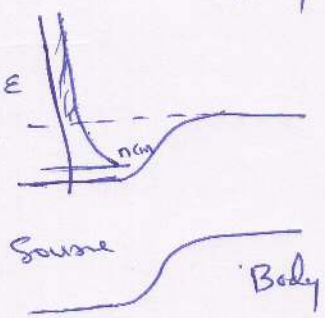
④ Field dependent mobility

We know that $I \propto \mu$ for a MOSFET in both linear & saturation regimes. For large V_G, the inversion layer is pulled closer & closer to the Si/oxide interface. This increases the interaction with the Si/oxide interface and the mobility degrades (due to surface roughness). Hence the I-V deviates from ideal.



⊛ Effect of body bias

In the derivation for ideal MOSFET we assumed that $V_S = V_B = 0$. However in many applications $V_S \neq V_B$ and this reverse bias affects the V_t significantly. In simple terms, for $V_{SB} > 0$ the ~~cha~~ inversion layer in the channel is maintained in steady state condition with the electron supply from source (and drain also, if $V_D > 0$)



If we apply a reverse bias to the S/B junction, the above is disturbed. To maintain the same carrier density in the channel, the channel band ~~bend~~ will have to be increased such that the barrier with the source becomes the same as before i.e if $V_{SB} \neq 0$, then

$$V_{G,\,threshold} = 2\psi_F + V_{SB} + \frac{\sqrt{2\varepsilon_{Si} N_a (2\psi_F + V_{SB})}}{C_{ox}}$$

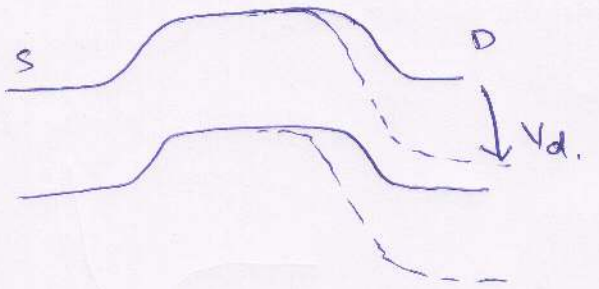
Hence $V_{GS,\,threshold} = V_{GB,\,threshold} - V_{SB}$.

$$= 2\psi_F + \sqrt{2\varepsilon_{Si} N_a (2\psi_F + V_{SB})}/C_{ox}.$$

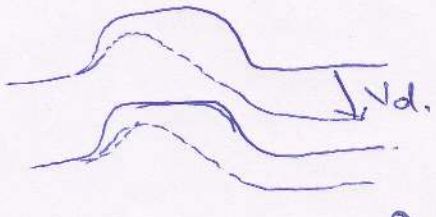
⊛ What happens if you apply -ve V_{SB} or slight forward bias?

⊛ Short channel Effects

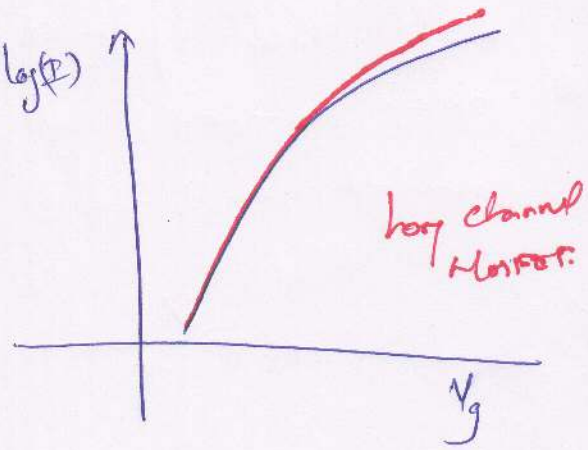
When the channel length becomes shorter, the drain bias can affect the ~~pot~~ source/channel potential barrier. This can affect the V_t and in worn condition could result in punch-through.

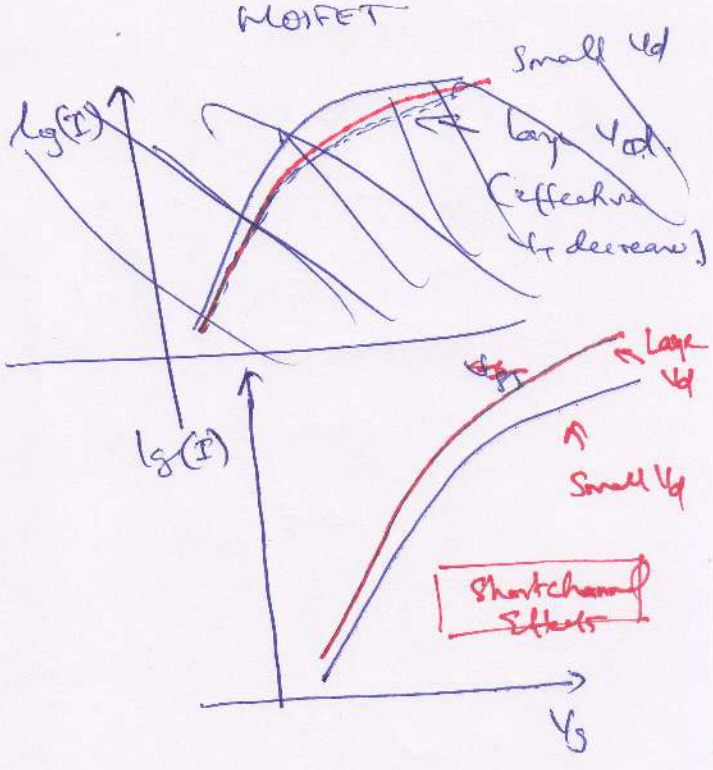


Long channel.



Short channel MOSFET





The above effect is known as Dram Induced barrier lowering. (DIBL).

Quantum Effects

As the gate oxide thickness is made smaller, applied biases result in increasing electric fields and this results in many quantum mechanical effects. A few are.

(1) Tunneling through Oxide. This increases the gate - body leakage current & increases the stand by power loss.

(ii) Band-Band Tunneling : Near the Drain, B-B tunneling can cause significant increase in the leakage current.

(iii). Quantization effects: We so far assumed Boltzmann distribution for electron and thus shows inversion charge peaks at oxide/Si interface. In reality, this is a potential well (almost triangular) and the electron confinement indicates that ψ (the wave function) should go to zero at Si/oxide interface. Accordingly the inversion charge peaks at a distance away from the interface & hence the "Effective or Electrical oxide thickness" is usually modified to account this.

Reliability

As discussed in lecture, interface passivation is an important step in MOSFET fabrication. During continuous operation, there could be generation of interface traps and an increase in oxide charge. Also the oxide could be damaged as well due to energetic electrons / holes. All these lead to time dependent shift in V_T & eventually breakdown of oxide (which could be a catastrophic ~~failure~~).

Historically some such reliability problems were TDDB (or PBTI) (Time dependent dielectric reliability), Negative bias temperature Instability (NBTI), channel Hot carrier injection, etc.

Reliability affects the long term performance of the devices & hence the chips. Thus correspondingly knowledge is required by circuit designers to allow for various "guard bands" such that the performance is not compromised. Hence both the physics, ~~and~~ & time dynamics are important to ~~excite~~ ascertain from a system level perspective.

Tutorial problems

1 ⊛ Two transistors with different metals at gate contact has the same V_T. ($\phi_{m1} = 4.5eV$, $\phi_{m2} = 4.8eV$). with a the doping density of one of them being $N_{B1} = 10^{16} cm^{-3}$ Find the doping density of the other transistor.

t ox and c ox should be given

2 ⊛ For a MOSFET with $t_{ox} = 10nm$, a sheet of charge of $Q_2 = +9 \times 10^{12} cm^{-3}$ is found at a distance of 4nm from metal/gate interface. How can this be compensated by introducing another charge sheet at a distance of 5nm. from oxide/metal interface

Text

3 ⊛ (a) Estimate the Subthreshold slope of a MOSFET with $N_A = 10^{16} cm^{-3}$.

(b). ⊛ If the sub-threshold slope of the above changes by + 30mv/decade, ⊛ estimate the D_{it}?

(c) Assuming uniform density of interface traps within the bandgap (Acceptor above midgap & donor below midgap). find the shift in threshold voltage?

(d) Assuming above, estimate the change in flat band voltage.

⊛ How would the above parameters change if the oxide has a bulk charge density of $Q_{ox} = 2 \times 10^{16} cm^{-3}$)?

(4) During operation, assume that D_{it} increases at a constant rate of 'x' per hour. If the maximum allowable degradation is 10%. Estimate the maximum tolerable 'x' for a device lifetime of 10 years.

(5). After long drain operation, a MOSFET has developed $D_{it} = 10^{12} cm^{+2} eV^{-1}$ over a region of length 1μm near the drain side. If the original length was 5μm, estimate the new I-V characteristics of the device. ($t_{ox} = 3nm$, $N_A = 10^{16} cm^{-3}$)