

## Chapter 16

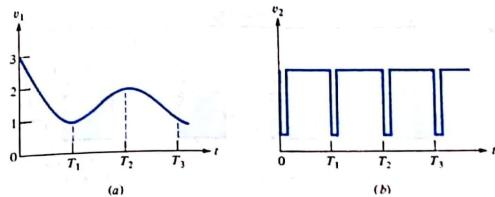
# SIGNAL CONDITIONING AND DATA CONVERSION

**E**lectronic control, communication, computation, and instrumentation systems can be considered to process information contained in the electrical signals present within the system. In previous chapters we indicated that the information exists in the characteristics of the signal waveform. For example, data can be contained by the frequency, phase, amplitude, pulse duration, or presence or absence of a pulse at a specific time. Circuits for generating a variety of these waveforms are treated in Chap. 15. In this chapter we describe a number of circuits used for signal conditioning and data conversion, specifically, circuits which provide appropriate signal characteristics for the particular application. Included are analog-to-digital (A/D) and digital-to-analog (D/A) converters (also referred to as ADCs and DACs, respectively) active-RC filters including switched-capacitor circuits, and a variety of circuits for analog computation.

**SIGNALS AND SIGNAL PROCESSING** Continuous signals and discrete signals are convenient classifications used to describe electrical waveforms. Continuous signals are displayed in Fig. 16-1, and the waveforms shown in Fig. 16-2 are discrete signals. As illustrated in Fig. 16-1, continuous signals are described by continuous time functions which are defined for all values of  $t$ ; that is,  $t$  is a continuous variable. The discrete signals exist only at specific instances of time; their functional description is valid only for the discrete time intervals.

Another feature of the waveforms in Figs. 16-1 and 16-2 can be discerned if we consider the signal in Fig. 16-1a to be a voltage representing a physical quantity. (Perhaps it can be the output voltage of a microphone.) The discrete signal in Fig. 16-2a has the same amplitude at times  $t = 0, T_1, T_2$ , and  $T_3$  as does the continuous signal in Fig. 16-1a. Both voltage waveforms have a one-to-one correspondence in time and amplitude with the physical quantity represented. The waveform in Fig. 16-2a is referred to as a *sampled-data signal*.

FIGURE 16-1  
Two waveforms of continuous signals.



or simply a *sampled signal*. Systems which utilize such signals are called *sampled-data systems*.

In the context of this discussion, the sequence of pulses in each time interval of Fig. 16-2b is a numeric, or digital, representation of the corresponding voltage samples shown in Fig. 16-2a. The waveforms in Fig. 16-1b may be the clock signal which sets the timing sequence used in the generation of the pulses in Fig. 16-2. Neither the amplitude or time of the signals in Figs. 16-1b and 16-2b correspond to the physical quantity  $v_1$ . Essentially, these are signals in which the information is contained by the presence or absence of a pulse during a given time interval.

The waveforms in Figs. 16-1a and 16-2a are analog signals, and those depicted in Figs. 16-1b and 16-2b are digital signals. Both types of signals are often present in modern electronic systems. Clearly, circuits which process these signals and convert one type to the other are required. The following qualitative descriptions help to indicate the several circuit functions that must be performed.

The pictorial representation of a commercial amplitude-modulation radio system is shown in Fig. 16-3. The primary purpose of the system is to transfer the audio information at the transmitting end to the receiving end. The first step in the process is to convert the acoustic energy into an electrical signal. The conversion is effected by a transducer, usually a microphone. As the output of the transducer is a low-level signal, amplification is necessary. Radio-frequency (rf) signals (signals whose frequencies are greater than 500 kHz) are

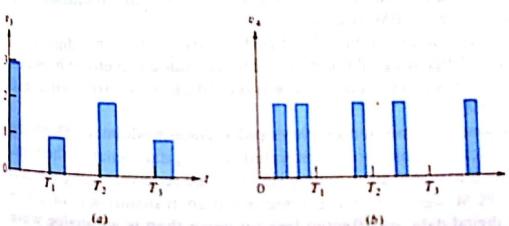
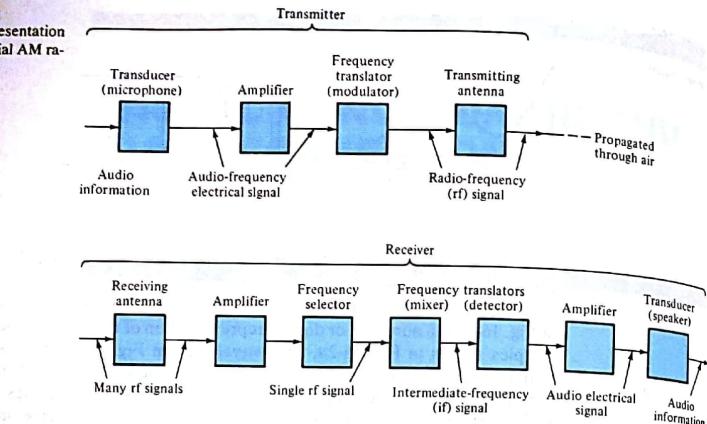


FIGURE 16-2  
Two discrete signals. The waveform in (a) represents pulses whose amplitudes are those in Fig. 16-1a at times (0),  $T_1$ ,  $T_2$ , and  $T_3$ , respectively. The waveform in (b) is the 2-bit binary representation of the amplitudes in (a) at  $T_1$ ,  $T_2$ , and  $T_3$ .



much more readily propagated through the atmosphere than are audio frequencies (20 to 20,000 Hz). Therefore, the audio information is frequency translated to radio frequencies. The frequency translation is achieved by a process called *modulation*.

At the receiver, the process of extracting the information is nearly the reverse of transmission. The received signal is weak and must be amplified. In addition, because many signals (stations) are present at the receiving antenna, the desired signal must be identified and extracted. This function is referred to as *frequency selection*. Practical considerations dictate two frequency translations (demodulation), the mixer and the detector, before the desired audio signal is extracted. The final transducer, usually a loudspeaker, reconverts the electrical signal into the audible acoustic wave.

In an AM system, the audio information is contained in the amplitude of the rf carrier (Fig. 16-4a). Variation of the frequency of the rf wave (Fig. 16-4b) contains the information in a frequency-modulated (FM) system. Voltage-to-frequency and frequency-to-voltage converters are used in the modulation and demodulation processes in FM systems.

If the audio information to be broadcast is the music stored on a digital-disk recording, the stored digital signal is converted to an analog waveform by means of a D/A converter. [Recall that a phonograph record can be considered a read-only memory (ROM).]

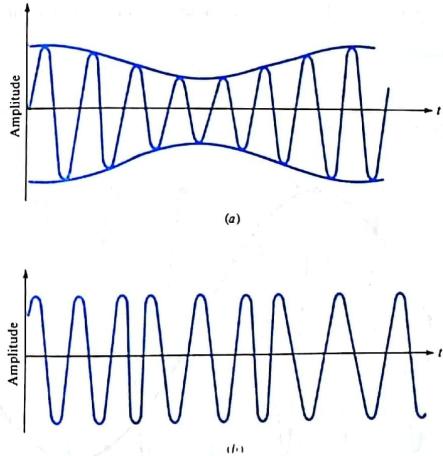
Modern telephone transmission employs pulse-code-modulated (PCM) signals, where the vocal information is converted to a digital signal at the transmitter and then reconstructed as an analog signal at the receiver. Long-distance transmission of PCM signals is more effective than transmission of analog signals because digital data are affected less by noise than is an analog wave-

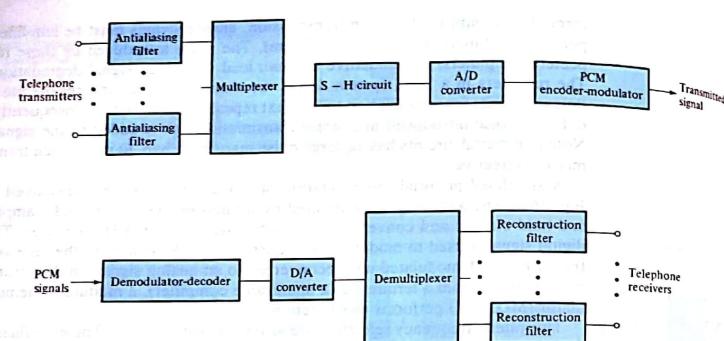
form. To account for losses in transmission, analog signals must be amplified periodically (approximately every 50 km). The noise introduced by these repeaters (amplifiers) is cumulative and can lead to serious signal degradation. The repeaters in a PCM system detect the incoming signal and regenerate a "clean" signal for transmission to the next repeater (or station). Consequently, only the noise introduced in a single transmission link is added to the signal. Note that digital circuits having large noise margins (Chap. 6) make such transmission effective.

A simplified pictorial representation of a telephone system is displayed in Fig. 16-5. The audio signal, generated by a microphone, is sampled (sample-and-hold circuit) and converted to a digital signal by an A/D converter. The digital signal is used to modulate the transmitted PCM signal. At the receiver, the carrier is demodulated and reconverted to an analog signal. In data transmission (e.g., from a terminal to a mainframe computer), a modulator-demodulator (MODEM) performs this function.

Two filters (frequency selection) are also shown in Fig. 16-5. The *antialiasing* filter is used at the transmitter and eliminates ambiguity in the sampled signal. To illustrate the origin of this ambiguity (aliasing), consider two sinusoidal signals  $v_1 = 2 \sin \pi \times 10^3 t$  and  $v_2 = -2 \sin 7\pi \times 10^3 t$  as shown in Fig. 16-6. The frequencies of these signals are 0.5 and 3.5 kHz, respectively. If  $v_1$  and  $v_2$  are sampled at a 4-kHz rate (i.e., once every 0.25 ms), the sampled values are those indicated by the black dots. As seen in Fig. 16-6, both  $v_1$  and  $v_2$  have the same value at these times. Consequently, an ambiguity exists and

**FIGURE 16-4**  
(a) Amplitude-modulated (AM) and (b) frequency-modulated (FM) waveforms.

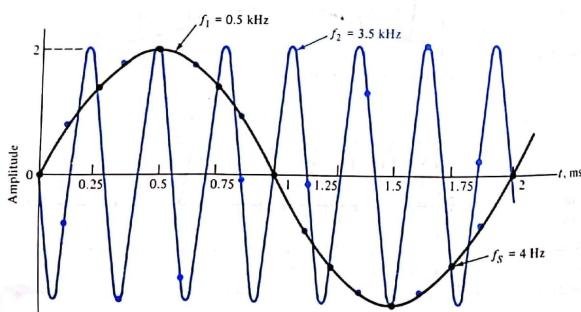




**FIGURE 16-5**  
A pictorial representation of a telephone system. Usually, 24 signals are applied to the multiplexer and a 24:1 demultiplexer is used to separate the different conversations.

renders unique reconstruction of the original signal impossible. If, however,  $v_1$  and  $v_2$  are sampled at an 8-kHz rate (one every 0.125 ms), no ambiguity exists, as indicated by the blue dots. To prevent aliasing, the sampling frequency must be at least twice the highest frequency contained in the analog signal. The purpose of the antialiasing filter is to limit the maximum frequency of the

**FIGURE 16-6**  
Illustration of aliasing. The 0.5-kHz sinusoid (black) and the 3.5-kHz sinusoid (blue) have the same amplitudes if these waves are sampled every 0.25 ms (blue dots) (a 4-kHz sampling frequency). However, sampling every 0.125 ms (an 8-kHz sampling frequency and indicated by blue dots) gives different values for the amplitudes of the two signals.



analog signal to be sampled to one-half the sampling frequency. The reconstruction filter is often required to "smooth" the output waveform of the D/A converter.

The representation in Fig. 16-5 is applicable to many systems which employ digital processing. For example, the input signal may be proportional to the velocity of the conveyor used to transport the wafer carrier in an IC fabrication facility. For utilization of the power of a digital computer (or microprocessor) in the control process, the input signal is sampled and converted to its digital equivalent. The computer operates on this information and provides an output signal (digital) which indicates whether the velocity of the conveyor must be corrected. The digital output is converted to an analog signal which is then amplified (usually) and applied to the drive system. If, in addition, the position of the conveyor is required for control, the velocity signal may be integrated and also converted to a digital signal. Multiplexing allows for the sampling of both the velocity and position (displacement) signals with the same circuitry.

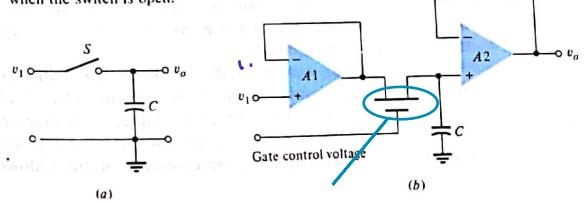
The qualitative descriptions in the previous paragraphs indicate the variety of circuit functions that need to be performed to process signals effectively. The next several sections deal with the interconversion of analog and digital signals. The remainder of the chapter treats a variety of circuits useful in signal conditioning and data acquisition.

**16-2 SAMPLE-AND-HOLD SYSTEMS** A typical data-acquisition system receives signals from a number of different sources and transmits these signals in suitable form to a computer or a communication channel. A multiplexer (Sec. 16-3) selects each signal in sequence, and then the analog information is converted into a constant voltage over the gating-time interval by means of a sample-and-hold system. The constant output of the sample-and-hold circuit may then be converted to a digital signal by means of an analog-to-digital (A/D) converter (Sec. 16-13) for digital transmission.

A sample-and-hold circuit in its simplest form is a switch  $S$  in series with a capacitor, as in Fig. 16-7a. The voltage across the capacitor tracks the input

**FIGURE 16-7**

(a) A simple sample-and-hold circuit. (b) A practical sample-and-hold system. The MOSFET switch replaces the switch  $S$  in (a). The low output resistance of the voltage follower  $A_1$  charges  $C$  quickly when the MOSFET switch is closed. The high input resistance of  $A_2$  maintains the charge on  $C$  when the switch is open.



signal during the time  $T_s$  when a logic control gate closes  $S$  and holds the instantaneous value attained at the end of the interval  $T_s$  when the control gate opens  $S$ . The switch may be a bipolar transistor switch, or a MOSFET controlled by a gating-signal voltage, or a CMOS transmission gate (Fig. 6-32).

The configuration shown in Fig. 16-7b is one of the simplest practical sample-and-hold systems. A positive pulse at the gate of the NMOS will turn the switch ON, and the holding capacitor  $C$  will charge to the instantaneous value of the input voltage with a time constant  $(R_o + r_{DS(ON)})C$ , where  $R_o$  is the very small output resistance of the input Op-Amp voltage follower  $A1$  and  $r_{DS(ON)}$  is the ON resistance of the FET (Sec. 4-2). In the absence of a positive pulse, the switch is turned OFF and the capacitor is isolated from any load through the Op-Amp  $A2$ . Thus it will hold the voltage impressed on it. It is recommended, in discrete-component or hybrid circuits, that a capacitor with polycarbonate, polyethylene, polystyrene, Mylar, or Teflon dielectric be used. Most other capacitors do not retain the stored voltage, as the result of a polarization phenomenon which causes the stored voltage to decay with a time constant of several seconds. In effect, this is the leakage resistance of the capacitor.

Recall that the basic cell in a MOS dynamic RAM (Sec. 9-5) had to be refreshed once every few milliseconds. Since a MOSFET is a capacitor, the decrease in charge in an IC is analogous to that described above. However, if an IC sample and hold is sampled frequently (at least once every few tenths of a millisecond, as is the usual practice), there is little leakage since the time between samples is considerably shorter than the time constant.

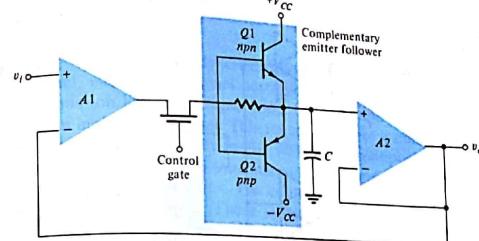
Dielectrics other than those mentioned above also exhibit a phenomenon called dielectric absorption, which causes a capacitor to "remember" a fraction of its previous charge (if there is a change in capacitor voltage). Even if the polarization and absorption effects do not occur, the OFF current of the switch ( $< 1 \text{ nA}$ ) and the bias current of the Op-Amp will flow through  $C$ . Since the maximum input bias current is  $< 1 \text{ nA}$ , it follows that with a  $0.5\text{-}\mu\text{F}$  capacitance the drift rate during the HOLD period will be less than  $2 \text{ mV/s}$ .

Two additional factors influence the operation of the circuit: the aperture time (typically less than  $100 \text{ ns}$ ) is the delay between the time that the pulse is applied to the switch and the actual time the switch closes, and the acquisition time is the time it takes for the capacitor to change from one level of holding voltage to the new value of input voltage after the switch has closed.

When the hold capacitor is larger than  $0.05 \mu\text{F}$ , an isolation resistor of approximately  $10 \text{ k}\Omega$  should be included between the capacitor and the + input of the Op-Amp. This resistor is required to protect the amplifier in case the output is short-circuited or the power supplies are abruptly shut down while the capacitor is charged.

If  $R_o$  and  $r_{DS(ON)}$  were negligibly small, the acquisition time would be limited by the slew rate, that is, by the maximum current  $I$  which the input Op-Amp follower can deliver. The capacitor voltage then changes at a peak rate of  $dv_o/dt = I/C$ . Since the short-circuit current of an Op-Amp is limited (25 mA for the 741 chip), an external complementary emitter follower is used to increase

FIGURE 16-8  
An improved sample-and-hold system. (The complementary emitter follower is discussed in Sec. 14-6.)



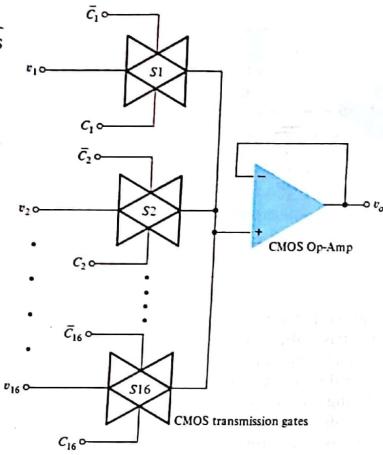
16-3 Analog Multiplexer and Demultiplexer 713

the current available to charge (or discharge)  $C$  extremely rapidly. Such an arrangement is indicated in Fig. 16-8 between the sampling switch and the capacitor. Note that  $A1$  is no longer operated as a follower, but its negative-input terminal now is connected to the output  $v_o$ . This connection ensures that  $v_o = v_i$  during the sample interval. In the hold interval  $v_o$  remains at the value which  $v_i$  attained at the end of the sampling time, except for the very small changes in voltage across  $C$  as a result of the bias current of the output Op-Amp and the leakage current of the switch and emitter follower. The larger the value of the capacitance  $C$ , the smaller is the drift in voltage during the hold mode. However, the smaller the capacitance  $C$ , the smaller is the acquisition time and, hence, the greater the fidelity with which the output follows the input during the sampling mode. Furthermore, the holding capacitor creates an additional pole which one must account for when considering loop transmission and stability. Hence the value of  $C$  must be chosen as a compromise between these three conflicting requirements, depending on the application.

A sample-and-hold (S-H) system is available on a single monolithic chip (e.g., Harris Semiconductor, HA 2420 or National Semiconductor, LF 198), with the storage capacitor added externally. The inverting terminal of  $A1$  is available at an external pin, and hence, this chip may be used to build either a noninverting or an inverting S-H system which exhibits gain, if the usual external resistors are added (Prob. 16-5).

**16-3 ANALOG MULTIPLEXER AND DEMULTIPLEXER** As indicated in Fig. 7-17b, a multiplexer selects one out of  $N$  sources and transmits the (analog) signals to a single transmission line. Of all the switches (mentioned in the preceding section) which are available to feed the input signals to the output channel, the best performance is obtained with the CMOS transmission gate (Fig. 6-32). If dielectric isolation is used in the fabrication of this gate, then typically a leakage current of only  $1 \text{ nA}$  at  $+125^\circ\text{C}$  with a switching time of  $250 \text{ ns}$  is obtainable. Large arrays of such CMOS gates are available for this application.

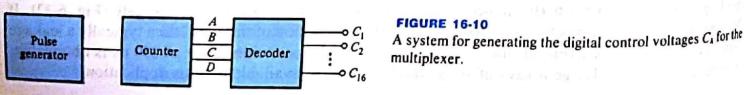
**FIGURE 16-9**  
A 16-input analog multiplexer using CMOS transmission gates.



A block diagram of a 16-input analog commutator is indicated in Fig. 16-9. Time-division multiplexing results if the complementary MOSFET switch  $S_1$  closes (i.e., it is in its low-resistance state) for a time  $T$ , switch  $S_2$  closes for the second interval  $T$ ,  $S_3$  transmits for the third period  $T$ , and so forth. In Fig. 16-9 the symbol  $C_k$  ( $k = 1, 2, \dots, 16$ ) represents the digital control voltage and  $\bar{C}_k$  is its complementary value obtained from an inverter (not shown). If  $C_k$  equals binary 1, the CMOS gate transmits the analog signal  $v_k$  to the output, but if  $C_k$  is binary 0, no transmission is allowed.

The block diagram for obtaining the required digital control voltages for the analog multiplexer in Fig. 16-9 is indicated in Fig. 16-10. The control  $C_k$  is the output of the  $k$ th line of a 4-to-16-line decoder (Sec. 7-6). The four address lines  $A, B, C$ , and  $D$  are the outputs from a binary counter which is excited by a pulse generator. If the time interval between pulses is  $T$ , time-division multiplexing is obtained with the system shown in Figs. 16-10 and 16-9 (cor-

**FIGURE 16-10**  
A system for generating the digital control voltages  $C_k$  for the multiplexer.



responding to parallel-to-serial conversion of the digital data, discussed in Sec. 7-7).

**Analog Demultiplexer** The multiplexer described above has entered the analog data on a single channel, each analog signal occupying its own time slot. At the end of the transmission line, each signal must be separated from the others and placed into an individual channel. This reverse process is called *demodulation* and is represented schematically in Fig. 7-17a. The multiposition switch in this figure is replaced by  $N$  CMOS transmission gates, and the serial data are applied to the input of all these gates. The control signals  $C_k$  are obtained in the manner indicated in Fig. 16-10. These systems for  $C_k$  must be synchronized at the sending and receiving ends of the channel. Such a multiplexer-demultiplexer system saves the size, weight, and cost of  $N - 1$  transmission channels since all the analog signals have been transmitted on a single channel ( $N$  may be as large as several hundred). The National Semiconductor CD4051M is an eight-channel analog multiplexer-demultiplexer.

**16-4 DIGITAL-TO-ANALOG (D/A) CONVERTERS** Many systems accept a digital word as an input signal and translate or convert it to an analog voltage or current. These systems are called *digital-to-analog*, or *D/A converters* (or *DACs*). The digital word is presented in a variety of codes, the most common being pure binary or binary-coded-decimal (BCD).

The output  $V_o$  of an  $N$ -bit D/A converter is given by the following equation:

$$V_o = (2^{N-1}a_{N-1} + 2^{N-2}a_{N-2} + \dots + 2^1a_1 + a_0)V \\ = \left( a_{N-1} + \frac{1}{2}a_{N-2} + \frac{1}{4}a_{N-3} + \dots + \frac{1}{2^{N-2}}a_1 + \frac{1}{2^{N-1}}a_0 \right) 2^{N-1}V \quad (16-1)$$

where  $V$  is a proportionality factor determined by the system parameters and where the coefficients  $a_n$  represent the binary word and  $a_n = 1(0)$  if the  $n$ th bit is 1(0). A stable reference voltage  $V_R$ , from which  $V$  is derived, is used in this circuit. The most-significant bit (MSB) is that corresponding to  $a_{N-1}$ , and its weight is  $2^{N-1}V$ , while the least significant bit (LSB) corresponds to  $a_0$ , and its weight is  $2^0V = V$ .

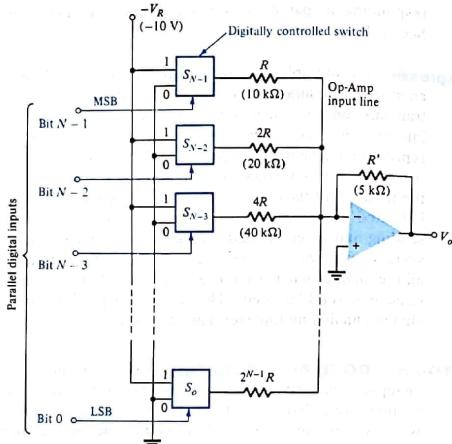
Consider, for example, a 5-bit word ( $N = 5$ ) so that Eq. (16-1) becomes

$$V_o = (16a_4 + 8a_3 + 4a_2 + 2a_1 + a_0)V \quad (16-2)$$

For simplicity, assume  $V = 1$ . Then, if  $a_0 = 1$  and all other  $a$  are zero, we have  $V_o = 1$ . If  $a_1 = 1$  and all other  $a$  values are zero, we obtain  $V_o = 2$ . If  $a_0 = a_1 = 1$  and all other  $a$  values are zero,  $V_o = 2 + 1 = 3$  V, etc. Clearly,  $V_o$  is an analog voltage proportional to the digital input.

A *binary-weighted D/A converter* is indicated schematically in Fig. 16-11. The blocks  $S_0, S_1, S_2, \dots, S_{N-1}$  in Fig. 16-11 are electronic switches which are digitally controlled. For example, when a 1 is present on the MSB line, switch  $S_{N-1}$  connects the resistor  $R$  to the reference voltage  $-V_R$ ; conversely,

**FIGURE 16-11**  
A D/A converter (DAC) with binary-weighted resistors.



when a 0 is present on the MSB line, the switch connects the resistor to the ground line. Thus the switch is a single-pole double-throw (SPDT) electronic switch. The operational amplifier acts as a current-to-voltage converter (Sec. 10-22). We see that if the MSB is 1 and all other bits are 0, the current through the resistor  $R$  is  $-V_R/R$  and the output is  $V_R R'/R$ . Similarly, the output of the LSB (if  $N = 5$ ) becomes  $V_o = V_R R'/16R$ . If all five bits are 1, the output becomes

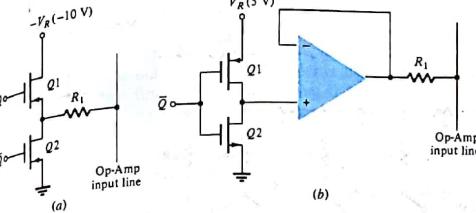
$$V_o = (1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16}) \frac{V_R R'}{R} = (16 + 8 + 4 + 2 + 1) \frac{V_R R'}{16R} \quad (16-3)$$

which agrees with Eq. (16-1) if  $V = V_R R'/16R$ . This argument confirms that the analog voltage  $V_o$  is proportional to the digital input.

Many implementations are possible for the digitally controlled switches shown in Fig. 16-11, two of which are indicated in Fig. 16-12. A totem-pole MOSFET driver in Fig. 16-12a feeds each resistor connected to the Op-Amp input. The two complementary gate inputs  $Q$  and  $\bar{Q}$  come from a MOSFET  $S-R$  FLIP-FLOP or register which holds the digital information to be converted to an analog number. Let us assume that logic 1 corresponds to  $-10\text{ V}$  and logic 0 corresponds to  $0\text{ V}$  (negative logic). A 1 on the bit line sets the FLIP-FLOP at  $Q = 1$  and  $\bar{Q} = 0$ ; and thus transistor  $Q1$  is on, connecting the resistor  $R_1$  to the reference voltage  $-V_R$ , while transistor  $Q2$  is kept off. Similarly, a 0 at the input bit line will connect the resistor to the ground terminal.

An excellent alternative single-pole double-throw electronic switch is that shown in Fig. 16-12b. This configuration consists of a CMOS inverter feeding

**FIGURE 16-12**  
Two implementations of the digitally controlled switch in Fig. 16-10.  
(a) A totem-pole and (b) a CMOS inverter configuration. The resistance  $R_1$  depends on the bit under consideration, thus, for the  $N - 3$  bit in Fig. 16-10,  $R_1 = 4R$ .



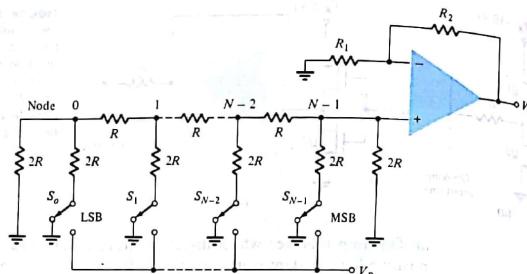
an Op-Amp follower which drives  $R_1$  from a very low output resistance. A positive logic system is indicated with  $V(1) = V_R = +5\text{ V}$  and  $V(0) = 0\text{ V}$ . The complement  $\bar{Q}$  of the bit  $Q = a_n$  under consideration is applied to the input. Hence, if  $a_n = 1$ , then  $\bar{Q}$  of the bit  $Q = a_n$  under consideration is applied to the input. Hence, if  $a_n = 1$ , then  $\bar{Q} = 0$ , the output of the inverter is logic 1, and  $5\text{ V}$  is applied to  $R_1$ . On the other hand, if the  $n$ th is a binary 0,  $\bar{Q} = 1$  and the output of the inverter is 0 V, so that  $R_2$  is connected to ground. This confirms the proper operation of the circuit in Fig. 16-12b as an SPDT switch.

The accuracy and stability of the DAC in Fig. 16-11 depend primarily on the absolute accuracy of the resistors and the tracking of each other with temperature. Since all resistors are different and the largest is  $2^{N-1}R$ , where  $R$  is the smallest resistor, their values become excessively large, and it is very difficult and expensive to obtain stable, precise resistances of such values. For example, for a 12-bit DAC, the largest resistance is  $5.12\text{ M}\Omega$  if the smallest is  $2.5\text{ k}\Omega$ . The voltage drop across such a large resistance due to the bias current would affect the accuracy. Also, practical fabrication of such large resistance values is precluded. On the other hand, if the largest resistance is a reasonable value ( $51.2\text{ k}\Omega$ ), the smallest ( $25\text{ }\Omega$ ) may become comparable to the output resistance of the switch, again affecting the accuracy. Consequently, this type of DAC is seldom used where more than 4 bits are required. The ladder-type converter described in the following avoids these difficulties of extreme resistance values and is frequently used in high-resolution data-conversion systems.

**16-5 Ladder-Type D/A Converter** A circuit utilizing twice the number of resistors in Fig. 16-11 for the same number of bits ( $N$ ) but of values  $R$  and  $2R$  only is shown in Fig. 16-13. The ladder used in this circuit is a current-splitting device, and thus the ratio of the resistors is more critical than their absolute value. We observe from the figure that at any of the ladder nodes the resistance is  $2R$  looking to the left or the right or toward the switch.

For example, to the left of node 0 there is  $2R$  to ground; to the left of node 1 there is the parallel combination of two  $2R$  resistors to ground in series with  $R$ , for a total resistance of  $R + 2R = 2R$ , and so forth. Hence, if any switch, say,  $N - 2$ , is connected to  $V_R$ , the resistance seen by  $V_R$  is  $2R + 2R \parallel 2R = 3R$  and the voltage at node  $N - 2$  is  $(V_R/3R)R = V_R/3$ .

**FIGURE 16-13**  
An  $R - 2R$  ladder D/A converter.



Consider now that MSB is logic 1 so that the voltage at node  $N - 1$  is  $\frac{1}{2}V_R$ , the output is

$$V_o = \frac{V_R}{3} \cdot \frac{R_1 + R_2}{R_1} \equiv V' \quad (16-4)$$

Similarly, when the second MSB bit ( $N - 2$ ) is binary 1 and all other bits are logic 0, the output voltage at node  $N - 2$  is  $V_R/3$ , but at node  $N - 1$  the voltage is half this value, because of the attenuation due to the resistance  $R$  between the nodes and the resistance  $R$  from node  $N - 1$  to ground. Hence  $V_o = \frac{1}{4}V'$  for the second MSB ( $N - 2$ ). In a similar manner (Prob. 16-6) it can be shown that the third MSB gives an output  $\frac{1}{8}V'$ , and so forth. Clearly, the output is of the form of Eq. (16-1) with  $V' = 2^{N-1}V$ .

Because of the stray capacitance from the nodes to ground, there is a propagation delay time from left to right down the ladder network. When switch  $S_0$  closes, the propagation delay is much longer than when the MSB switch closes. Hence, when the digital voltage changes, a transient waveform will appear at the output before  $V_o$  settles down to its proper value. These transients are avoided by using an inverted-ladder DAC (Prob. 16-7).

**Multiplying D/A Converter** A D/A converter which may use a varying analog signal  $V_a$  instead of a fixed reference voltage is called a *multiplying D/A converter*. From Eq. (16-1) we see that the output is the product of the digital word and the analog voltage  $V_a (= 2^{N-1}V)$  and its value depends on the binary word (which represents a number smaller than unity). This arrangement is often referred to as a *programmable attenuator* because the output  $V_o$  is a fraction of the input  $V_a$  and the attenuator setting can be controlled by digital logic. This type of DAC is sometimes used to control the center frequency or bandwidth of a state-variable filter (Sec. 16-11).

The basic DACs described in this section must be augmented by additional circuitry. Such circuitry includes the reference voltage, the Op-Amp, and the

latches and logic circuits needed to input the data. Monolithic systems containing all these circuits are commercially available. The Analog Devices AD558 is an 8-bit bipolar DAC in which the digital circuits are realized in  $I^2L$  technology. The  $R - 2R$  ladder is also used in the AD7541, a 12-bit DAC (which can function as a multiplying D/A converter).

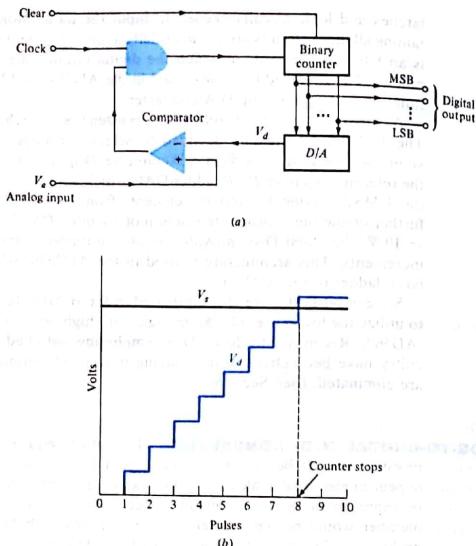
A two-stage segmented architecture is often used to achieve 16-bit resolution. The 4 MSBs are digitally decoded to select a voltage from a resistor chain similar to that used in the flash A/D converter (Fig. 16-16). This voltage becomes the reference  $V_R$  in an  $R - 2R$  ladder DAC which converts the 12 LSBs. In effect, the 4 MSBs divide  $V_R$  into 16 segments from 0 to  $15V_R/16$  V. The 12 LSBs further divide the appropriate fraction of  $V_R$  into 4096 ( $2^{12}$ ) parts. Thus, for  $V_R = 10$  V, the 16-bit DAC provides an analog output from 0 to 10 V in  $153\text{-}\mu\text{V}$  increments. This architecture is used in the AD7546, which incorporates the basic ladder of the AD7541.

Sixteen-bit DACs are also fabricated in the BIMOS technology (Sec. 14-10) to utilize the low power of CMOS logic with high-speed bipolar analog circuits (AD569). Recently introduced D/A employing switched-capacitor CMOS circuitry have been effective in reducing power consumption as most resistors are eliminated. (See Sec. 16-12.)

**16-5 ANALOG-TO-DIGITAL (A/D) CONVERTERS** It is often required that data taken in a physical system be converted into digital form. Such data would normally appear in electrical analog form. For example, a temperature difference would be represented by the output of a thermocouple, the strain of a mechanical member would be represented by the electrical unbalance of a strain-gauge bridge, etc. The need therefore arises for a device that converts analog information into digital form. A very large number of such devices have been invented. We shall consider the four most popular systems: (1) the counting analog-to-digital converter (ADC), (2) the successive-approximation ADC, (3) the parallel-comparator ADC, and (4) the dual-slope or ratiometric ADC.

**The Counting A/D Converter** This system will be explained with reference to Fig. 16-14a. The clear pulse resets the counter to the zero count. The counter then records in binary form the number of pulses from the clock line. The clock is a source of pulses equally spaced in time. Since the number of pulses counted increases linearly with time, the binary word representing this count is used as the input of a D/A converter whose output is the staircase waveform shown in Fig. 16-14b. As long as the analog input  $V_a$  is greater than  $V_d$ , the comparator (which is a high-gain differential amplifier; see Sec. 15-7) has an output which is high and the AND gate is open for the transmission of the clock pulses to the counter. When  $V_d$  exceeds  $V_a$ , the comparator output changes to the low value and the AND gate is disabled. This stops the counting at the time when  $V_a \approx V_d$  and the counter can be read out as the digital word representing the analog input voltage.

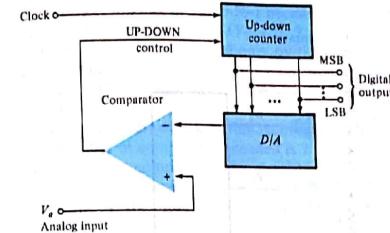
**FIGURE 16-14**  
(a) A counting A/D converter (ADC) and (b) D/A output staircase waveform.



If the analog voltage varies with time, it is not possible to convert the analog data continuously, but it will be necessary that the input signal be sampled at fixed intervals. If the maximum value of the analog voltage is represented by  $n$  pulses and if the period of the clock is  $T$  seconds, the minimum interval between samples (the conversion time) is  $nT$  seconds.

An improved version of the counting ADC, called a *tracking or servo converter*, is obtained by using an up-down counter (Sec. 8-6, Fig. 8-18). This modification of the system of Fig. 16-14a is indicated in Fig. 16-15. Neither a START command (a clear pulse) nor an AND gate is now used. However, an up-down counter is now required and the comparator output feeds the UP-DOWN control of the counter. To understand the operation of the system, assume initially that the output of the DAC is less than the analog input  $V_a$ . Then the positive comparator output causes the counter to read UP. The D/A converter output increases with each clock pulse until it exceeds  $V_a$ . The UP-DOWN control line changes state so that it now counts DOWN (but by only one count, LSB). This causes the control to change to UP and the count to increase by 1 LSB. This process keeps repeating so that the digital output bounces back and forth

**FIGURE 16-15**  
A tracking A/D converter.

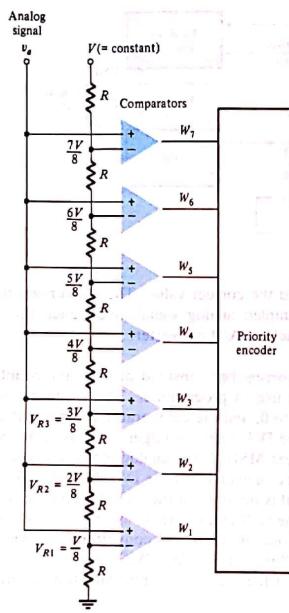


by  $\pm 1$  LSB around the correct value. The conversion time is small for small changes in the sampled analog signal, and hence this system can be used effectively as a tracking A/D converter.

**Successive-Approximation A/D Converter** Instead of a binary counter, as shown in Fig. 16-15, this system uses a programmer. The programmer sets the MSB to 1, with all other bits to 0, and the comparator compares the D/A output with the analog signal. If the D/A output is larger, the 1 is removed from the MSB, and it is tried in the next MSB. If the analog input is larger, the 1 remains in that bit. Thus a 1 is tried in each bit of the D/A decoder until the binary equivalent of the analog signal is obtained at the end of the process. For an  $N$ -bit system, the conversion time is  $N$  clock periods as opposed to a worst case of  $2^N$  pulse intervals for the counting-type A/D converter. The AD7582 (Analog Devices Co.), which is a 28-pin dual-in-line CMOS package, is a 12-bit A/D converter which makes use of the successive-approximation technique.

**The Parallel-Comparator (Flash) A/D Converter** This system is by far the fastest of all converters. Its operation is easily understood if reference is made to the 3-bit A/D converter in Fig. 16-16. The analog voltage  $v_a$  is applied simultaneously to a bank of comparators with equally spaced thresholds (reference voltages  $V_{R1} = V/8$ ,  $V_{R2} = 2V/8$ , etc.). This type of processing is called *bin conversion*, because the analog input is sorted into a given voltage range or "voltage bin" determined by the thresholds to two adjacent comparators. Note that the comparator outputs  $W$  take on a very distinctive pattern: low output (logic 0) for all comparators with thresholds above the input voltage and high output (logic 1) for each comparator whose threshold is below the analog input. For example, if  $\frac{1}{2}V < v_a < \frac{3}{8}V$ , then  $W_1 = 1$ ,  $W_2 = 1$ , and all other  $W$  values are 0. For this situation the digital output should be 2 ( $Y_0 = 0$ ,  $Y_1 = 1$ ,  $Y_0 = 0$ ), which is interpreted to mean an input analog voltage between  $\frac{1}{2}V$  and  $\frac{3}{8}V$ .

The truth table with inputs  $W$  and outputs  $Y$  is given in Table 16-1. A comparison with Table 7-3 shows that the logic is that of a 3-bit priority encoder. The  $X$  values in Table 7-3 are all replaced by 1s. The column labeled  $W_0$  in



**FIGURE 16-16**  
A 3-bit parallel-comparator (flash) A/D converter.

**TABLE 16-1** Truth Table for the A/D Converter in Fig. 16-15

Inputs							Outputs		
W <sub>7</sub>	W <sub>6</sub>	W <sub>5</sub>	W <sub>4</sub>	W <sub>3</sub>	W <sub>2</sub>	W <sub>1</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

Table 7-3 is missing in Table 16-1 because, if  $v_a < \frac{1}{8}V$  then  $W_1$  through  $W_7$  are all 0, and the output is zero ( $Y_2 = 0, Y_1 = 0, Y_0 = 0$ ).

Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a TI147 priority-encoder conversion, delays of the order of 20 ns can be obtained.

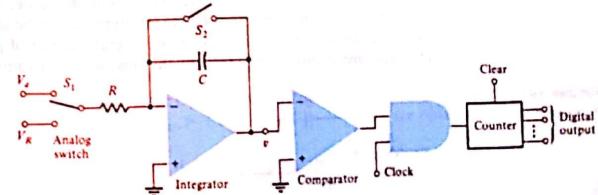
An obvious drawback of this technique is the complexity of the hardware. The number of comparators needed is  $2^N - 1$ , where  $N$  is the desired number of bits (seven comparators for the 3-bit converter in Fig. 16-16). Hence the number of comparators approximately doubles for each added bit. Also the larger the  $N$ , the more complex is the priority encoder.

**Dual-Slope or Ratiometric A/D Converter** This widely used system is depicted in Fig. 16-17. Consider unipolar operation with  $V_a > 0$  and  $V_R < 0$ . Initially  $S_1$  is open,  $S_2$  is closed, and the counter is cleared. Then at  $t = t_1$ ,  $S_1$  connects  $V_a$  to the integrator and  $S_2$  opens. The sampled (and hence constant) analog voltage  $V_a$  is now integrated for a fixed number  $n_1$  of clock pulses. If the clock period is  $T$ , the integration takes place for a definite known time  $T_1 = n_1 T$ , and the waveform  $v$  at the output of the integrator (Sec. 16-7) is indicated in Fig. 16-18.

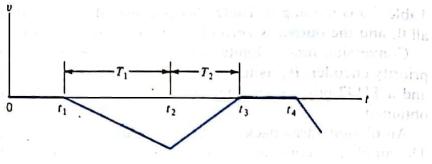
If an  $N$ -stage ripple counter is used and if  $n_1 = 2^N$ , then at time  $t_2$  (the end of the integration of  $V_a$ ) all FLIP-FLOPS in the counter read 0. This is clearly indicated in the waveform chart of Fig. 8-19 for a four-stage ripple counter where, after  $n_1 = 2^4 = 16$  counts,  $Q_0 = 0, Q_1 = 0, Q_2 = 0$ , and  $Q_3 = 0$ . In other words, the counter automatically resets itself to zero at the end of the interval  $T_1$ . Note also from Fig. 8-14 that at the 2<sup>nd</sup> pulse, the state of  $Q_{N-1}$  (MSB), changes from 1 to 0 for the first time. This change of state can be used as the control signal for the analog switch or transmission gate (Fig. 6-32).

Because of the counter operation described in the preceding paragraph, the reference voltage  $V_R$  is automatically connected to the input of the integrator at  $t = t_2$ , at which time the counter reads zero. Since  $V_R$  is negative, the waveform  $v$  has the positive slope shown in Fig. 16-18. We have assumed that  $|V_R| > V_a$ , so that the integration time  $T_2$  is less than  $T_1$ , as indicated. As

**FIGURE 16-17**  
Schematic representation of a dual-slope ADC.



**FIGURE 16-18**  
The output waveform of the integrator shown in Fig. 16-17.



long as  $v$  is negative, the output of the comparator is positive and the AND gate allows clock pulses to be counted. When  $v$  falls to zero, at  $t = t_3$ , the AND gate is inhibited and no further clock pulses enter the counter.

We now show that the reading of the counter at time  $t_3$  is proportional to the analog input voltage. The value of  $v$  at  $t_3$  is given by

$$v = -\frac{1}{RC} \int_{t_1}^{t_2} V_a dt - \frac{1}{RC} \int_{t_2}^{t_3} V_R dt = 0$$

With  $V_a$  and  $V_R$  constant,

$$V_a(t_2 - t_1) + V_R(t_3 - t_2) = 0 \quad \text{or} \quad V_a = |V_R|T_2/T_1$$

If the number of pulses accumulated in the interval  $T_2$  is  $n_2$ , then  $T_2 = n_2 T$ . Since  $T_1 = n_1 T = 2^N T$ , then

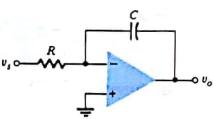
$$V_a = \frac{T_2 |V_R|}{T_1} = \frac{n_2 |V_R|}{n_1} = n_2 \frac{|V_R|}{2^N}$$
 (16-5)

Since  $|V_R|$  and  $N$  are constant, we have verified that  $V_a$  is proportional to the counter reading  $n_2$ . Note that this result is independent of the time constant  $RC$ .

The system includes automatic logic sequencing (not shown in Fig. 16-17), which clears the counter between  $t_3$  and  $t_4$ , takes a new sample of the analog voltage, and moves  $S_1$  back to  $V_a$  at  $t_4$ , so that the process is repeated; thus a new reading of  $V_a$  is obtained each  $t_3 = t_1 + T_1 + T_2$  seconds. This technique can be very accurate; six-digit digital voltmeters employ such signal processing. The counter feeds a decoder/lamp driver so that the output is visible. For each cycle of operation a new voltage reading is obtained.

The dual-slope system is inherently noise-immune because of input-signal integration, i.e., the ubiquitous 60-Hz interference can be all but eliminated by choosing the integration time to be an integral number of power line periods. This statement also brings to light the obvious disadvantage of the system.

**FIGURE 16-19**  
A Miller integrator.



namely, the conversion time is long since  $\Delta s \approx 16$  ms. Such a dual-slope A/D converter can be obtained in various degrees of user complexity. The Datel Intersil ICL7109 is a monolithic 12-bit dual-slope A/D with microprocessor compatibility.

**16-6 INTEGRATOR AND DIFFERENTIATOR CIRCUITS** The analog integrator is very useful in many signal-processing applications. The ideal integrator, introduced in Sec. 10-22 and repeated for convenience in Fig. 16-19, employs an ideal Op-Amp. Several waveform generation circuits which incorporated the circuit shown in Fig. 16-19 were described in Chap. 15. Our objective in this section is to treat practical integrator circuits in which the nonideal behavior of the Op-Amp is included.

**DC Offset and Bias Current** The input stage of the Op-Amp used in Fig. 16-19 is usually a differential amplifier. The dc input offset voltage  $V_{io}$  appears across the amplifier input, and this voltage will be integrated and will appear at the output as a linearly increasing voltage. The input bias current will also flow through the feedback capacitor, charging it and producing an additional linearly increasing component of the output voltage. These two effects (error sources) cause a continually increasing output until the amplifier reaches its saturation point. We see then that a limit is set on the feasible integration time by the above error components. The effect of the bias current can be minimized by increasing the feedback capacitor  $C$  while simultaneously decreasing the value of  $R$  for a given value of the time constant  $RC$ .

**Finite Gain and Bandwidth** The integrator supplies an output voltage proportional to the integral of the input voltage, provided the operational amplifier shown in Fig. 16-19 has infinite gain  $|A_e| \rightarrow \infty$  and infinite bandwidth. The voltage gain as a function of the complex variable  $s$  is, upon transforming Eq. (10-117),

$$A_e(s) = \frac{V_o(s)}{V_i(s)} = -\frac{Z_2'}{Z_1} = -\frac{1}{RCs} \quad (16-6)$$

and it is clear that the ideal integrator has a pole at the origin.

Let us assume that in the absence of  $C$  the Op-Amp has a dominant pole at  $f_1$ , or  $s_1 = -2\pi f_1$ . Hence its voltage gain  $A_e$  is approximated by

$$A_e = \frac{A_{eo}}{1 + j(f/f_1)} = \frac{A_{eo}}{1 - s/s_1} \quad (16-7)$$

If we assume that the Op-Amp output resistance  $R_o = 0$  and the input resistance  $R_i \rightarrow \infty$ , then, for  $A_{eo} \gg 1$  and  $A_{eo} RC \gg 1/|s_1|$ , we obtain

$$A_e(s) = \frac{-A_{eo}}{(1 + s/A_{eo}|s_1|)(1 + sRC)} \quad (16-8)$$

where  $A_{eo}$  is the low-frequency voltage gain of the Op-Amp.