PMOS I/V Characteristics and Effect of Body Bias

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The Problem Statement

In this experiment, we will do the following:

* Measure the I_D v/s V_{DS} characteristics of a PMOS transistor
* Investigate the effect of body bias on its characteristics

Background Information and Conventions

We have characterized a NMOS transistor in the last week. Today we will work with a PMOS transistor. The working of a PMOS transistor is same as that of a NMOS, only the voltage polarities are opposite.

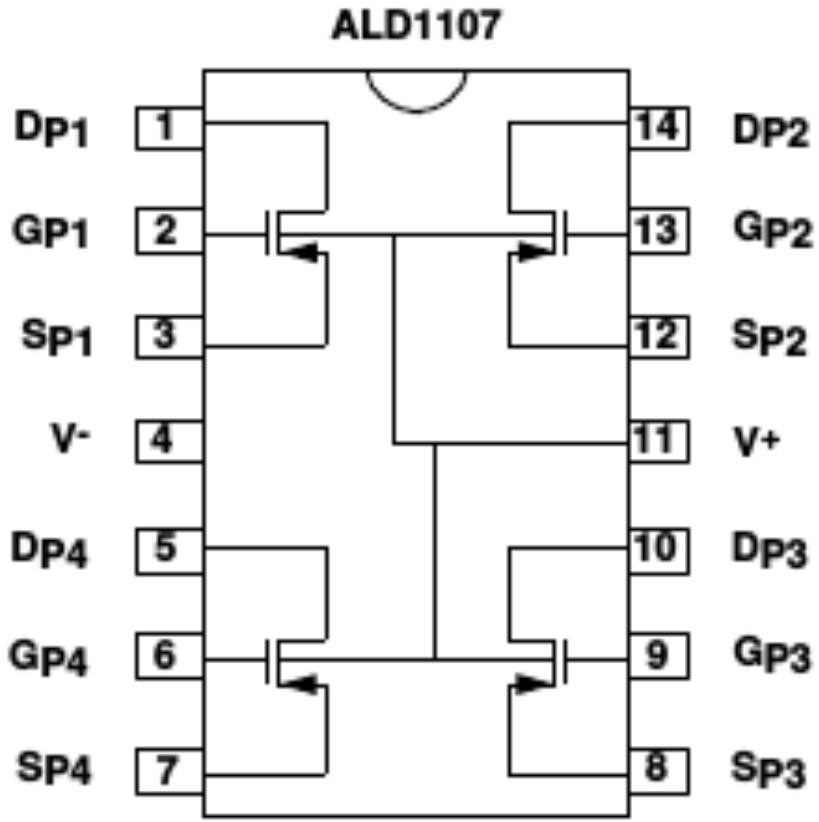
Note that the threshold voltage V_t for a PMOS is negative, i.e., $V_t < 0$.

For the transistor to be ON, the applied gate voltage must be **less** than the threshold voltage, i.e., $V_G < V_t$. The definitions for the operating regions of a PMOS is exactly the opposite of that of the NMOS, i.e.

$$\begin{aligned} V_{GS} - V_t &< V_{DS} \qquad \text{(Linear Region)} \\ V_{GS} - V_t &> V_{DS} \qquad \text{(Saturation Region)} \end{aligned} \tag{1}$$

ALD1107 Pin diagram

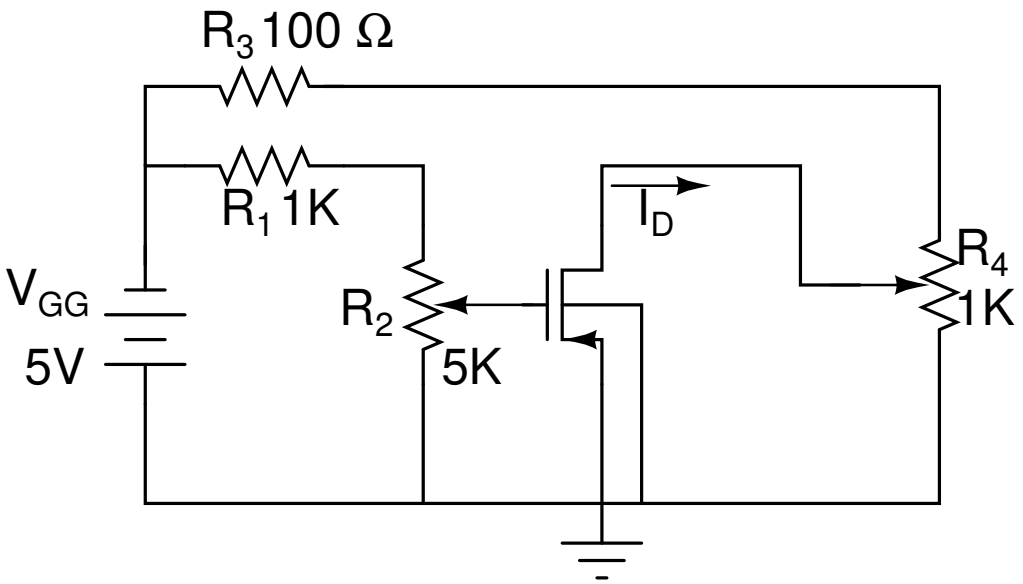
Pin diagram:



Note: The body terminal of all the transistors are connected together and brought out on pin 11.

Part 1- I_D-V_{DS} Characteristics

In this part, we investigate the $I_D - V_{DS}$ characteristics for a constant value of V_{GS}.



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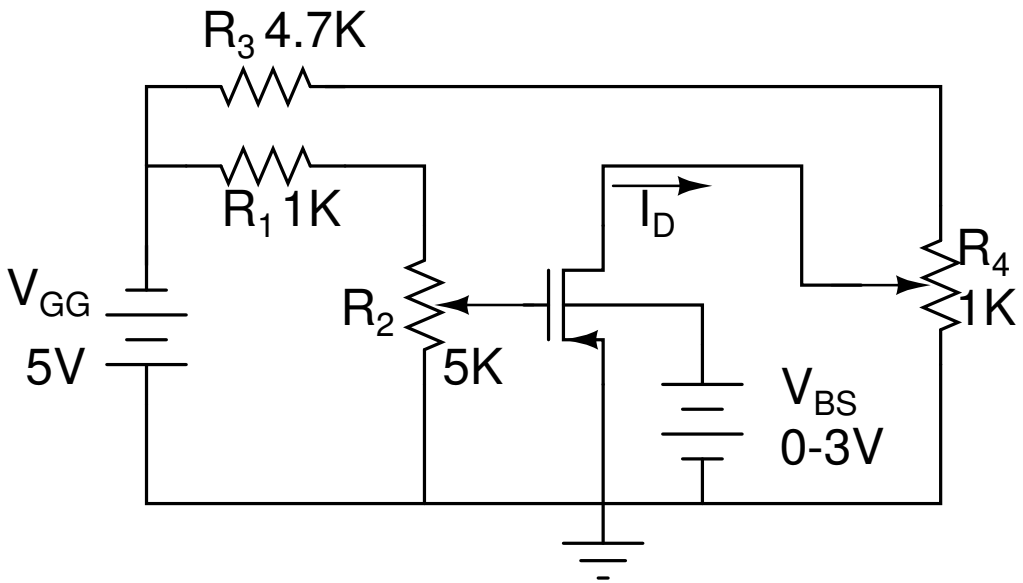
1. Make the connections as shown in the above circuit diagram. 6
2. Adjust V_{GS} = -1.5 V and monitor it to ensure it stays constant.
3. Vary V_{DS} in small steps from 0 to -5 V and note the corresponding value of I_D.
4. Repeat steps 2-3 for V_{GS} = -2, -2.5 and -3 V to get different sets of (I_D, V_{DS}) values. Do not dismantle the circuit. We will use the same circuit with slight modifications for the next part.

Part 2- I_D-V_{GS} Characteristics for different values of V_{BS}

In this part, we will investigate the effect of body bias on the I_D v/s V_{GS} characteristics.



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1. The circuit to be used is shown in the figure above. Replace R_3 by a 4.7 KΩ resistor.
2. Set V_{BS} to 0 V and V_{DS} around 200mV to be kept constant for all the subsequent steps.
3. Vary V_{GS} in small steps from 0 to -4 V and note the corresponding value of I_D.
4. Repeat Step 3 for $V_{BS} = 1$, 2 and 3 V to get different sets of (I_D, V_{GS}).

Obtaining Results and Interpreting Them

Part 1:

Draw an I_D v/s V_{DS} plot for different values of V_{GS}. Calculate the Drain-Source resistance and the Early voltage. Is the early voltage same for both PMOS and NMOS? Why?

You have already done the NMOS experiment, hence this part of the analysis is identical. Refer the previous lab sheet in case of any confusion.

Obtaining Results and Interpreting Them (cont'd...)

Part 2:

1. Plot I_D-V_{GS} characteristic for each value of body bias V_{BS}.
2. Obtain threshold voltage for each value of V_{BS}.
3. Plot V_t v/s V_{SB} (V_{SB} = -V_{BS}). You should get four points.
4. Obtain body effect coefficient α from V_t v/s V_{SB} plot.