MOSFET I/V Characteristics and Device Parameters

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18 July 2014

Background Information

* The MOSFET is one of the most commonly used transistors.
* It has four terminals- Gate (G), Drain (D), Source (S) and Body (B).
* The device working principle is that the voltage applied between its gate and source terminal controls the current through the source and drain terminals.
* The body terminal of an NMOS is connected to the **lowest potential** while that of a PMOS is connected to the **highest voltage** in the circuit, i.e. V_{DD}.

$$\begin{aligned} I_D &= \frac{k}{2}(2(V_{GS}-V_T)V_{DS}-V_{DS}^2) \quad V_{GS}-V_T > V_{DS} \text{ (linear region)} \\ I_D &= \frac{k}{2}(V_{GS}-V_T)^2 \quad V_{GS}-V_T < V_{DS} \text{ (saturation region)} \end{aligned} \tag{1}$$

Background Information (cont'd...)

Q: Why do we care about the potential at Body terminal?

A:

1. **Souce-Body leakage current:**
   Source-Body and Drain-Body junctions of a MOSFET can be visualised as two PN junctions. Since no current is expected to flow through these junctions, we need to reverse bias them. Connecting the Body of the PMOS to the highest potential and that of the NMOS to the lowest potential serves this purpose.

2. **Drift in threshold voltage**
   The voltage applied to the Body terminal will influence the flow of minority carriers which are responsible for the channel formation and hence can change the threshold voltage.

Background Information (cont'd...)

Some information and conventions which we use:

* The threshold voltage (V_{TN}) of an NMOS is positive, while that of a PMOS (V_{TP}), is negative.
* The parameter k in eq. (1) is k_n and k_p for NMOS and PMOS respectively, and is given as

$$k = \mu C_{ox} \left(\frac{W}{L} \right) \tag{2}$$

Where;
μ- mobility of charge carriers (electrons/holes) in the channel of the MOSFET.

C_{ox}- per unit area capacitance between the gate and body.

W, L- width and length of the channel respectively.

The Problem Statement

In this experiment, we will do the following for an NMOS transistor:

* Determine the threshold voltage V_{TN}
* Obtain the output DC characteristics I_D v/s V_{DS}
* Obtain the I_D v/s V_{GS} characteristics in the saturation region
* Determine the small signal transconductance g_m

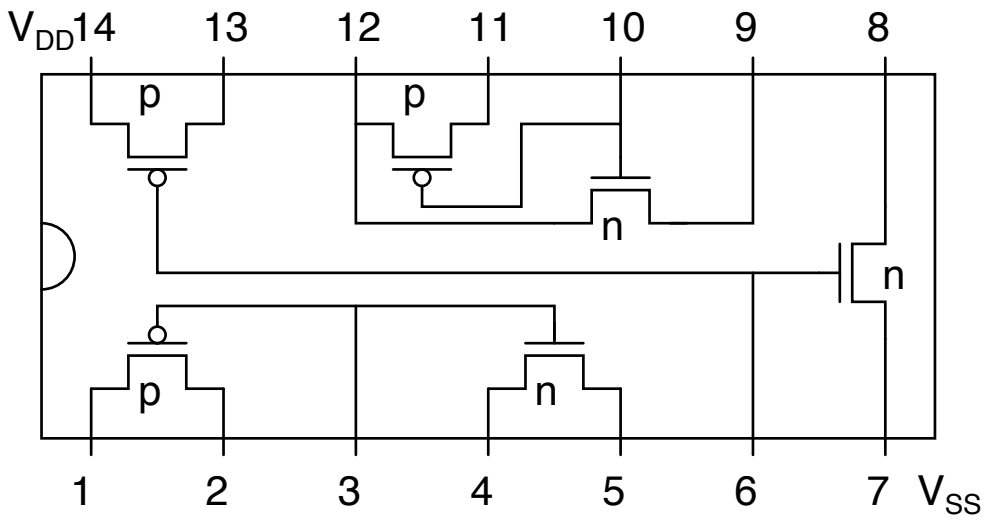
What You Will Need

Before starting the experiment, ensure that you have

* CD4007 MOSFET IC
* 5.6 V Zener diode
* Resistors- 680 Ω, 100 Ω, 5 kΩ pot, etc.
* Capacitor- 10 μF
* Multimeters (three), a function generator, a DC power supply, oscilloscope
* Breadboard and connecting wires (but of course!)

Some Information about CD4007

Pin diagram:



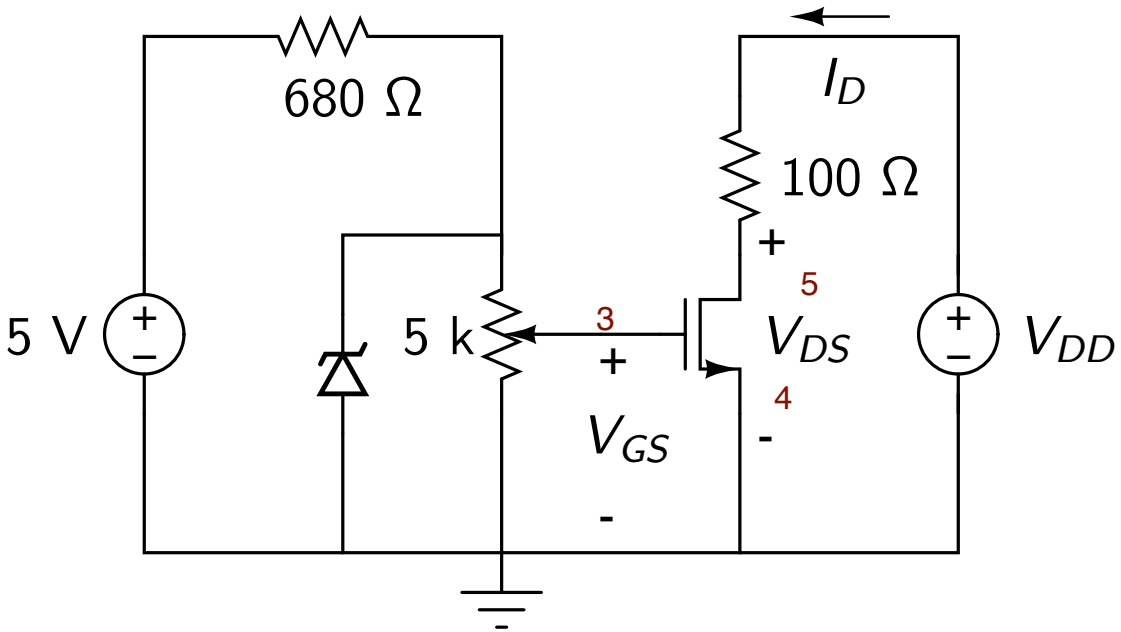
* The body terminals of all the NMOS transistors are connected together and brought out on pin 7. **Therefore, always connect pin 7 to the lowest potential.**

* The body terminal of all the PMOS transistors are connected together and brought out on pin 14. **Therefore, always connect pin 14 to the highest DC voltage in your circuit.**

Part 1- Threshold Voltage of NMOS

The threshold voltage can be easily found by biasing the NMOS in linear region and varying V_{GS} in small steps and correspondingly noting the linear change in I_D.

We use the circuit shown below. The zener diode is used to prevent gate voltages from going above 5.6 V which may cause the device oxide to break down.



Part 1- Threshold Voltage of NMOS (cont'd...)

Procedure:

1. Wire up the above circuit. Adjust V_{DD} such that $V_{DS} \approx 200$ mV. **Keep monitoring V_{DS} throughout this part- it should be kept constant at 200 mV.**

2. Vary V_{GS} by means of the 5 k pot and note the corresponding value of I_D. Take (I_D, V_{GS}) readings till $V_{GS} = 5$ V.

3. **Do not dismantle this circuit**- you will be using it for Part 2 as well.

Part 2- I_D-V_{DS} Characteristics

In this part, we investigate the $I_D - V_{DS}$ characteristics for a constant value of V_{GS}.

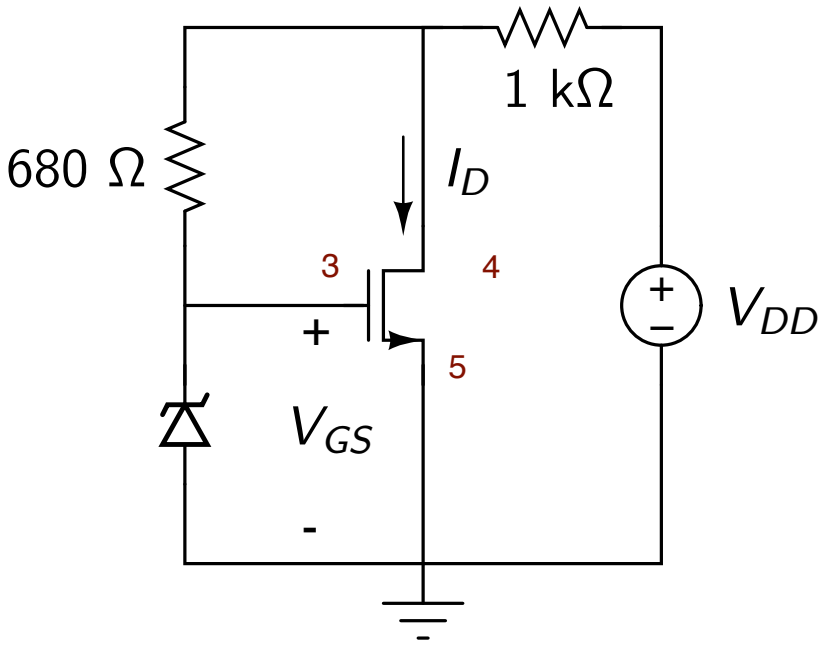
1. The circuit to be used is the same as in Part 1.
2. Adjust $V_{GS} = 2.5$ V and monitor it to ensure it stays constant.
3. Vary V_{DS} in small steps from 0 to 5 V and note the corresponding value of I_D.
4. Repeat Steps 1-3 for $V_{GS} = 3$V and 3.5 V to get different sets of (I_D, V_{DS}) values.

Part 3- I_D v/s V_{GS} Characteristics in Saturation

In this part, we look at the $I_D - V_{GS}$ relationship for an NMOS in the saturation region.

1. Wire up the circuit shown below. The circuit is designed to make $V_{GS} < V_{DS}$. This ensures that $V_{DS} > V_{GS} - V_{TN}$ i.e. the transistor always remains in saturation.

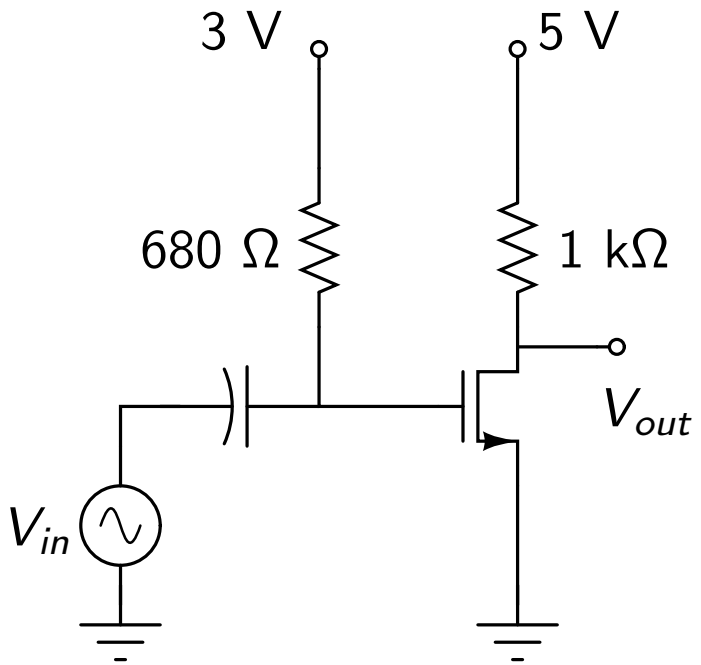
2. Now vary V_{GS} by varying V_{DD} in small steps from 0 to 5 V. Note down the corresponding values of I_D.



Part 4- Small Signal Transconductance

Here, we will determine the small signal transconductance g_m of the NMOS.

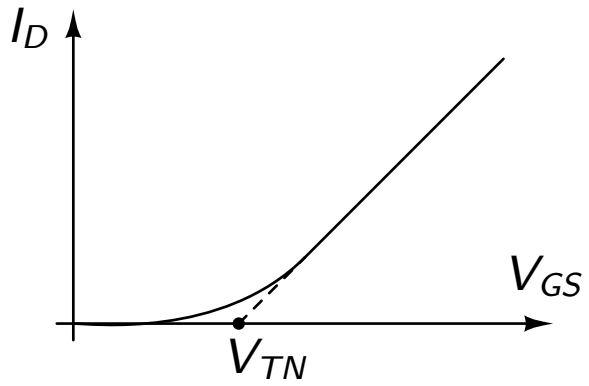
1. Wire up the circuit shown below.
2. Bias the NMOS in saturation with $V_{GS} = 2$ V and $V_{DS} = 5$ V (you need not have these exact values of V_{GS} and V_{DS}, but V_{GS} should be below V_{DS}).
3. Now apply a sine wave (50 mV peak, 1 kHz) at the input and find out the voltage gain ratio $A_v = V_{out}/V_{in}$.



Obtaining Results and Interpreting Them

From the I_D-V_{GS} data in Part 1:

1. Plot a graph of I_D v/s V_{GS} on a linear scale.
2. Extrapolate the linear portion of the plot as shown below to find the intercept on the V_{GS} axis. This will give you the threshold voltage V_{TN}.



3. Also compute the transconductance $g_m = \partial I_D / \partial V_{GS}$. At what value of V_{GS} is the g_m maximum?
4. Calculate the linear region resistance r_o and plot it as a function of $V_{GS} - V_{TN}$.
5. Calculate the subthreshold slope (below V_{TN}) $SS = (\partial \ln I_D / \partial V_{GS})^{-1}$ in units mV/decade.

Obtaining Results and Interpreting Them (cont'd...)

Q: Why do we need to extrapolate to get V_{TN}?

A: Recall that in the experiment, we are increasing V_{GS} from 0 to 5 V while keeping V_{DS} fixed at 0.2 V. For small values of V_{GS}, the $V_{GS} - V_{TN}$ difference is below V_{DS}. For this small region, the transistor is actually in saturation, while we expect it to be in linear region! Hence I_D varies non-linearly with V_{GS} for a small range of V_{GS}, after which it changes linearly.

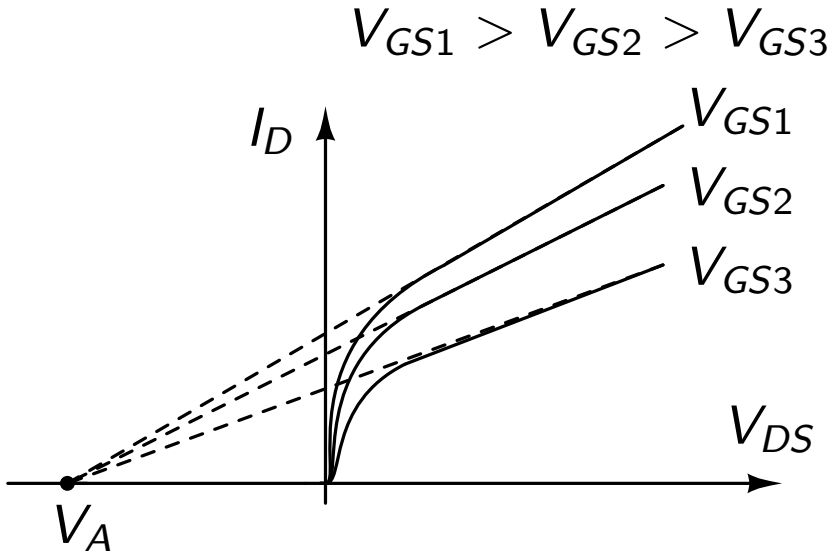
Obtaining Results and Interpreting Them (cont'd...)

From the I_D-V_{DS} data in Part 2:

1. Plot a graph of I_D v/s V_{DS} on a linear scale. For each value of V_{GS}, you have one set of I_D-V_{DS} data. Plot all of these on the same graph, as shown below.
2. From the slope of the linear portion of the graph, calculate the output drain-source resistance r_o at $V_{DS} = 5$ V for different values of V_{GS} as

$$\text{slope} = \frac{1}{r_o} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}} \tag{3}$$

3. Extrapolate the linear portion of the graph to find the intercept on the V_{DS} axis. This will give you the Early Voltage V_A.



Obtaining Results and Interpreting Them (cont'd...)

From the I_D-V_{GS} data in Part 3:

Plot a graph of I_D v/s V_{GS} on a linear scale. Comment on the nature of the plot.

From Part 4:

You already have the small-signal voltage gain A_v, which is given by (refer the small signal model)

$$|A_v| = g_m R_D \tag{4}$$

Since you already know $|A_v|$ and R_D, you can easily calculate the transconductance g_m.

Post lab assignment:

1. Find out the effect on the threshold voltage of the NMOS, if
   a. Positive Body voltage is applied.
   b. Negative Body voltage is applied.

2. Subthreshold slope is a key metric for any switching device. Why?

3. The linear region of the $I_D - V_{GS}$ curve is not perfectly linear. Its slope increases first and decreases after attaining a peak value. For such a case, find out an accurate method to calculate the threshold voltage.

4. Given the $I_D - V_{GS}$ characteristics in saturation, how will you find the threshold voltage?