1. Design a counter which goes through the sequence

$000 \rightarrow 010 \rightarrow 100 \rightarrow 001 \rightarrow 011 \rightarrow 101 \rightarrow 111$ (back to 000)

2. Design a 2 bit multiplier ckt using (a) combinational circuit, (b) sequential circuit (using a shift register.

3. Design a ckt which divides the CP by n. 2 I/P

4. Design a 2 I/P XOR gate using minimum number of NAND gates.

5. The following Boolean expression $BE + \bar{B}D\bar{E}$ is a simplified version of the Expression

$$\bar{A}BE + BCDE + B\bar{C}\bar{D}E + \bar{A}\bar{B}D\bar{E} + \bar{B}\bar{C}D\bar{E}.$$

Are there any don't care conditions? If so, what are they?

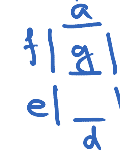
6. With the use of maps, find the simplest form in sum of products of the function $F = fg$, where f and g are given by

$$f = wx\bar{y} + \bar{y}z + \bar{w}y\bar{z} + \bar{x}y\bar{z}$$

$$g = (w + x + \bar{y} + \bar{z})(\bar{x} + \bar{y} + z)(\bar{w} + x + \bar{z})$$

7. There are two channels in a communication system. The incoming bitstreams are $A_0 A_1 A_2 A_3 \cdots A_n$ and $B_0 B_1 B_2 B_3 \cdots B_n$ Design a ckt such that the o/p sequence from the ckt is $A_0 B_0 A_1 B_1 A_2 A_3 \cdots A_n B_n$.

8. A seven segment LED display is shown below.



Desig a combination of sequential and combinational ckt such that the LED display counts from 0 to 9 and then back to 0.

9. Implement Boolean functions using decoders, multiplexers, ROM, PLA etc.

10. Obtain an 8x1 multiplexer with a dual 4-line to 1-line multiplexer having seperate enable inputs but common selection lines. Use a block diagram construction.

11. Design a 4 bit shift register such that when an input $x=0$, it loads an external input at the next CP and when $x=1$, it shifts the content of the register to the right inserting 0 in the MSB.

12. Think of practical real problem and then try to find a solution using digital circuits.