Experiment 1:
Characterization of a CMOS Inverter

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1 Overview

The CMOS inverter is one the simplest CMOS logic gate, and an important component of several digital circuits. In this experiment, we have attempted to characterize the CMOS inverter and observe its DC AC behaviour. The analysis includes the following-

- DC transfer characteristics
- Output Characteristics
- Delay Characteristics of the Inverter
- Delay variation with supply voltage
- Current drawn by the Ring Oscillator

While measuring the transfer and output characteristics, IC MM74C04 was used. The delay measurements for a single CMOS inverter due to their very small order of magnitude require high precision measurements which we are not equipped with and hence for carrying out the delay measurement, a ring oscillator with 17 inverters was used. The variation of the period of oscillation with the load can be used to obtain a good estimate on the delay. In the last part, the total current measurements are observed reflecting the superposition of the switching currents of all the inverters.

In Section 2, I have attempted to briefly describe the experimental setup for the various sub-parts of the experiment performed after which I have

presented the observations from the experiments, with relevant figures of the wave forms.

2 Observations:

The fundamental unit of each paart of the experiment is the CMOS inverter. For the CMOS invereters, I have used the *IC MM74C04* provided. I have also used the Opamp buffer *(TL072)* in order to prevent the DSO from adding extra load to the circuit during the measurement in current drawn by the ring oscillator.
Components Used: MM74C04 4, TL072, Capacitors (0.1F) 1, 20 KΩ potentiometer, resistors (1.2KΩ,1Ω).

2.1 DC Transfer Characteristics

The inverter transfer characteristic is the plot of the output voltage as a function of the input voltage. As we vary the input voltage from 0V to V_{DD} ,the output voltage will vary from V_{DD} to 0V. The point in the transfer characteristics where the input and output voltages equal is called the *switching point*. This is a crucial determinant for any switching circuit.

The observation is tabulated in Table 1 and the characteristics have been plotted in Figure 1. From these observed values we get that $V_{SW} \approx 2.6$V. But we know,

$$V_{SW} = \frac{\sqrt{\beta_p}(V_{DD} - V_t) + \sqrt{\beta_n}V_t}{\sqrt{\beta_p} + \sqrt{\beta_n}} \tag{1}$$

Substituting the values we get $\frac{\beta_p}{\beta_n} = 1.306$

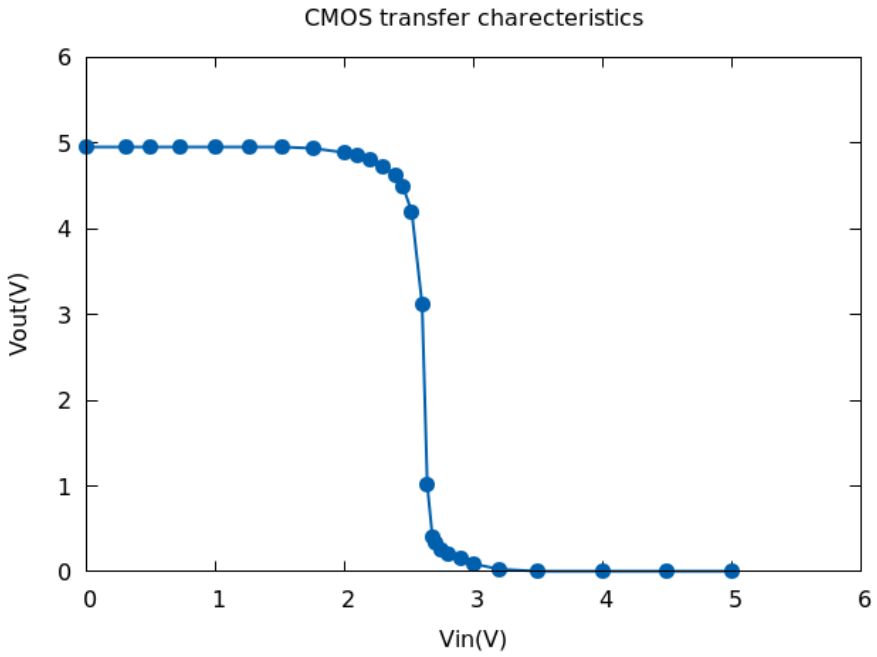

Figure 1: The plot represents the observed nature of the transfer characteristics

2.2 Output Characteristics

In this part we try to measure the output characteristics of the CMOS inverter. The figures 2 and 3 represent the output characteristics of the device.

Vin (V)	**Vout (V)**
0	4.94
0.313	4.94
0.5	4.94
0.722	4.94
1	4.94
1.26	4.94
1.514	4.94
1.755	4.93
2	4.89
2.1	4.86
2.2	4.8
2.3	4.72
2.4	4.62
2.45	4.5
2.52	4.2
2.6*	3.12
2.64	1.01
2.68	0.4
2.7	0.33
2.75	0.25
2.8	0.21
2.9	0.15
3	0.09
3.2	0.03
3.5	0
4	0
4.5	0
5	0

Table 1: DC Transfer Characteristics of the CMOS inverter

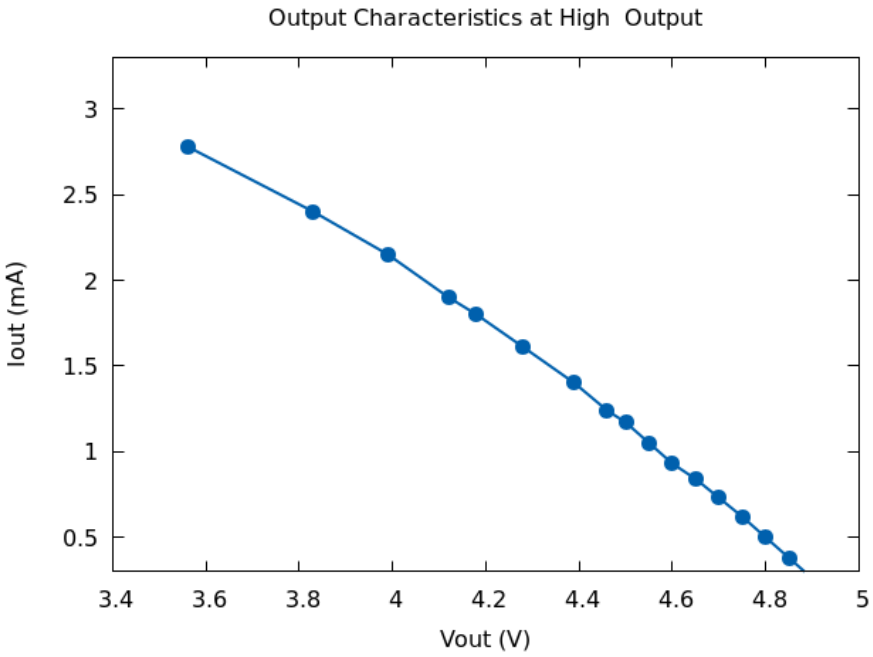

Figure 2: The plot represents the observed nature of the output characteristics at high output

We also measure the output characteristics when the output is low. From the linear characteristics of the graphs we can infer that the output impedance of the device can be said to be constant.The observed values have been tabulated in Table 2 and 3.

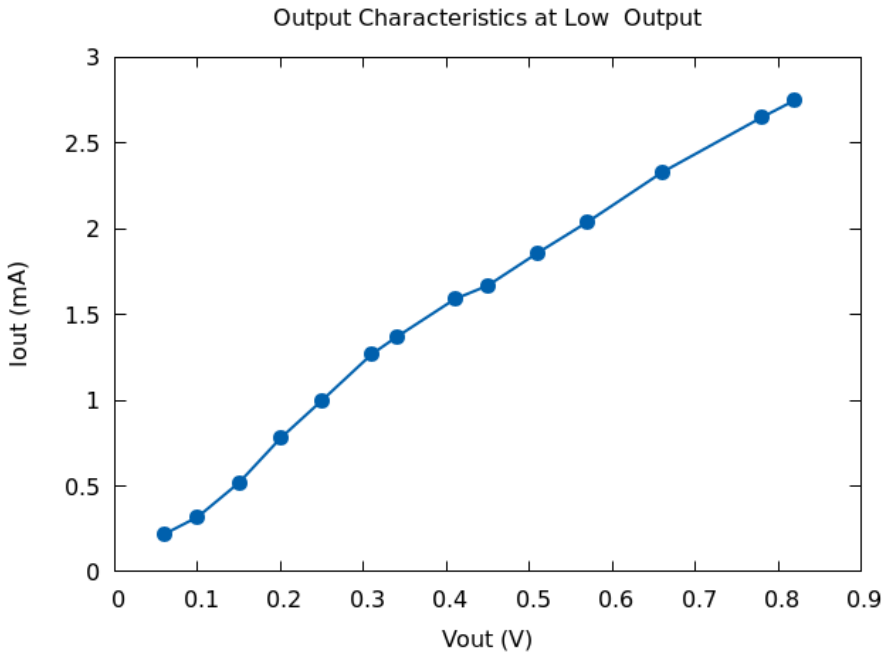

Figure 3: The plot represents the observed nature of the output characteristics at low output

2.3 Delay Characteristics of the CMOS Inverter

In any digital circuit, an important characteristic of any device is the delay caused by it. However, this delay is very small for each independent inverter and hence would require a very sophisticated equipment for measurement. In this part of the experiment we have achieved this task by using a 17- stage ring oscillator.

The delay in this circuit can be modelled as-

$$d_{abs} = k_o + k_1 C_{load} \tag{2}$$

Here, k_o and k_1 are constants, C_{load} is the load capacitance being driven by the inverter, and d_{abs} is the delay measured in seconds. It is convenient to express the C_{load} as a multiple of the input capacitance C_{in} of the inverter. The equation (2) can be re-written as-

$$d_{abs} = k_o + \tau_{inv} \frac{C_{load}}{C_{in}} \tag{3}$$

Vout (V)	**Iout (mA)**
4.92	0.22
4.9	0.26
4.85	0.38
4.8	0.5
4.75	0.62
4.7	0.73
4.65	0.84
4.6	0.93
4.55	1.05
4.5	1.17
4.46	1.24
4.39	1.4
4.28	1.61
4.18	1.8
4.12	1.9
3.99	2.15
3.83	2.4
3.56	2.78

Table 2: Output characteristics at high output or low input

Vout (V)	**Iout (mA)**
0.06	0.22
0.1	0.32
0.15	0.52
0.2	0.78
0.25	1
0.31	1.27
0.34	1.37
0.41	1.59
0.45	1.67
0.51	1.86
0.57	2.04
0.66	2.33
0.78	2.65
0.82	2.75

Table 3: Output Characteristics at low output or high input

The delay can be expressed in multiples of τ_{inv} as

$$d_{inv} = p_{inv} + \frac{C_{load}}{C_{in}} \tag{4}$$

where, $p_{inv} = \frac{k_o}{\tau_{inv}}$

In table 4, the observed data for the variation of frequency or time period with load is presented. The results are summarized in the figure 4 and the snapshots are presented in Table 5.

Number of Load	Frequency (MHz)	Time Period (ns)
2	1.19047619	840
3	1.162790698	860
4	1.136363636	880
5	1.118568233	894
6	1.094091904	914
7	1.067235859	937

Table 4: Variation of frequency or time period with number of loads

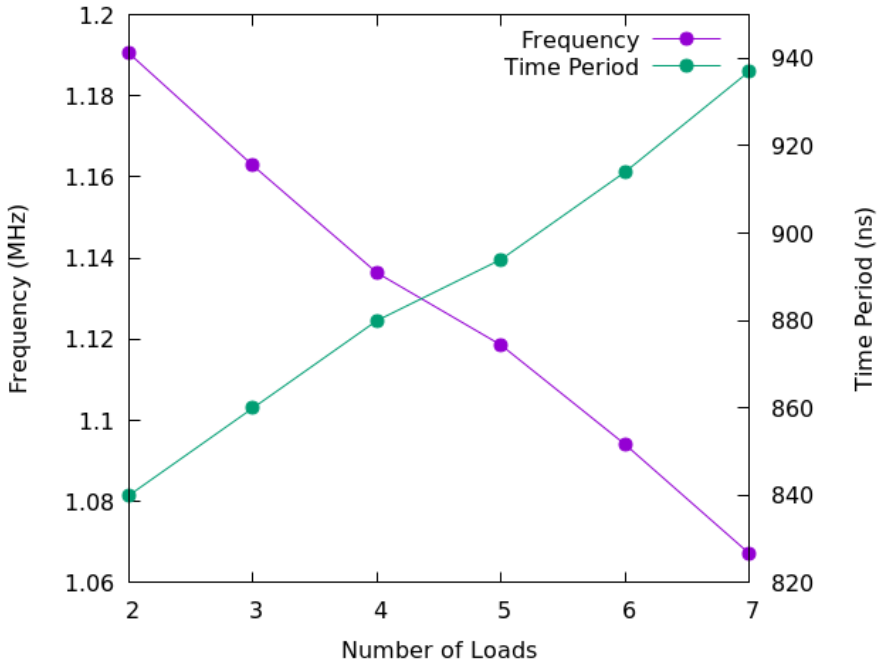

Figure 4: The plot represents the variation of the frequency and time period with respect to the number of loads VDD= 5V

The time period of oscillation is given by

$$\tau_{inv} \times (34p_{inv} + (32 + (2 \times (1 + Additionaloutputload))) \tag{5}$$

As the rise and fall times are equal we have,

$$Slope = 2\tau_{inv} = 20.85ns \tag{6}$$

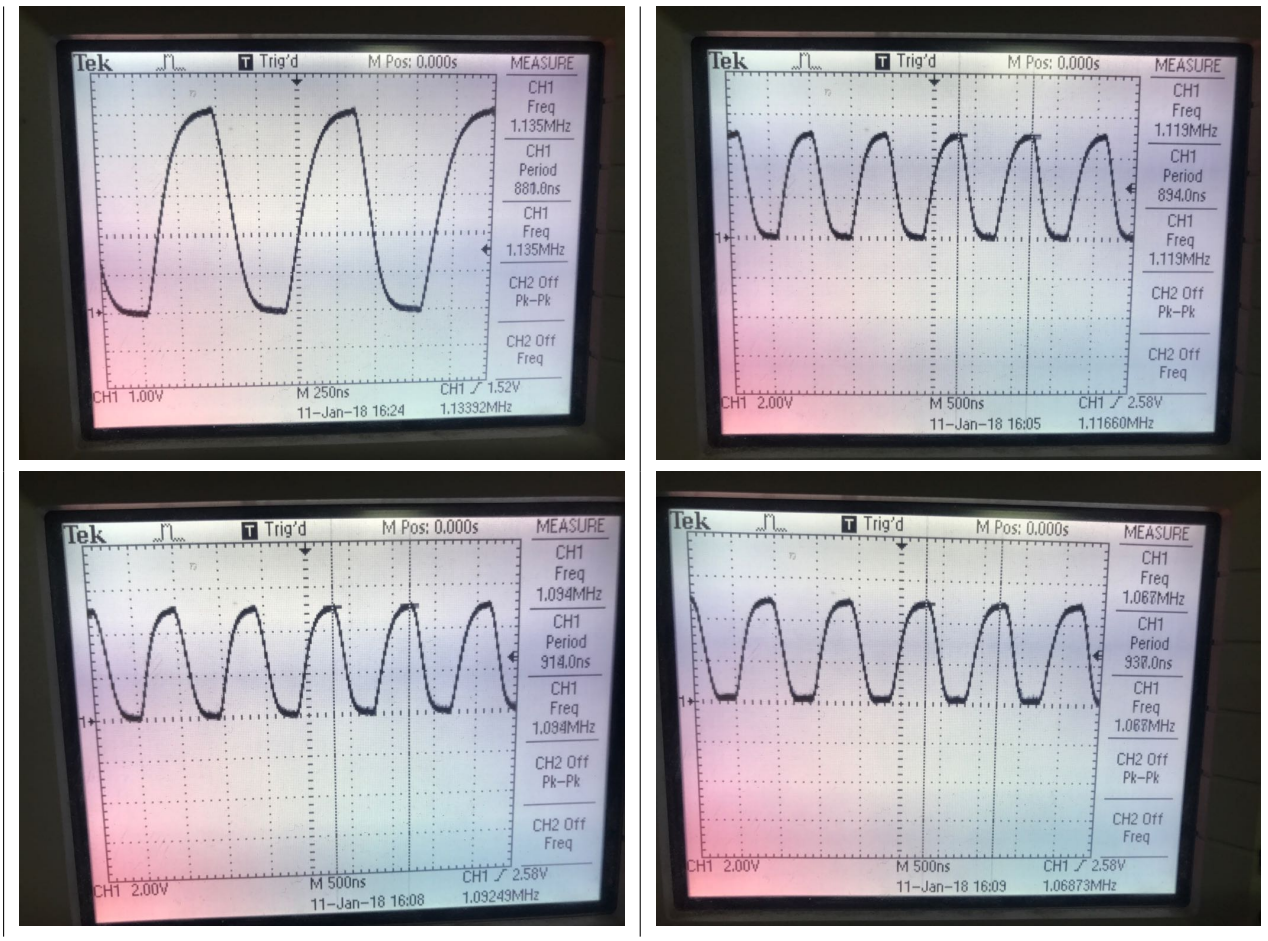

Table 5: Snapshots at different number of loads VDD=5V

$$Intercept = 34\tau_{inv}(p_{inv} + 1) = 829.8 \tag{7}$$

$$\tau_{inv} = 10.425ns \tag{8}$$

$$p_{inv} = 1.34 \tag{9}$$

2.4 Delay variation with Supply Voltage

The delay of the CMOS inverter varies with the supply voltage V_{DD}. This dependency is given below-

$$Time\ Period\ \alpha\ \frac{V_{DD}}{(V_{DD} - V_t)^2} \tag{10}$$

VDD (V)	**Time Period (μs)**
3	2.48
3.5	1.6
4	1.28
4.5	0.976
5	0.84
5.5	0.75
6	0.708

Table 6: Variation of time period of oscillation with Vdd at load=2

This part of the experiment is meant to verify this relation experimentally. The observed values are presented in Table 6.

We observe an reduction of the time period with the increase in supply voltage is evident as suggested by the relation. This is can be better visualized in the snapshots in table 7 and plots in figure 5.

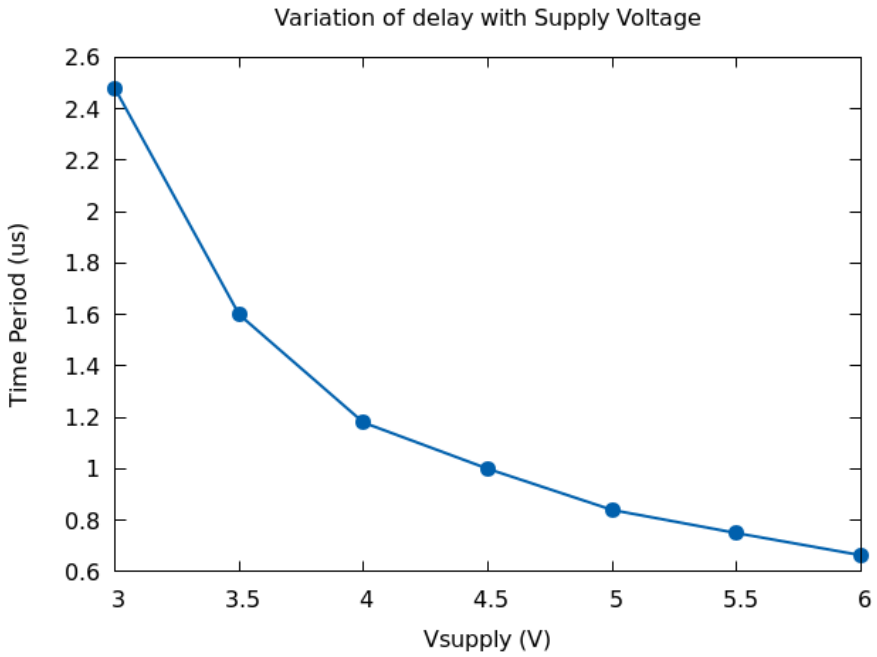

Figure 5: The plot represents the variation of time period of oscillation with VDD at load=2

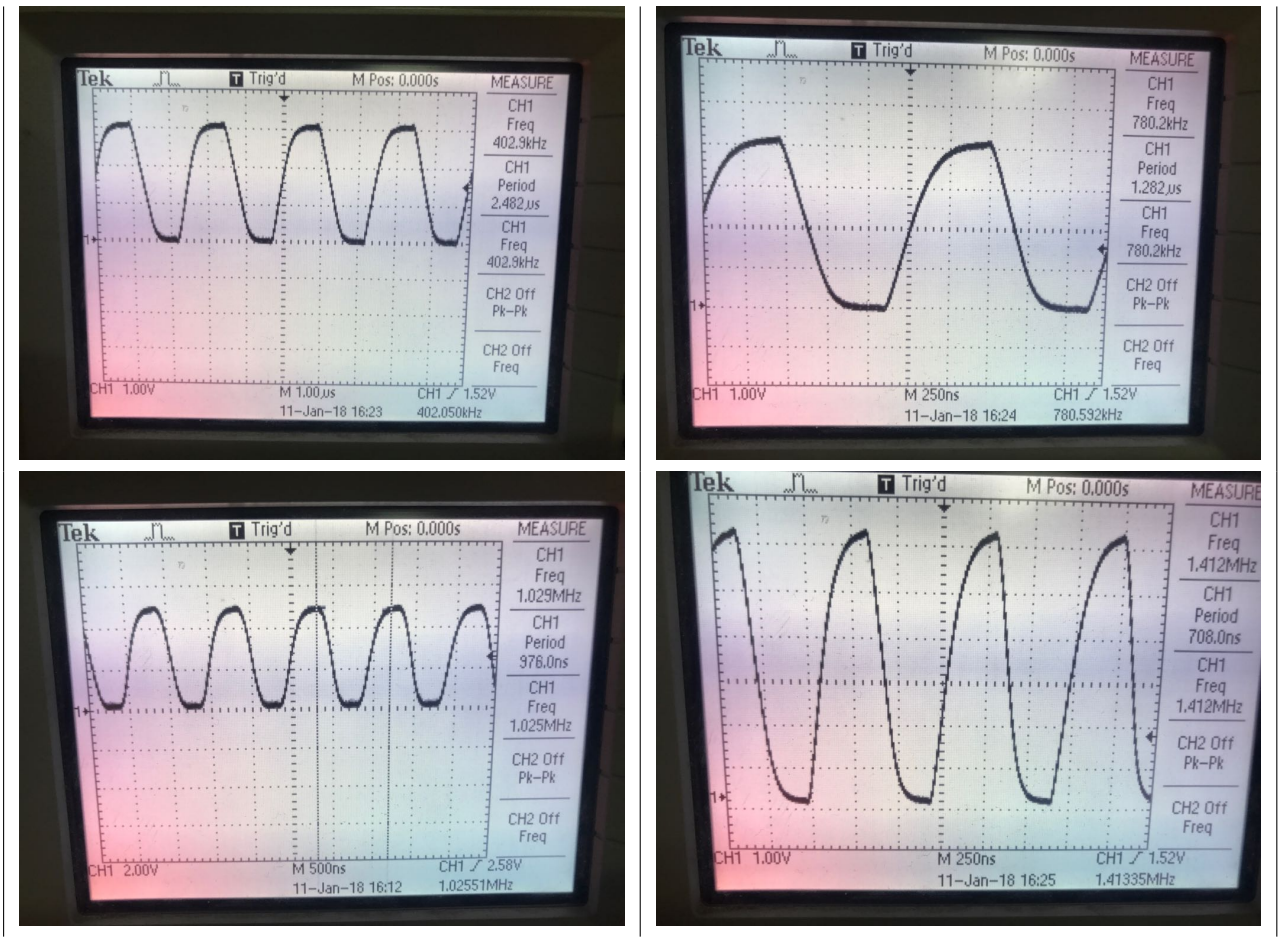

Table 7: Snapshots at varying VDD for number of loads= 2

2.5 Current drawn by the Ring Oscillator

We know that using CMOS technology the steady power loss is zero and so is the current. Hence, when the inverter output switches from low to high or vice versa, current is drawn from the power supply.In our set up, the current drawn by the ring oscillator is the sum of the currents drawn by the individual inverters. This is seen in the snapshot of the DSO in figure 6.

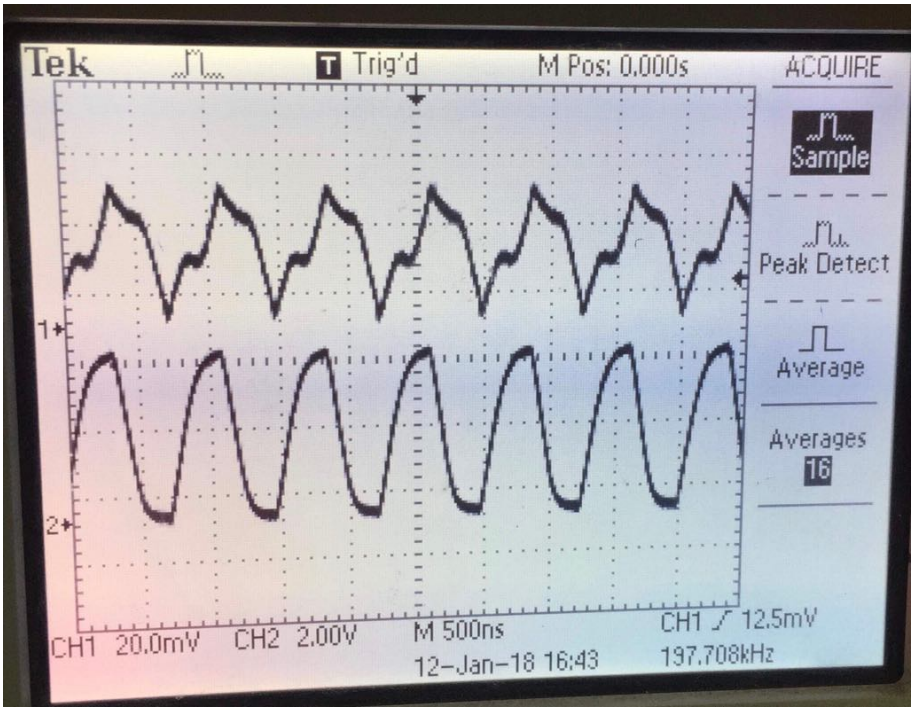

Figure 6: Snapshot of the DSO, measuring the switching current alongside Vout

The measured values of $<$ I $>$=1.96 mA and I_{P-P}=19.2 mA.

References

[1] Lab Manual, Chapter 3