Basic Switched Capacitor circuits

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Introduction

In all the previous experiments we have dealt with the circuits where both the input and output signals were continuously available in time as well as they were well defined within a voltage range. The circuits implementing such behaviour are called "continuous-time circuits", these circuits are widely used in the applications employing audio, video and high speed analog signal processing systems [1]. However, their exists another class of circuits called "discrete-time circuits" or "sampled data circuits"[1], where we are interested in signals only at periodic instants of time and we ignore the signal values at other instants, i.e. we only process signal "samples" not the whole signal and monitor a valid output at the end of each period. The circuits are widely used in the design of discrete-time filters, sampling circuits, comparators, ADCs, DACs etc..

This document provides an introduction of the basic understanding to a common class of these discrete-time systems, called switched-capacitor circuits. This document describes the analogy between a resistor and its switched-capacitor counter part.

Why Switched Capacitor ?

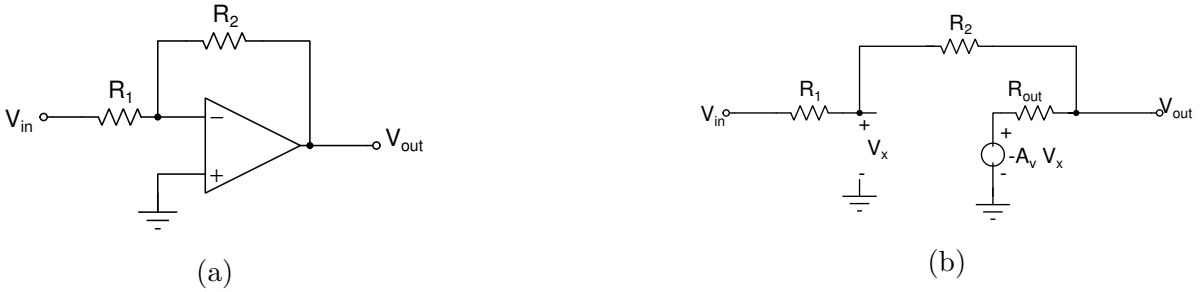


Figure 1: (a) Conventional inverting Amplifier (b) Equivalent circuit of Fig.(1a)

Consider the circuit given in Fig.(1a), this circuit poses difficulty when the op-amps are implemented in CMOS technology. Recall that, to obtain high gain in CMOS based op amps we desire high open loop output resistance, thereby the output impedance of the op-amp reaches to a very high value (typically in the orders of few hundred *kilo-Ohms*), which ideally should be very low (in the orders of few hundred *Ohms*).

Therefore, adding another resistor R_2 drops the open-loop gain heavily and worsens the precision of the amplifier [1]. For the equivalent circuit as shown in Fig.(1b), we can write that:

$$-A_v\Big(\frac{V_{out}-V_{in}}{R_1+R_2}R_1+V_{in}\Big)-R_{out}\frac{V_{out}-V_{in}}{R_1+R_2}=V_{out} \tag{1}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}.\frac{A_v - \frac{R_{out}}{R_2}}{1 + \frac{R_{out}}{R_1} + A_v + \frac{R_2}{R_1}} \tag{2}$$

From eq.(2) it can be clearly observed that in contrast to case where $R_{out} = 0$, we see the closed loop gain is no more equal to the value $\frac{-R_2}{R_1}$. Also, the input resistance R_1 not just loads the output of the previous stage but also adds to its thermal noise.

In order to avoid the reduction in the open loop gain (dc) of the op-amp we can use capacitive feedback amplifiers rather than using resistive feedback amplifier, as capacitors offer infinite impedance at dc, open loop gain of the amplifiers remains unaltered. The circuit used for high signal amplification is as shown in Fig.(2). Here, resistance R_f is used to establish dc operating point at inverting node of the op-amp, while negligibly affecting the ac behaviour of the circuit.This can be seen as given below:

$$\frac{V_{out}(s)}{V_{in}(s)} \approx -\frac{\frac{R_f \frac{1}{sC_2}}{R_f + \frac{1}{sC_2}}}{\frac{1}{sC_1}} \tag{3}$$

$$\Rightarrow \frac{V_{out}(s)}{V_{in}(s)} = -\frac{R_f C_1 s}{R_f C_2 s + 1} \tag{4}$$

Looking at eq.(4) we can say that, for $\omega >> (R_f C_1)^{-1}$ then only we can say that $\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$, i.e. we may not be able to use this circuit for the amplification of wideband amplification due to its high pass nature. Therefore, we may need to resort to other circuits for the amplification of wideband applications.

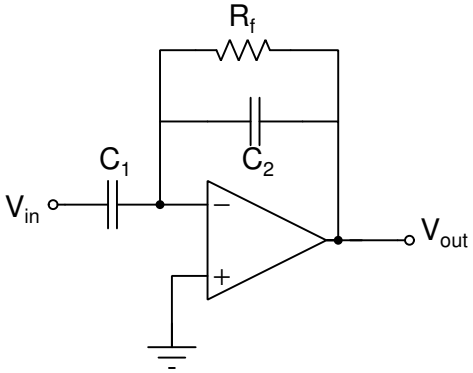


Figure 2: Capacitance Amplifier

Consider the switched-capacitor circuit as given in Fig.(3), assuming in the begining that open loop gain of the op-amp is large and we have two phase operation of the circuit, i.e. when switches S_1 and S_2 are on and S_3 is off at instant t=0 (**Sampling Phase**), thereby leading to circuit as shown in Fig.(4a), then due to virtual ground we will have $V_x = V_{out} = V_+ = 0$, hence the C_1 is charged to input voltage (V_{in}). At instant t=t_0 (**Amplification Phase**) S_1 and S_2 turns off and S_3 turns on, i.e. we can see that the capacitance C_1 has a net voltage of 0V across it. voltage zero across it as node Y is now brought down to 0V. Therefore,

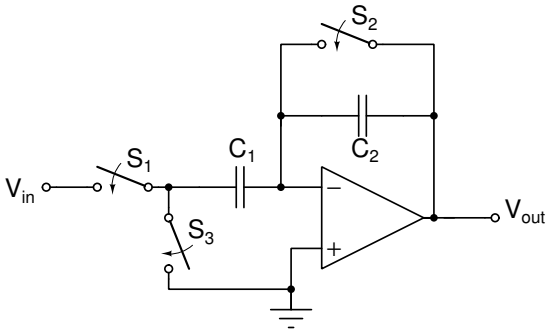


Figure 3: Switched Capacitor Amplifier

based on the law of conservation of charge we can say that:

$$Q_{c_1}(t = t_0^-) + Q_{c_2}(t = t_0^-) = Q_{c_1}(t = t_0^+) + Q_{c_2}(t = t_0^+) \tag{5}$$

$$V_{in}C_1 = V_{out}C_2 \Rightarrow V_{out} = \frac{C_1}{C_2}V_{in} \tag{6}$$

This transfer of charge is demonstrated in Fig.(5). Also, from eq.(6) it is clear that circuit amplifies the V_{in} at instant t=0 to a value $\frac{C_1}{C_2}V_{in}$

(a) (b)

Figure 4: (a) Circuit of Fig.(3) during phase - 1 (b) Circuit of Fig.(3) during phase - 2

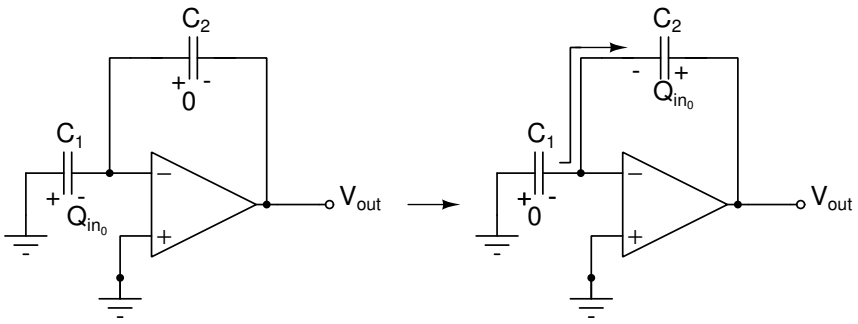


Figure 5: Transfer of Charge from C_1 to C_2
during instant t=t_0

Based on above analysis we can list the advantages of switched capacitor amplifier (Fig.(4a)) over the normal resistive amplifier (Fig.(1a)) as [1]:

- We note that as soon as V_{out} settles, the current through C_2 becomes zero. That is given enough time for output to settle switched-capacitor amplifier does not reduce the open loop gain of the op-amp. On the other hand, as discussed R_2 continuously load the op-amp affecting its open loop gain.

- Switched capacitors circuits are much easy to implement in CMOS technology then compared to other ones. This because discrete time circuits requires switches to perform sampling and to maintain high input impedance of op-amp to store the sampled charge without any leakage. If op-amps are implemented using bipolar technologies we will have a significant base current and hence charge leakage, leading to error in output voltage. The high input impedance and better switching property of CMOS technology has made them a popular choice for discrete-time applications.

Hence, one can view discrete-time circuits operating in two phases as shown in Fig.(6)

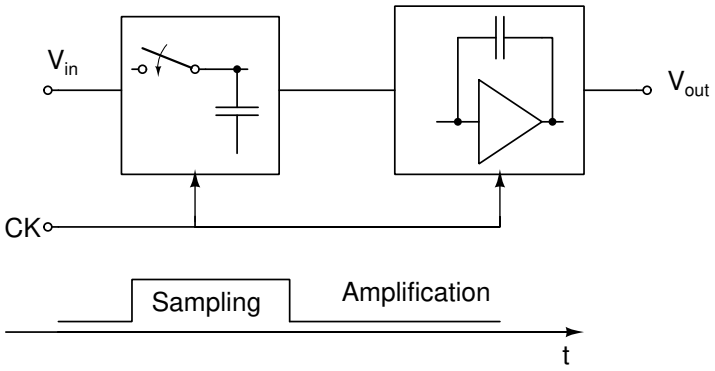


Figure 6: General View of Switched Capacitor Amplifier

Switch Capacitor as a resistor

Consider the circuit as shown in Fig.(7), initially assume that $C_1 = C_2 = C$ has zero charge and both S_1 and S_2 are off. Say, now we turn on only S_1, then we can say that:

$$Q_1 = VC, Q_2 = 0 \tag{7}$$

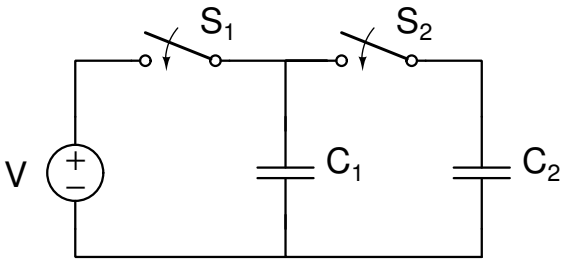


Figure 7: Charge-Energy Conservation

Also,

$$Energy_{C_1} = \frac{1}{2}C_1V^2, Q_2 = 0 \tag{8}$$

Now, we turn off S_1 and S_2 is turned on and $V^{'}$ is the final charge on both the capacitances then, due to charge conservation we have:

$$Q_{1_{initial}} = Q_{1_{final}} + Q_{2_{final}} \Rightarrow CV = CV^{'} + CV' \Rightarrow V' = \frac{1}{2}V \tag{9}$$

and

$$Energy_1 = Energy_2 = \frac{1}{2}CV^{'} = \frac{1}{2}C(\frac{1}{2}V)^2 = \frac{1}{8}CV^2 \Rightarrow Energy_{total} = \frac{1}{4}CV^2 \tag{10}$$

From eq.(10) it is clear that following the law of charge conservation we cannot satisfy the law of conservation of energy. But is it so? We see eq.(10) hints for the loss of $\frac{1}{2}CV^2$ energy, and the passive element which is responsible for loss in energy/power is resistor, i.e. in the above circuit we observe a inherent presence of a resistor.

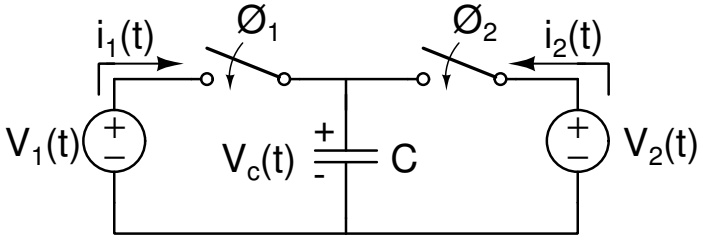


Figure 8: Parallel Switched Capacitor Equivalent Resistor[2]

On the basis of above analysis we see that we can have a resistive action if we periodically charge and discharge a capacitor!! But what will be the value of the resistor? To answer this question consider the

circuit as shown in Fig.(8). If Φ_1 and Φ_2 are the two non-overlapping clocks (alternatively, called as two phase clocks), such that Φ_1 is on for 0 to $\frac{T}{2}$ and Φ_2 is on for $\frac{T}{2}$ to T, where T is the clock period then:

During $0 < t < \frac{T}{2}$ we have circuit as shown in Fig.(9). Assuming $V_1(t)$ and $V_2(t)$ are changing very slowly compared to clock cycle, we can say that the average current through the capacitor is:

$$i_{1_{avg}} = \frac{1}{T}\int_0^T i_1(t)dt = \frac{1}{T}\int_0^T \frac{dq_1(t)}{dt} = \frac{q_1(T/2) - q_1(0)}{T} = \frac{CV_C(T/2) - CV_C(0)}{T} = \frac{CV_1 - CV_2}{T} \tag{11}$$

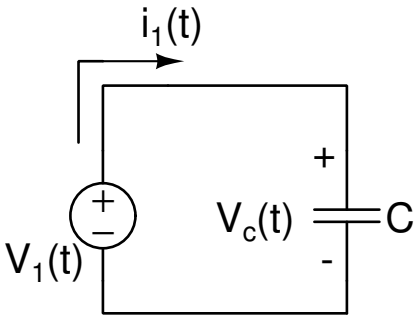


Figure 9: During Phase Φ_1

For the continuous time circuit as shown in Fig.(10), we can write:

$$i_{1_{avg}} = \frac{V_1 - V_2}{R} \tag{12}$$

Comparing the result of eq.(11) and that of eq.(12) we can say that the circuit in Fig.(8) emulates a

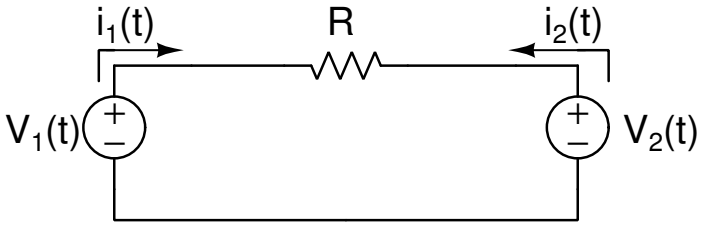


Figure 10: Continuous Time resistor circuit

resistance of equivalent value:

$$R = \frac{T}{C} \tag{13}$$

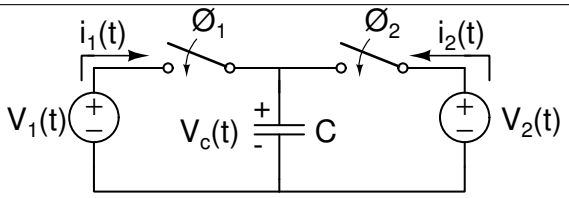
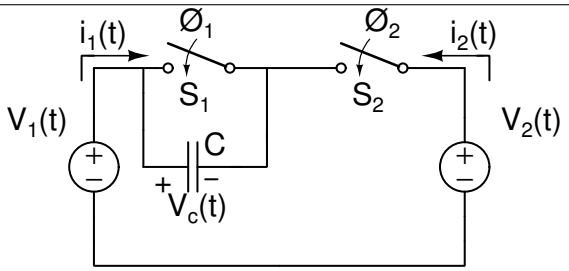
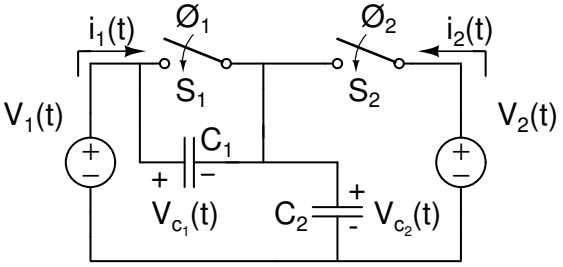
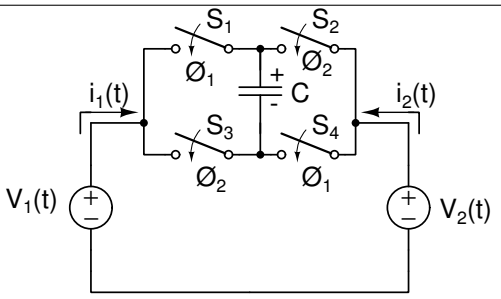
Also, verify on the similar analogy the circuits given in Table(1) corresponds to the value given on the right most column.

References

1. http://www.seas.ucla.edu/brweb/teaching/AIC_Ch12.pdf

2. http://mgh-courses.ece.gatech.edu/ece4430/ECE4430/Unit2/Switch-Cap01.pdf

Table 1: Switched Capacitor Circuits and their corresponding resistance values

Switched Capacitor Resistor Emulation Circuit	Schematic	Equivalent Resistance
Parallel		$\frac{T}{C}$
Series		$\frac{T}{C}$
Series-Parallel		$\frac{T}{C_1+C_2}$
Bilinear		$\frac{T}{4C}$