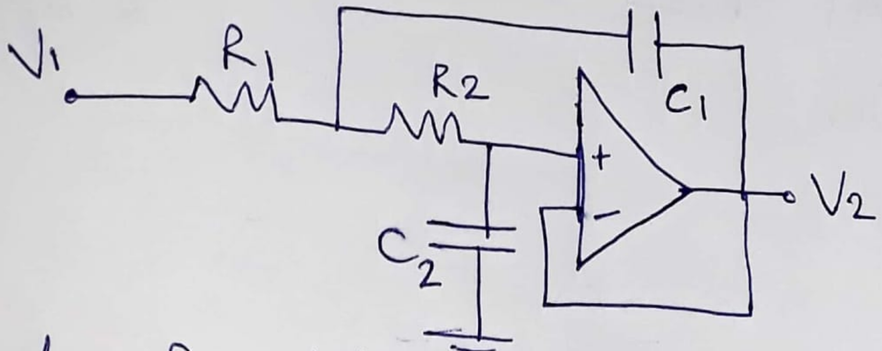
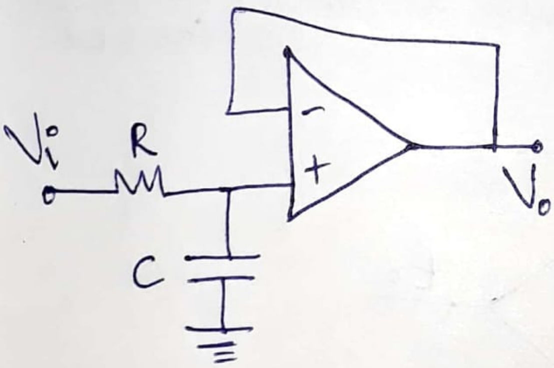


Low Pass filter (2nd order)

$$\frac{V_2}{V_1} = \frac{1/R_2R_1C_1C_2}{s^2 + \left(1/R_1C_1 + 1/R_2C_1\right)s + 1/R_1R_2C_1C_2}$$

$$= \frac{\omega_o^2}{s^2 + (\omega_o/Q)s + \omega_o^2}$$



$$\frac{V_o}{V_i} = \frac{1}{1+sCR}$$

1st order low pass

5th order

∴ For higher orders, just cascade these two filters.

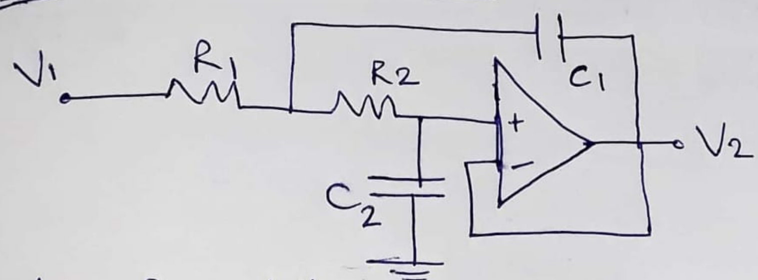
Impedance Transformation (To convert lp to hp)

Date

For $n=2$,

$$|T|^2 = \frac{K^2}{1+\omega^4} \Rightarrow |A_{\omega n}|^2 = \frac{\omega^4}{1+\omega^4}$$

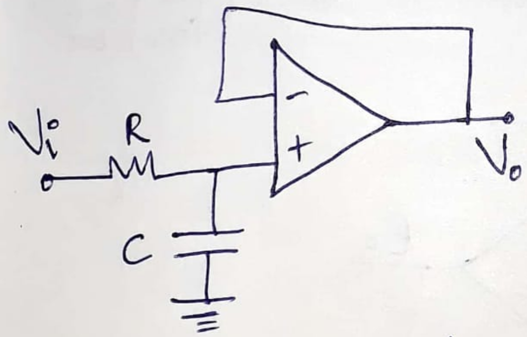
Sallen-Key Filter



Low Pass filter (2nd order)

$$\frac{V_2}{V_1} = \frac{1/R_2R_1C_1C_2}{s^2 + \left(1/R_1C_1 + 1/R_2C_1\right)s + 1/R_1R_2C_1C_2}$$

$$= \frac{\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$



$$\frac{V_o}{V_i} = \frac{1}{1+sCR}$$

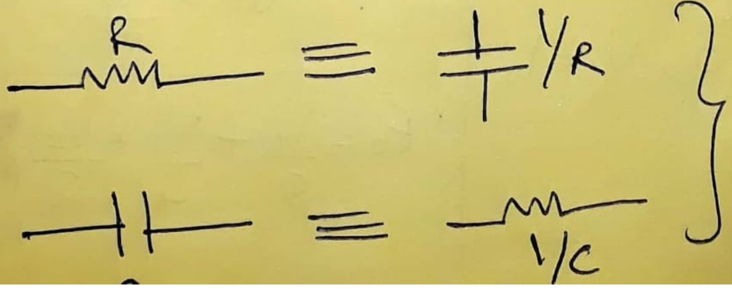
1st order low pass

5th order

∴ For higher orders, just cascade these two filters.

Impedance Transformation (To convert lp to hp)

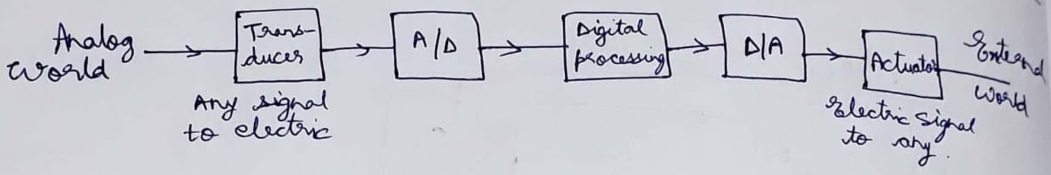
Notes:



$s \rightarrow \omega_0'/s$

Date 16/4/18

D to A and A to D converter (Mixed Signal Processing)



D to A

I/p

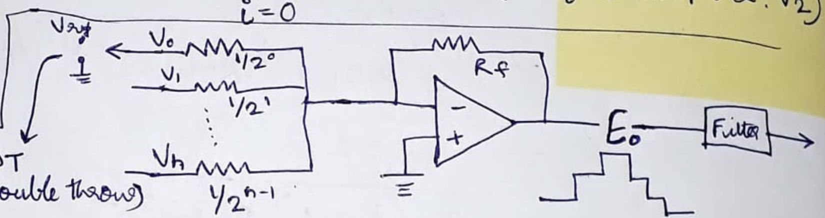
3bit

V_2	V_1	V_0
0	0	0
1	0	1
1	0	0
1	1	1

$0 \longrightarrow 0V$

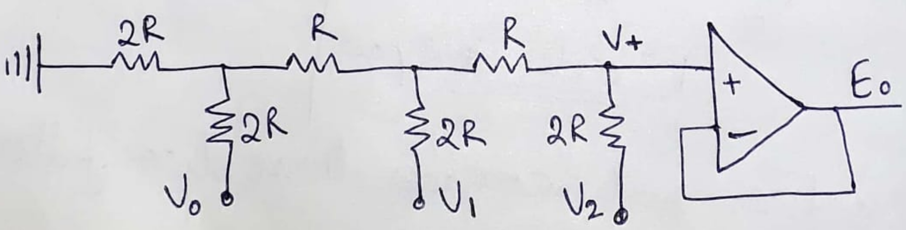
$1 \longrightarrow V_{ref}$

$$E_0 = K\sum_{i=0}^{n-1} V_i\, 2^i = K(2^0.V_0 + 2^1.V_1 + 2^2.V_2)$$



It is difficult to have the resistance values precisely & the range of resistance values is large (1Ω to $2^8\Omega$) for 8 bit

∴ R-2R ladder D/A converter



Case I: $V_0 = V_1 = 0,\ V_2 = 1,$

$$\therefore V_+ = \frac{V_2}{2}$$

Case II: $V_0 = V_2 = 0,\ V_1 = 1,$

$$\therefore V_+ = \frac{V_1}{4}$$

Case III: $V_0 = 1,\ V_1 = V_2 = 0$

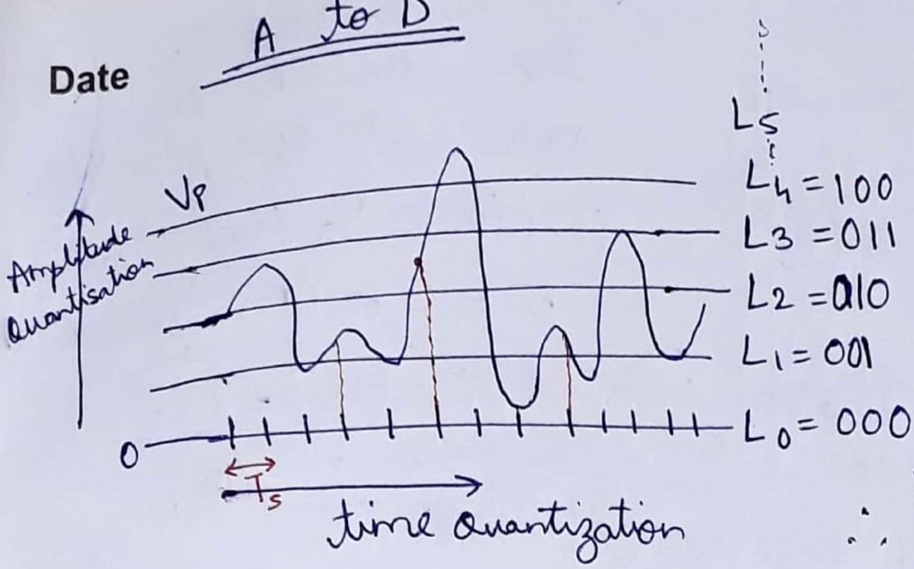
$$\therefore V_+ = \frac{V_0}{8}$$

$$\therefore E_0 = \frac{V_0}{8} + \frac{V_1}{4} + \frac{V_2}{2}$$

Notes:

Date

A to D

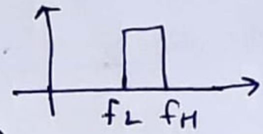


$f_s = \frac{1}{T_s}$

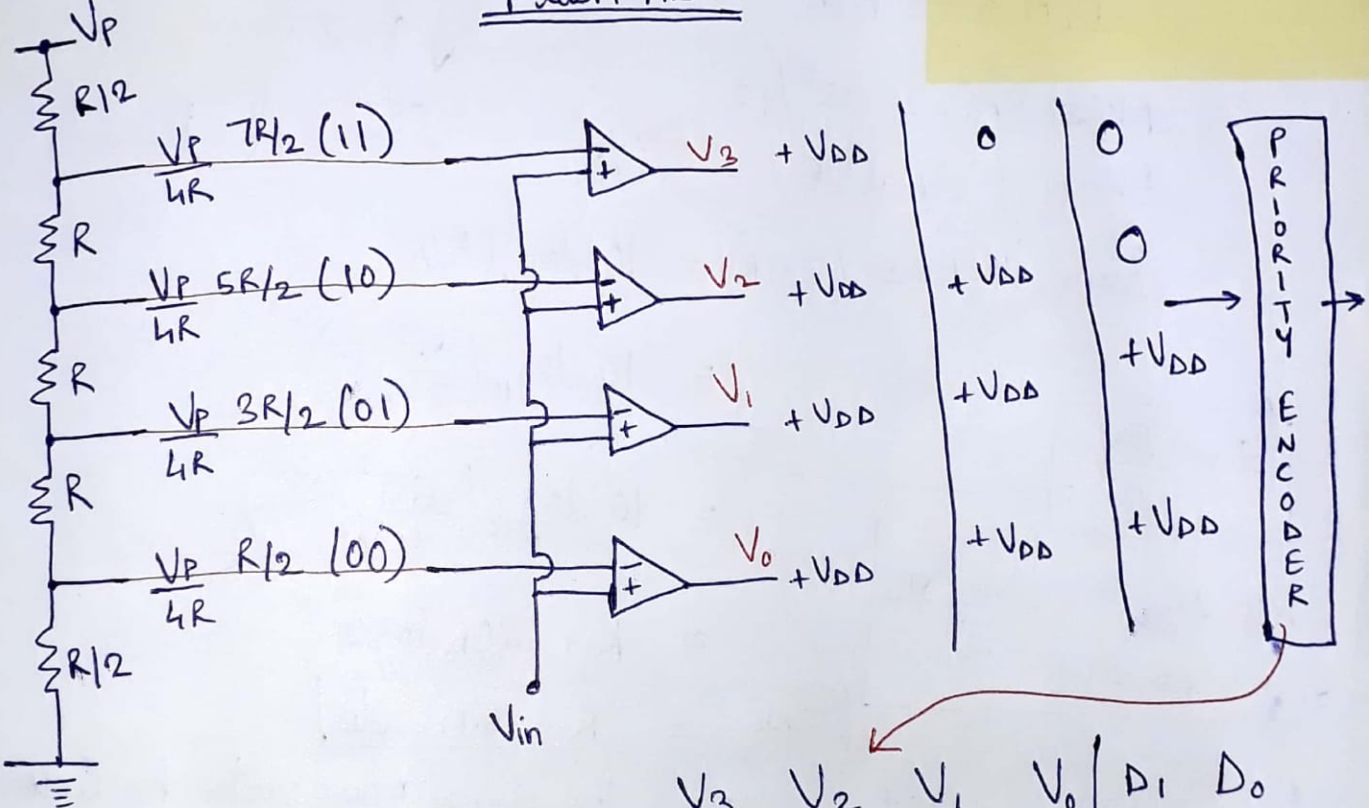
Sampling freq.
No. of samples taken per second.

$\therefore \boxed{f_s > 2f_i}$ → highest freq. in input

or $f_s > 2(f_H - f_L)$ → even works
(choose anti-aliasing filter) appropriately



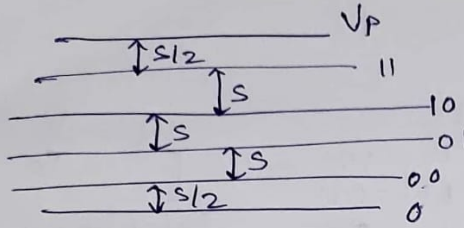
Flash ADC



V_3	V_2	V_1	V_0	D_1	D_0
1	X	X	X	1	1
0	1	X	X	1	0

Single slope ADC
Dual slope ADC

Date



$\therefore$ Within a step, the signal can take any Value with equal probability.

$\therefore f(x) = 1/s$ (Uniform dist.)

$\bar{x} = 0$ or $E(x) = \int_{-s/2}^{s/2} x\left(\frac{1}{s}\right)dx = 0$

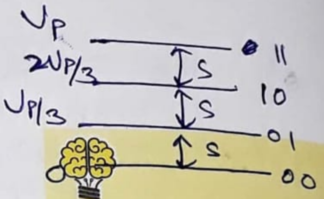
$\therefore S = \dfrac{V_P}{4}$

$\therefore Var = E(x^2) - E(\bar{x})^2 = E(x^2)$

Quantization Error. $\leftarrow$ $\therefore$ $\boxed{Var. = s^2/12}$

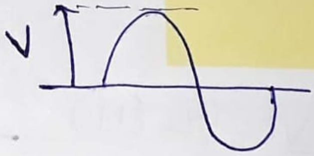
$\therefore$ A lower step size is desirable.

Higher Quantization error $\Leftarrow S = \dfrac{V_P}{3} \Leftarrow$



17/4/18

D/A $\longleftrightarrow$ A/D



Noise (N) $= s^2/12$

Energy of signal (E) $= V^2/2$

Signal to noise ratio (SNR) $= 10\log_{10}(E/N)$

$$= 10\log_{10}\left(\frac{V^2 \cdot 12}{2 \cdot s^2}\right)$$

$\boxed{S = \dfrac{2V}{2^n}}$

$$= 10\log_{10}\left(\frac{6V^2 \cdot 2^{2n}}{4V^2}\right)$$

Step size (S) $= \dfrac{V_{pk-pk}}{2^n}$

n = no. of bits

$$= K + 20n\log 2$$

$$\boxed{SNR = K + 6n \text{ dB}}$$

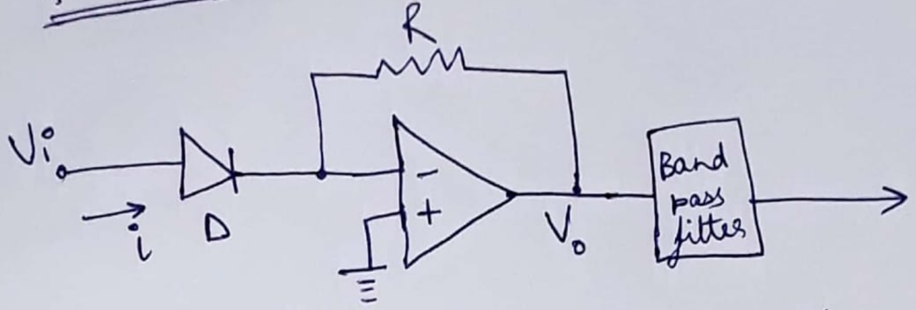
$\therefore$ Adding 1 bit, improves the signal noise ratio by 6 dB.

es:

Date

Scanned by CamScanner

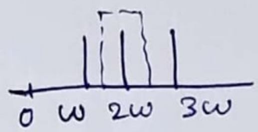
Date # $f \longrightarrow 2f$



$$i = I_o e^{V_i/\eta kT} = -\frac{V_o}{R} \quad \Bigg\} \quad V_o = -I_o R e^{V_i/\eta kT}$$

$$= -I_o R\left[1 + \frac{V_i}{\eta kT} + \frac{V_i^2}{2\eta^2 k^2 T^2} + \dots\right]$$

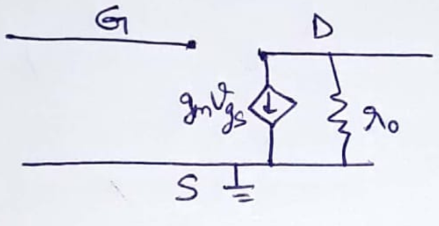
Filter out the $2f$ freq.

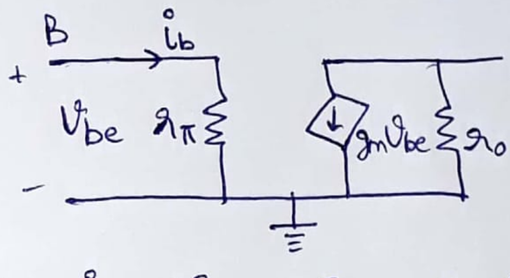


For, $V_i = V_A \sin \omega t$

M II Take square wave with 0, 2ω, 4ω frequencies & then filter out just 2ω freq^n.

BJT & MOS





$i_c = \beta i_b$, $\beta = g_m r_\pi$

Bi CMOS $\longrightarrow$ CMOS + BJT.

Stability

$A\beta = 1 \longrightarrow$

$\therefore \uparrow$ gain & phase margin for stability