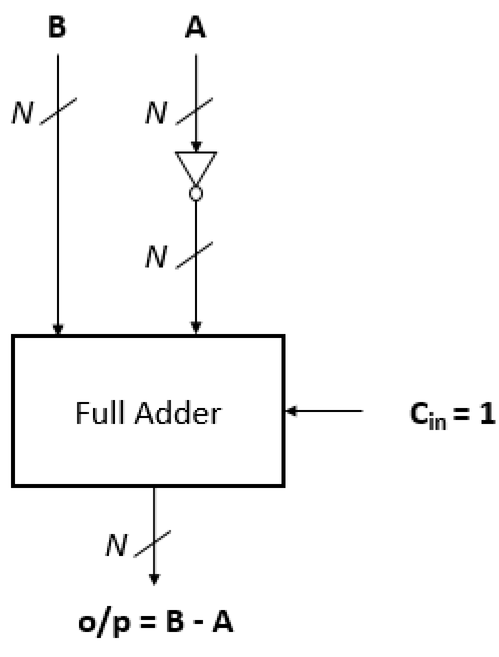
EE 224 Midterm Exam Solutions

1(a)

$$\begin{aligned}
A &= \sum_{k=0}^{N} x_k.2^k \\
B &= \sum_{k=0}^{N} \bar{x_k}.2^k \\
&= \sum_{k=0}^{N} (1 - x_k).2^k \\
&= \sum_{k=0}^{N} 2^k - \sum_{k=0}^{N} x_k.2^k \\
&= (2^{N+1} - 1) - A
\end{aligned}$$

1(b)

$$\begin{aligned}
(B - A)_{bottom\ N\ bits} &= (B + 2^{N+1} - A)_{bottom\ N\ bits} \\
&= (B + [(2^{N+1} - 1) - A] + 1)_{bottom\ N\ bits}
\end{aligned}$$



Solution: Question 2

A logic circuit has n inputs $x_0, x_1, ...x_{n-1}$ and its output is 1 iff the no. represented by these bits is a power of 2.

(a) We have to design a circuit so that it uses $O(n)$ two-input logic gates and has a delay of $O(\log n)$ units.

Number is power of 2.
$\implies$ exactly 1 bit in $x_0, x_1, ...x_{n-1}$ is set to 1

Therefore, Divide and Conquer.

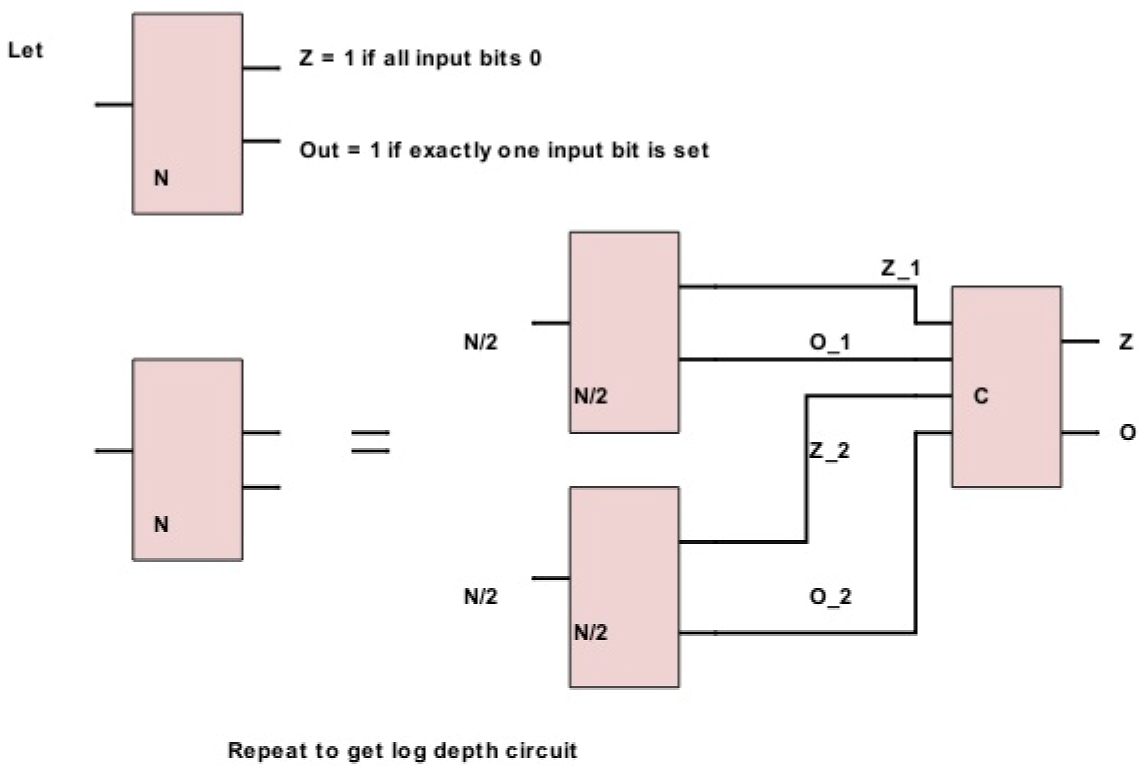


Figure 1: Divide and Conquer

Note : Z= $Z_1.Z_2$
$O = Z_1.O_2 + O_1.Z_2$

(b) Using two-input AND, OR and NOT gates we have to implement the above circuit for n = 8.

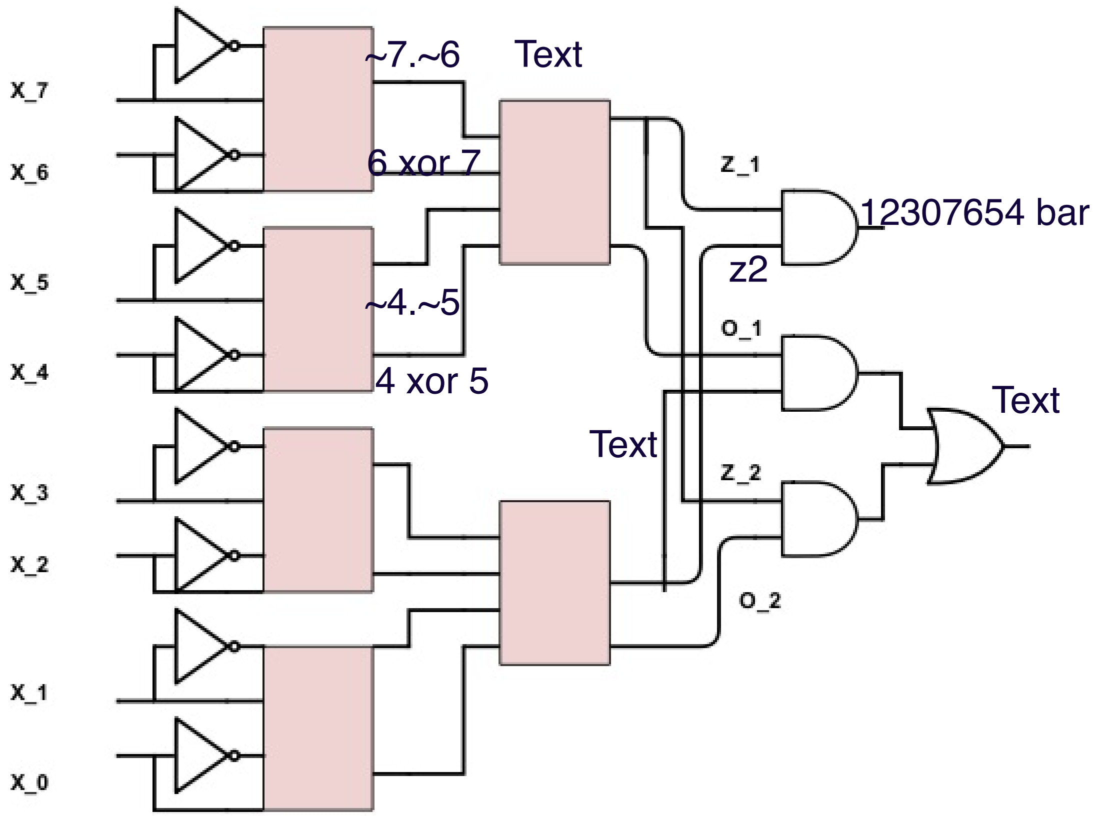
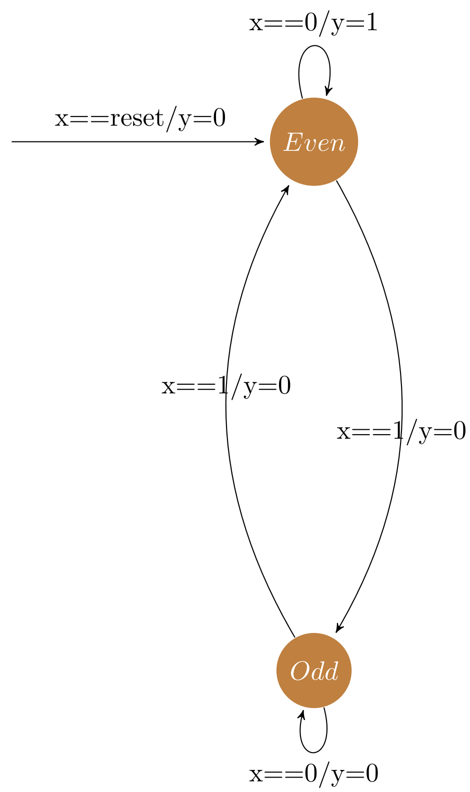


Figure 2: Divide and Conquer for n = 8

Total delay = 7

Question 3 solution

1. The mealy FSM just requires two states :
   - Even : The number of 0's are even
   - Odd : The number of 0's are odd
2. The mealy FSM should look like this (with reset or initial state mentioned):



Evaluation scheme :

Part a: Mentioning of 2 states and their description carries a mark each

Part b: Meaningful FSMs are given 3 marks. +1 mark if only 2 states used. +1 mark if correct reset/initial state mentioned

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4(a)

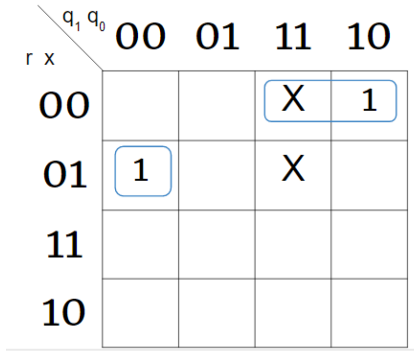

Figure 1: $nq_0 = \bar{r}.x.\bar{q_1}.q_0 + \bar{r}.\bar{x}.q_1$

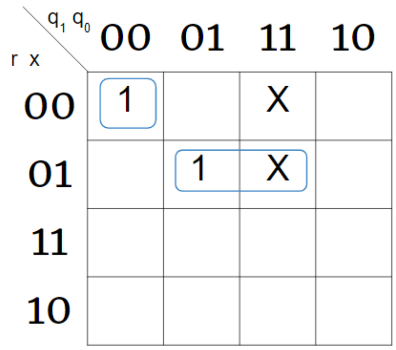

Figure 2: $nq_1 = \bar{q_1}.\bar{q_0}.\bar{r}.\bar{x} + \bar{r}.x.q_0$

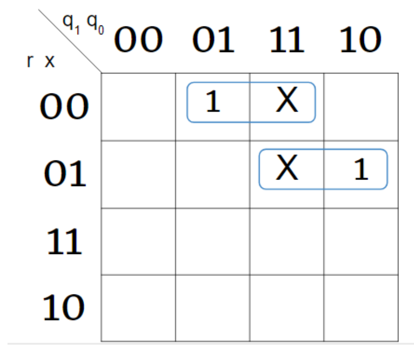

Figure 3: $z = q_0.\bar{r}.\bar{x} + \bar{r}.x.q_1$

4(b)

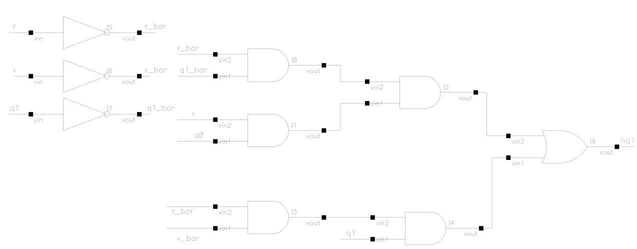

Figure 4: nq_0

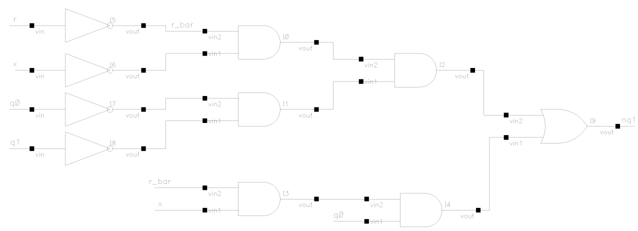

Figure 5: nq_1

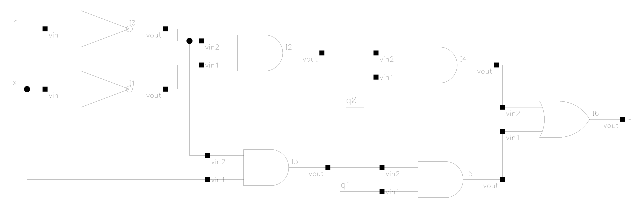

Figure 6: z

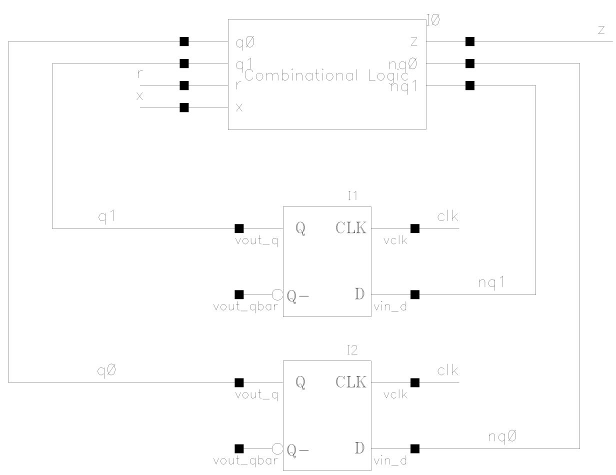

Figure 7: FSM diagram.

4(c)

It takes 8 time units to generate nq_1, nq_0, z after all the required inputs are available. Output 'z' must be ready at the most by time t.
nq_1, nq_0 must be ready by t-2(setup and hold time). Consider that

at/before t = 0 z, nq_0, nq_1 of previous cycle are ready. Clock edge arrives at t= 0, q_1 and q_0 are ready by t = 3 (clock to output delay). r, x become ready at T/2. Case 1: Assume that r, x arrive late as compared to q_1, q_0 i.e. $T/2 \geq 3$

$$T \geq 6$$

For output z

$$T/2 + 8 \leq T$$

for nq_1, nq_0

$$T/2 + 8 \leq T - 2$$

$$10 \leq T/2$$

$$T \geq 20$$

which satisfies $T \geq 6$

Case 2 :

$$T/2 \leq 3$$

$$T \leq 6$$

For z

$$3 + 8 \leq T$$

For nq_1, nq_0

$$3 + 8 \leq T - 2$$

$$T \geq 13$$

assumption $T \leq 6$ is violated.