A first look at CMOS logic gates

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Logic Gate?

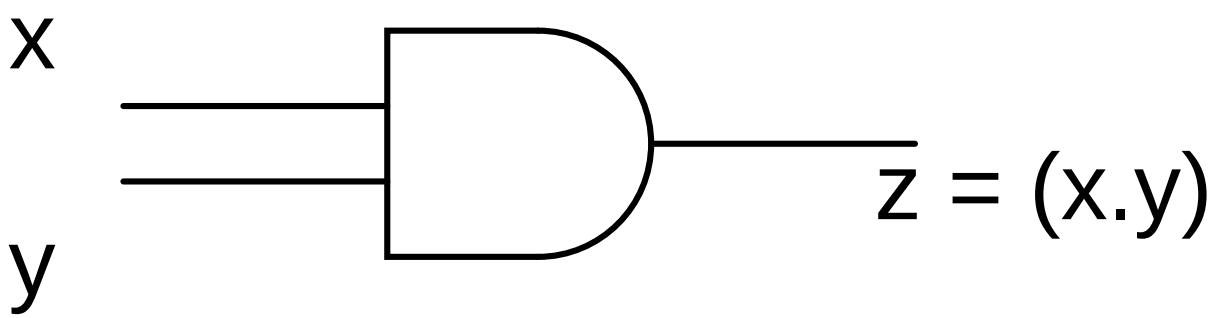

Figure: AND logic gate

Other two input logic gates

- OR2: $z = x + y$.
- NAND2: $z = \overline{x.y}$.
- NOR2: $z = \overline{x + y}$.
- XOR2: $z = (x + y).(\overline{x} + \overline{y})$.
- etc..

The CMOS inverter

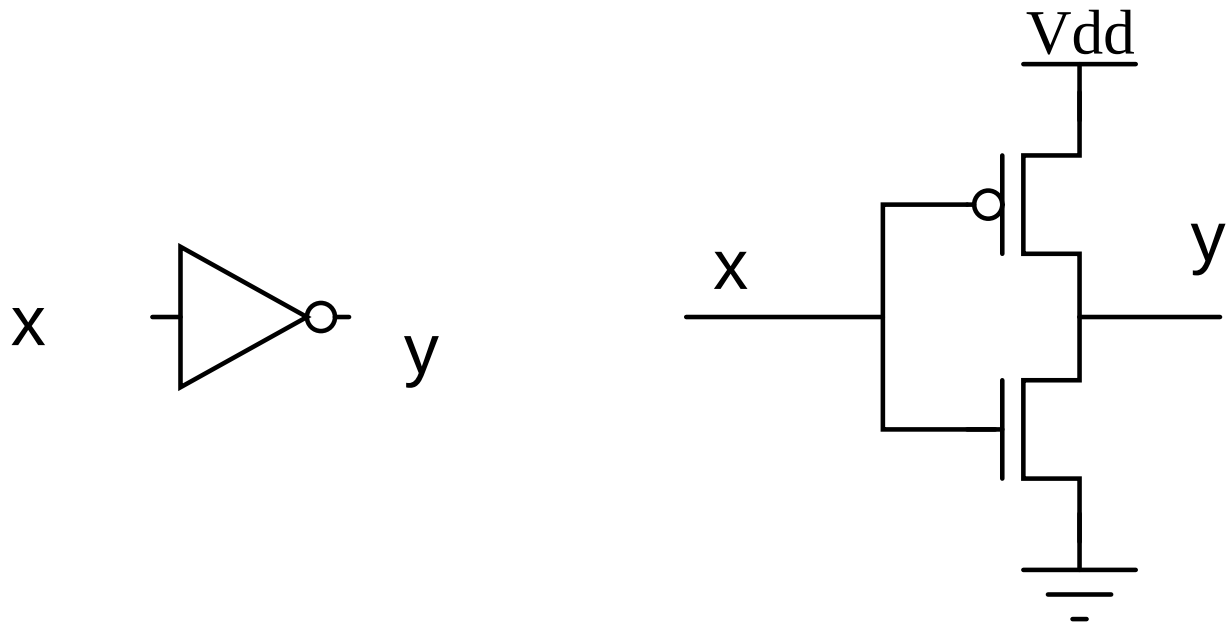

Figure: CMOS inverter

Inverter characteristics: Transfer characteristics

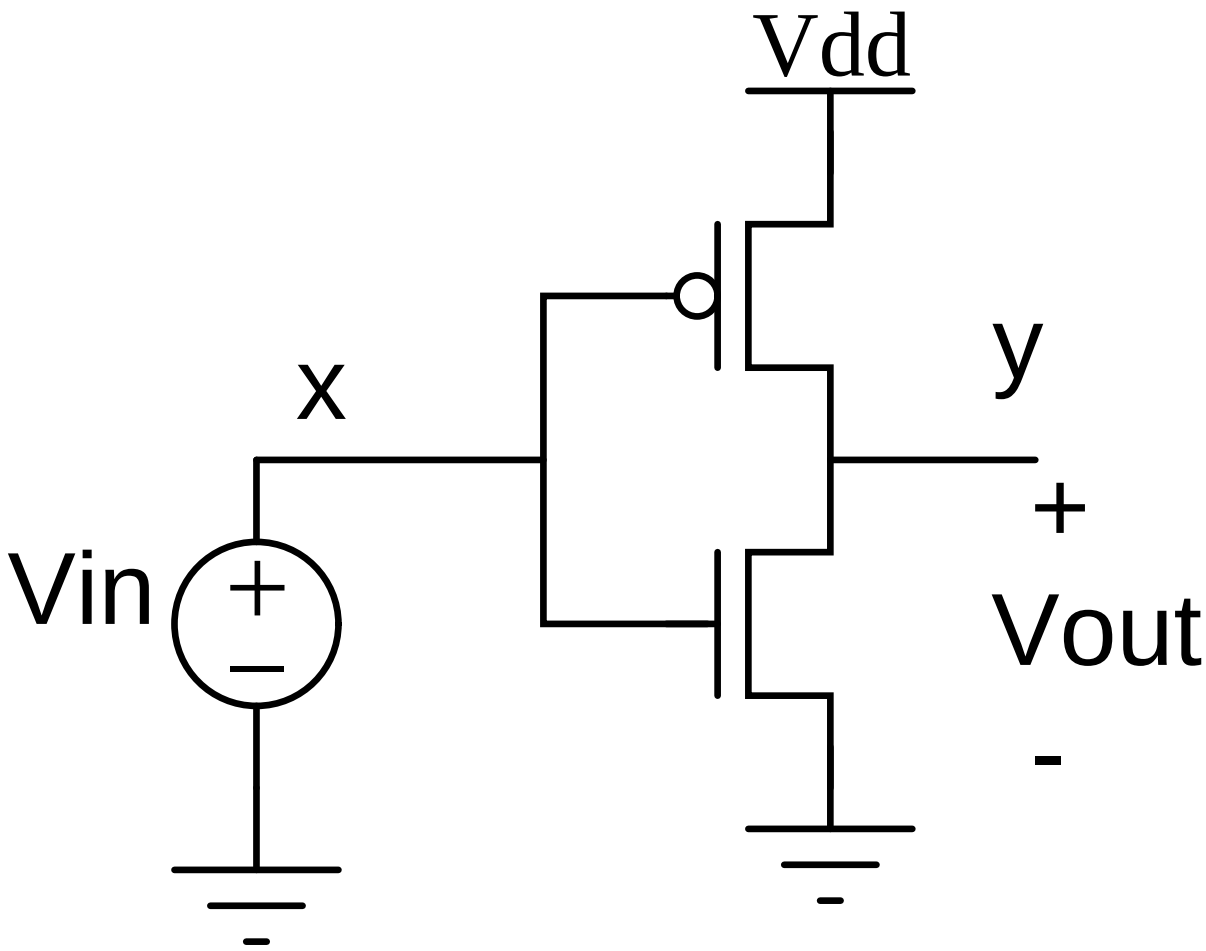

Figure: CMOS inverter transfer characteristic (with capactive load)

Inverter characteristics: Output characteristics

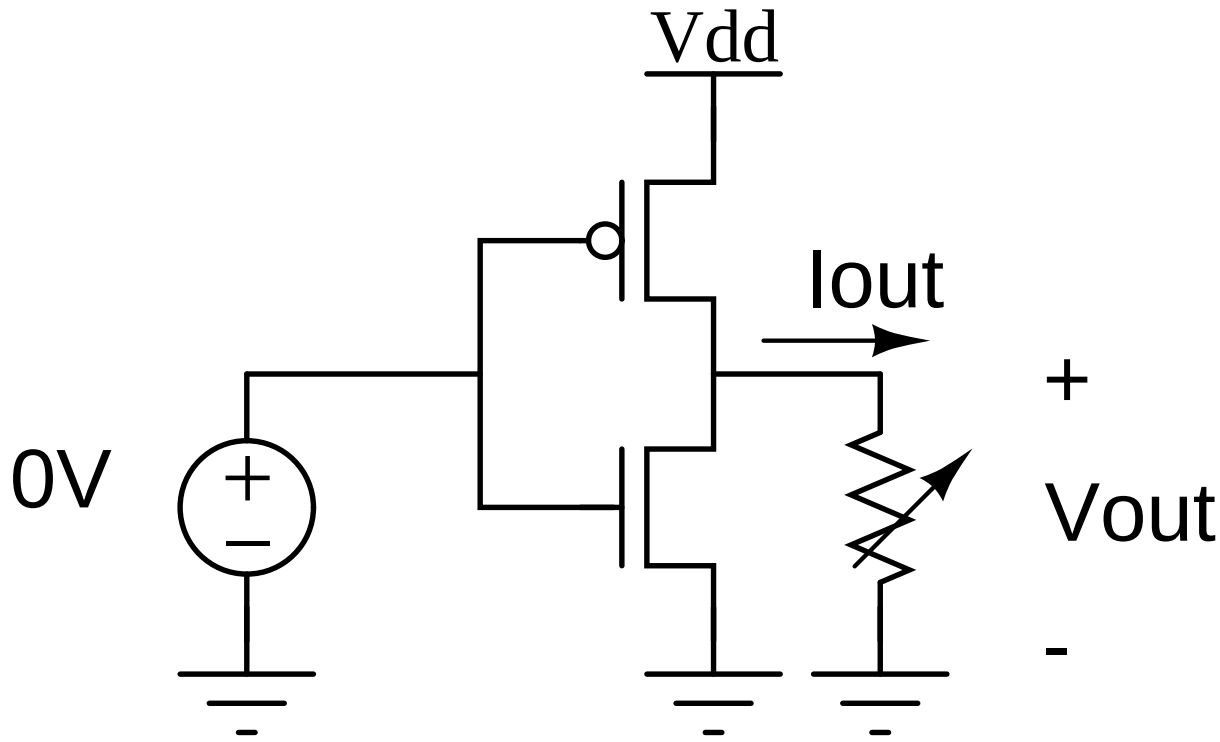

Figure: CMOS inverter output characteristic with input tied low

Inverter characteristics: Output characteristics

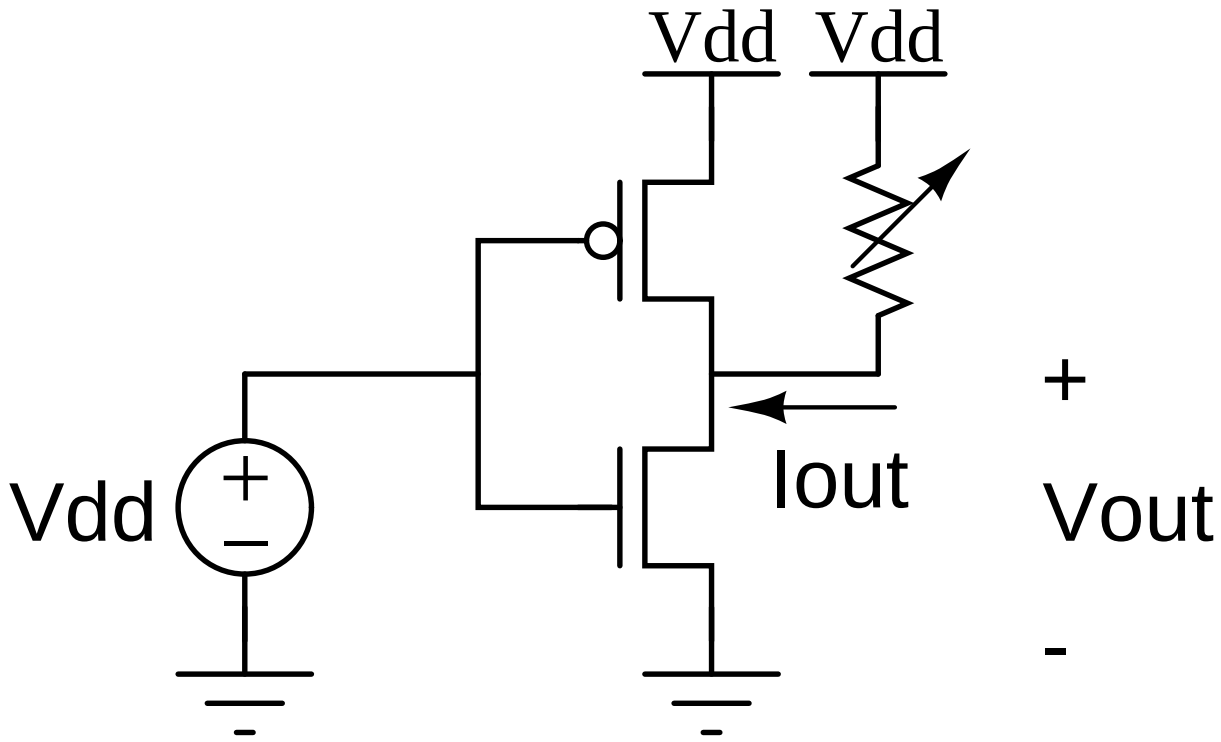

Figure: CMOS inverter output characteristic with input tied high

Inverter characteristics: Delay

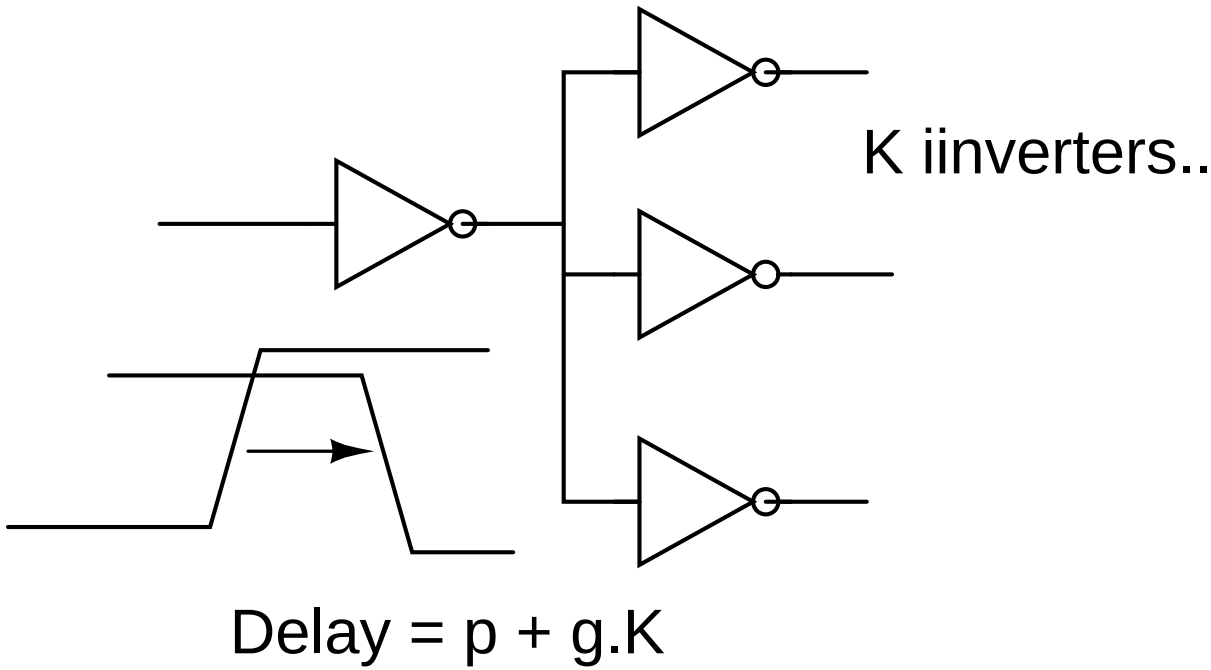

Figure: CMOS inverter delay

Inverter characteristics: I_{DD}

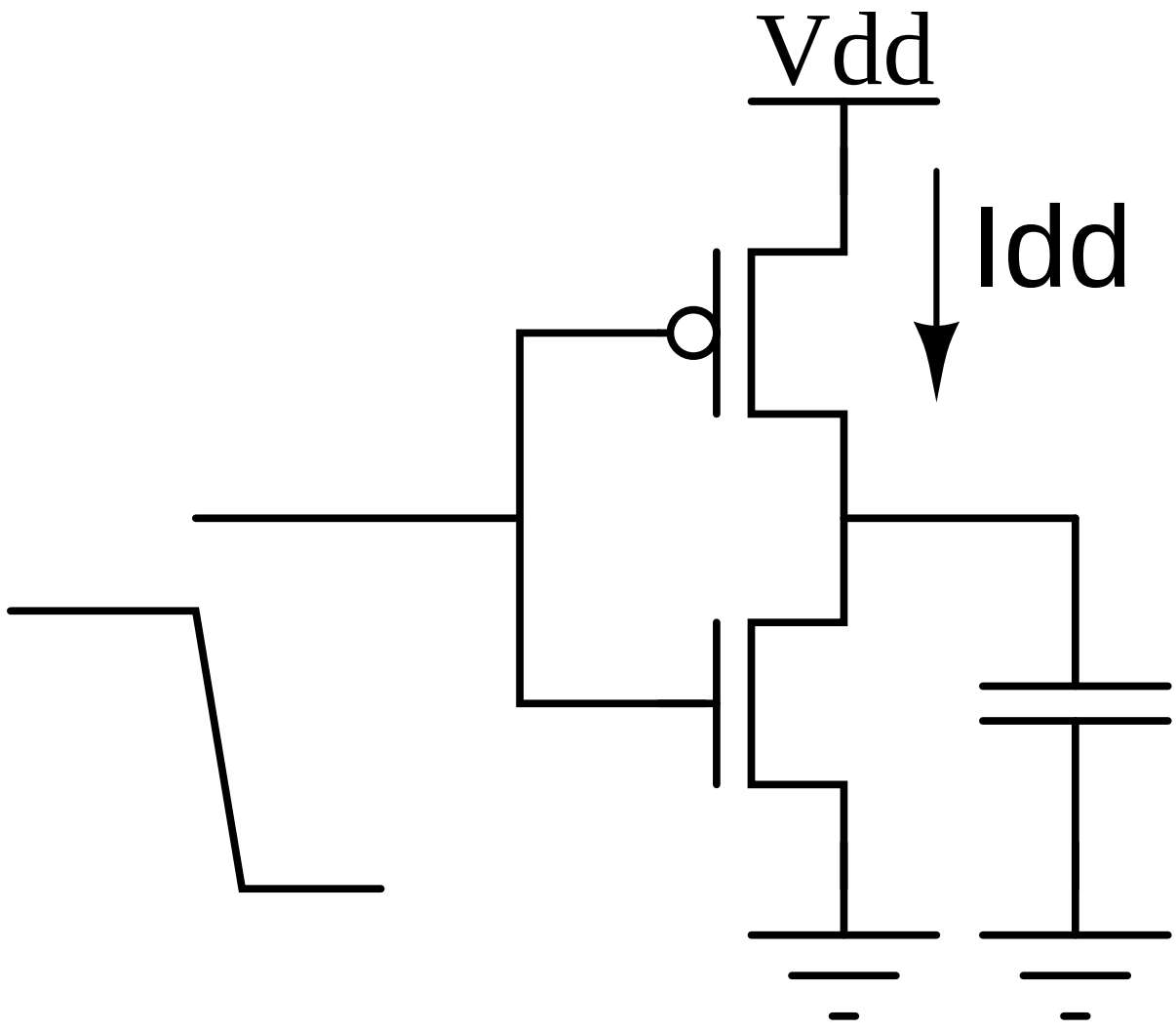

Figure: CMOS inverter power supply current

Other CMOS logic gates: NAND2

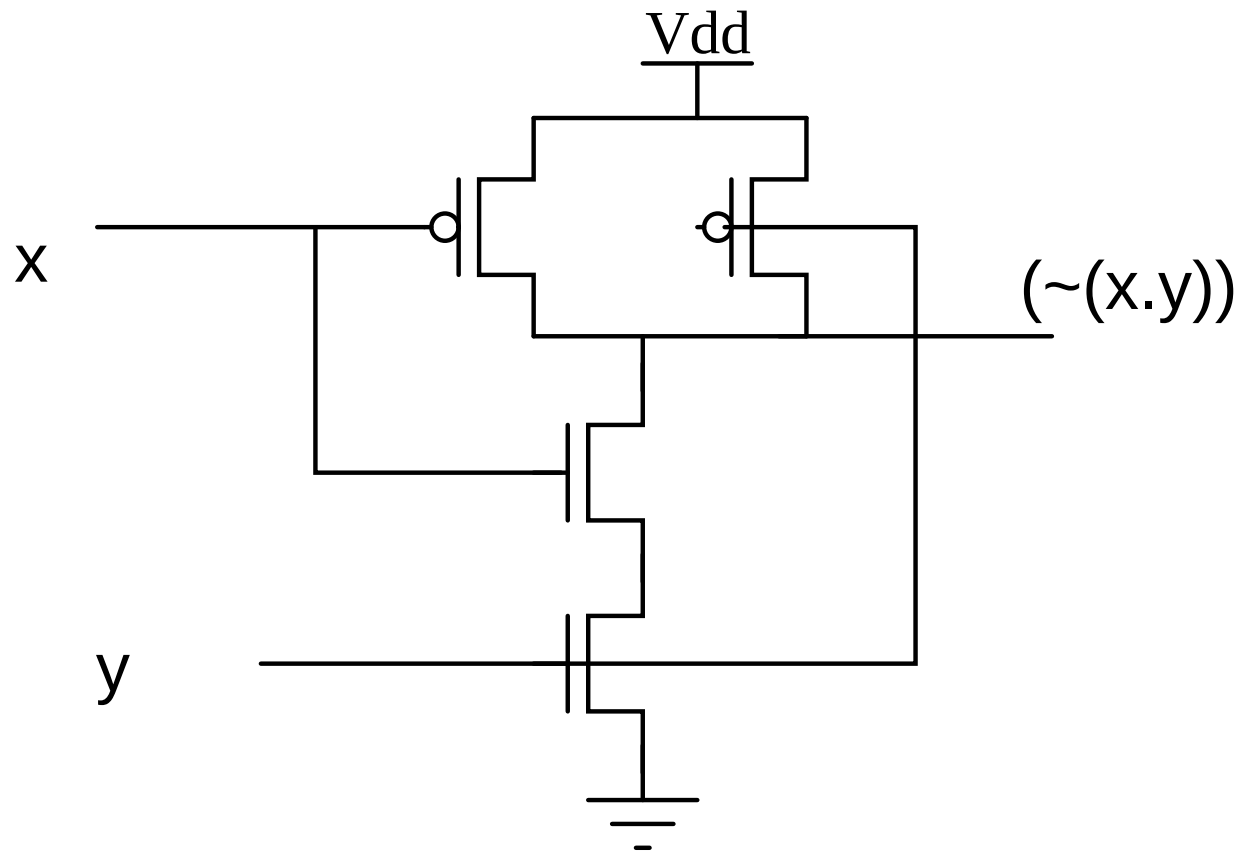

Figure: CMOS NAND2

Other CMOS logic gates: NOR2

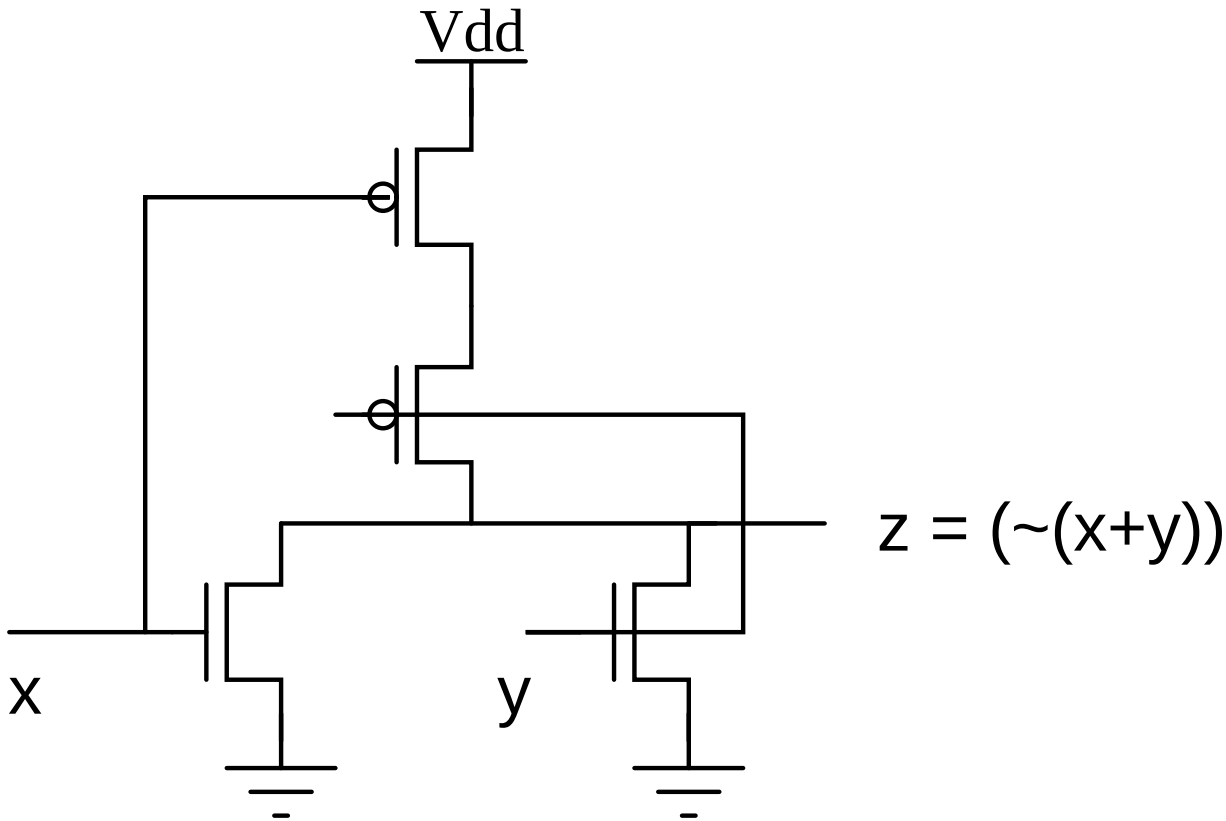

Figure: CMOS NOR2

Static Complementary CMOS logic gate construction

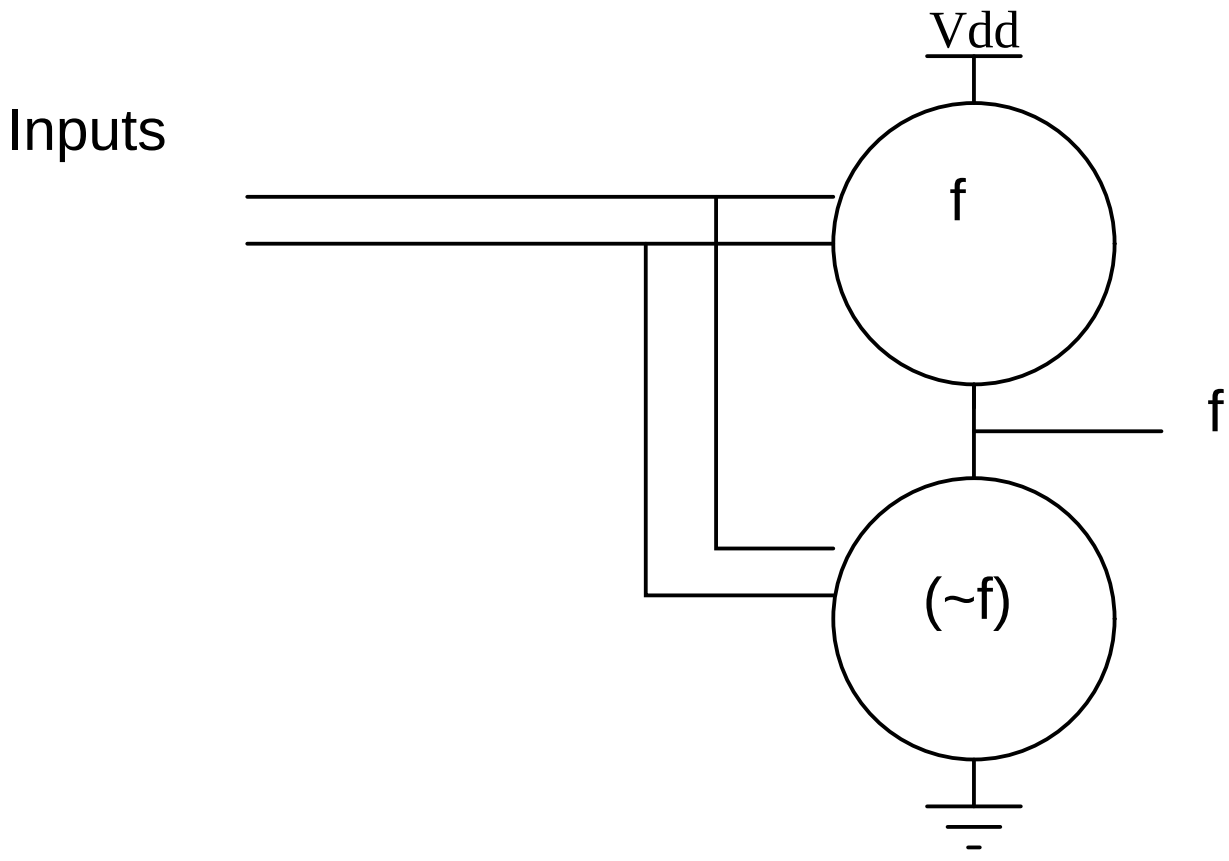

Figure: CMOS NOR2

Summary

- Easy to construct logic gates using CMOS technology.
- CMOS inverter is prototype for more complex CMOS gates.
- CMOS inverter characteristics
  - Transfer characteristic.
  - Output characteristics.
  - Delay characteristics.
  - Supply current characteristics.
- Characterization necessary for predicting delay, power dissipation, cost of final logic circuit.