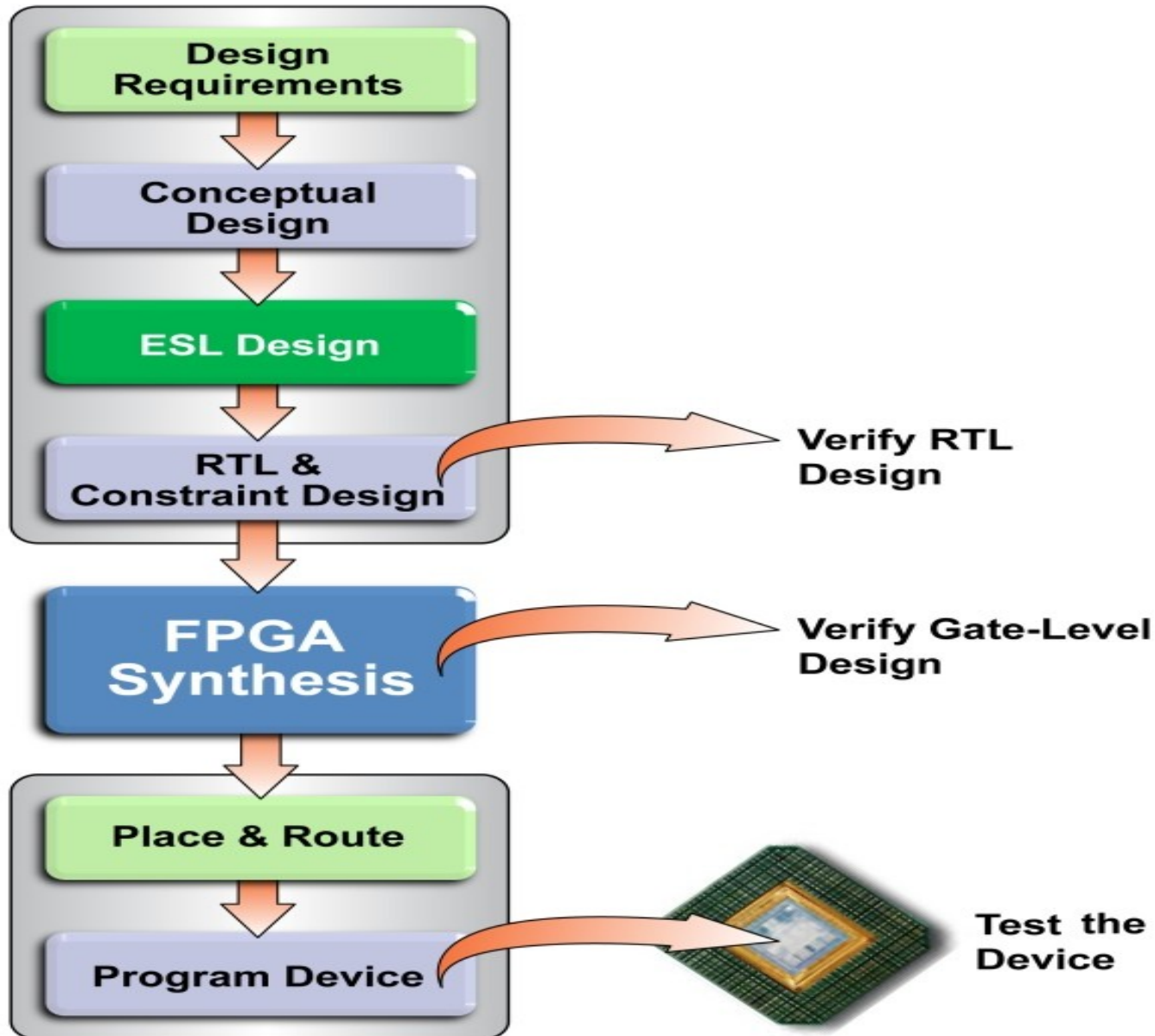


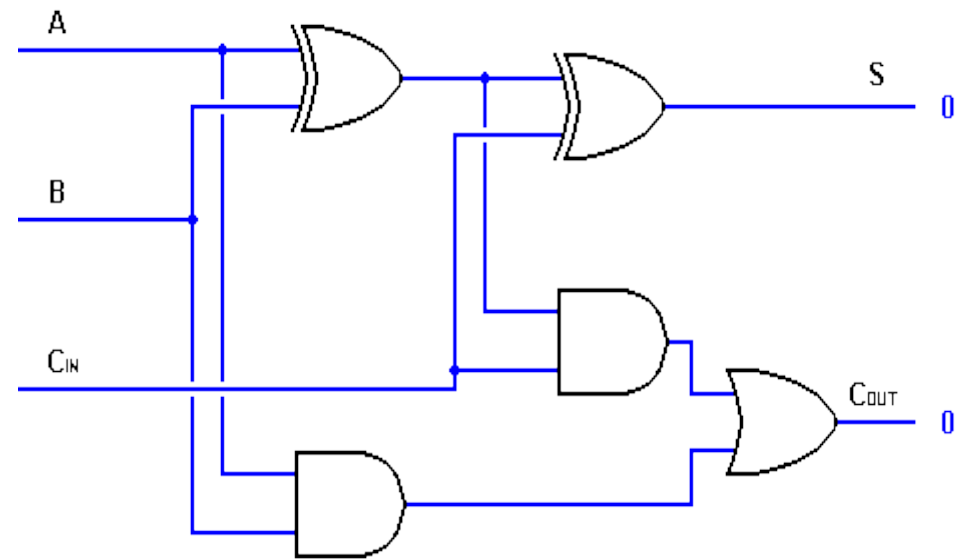
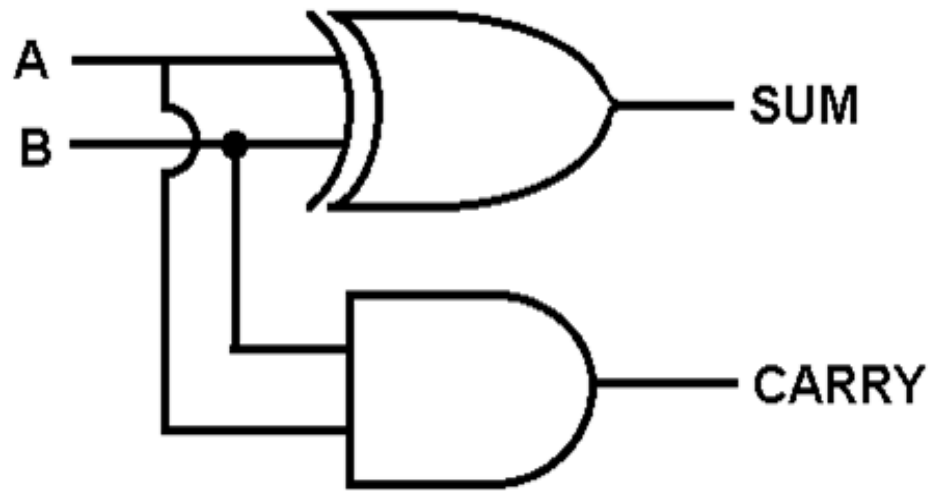
Digital Design with Quartus

by
Varun Warriar

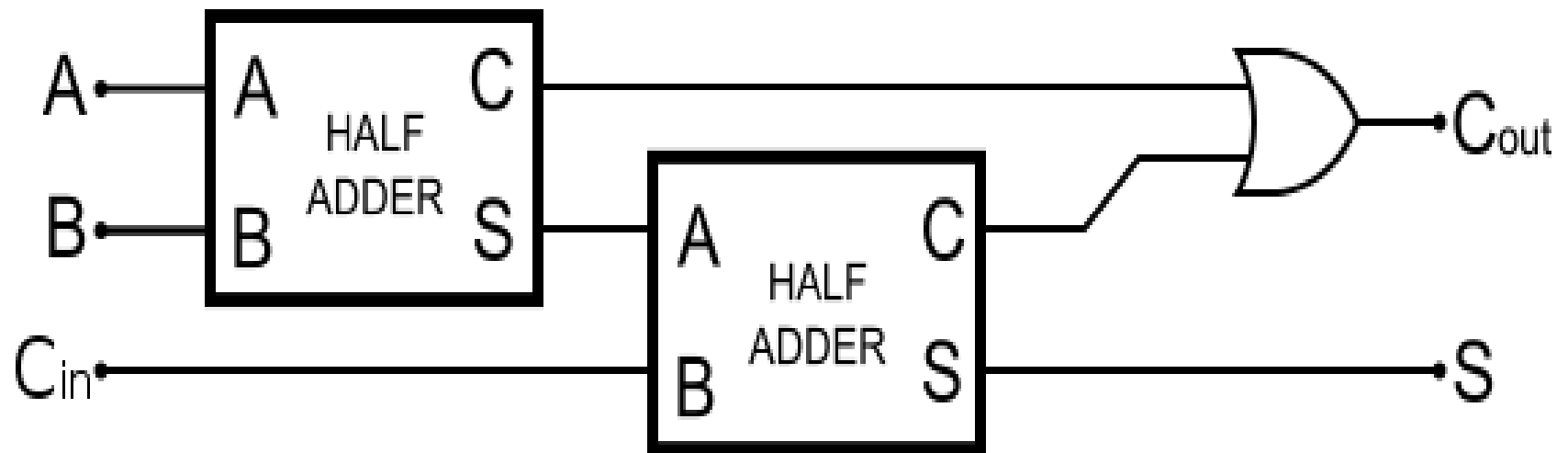
Design Flow



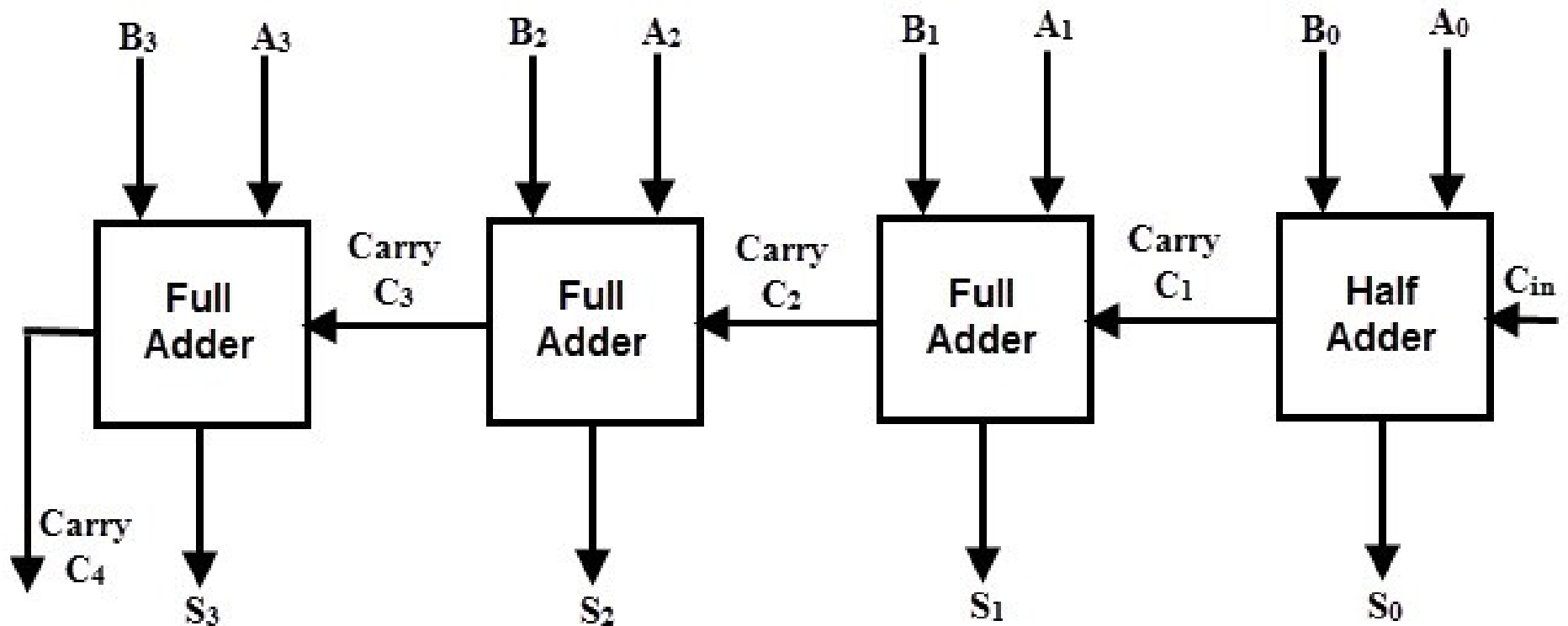
Half Adder & Full Adder



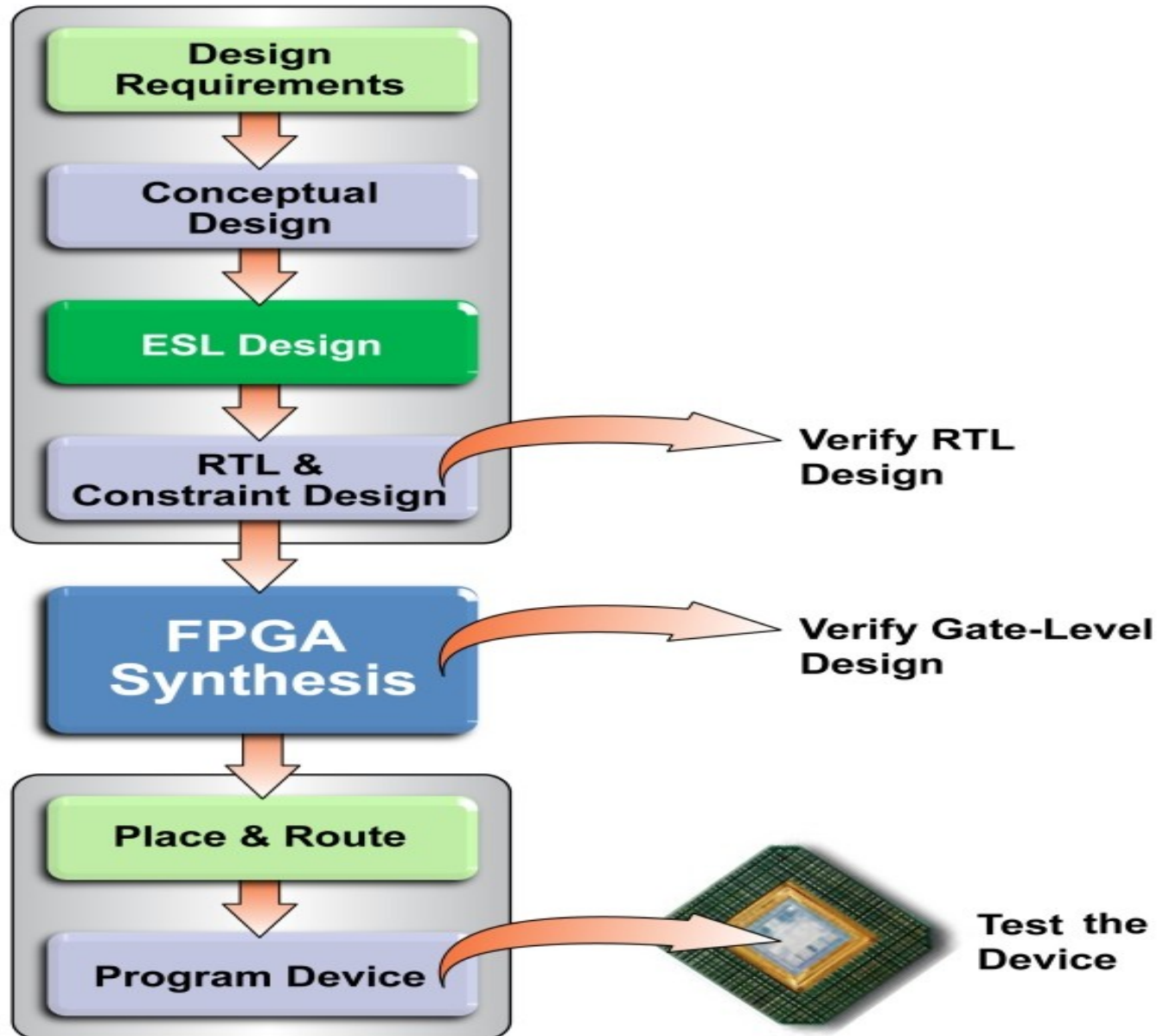
Full Adder – Another Approach



4 bit Adder – Structural Modelling

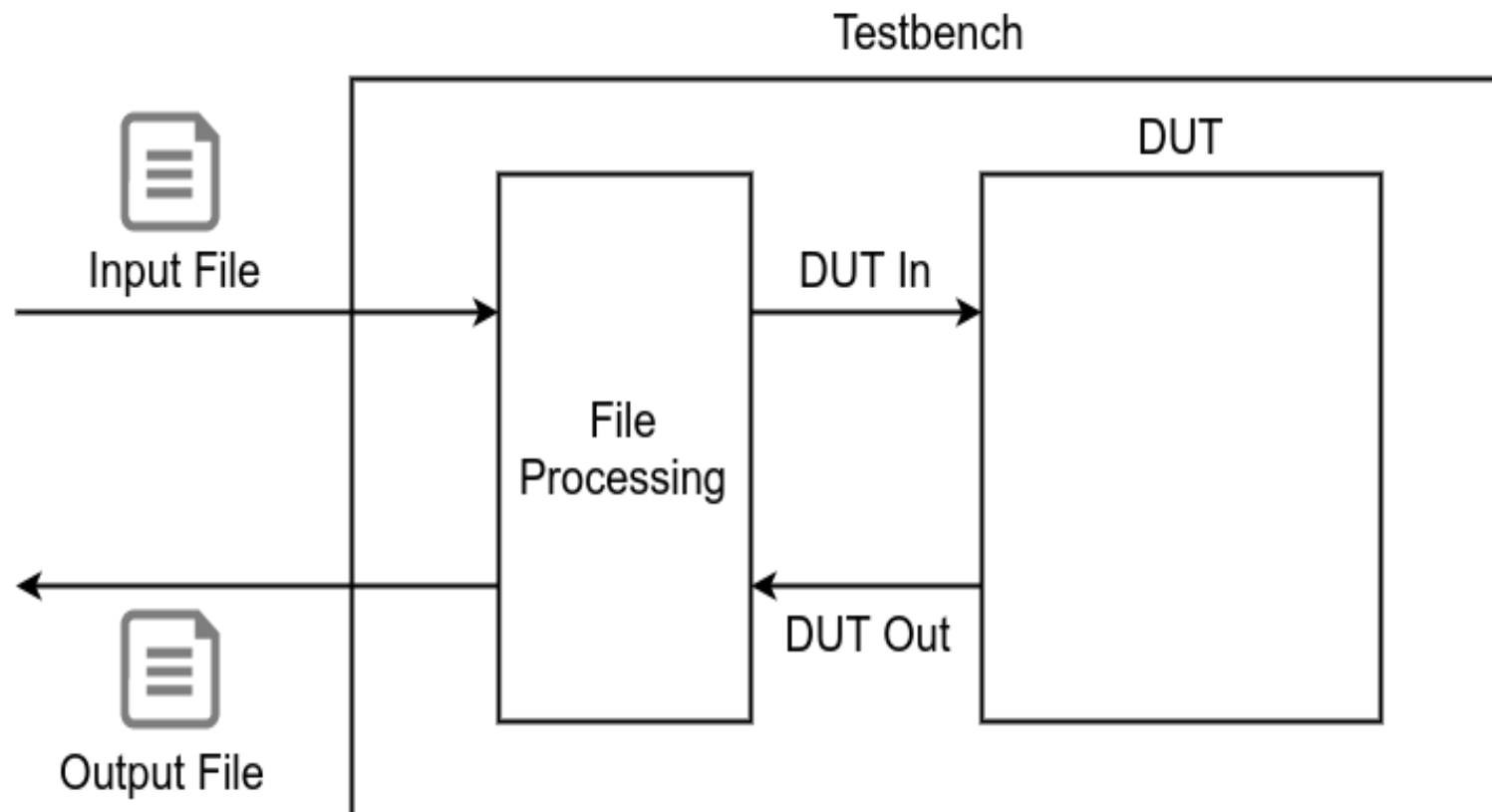


Design Flow

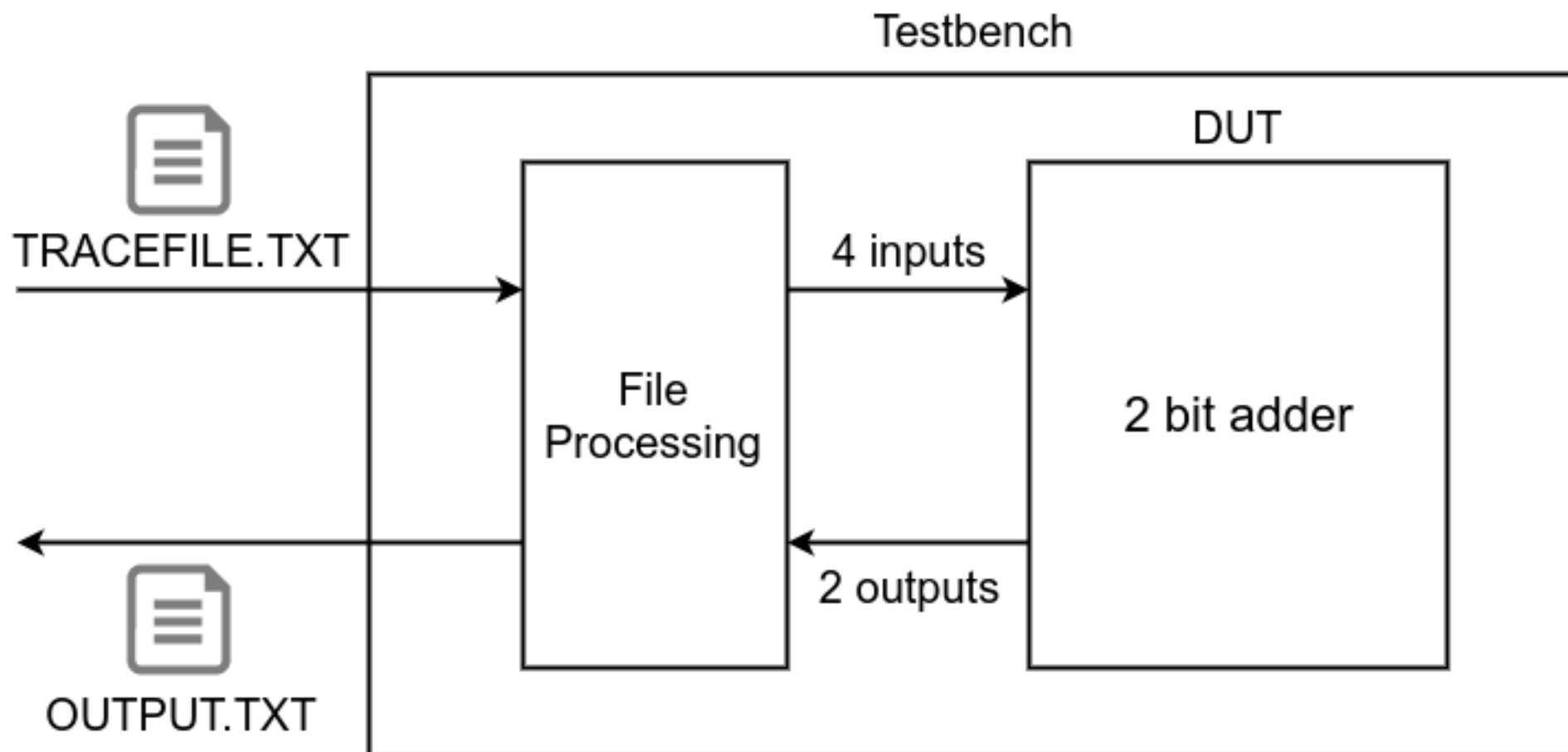


Design Verification

- RTL Simulation
- Gate Level Simulation
- Test Benches



Two Bit Adder Example



Simulation Setup

Settings - two_bit_adder

Category: Device/Board...

- General
- Files
- Libraries
- ▼ IP Settings
 - IP Catalog Search Locations
 - Design Templates
- ▼ Operating Settings and Conditions
 - Voltage
 - Temperature
- ▼ Compilation Process Settings
 - Incremental Compilation
- ▼ EDA Tool Settings
 - Design Entry/Synthesis
 - Simulation**
 - Board-Level
- ▼ Compiler Settings
 - VHDL Input
 - Verilog HDL Input
 - Default Parameters
- TimeQuest Timing Analyzer
- Assembler
- Design Assistant
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- PowerPlay Power Analyzer Settings
- SSN Analyzer

Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: ModelSim-Altera

☐ Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: VHDL Time scale: 100 us

Output directory: simulation/modelsim

☐ Map illegal HDL characters ☐ Enable glitch filtering

Options for Power Estimation

☐ Generate Value Change Dump (VCD) file script Script Settings...

Design instance name:

More EDA Netlist Writer Settings...

NativeLink settings

☐ None

☒ Compile test bench: Test Benches...

☐ Use script to set up simulation:

☐ Script to compile test bench:

More NativeLink Settings... Reset

Buy Software OK Cancel Apply Help

Simulation Setup

Quartus Prime 16.1 Lite Edition

Category: Device/Board...

Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: ModelSim-Altera

☐ Run gate-level simulation automatically after compilation

Time scale: 100 us

Enable glitch filtering

Test Benches

Specify settings for each test bench.

Existing test bench settings:

| Name | op Level Modul | Design Instance | Run For | Test Bench File(s) |
|------|----------------|-----------------|---------|--------------------|
|------|----------------|-----------------|---------|--------------------|

New...
Edit...
Delete

☒ Compile test bench: Test Benches...

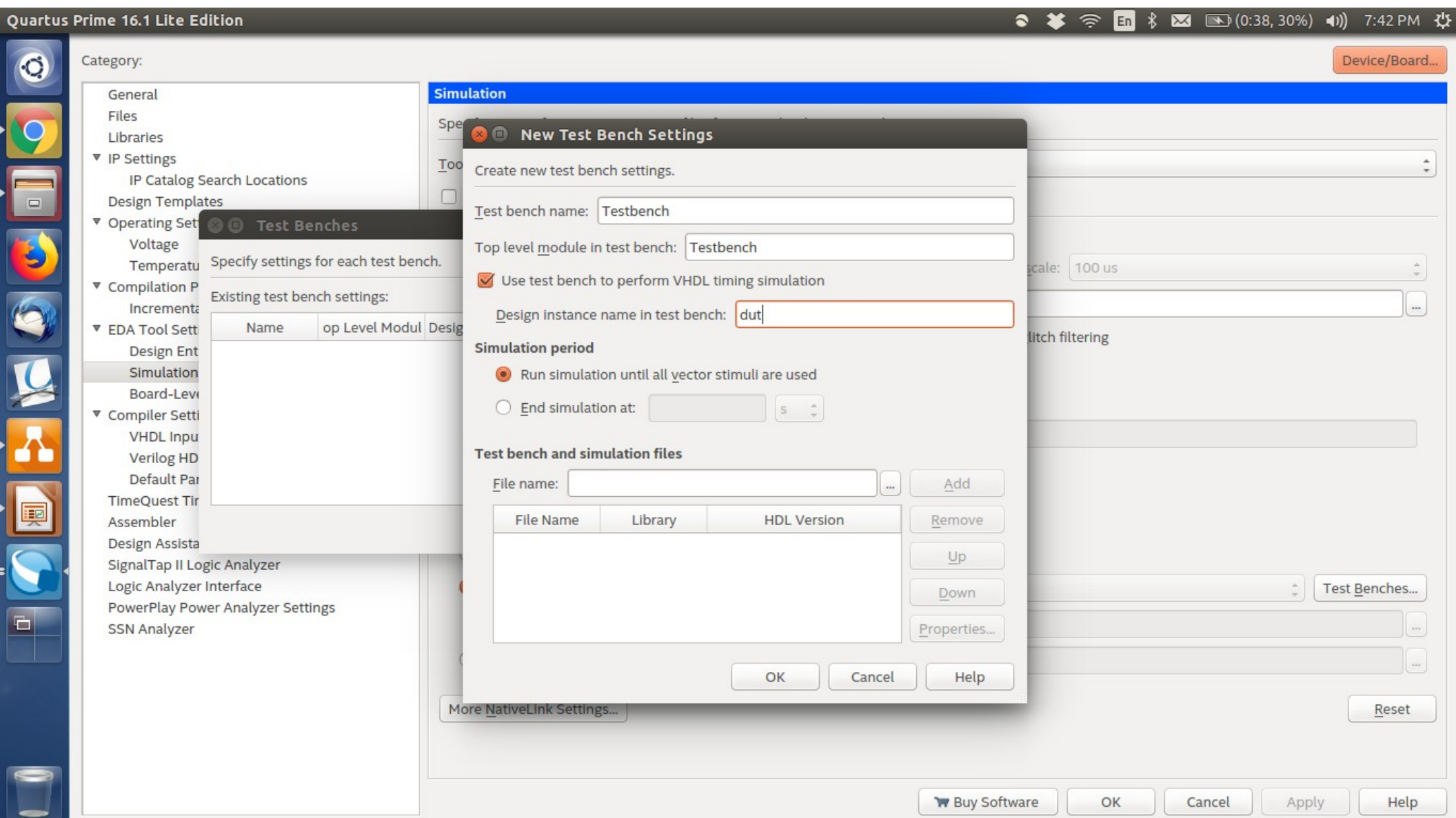
☐ Use script to set up simulation: ...

☐ Script to compile test bench: ...

More NativeLink Settings... Reset

Buy Software OK Cancel Apply Help

Simulation Setup



Simulation Setup

Quartus Prime 16.1 Lite Edition

Category:

- General
- Files
- Libraries
- ▼ IP Settings
 - IP Catalog Search Locations
- Design Templates
- ▼ Operating Set
- Voltage
- Temperatu
- ▼ Compilation P
- Increments
- ▼ EDA Tool Sett
- Design Ent
- Simulation
- Board-Lev
- ▼ Compiler Sett
- VHDL Inpu
- Verilog HD
- Default Pai
- TimeQuest Tir
- Assembler
- Design Assista
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- PowerPlay Power Analyzer Settings
- SSN Analyzer

Test Benches

Specify settings for each test bench.

Existing test bench settings:

| Name | op Level Modul | Design |
|------|----------------|--------|
|------|----------------|--------|

New Test Bench Settings

Create new test bench settings.

Test bench name: Testbench

Top level module in test bench: Testbench

☒ Use test bench to perform VHDL timing simulation

Design instance name in test bench: dut

Simulation period

☒ Run simulation until all vector stimuli are used

☐ End simulation at: [] S

Test bench and simulation files

File name: [] Add

| File Name | Library | HDL Version |
|---------------|---------|-------------|
| Testbench.vhd | | Default |

Remove Up Down Properties...

OK Cancel Help

More NativeLink Settings...

Device/Board...

scale: 100 us

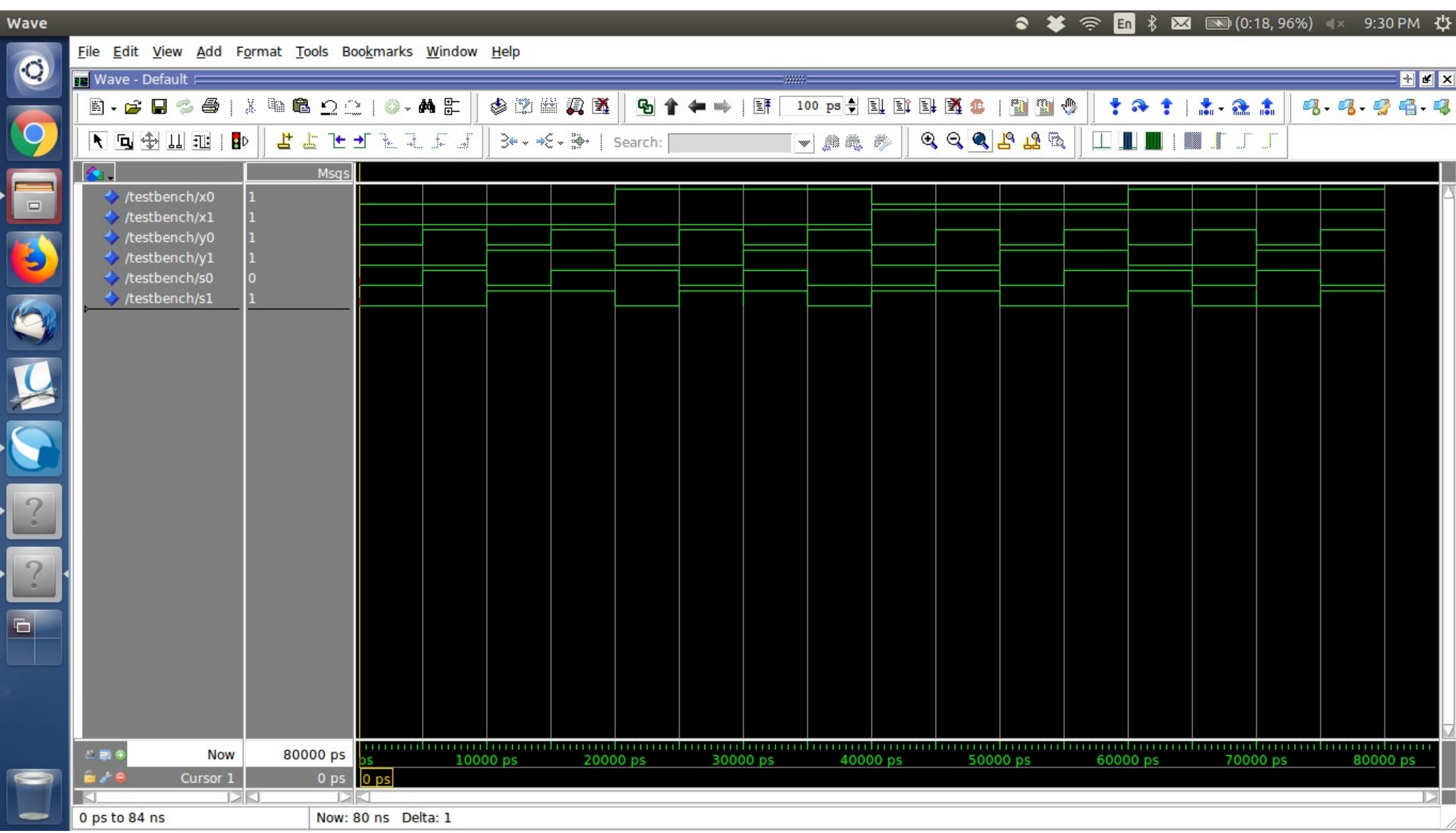
latch filtering

Test Benches...

Reset

Buy Software OK Cancel Apply Help

RTL Simulation



RTL Simulation

ModelSim - INTEL FPGA STARTER EDITION 10.5b

File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout AllColumns

sim - Default

| Instance | Design unit | Design unit type | Top Category | Visibility | Total cover |
|------------------|----------------|------------------|--------------|------------|-------------|
| testbench | testbench(...) | Architecture | DU Instance | +acc=<... | |
| dut | two_bit_ad... | Architecture | DU Instance | +acc=<... | |
| line_37 | testbench(...) | Process | - | +acc=<... | |
| standard | standard | Package | Package | +acc=<... | |
| textio | textio | Package | Package | +acc=<... | |
| std_logic_1164 | std_logic_1... | Package | Package | +acc=<... | |
| ee224_components | ee224_com... | Package | Package | +acc=<... | |

Objects

| Name | Value | Kind | Mode |
|------|-------|--------|----------|
| x0 | 1 | Signal | Inter... |
| x1 | 1 | Signal | Inter... |
| y0 | 1 | Signal | Inter... |
| y1 | 1 | Signal | Inter... |
| s0 | 0 | Signal | Inter... |

Processes (Active)

| Name | Type (filtered) | State | Order | Parent Path | Class Info |
|------|-----------------|-------|-------|-------------|------------|
|------|-----------------|-------|-------|-------------|------------|

Library x sim x

Transcript

```
# Loading work.half_adder(ha_arch)
# Loading work.xor2(behave)
# Loading work.and_2(behave)
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
** Note: SUCCESS, all tests passed.
#   Time: 80 ns  Iteration: 0  Instance: /testbench
#
# stdin: <EOF>
```

VSIM 2>

Gate Level Simulation -Failure

Quartus Prime 16.1 Lite Edition

File Edit View Project Assignments Processing Tools Window Help

two_bit_adder

Project Navigator Hierarchy

Entity:Instance

- MAX V: 5M1270ZT144C5
 - two_bit_adder
 - full_adder:fa1
 - XOR2:cy_x
 - half_adder:ha1
 - AND_2:cy_a
 - XOR2:sum_x

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming file)
- TimeQuest Timing Analysis

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

<<Filter>>

| | |
|-----------------------|---|
| Flow Status | Successful - Wed Jan 24 19:45:47 2018 |
| Quartus Prime Version | 16.1.0 Build 196 10/24/2016 SJ Lite Edition |
| Revision Name | two_bit_adder |
| Top-level Entity Name | two_bit_adder |
| Family | MAX V |
| Device | 5M1270ZT144C5 |
| Timing Models | Final |
| Total logic elements | 2 / 1,270 (< 1 %) |
| Total pins | 6 / 114 (5 %) |

EDA Gate Level Simulation

Timing model: "Slow Model" Run

IP Catalog

Installed IP

- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Processors and Peripherals
 - University Program

Search for Partner IP

Messages

All

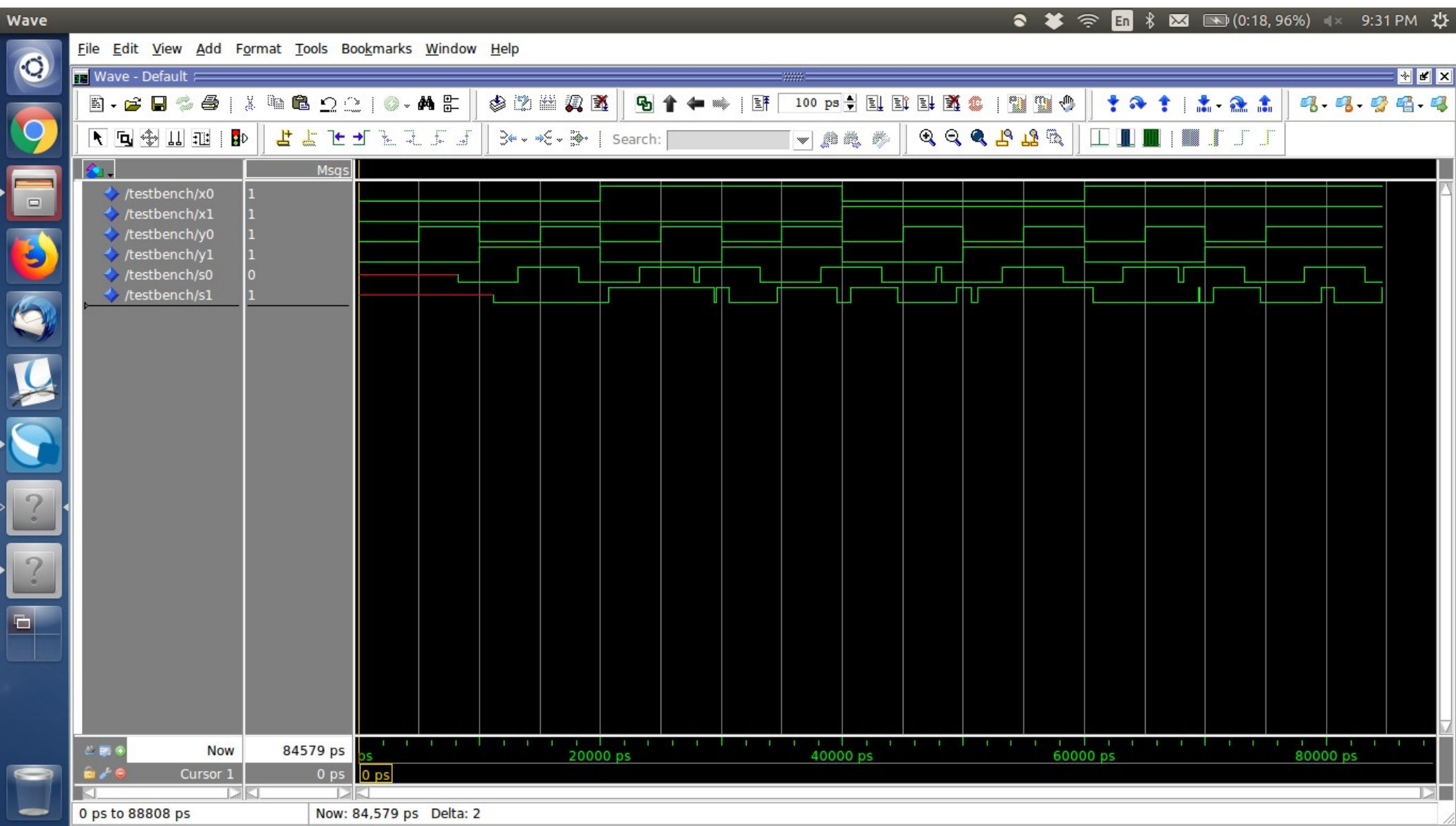
Type ID Message

- 22036 Successfully launched NativeLink simulation (quartus_sh -t "/home/varun/intelFPGA_lite/16.1/quartus/common/tcl/internal/nativeLink/qnativesim.tcl")
- 22036 For messages from NativeLink execution see the NativeLink log file /home/varun/iitb/wel/digital_lab/2018/TwoBitAdder/two_bit_adder_nativeLink_simul
- 22036 Successfully launched NativeLink simulation (quartus_sh -t "/home/varun/intelFPGA_lite/16.1/quartus/common/tcl/internal/nativeLink/qnativesim.tcl")
- 22036 For messages from NativeLink execution see the NativeLink log file /home/varun/iitb/wel/digital_lab/2018/TwoBitAdder/two_bit_adder_nativeLink_simul

System (4) Processing (103)

100% 00:00:19

Gate Level Simulation -Failure



Gate Level Simulation -Failure

ModelSim - INTEL FPGA STARTER EDITION 10.5b

File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout AllColumns

sim - Default

| Instance | Design unit | Design unit type | Top Category | Visibility | Total cover |
|------------------|------------------|------------------|--------------|------------|-------------|
| testbench | testbench(...) | Architecture | DU Instance | +acc=<... | |
| dut | two_bit_ad... | Architecture | DU Instance | +acc=<... | |
| line_37 | testbench(...) | Process | - | +acc=<... | |
| standard | standard | Package | Package | +acc=<... | |
| textio | textio | Package | Package | +acc=<... | |
| std_logic_1164 | std_logic_1... | Package | Package | +acc=<... | |
| vital_timing | vital_timing | Package | Package | +acc=<... | |
| vital_primitives | vital_primiti... | Package | Package | +acc=<... | |
| maxv_atom_pack | maxv_atom... | Package | Package | +acc=<... | |
| maxv_components | maxv_com... | Package | Package | +acc=<... | |
| std_logic_arith | std_logic_ar... | Package | Package | +acc=<... | |

Objects

| Name | Value | Kind | Mode |
|------|-------|--------|----------|
| x0 | 1 | Signal | Inter... |
| x1 | 1 | Signal | Inter... |
| y0 | 1 | Signal | Inter... |
| y1 | 1 | Signal | Inter... |
| s0 | 0 | Signal | Inter... |

Processes (Active)

| Name | Type (filtered) | State | Order | Parent Path | Class Info |
|------|-----------------|-------|-------|-------------|------------|
|------|-----------------|-------|-------|-------------|------------|

Library x sim x

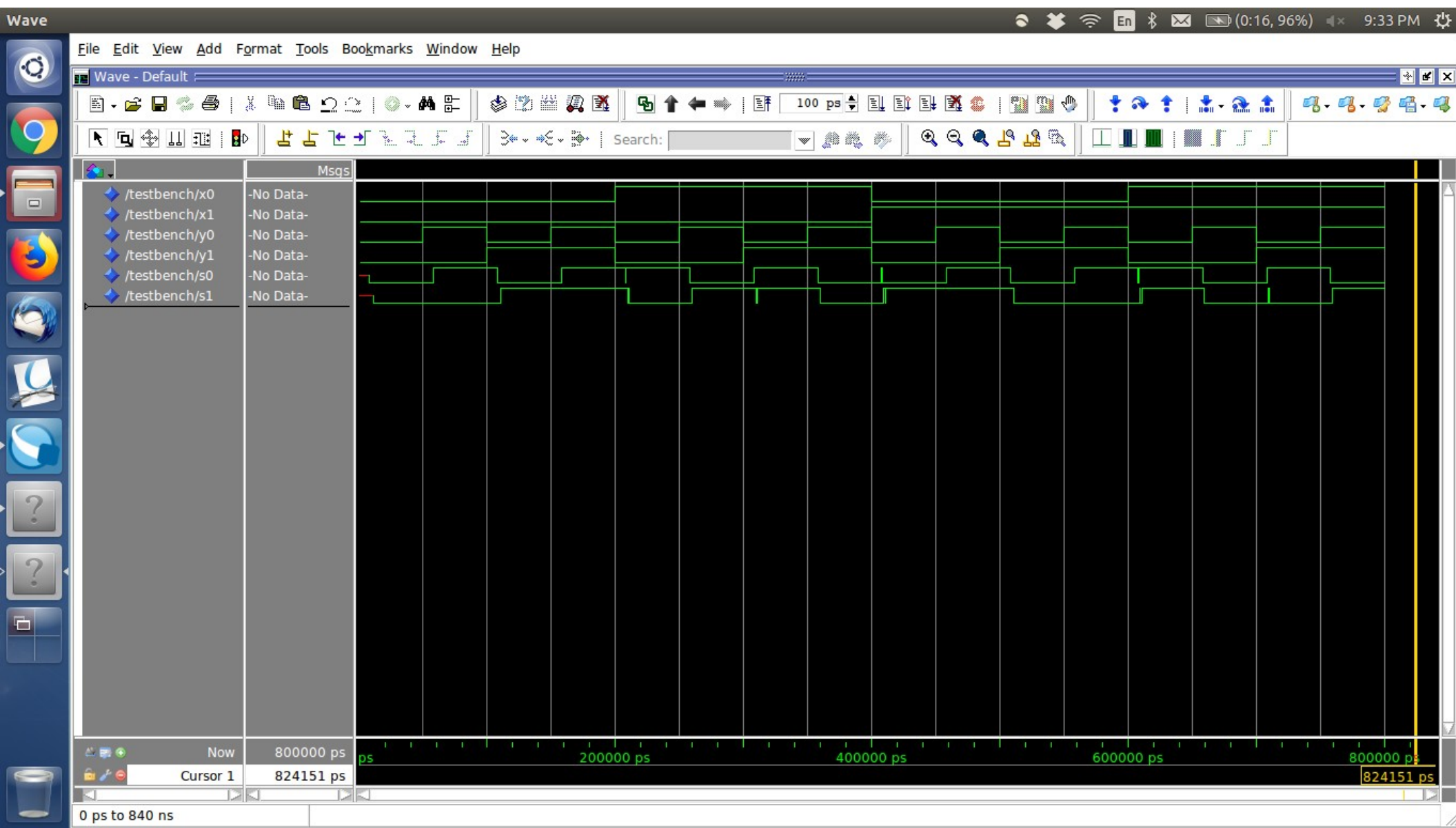
Transcript

```
# Loading timing data from two_bit_adder_vhd.sdo
# ** Note: (vsim-3587) SDF Backannotation Successfully Completed.
#   Time: 0 ps   Iteration: 0   Instance: /testbench File: /home/varun/iitb/wel/digital_lab/2018/TwoBitAdder/Testbench.vhd
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ** Error: FAILURE, some tests failed.
#   Time: 80 ns   Iteration: 0   Instance: /testbench
#
# stdin: <EOF>
```

VSIM 2>

Now: 84,579 ps Delta: 2 Package

Gate Level Simulation - Success



Gate Level Simulation - Success

ModelSim - INTEL FPGA STARTER EDITION 10.5b

File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout AllColumns

sim - Default

| Instance | Design unit | Design unit type | Top Category | Visibility | Total cover |
|------------------|------------------|------------------|--------------|------------|-------------|
| testbench | testbench(...) | Architecture | DU Instance | +acc=<... | |
| dut | two_bit_ad... | Architecture | DU Instance | +acc=<... | |
| line_37 | testbench(...) | Process | - | +acc=<... | |
| standard | standard | Package | Package | +acc=<... | |
| textio | textio | Package | Package | +acc=<... | |
| std_logic_1164 | std_logic_1... | Package | Package | +acc=<... | |
| vital_timing | vital_timing | Package | Package | +acc=<... | |
| vital_primitives | vital_primiti... | Package | Package | +acc=<... | |
| maxv_atom_pack | maxv_atom... | Package | Package | +acc=<... | |
| maxv_components | maxv_com... | Package | Package | +acc=<... | |
| std_logic_arith | std_logic_ar... | Package | Package | +acc=<... | |

Objects

| Name | Value | Kind | Mode |
|------|-----------|--------|----------|
| x0 | -No Data- | Signal | Inter... |
| x1 | -No Data- | Signal | Inter... |
| y0 | -No Data- | Signal | Inter... |
| y1 | -No Data- | Signal | Inter... |
| s0 | -No Data- | Signal | Inter... |

Processes (Active)

| Name | Type (filtered) | State | Order | Parent Path | Class Info |
|------|-----------------|-------|-------|-------------|------------|
|------|-----------------|-------|-------|-------------|------------|

Library x sim x

Transcript

```
# Loading timing data from two_bit_adder_vhd.sdo
# ** Note: (vsim-3587) SDF Backannotation Successfully Completed.
#   Time: 0 ps  Iteration: 0  Instance: /testbench  File: /home/varun/iitb/wel/digital_lab/2018/TwoBitAdder/Testbench.vhd
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ** Note: SUCCESS, all tests passed.
#   Time: 800 ns  Iteration: 0  Instance: /testbench
#
# stdin: <EOF>
```

VSIM 2>

Now: 800 ns Delta: 1 sim:/testbench

- Device

- 5M1270ZT144C5

JTAG Commands

- JTAG

- cable ft2232 vid=0x0403 pid=0x6010

- detect

- svf <filename> progress