EE204 - Design Challenge#1

Design Rules

Design a differential amplifier having a maximum of two stages using ngspice with the following constraints:

I. You can **ONLY** use pMOS and nMOS from TSMC model files already uploaded.
II. The maximum (minimum) W/L you can use is 100 (1) for both the nMOS and pMOS.
III. You can not put two transistors in parallel to increase effective W/L.
IV. There is no limit on the number of transistors, resistors (any value), capacitors (any value) you use.
V. Only two power supplies are available V_{DD} = +15 V and V_{SS} = -15 V.
VI. The final output will be taken with respect to the ground only (single ended output).

Winning criteria

I. The design with the maximum differential gain (A_{DM}) will be the winner.
II. If A_{DM} is the same, the design with minimum number of resistors (n) will be the winner.
III. If A_{DM} and n are the same, the design with the minimum number capacitors (m) will the winner.
IV. If ADM, n and m are the same, the design with the maximum 3 dB bandwidth will be the winner.

Reward

There will be an extra 10 credits on top of the total 100 credits. There will be just one winner.

Rule for claiming the reward

I. You have to make your first entry by 24th Feb. You are not allowed to continue unless first entry is made. Link to make your entry: https://docs.google.com/spreadsheets/d/1mD4JELCXOOFPQqffDn5l4-0L-L_wbdSkqdk_B7KWxrg/edit?usp=sharing
II. Last entry allowed 1st Mar. Also, claim your final performance details through Moodle.
III. Demonstration of your design/claim in front of the class.

For healthy competition, I expect you to share your design performance through the google sheet so that others get inspired.

Anyone found using unfair means or cheating will be penalized with -10 credit.