VLSI - Verilog

Very-Large-Scale Integration (VLSI) Is The Process Of Creating Integrated Circuits By Combining Thousands Of Transistors Into A Single Chip. This Is The Field Which Involves Packing More And More Logic Devices Into Smaller And Smaller Areas. VLSI Circuits Are Everywhere ... Your Computer, Your Car, Your Brand New State-Of-The-Art Digital Camera, The Cell-Phones, And Whatever You Have.

Topics to be Covered:

Digital Design

Logic Gates

Combination Logic

Synchronous Sequential Logic

Asynchronous Sequential Logic

Register and Counters

Memory and Programmable Logic

Verilog

Introduction of HDL

Hierarchical Modeling Concepts

Basic Concepts

Modules and Ports

Gate- Level Modeling

Dataflow Modeling

Behavioral Modeling

Task and Functions

Timing and Delays

Switch- Level Modeling

User- Defined Primitive

Test Bench Simulation

Logical Synthesis

Lab Session and Projects

AND, OR, NOR, XOR and NOT Gate

Half Adder

Full Adder

Half Subtractor

Full Subtractor

Encoder

MUX

Asynchronous Rest MUX

Synchronous MUX

Decoder

Comparator

Priority Encoder

Asynchronous Reset D Flip Flop

Asynchronous Reset T Flip Flop

Synchronous D Flip Flop

Synchronous T Flip Flop

Asynchronous Reset JK Flip Flop

Synchronous JK Flip Flop

Up Counter

Down Counter

Up and Down Counter

Divide by N Counter

Parallel Loadable Counter

Ripple Counter

Ring Counter

Shift Register

Duration: The duration of this workshop will be two consecutive days, with 6-7 hours session each day in a total of 12-14 hours.

Eligibility: It\'s a basic level workshop so there are no prerequisites. Anyone interested, can join this workshop.

Fee: Rs. 1200/-(inclusive of all Taxes) per participant.