EE224 Handout
Construction of a D Flip-flop

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In this write-up we summarize the construction of an edge triggered D flip-flop, starting from logic gates, moving on to level triggered latches and ending with an edge triggered flip-flop. We will also quantify the setup time, hold time and delays of these circuits.

1 A memory element

if we do not have any loop then we can see that the output will be the function of current input not the past input

To build a memory element, we must have a combinational loop in a logic circuit (why?). The simplest such circuit is the one shown in Figure 1. This circuit has two stable states: $Q = 1, \overline{Q} = 0$ and $Q = 0, \overline{Q} = 1$. To make the memory element usable, we need a mechanism to force values into the memory element. This can be done by using the SR-bistable circuit shown in Figure 2, in which Q and $\overline{Q}$ can be controlled using the inputs $\overline{S}, \overline{R}$.

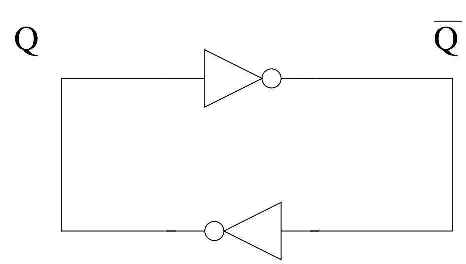

Figure 1: Back-to-back inverter loop

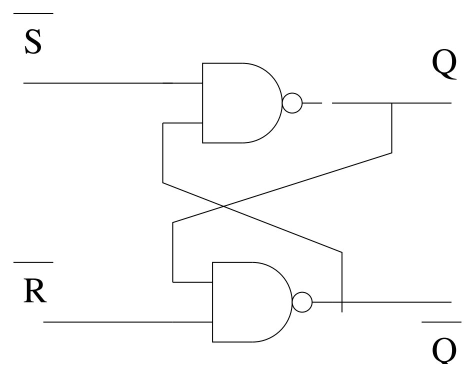

Figure 2: SR Bi-stable

In the SR-bistable, we observe the following *excitation table*:

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Q_{last}	$\overline{Q}_{last}$

To force the state $Q = 0, \overline{Q} = 1$, we make $\overline{S} = 1, \overline{R} = 0$ and to force the state $Q = 1, \overline{Q} = 0$, we make $\overline{S} = 0, \overline{R} = 1$. To hold the current state, we make $\overline{S} = \overline{R} = 1$. The input combination $\overline{S} = \overline{R} = 0$ is not used because if we go from this input combination to the hold input combination $\overline{S} = \overline{R} = 1$, the values at Q, $\overline{Q}$ are unpredictable (they depend on the relative delays of the two NAND gates).

To summarize, the SR-bistable allows us to store a bit of information using a pair of controlling signals $\overline{S}$ and $\overline{R}$.

How about the timing of the latch? To force $Q = 1$, we must make $\overline{S} = 0$ and $\overline{R} = 1$. For how long must we hold the forcing input $\overline{S} = 1$? We must hold it low until $\overline{Q}$ becomes 0, because after this happens, the output of the upper NAND gate remains 1 even if we make $\overline{S} = \overline{R} = 1$. Thus, the minimum duration for which $\overline{S}$ must be held low in order to force $Q = 1$ is $(d_1 + d_2)$.

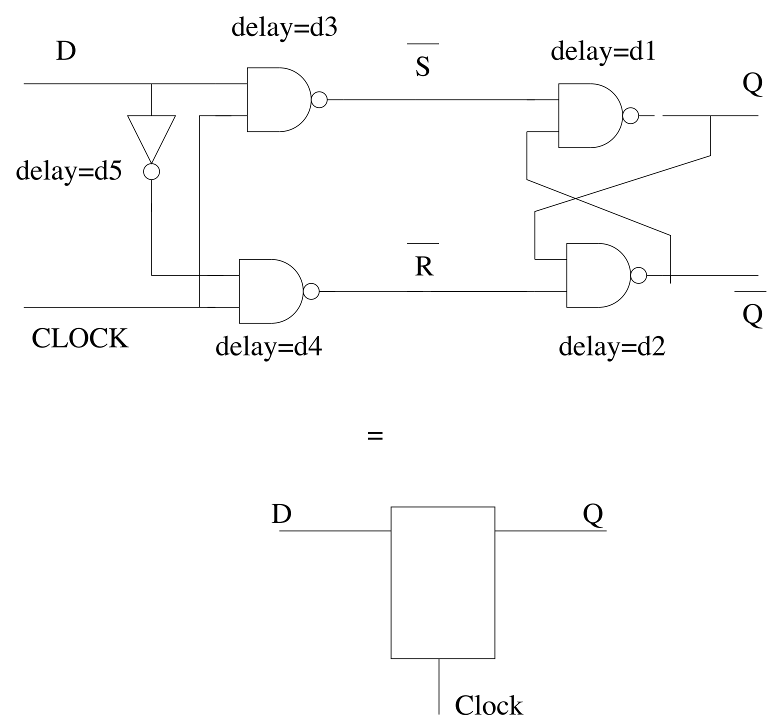

Figure 3: Positive level triggered latch

2 Level triggered latches

From the SR-bistable, we can construct a simple clocked memory circuit known as the positive level triggered D latch (see Figure 3). In this latch it is easy to see that if $Clock = 1$, then $Q = D$, and if $Clock = 0$, then $Q = Q_{last}$.

How do we characterize the timing of this latch? First of all we observe that the sampling edge is the falling edge of clock. Thus, we will calculate setup and hold times relative to the falling edge of the clock.

- If we wish to force $Q = 1$, D must be held 1 long enough while clock is 1. When $D = Clock = 1$, we will have $\overline{S} = 0$ which will make $Q = 1$. But to ensure that Q stays 1 we must check that $\overline{S}$ stays low for at least $d_1 + d_2$ units of time. That is, D and $Clock$ must both be 1 for at least $d_1 + d_2$ units of time. See Figure 4 for a visualization.

- If we wish to force $Q = 0$, $\overline{D}$ must be held 1 long enough while clock

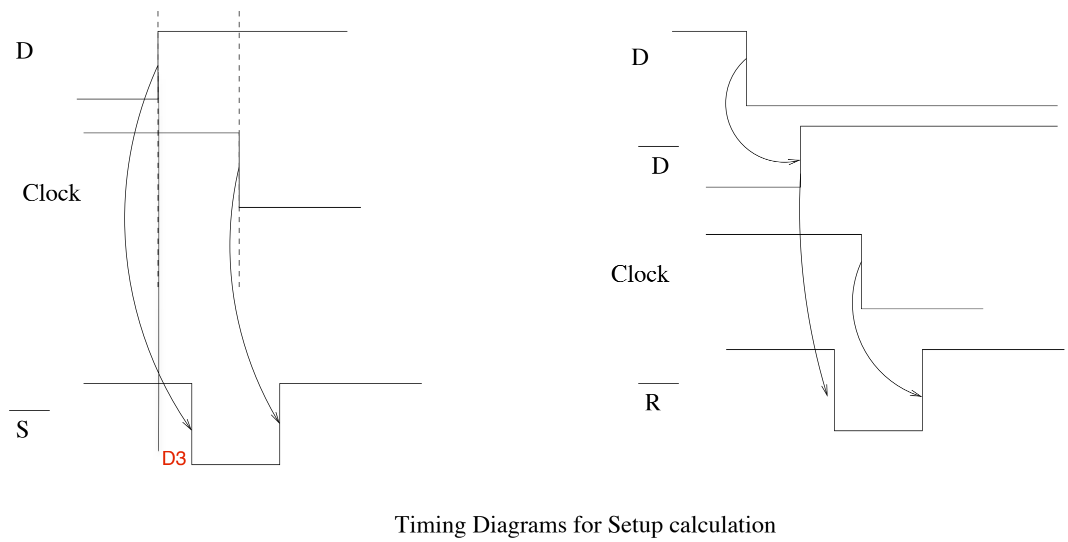

Figure 4: Timing diagram for setup calculation

is 1. In fact, we need to ensure that $\overline{D} = 0$ and $Clock = 1$ for at least $d_1 + d_2$ units of time. But $\overline{D}$ is a delayed version of D (delay = d_5). Thus, to force $Q = 0$, we must ensure that $D = 0$ and $Clock = 1$ for $d_1 + d_2 + d_5$ units of time. See Figure 4 for a visualization.

From this discussion, we conclude that if we change D and if we wish that this change is to sampled correctly into the latch, then we must allow a setup time of $d_1 + d_2 + d_5$ (in the worst case).

How about the hold time? We observe that as soon as $Clock$ goes to 0, the wires and $\overline{S}$ and $\overline{R}$ are no longer influenced by D, and consequently, we can change D without affecting Q. That is, the hold time of this latch is 0.

The positive level triggered latch is also called an A-latch, its setup time is thus $S_A = (d_1 + d_2 + d_5)$, and its hold time is $H_A = 0$. The two paths from D to Q have delays $d_1 + d_3$ and $d_1 + d_2 + d_4 + d_5$ respectively. Thus,

$$d_{D \to Q,A} \in [min(d_1 + d_3, d_1 + d_2 + d_4 + d_5), max(d_1 + d_3, d_1 + d_2 + d_4 + d_5)]$$

Similarly

$$d_{Clock \to Q,A} \in [min(d_1 + d_3, d_1 + d_2 + d_4), max(d_1 + d_3, d_1 + d_2 + d_4)]$$

By adding an inverter in the clock path, we obtain the negative level triggered latch shown in Figure 5. We see that Q follows D when $Clock = 0$

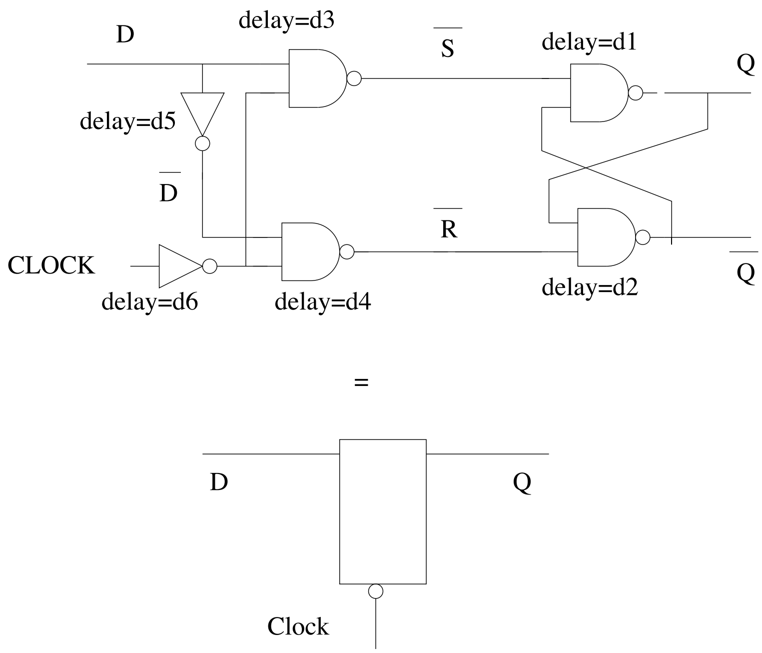

Figure 5: Negative level triggered latch

and when $Clock = 1$, Q remembers the last value it had at the point that $Clock$ went from 0 to 1. The sampling edge for this is the positive edge of clock. Applying a similar analysis as used for the A-latch, we find that the setup-time of the B-latch is $S_B = (d_1 + d_2 + d_5) - d_6$ and the hold-time of the B-latch is $H_B = d_6$.

For the B-latch, the two paths from D to Q have delays $d_1 + d_3$ and $d_1 + d_2 + d_4 + d_5$ respectively. Thus,

$$d_{D\rightarrow Q,B} \in [min(d_1 + d_3, d_1 + d_2 + d_4 + d_5), max(d_1 + d_3, d_1 + d_2 + d_4 + d_5)]$$

Similarly

$$d_{Clock\rightarrow Q,B} \in [min(d_1+d_3+d_6, d_1+d_2+d_4+d_6), max(d_1+d_3+d_6, d_1+d_2+d_4+d_6)]$$

3 Master-Slave D flip-flop

Using a cascade of a B-latch followed by an A-latch, one can construct a D-flipflop (see Figure 6). To see that this circuit functions as a D-flipflop, observe that

- When $Clock$ is 0, the net X follows D.
- At the instant that $Clock$ switches from 0 to 1, X will contain the value of D, of course assuming that D is not changing at this instant (which it will not be, because D must satisfy the setup requirement).
- After $Clock$ becomes 1, Q will follow X, which holds the value which D had at the rising edge of clock.
- Thus, Q will contain the value of D sampled by the rising edge of $Clock$.
- Notice that there is never a direct path from D to Q.

What about the timing of the master-slave D-flipflop? Look at the Figure in 7. One clock cycle of activity is shown. The following points are marked with dashed lines

- At $t = 0$, $Clock$ falls from 1 to 0.
- The line at t_{HA} marks the boundary of the hold region for the A-latch.
- The line at t_D marks the time at which D changes.
- The line t_X marks the time at which X changes.
- The line at t_{SB} marks the boundary of the setup region for the B-latch.
- The line at t_{HB} marks the boundary of the hold region for the B-latch.
- The line at t_{SA} marks the boundary of the setup region for the A-latch.

For correct operation:

- We must have $t_D \leq t_{SB}$ for the change in D to be setup correctly to be captured by the B-latch.
- We must have $t_D \geq t_{HB}$ for the change in D to not be captured or influence the B-latch.
- We must have $t_X \geq t_{HA}$ for the change in X to not influence the A-latch. The minimum possible value for t_X is $d_{Clock \rightarrow Q,B}$. Thus, we must have
$$d_{Clock \rightarrow Q,B} \geq H_A$$
for the flip-flop to work correctly.

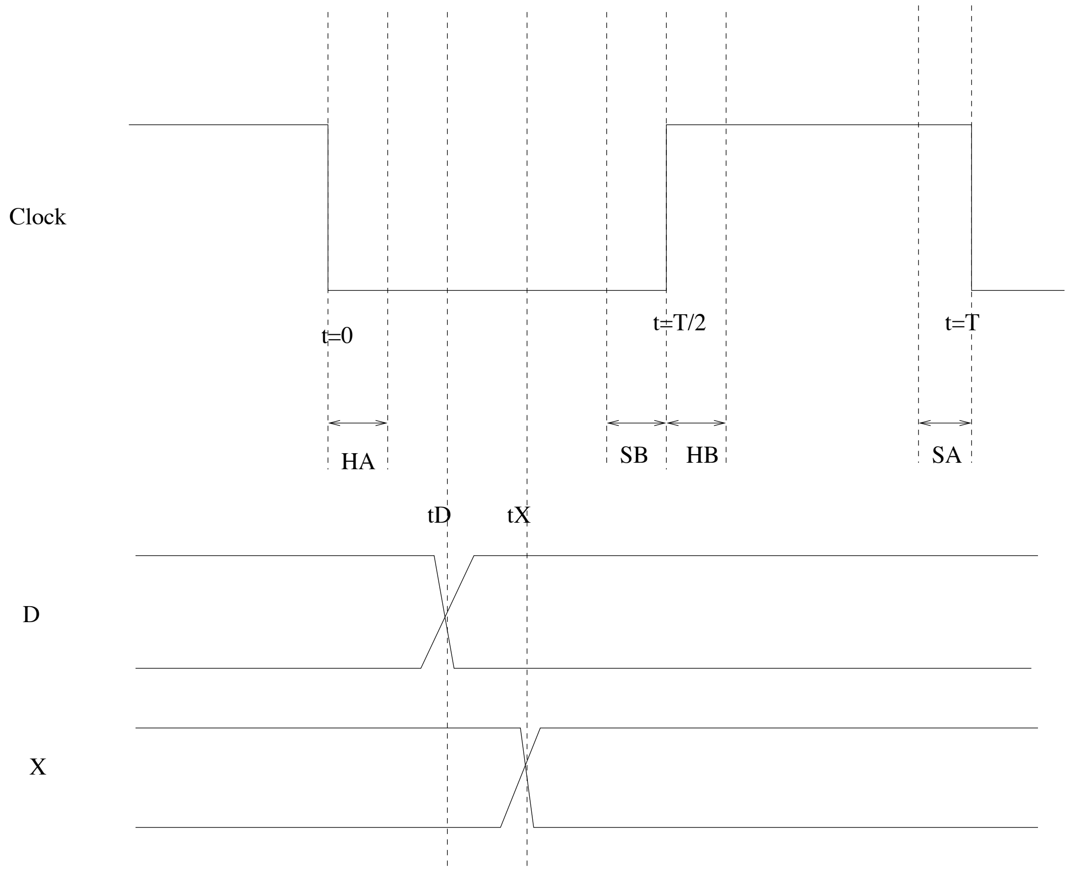

Figure 7: Timing analysis of the Master-Slave D flip-flop

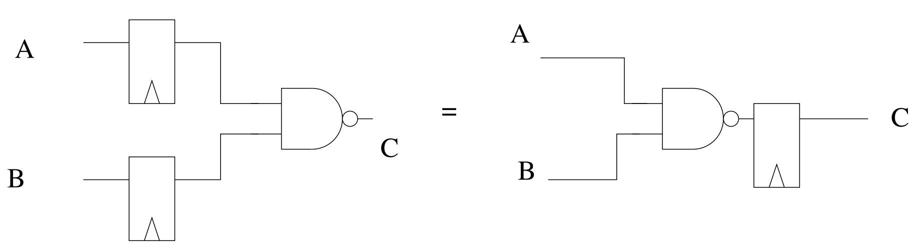

Figure 8: Retiming a circuit by moving D flip-flops

- We must have $t_X \leq t_{SA}$ for the change in X to be correctly captured by the A-latch. The maximum possible value for t_X is $t_{SB} + d_{D \to Q,B}$. Thus, we must have

  $$T/2 - S_B + d_{D \to Q,B} \leq T - S_A$$

  that is

  $$d_{D \to Q,B} + (S_A - S_B) \leq T/2$$

  for the flip-flop to work correctly at clock period T.

The last two conditions are necessary for correct operation of the flip-flop. The first two conditions give us the setup and hold time of the flip-flop, which turn out to be S_B and H_B respectively.

How about the $Clock \to Q$ delay of the flip-flop? The earliest that Q can change will be $(T/2) + d_{Clock \to Q,A}$, because the A-latch opens at $T/2$. The latest time at which Q can change is determined by the latest time at which X can change. Note that X changes late if D changes as late. The latest that D can change is at t_{SB}, and consequently, the latest that X can change is $t_{SB} + d_{D \to Q,B}$. Thus, the latest that Q can change is

$$\begin{aligned} t_Q^{max} &= t_{SB} + d_{D \to Q,A} + d_{D \to Q,B} \\ &= ((T/2) - S_B) + d_{D \to Q,A} + d_{D \to Q,B} \\ &= T/2 \ + \ (d_{D \to Q,A} + (d_{D \to Q,B} - S_B)) \end{aligned}$$

Thus, we conclude that for the flip-flop

$$t_{Clock \to Q} \in [d_{Clock \to Q,A}, d_{Clock \to Q,A} + (d_{Clock \to Q,B} - S_B)]$$

4 Retiming

It is possible to move flip-flops around in order to improve the circuit performance while preserving the functionality. For example, in Figure 8, the two circuits shown are identical functionally (in both cases, $C(k+1) = \overline{A(k).B(k)}$), but the timing of the two circuits different.

This concept can be taken further with latches as well. The circuit transformations shown in Figure 9 preserve circuit functionality but alter its timing.

Retiming of this kind is a powerful tool in the design of fast circuits. We will not study it further in this course, but its good to be aware of it.

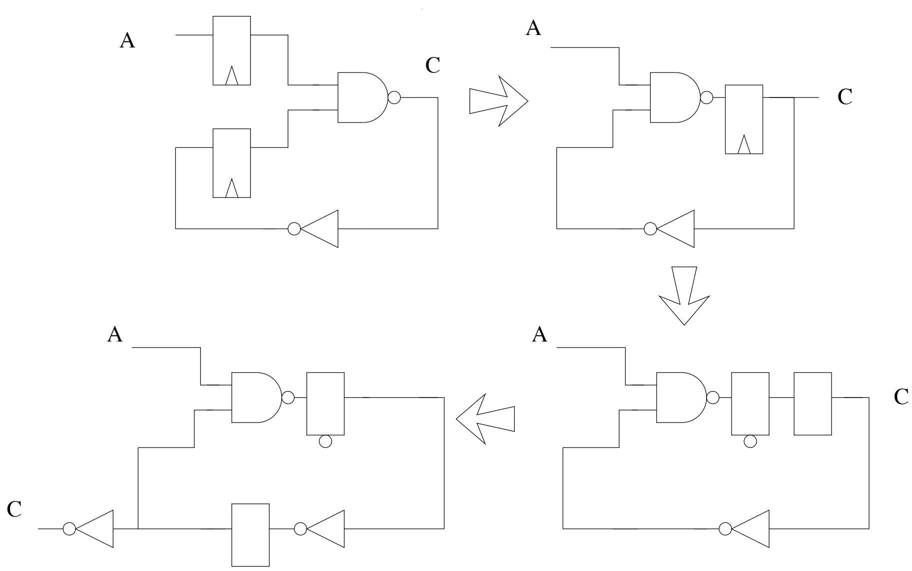

Figure 9: Retiming a circuit by moving latches

5 Assignment

Consider the positive level triggered latch, negative level triggered latch, and the master-slave D flip-flop introduced earlier. Assume that the delay of each gate used in the positive level triggered latch is x units, and that the delay of each gate used in the negative level triggered latch is y units. The clock period may be assumed to be T.

1. Find the setup time, hold time, and the delays of the latches in terms of x and y.
2. For what values of x and y will the master-slave D flip-flop function correctly? In particular, what is the smallest clock period (in terms of x and y) at which the D flip-flop will function correctly?
3. Find the setup time, hold time and delay of the D flip-flop in terms of x and y.

Suppose $x = y = 1$. Assume that the clock to the positive level triggered flip-flop is delayed by an amount w relative to the clock to the negative level triggered flip-flop. The clock period may be assumed to be $T = 10$.

1. For what values of w will the flip-flop function correctly?

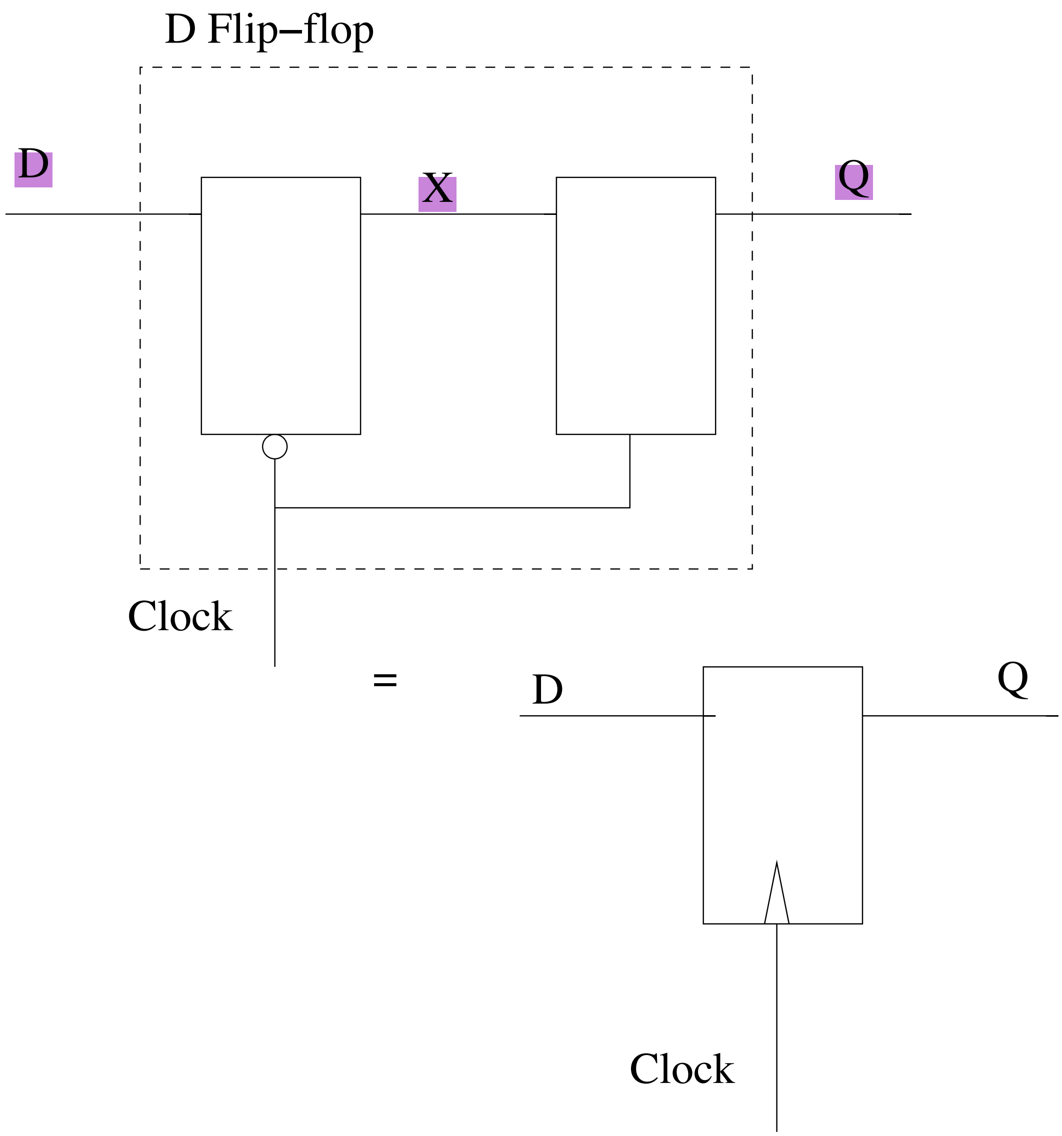

Figure 6: Master-Slave D flip-flop

2. Assuming that w is chosen so that the flip-flop functions correctly, find the setup time, hold time and clock-to-q delay of the master-slave flip-flop in terms of w.