EE230: Simulation Report
Universal Sensor Signal Conditioning

Kumar Ashutosh, 16D070043
Devesh Kumar, 16D070044

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1 Goal

Preparation of signal before using it for our purpose is essential. In order to obtain desired behaviour, the signal needs to be corrected for aberrations before use. The required conditioning varies with its application. For data acquisition we need to digitize the signal and thus Signal Conditioning is used to make the input read to be given to a Digital Interpreter.

2 Simulation Setup and Results

We used **ng-spice** to simulate the circuit. The task of Signal Conditioning is broken down in sub modules and analyzed. All the sub-modules are discussed in next sections.

2.1 Attenuator

We use Attenuator to decrease the Voltage level.
For a Voltage signal in range $\pm 5V$, we use an inverting amplifier and thus the attenuation is given by

$$G = -\frac{R4}{R3}$$

This setup was simulated on ngspice and the results are included below.

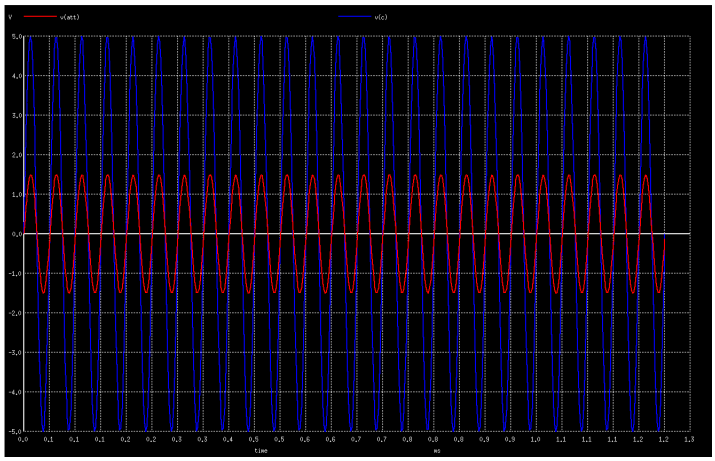


Figure 1: Attenuator for a Voltage Level of $\pm 5V$

For a Voltage signal in range $\pm 15V$, a Voltage divider is first used and then the output of the voltage divider is fed to the inverting amplifier. Thus the attenuation in this case is given by

$$G = -\frac{R4}{3 * R1}$$

The circuit using a Voltage Divider was again simulated to obtain the results presented below.

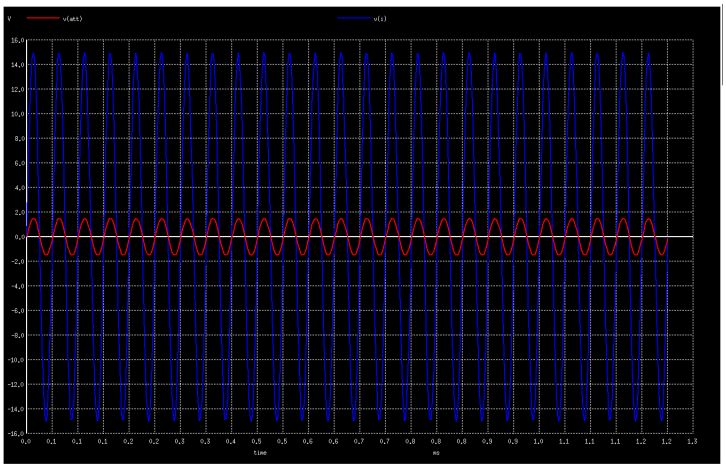
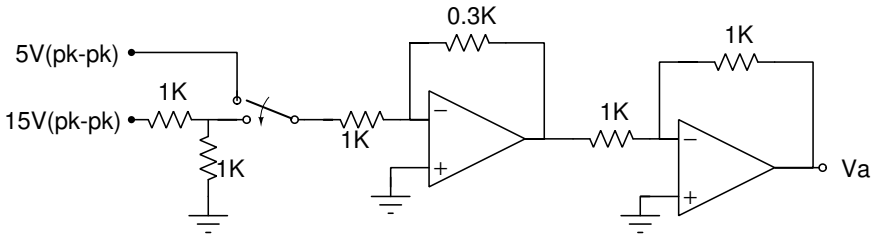


Figure 2: Attenuator for a Voltage Level of $\pm 15V$

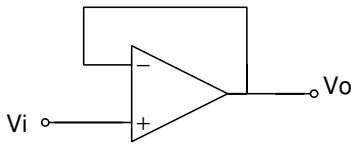
Both the above waveforms validates our simulation. The former uses an inverting amplifier only and the latter one uses a voltage divider in addition to the inverting amplifier.



Circuit 1: Attenuator Circuit

2.2 Isolation Amplifier

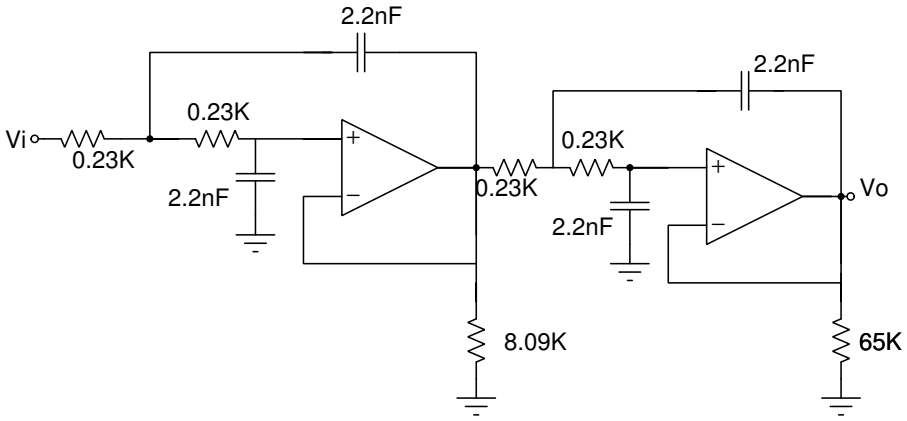
The output of the attenuator is isolated using an Isolation Amplifier. For the purpose of the Simulation, we used a Buffer which acts as an Isolation Amplifier. The $V-$ of the operational amplifier is connected to the output terminal directly and the input is supplied to the $V+$.



Circuit 2: Buffer Circuit/Isolation Amplifier

2.3 Antialiasing Filter

Antialiasing Filter is used to remove the aliasing effects which may have crept into the signal. The filter is a 4th Order Butterworth Filter. The cutoff frequency of the filter is desgined in order to accommodate the audible range frequency ($20Hz - 20KHz$) and to block the higher frequency components which are potentially noise.



Circuit 3: 4th Order Butterworth Filter Circuit

The above discussed Butterworth Filter is simulated and results are obtained as follows.

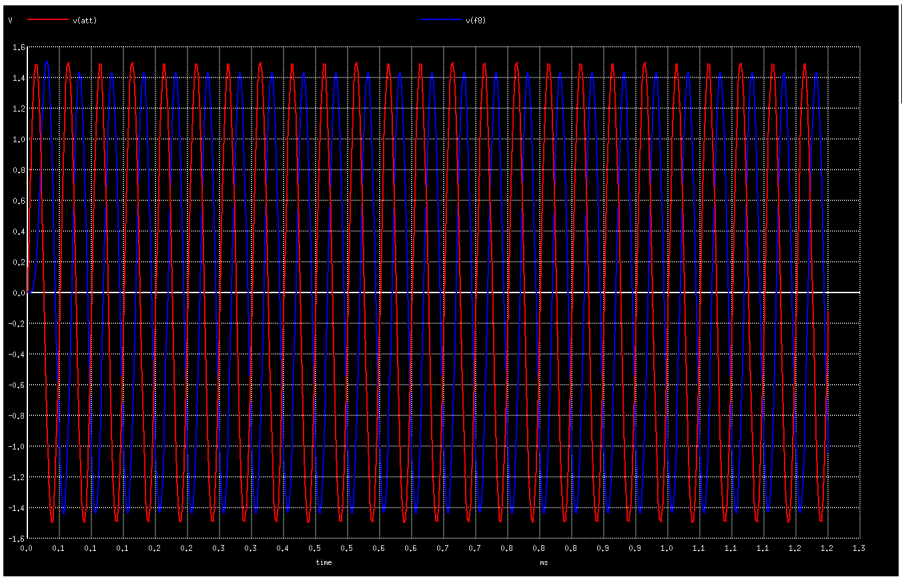


Figure 3: 4th Order Butterworth Filter

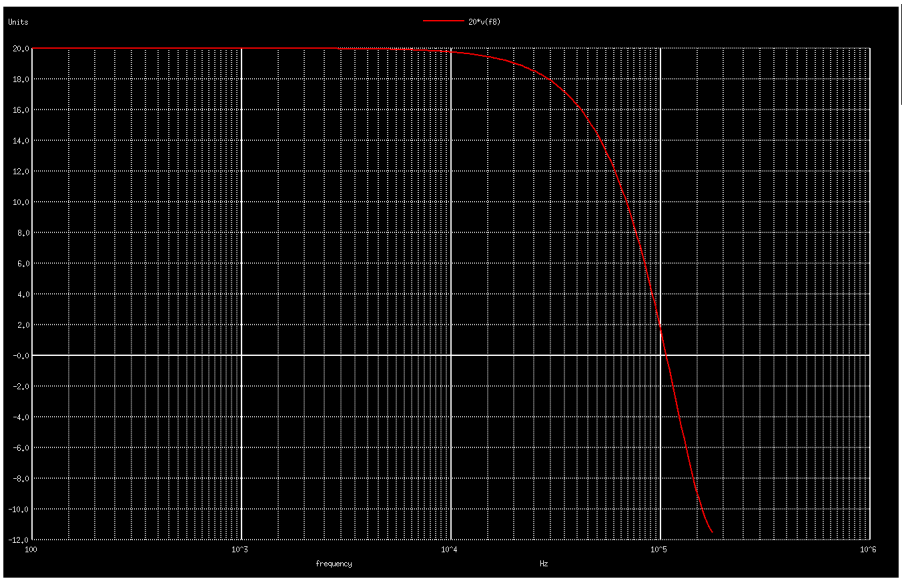


Figure 4: Magnitude Plot of 4th Order Butterworth Filter

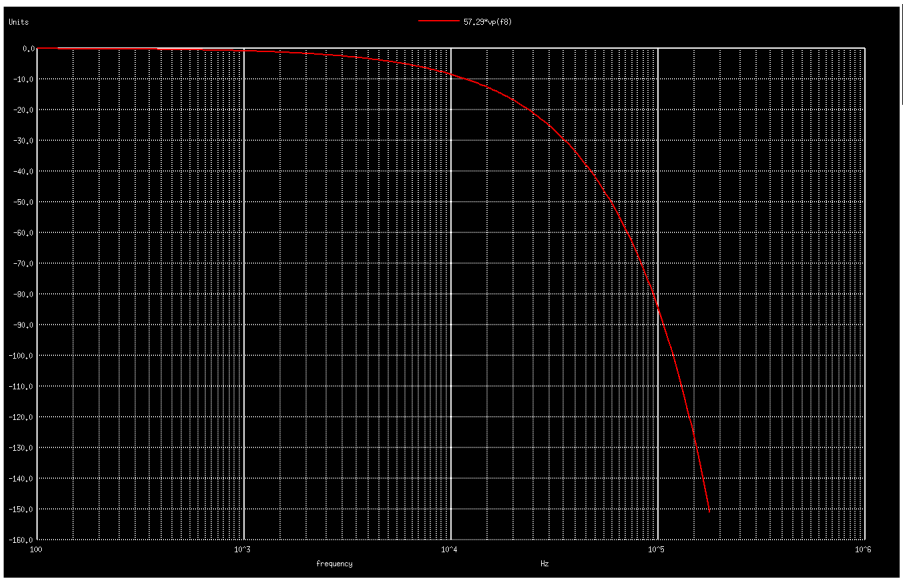
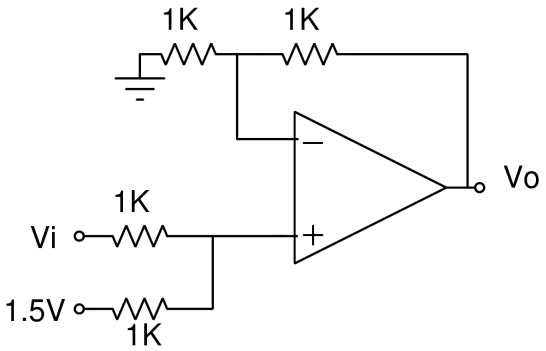


Figure 5: Phase Plot of 4th Order Butterworth Filter

2.4 DC Level Shift

The typical acceptable range of DSP machines are in the range $0 - 3V$ and thus we shift the Voltage levels in order to lie in the required range. For

getting a Voltage in the the range $0 - Vx$ we need to have a DC Shift of $\frac{Vx}{2}$. Here for the purpose of our project we have used Vx to be 3. Thus we introduce a DC Shift of $1.5V$.



Circuit 4: DC Level Shift Circuit

The DC Level Shift circuit was simulated on ngspice and we obtained the following result.

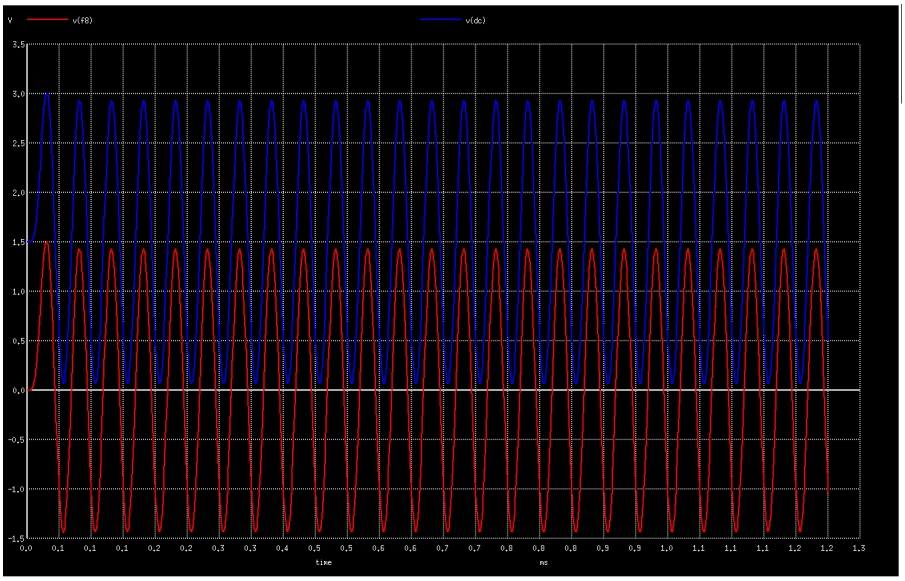
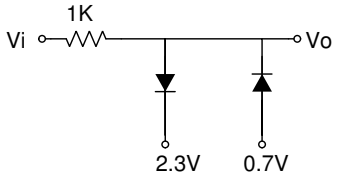


Figure 6: A DC Level Shifter

It can be seen from the simulation result that an input voltage of $\pm 1.5V$ has been converted to an output voltage of $0-3V$ which is as per our requirement.

2.5 Limiter

The output signal which is fed to DSP devices like FPGA and CPLD needs to be in a specified range. Exceeding the range might create problems in the device. Hence we use a Voltage Limiter to keep a check on the output and to not let is exceed a particular voltage (3V in our application).



Circuit: 5 Limiter Circuit

The Voltage Limiter was simulated in ngspice and the following result was observed.

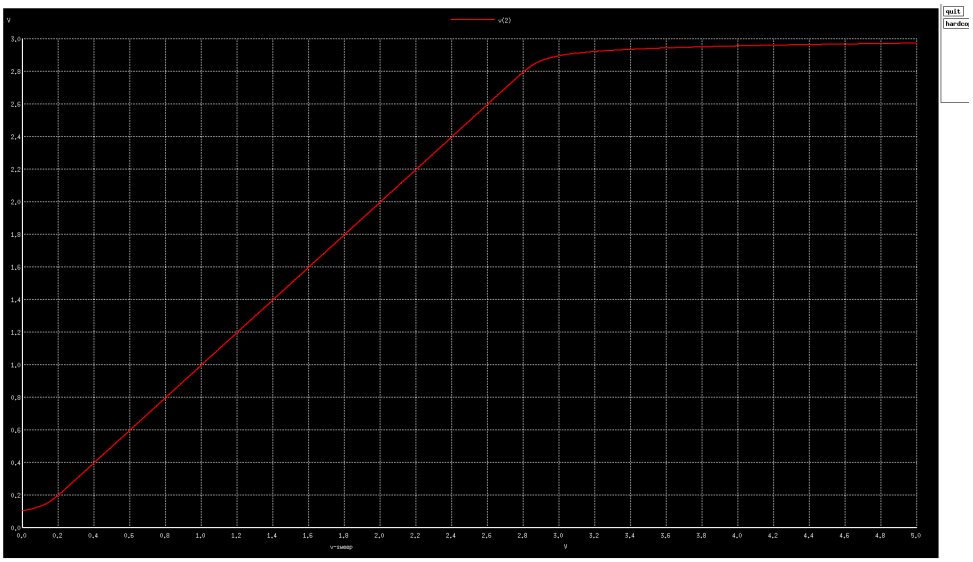


Figure: 7 A Voltage Limiter

It can be clearly seen that the Voltage is limited to a value very close to $3V$. This is again in accordance to the desired functioning of a Voltage Limiter.

3 Observations and Inferences

After simulation of individual blocks, we combined the blocks and simulated the resulting circuit.

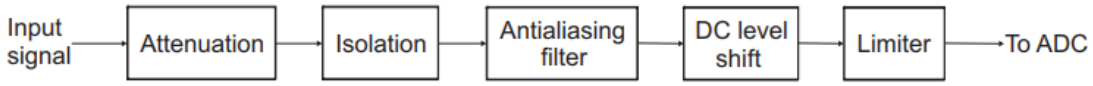


Figure: 8 Block Diagram

The circuit is then tested for both the case, that is when the input is in the range $\pm 5V$ and $\pm 15V$.

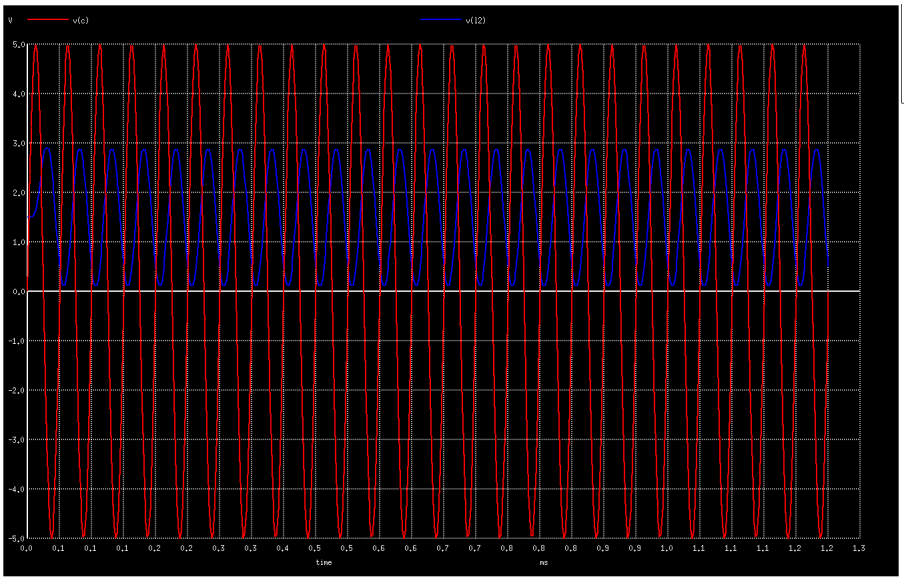


Figure: 9 For input in range $\pm 5V$

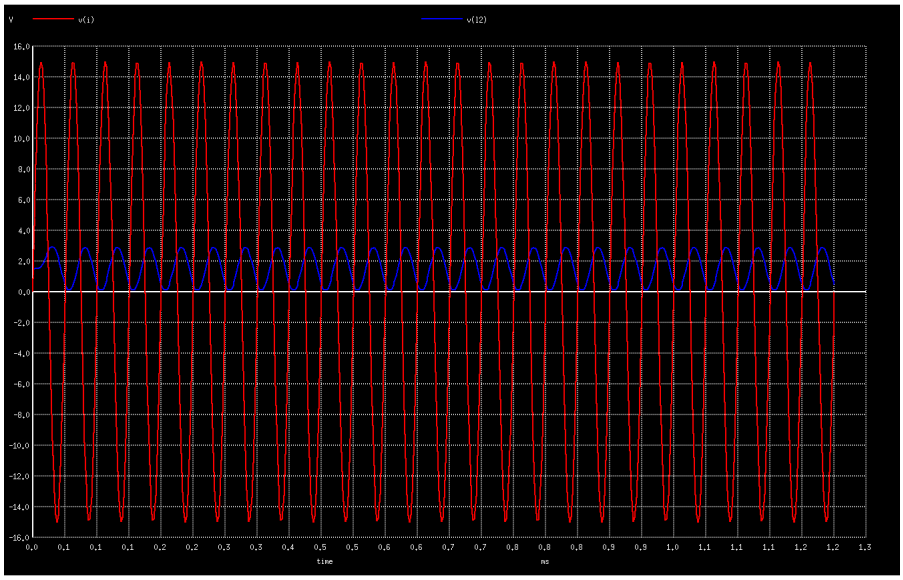


Figure: 10 For input in range $\pm 15V$

The simulation result is in accordance to our earlier expected value and now the output is in the desired range of $0 - 3V$. If the required frequency is different, it can be adjusted by changing the cutoff frequencies. Also, the gain can be varied by changing the resistance R_4 in the circuit.

References

[1] Irwin A. Diaz-Diaz, and Ilse Cervantes *Design of a flexible analog signal conditioning circuit for DSP-based systems*. The 2013 Iberoamerican Conference on Electronics Engineering and Computer Science, 2013

[2] National Instruments. *What is Signal Conditioning?*. Link

Appendix

The following is the code used to obtain the above results. Individual parts are separated by a commented line.

```
*-------------------------------------------------------------------------
*
* To use a subcircuit, the name must begin with 'X'.  For example:
* X1 1 2 3 4 5 ua741
*
* connections:   non-inverting input
*                |  inverting input
*                |  |  positive power supply
*                |  |  |  negative power supply
*                |  |  |  |  output
*                |  |  |  |  |
.subckt ua741    1  2  3  4  5
*
  c1   11 12 8.661E-12
  c2    6  7 30.00E-12
  dc    5 53 dx
  de   54  5 dx
  dlp  90 91 dx
  dln  92 90 dx
  dp    4  3 dx
  egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
  fb    7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -10E6 10E6 10E6 -10E6
  ga    6  0 11 12 188.5E-6
  gcm   0  6 10 99 5.961E-9
  iee  10  4 dc 15.16E-6
  hlim 90  0 vlim 1K
  q1   11  2 13 qx
  q2   12  1 14 qx
  r2    6  9 100.0E3
  rc1   3 11 5.305E3
  rc2   3 12 5.305E3
```

```
  re1  13 10 1.836E3
  re2  14 10 1.836E3
  ree  10 99 13.19E6
  ro1   8  5 50
  ro2   7 99 100
  rp    3  4 18.16E3
  vb    9  0 dc 0
  vc    3 53 dc 1
  ve   54  4 dc 1
  vlim  7  8 dc 0
  vlp  91  0 dc 40
  vln   0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=93.75)
.ends

*-----------------------Attenuator---------------------------------------

X1 0 e 1 2 f ua741
X2 0 g 1 2 att ua741

Rsw d c 0
* make it to a for switching to 15 v input and c for 5 v input
R1 i a 1K
R2 d e 1K
R3 a 0 1K
R4 e f 300
*R4 is variable
R5 f g 1K
R6 g att 1K

VL  C 0 sin(0 5 20K 0 0)
VH  I 0 sin(0 15 20K 0 0)
VSS 1 0 DC 15v
VDD 2 0 DC -15v

*-----------------------Buffer-------------------------------------------
```

```
Xb1 att 1b 1 2 1b ua741
rbu 1b f1 0

*-----------------------4th Order Butterworth-----------------------------------

Xf1 f3 f5 1 2 f4 ua741

cf1 f2 f4 2.2nf
cf2 f3 0 2.2nf

Rf1 f1 f2 0.23K
Rf2 f2 f3 0.23K
Rf3 f4 f5 0K
Rf4 f5 0 8.09K

Xf2 f7 f9 1 2 f8 ua741

RF5 F4 F6 0.23K
RF6 F6 F7 0.23K
RF7 F8 F9 0K
RF8 F9 0 65.79K

CF3 F6 F8 2.2nf
CF4 F7 0 2.2nf


*-----------------------DC Level Shifter-------------------------------------

X3 l j 1 2 dc ua741

R8 f8 L 1K
R9 m l 1K
R10 0 j 1K
R11 j dc 1K

Vdc m 0 1.5v

*-----------------------Limiter----------------------------------------
```

```
R12 dc l2 1k
D1 l2 l3
D2 l4 l2


Vtest1 l3 0 DC 2.3V
Vtest2 l4 0 DC 0.7V

.control
tran 0.020m 01.25m
plot v(att) v(c)
plot v(att) v(f8)
plot v(f8)  v(dc)
plot v(dc) v(l2)
plot v(c) v(l2)
.endc
.end
```