Experiment 1:Characterization of a CMOS Inverter

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1 Overview

Cmos inverter is one of the most easily available and cheep inverters which are widely used in the electrical circuits.

The cmos has three terminal basically gate, source, and drain. The current in the source drain can be controlled by gate voltage.Apart of these three terminals Cmos also has a fourth terminal i.e. sub strait. there are two types of c mos : n type and p type. it operates in three region linear, saturation, cutoff.

A inverter is a device that performs logical negation on its input. In other words, if the input is true, then the output will be false

The purpose this experiment was to study the:

- Transfer characteristic.
- Output characteristics.
- Delay characteristics
- Ring oscillator

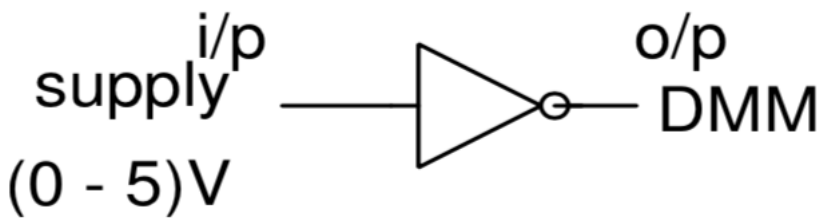
Components required for this experiment :

- IC MM74C04 - 4
- Decoupling capacitors -0.1 F..
- 1 1.2 k Resistor
- 20 K potentiometer
- Opamp as buffer

2 Observations

2.1 Plot the transfer characteristics of inverter and tabulate the input and corresponding output voltages. Find the switching point on the transfer characteristic.

In this experimental setup we try to find the transfer characteristics of the not gate. Ideally it should have sudden fall . it should be higher for lower input and vice versa



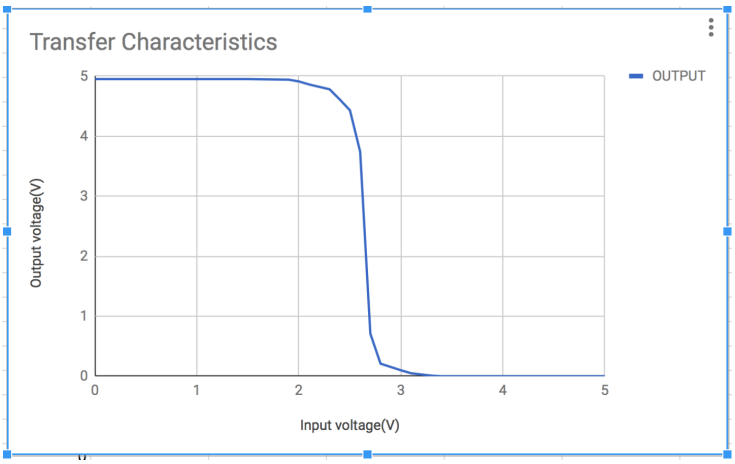


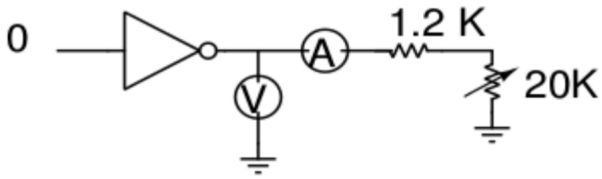
figure : transfer characteristic

Input Voltage	output Voltage
0	4.95
0.4	4.95
0.7	4.95
0.9	4.95
1.5	4.95
1.9	4.94
2	4.91
2.1	4.86
2.3	4.78
2.4	4.61
2.5	4.43
2.6	3.74
2.7	0.71
2.8	0.21
3	0.1
3.1	0.05
3.2	0.03
3.3	0.01
3.4	0
4	0
5	0

switching point is :2.5 V

We wire up the circuit and give input from zero to 5 v and measure the output voltages. the switching point will be the point about which maximum change in the output will be . Ideally the graph should have a sudden fall.

2.2 Plot the output characteristics of the inverter in the two cases: output- high and output-low. Tabulate the input and corresponding output voltages for both the cases.



Ciruit Layout for observing output characteristics at *low input*

for high input we just put input voltage as 5v

In this we try to find the output characteristics of cmos inverter. for this we fix the input as low in first case and then study the change in output voltage corresponding to change in current. we change the current with the help of potentiometer.

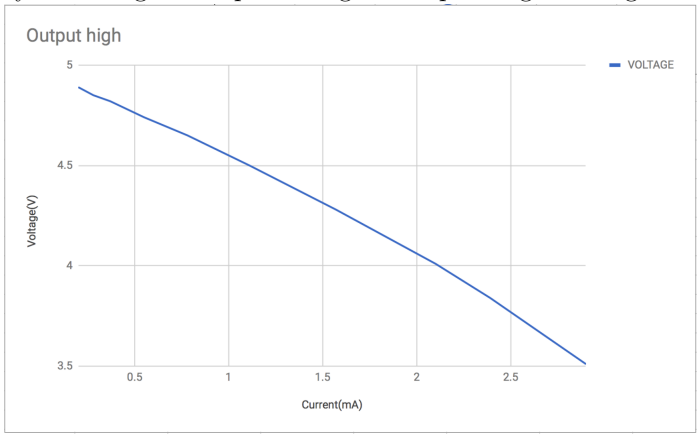


figure : input low

current(mA)	Voltage(v)
0.2	4.89
0.28	4.85
0.37	4.82
0.55	4.74
0.78	4.65
1.11	4.5
1.57	4.28
2.1	4.01
2.39	3.84
2.9	3.51

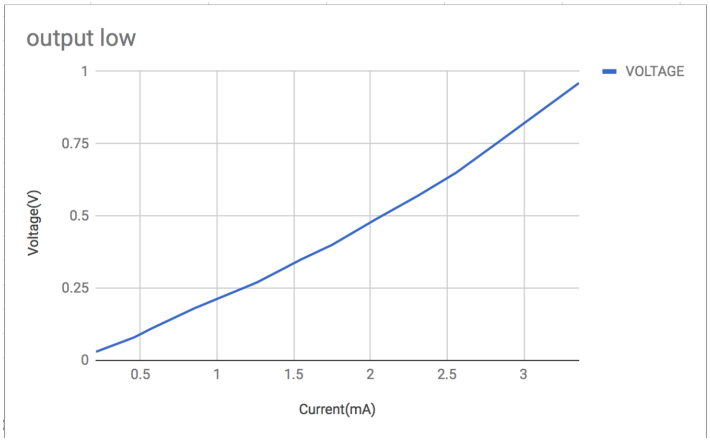


figure : input high

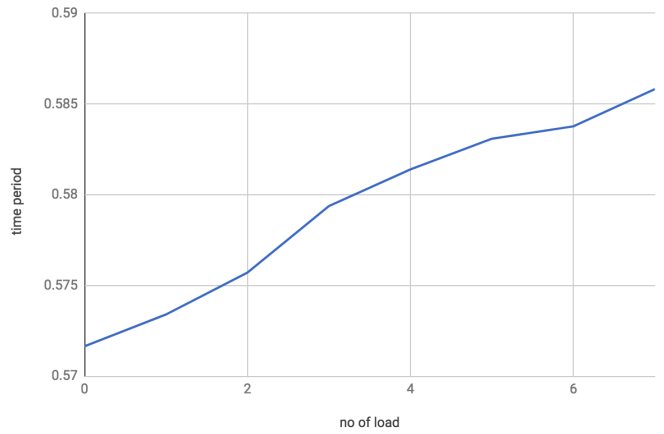
current(mA)	Voltage(v)
0.21	0.03
0.36	0.06
0.46	0.08
0.57	0.11
0.85	0.18
1.26	0.27
1.55	0.35
1.75	0.4
2.04	0.49
2.31	0.57
2.56	0.65
2.82	0.75
3.36	0.96

2.3 Plot the oscillation period of the ring oscillator as a function of the load at the output. Find pinv and . A snap-shot of the DSO (get help from Laboratory staff if you do not have a camera) showing the ring-oscillator output with load = 2 should also be included in the report.

mos is a electrical device, so it has a time delay between the input applied and output supplied. this can be due to two reasons . firstly due to the cmos it self. And secondly due to the the load which is applied to it.

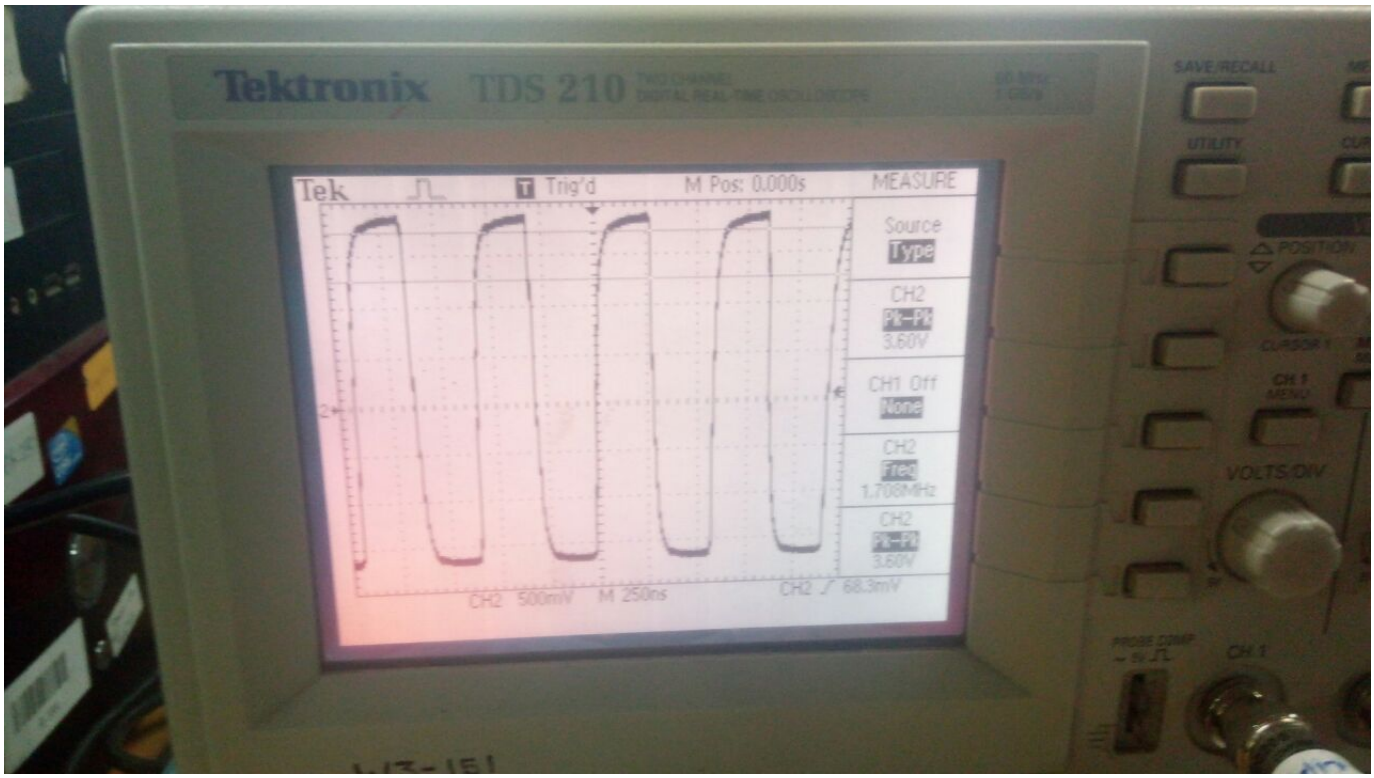
However this time delay is very less. so inorder to calculate this time period we join an odd no (17 in our experiment).as their are many c mos inverters so their delays will be added and can be easily calculated. The delay due to the load will increase linearly with the load.

The period of osccilation is given by: t *(34pinv + (32 + (2 * (1 + AdditionalLoadOutput)))



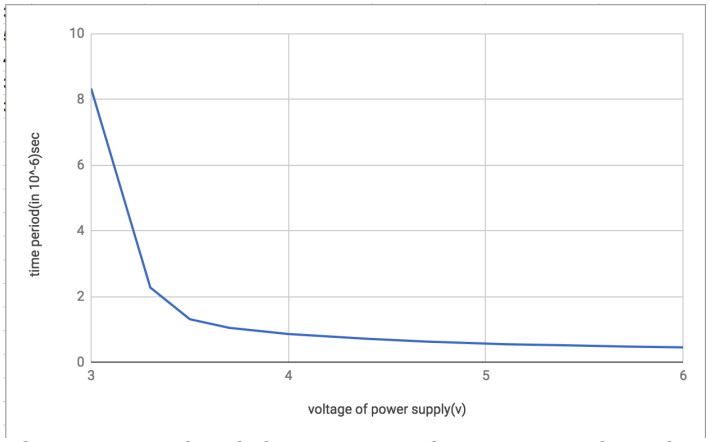
No. of load	time period($10^{-6} sec$)
0	0.5716402392
1	0.5724098454
2	0.5757052389
3	0.5793742758
4	0.5813953488
5	0.583090379
6	0.5837711617
7	0.5858230814

slope = t = 0.001020244765x$10^{-6} sec$ $Pin = 7.247774223$



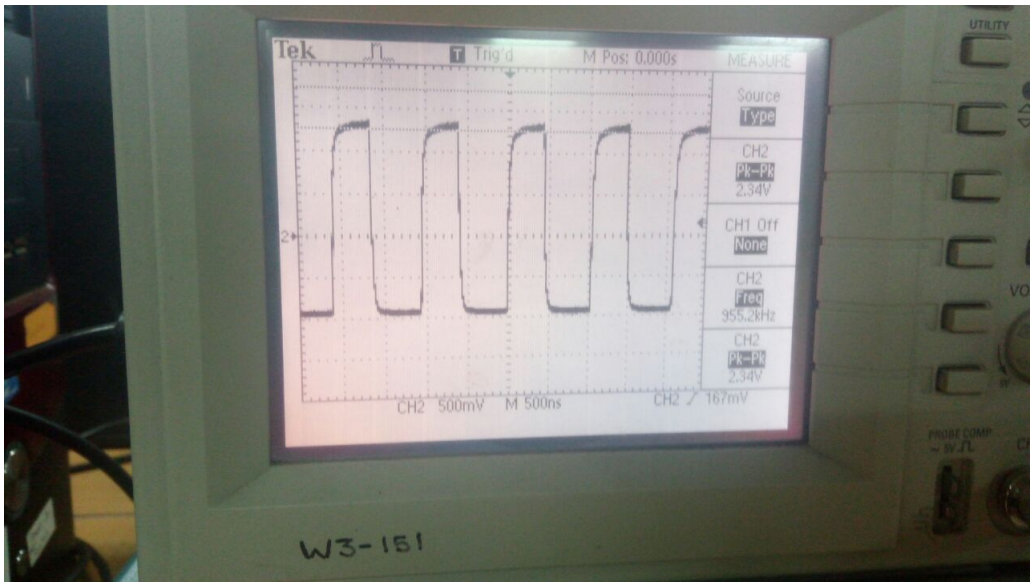
at load =7.

2.4 Plot the ring oscillator period as a function of the power supply voltage (varied from 3V to 6V). Record your observations in a table. How does the delay vary with the power supply voltage?

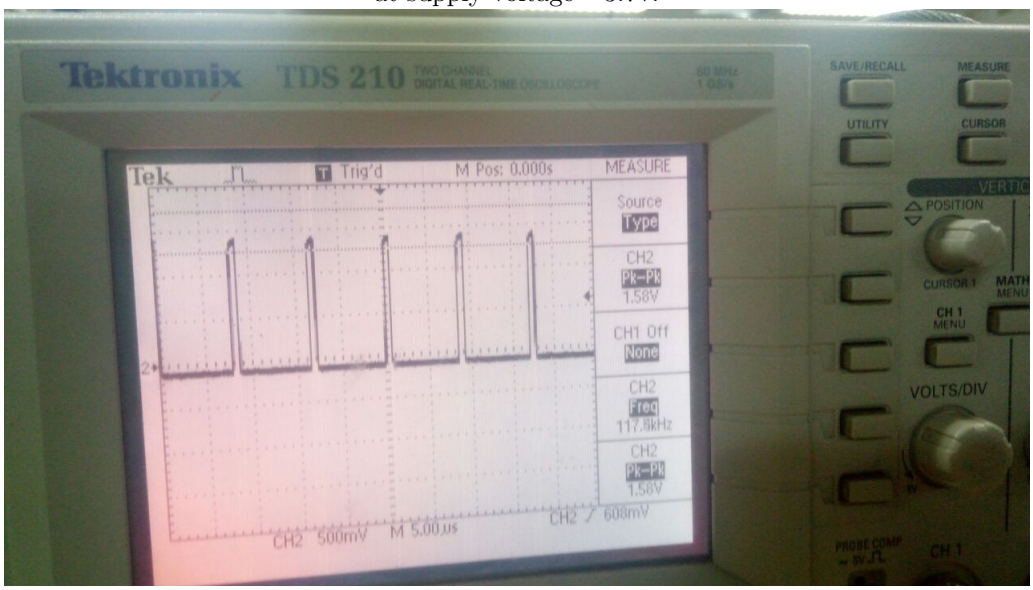


power supply voltage	time period$(10^{-6})sec$
6	0.456412597
5.7	0.4830917874
5.4	0.5208333333
5.1	0.5540166205
5	0.5743825388
4.7	0.634115409
4.4	0.7178750897
4	0.8643042351
3.7	1.052631579
3.5	1.314060447
3.3	2.277904328
3	8.333333333

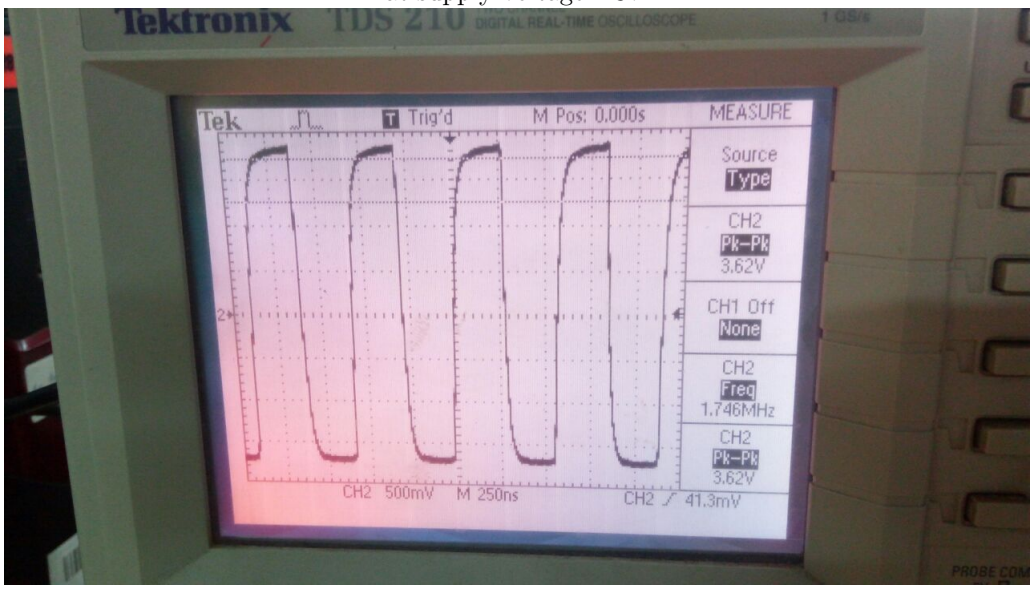
The time period and the power supply vary inversely with each other i.e. t =c*1/vdd



at supply voltage =3.7v.



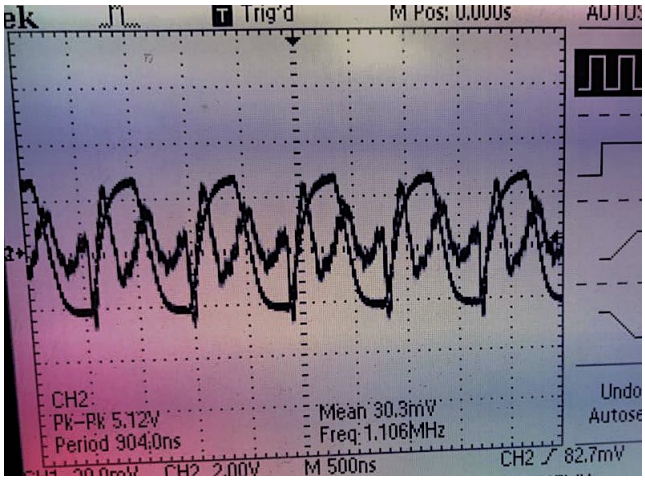
at supply voltage =3v.



at supply voltage =5v.

2.5 Observe the power-supply current drawn by the ring oscillator. Mea- sure the peak and average value. Include a snapshot of the DSO measurement.

When output switches from low to high, current is drawn from the power supply. The current drawn triangular pulse whose width is the delay of the gate.



Vp-p=22mv Vavg= 4mv

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circuit source :lab manual