EE230: Experiment 1
Differential Amplifier and Current Mirrors

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1 Overview of the experiment

1.1 Aim of the experiment

In this experiment we try to design a differential amplifier i.e. a circuits that amplifies the difference between the two input supplied to it. Study, how to use current mirrors and how to find CMRR of differential amplifier

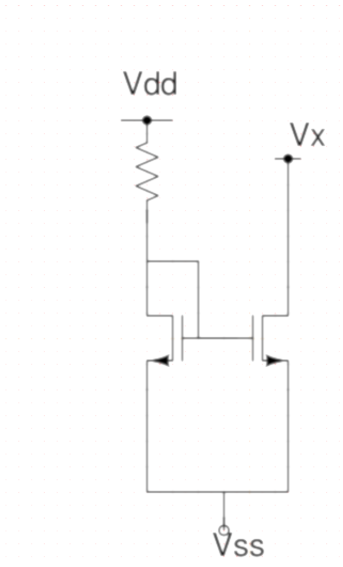
1.2 Methods

To design a differential amplifier we use cmos. For our experiment cmos should be in saturation mode. To achieve this we try to fix Iss = 1mA. Instead of using a current source to achieve this we use a current mirror with a variable resistance. we adjust the resistance such a way that Iout is 1mA. Both the cmos will now be in saturation mode and will amplify their respective gate source voltage. we will take the difference in the output of these two cmos to get the differential output

2 Design

Current Mirror
To design a current mirror we take two nmoss M1 and M2 and connect their gate terminal we further connet gate of M1 with its drain, this ensures that the mos will always be in saturation as $Vgs = Vds$, so $Vgs - Vt < Vds$. we control the current in M1 by changing the resistance connected to drain of

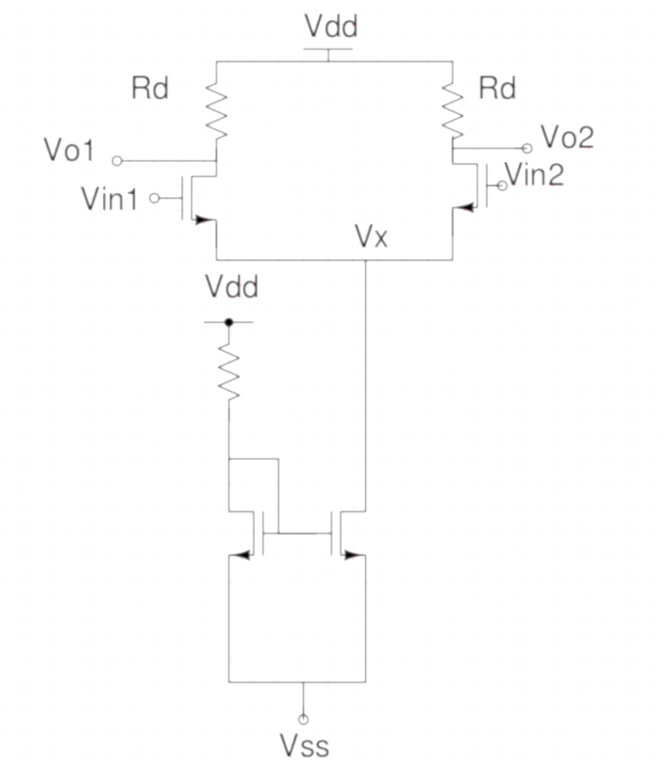
M1. the current in the M1 gets mirrored in M2 as the terminals of both the mos are equi potential.



Current mirror

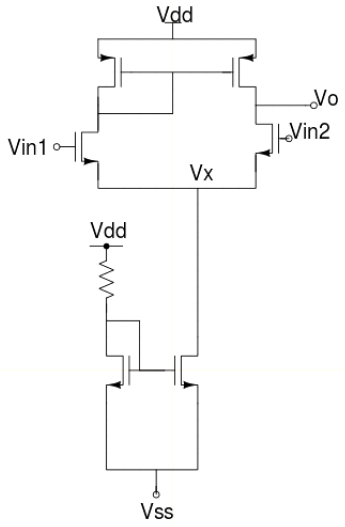
differential amplifier with resistive loads
We amplify both the input signal by the same amount i.e.$-Gm * Rd$ and then take the difference between Vo1 and Vo2 to get the desired result.

expression for gain.
considering small signal model for the mos
Vo1=-Gm x Rd x Vin1
Vo2=-Gm x Rd x Vin2
Vo1-Vo2=-Gm x Rd(Vin1-Vin2)
Ad = -Gm x Rd
We ensure that the mos is in saturation by a current source made of current mirror. it is important that same drain current flows through both the moss



passive load

Active Load To incease the gain and Cmrr we replace the resistance Rd with a current mirror setup. This ensures that resistance offered by both mos are equal and same current flows through the moss.



active load

3 Simulation results

3.1 Code snippet

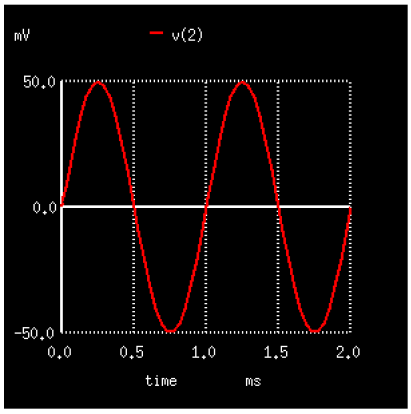
for part 1(passive load)

```
     *Model file for ALD1106 and ALD1107
*SPICE Level 1
*Created by: Debapratim Ghosh, IIT Bombay
*Date: 12 Dec 2013

.MODEL ALD1106 NMOS (LEVEL=1 CBD=0.5p CBS=0.5p CGDO=0.1p CGSO=0.1p GAMMA=.85
+ KP=479u L=10E-6 LAMBDA=0.029 PHI=.9 VTO=0.8 W=20E-6)

.MODEL ALD1107 PMOS (LEVEL=1 CBD=0.5p CBS=0.5p CGDO=0.1p CGSO=0.1p GAMMA=.45
+ KP=206u L=10E-6 LAMBDA=0.0304 PHI=.8 VTO=-0.82 W=20E-6)



M1 1 2 3 7 ALD1106
M2 4 6 3 7  ALD1106
M3 8 8 7 7 ALD1106
```

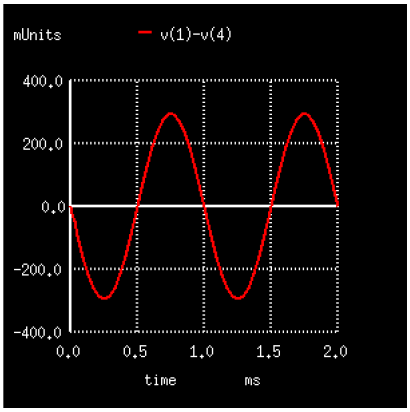
```
M4 3 8 7 7  ALD1106
VSS 7 0 -4.5v
VDD 5 0 4.5v
rd1 1 5 9.7k
rd2 4 5 9.7k
rvar 8 5 6.923k


Vin 2 0 SIN(0 50m 1k)
r3 0 6 0k

.TRAN 0.05m 2m
.control
run
plot v(1)-v(4)
plot v(2)
.endc
.end
```

for active load

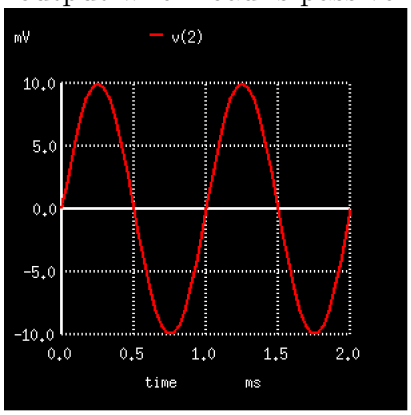
3.2 Simulation results



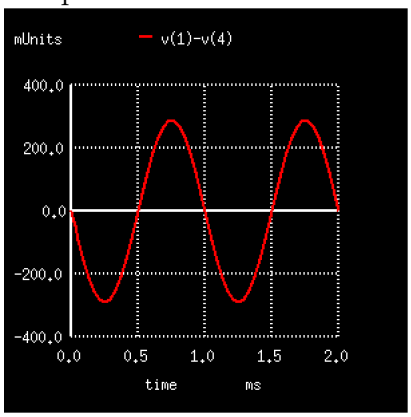
input when load is passive



output when load is passive



input when load is active

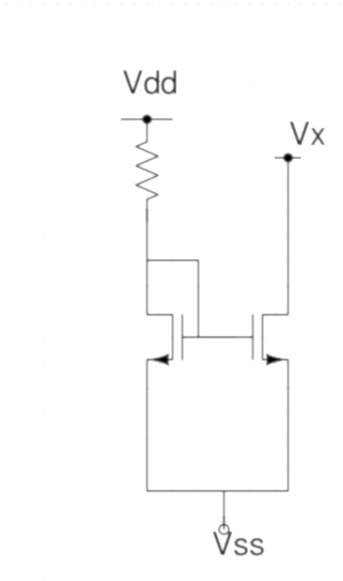


output when load is active

4 Experimental results

4.1 Current mirror

In this part we varied r through potentiometer such that the current in the main circuit comes to be 1mA.

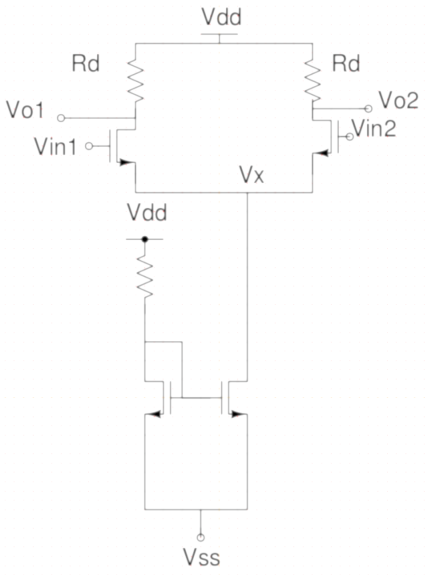


current mirror

4.2 Differential amplifier with resistive load

We connected the input between Vin1 and Vin2 .Measured the Vo1 in one probe and Vo2 on other probe.to get the final output we subtracted the two output using the math function of the DSO. we then find out the ratio of amplitude of input and M(output of the math function) to get the differential gain.
To measure the swing we increased the amplitude and saw its variation in the DSO. the swing will be the maximum and minimum amplitude for which the output does not distort.

To get the Common mode gain we sorted both Vin1 and Vin2 and then applied input voltage on Vin1. We then measured the output i.e Vo1 and Vo2 on the Dso. Found out their difference with the math funtion. the common mode gain will be the ratio of amplitude of M(output of the math) and input voltage



passive load

differential gain at 1Khz

`differentialgain2.jpeg`

maximum amplitude for which ouput does not distort

frequency	Ad
1000	8.24
10000	8.32
100000	6.96
500000	2.62
1000000	1.52

1. What value of resistive load did you apply? What gain did you measure, vs what you expected? Explain why there are discrepancies, if any. Was the output swing symmetric?

We used 10kohms as the resistive load. from the data sheet of ALD1106 which came out to be $0.52 * 10^{-3}$ SI units
Gm from this K came out to be $0.72\text{X}10^{-3} SIunits$

$$Rd = \frac{gain}{(Gm)} = 9.7kohms \tag{1}$$

2. Was there distortion? How did you tweak the circuit to address this challenge?
Yes there was distortion in the output when we increase the amplitude of the input.this can be removed when we decrease the amplitude. Also the distortion can be due to loose connections and can be removes by checking the wire.
3. Maximum symmetric output swing at 1kHz.

1.14V

4. Measured common mode gain, and CMRR.

frequency	Acm	CMRR(db)
1000	0.085	40.14884386
10000	0.09	39.41466639
100000	0.093	37.38962772
500000	0.097	28.81155372
1000000	0.099	23.90143707

5. Measured offset voltage of differential amplifier.
80mv

6. Comparison with 2 other groups - mention which groups you compared to (names and roll numbers), and comment on any differences in observations - why are the answers different?
Anhad Bhati(16d070045)

frequency	Gain	ACM	CMRR(db)
1000	7.6	0.08	39.55447211
10000	7.04	0.08	38.88965344
100000	6.08	0.224	28.67311122
500000	2.28	0.128	25.01449755
1000000	1.28	0.128	20

Nisha Brahmankar(16d070019)

frequency	gain	ACM	CMRR(db)
1000	7.52	0.12	35.94073189
10000	7.68	0.32	27.60422483
100000	6.64	0.56	21.47960105
500000	2.44	0.64	11.62419705
1000000	1.48	0.4	11.36403448

Our gain was larger than rest of the groups the reason could be human error or loose connections. There was difference between common mode gain which could be due to the efficiency of the moss that each group had. This could also depend DSO. The difference in the value of the CMRR was not much

5 Questions for reflection

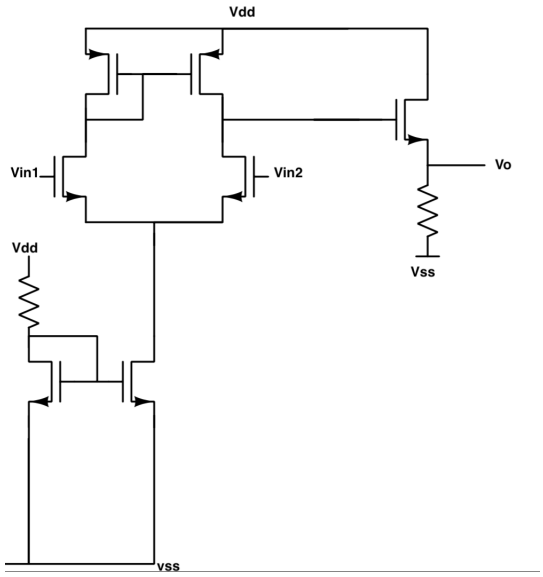
1. What difficulties did you face in performing the experiment?
Ans. The circuit was quite big on the breadboard so it was very difficult to debug the circuit. There was also noise in the circuit.

2. What advantages or disadvantages did you notice for the diff-amp with active load, as compared to resistive load?
Ans. Active load has greater gain and its CMRR value is also High

3. If you increase the supply voltage magnitude for the diff-amp, would the maximum output swing increase or decrease? Explain your answer.
Ans. the swing would increaseas we use this differential ampliphier on the assumption that
$Vgs - Vt > vgs$
as we increase Vgs so are approximation becomes more valid hence swing inreases.

4. In the simple current mirror, one can introduce "current gain" by sizing the two transistors differently. Assuming different W/L ratio for the transistors, obtain a value for this current gain. Can you suggest why this might be a better way to distribute currents in a circuit, as compared to setting up separate reference branches with separate resistors?
Ans. the current distributes according to the relation K2 / K1
If we need more than one current source in our circuit then we do this by only one Iref when we use a current mirror.
Is better than a resistance as it very hard to find a pair of resistance whose ratio remains constant. Moreover resistance is a function of temperature.

5. In class you learnt that a cascode configuration is better for large gain and low output resistance. Propose a possible circuit diagram using cascode differential amplifier, and active load, with appropriate biasing network for providing bias currents. (Only the circuit diagram made in xcircuit is expected)
Ans.


Vdd
Vin1
Vin2
Vo
Vss
Vdd
vss