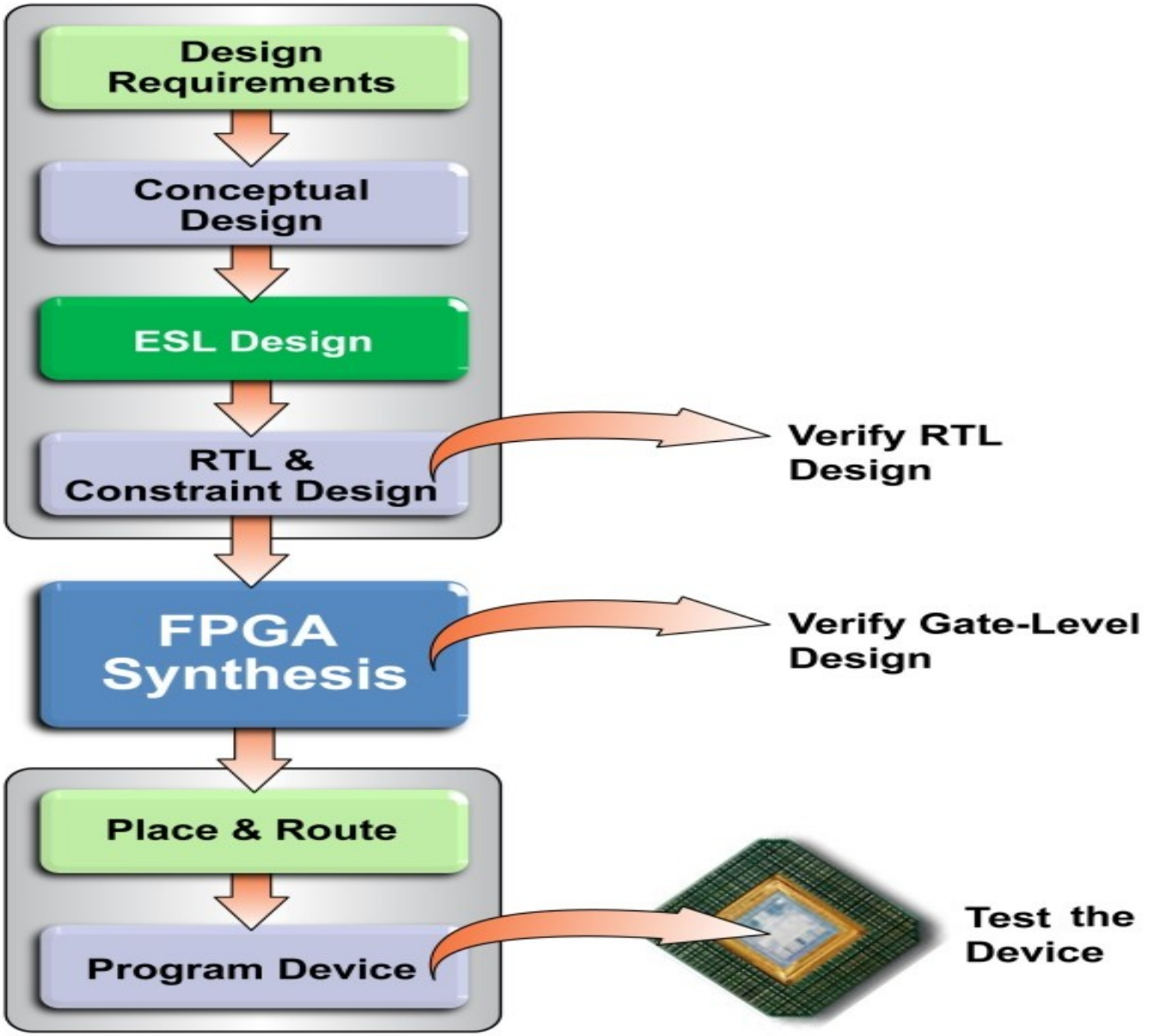
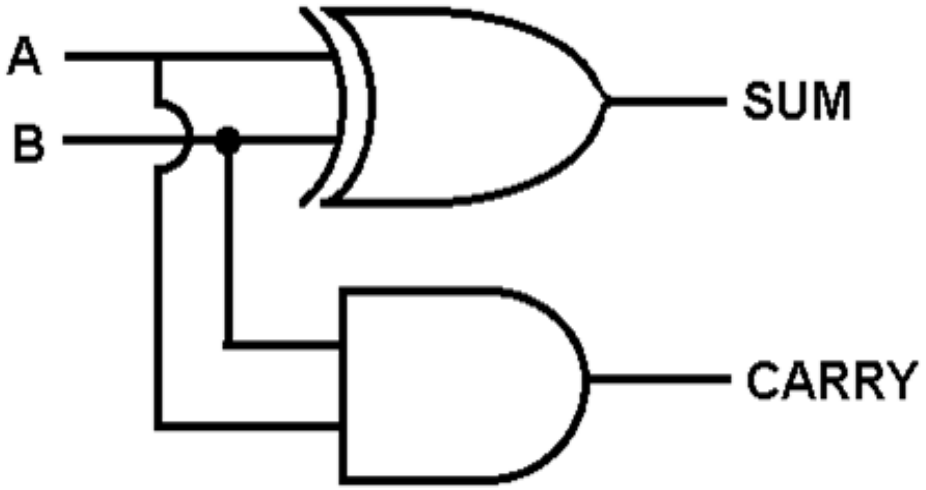
# Digital Design with Quartus

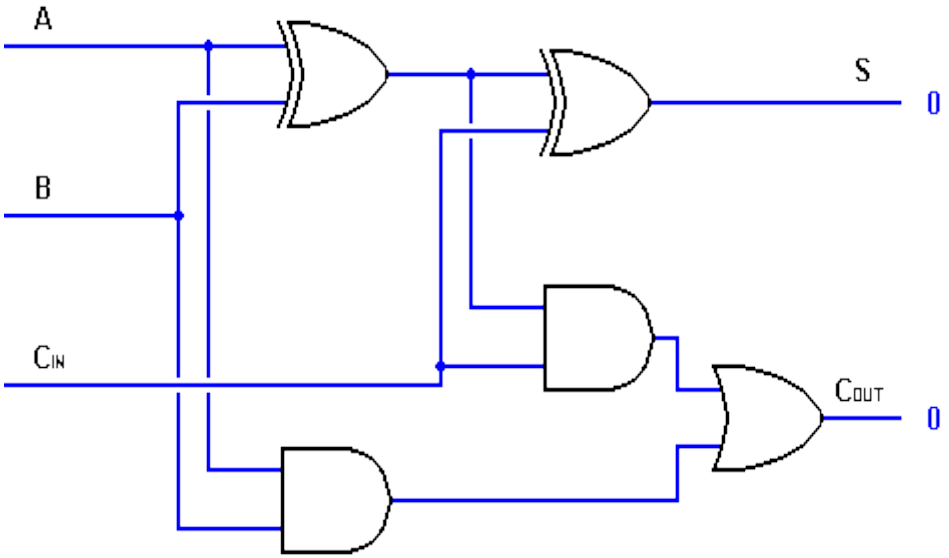
by
Varun Warrier

# Design Flow

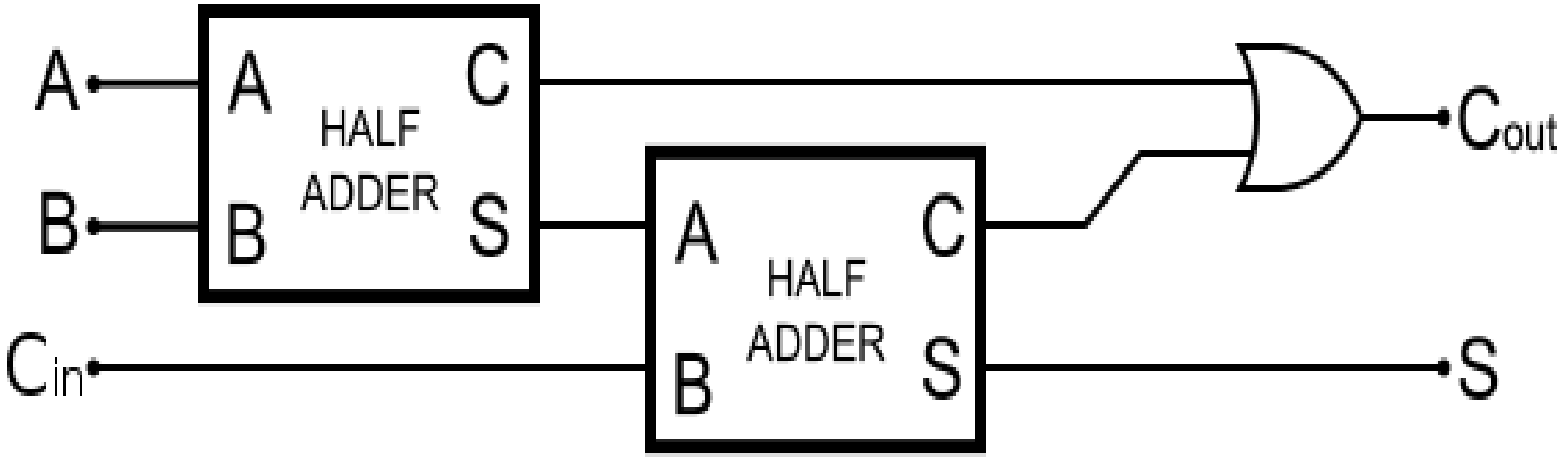

Design Requirements
Conceptual Design
ESL Design
RTL & Constraint Design
Verify RTL Design
FPGA Synthesis
Verify Gate-Level Design
Place & Route
Program Device
Test the Device

# Half Adder & Full Adder

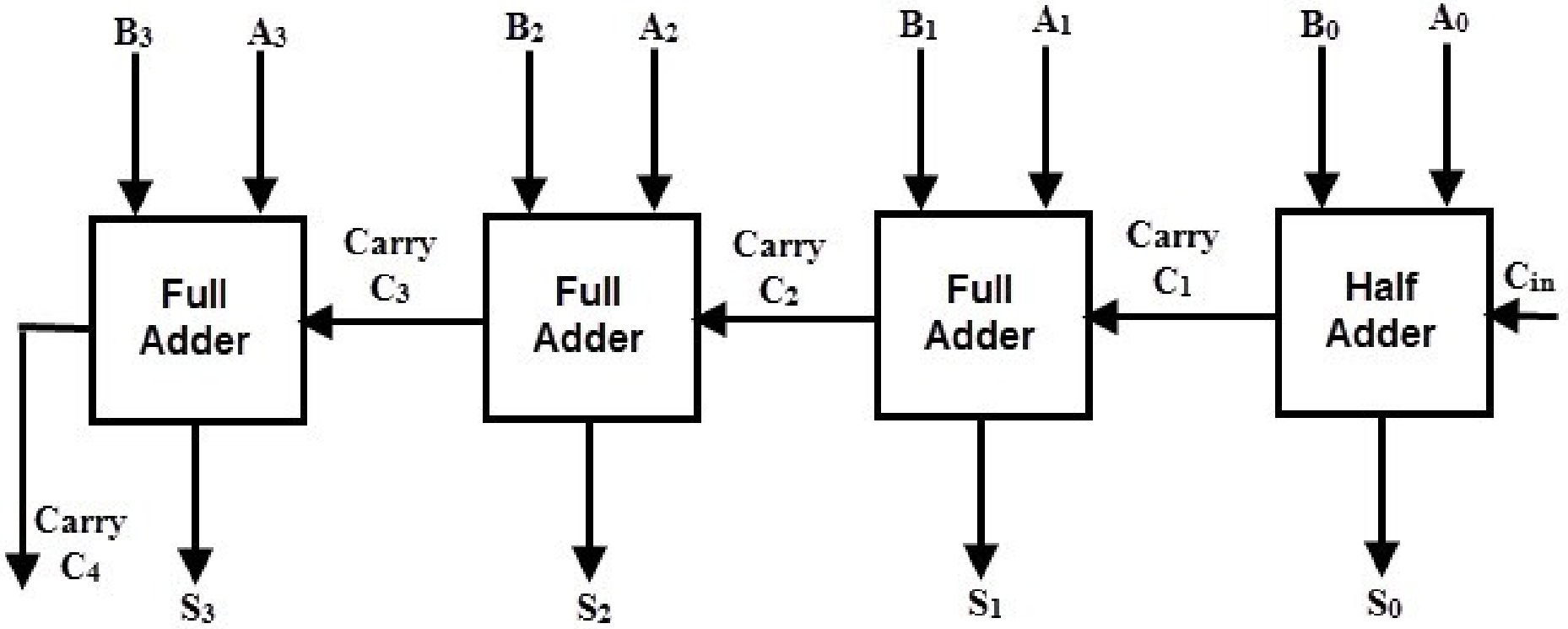


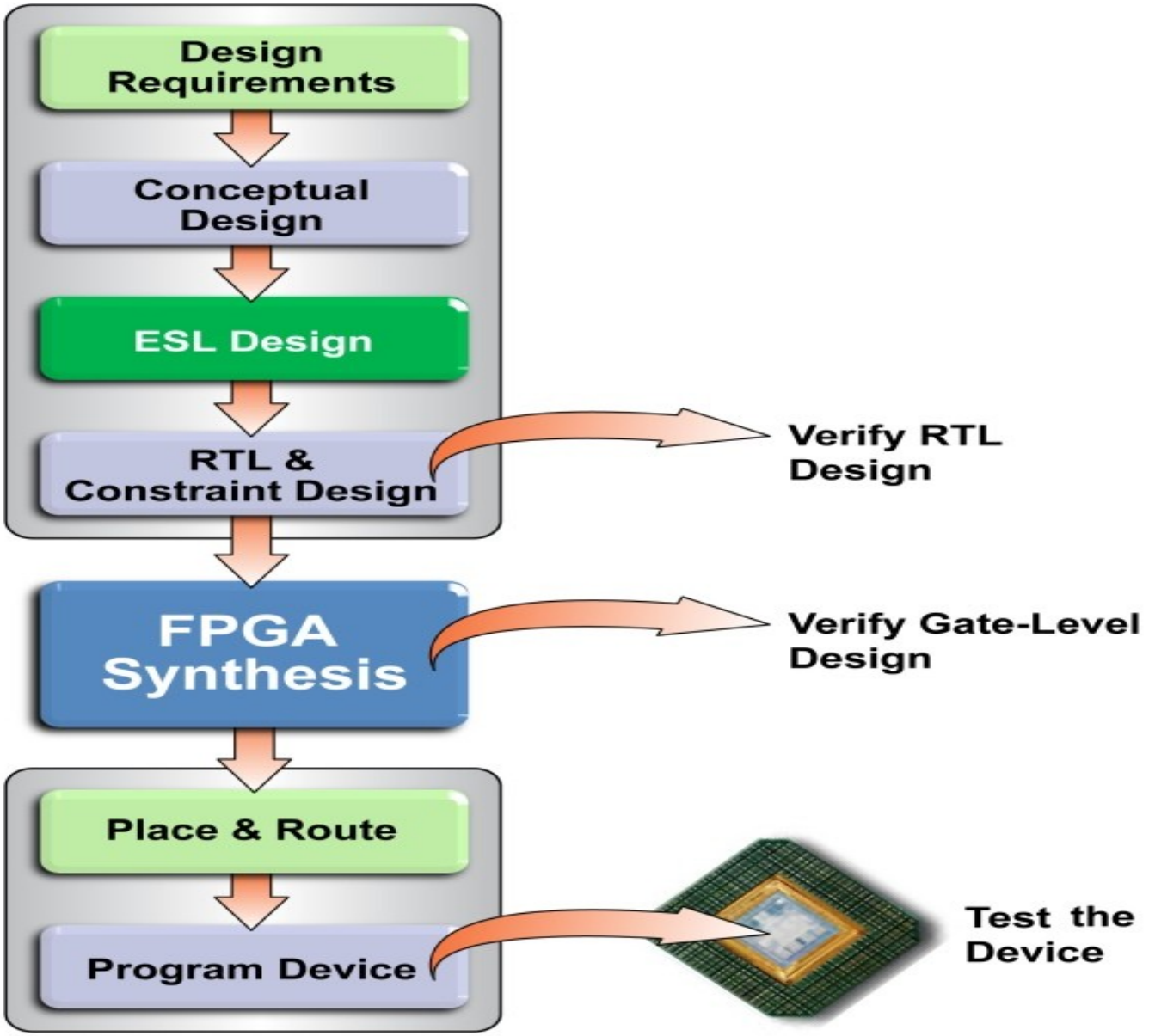
# Full Adder – Another Approach



# 4 bit Adder – Structural Modelling



# Design Flow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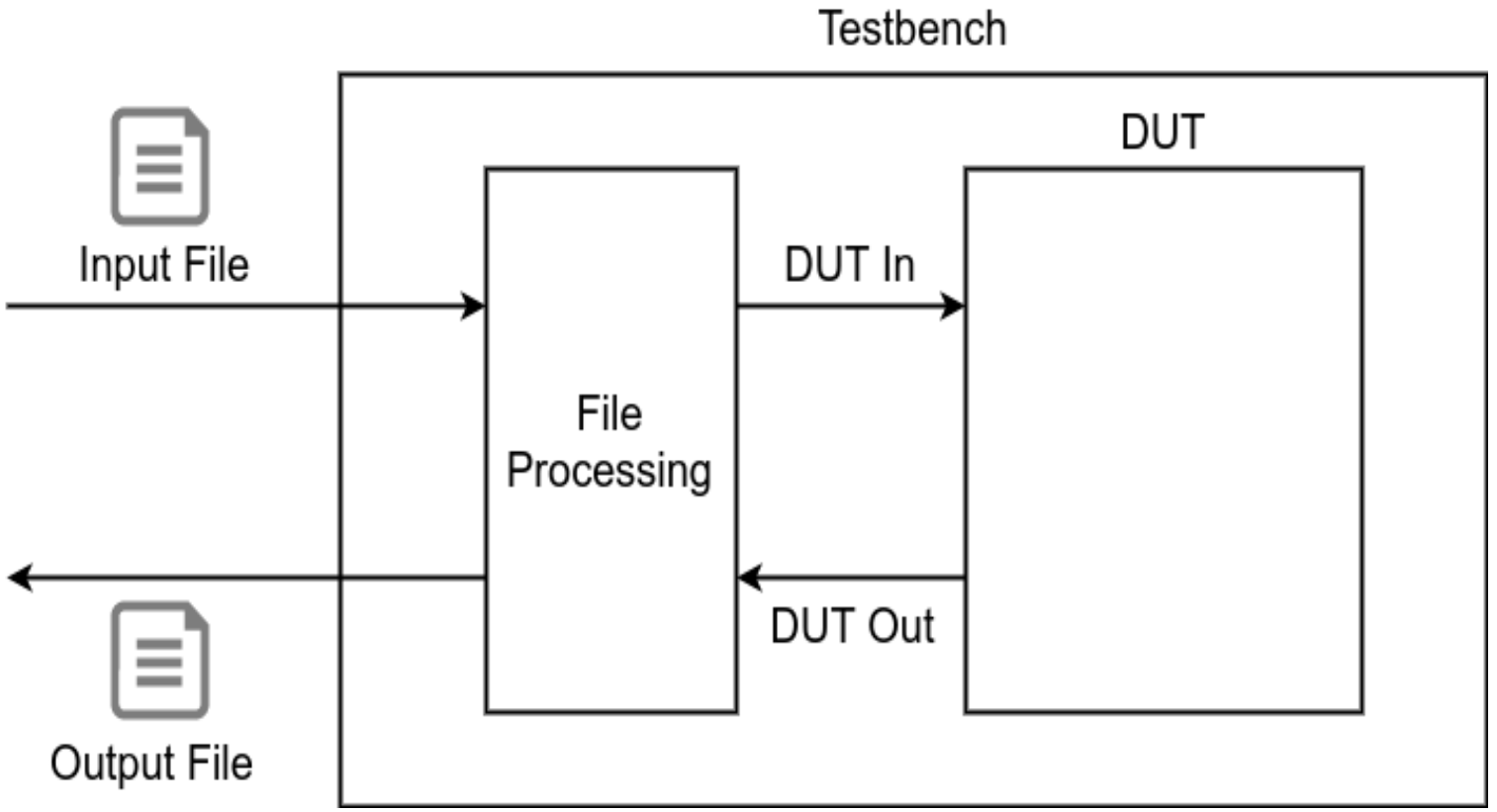
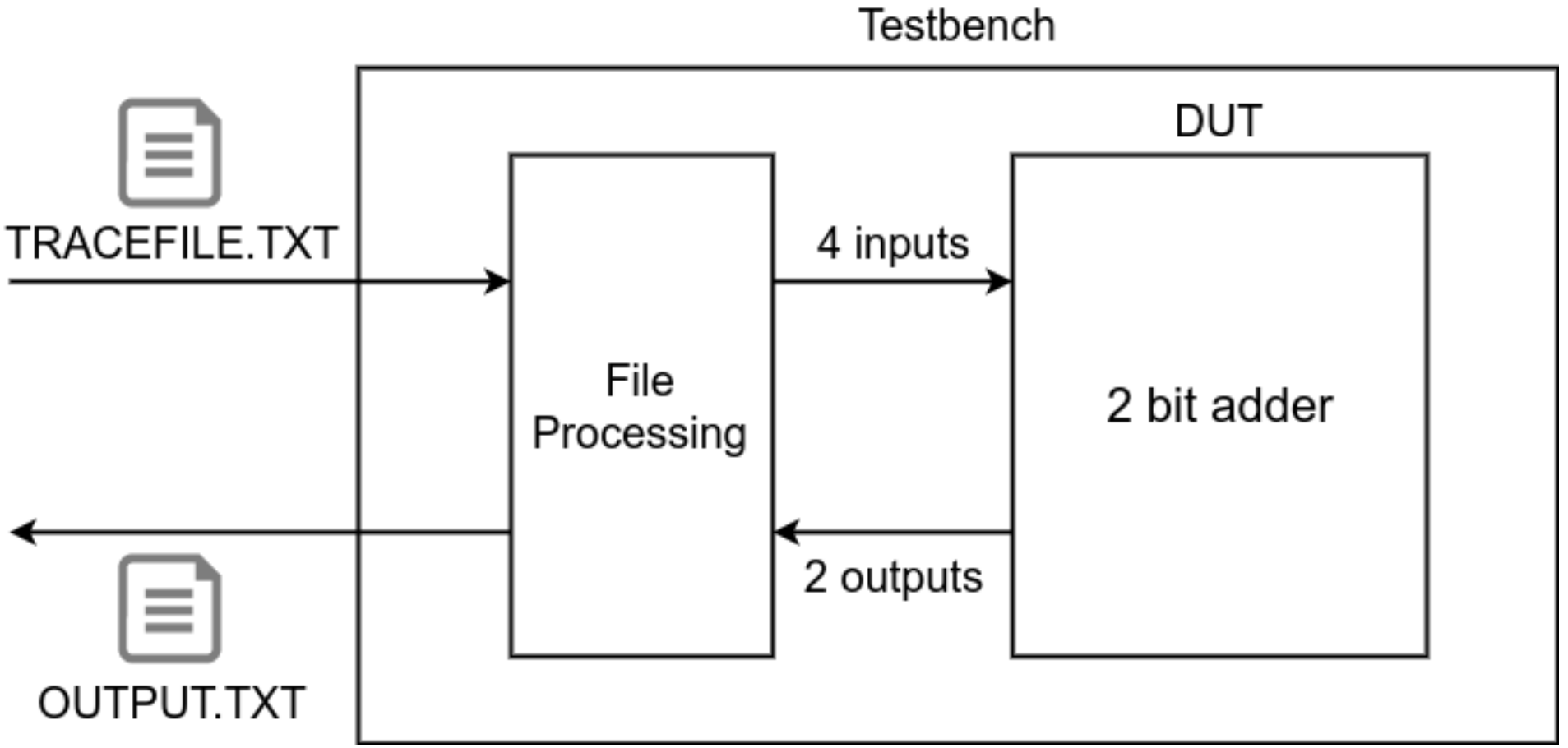
# Design Verification

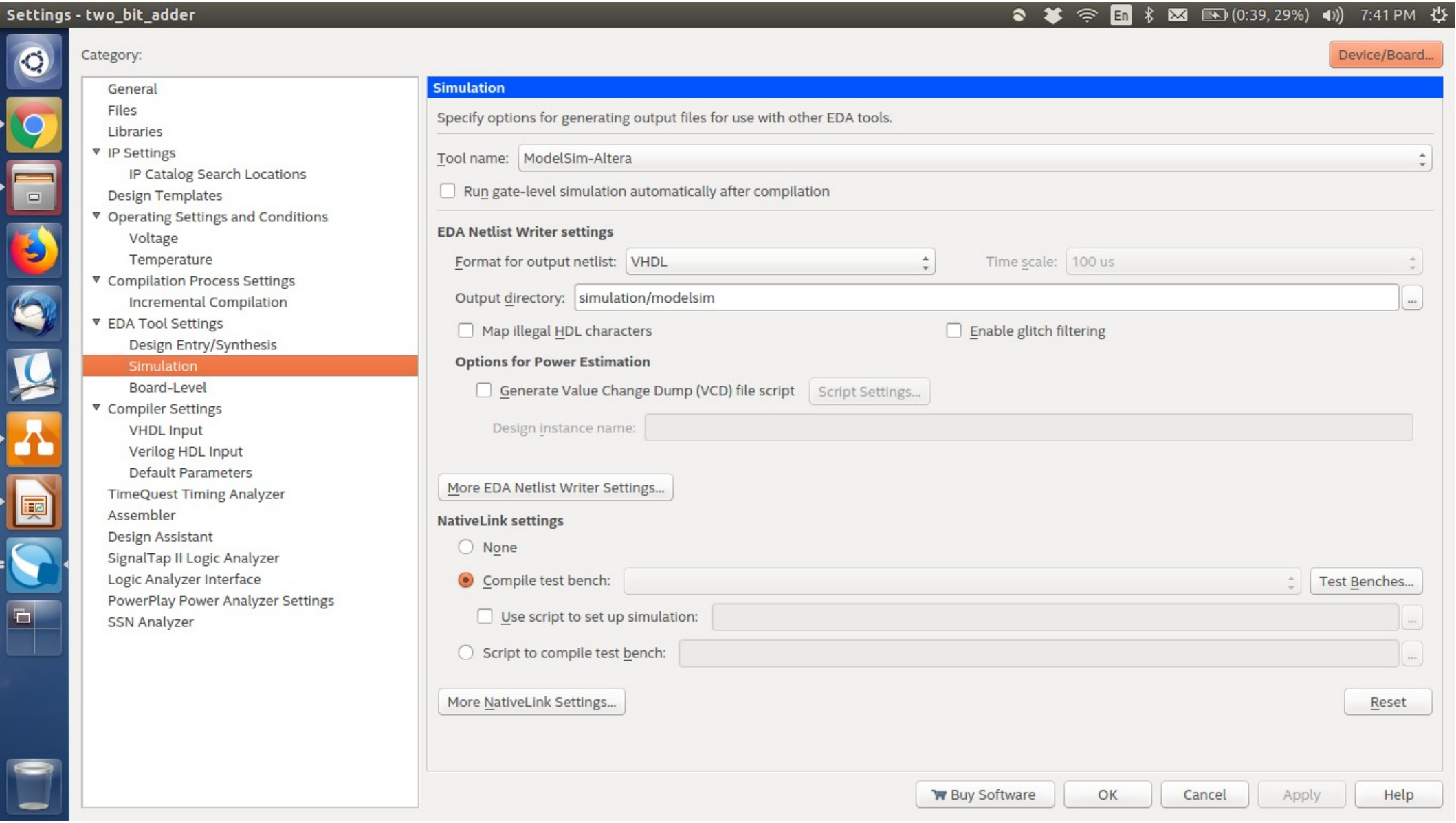
- RTL Simulation
- Gate Level Simulation
- Test Benches



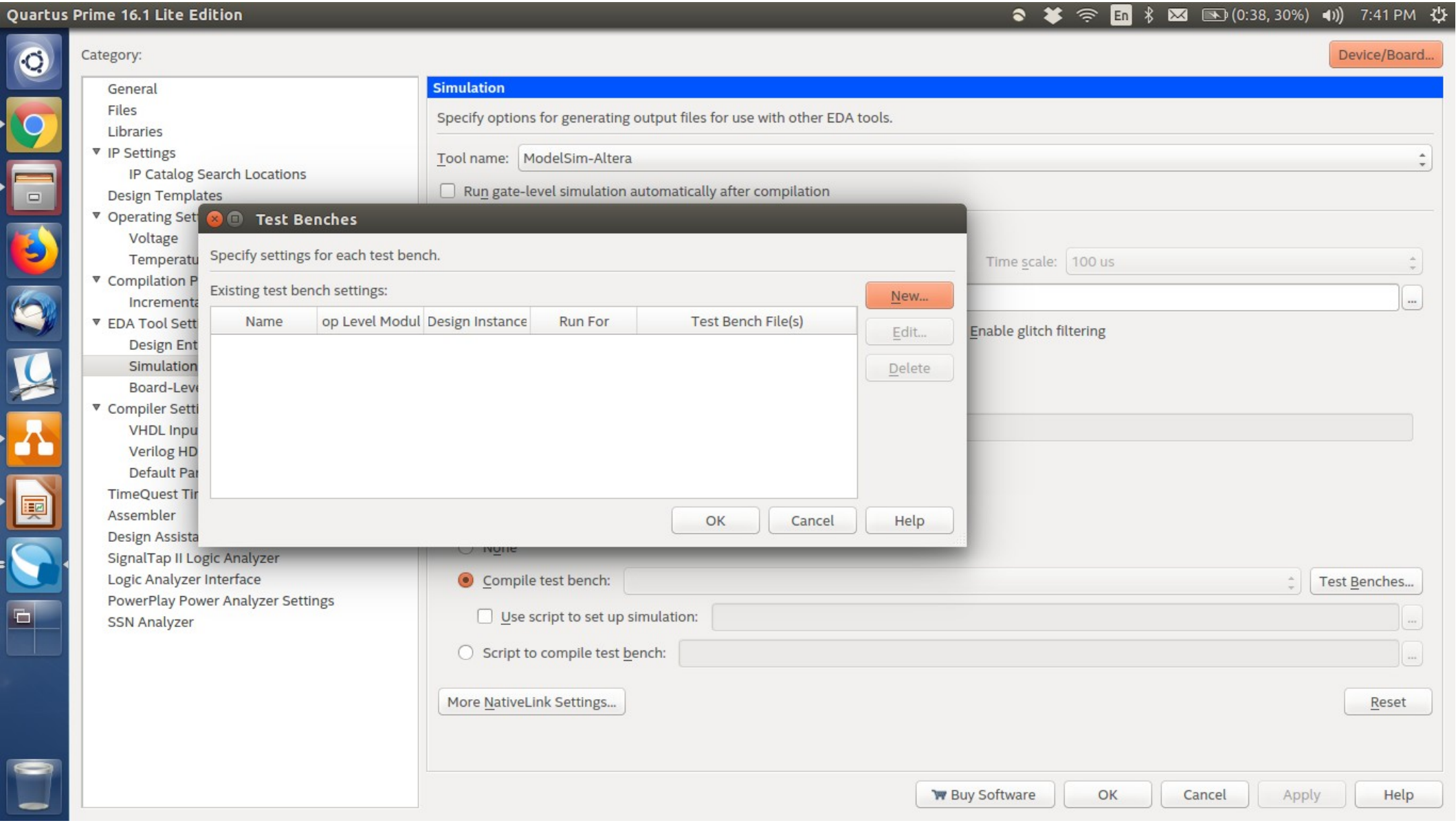
# Two Bit Adder Example



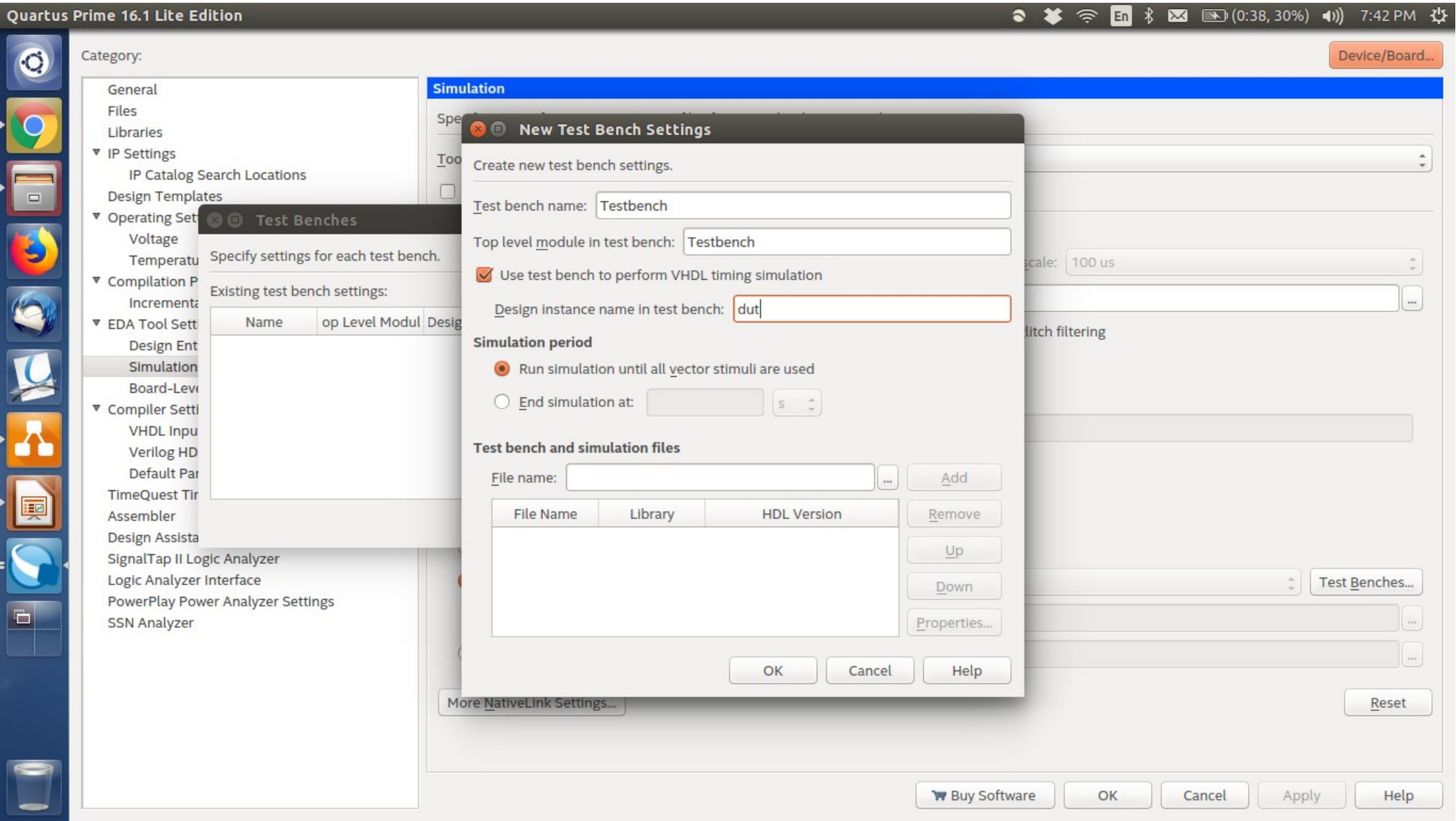
# Simulation Setup



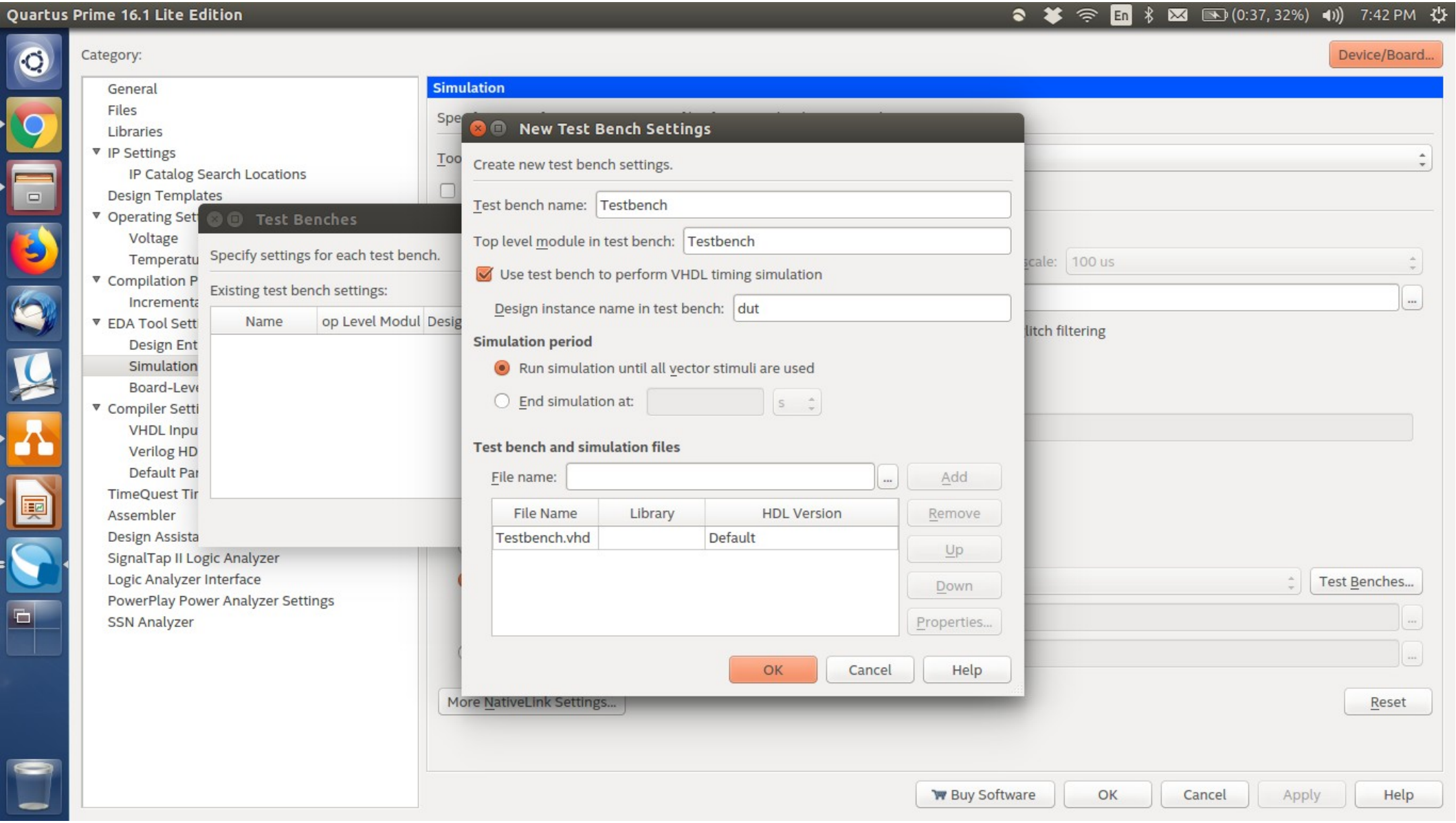
# Simulation Setup



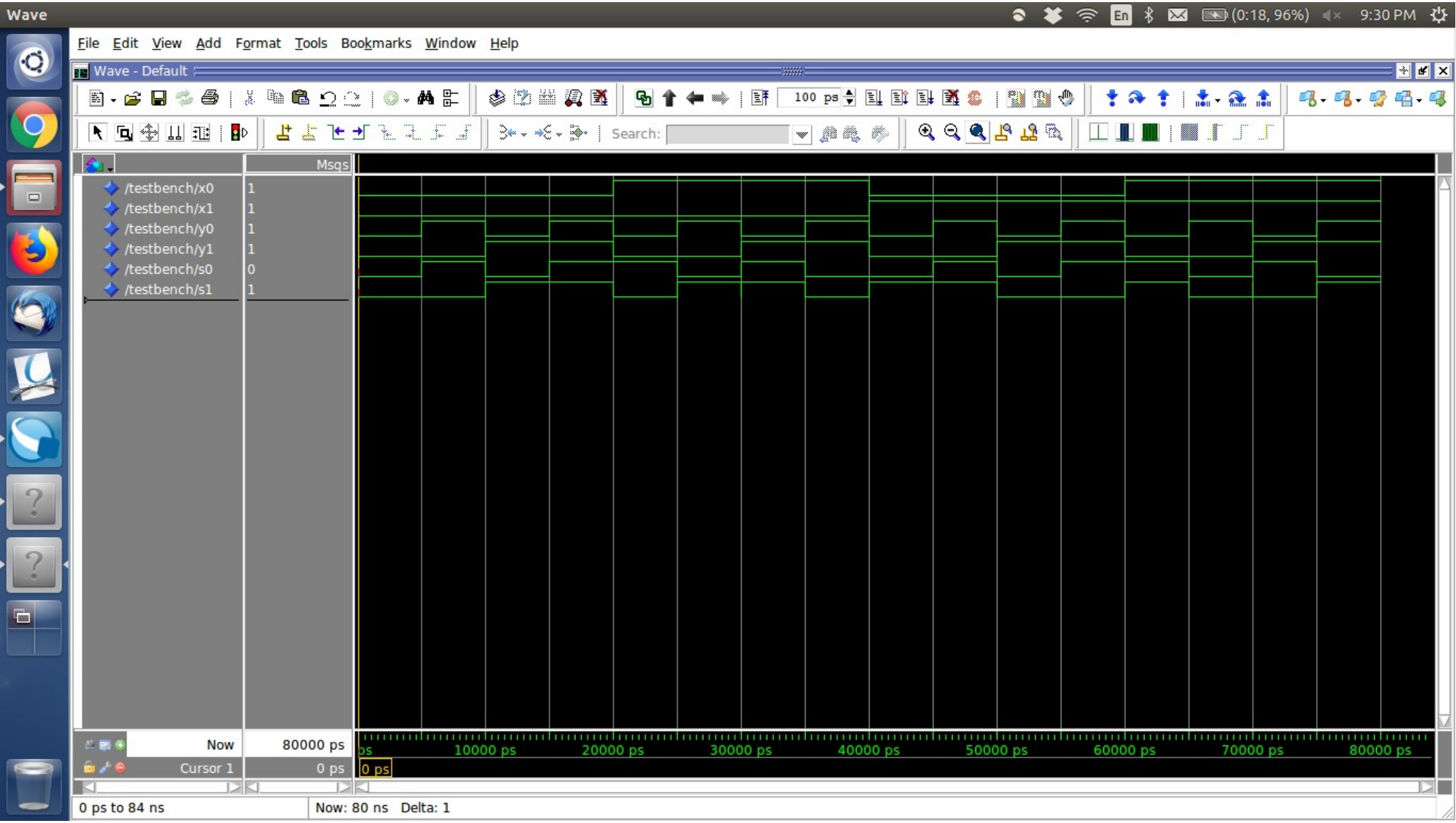
# Simulation Setup



# Simulation Setup



# RTL Simulation



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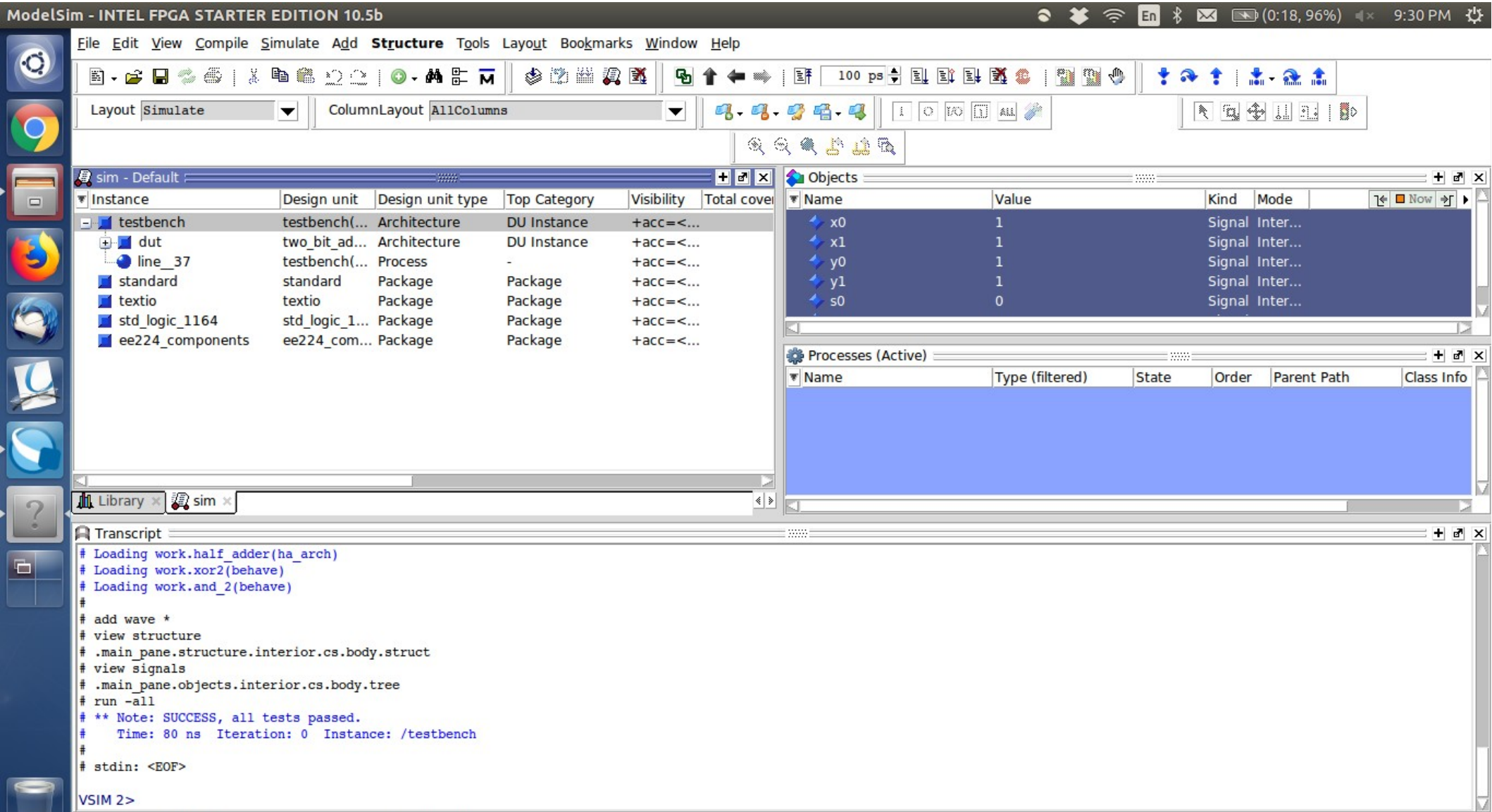
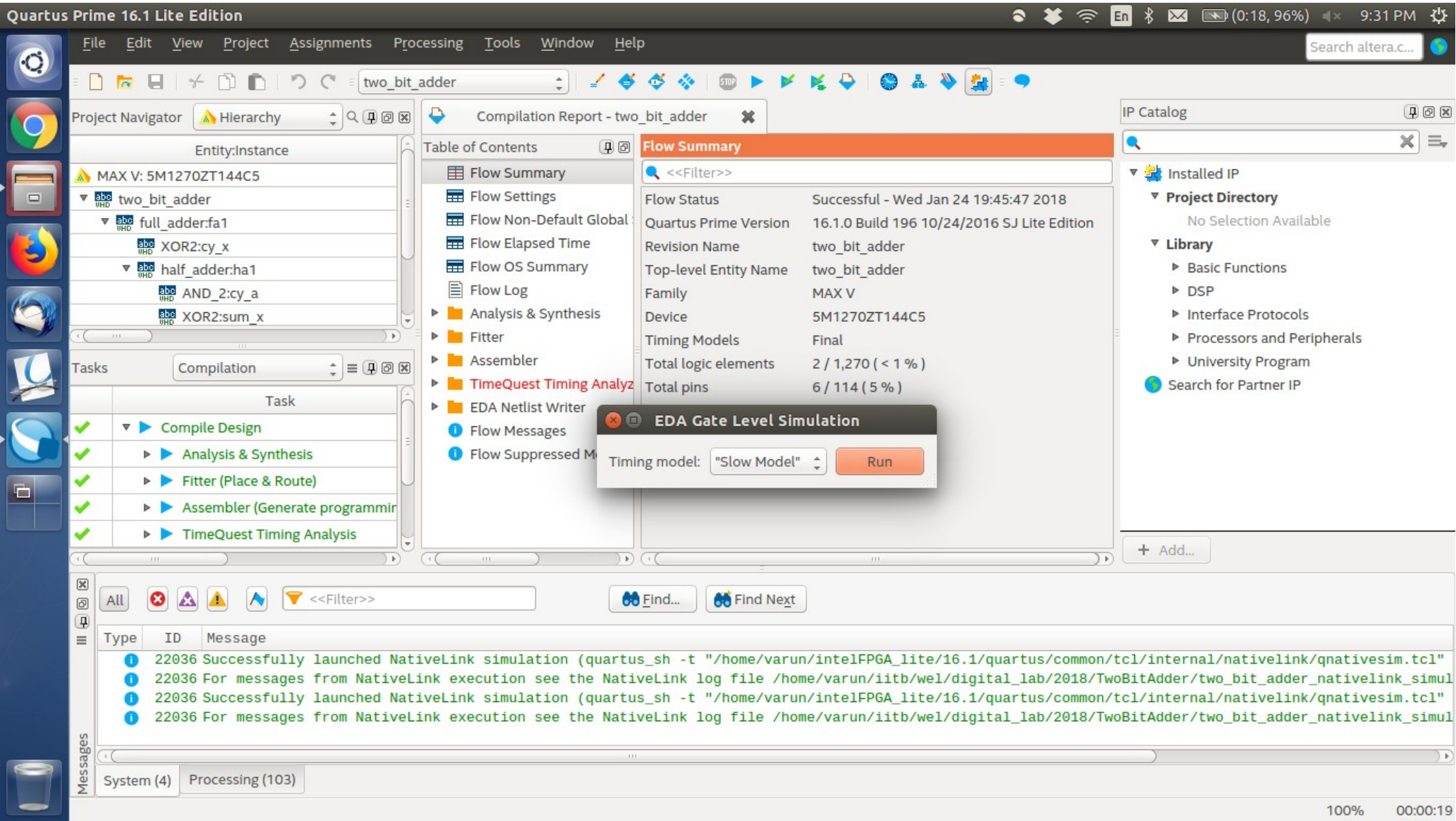
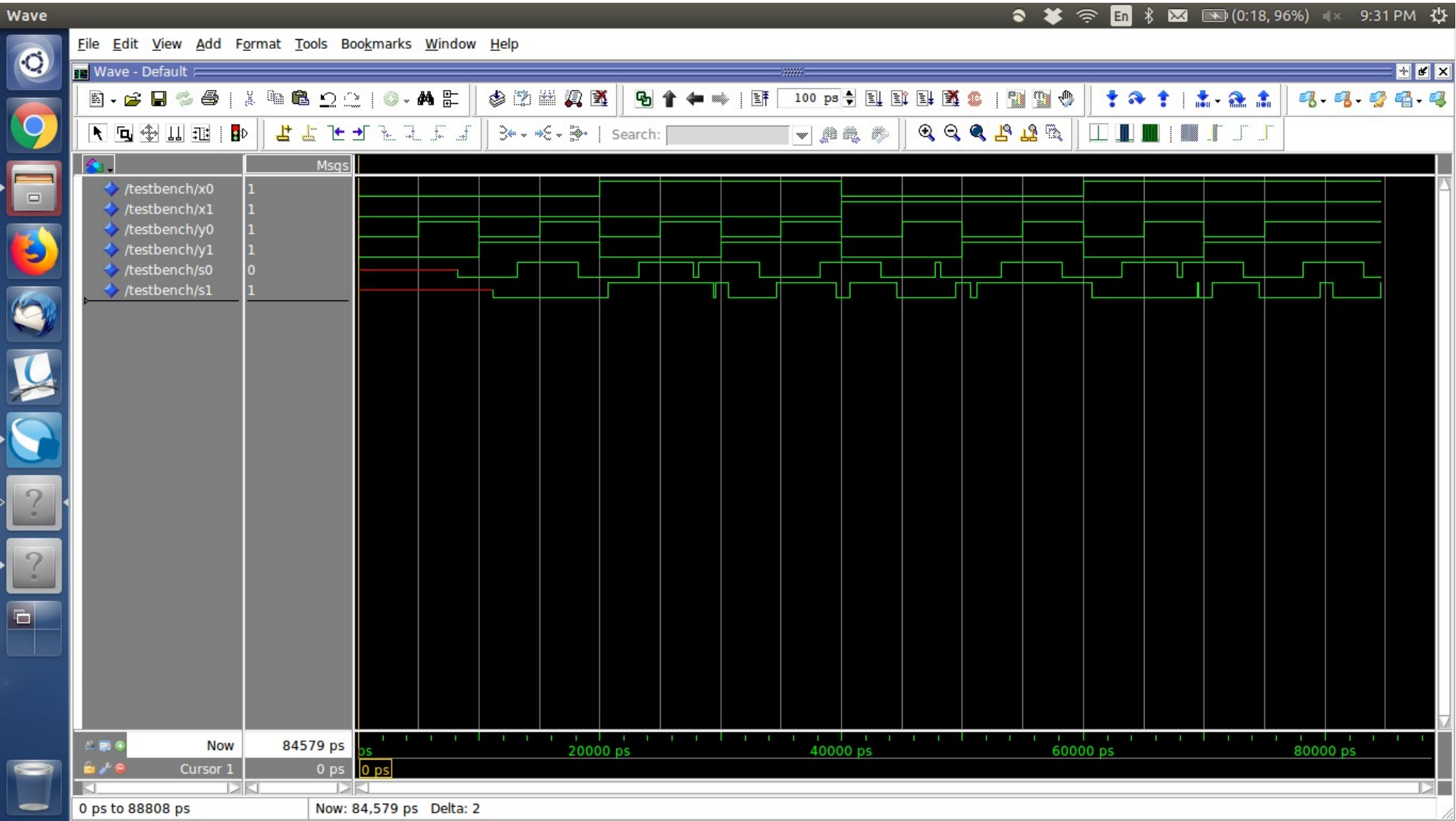


# Gate Level Simulation -Failiure



# Gate Level Simulation -Failiure



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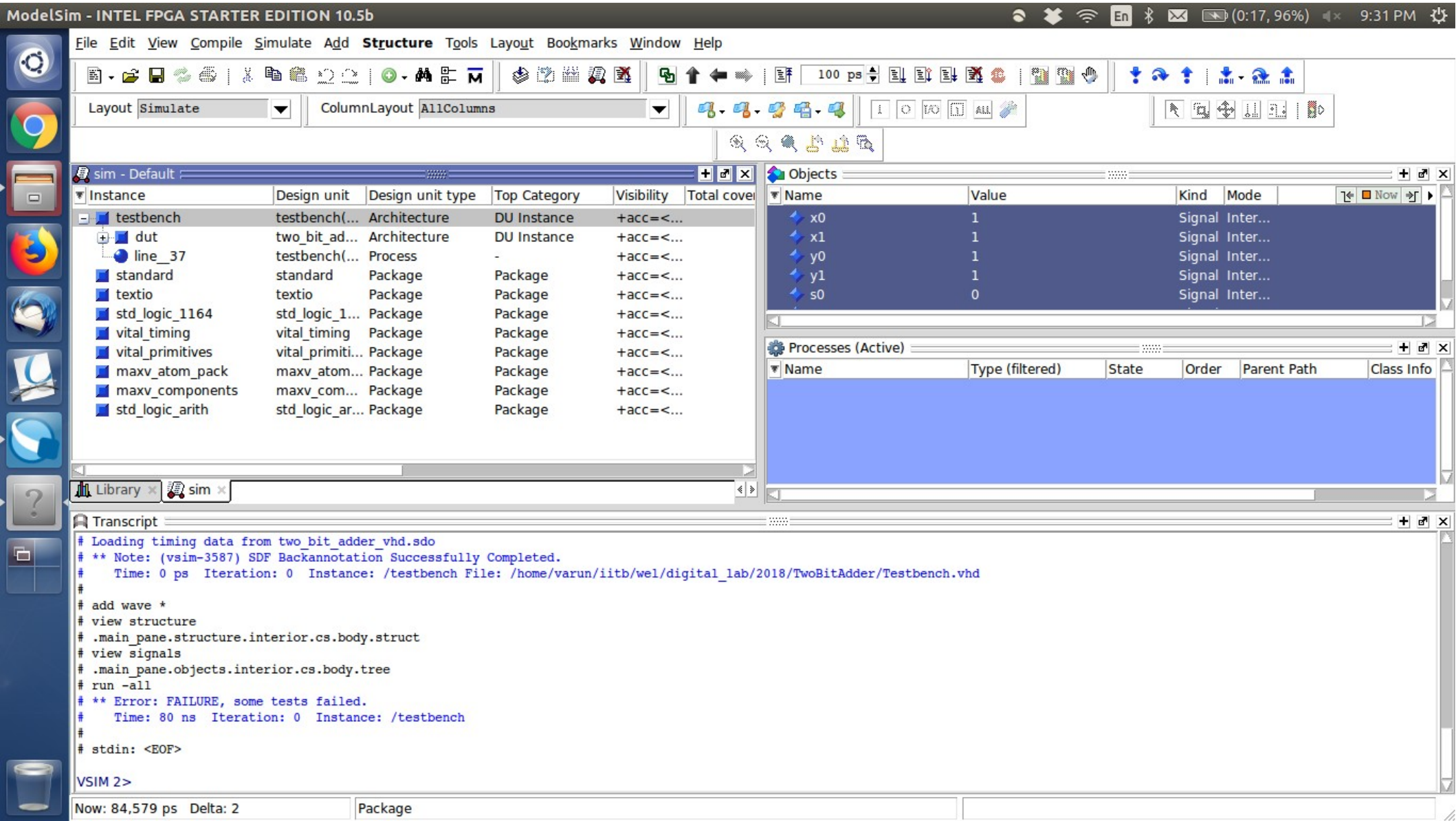
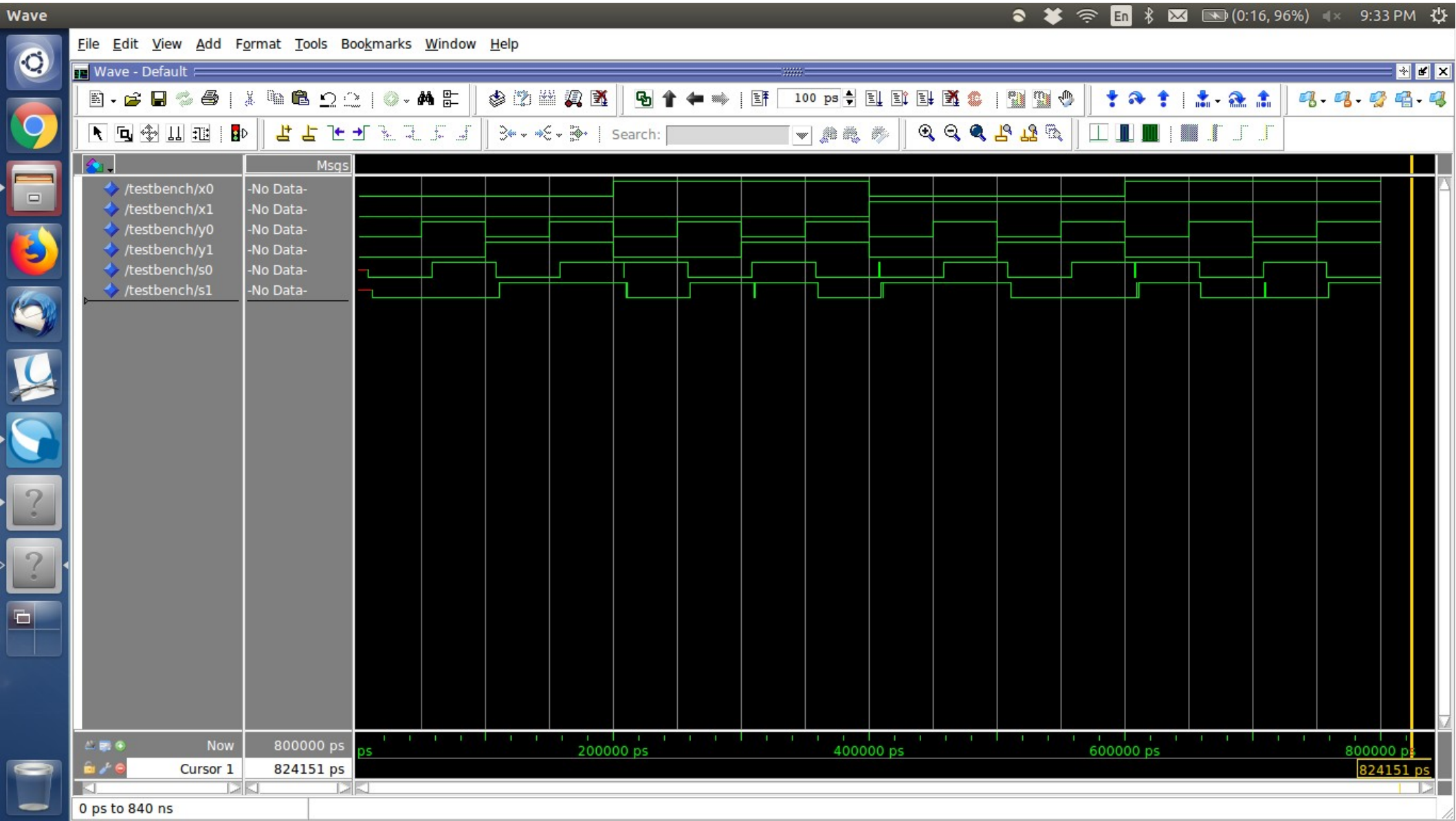
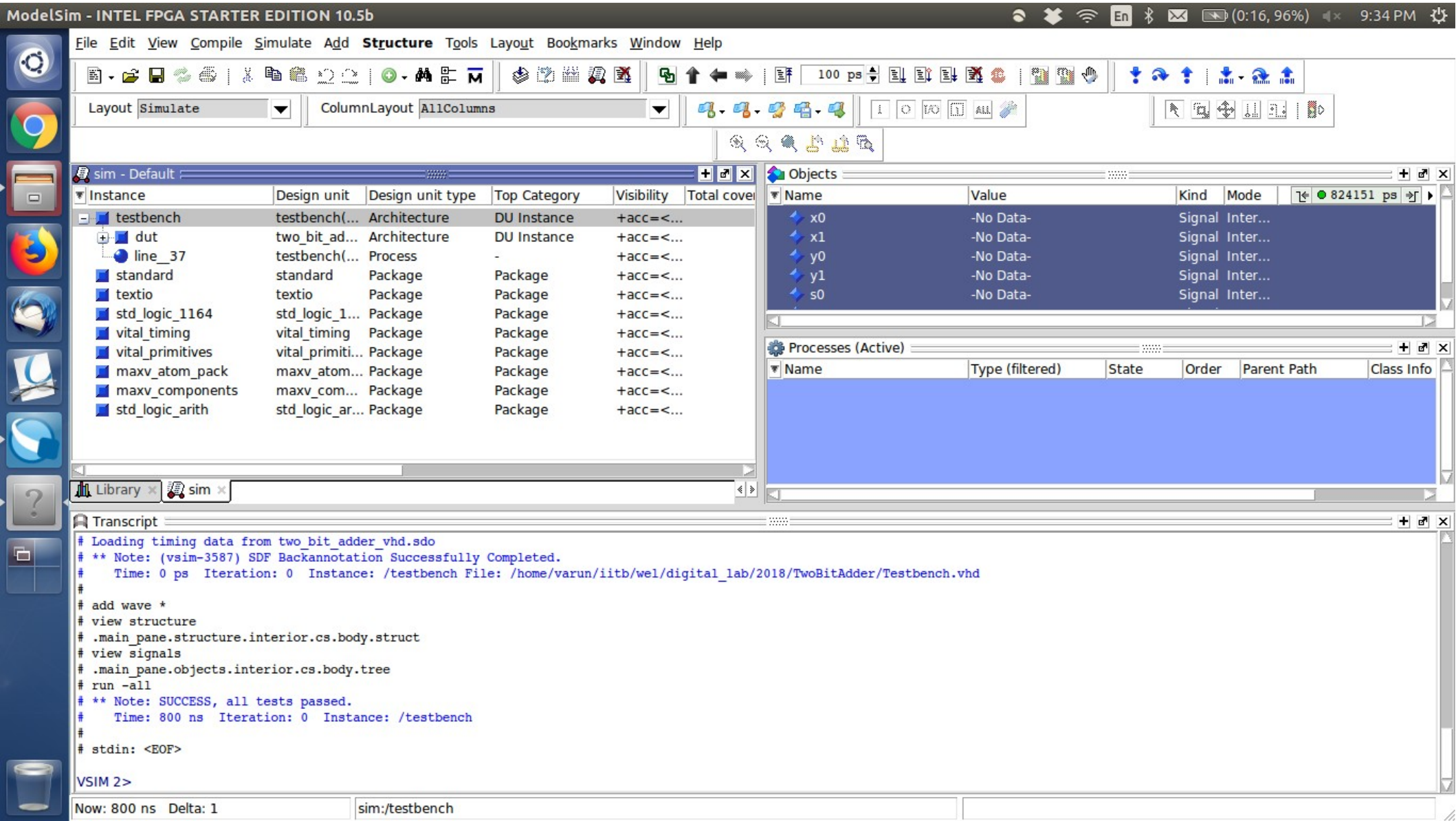


# Gate Level Simulation - Success



# Gate Level Simulation - Success



- Device
  - 5M1270ZT144C5

  JTAG Commands
  - JTAG
  - cable ft2232 vid=0x0403 pid=0x6010
  - detect
  - svf <filename> progress