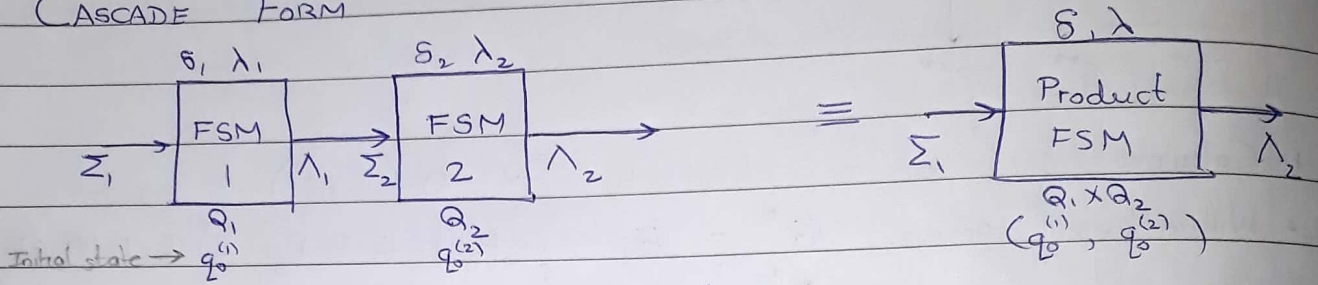
→ Combination of FSMs

- Easier debugging
- Modularity
- Smaller problem size

III CASCADE FORM

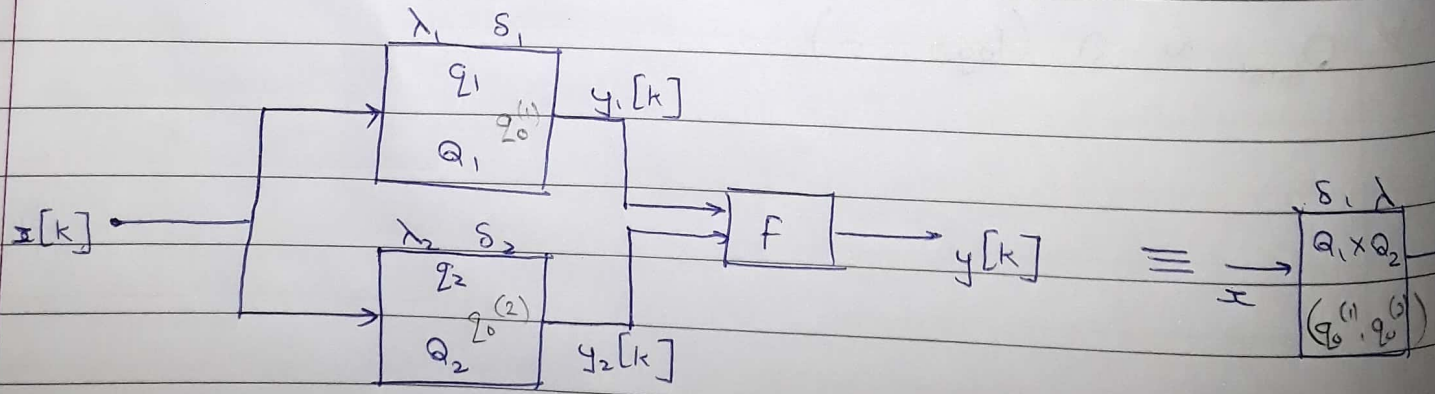


eg. 15-step counter using 3-step × 5-step

- $\delta((q^{(1)}, q^{(2)}), x) = (\delta_1(q^{(1)}, x), \delta_2(q^{(2)}, \lambda(q^{(1)}, x)))$ For nq
- $\lambda((q^{(1)}, q^{(2)}), x) = \lambda_2(q^{(2)}, \lambda_1(q^{(1)}, x))$ For y

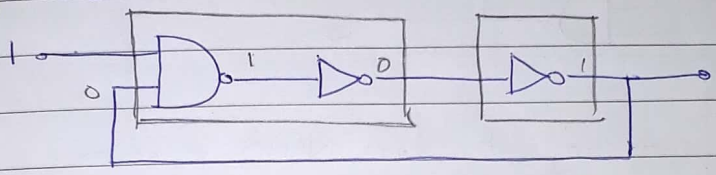
/3 Parallel FSMs

III PARALLEL FORM



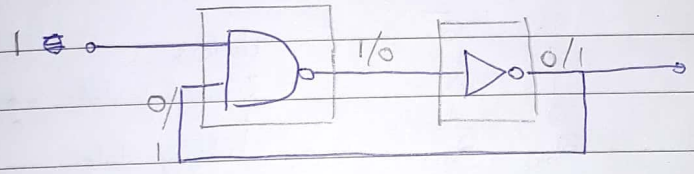
- $\delta[(q_1, q_2), x] = (\delta_1(q_1, x), \delta_2(q_2, x)) = nq[x]$
- $\lambda[(q_1, q_2), x] = f(\lambda_1(q_1, x), \lambda_2(q_2, x)) = y[x]$

∴ eg Oscillatory cascade



No stable output

∴ eg Cascade with uncertain output



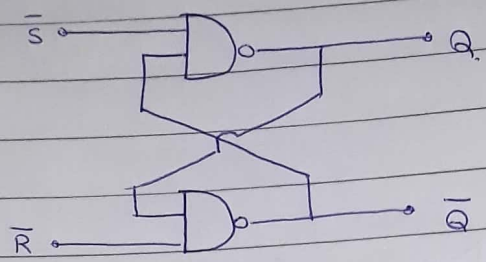
Two possible stable outputs

- Hence, we avoid combinatorial logic loops.

→ y

IV D Flip Flop

A] SR Bistable

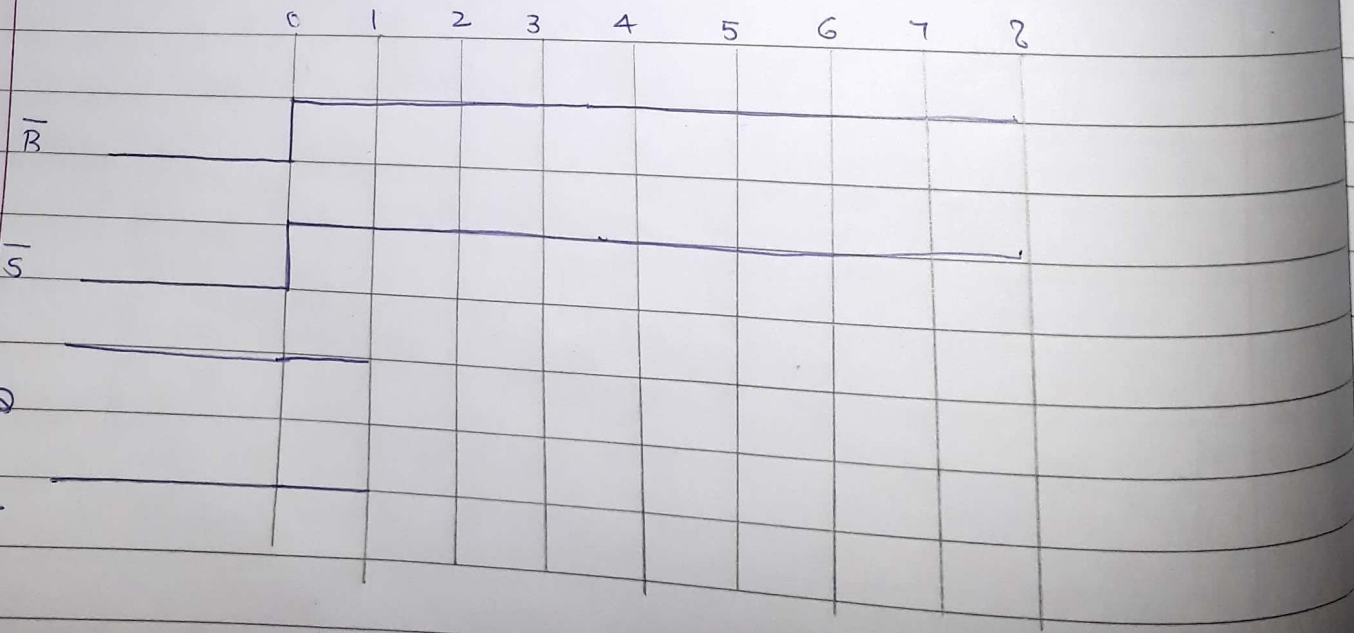


- Contains loop consisting of two NAND in series.
- Can store one bit (Q) ~~at~~ for given $\bar{S}, \bar{R}$

	$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
×	0	0	1	1	useless
	0	1	1	0	} forcing state → Set
	1	0	0	1	→ Reset
	1	1	Q_{old}	$\bar{Q}_{old}$	..... holding state

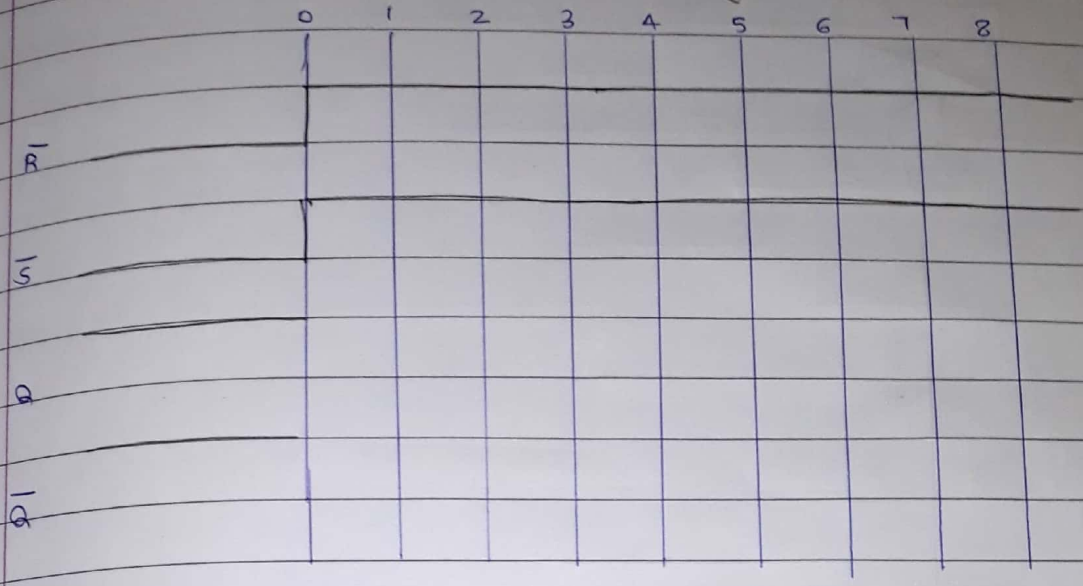
15/3

- ~~For~~ $(\bar{S}, \bar{R}) \equiv (0,0)$, the circuit is entering an indeterminate. ~~For any future input~~, ~~We~~ cannot know what value Q will take if we give $(\bar{S}, \bar{R}) \equiv (1,1)$ just after $(0,0)$



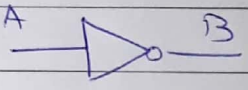
if both NAND gates have delay !

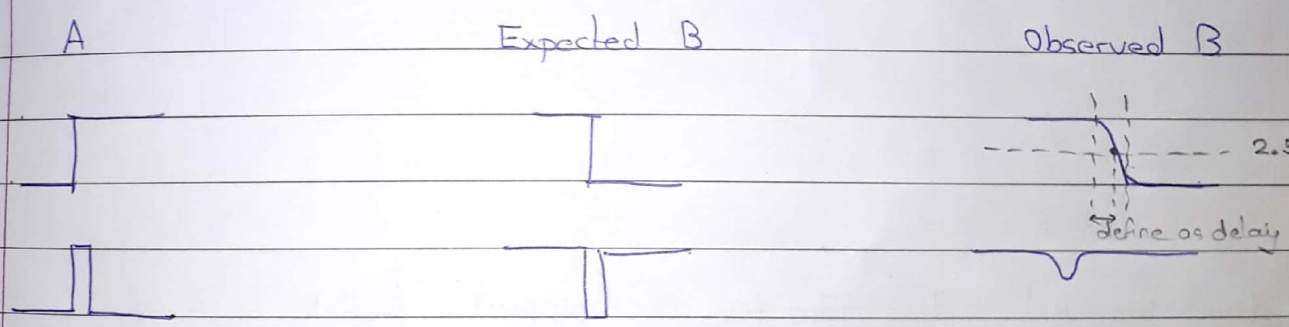
If NAND with $\bar{S}$ has delay 0.1 instead of 1



5/3

→ Problems in our delay model

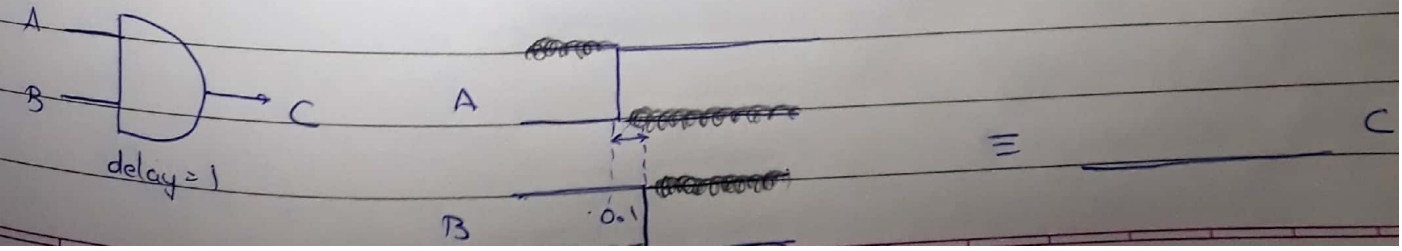


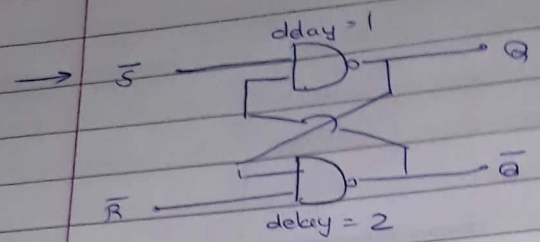


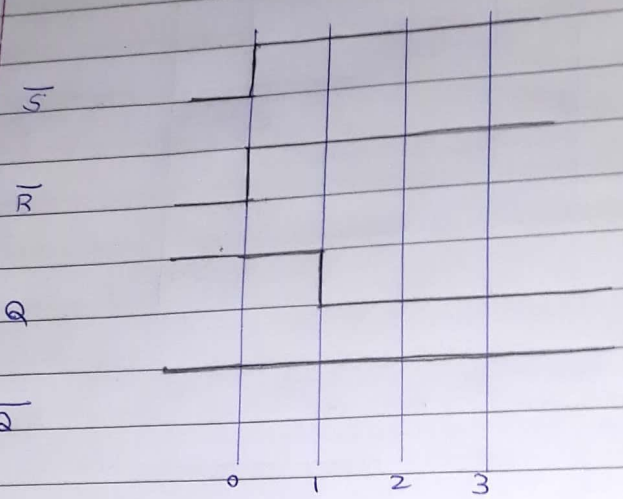
→ Inertial Delay Model

If the input pulse width is narrower than the delay of the gate, it does not appear at the output.

eg





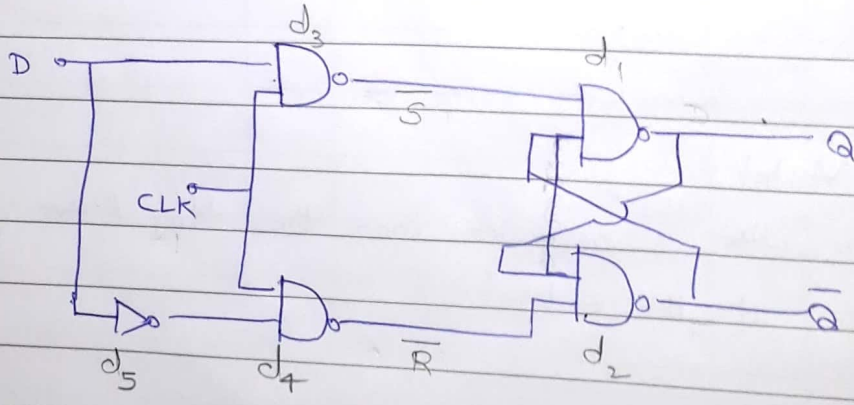


Change in Q is swallowed by lower NAND gate

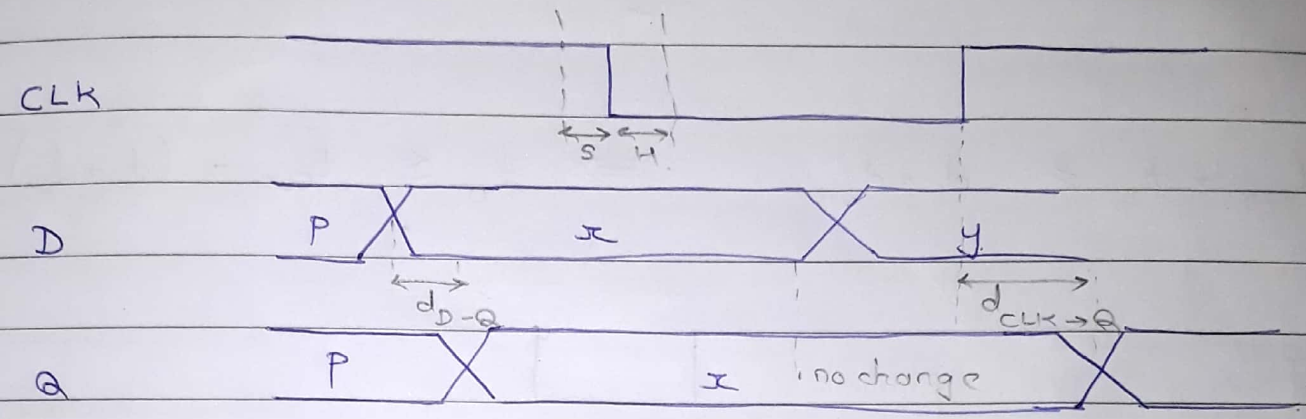
- How long should $\bar{S}$ be made 1 to change both Q & $\bar{Q}$ successfully

3

B] → Level-triggered ~~D-Flip flop~~ (~~latch~~) Latch



- When CLK = 1, Q = D .... after a small delay
  When CLK = 0, Q holds its previous value.
  Hence, the negative edge of CLK is the sampling instant of D.
  When CLK = 0, Q holds value of D that was at negative edge of CLK
- This is not a flip-flop because Q follows D all throughout CLK instead of just at positive edge.

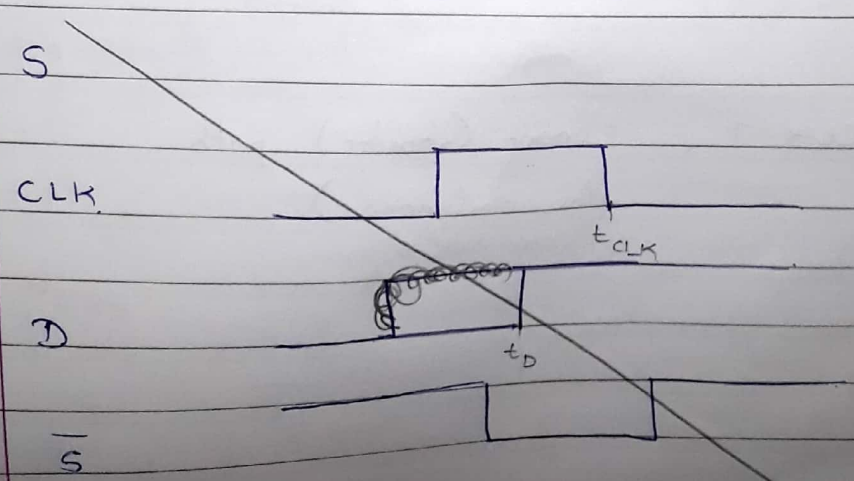


- For correct sampling of D, value of D should not change in 'S+H' time. We cannot comment on final Q if it does

→ H = 0

?

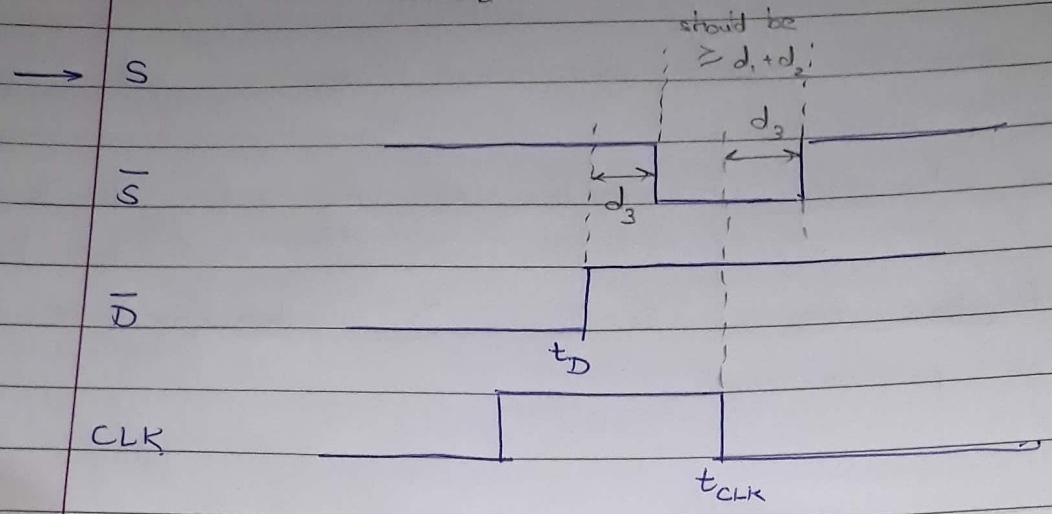
→ S



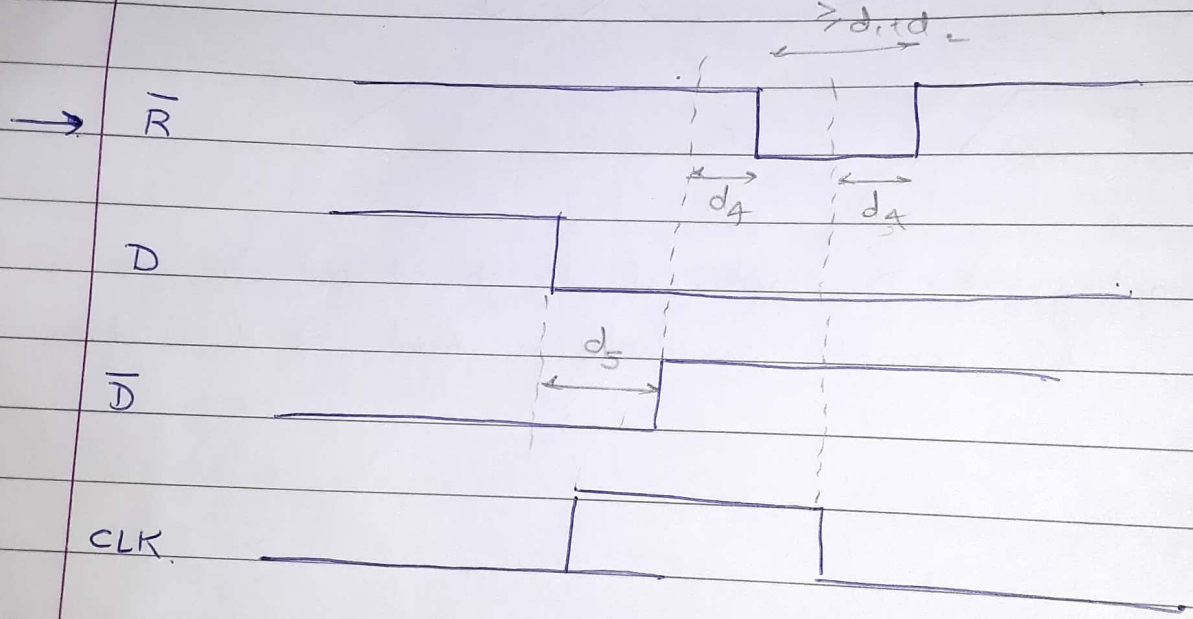
$S = d_1 + d_2 + d_5$

$d_{D \to Q} = d_1 + d_3$ or $d_4 + d_1 + d_2 + d_5$

$d_{CLK \to Q} = d_1 + d_2$ or $d_4 + d_1 + d_2$



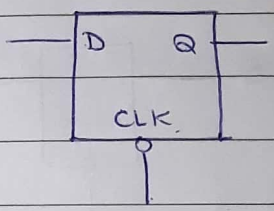
$t_{CLK} - t_D \geq d_1 + d_2 \Rightarrow t_D \leq t_{CLK} - (d_1 + d_2)$



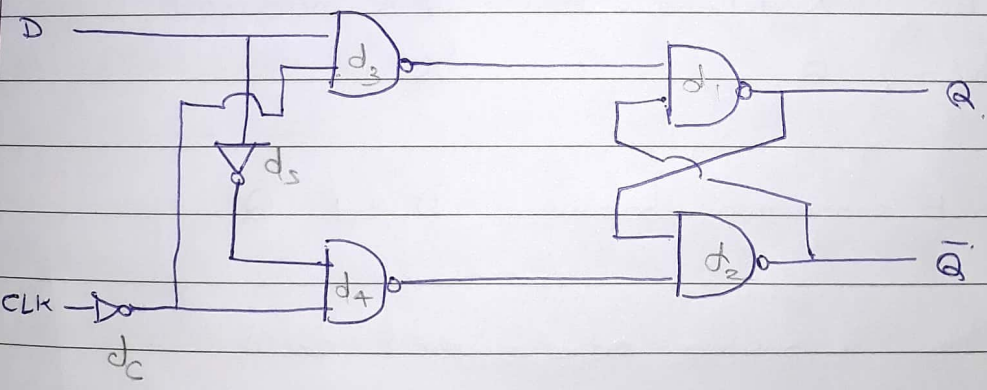
d_{CLK-Q}

- If D = 1 when CLK ↑, upper (shorter) path.
  D = 0 , lower (longer)

A Inverted clock latch.



- Rising edge of CLK is now sampling edge.
  - When CLK is low, Q follows D
  - high, Q will become D at falling edge.



→ $d_{D \to Q}$ ≡ same

$d_{\uparrow}$ H = d_6 (previous H + d_6)

S = previous S − d_6

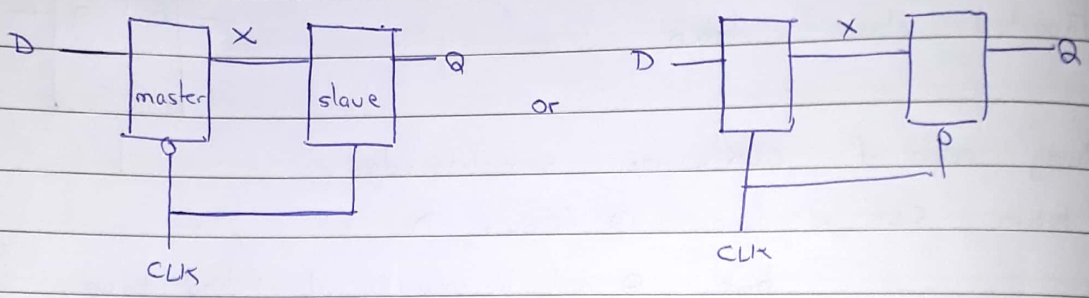
$d_{CLK \to Q}$ = previous + d_6

— CLK

D

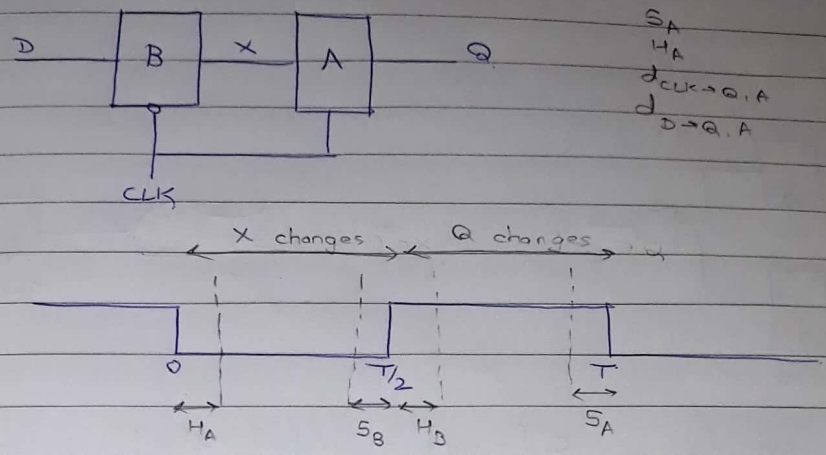
Q

3 Master - Slave Flip-flop



- When CLK is low, X follows D. Q is unchanged
  high, Q X X
- There is no direct connection between D and Q.
- This behaves like a positive edge-triggered circuit.

20/3 • Sampling edge :- Master - Positive
Slave - Negative



S_A, H_A, $d_{CLK \to Q, A}$, $d_{D \to Q, A}$

S_B, H_B, $d_{CLK \to Q, B}$, $d_{D \to Q, B}$

- t_D = time at which D changes

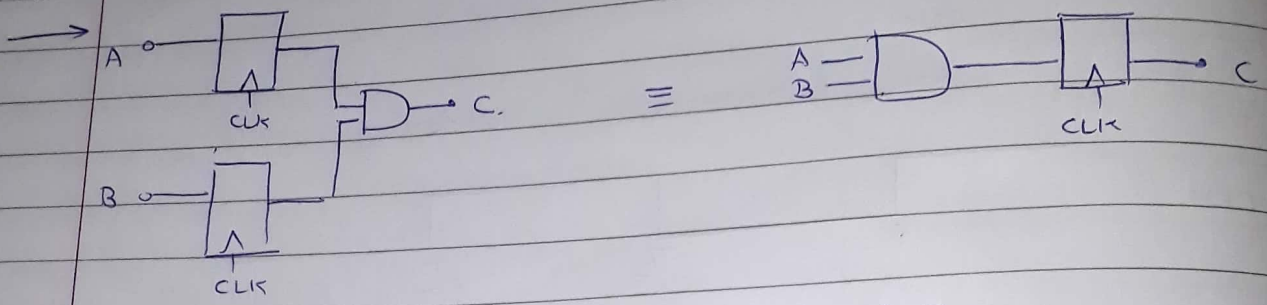
If we want D to appear at X, $t_D \leq \frac{T}{2} - S_B$

don't want " " " " later, $t_D \geq \frac{T}{2} + H_B$

- Changes in X :- (CLK is low)
  - X changes earliest when CLK ↓ :- $d_{CLK \to Q, B} \geq H_A$
  - latest when CLK is low and D updates latest :- $\frac{T}{2} - S_B + d_{D \to Q, B} \leq T$

- Changes in Q :- (CLK is high)
  - Earliest, when CLK ↑ :- $\frac{T}{2} + d_{CLK \to Q, A}$
  - Latest :- Latest of $X + d_{D \to Q, A} = \underbrace{\frac{T}{2} - S_B + d_{D \to Q, B}}_{\leq T - S_A, \text{ as seen above}} + d_{D \to Q, A}$
  - No constraint on outputs (Q)

C] Retiming



For both circuits, $C[k+1] = A[k] \cdot B[k]$.

☺ • In left circuit, setup time of A & B for both flip flops is small

☹ right A-B the flip flop is large.