Power Electronics

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Outline of the course

⇒ Introduction

⇒ Power semi-conductor devices

⇒ AC-DC converters

⇒ DC-DC converters

⇒ DC-AC converters

⇒ AC-AC converters

Reference Books:

1. M.H.Rashid,"Power Electronics: Circuits, Devices & Application" Prentice hall of India, (IIIrd Ed.),2004.
2. Ned Mohan, "Power Electronics, Applications & Design", John Wiley & Sons., (IIIrd Ed.) 2002.
3. Cyril Lander, "Power Electronics", McGRAW Hill Co., (IIIrd Ed.), 1993.
4. B.K.Bose, "Modern Power Electronics & A.C. Drives", Pearson Education Inc., 2002.

Introduction :

Quotes from IEEE papers :

We now live in a truly global society.

In the highly automated industrial front with economic competitiveness of nations, in future two technologies will dominate :

Computers and power electronics - the former providing intelligence as to "what to do" and the latter - "the means to do it".

⇒ "Modern computers, communication and electronic systems get their life blood from power electronics"

⇒ "Solid state electronics brought in the first electronics revolution, whereas solid-state power electronics brought in the second electronics revolution"

Energy scenario :

Globally 87% of total energy from fossil fuel (coal, oil & natural gas)

 6% nuclear

Remaining from renewable (hydro, wind, solar)

[In India 70% coal]

⇒ World has limited fuel

Projected that natural uranium fuel is expected to last 50 years

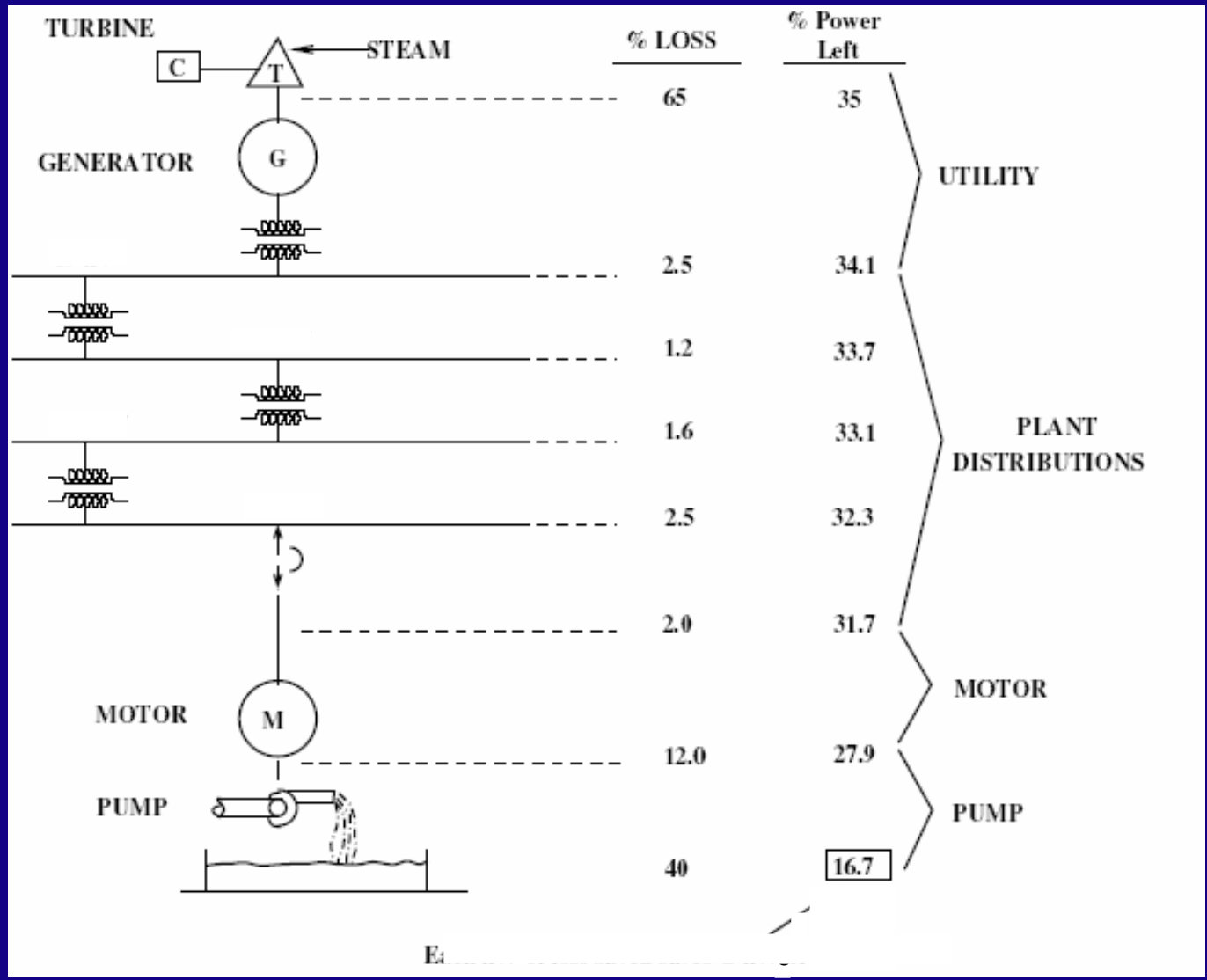
Oil for 100 years

Natural Gas 150 years and

Coal 200 years

Will the wheels of civilization come to a halt at the end of the 22nd century?

How to solve / mitigate the problem?



If i/p is 100 KW of fuel energy, output is around 15-20 KW of useful work,

⇒ Why spend much effort on motors and their equipment when losses are the front end?

⇒ Answer : Every KW of loss saved in the process drive, 6KW of fuel energy gets saved on the front end.

Can power from renewables (wind, solar) be explored?

Nuclear power plant ⇒ Safety

⇒ Waste handling

Burning fossil fuel ⇒ CO_2, NO_2, O_3, CO etc.

⇒ Fly ash

⇒ Global warming

⇒ Climatic changes

In 1997, conference at Kyoto, Japan

Protocol : Developed countries agreed to specific targets for cutting their emissions of gases.

[Mt. Everest losing height 10cm every year]

⇒ Affects agriculture & vegetation

Urban pollution ⇒ IC engine vehicles

⇒ Use electrical energy very efficiently

⇒ Increase the conversion efficiency

⇒ Estimated that 15-50% electricity consumption can be saved by extensive use of power electronics.

Bulk of the power is consumed by

⇒ Electric motors ⇒ majority are IM (constant speed m/c)

⇒ Common loads (fans, pump)

⇒ Lighting

Fan : $T_L \propto \omega^2$; $P \propto \omega^3$

If $\frac{\omega_1}{\omega_2} = \frac{1}{2}$; $\frac{P_1}{P_2} = \frac{1}{8}$

$\Rightarrow$ Frequency converter

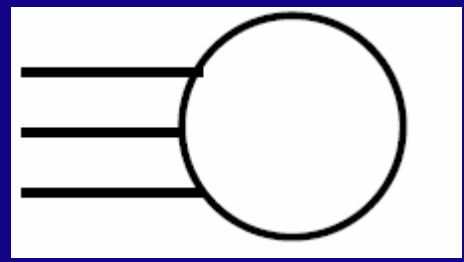
$\Rightarrow$ $\because$ Input 'F' can be $\downarrow$, $N_s - N_r = N_s$ at s=1 $\downarrow$

$\Rightarrow$ $\because$ N_s is low, magnitude of inrush current $\downarrow$.

$\Rightarrow$ Voltage dip can be eliminated

$\Rightarrow$ Stress on cable $\downarrow$ & life of m/c $\uparrow$.

⇒ Machine is being fed by constant V & F supply.



⇒ V is constant ⇒ Φ and ∴ core loss remains constant.

⇒ Assume that the load in the m/c is varying.

⇒ As the load ↓, variable loss ↓.

$\eta = \eta_{max}$ when core loss = variable loss

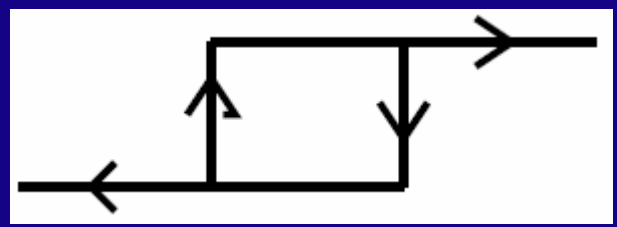
⇒ 'V' should be ↓ as load ↓.

⇒ Auto-transformer ⇒ Not a solution.

Fan Regulator - Old rugged Vs New Elegant and small in size

⇒ In Japan, 70% of air-conditioners use variable speed drives.

⇒ Smooth control.



Slip ring IM $\Rightarrow$ High Power motor

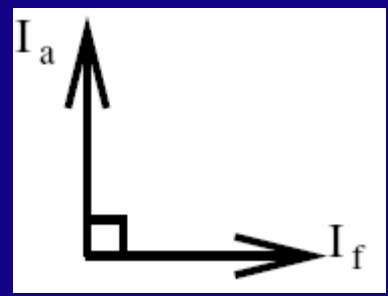
$\Rightarrow$ sP_{in} is rotor copper loss

$\Rightarrow$ can this be fed back to the source?

$\Rightarrow$ can the starting torque $\uparrow$ and starting current $\downarrow$ electronically?

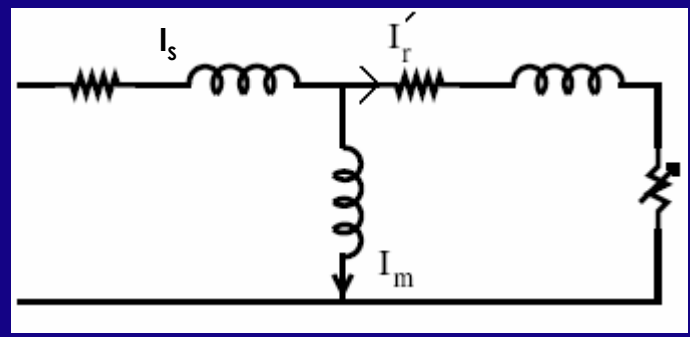
D.C. machine $\Rightarrow$ superior control characteristics

$T = kI_aI_F$



I.M. machine = $\bar{I}_s = \bar{I}_m + \bar{I}_r$

Is it possible to independently control T & Φ (similar to that of S.E. m/c)?



Sync motor ⇒ High power motor,

⇒ Speed depends of F_s

⇒ Not a self starting m/c

⇒ Stability problem

Is it possible to make $F_s \propto$ rotor speed ?

$\Rightarrow$ no stability problem?

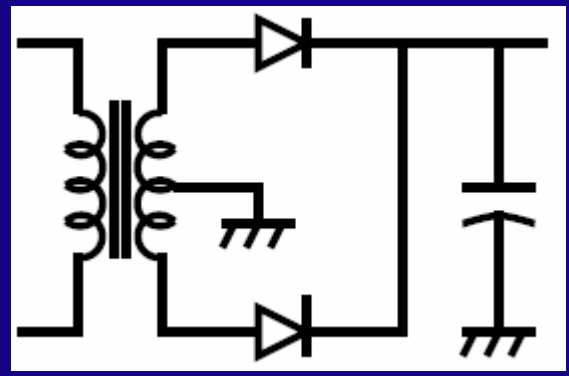
Can the speed of the machine be $\downarrow$ faster & the power be fed back to the source?

$$\frac{d\omega}{dt} = \frac{T_e - T_L}{J}$$ During motoring,

$$\frac{d\omega}{dt} = \frac{-(T_e + T_L)}{J}$$ During regeneration

$\Rightarrow$ Power conservation & faster deceleration

Power supply :



50Hz step down transformer

⇒ can the size and weight of transformer be reduced?

Speed of PC ↑

IC's ⇒ TTL, CMOS

As clock F ↑, biasing voltage ↓

⇒ 0.9V, 100A DC power supply will be required 2 years from now

⇒ Can this be designed?

Applications in Power Systems :

⇒ If lagging VAR, demand ↑ $|V_R|$ ↓.

⇒ Desired that $|V_R|$ should remain constant.

⇒ Provide reactive power support.

⇒ If 'C' is connected at the receiving end

$$\Rightarrow Q = \frac{V_R^2}{X_C} \downarrow \text{ as } V_R \downarrow .$$

⇒ "Unreliable" friend.

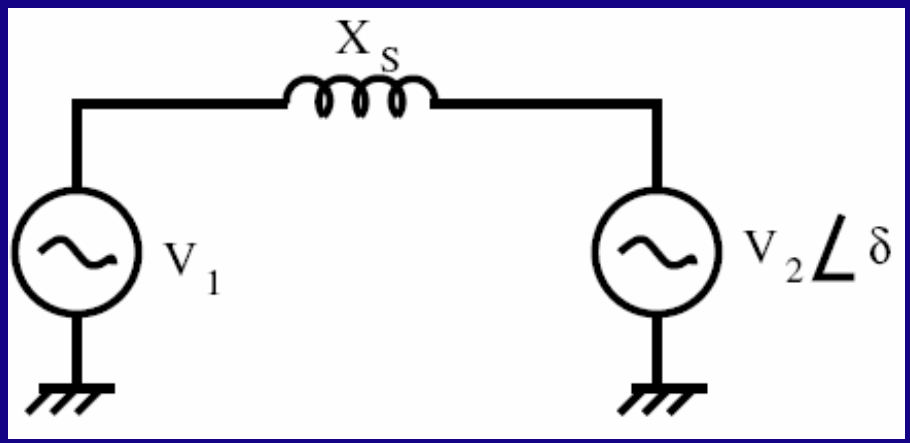
⇒ Smooth control of Q is not possible.

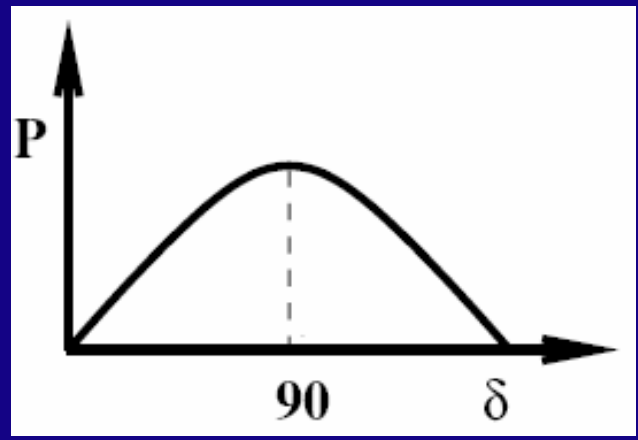
⇒ Can a circuit be designed which supplies $\pm Q$ VARS & independent of $|V_R|$?

Case 1:

$$P = \frac{V_1 V_2}{X_S} \sin\delta = \frac{\sin\delta}{X_S}$$, assuming $V_1 = V_2 = 1$ p.u.

Is it possible to ↑ P through line securely?

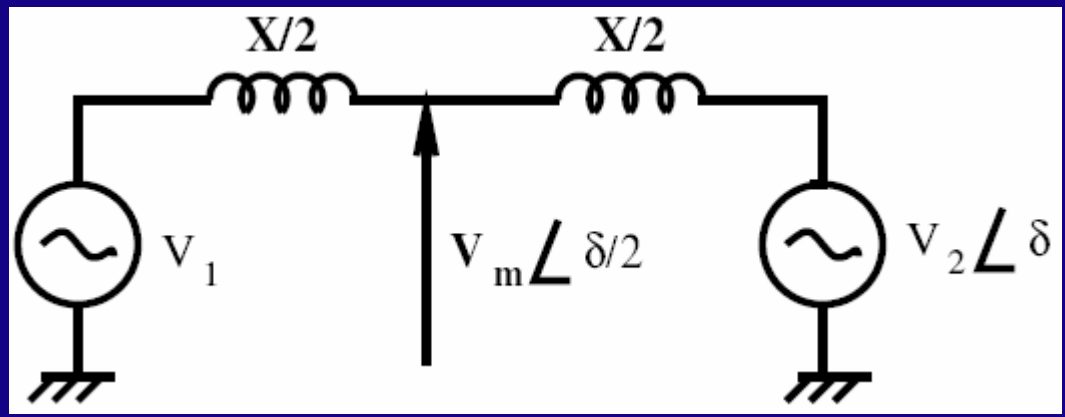


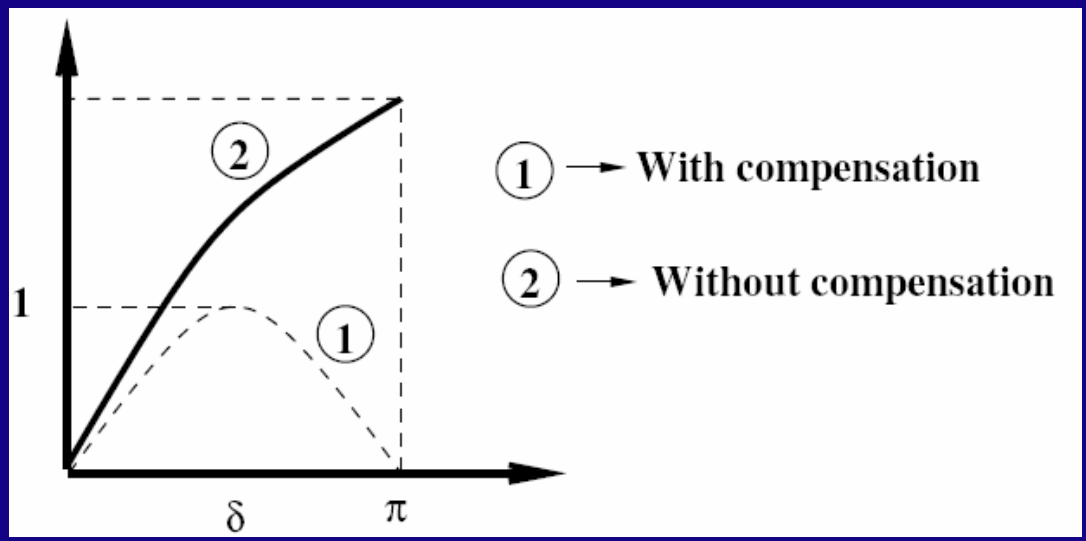


Now provide Q support as at the mid-point such that

$|V_m| = 1$ p.u.

$$P = \frac{V_1 V_m \sin\left(\frac{\delta}{2}\right)}{\left(\frac{X}{2}\right)}$$

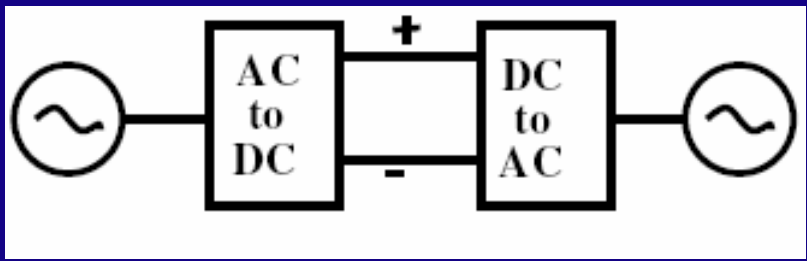




In long distnace AC power transmission

1) Voltage drop

2) Stability problem



Can the bulk power be transformed by converting it to DC?

Lighting :

(lumen/watt) for incandescent lamp < (lumen/watt) for flourescent lamp

$\Rightarrow$ needs a ballast (lamp has -ve resistance characteristic once the arc has been struck)

$\Rightarrow$ operate at 50 Hz $\Rightarrow$ size & noise

$\Rightarrow$ lossy

$\Rightarrow$ overall p.f. is poor

$\Rightarrow$ stroboscopic effect

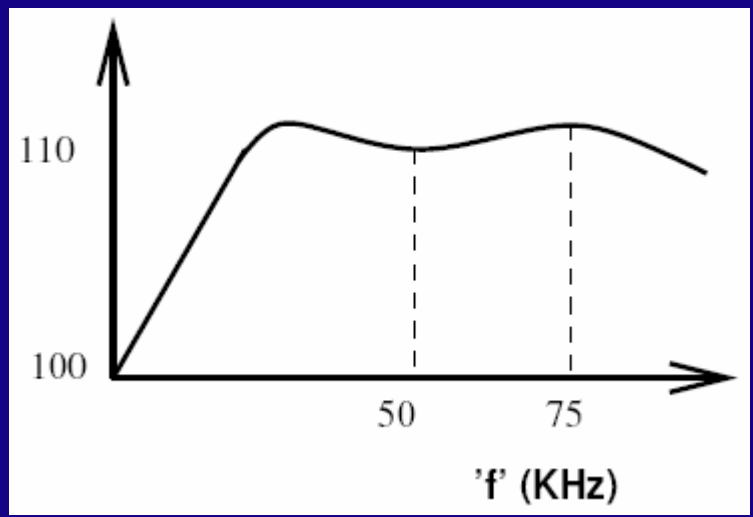
(lamp is turned off and ignited at 100 Hz)

⇒ Found that lumen output ↑ if operating F is ↑

⇒ If F is high, size of energy storage element ↓

⇒ If F>20 Khz ⇒ > audible range

⇒ Source side p.f. can also be improved.



Energy from alternate source:

Clean Technology.

Future energy source

High technology generator using renewable recourses like solar, wind power, biomass, hydro

Today's energy source

Advanced technology using oil, coal, nuclear

Historic energy source

Simple technology using wind power, wood, hydro

→ Solar ⇒ o/p is DC

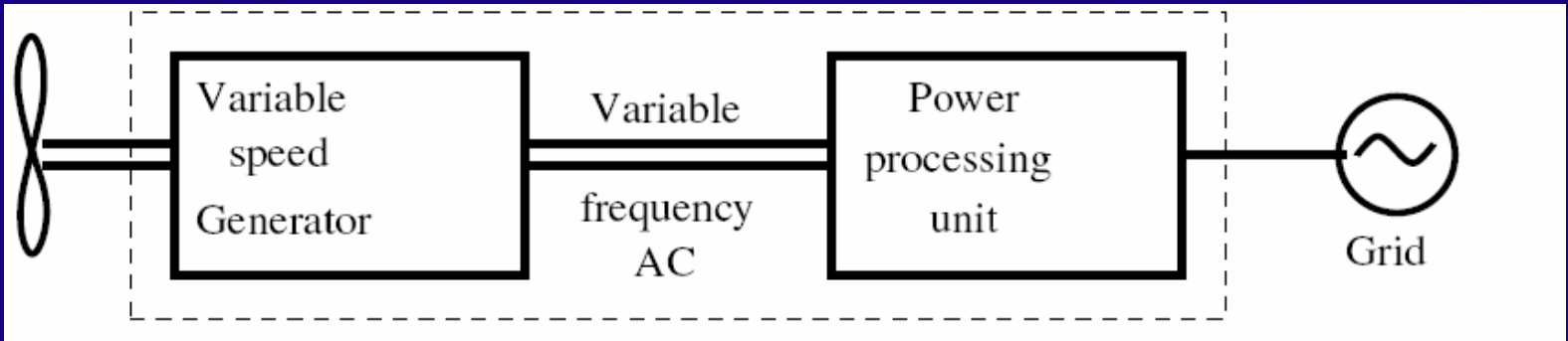
⇒ Expensive, but decreasing

→ Wind ⇒ cheapest, environmental clean

Wind energy now provides more than 31,000 MW of power around the world. In India Installed capacity 1900 MW

(target = 6000 MW by 2012)

It is estimated that the wind could supply 12% of the world's electrical demand by 2020



⇒ O/p is AC

⇒ Variable speed wind turbines with permanent magnet m/c are gaining popularity

⇒ O/P frequency of variable speed wind turbine is a function of speed.

⇒ If the power is to be fed to the grid, frequency should be constant

⇒ Frequency converter is required.

Urban pollution $\Rightarrow$ Can be $\downarrow$ by wide spread use of electric vehicle

$\Rightarrow$ Use electric vehicles / hybrid EV

$\rightarrow$ I.C. engine + energy storage

Gasoline based vehicles are efficient at particular speeds.

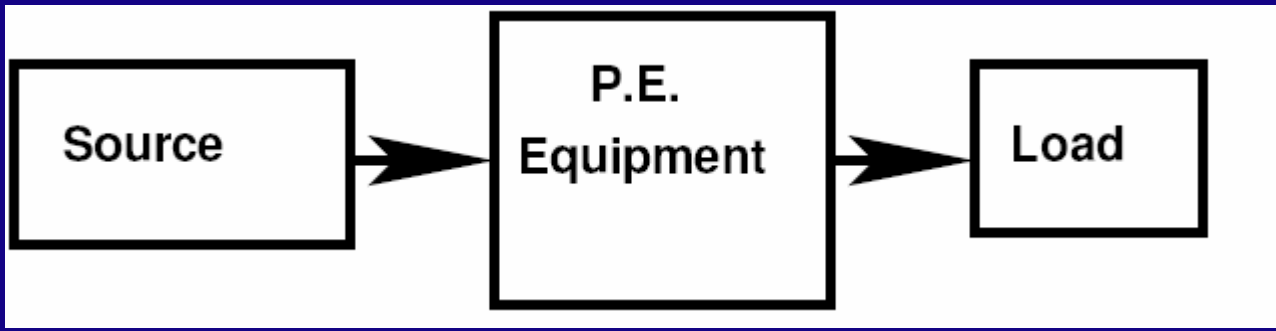
$\Rightarrow$ At other speeds, motor driving the wheels

Power Electronics :

Definition & Goal :

Power Electronics is the technology associated with efficient conversion and control of electric power by power semiconductor devices.

Goal of P.E. : To control the flow of energy from electric source to electric load.



⇒ η and reliability should be high

⇒ size, weight and cost should be low

⇒ η is a good measure of the success of any technology

As $\eta \uparrow$,

⇒ Power loss & $\therefore$ cooling requirement $\downarrow$

⇒ Packaging density can be increased

⇒ Size $\downarrow$.

How can the circuit change the voltage level, yet dissipate low power?

Circuit elements = R,L,C $\Rightarrow$ passive

Transistors, MOSFETS $\Rightarrow$ active

L & C $\rightarrow$ do not consume power

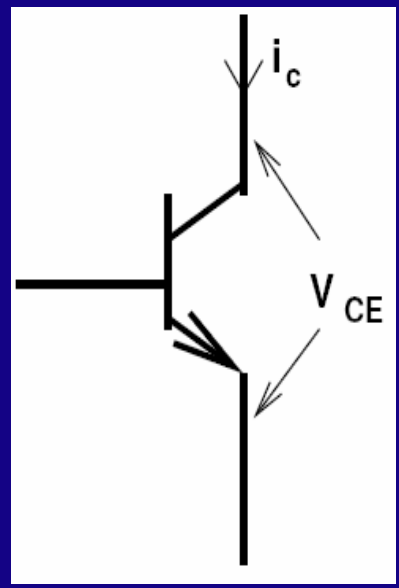
Power loss in the BJT = V_{CE} * I_C

In the active region, V_{CE} is high

In saturation, $V_{CE} = (V_{CE})_{SAT}$

$\Rightarrow$ very low

Power loss $\rightarrow$ 0



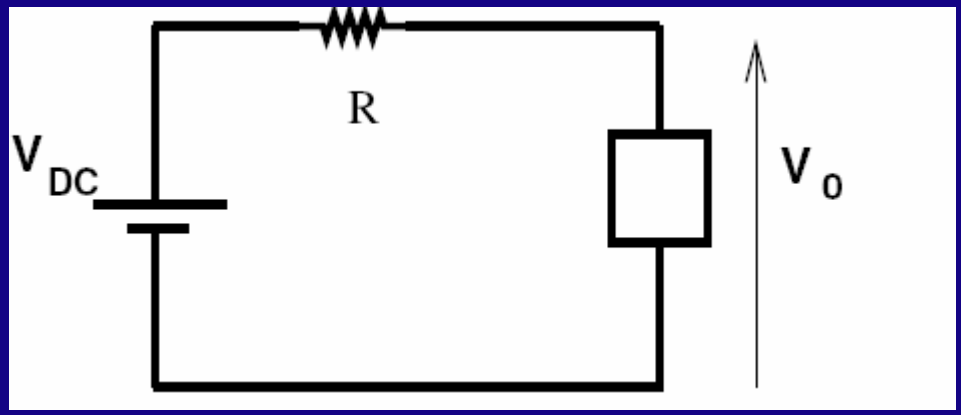
⇒ Resistor and active elements operated in the active region result in power dissipation

For high η ⇒ active elements should be operated either in saturation region or cut-off.

In addition, use only L & C elements

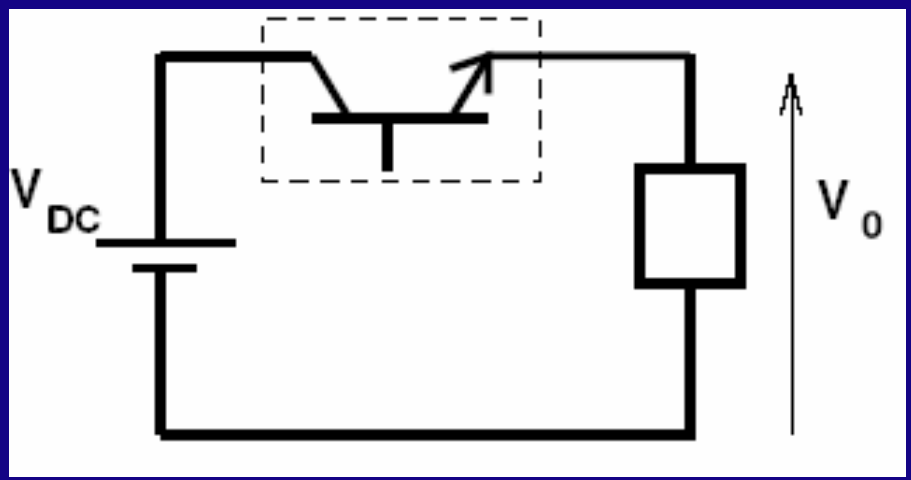
e.g.: Input is 30V DC, O/P is 5V DC

⇒ **Use potential divider**



⇒ **operate transistor in active region**

(V_{CE} ≥ 25V)

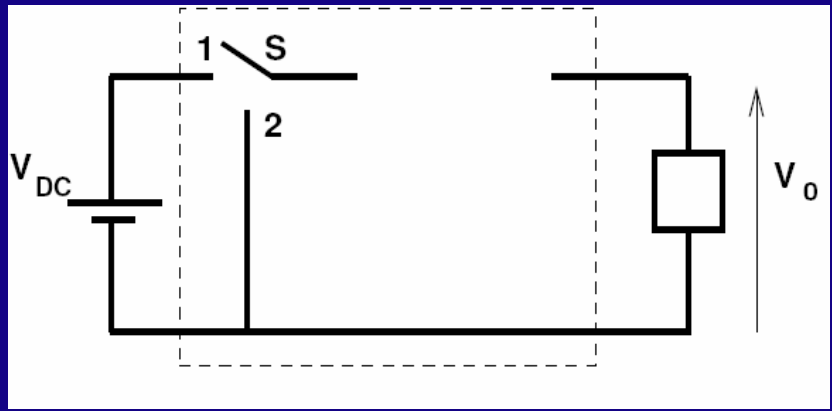


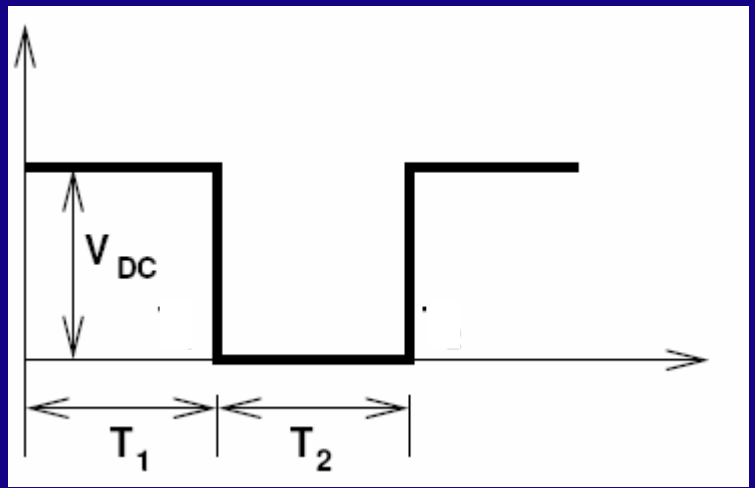
⇒ close to 1 for some time & then transfer it to 2

$$V_0 = V_{dc} \frac{T_1}{T_1 + T_2}$$

⇒ Power loss ⇒ 0

∵ Voltage drop across the device during ON period ≠ 0





Power electronics is extensively used in

⇒ In motor drives

⇒ Power supplies (both AC & DC)

⇒ Lighting

⇒ High frequency induction heating

⇒ Electric welding

⇒ Active filters

⇒ Bulk power transmission

⇒ Electric vehicles

⇒ To process power from non-conventional sources

Progress in PE is primarily due to advances in power semiconductor devices.

Fast processors, dedicated chips, circuit configurations, control and estimation techniques.

Significant events in the past history of PE

1783 : Concept of semiconductor (VOLTA)

1830 : Rectification effect of copper oxide (OHM)

1876 : Selenium rectifier (SIEMENS)

1896 : Single phase rectifier bridge circuit (POLLAK)

1897 : 3 phase bridge circuit

1901 : Invention of glass bulb mercury arc rectifier

1948 : Invention of the transistor

1953 : Germanium power diode

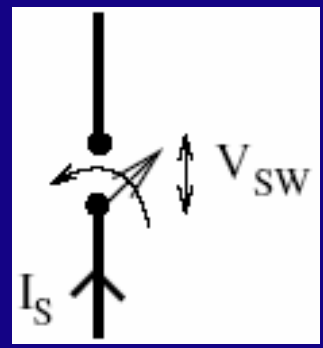
1954 : Silicon power diode

1957 : Thyristor (SCR) ; blocking voltage capability 500V to 6.5KV

Power Semiconductor Devices:

⇒ Is the heart and soul of modern P.E. equipment

⇒ Used as switches.



Properties of ideal switches :

⇒ When switch is OFF (open), $I_S = 0$.

Should be able to withstand any V across it.

$$-\infty \leq V_{SW(OFF)} \leq +\infty$$

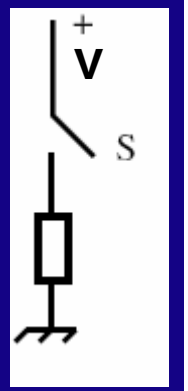
⇒ When ON, 'V' across it = 0 ($V_{SW(ON)} = 0$) & it is capable of passing any I through it.

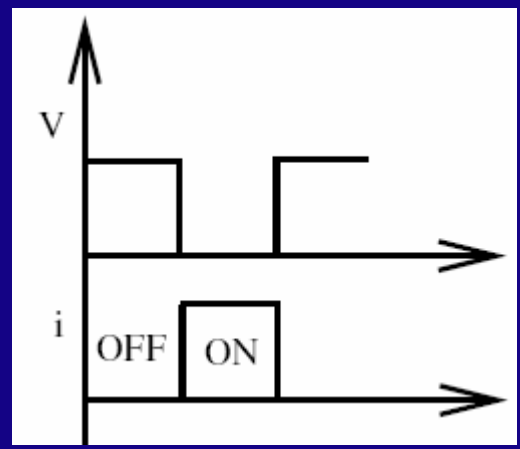
⇒ 'P' dissipated in the switch when ON or OFF = 0 (conduction & blocking loss)

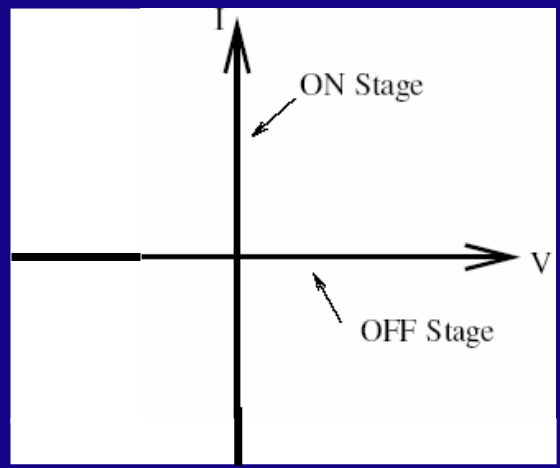
⇒ Switch can be turned ON & OFF instantaneously.

$t_{ON} = t_{OFF} = 0$

⇒ turn-on and turn-off losses (switching loss=0)







Characteristics of practical devices are very close to the ideal switches.

⇒ OFF state, I ≠ 0 & V ≠ ∞ in the OFF state.

⇒ $V_{SW(ON)}$ ≠ 0, ON state current carrying capacity is limited.

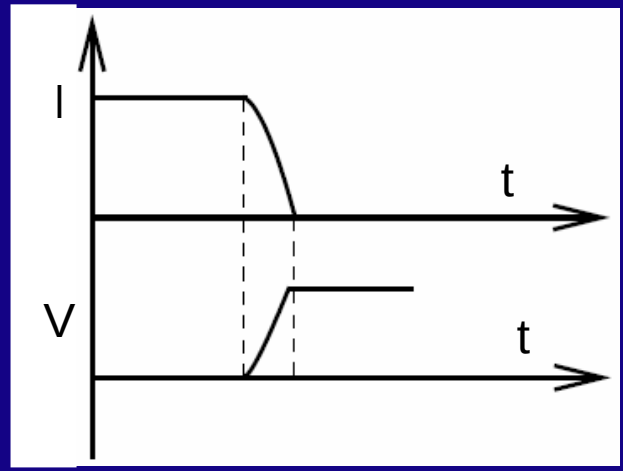
⇒ 'P' loss in OFF state (blocking loss) & ON state (conduction loss) ≠ 0.

⇒ t_{ON} ≠ 0 ; t_{OFF} ≠ 0

⇒ Takes finite time to switch from one state to another

⇒ switching loss

⇒ operating point should lie within safe operating area (SOA)

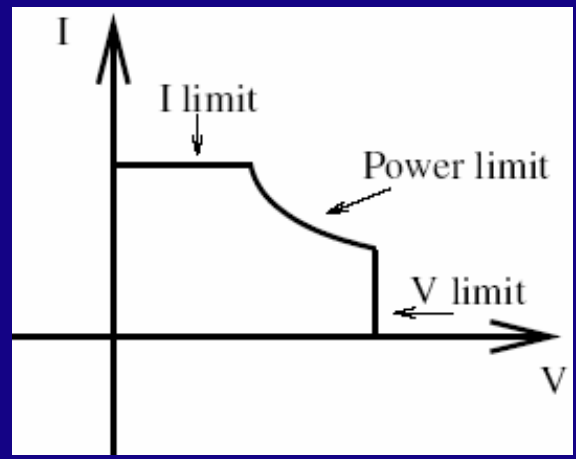


Device characteristics are thermaly unstable

P dissipated ≠ 0

⇒ Heat and ∴ temperature rise

⇒ Cooling requirement



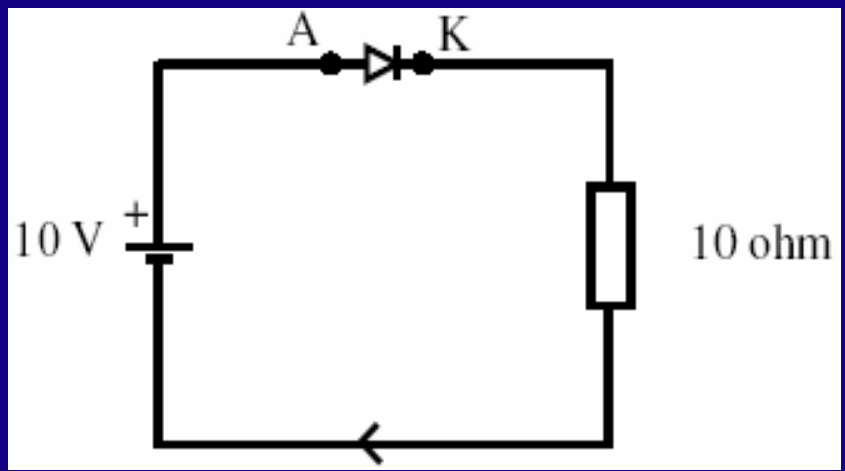
Power switching devices :

Uncontrolled switch ⇒ only two terminal device.

⇒ ON/OFF determined by state of the circuit in which the device is connected.

'D' is ON

$$i = \frac{10 - 0.7}{10} A$$

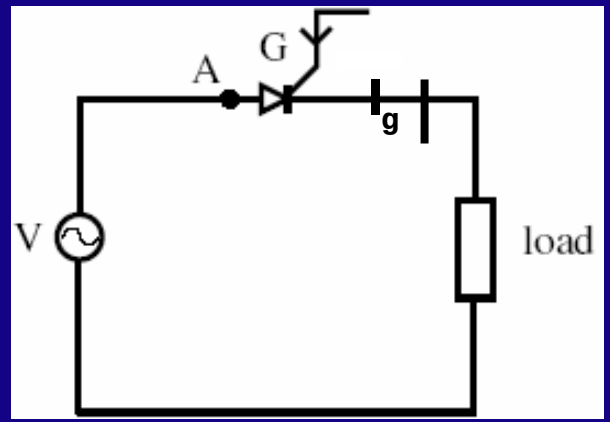


Semicontrolled switch :

⇒ **3 terminal device**

Switch may be turned to ONE of its state (either ON/OFF)

⇒ **Other state is reachable only through the circuit.**



⇒ **It is possible to turn-on silicon controlled rectifier (SCR) by +ve I_g**

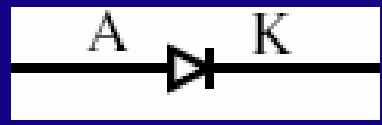
⇒ **Cannot be turned OFF through GATE.**

Controlled Switch :

Both the states On/OFF are reachable through appropriate control signals applied to the control terminal

BJT = Bipolar Junction Transistor

Diode = 2 Terminal Device



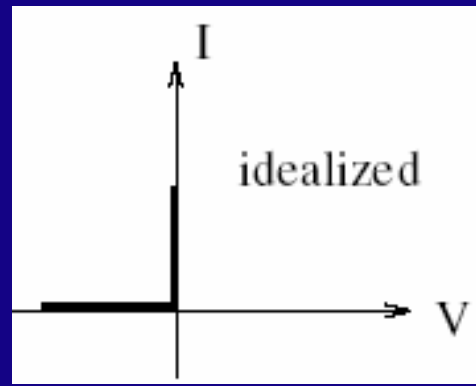
V_{AK} → should be +ve

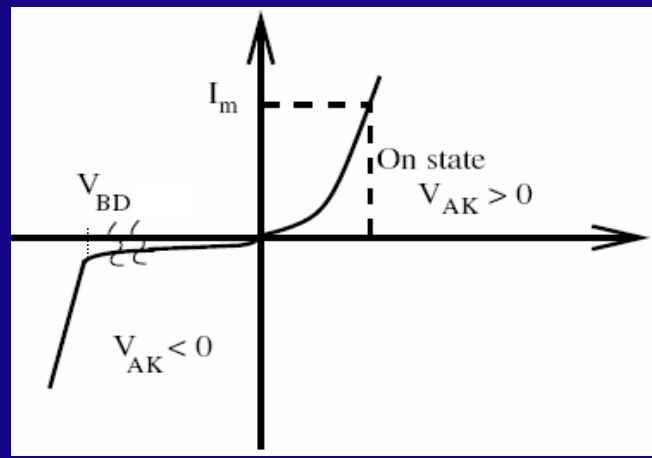
→ 0.7V

→ 1.5V for high power diodes

Current in ON mode is limited by load.

'V' across diode when it is reverse biased < V_{BD}





⇒ ON state (conduction loss) = V_F * I_A

V_F → V across the diode when it is ON

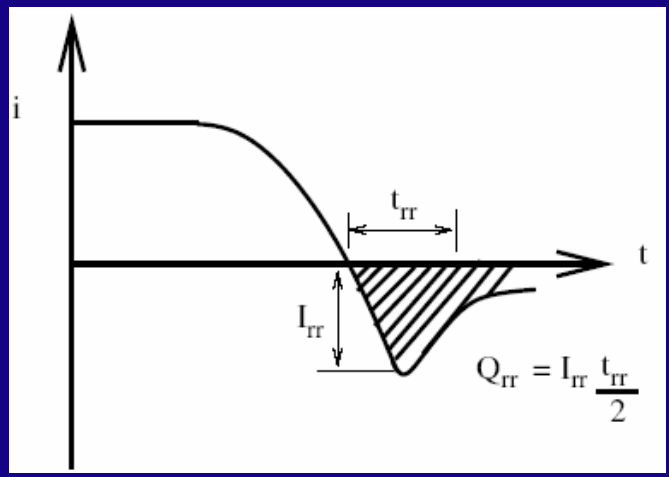
⇒ Heat sink is required as the loss ↑

⇒ Reaches ON state with some delay when forward biased.

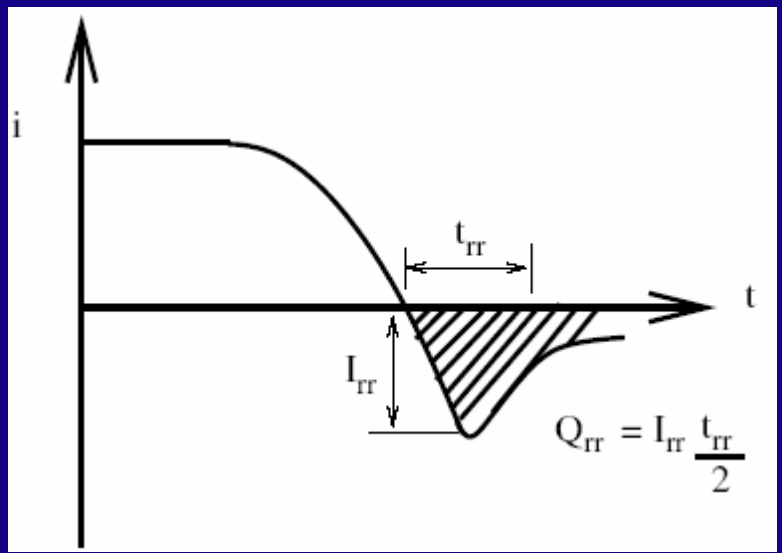
⇒ Goes to OFF state after t_{rr} when forward current goes to zero.

The minority carriers require certain time to recombine with opposite charge and to get neutralized.

⇒ This is reverse recovery time (t_{rr})

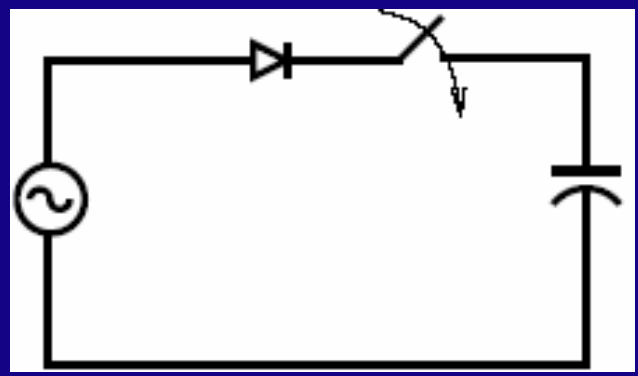


- ⇒ t_{rr} → time from Ist initial zero crossing of diode current to 25% of maximum reverse recovery current (I_{rr})
- ⇒ During t_{rr}, -ve I flows through the device.
- ⇒ Decides the maximum frequency of operation.



Important specification : –

1) Average forward current
   (to assess suitability with a power circuit)
2) Reverse blocking voltage (---------do-----)
3) ON state voltage $\Rightarrow$ to determine conduction loss
4) t_{rr} $\Rightarrow$ to assess high frequency switching capability
5) I^2t rating $\Rightarrow$
   short time surge energy that the diode can withstand.



Type of diode :

1) Rectifier diode or slow diode:

suitable for line frequency applications.

Recovery time is not specified.

6 KV, 4500A diodes are available.

2) Fast recovery diode: In high frequency switching application, 6 KV, 1.1KA diodes are available.

t_{rr} could be 0.1 μsec.

3) Schottky diode : They have low ON state voltage drop

V rating 100V, I = 300A

4) Silicon Carbide Diode :

⇒ Ultra low power loss

⇒ Ultra fast switching behaviour

⇒ Highly reliable (no temperature influence on the switching behaviour)

Thyristor or Silicon Controlled Rectifier (SCR)

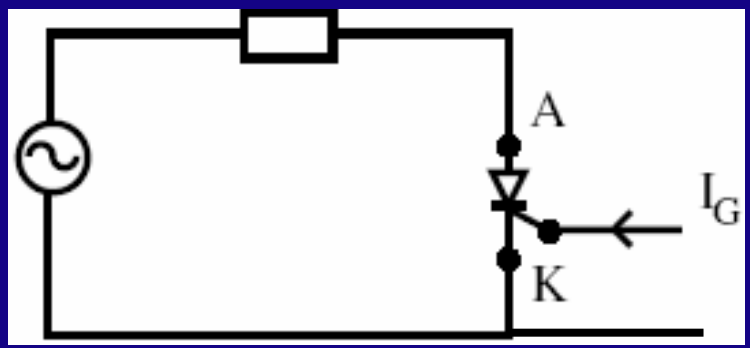
⇒ Three element device

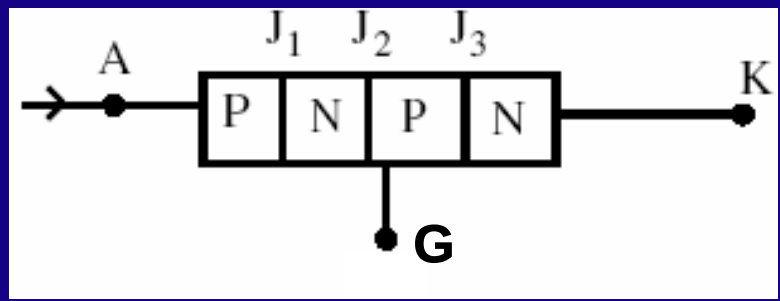
⇒ Anode (A), Cathode (K) & Gate (G)

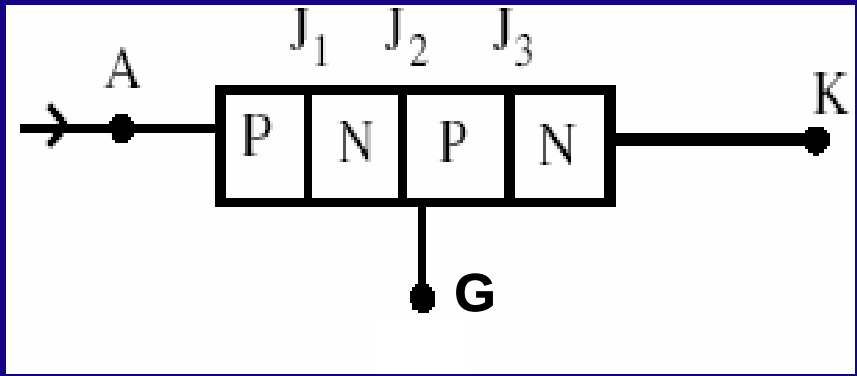
⇒ A & K ⇒ power circuit terminals

control signal is applied to the Gate w.r.t K.

⇒ 4 layers







$N_2 \rightarrow$ Layer is very thin & highly doped

$P_2 \rightarrow$ Layer is thicker & less highly doped

$N_1 \rightarrow$ (Blocking layer) is thickest & less doped

$P_1 \rightarrow$ is similar to P_2

Junction J_3 has low breakdown V in either direction

$J_3 \rightarrow$ cannot support high reverse voltage

When $V_{AK} > 0$ & device current = 0

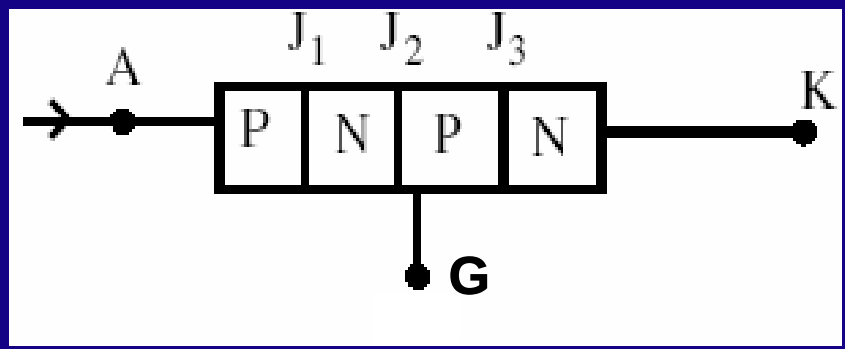
$\Rightarrow$ forward blocking mode

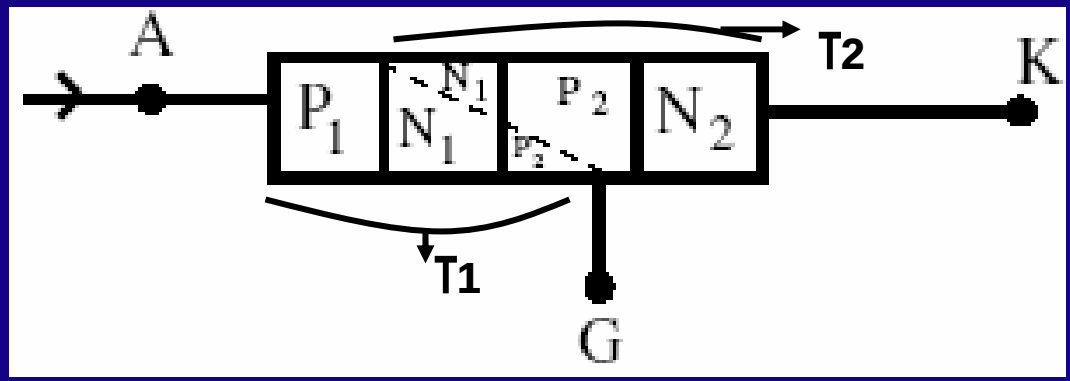
J_1 & J_3 are Forward Biased (F.B)

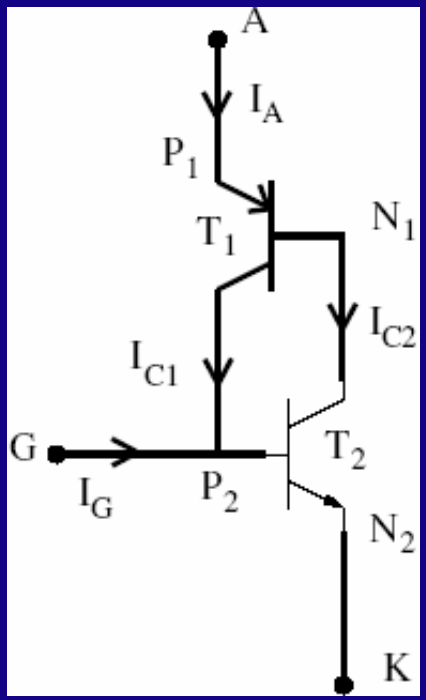
J_2 is reverse biased (R.B)

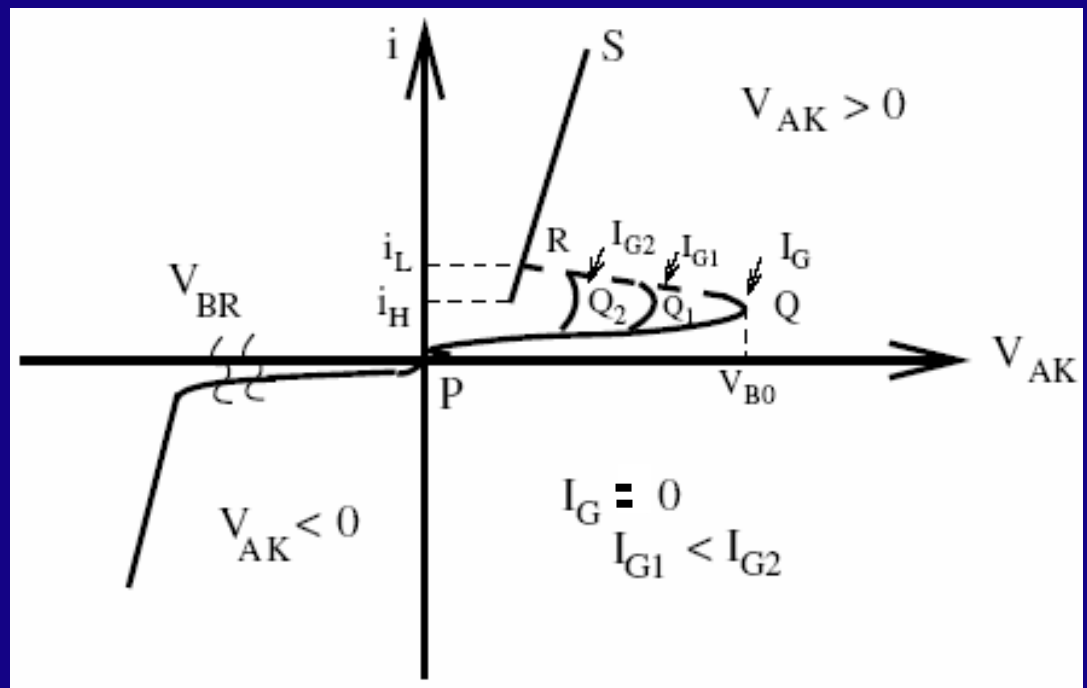
When $V_{AK} < 0$, J_2 is F.B. & J_1, J_3 are R.B.

$\Rightarrow$ J_1 should block the entire V when R.B.




A
K
T2
T1
G
P1
N1
P2
N2


A
IA
P1
T1
N1
IC2
IC1
G
IG
P2
T2
N2
K


i
S
VAK > 0
iL
iH
R
IG2
IG1
IG
VBR
Q2
Q1
Q
VAK
P
VB0
VAK < 0
IG = 0
IG1 < IG2

PQ (or PQ_1 or PQ_2) $\rightarrow$ forward blocking mode.

i_A □ 0 (mA) Forward leakage I

QR (or Q_1R or Q_2R) $\rightarrow$ negative resistance region

$\rightarrow$ unstable

RS $\rightarrow$ forward conduction mode.

When F.B., SCR goes into conduction mode

when $V_{applied} > V_{B0}$ if $I_G = 0$.

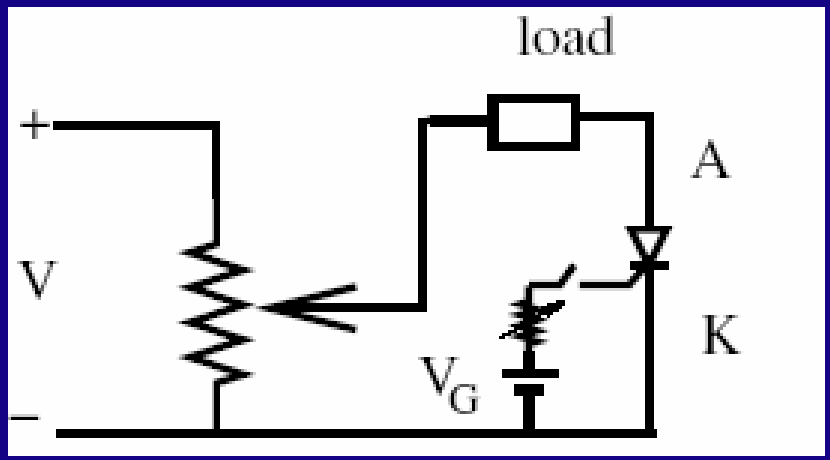
V_{B0} $\rightarrow$ forward breakover voltage

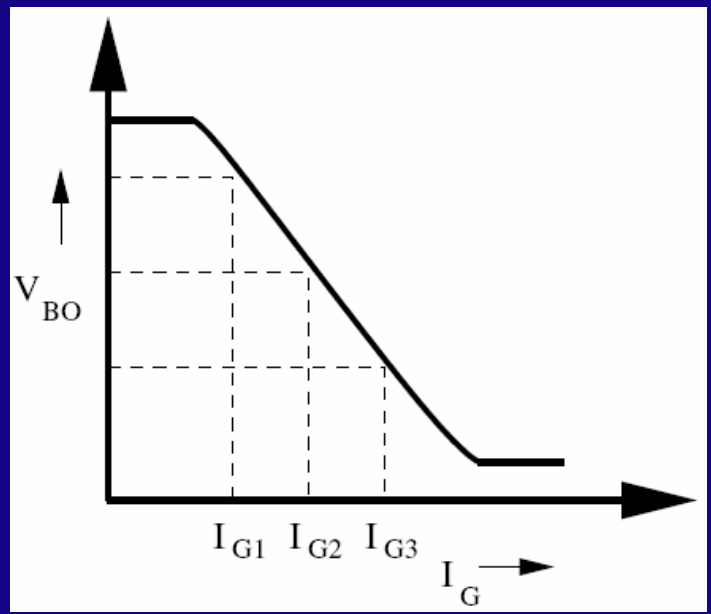
$\rightarrow$ forward blocking voltage

capacity is determined by J_2

i) If $I_G \neq 0$, 'V' at which device goes into conduction mode $\downarrow$.

(I_G reduces the deplection layer around J_2)





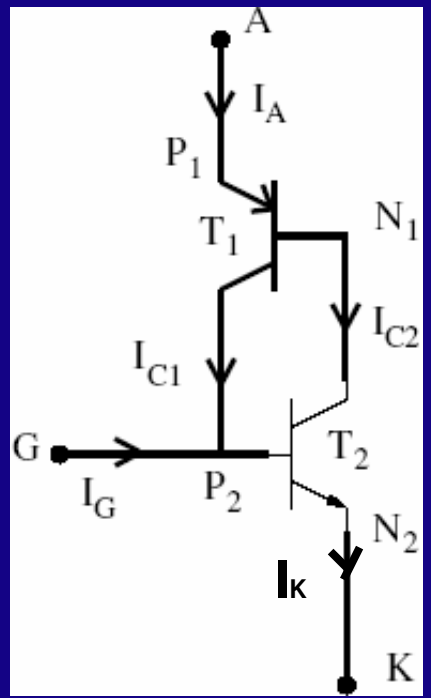
For any transistor

$I_C = \alpha I_E + I_{CBO}$

$\alpha \rightarrow$ common base current gain

$\square \quad \frac{I_C}{I_E}$,

$I_{CB0} \rightarrow$ leakage current of the C-B junction.



$\therefore$ for T_1, $I_E = I_A$ $\quad I_{C1} = \alpha_1 I_A + I_{CBO1}$

for T_2, $I_E = I_K$ $\quad \therefore I_{C2} = \alpha_2 I_K + I_{CBO2}$

Now, $I_E = I_C + I_B$

$I_{E1} = I_A$ and $I_{B1} = I_{C2}$

$\therefore\ I_{C1} + I_{C2} = I_A = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_K + I_{CBO2}$

$I_K = I_{B2} + I_{C2}$

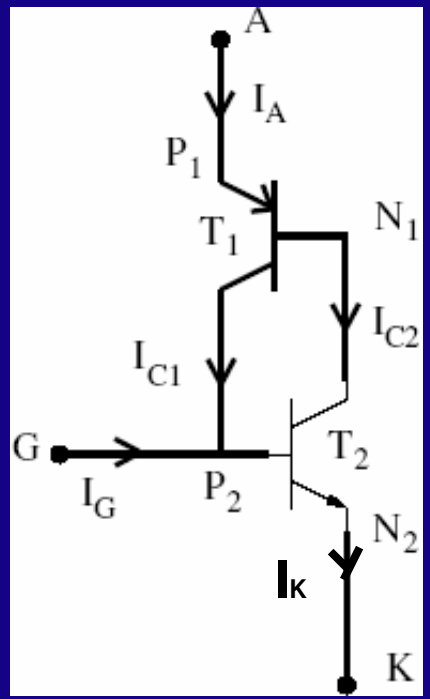
for finite I_G,

$I_K = I_{C1} + I_G + I_{C2}$

$= I_A + I_G$

$$\therefore\ I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

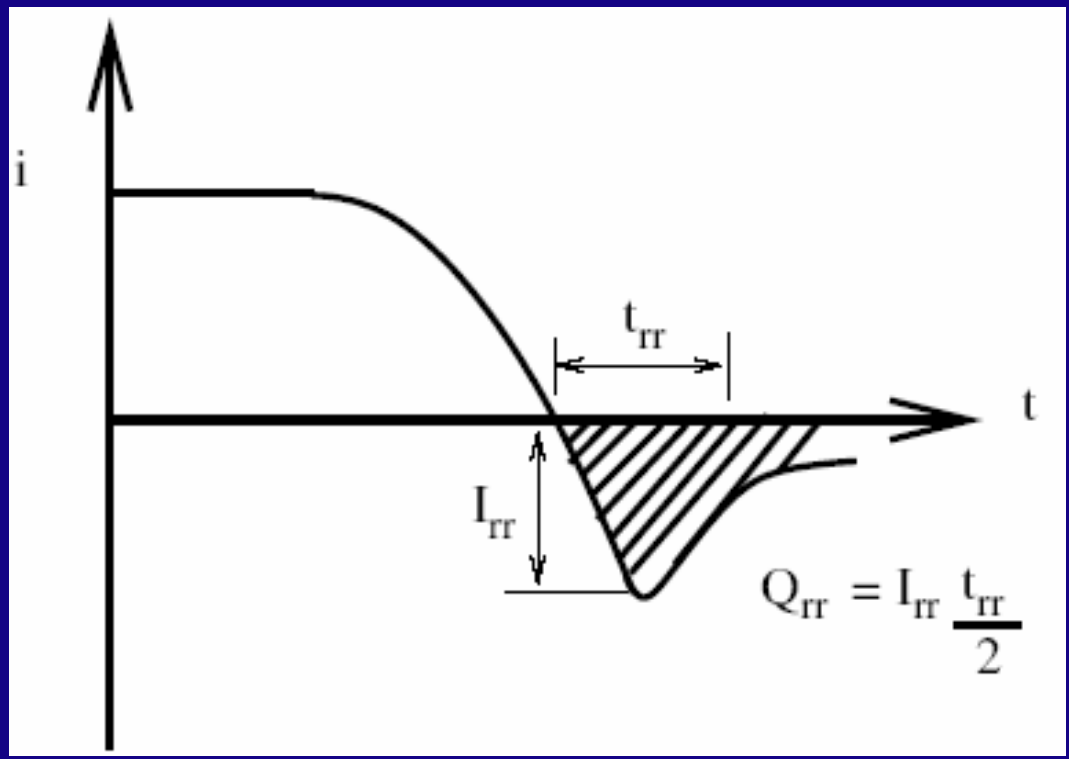
$\alpha \uparrow$ with I_E



Review :

1) t_{rr} $\rightarrow$ reverse recovery time

2) Reverse recovery charge, $Q_{rr} = \frac{1}{2} t_{rr} I_{rr}$



3) S.C.R $\Rightarrow$ minority carrier device

$J_3 \rightarrow$ cannot block high reverse voltage

When forward blocking mode $\rightarrow$ J_1, J_3 = F.B.

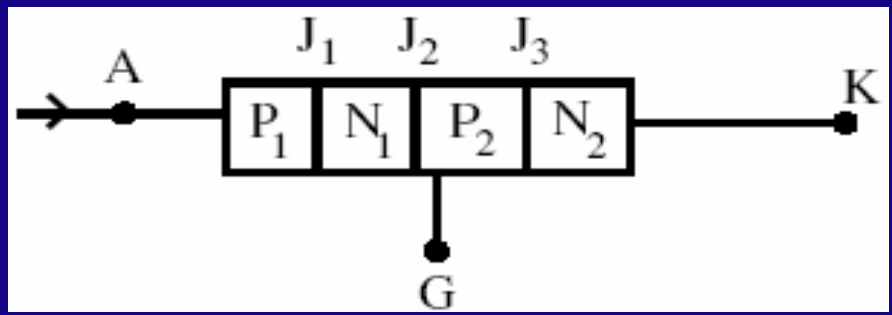
and J_2 = R.B.

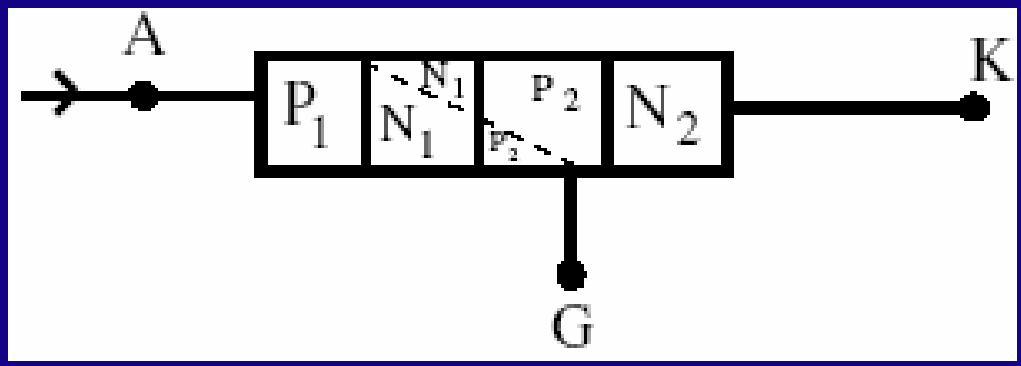
Entire 'V' appears across J_2.

$\Rightarrow$ Breakdown 'V' of J_2 can be $\downarrow$ by $+I_G$.

When R.B. : entire reverse 'V' is blocked by J_1

$\because$ J_2 is F.B. & J_3 cannot block high 'V'.

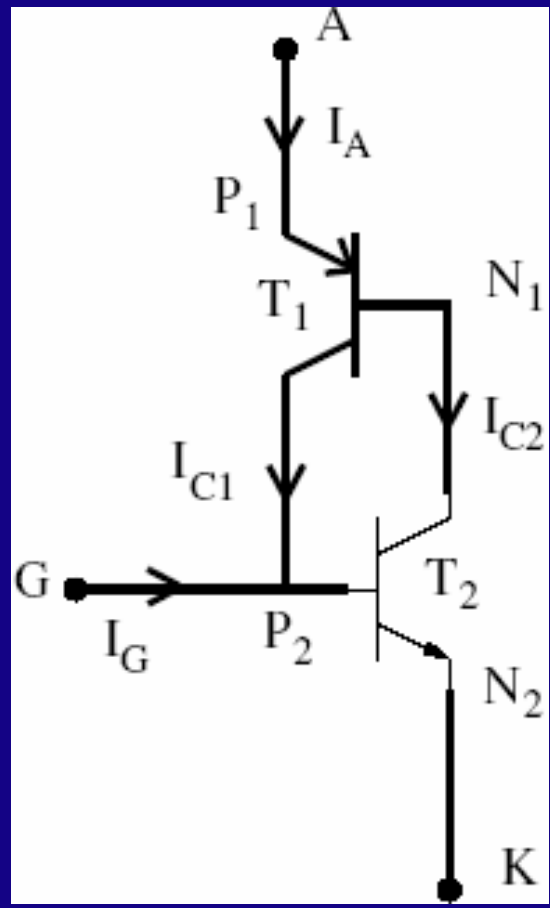


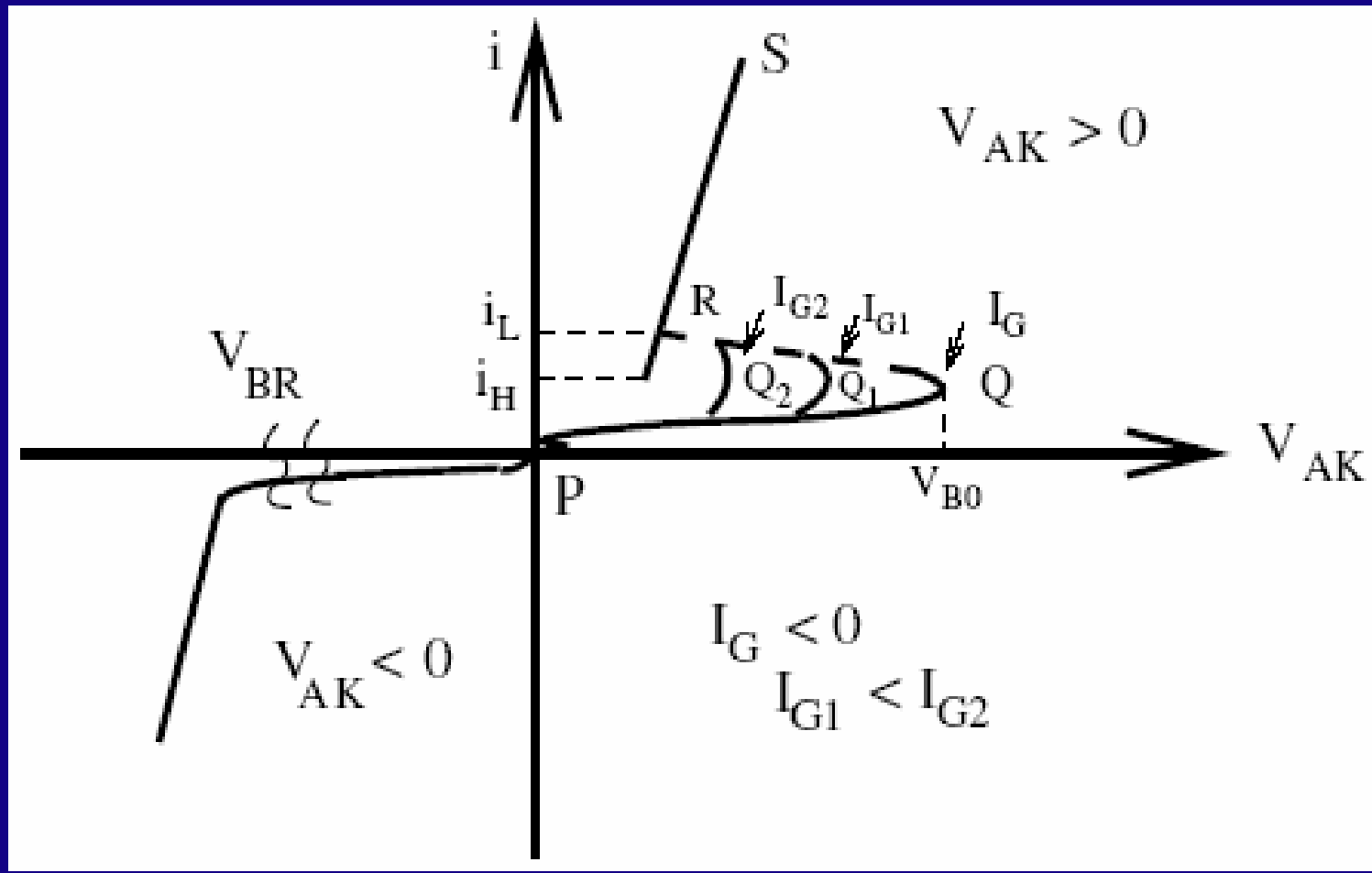


$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

I_{CBO} → reverse current flowing from collector to base with emitter open circuited.

↑ with temperature




i
S
$V_{AK} > 0$
R
I_{G2}
I_{G1}
I_G
i_L
i_H
V_{BR}
Q_2
Q_1
Q
V_{AK}
P
V_{B0}
$V_{AK} < 0$
$I_G < 0$
$I_{G1} < I_{G2}$

α increases with I_E

$\therefore$ α_1 also increases with I_A $\because$ $I_{E1} = I_A$

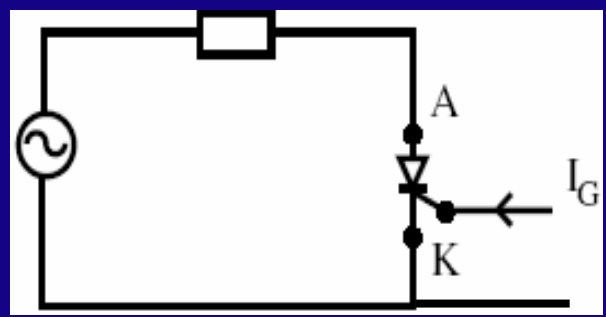
Similarly α_2 varies with I_K $\because$ $I_{E2} = I_K = I_A + I_G$

If I_G is suddenly $\uparrow$, I_A $\uparrow$ $\because$ $$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

As I_A $\uparrow$, α_1 $\uparrow$ and $\therefore$ α_2 $\uparrow$.

$\Rightarrow$ $\uparrow$ in α_1 and α_2 further increases I_A

$\Rightarrow$ +ve feedback.



If $(\alpha_1 + \alpha_2) \rightarrow 1$, I_A is large (determined by load)

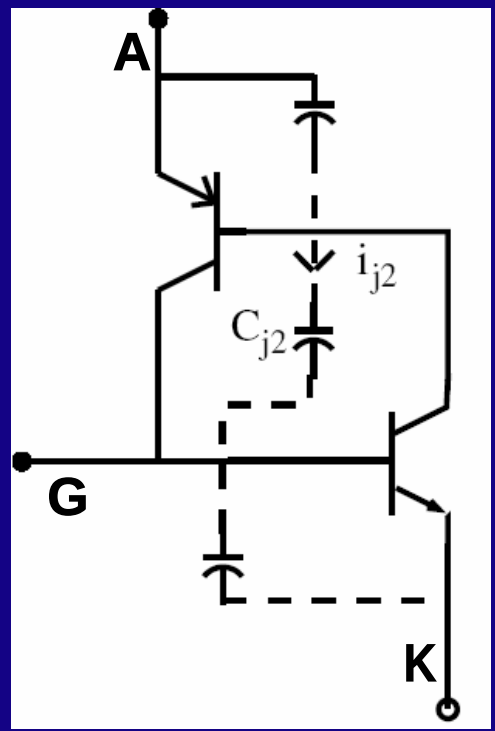
$\Rightarrow$ Requires a small I_G

If $\frac{dV}{dt}$ is large, i_{j2} would be large and this may increase I_{CBO1} and I_{CBO2}.

$\Rightarrow$ gets amplified by transistor action

$\Rightarrow$ $(\alpha_1 + \alpha_2)$ may $\rightarrow 1$

$\Rightarrow$ device may turn ON.



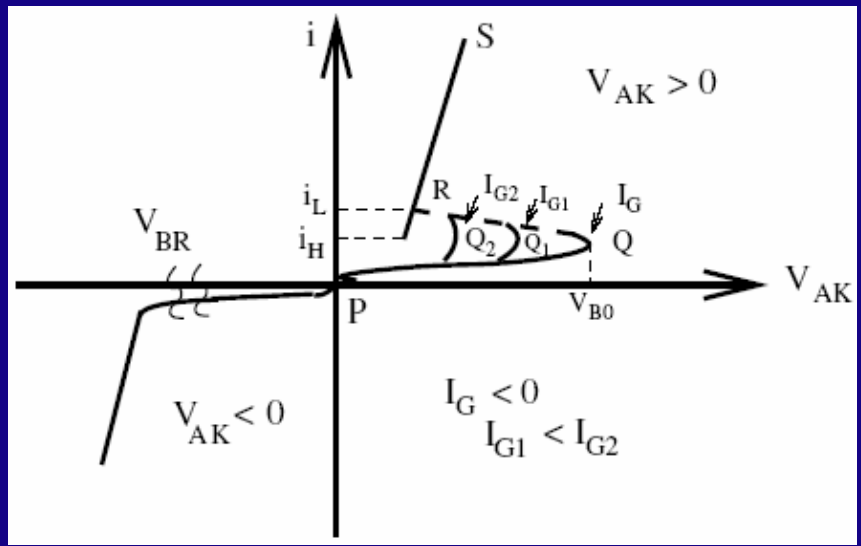
$\therefore$ **When F.B., device goes into conduction mode.**

1) if $V_{applied} > V_{B0}$

2) by +ve $I_G \Rightarrow I_G$ should be present till $i_A \geq i_{LATCHING}$

$\Rightarrow$ **Having gone into conduction mode, device cannot be turned OFF through Gate.**

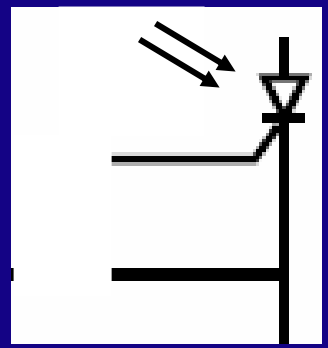
$I_A < i_{HOLDING}$



3) If $\frac{dV}{dt}$ is above a certain rate

4) Temperature effect $\Rightarrow$ At high temperature, leakage I of transistor $\uparrow$.

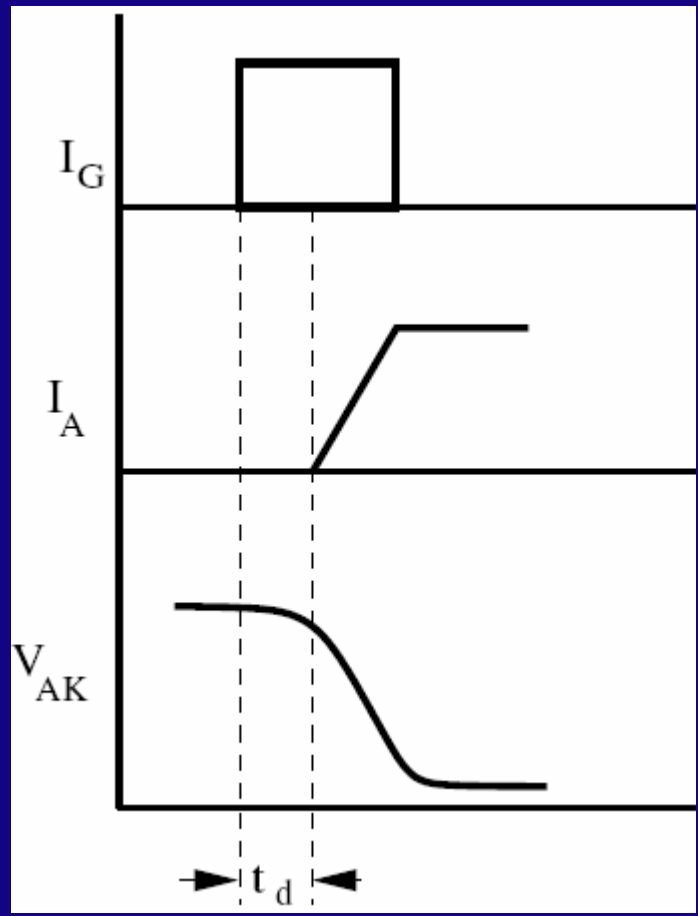
5) By direct light radiation.



Switching characteristics:

In forward blocking mode, when I_G starts flowing, there is a finite delay time (t_d) before device current builds up

After t_d, device current builds up attains a value determined by load



If $\frac{di}{dt}$ is very high $\Rightarrow$ device may fail.

Initially turn ON of the device occurs near the gate-cathode periphery & then it spreads across the entire junction with a finite velocity

If $\frac{di}{dt}$ is high

$\Rightarrow$ Current is confined to small area of the device

$\Rightarrow$ Overheating of the junction $\Rightarrow$ destruction of the device

⇒ Durning turn-ON, $\frac{di}{dt}$ has to be controlled

⇒ In conduction mode J_2 is highly saturated with minority carriers

⇒ Gate has no further control

⇒ 'V' across the device 1.5 V

SCR can be turned OFF by temperorily applying a -ve voltage across it

⇒ When reverse voltage is applied, I_A becomes zero & then reverses.

⇒ V_{AK} is still +ve untill J_1 & J_3 starts to become R.B.

⇒ When this reverse current reaches maximum junctions begin to block.

J_1 blocks just before J_3

($\because$ N_1 is less heavily doped than N_2)

⇒ Reverse I starts decaying

⇒ Fast decay of recovery current causes a voltage overshoot across the device due to leakage L effect.

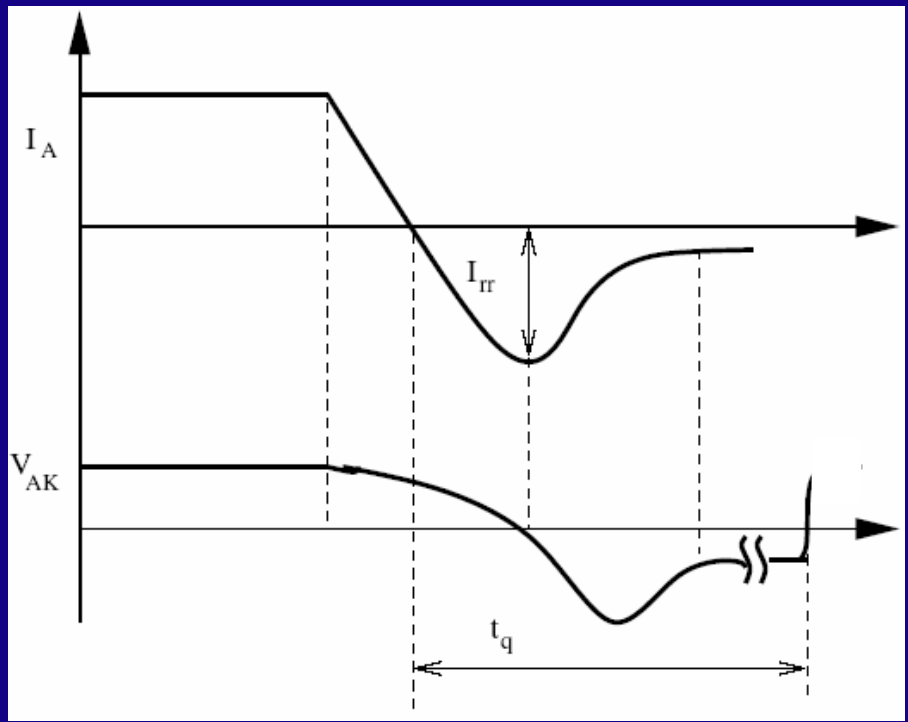
Reverse recovery current sabilizes to very low value

⇒ J_2 is still F.B.

⇒ There are still residual charge carriers trapped in P_2 & N_1 layer

⇒ Charge carriers must be given time for recombination

⇒ Takes considerable time

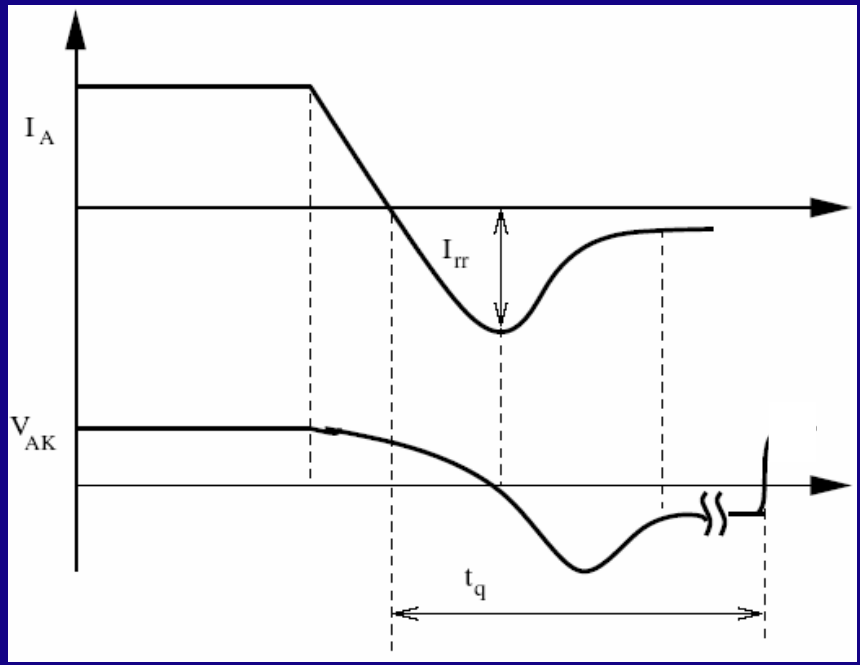


$\Rightarrow$ Reapplied $\frac{dv}{dt}$ should be within a safe limit

else it may turn ON

$t_q \rightarrow$ Minimum time interval between ON state

(I_A) current becomes zero & the instant when thyristor is capable of withstanding forward voltage without turning ON



Important parameters

⇒ Average forward current (to assess suitability with a power ckt)

⇒ Reverse blocking voltage

⇒ ON state voltage drop

⇒ OFF state current

⇒ $\frac{di}{dt}$ during turn-ON & during turn-OFF

⇒ Reapplied $\frac{dv}{dt}$

To design protection ckt (snubber ckt)

$\Rightarrow I^2R$ rating

$\Rightarrow$ Device turn-OFF time 't_q' $\rightarrow$ to assess high frequency switching capability

How to limit $\frac{di}{dt}$ & $\frac{dv}{dt}$?

High $\frac{dv}{dt} \rightarrow$ Device may turn ON with

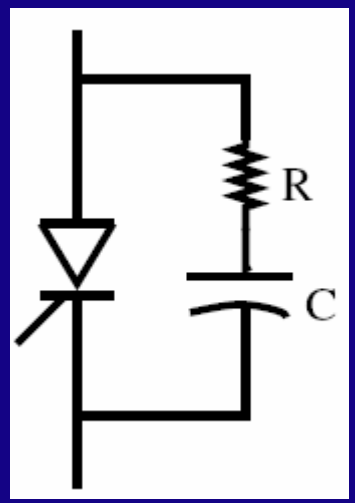
$$I_G = 0 \;\&\; V_{AK} < V_{BO}$$

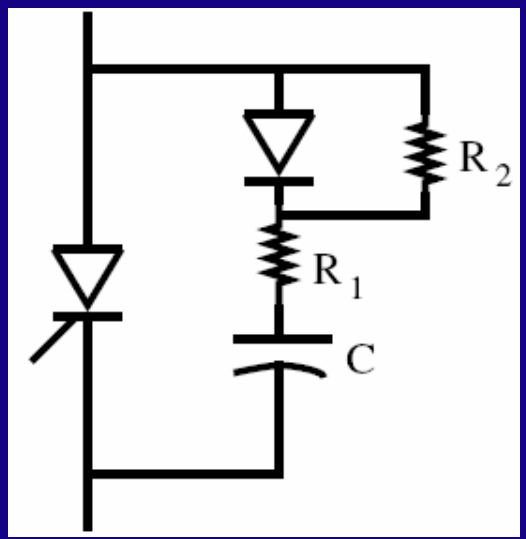
Also protection against voltage spike due to stray inductance $\left(L\frac{di}{dt}\right)$

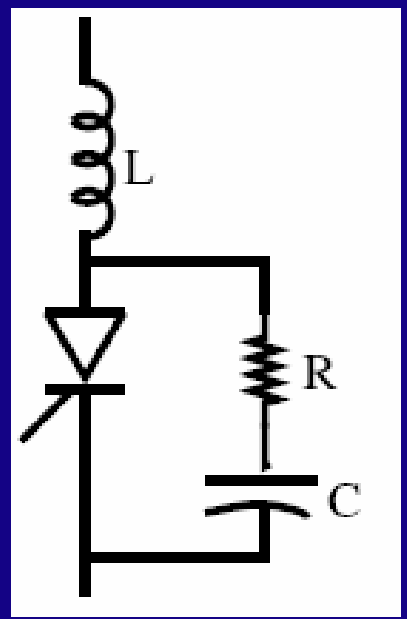
⇒ Connect RC ckt (snubber) across the thyristor

R → Rated such that discharge current is controlled during turn ON

⇒ $\frac{di}{dt}$ can be contolled by connecting a small L in series with the device





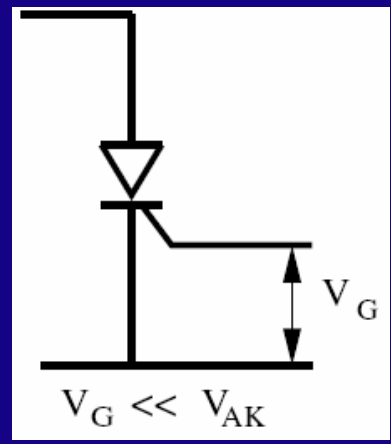


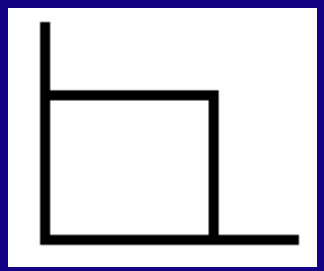
Gating requirement

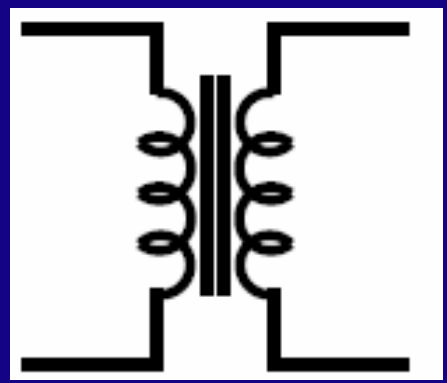
⇒ I_G should be present till $I_A > I_{Latching}$

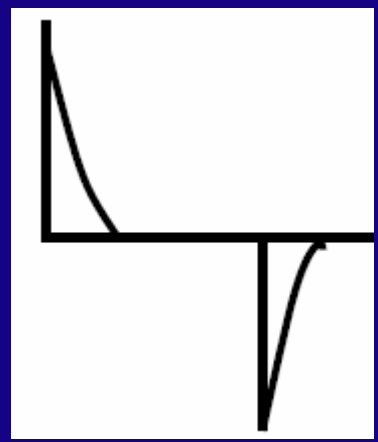
⇒ One of the requirements is control ckt should be isolated from power ckt

⇒ Use a pulse transformer

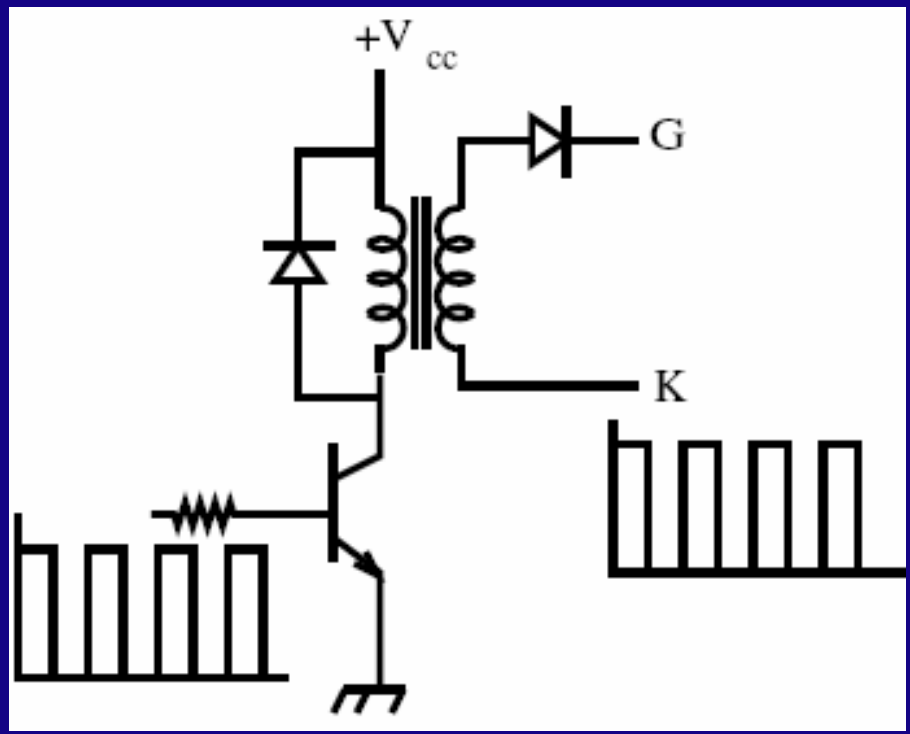








→ One pulse may not be sufficient to turn ON the SCR



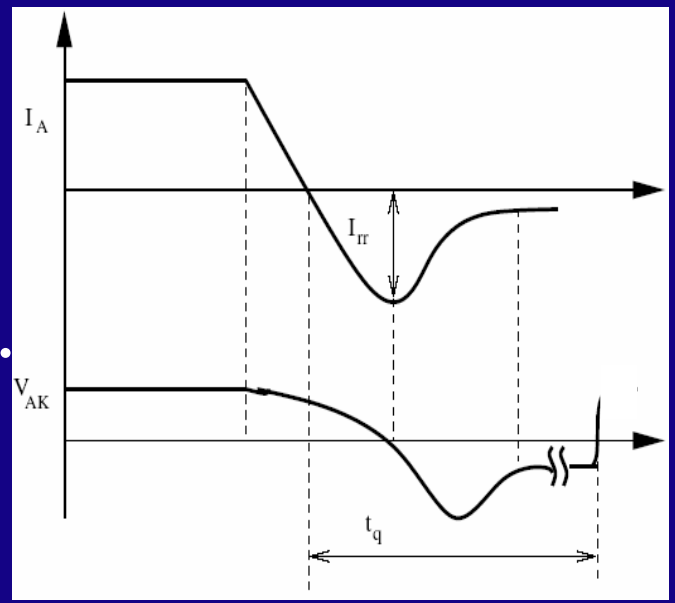
Review :

1) During turn – OFF

When J_1 & J_3 have recovered blocking capability

$\Rightarrow$ -ve 'V' is applied across thyristor.

In addition 'V' spike due to $\frac{di}{dt}$ in 'L' in series with thyristor



$\Rightarrow$ Use RC snubber

2) If $\frac{di}{dt} > \left.\frac{di}{dt}\right|_{rated}$ device will get damaged

3) High frequency pulses are used to trigger the thyristor

Types of SCR :-

1) Converter grade SCR $\Rightarrow$ slow

2) Inverter grade SCR $\Rightarrow$ fast

$\Rightarrow$ suitable for high frequency application

TT 46 F 08...13

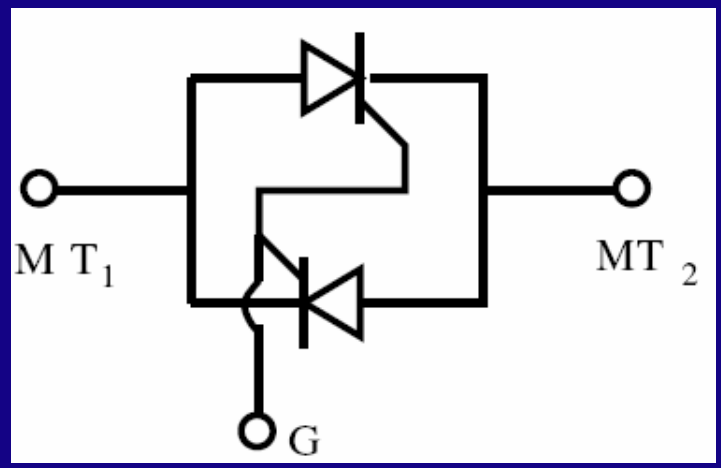
Electrical properties			
Maximum rated values			
repetitive peak forward off-state and reverse voltages	V_{DRM}, V_{RRM}	800, 1000, 1100 1200, 1300	V [1]
non-repetitive peak forward off-state voltage	V_{DSM}	800, 1000, 1100 1200, 1300	V
non-repetitive peak reverse voltage	V_{RSM}	900, 1100, 1200 1300, 1400	V
RMS on-state current	I_{TRMSM}	120	A
average on-state current	I_{TAVM}	45	A
		76	A
surge current	I_{TSM}	1300	A
		1150	A
I^2t-value	I^2t	8450	A^2s
		6600	A^2s

critical rate of rise of on-state current	$(di_T/dt)_{cr}$	120	A/µs
gate trigger current	I_{GT}	max. 150	mA
gate trigger voltage	V_{GT}	max. 1,4	V
holding current	I_H	max. 250	mA
latching current	I_L	max. 1000	mA

TRIAC: (1964-General Electric)

⇒ TRIAC has a complicated structure

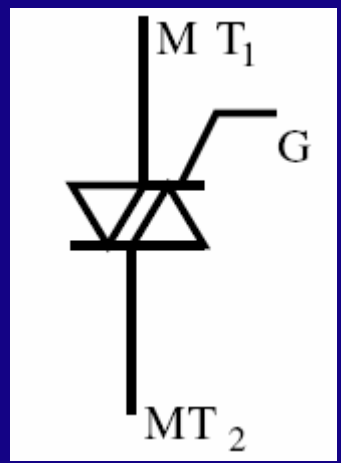
⇒ Functionally equivalent to two thyristors connected antiparallel



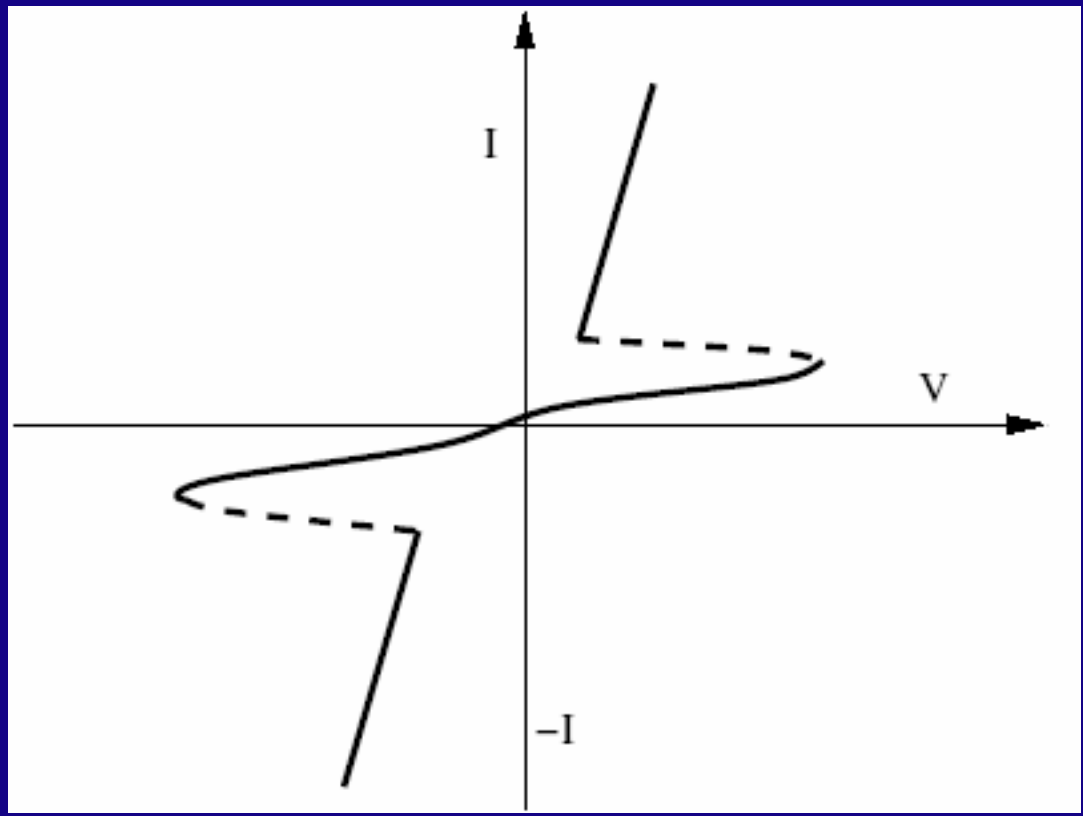
⇒ Bidirectional device

⇒ Can be triggered when MT_2 is +ve w.r.t. MT_1 & +ve I_G w.r.t. to MT_1

⇒ Can also be triggered when MT_2 is -ve w.r.t. MT_1 & -ve I_G w.r.t. to MT_1



⇒ Used in fan regulators, Light intensity controller, Temperature controller



V – I characteristics

Limitations :

In the case of thyristor,

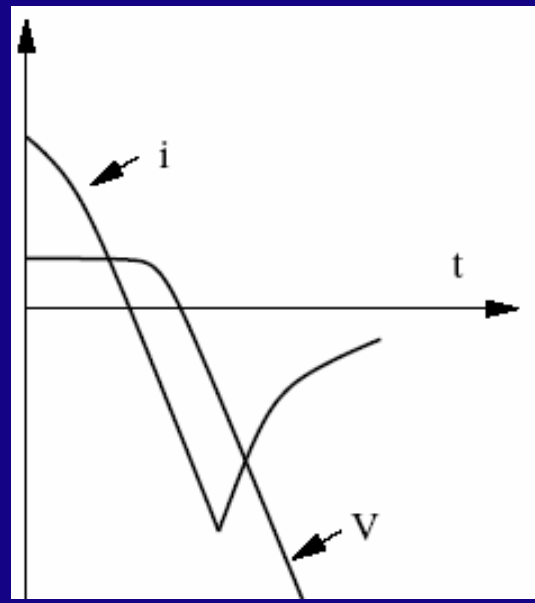
$\frac{dv}{dt}$ during OFF state is as shown.

$\Rightarrow$ Device may go to conduction mode due to $\frac{dv}{dt}$ during turn-OFF

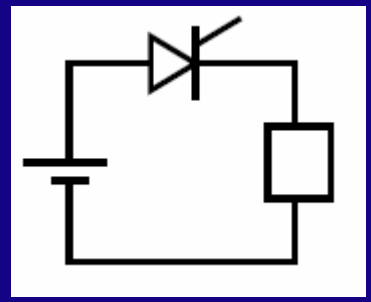
$\Rightarrow$ When i=0, 'V' across is very different from zero

$\Rightarrow$ Has less time than thyristor to recover its blocking power

$\Rightarrow$ dv/dt rating is lower



SCR is nearly an ideal switch



→ Requires a sharp pulse to turn-ON
(No continuous gate drive)

→ Block +ve as well as -ve 'V'

→ High V & high I devices are available

→ Rugged

⇒ Inability to turn -OFF by application of a control signal at the thyristor gate.

⇒ Inclusion of turn-OFF capability in thyristor requires device modification with some compromise in operational capability

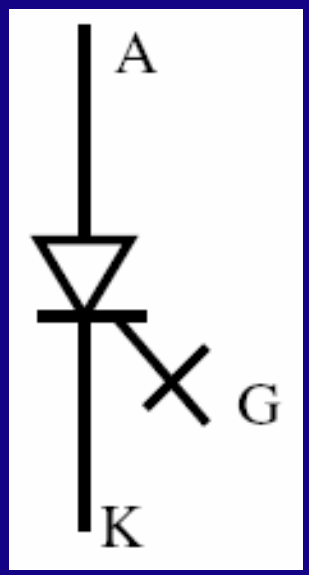
Gate Turn-OFF Thyristor (GTO)

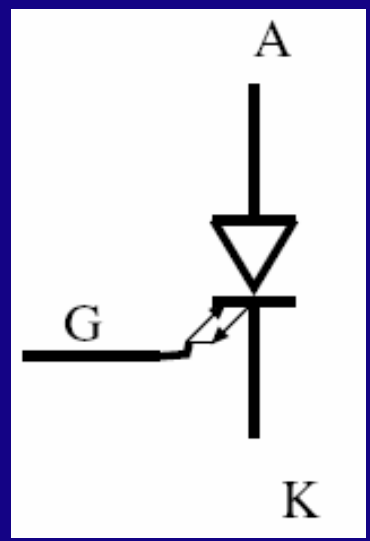
(1961-Small power GTO -GE)

(1981-2.5kV, 1kA - Hitachi, Toshiba)

⇒ can be turned-ON by +ve I_G,

can be turned-OFF by -ve I_G





Description :

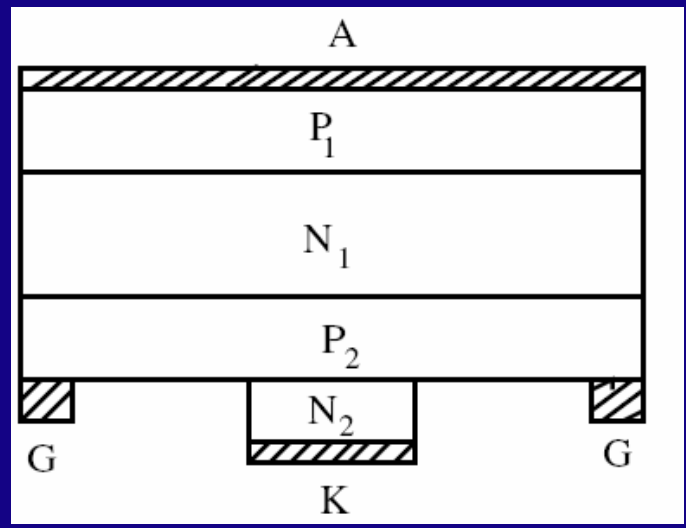
Four layer structure ⇒ similar to SCR

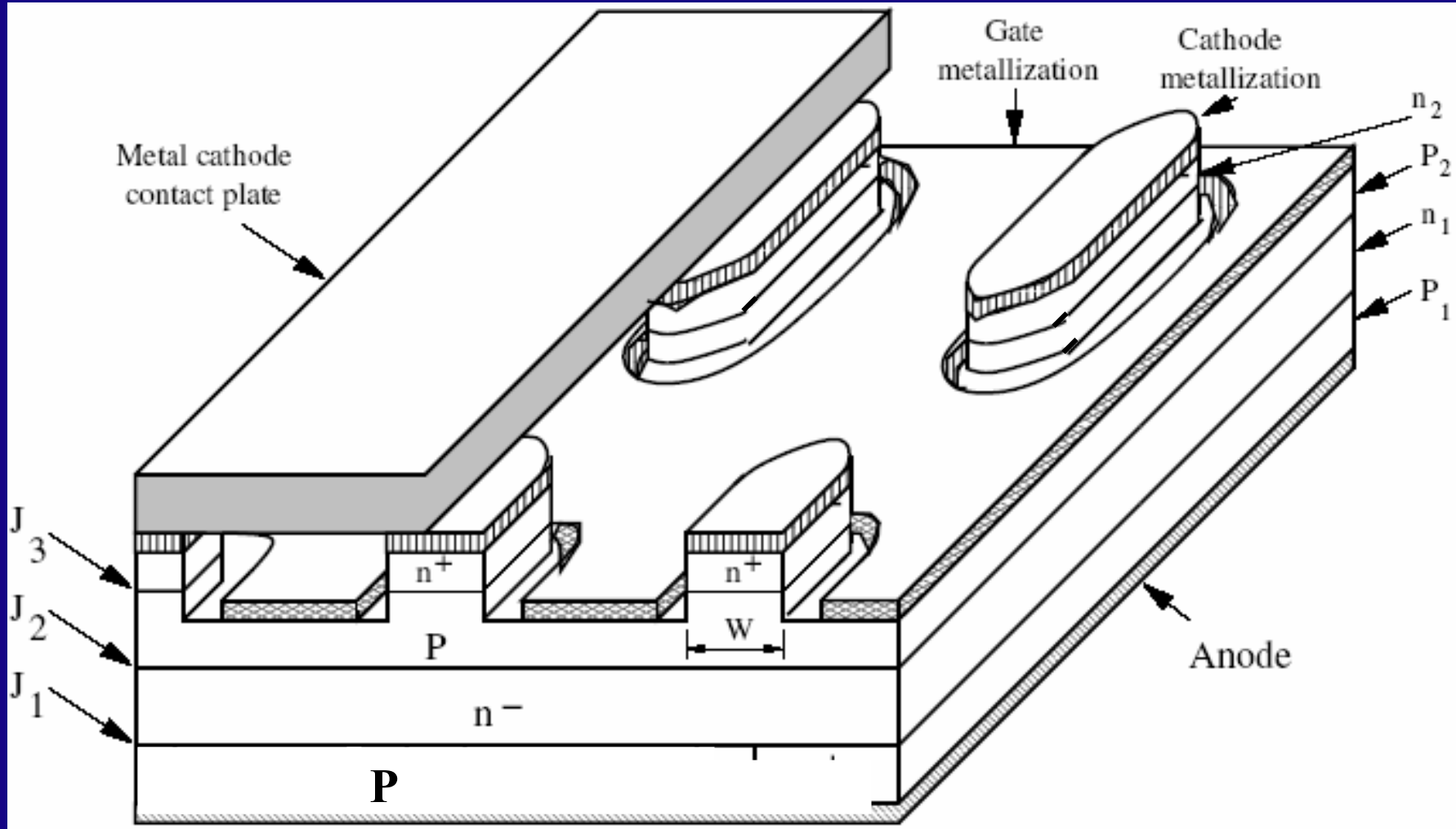
⇒ Thickness of P_2 < that in SCR

⇒ N_2 layer is removed by itching in place where gate contacts are situated

⇒ These cells are surrounded by gate,they are brought together by a cathode plate

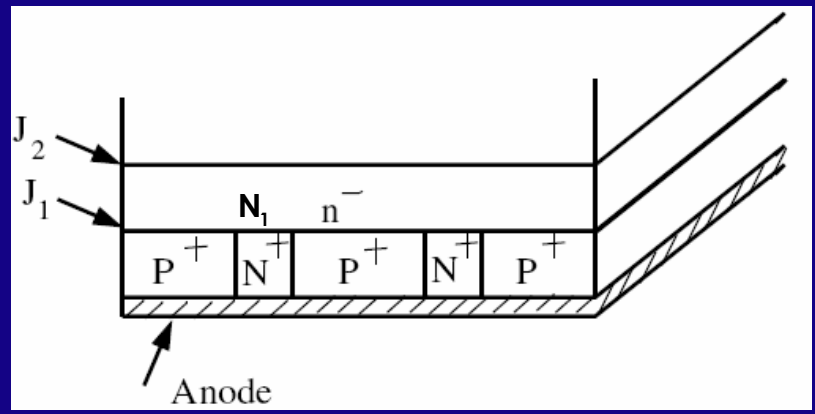
⇒ GTO can be seen as a large number of GTO's in parallel





Vertical cross section & perspective view of a GTO.

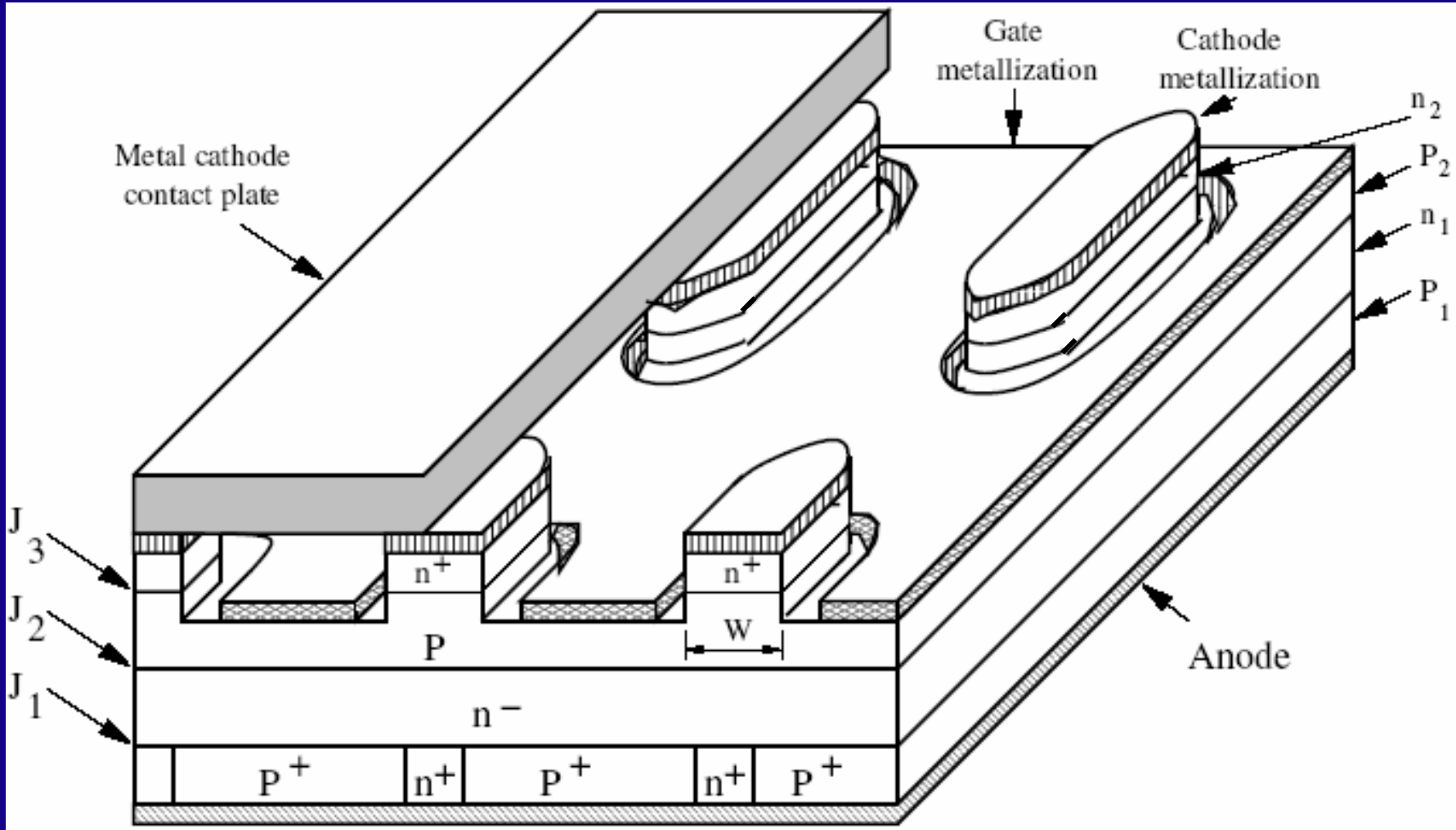
ii) At regular intervals n^+ region penetrates P_1 layer to make contact with n^- region (N_1 base layer)



⇒ Used to speed up the turn-OFF process

⇒ No reverse blocking capability
(only J_3 can now block -ve V. It is very low)

⇒ GTO without anode short can block -ve V



Vertical cross section & perspective view of a GTO.

High level of gate interdigitation results in

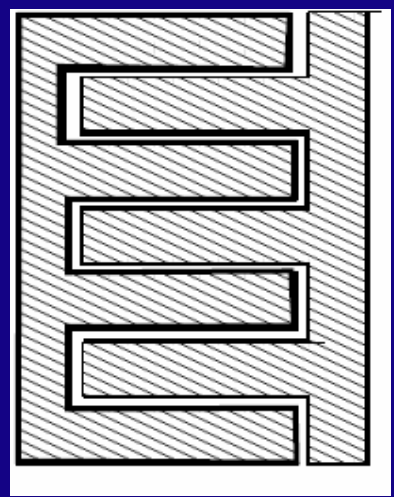
⇒ Even a remote part of cathode region is very near to a gate edge since

⇒ Fast turn-ON speed

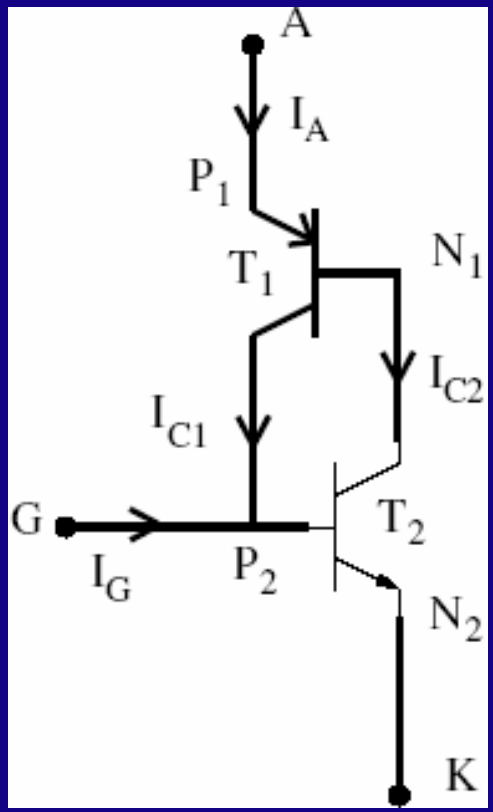
⇒ Like SCR only the area of cathode adjacent to gate electrode is turned ON initialy & then it spreads

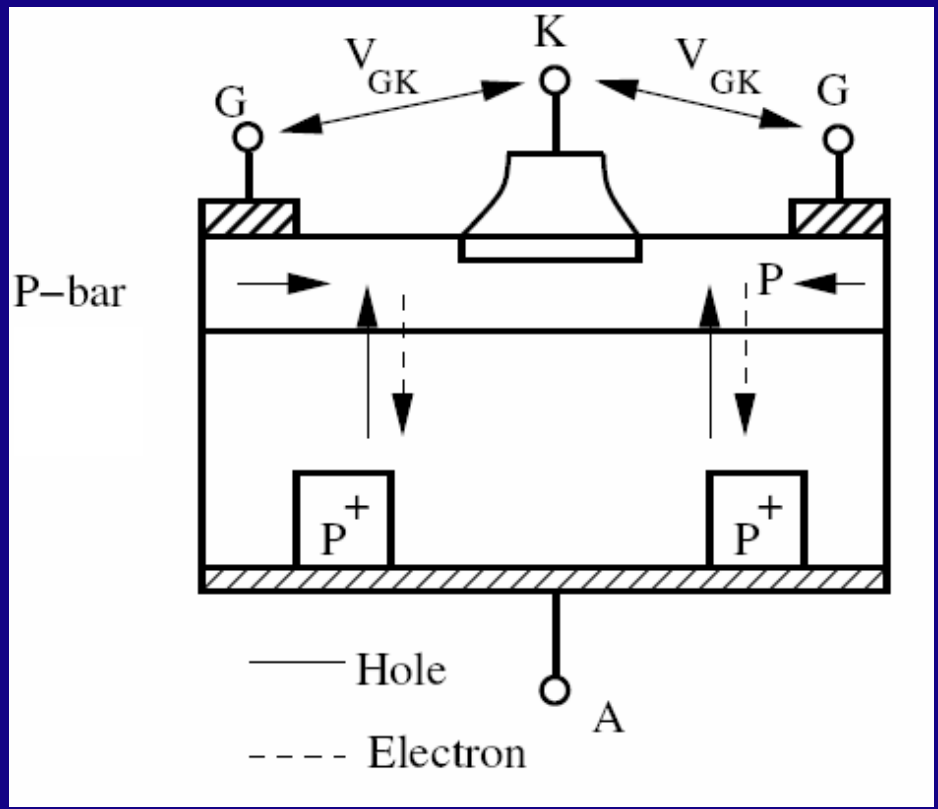
⇒ Turn-ON area is large

⇒ High $\frac{di}{dt}$



$\Rightarrow \therefore$ GTO can be brought into conduction very rapidly





ON – state characteristics:

⇒ They are similar to SCR

⇒ Gate signal can be removed if

$I_A > I_{latching}$

⇒ Recommanded that +ve I_G is not removed.

⇒ $I_{Holding}$ for GTO > $I_{Holding}$ of SCR

⇒ Under transient condition if $i_A \downarrow$ below $I_{Holding}$ some regions may turn off.

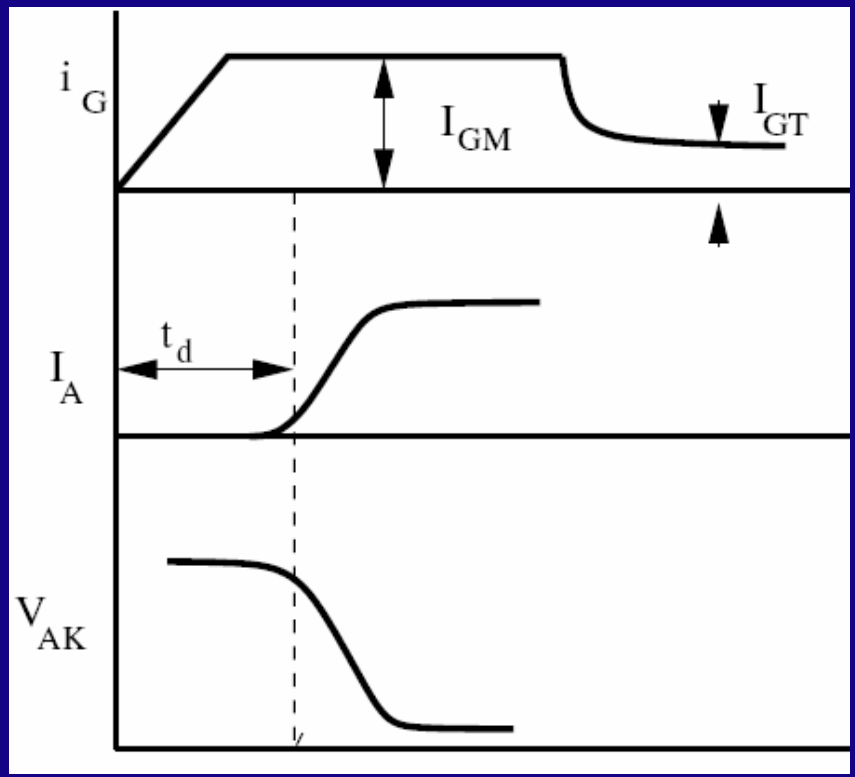
⇒ Anode I now ↑ at a high rate

⇒ Could be destructive.

During turn ON, $\frac{di_G}{dt}$ peak value of I_A should be large enough to ensure that all cathode islands begin to conduct & there is a sharing of anode I

$\Rightarrow$ Else hot spots & could damage the device

$\Rightarrow I_{GM} \geq 10\, I_{GT}$

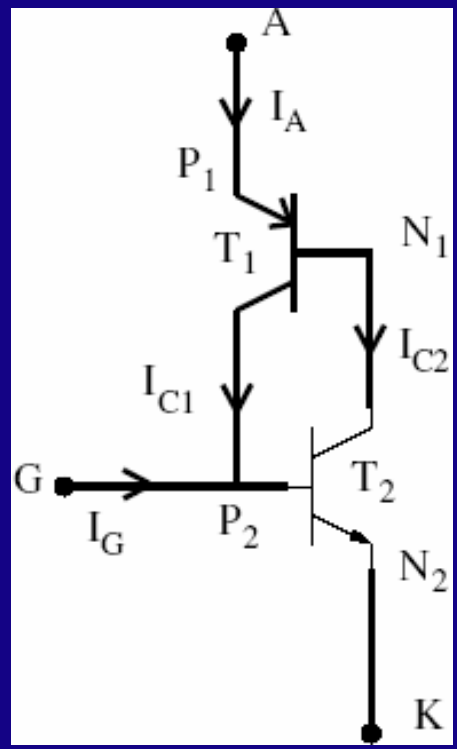


Turn – off of GTO:

When thyristor (or GTO) is ON, both T_1 & T_2 are in saturation.

By $\downarrow I_{B2}$, T_2 can be brought out of saturation.

The total saturation current of the GTO



$$i_A = \frac{a_2 I_G + i_{CBO}}{1-(a_1 + a_2)} \text{-----(A)}$$

$$i_{CBO} = i_{CBO1} + i_{CBO2}$$

When GTO is in ON state, i_G is very small.

$$\therefore\ i_{A(ON)} = \frac{i_{CBO}}{1-(\alpha_1+\alpha_2)}$$

Is the current to be turned OFF

From eqn. (A), $i_A = 0$ if there is a large gate current

such as $i_G = \dfrac{-i_{CBO}}{\alpha_2}$

$$\therefore\ \frac{i_{A(ON)}}{i_G} = \frac{\alpha_2}{(\alpha_1+\alpha_2)-1}$$

$\alpha_2 \rightarrow$ Should be as high as possible

transistor $N_1\ P_2\ N_2 \Rightarrow$ should have a high current gain

$\Rightarrow P_2$ layer should be very thin & N_2 should be heavily doped.

To turn – OFF a GTO:

⇒ Gate is reversed biased w.r.t. cathode

⇒ Holes from anode are extracted from P-base (P_2)

⇒ 'V' drop is developed in P-base region

⇒ Eventually reversed biases G-K junction & cut-off injection of electrons

⇒ As the holes extraction continues, P_2 is further depleted.

⇒ Conduction area ↓

⇒ Anode I flows through the area which is far away from gate.

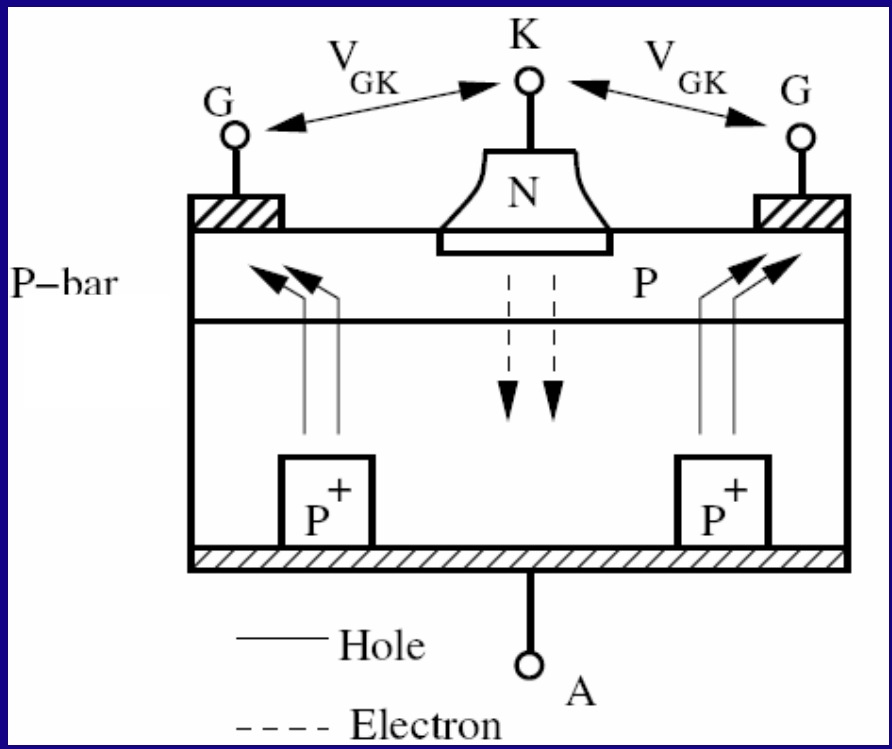
⇒ May form high current density filaments

⇒ May lead to localised heating

⇒ Should be controlled

⇒ Device may fail

⇒ Eventually device turns-OFF



Turn – OFF :

Performance is generally influenced by the characteristics of gate turn-OFF circuit.

$\Rightarrow$ Turn-OFF gain is low (around 6-15)

$\Rightarrow$ If $i_A = 100A$, $i_G = 10A$ (but for a short period)

As -ve I_G is established, anode I starts $\downarrow$ after a time $t_s \rightarrow$ storage time

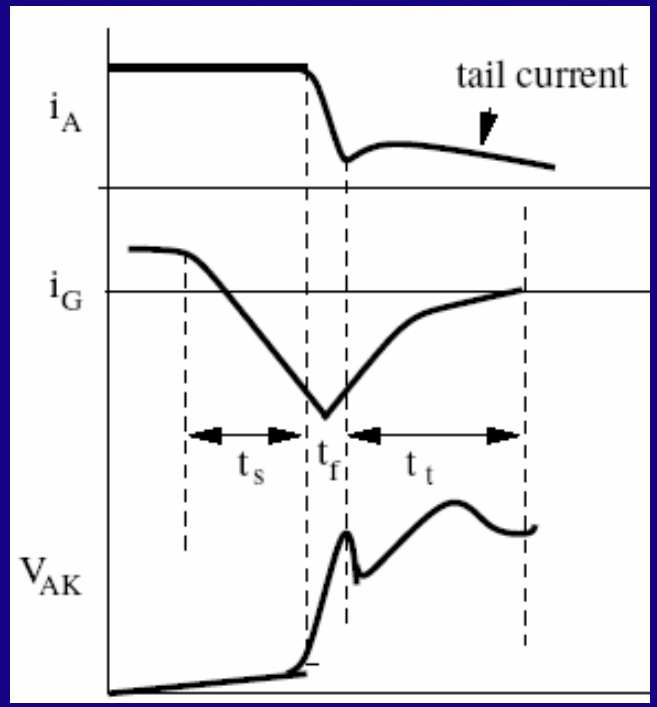
Turn-OFF process can not be studied without taking the snubber into account.

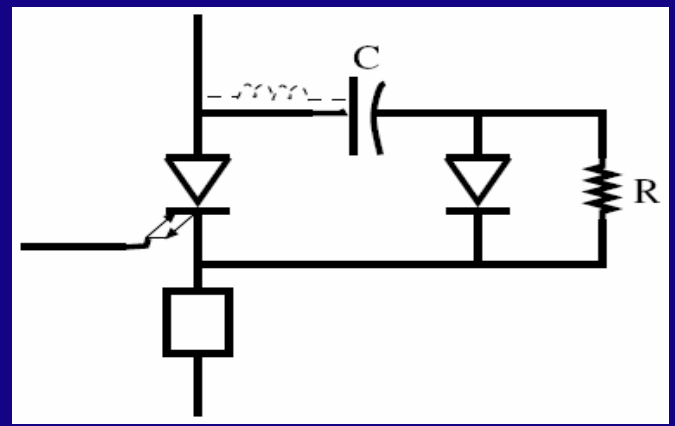
(Turn on: Small L is sufficient compared to that used in SCR because of interdigitated structure.)

$t_s \rightarrow$ Storage time is of the order of few μs.

Application of $-I_G$ brings about a fast & sudden $\downarrow$ in I_A.

($\frac{di}{dt}$ could be 10^9 A/S)





After t_s anode I starts $\downarrow$ steeply to a tail current in t_f (fall time)

$\Rightarrow$ start flowing through the snubber 'c'

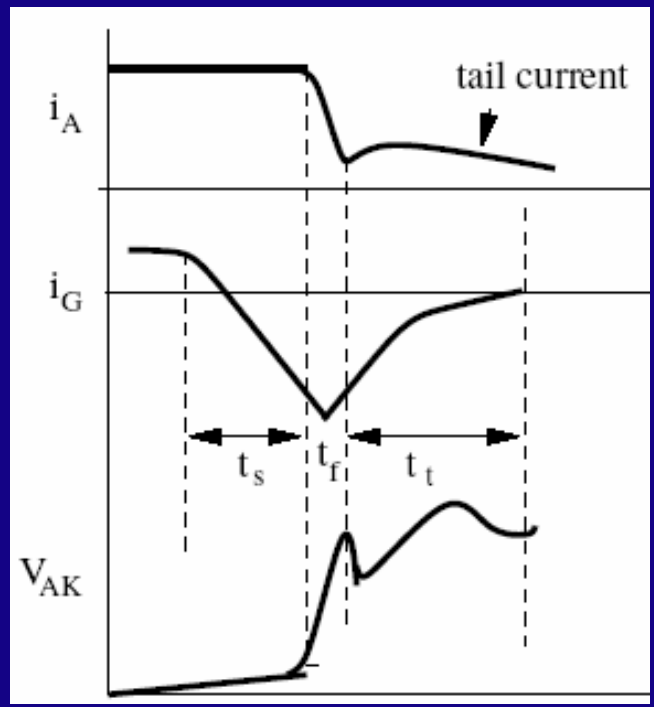
$\Rightarrow$ A large 'V' spike due to stray inductance in the loop formed by C, D & GTO.

$\Rightarrow$ Should be controlled

$\Rightarrow$ Loop L should be very low

$\Rightarrow$ Snubber ckt layout is very important.

$\Rightarrow$ After the spike capacitor limits $\frac{dv}{dt}$



Tail current : ($I_K = 0 \ \therefore \ I_G = I_A$)

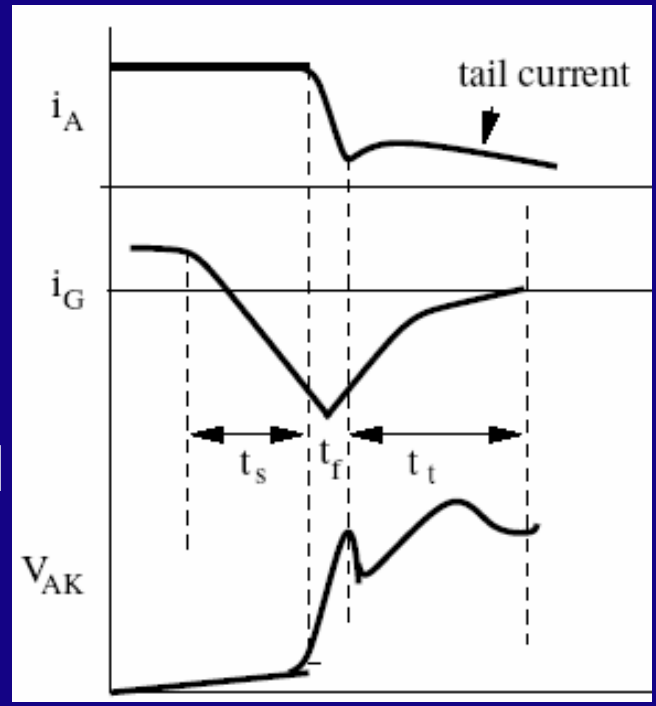
Corresponding to the free charge carriers which exist in blocking layer N_1 (very thick & lightly doped).

Carriers are numerous & they recombine slowly (Higher the forward V to be blocked, thicker the N_1 layer, & longer the tail current period).

t_t is relatively long compared to t_s & t_f.

$\Rightarrow$ During t_f V_{AK} is $\uparrow$

$\Rightarrow$ Turn-OFF losses are significant



Anode short : It produces a short circuit between anode & N_1

$\Rightarrow$ Heavily doped 'N ' cells make the minority carriers trapped in N_1 recombine more quickly

$\Rightarrow$ Structure is no longer symmetrical.

BJT (1948)

In 1975 $\Rightarrow$ 300V, 400A, giant Transistor by Toshiba.

Power transistor are normally of NPN type.

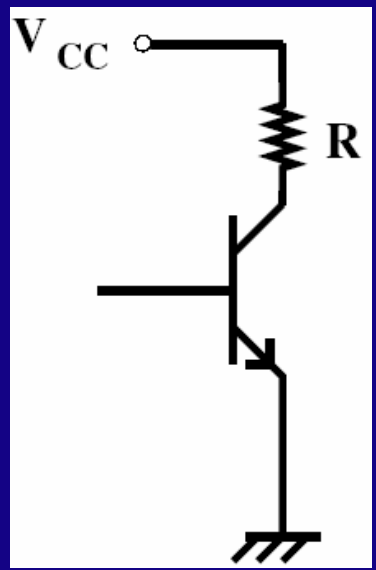
N layer which forms the collector is thickest.

Reverse blocking capability is small.

$\Rightarrow$ Emitter is heavily doped to increase β.

Operated in quasi – saturation

& cut-off



In saturation $I_c = \dfrac{V_{cc} - V_{CE(sat)}}{R}$

$\neq \beta I_B$

⇒ For high voltage BJT, current gain is low when operated in saturation.

⇒ Use Darlington circuit

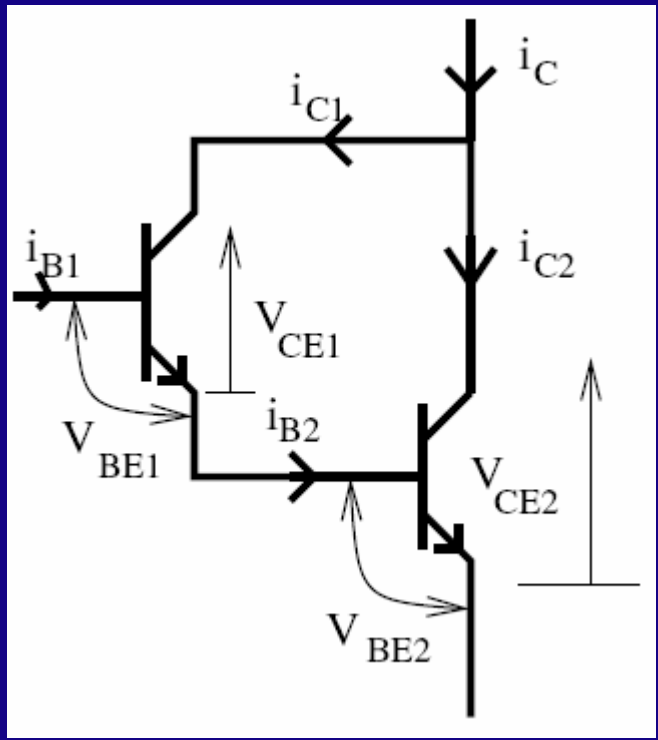
⇒ Requires a low base current

⇒ β_1 & β_2 are current gains of transistors.

$i_C = i_{C1} + i_{C2}$

$i_C = \beta_1 i_{B1} + \beta_2 i_{B2}$

But $i_{B2} = i_{E1} = (\beta + 1) i_{B1}$



$$i_C = \beta_1 i_{B1} + \beta_2(1+\beta_1) i_{B1}$$

$$= (\beta_1 + \beta_2 + \beta_1\beta_2) i_{B1}$$

$\Rightarrow$ Over all gain = $\underline{\beta_1 + \beta_2 + \beta_1\beta_2}$

$\Rightarrow$ Cannot operate T_2 in saturation

since $V_{CE2} = V_{CE1} + V_{BE2}$

$\Rightarrow$ T_2 may be in <u>quasi-saturation</u>

On – State Safe operating Area (FBSOA)

(2) if transistor is ON for a very small time.

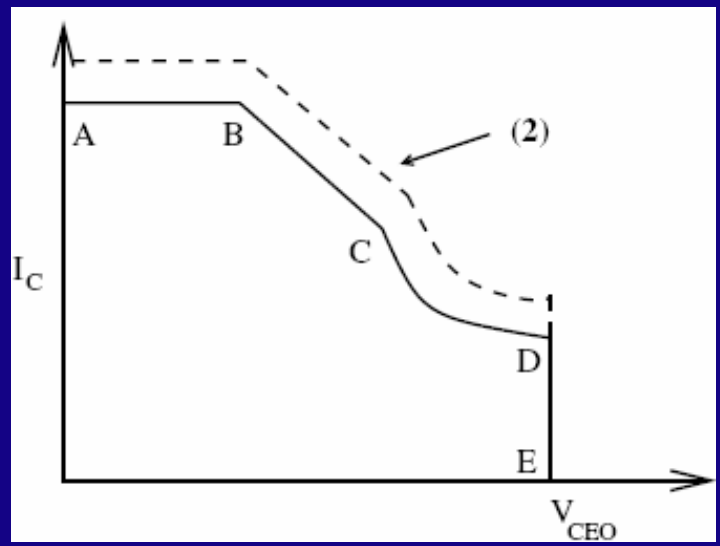
AB → admissible current I_C in steady state

BC → Maximum power that transistor can dissipate

CD → Secondary breakdown

P_{max} limitation (or $T_{j(max)}$)

assumes a uniform current density in the various transistor region.



⇒ Difficult to achieve

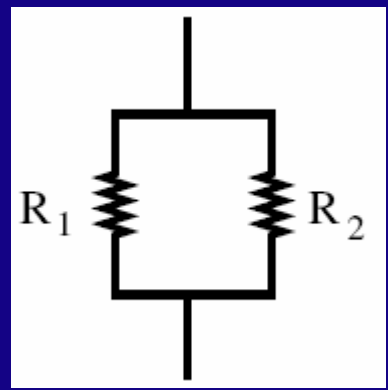
⇒ BJT is a minority carrier device

⇒ Have a -ve resistance coefficient.

⇒ Resistance ↓ as temp ↑

(∵ Minority carrier density ∝ to intrinsic current density which increases exponentially with temperature)

⇒ Power dissipation ↑ as R ↓



⇒ Temp ↑

⇒ Goes ON till device fails
(Thermal runaway)

⇒ Paralleling the devices is difficult.

DE = corrosponding to max. voltage limit.

⇒ If BJT is ON for very small period
boundaries of SOA expand.

Turn-ON:

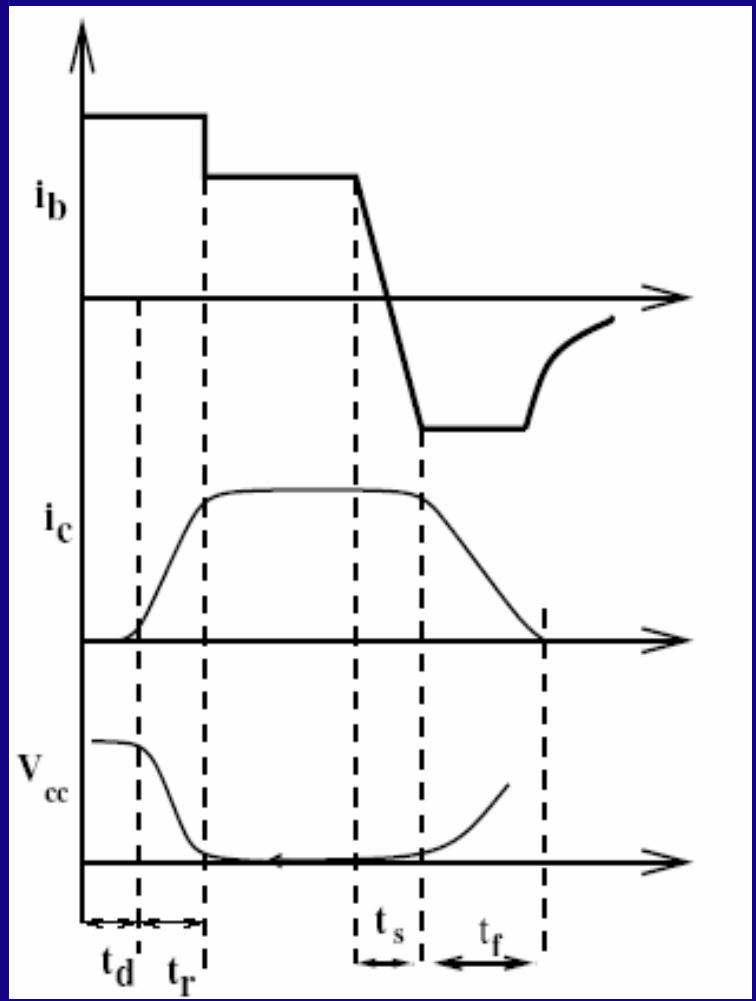
Requires $+I_\beta$ to turn on

$t_{ON} = t_d + t_r$

$t_d \rightarrow$ delay time

$t_r \rightarrow$ rise time

During turn-on, there is a progressive accumulation of charge in the base which increases i_C.



$t_d \rightarrow$ Corrosponding to charging of B-E capacitance

$t_r \rightarrow$ should be very small

In order to reduce t_{ON}, supply $I_B = 1.5I_{B(required)}$

$\Rightarrow$ Transistor is operated in quasi saturation mode.

On state loss $= V_{CE(\square sat)} * I_C$

Turn – off :

$t = t_s + t_f$

$t_s \rightarrow$ Storage time

= delay between the change of base current & the instant when I_C starts $\downarrow$.

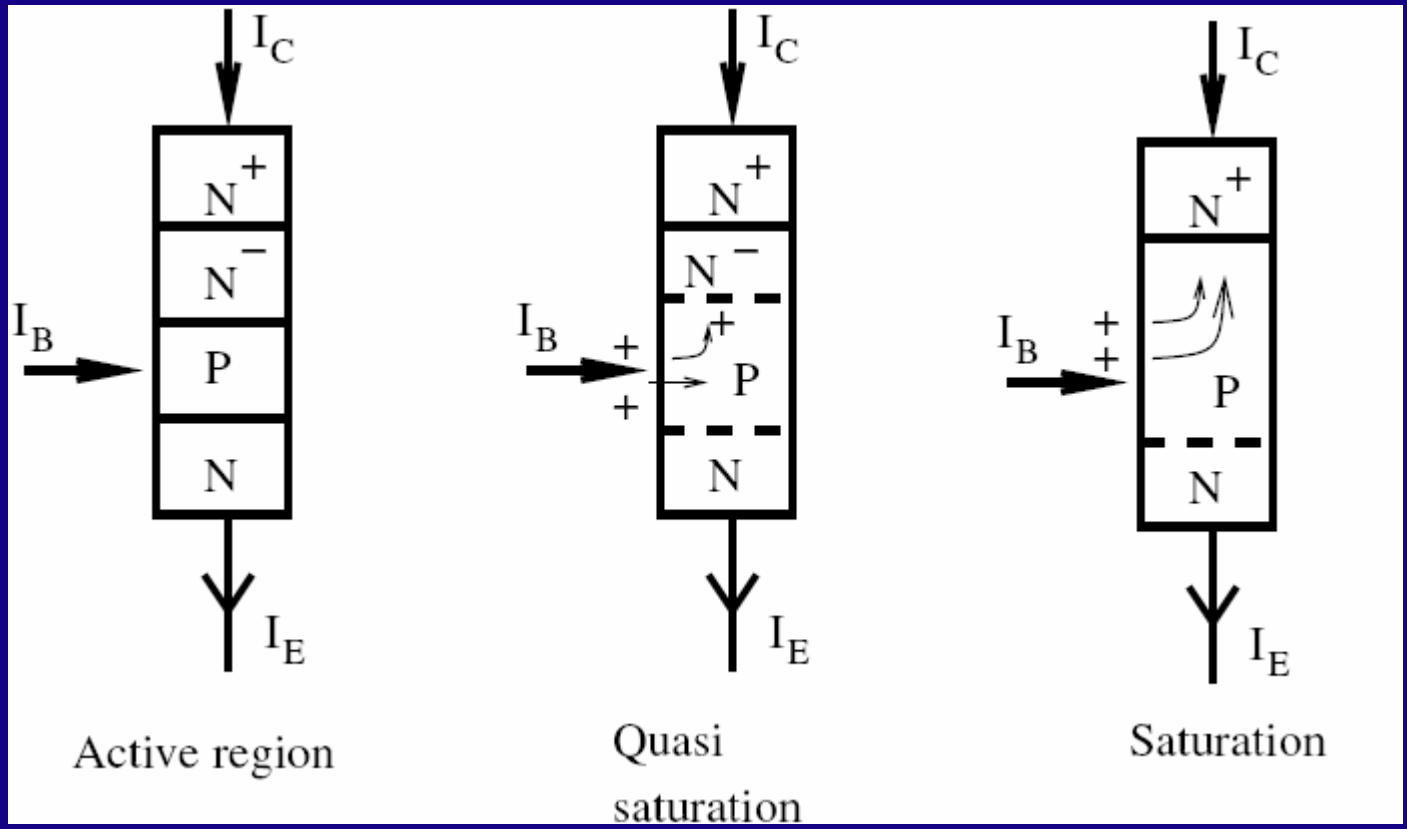
$\Rightarrow$ Limits the upper frequency of operation

$t_f \rightarrow$ Fall time of I_C

Storage time : If transistor is in saturation/quasi saturation, width of base region $\uparrow$

$\Rightarrow$ Equivalent to as if a part of collector is transformed to base. I_C remains constant.

I_C does not fall even though I_B has reversed.



- When excessive number of charges are injected into the base,

⇒ they are diffused in N^- layer of the collector.

⇒ equivalent to P-type doping & to an extension of base thickness, with a corresponding ↓ in N^-.

⇒ due to a ↓ in N^- (highly resistive layer), V_{CE} ↓ for a given I_C. Also β ↓.

⇒ Quasi saturation.

⇒ As I_B ↑ further, N^- is completely changed to P-type.

Highly doped N^+ layer of collector prevents the base region from extending further.

Turn-off

Involves removing all of the stored charge in the transistor

$\Rightarrow$ Could be accomplished by making $I_B = 0$

$\Rightarrow$ Takes long time

$\Rightarrow$ Instead make I_B -ve

What should be the value of I_B during turn off ?

If prior to turn off, the transitor is over saturated state, if large I_B is applied

$\Rightarrow$ Rapid evacuation of the carriers at the base

$\Rightarrow$ Results in rapid cut-off of B-E junction

$\Rightarrow$ Holes in collector region requires certain time to recombine and -ve I_B has negligible effect on this time.

⇒ From the time B-E junction is in cut-off and base collector current continuous to flow, operation is equivalent to diode during t_{rr}

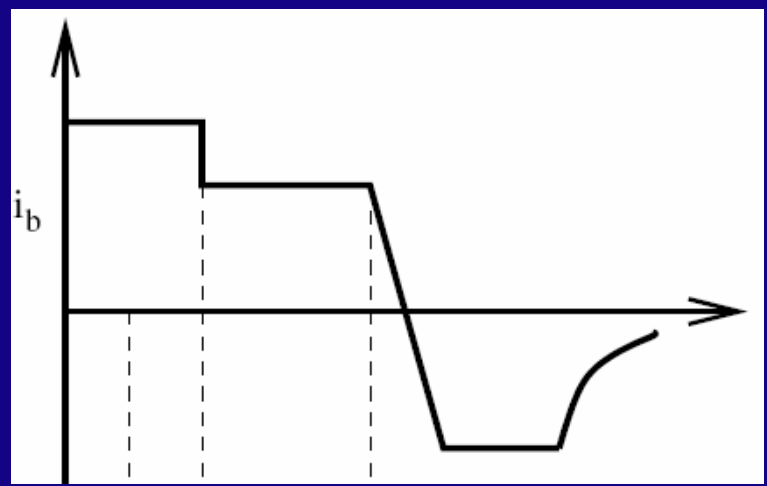
⇒ Also known as current tail

⇒ During this period, in most cases V_{CE} is already high

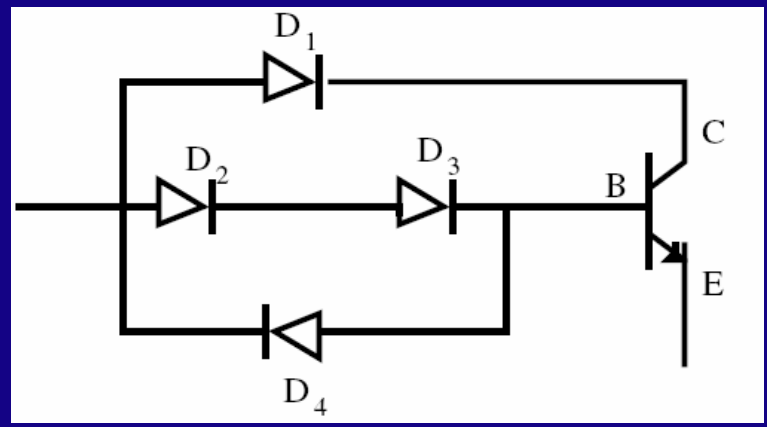
⇒ High losses

⇒ Risk of thermal runaway

⇒ ↑ i_B gradually in the -ve direction



Anti Saturation network(Baker clamp)



Operating the transistor in Quasi saturation region increases V_{CE} slightly.

But t_s is greatly reduced.

Prevent the BJT from over saturating.

Now, $V_{CE} = V_{BE} + V_{D2} + V_{D3} - V_{D1}$

$\Rightarrow$ V_{CE} is maintained at $V_{BE} + V_{D1}$

By connecting additional diodes in series with D_2 or D_3, V_{CE} can be $\uparrow$

-Assume Transistor is off.

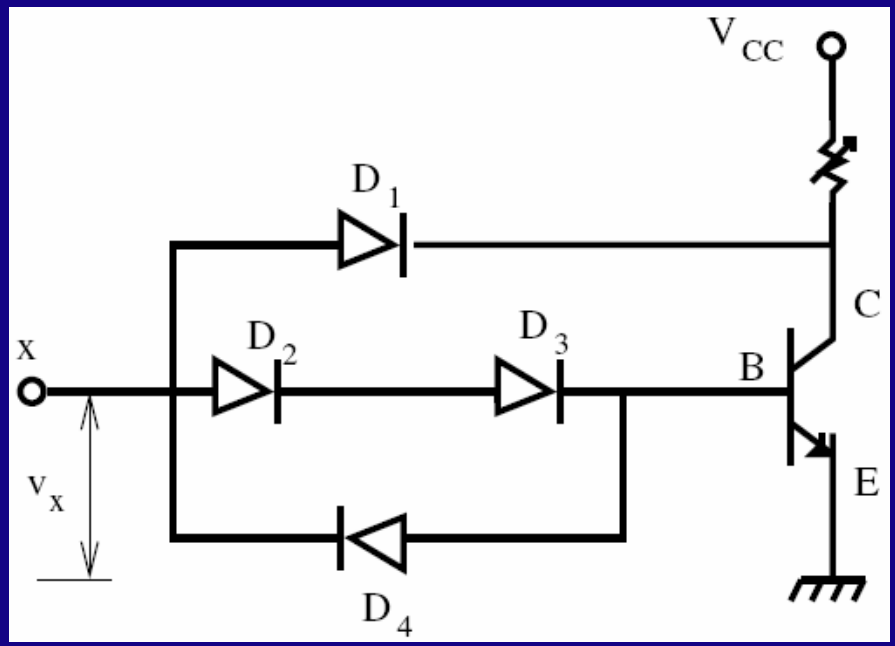
+ve I_B applied at point x

Till $V_{CE} = V_x + V_{D1}$

D_3 is off.

All I_B will flow through

D_2 & D_3 & into the base.



Assume that load has ↓

Since I_B is held constant corresponding to rated load, transistor might get saturated.

$\Rightarrow$ V_{CE} ↓

$\Rightarrow$ When $V_{CE} = V_x + V_{D1}$, D_1 turns on.

Part of I_B flows through D_1

I_B flows into the base ↓

Transistor comes out of saturation

$\Rightarrow$ -ve feedback or 'control value'

$\Rightarrow$ D_4 provides a path for -ve I_B

Review :

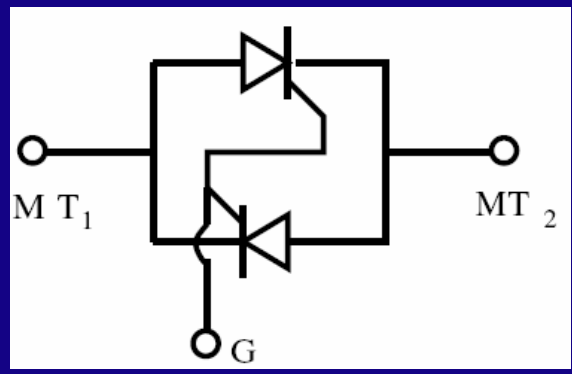
TRIAC :→ Functionally equivalent to 2 thyristors connected anti-parallel.

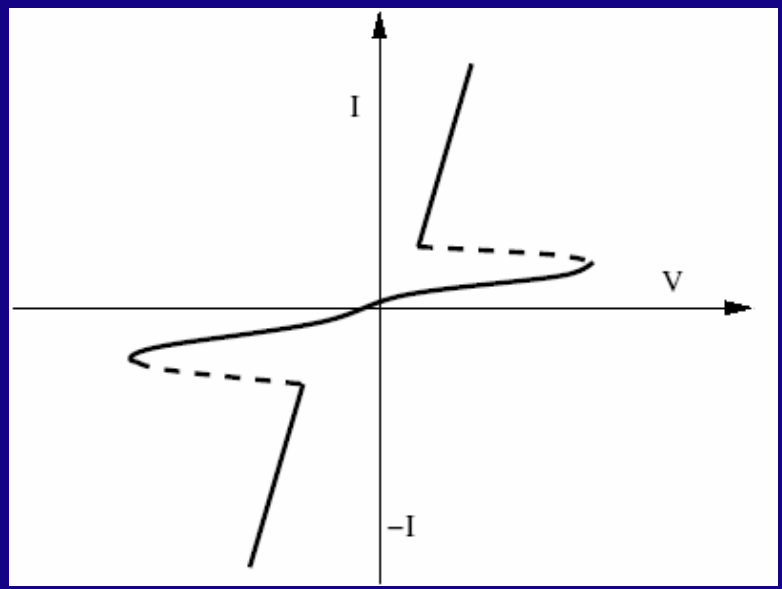
Can be triggered by

MT_2 + ve
I_G +ve $\Big\|$ W.R.T. MT_1

MT_2 - ve
I_G -ve $\Big\|$ W.R.T. MT_1

$\Rightarrow \frac{dv}{dt}$ rating < than that of SCR





GTO: $\rightarrow$ High power device

(6KV, 6KA by MITSUBISHI)

Turn ON $\rightarrow$ by $+I_G$

OFF $\rightarrow$ by $-I_G$

$\Rightarrow$ 4 layer structure

$\Rightarrow$ Thickness of P_2 layer is reduced by $\uparrow$ $\underline{a_2}$

thereby increasing gain during turn-off.

$\Rightarrow$ Gate cathode structure is highly interdigitited

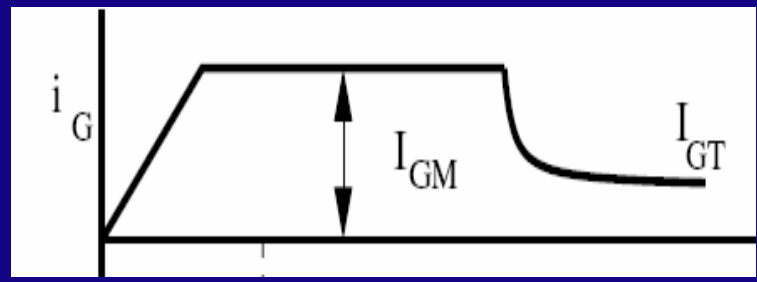
$\Rightarrow$ High $\frac{di}{dt}$ rating

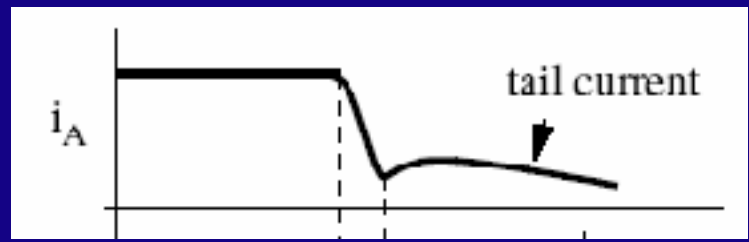
⇒ Gate current to turn-off the GTO is high 10% of I_A

⇒ Though it is a latching device, I_G is maintained during ON period.

⇒ Turn-off loss is high. Can be ↓ by reducing tail current.

⇒ Tail current is due to minority carriers in N_1 layer.



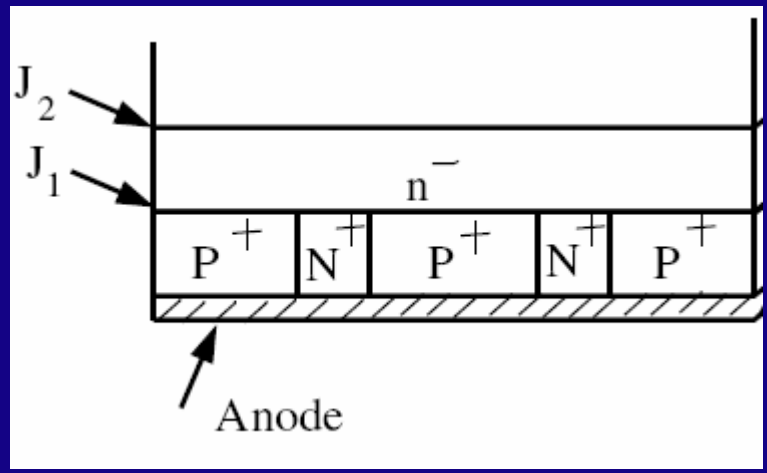


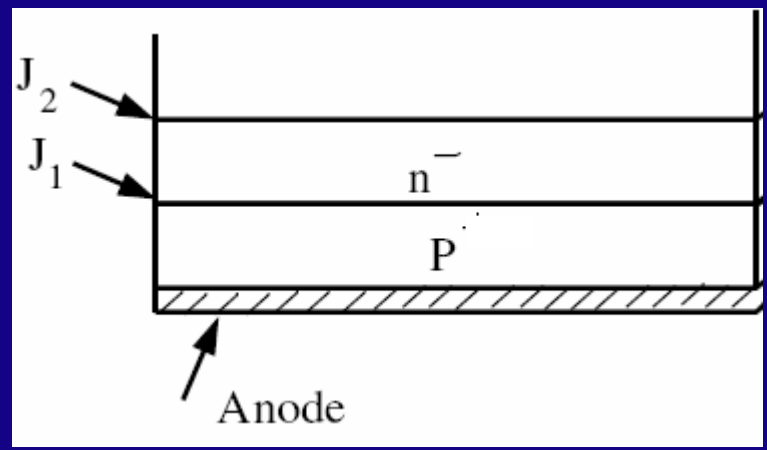
⇒ Duration of tail current ↑ with thickness of N_1 layer

⇒ This duration can be ↓ by using anode short structure

At regular intervals N^+ region penetrates P_1 layer to make contact with N^- region.

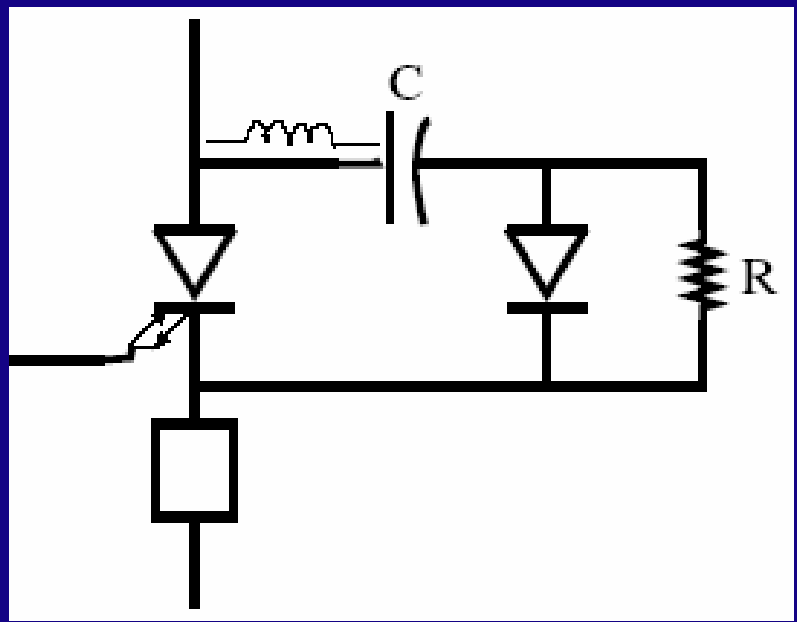
⇒ Cannot block -ve V





Inductance in GTO & turn-off snubber loop should be very small.

A large voltage spike due to loop 'L'.



BJT (1948)

In 1975 $\Rightarrow$ 300V, 400A, giant Transistor by Toshiba.

$\Rightarrow$ Power transistors are normally of NPN type.

$\Rightarrow$ N layer which forms the collector is thickest.

$\Rightarrow$ Reverse blocking capability is small.

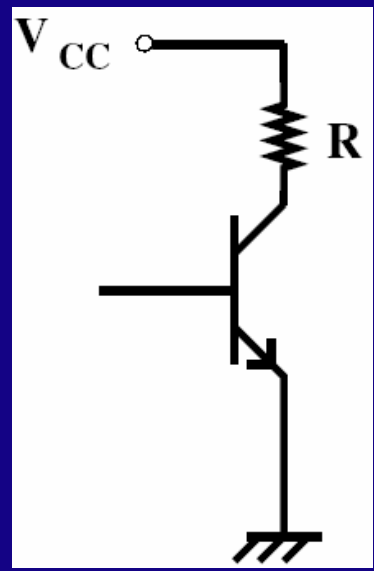
$\Rightarrow$ Emitter is heavily doped to increase β.

$\Rightarrow$ Operated in quasi – saturation

& cut-off

In saturation $I_c = \dfrac{V_{cc} - V_{CE(sat)}}{R}$

$\neq \beta I_B$

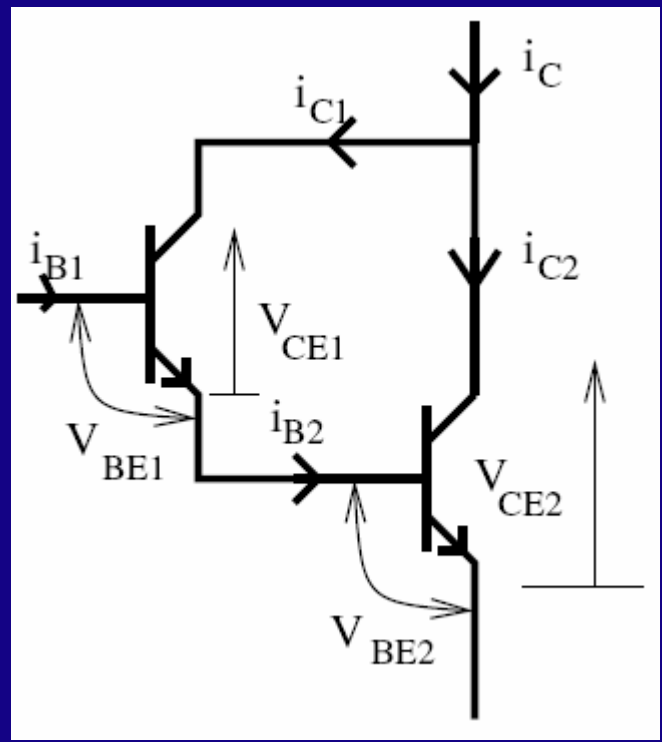


⇒ For high voltage BJT, current gain is low when operated in saturation.

⇒ Use Darlington circuit

⇒ Requires a low base current

⇒ β_1 & β_2 are current gains of transistors.



$$i_C = i_{C1} + i_{C2}$$

$$i_C = \beta_1 i_{B1} + \beta_2 i_{B2}$$

But $i_{B2} = i_{E1} = (\beta + 1) i_{B1}$

$$i_C = \beta_1 i_{B1} + \beta_2(1+\beta_1) i_{B1}$$

$$= (\beta_1 + \beta_2 + \beta_1\beta_2) i_{B1}$$

$\Rightarrow$ Overall gain = $\underline{\beta_1 + \beta_2 + \beta_1\beta_2}$

$\Rightarrow$ Cannot operate T_2 in saturation

since $V_{CE2} = V_{CE1} + V_{BE2}$

$\Rightarrow$ T_2 may be in <u>quasi-saturation</u>

On – State Safe operating Area (FBSOA)

(2) if transistor is ON for a very small time.

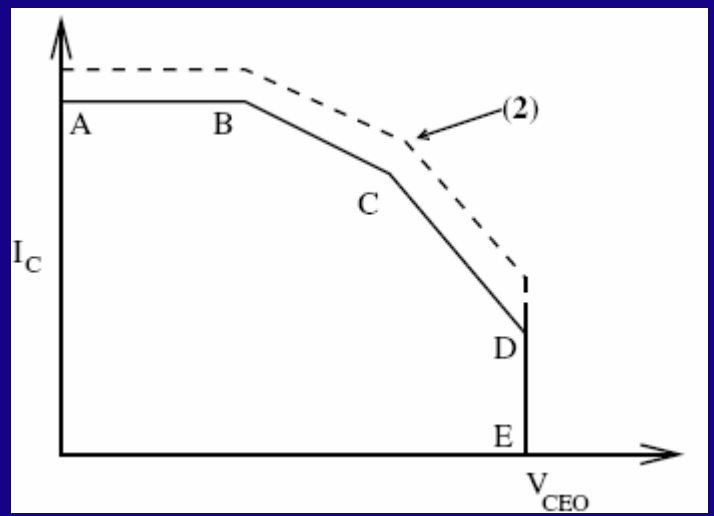
AB → admissible current I_C in steady state

BC → Maximum power that transistor can dissipate

CD → Due to secondary breakdown.

P_{max} limitation (or $T_{j(max)}$)

assumes a uniform current density in the various transistor regions.



⇒ Difficult to achieve

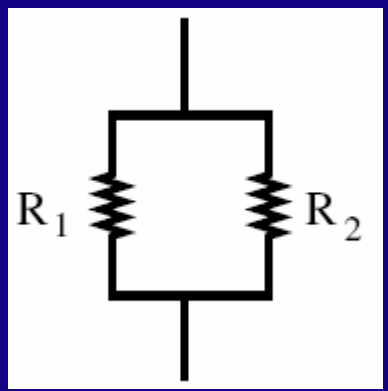
⇒ BJT is a minority carrier device

⇒ Has a -ve resistance coefficient.

⇒ Resistance ↓ as temp. ↑

(∵ Minority carrier density ∝ to intrinsic current density which increases exponentially with temperature)

⇒ Power dissipation ↑ as R ↓



⇒ Temp ↑

⇒ Goes ON till device fails
(Thermal runaway)

⇒ Paralleling the devices is difficult.

DE = corresponds to max. voltage limit.

⇒ If BJT is ON for a very small period, boundaries of SOA expand.

Turn-ON:

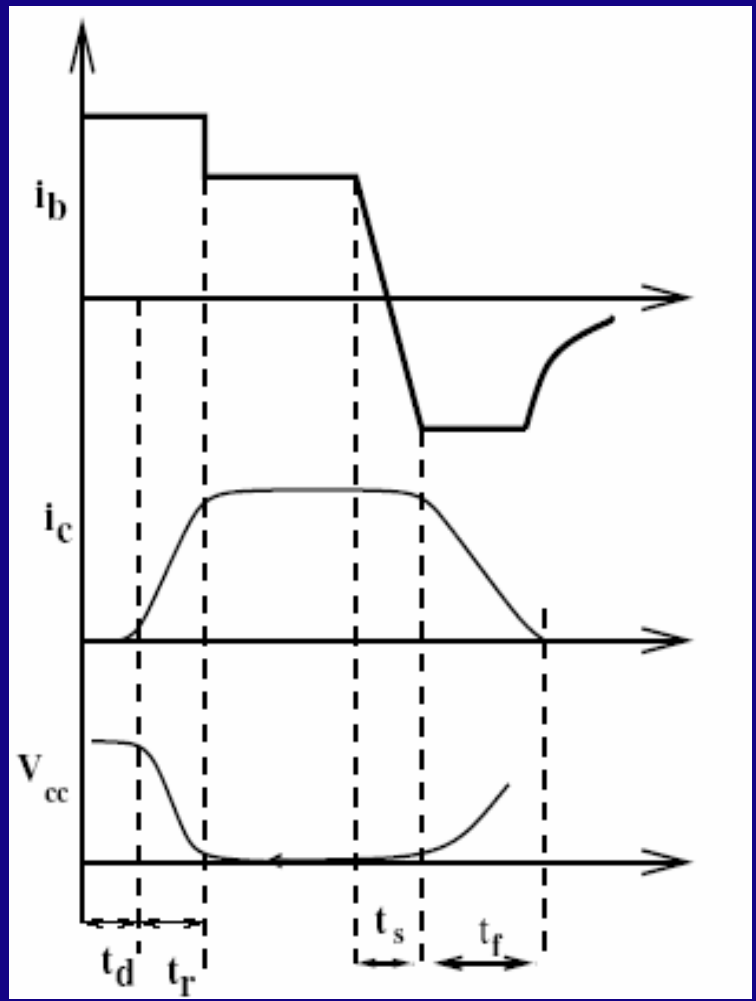
Requires $+I_\beta$ to turn on

$t_{ON} = t_d + t_r$

$t_d \rightarrow$ delay time

$t_r \rightarrow$ rise time

During turn-on, there is a progressive accumulation of charge in the base which increases i_C.



$t_d \rightarrow$ delay time.

$t_r \rightarrow$ should be very small

In order to reduce t_{ON}, supply $I_B = 1.5 I_{B(required)}$

$\Rightarrow$ Transistor is operated in quasi saturation mode.

On state loss = $V_{CE(\square sat)} * I_C$

Turn – off :

$t = t_s + t_f$

$t_s \rightarrow$ Storage time

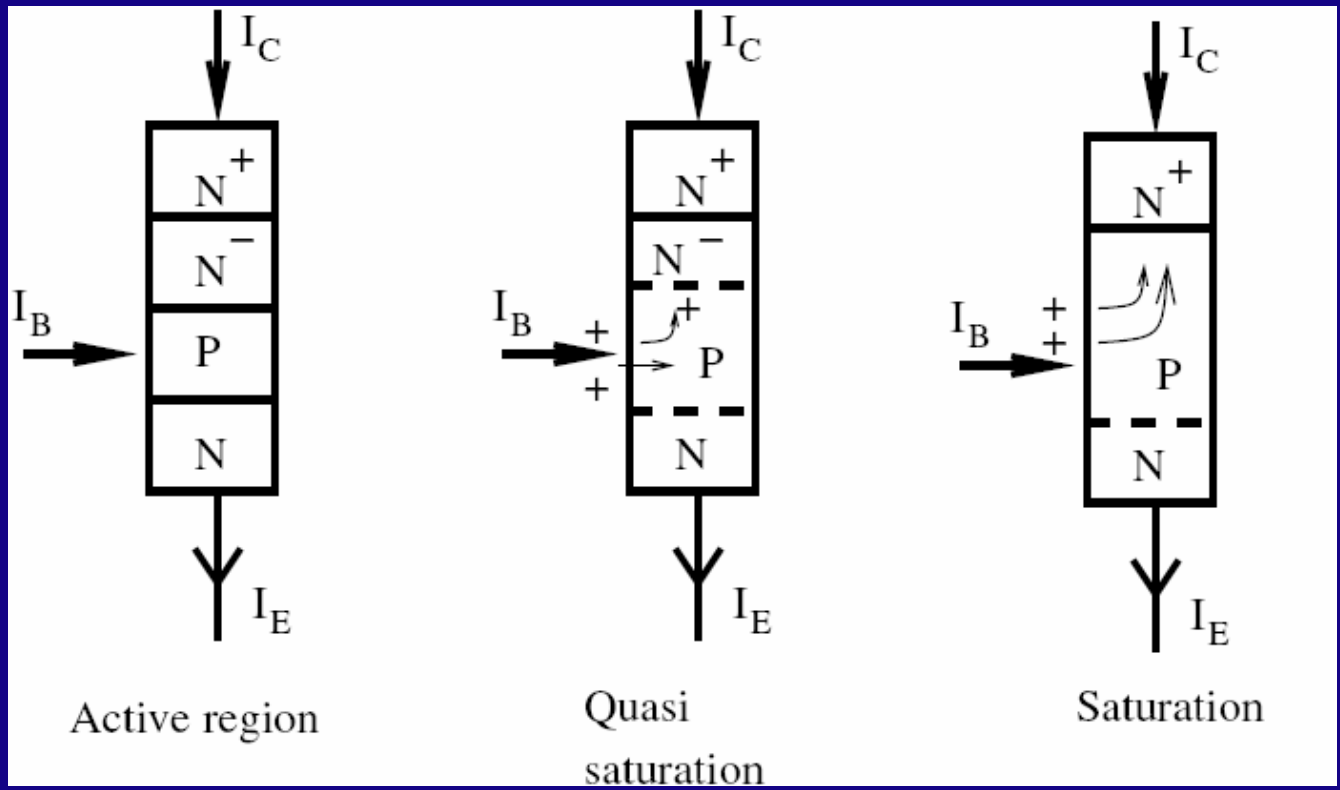
= delay between the change of base current & the instant when I_C starts $\downarrow$.

$\Rightarrow$ Limits the upper frequency of operation

$t_f \rightarrow$ Fall time of I_C

Storage time : If transistor is in saturation/quasi saturation, width of base region $\uparrow$

$\Rightarrow$ Equivalent to as if a part of collector is transformed to base. I_C remains constant.



⇒ When excessive number of charges are injected into the base,

⇒ They are diffused in N^- layer of the collector.

⇒ equivalent to P-type doping & an extension of base thickness, with a corresponding ↓ in N^-.

⇒ due to a ↓ in N^- (highly resistive layer), V_{CE} ↓ for a given I_C. Also β ↓.

⇒ Quasi saturation.

⇒ As I_B ↑ further, N^- is completely changed to P-type.

Highly doped N^+ layer of collector prevents the base region from extending further.

Turn-off

Involves removing all of the stored charge in the transistor

$\Rightarrow$ Could be accomplished by making $I_B = 0$

$\Rightarrow$ Takes a long time

$\Rightarrow$ Instead make I_B -ve

What should be the value of I_B during turn off ?

If prior to turn off, the transitor is in over-saturated state and a large I_B is applied

$\Rightarrow$ Rapid evacuation of the carriers at the base

$\Rightarrow$ Results in rapid cut-off of B-E junction

$\Rightarrow$ Holes in collector region requires certain time to recombine and -ve I_B has negligible effect on this time.

⇒ From the time B-E junction is in cut-off and base collector current continues to flow, operation is equivalent to a diode during t_{rr}

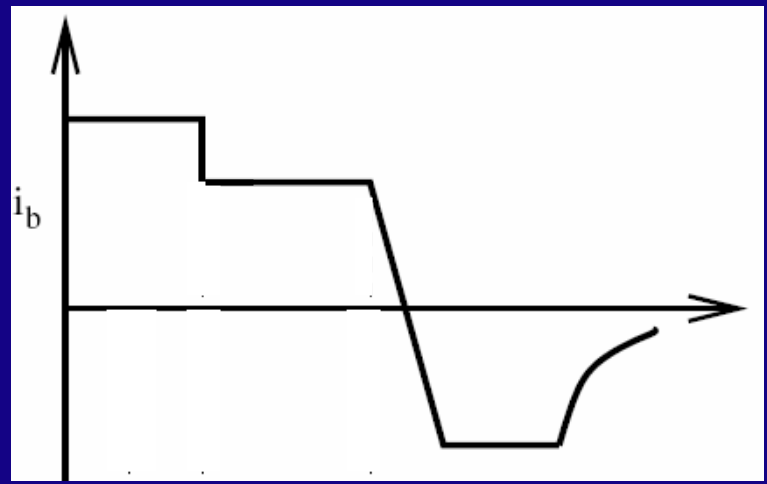
⇒ Also known as <u>current tail</u>

⇒ During this period, in most cases V_{CE} is already high

⇒ High losses

⇒ Risk of thermal runaway

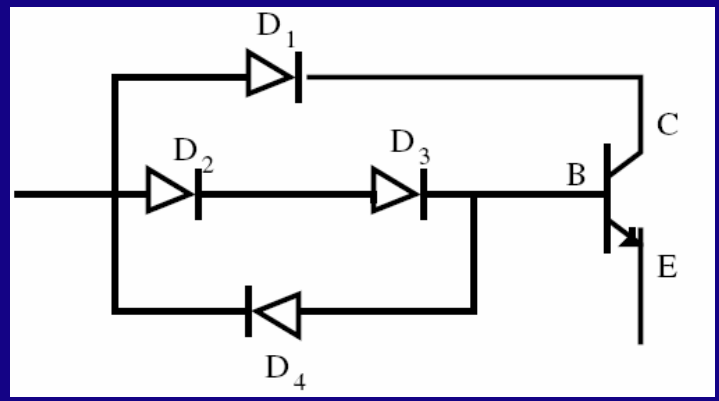
⇒ ↑ i_B gradually in the -ve direction



Anti-Saturation network (Baker clamp)

Operating the transistor in Quasi saturation region increases V_{CE} slightly.

But t_s is greatly reduced.



Prevent the BJT from over saturating.

Now, $V_{CE} = V_{BE} + V_{D2} + V_{D3} - V_{D1}$

$\Rightarrow$ V_{CE} is maintained at $V_{BE} + V_{D1}$

By connecting additional diodes in series with D_2 or D_3, V_{CE} can be increased.

Assume Transistor is off.

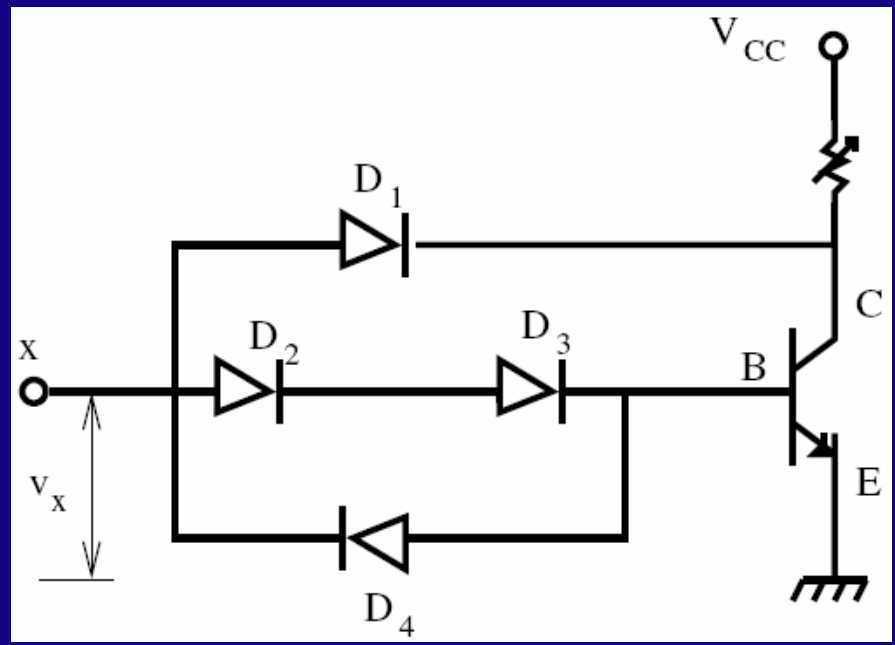
+ve I_B applied at point x

Till $V_{CE} = V_x + V_{D1}$

D_1 is off.

All I_B will flow through

D_2 & D_3 & into the base.



Assume that load has $\downarrow$

Since I_B is held constant corresponding to rated load, transistor might get saturated.

$\Rightarrow$ $V_{CE} \downarrow$

$\Rightarrow$ When $V_{CE} = V_x - V_{D1}$, D_1 turns on.

Part of I_B flows through D_1

$\Rightarrow$ Current flowing into the base $\downarrow$

$\Rightarrow$ Transistor comes out of saturation

$\Rightarrow$ -ve feedback or 'control value'

$\Rightarrow$ D_4 provides a path for -ve I_B

Review :

1) B.J.T $\Rightarrow$ Should not be driven into saturation

$\Rightarrow$ Storage time $\uparrow$

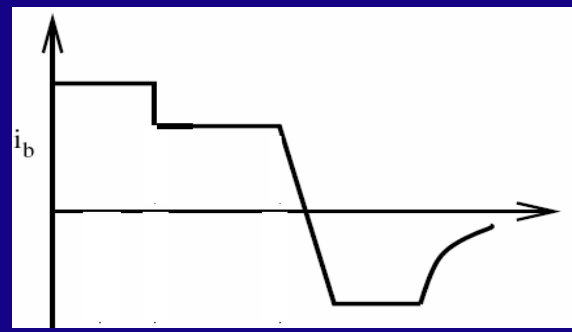
$\Rightarrow$ Operated in quasi-saturation

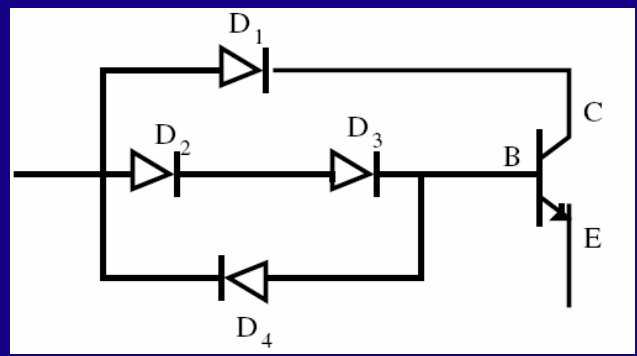
$\Rightarrow$ Supply I_B ; $1.5I_{B(st)}$ to $\downarrow$ T_{ON}

$\Rightarrow$ Supply -ve I_B to turn off BJT.

$\Rightarrow$ Should be gradually increased.

$\Rightarrow$ Use Baker clamp to prevent the transistor operating in saturation.



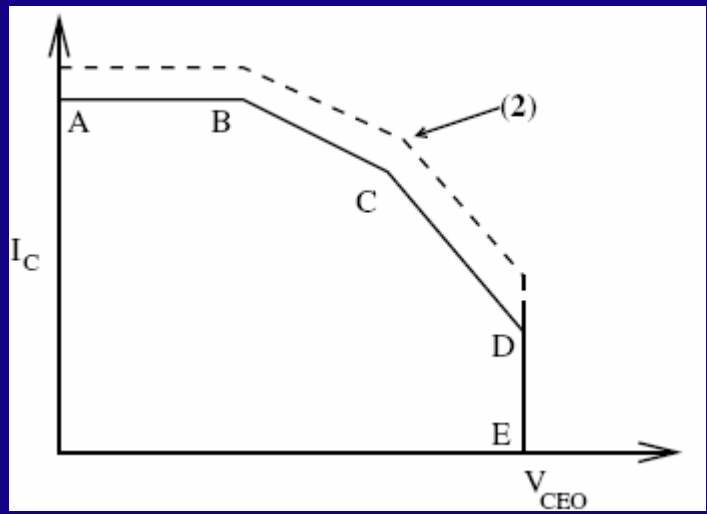


2) Minority carrier device

⇒ -ve resistance coefficient

⇒ paralleling is difficult

⇒ SOA has secondary breakdown limit.

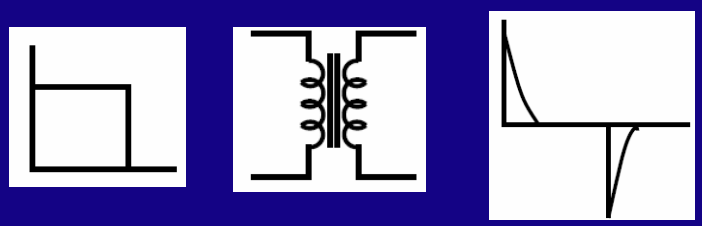


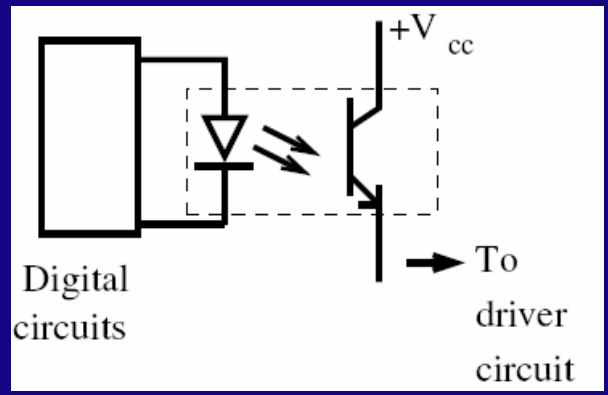
Isolation : In latching devices, pulse transformer is used.

⇒ BJT requires continuous base drive.

⇒ Use OPTO ISOLATOR

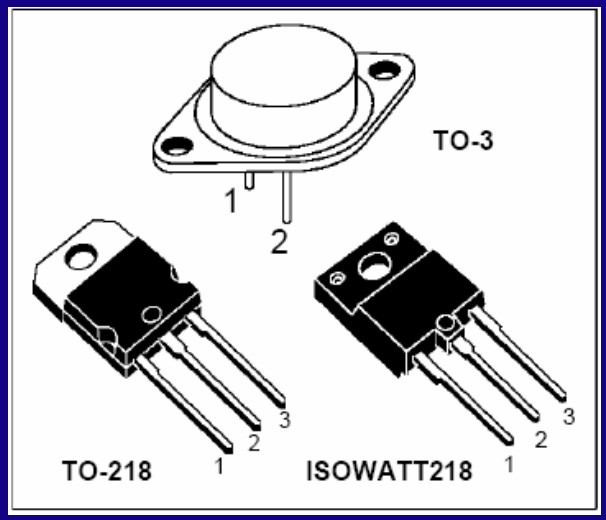
⇒ Transistor requires supply voltage.

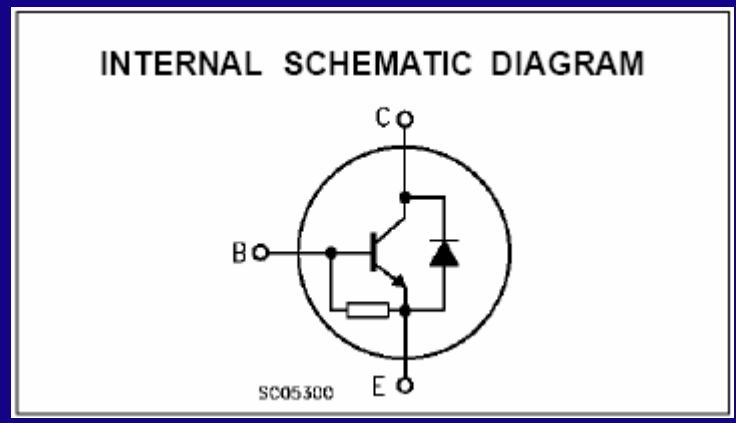




As the no. of devices ↑, base drive circuit may become bulky.

BU208D





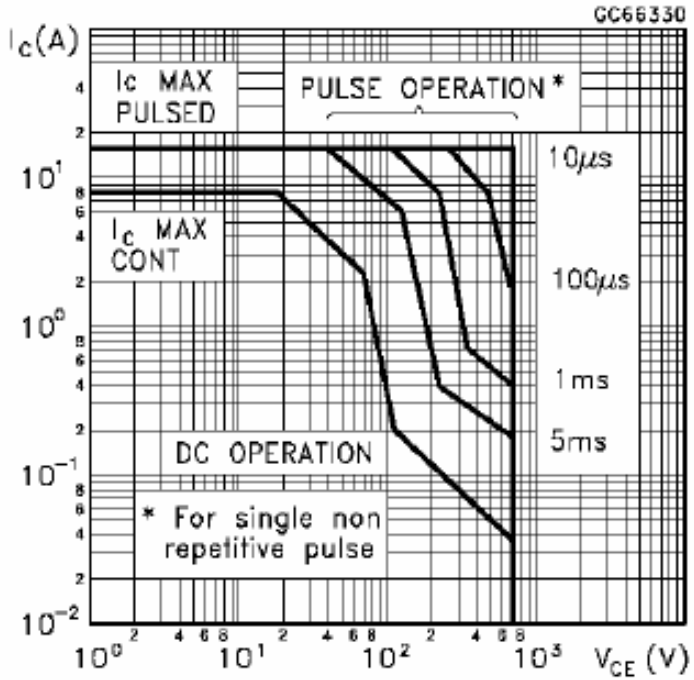
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	8	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	15	A

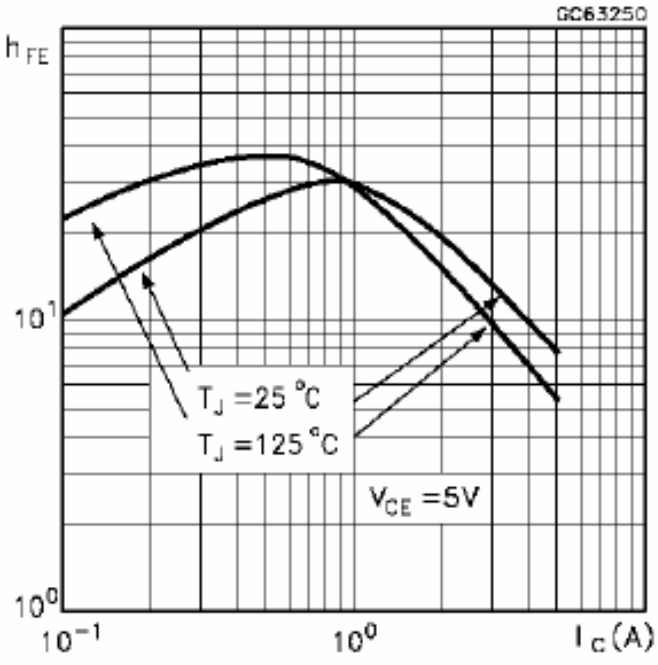
ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 4.5 A I_B = 2 A			1	V
	INDUCTIVE LOAD	I_C = 4.5 A h_{FE} = 2.5 V_{CC} = 140 V				
t_s	Storage Time	L_C = 0.9 mH L_B = 3 µH		7		µs
t_f	Fall Time			550		ns

Safe Operating Area (TO-3)



DC Current Gain



BU208D-BJT: $V_{CEO} = 700V,\ I_C = 8A, t_S = 7\mu s, t_F = 500ns$

h_{FE} **at 5A ;** $\underline{5}$

$\therefore I_B = \underline{1}$ **A**

$I_{B(START)} = \underline{1.5}$ **A**

$\Rightarrow$ **A small PT to drive another PT!**

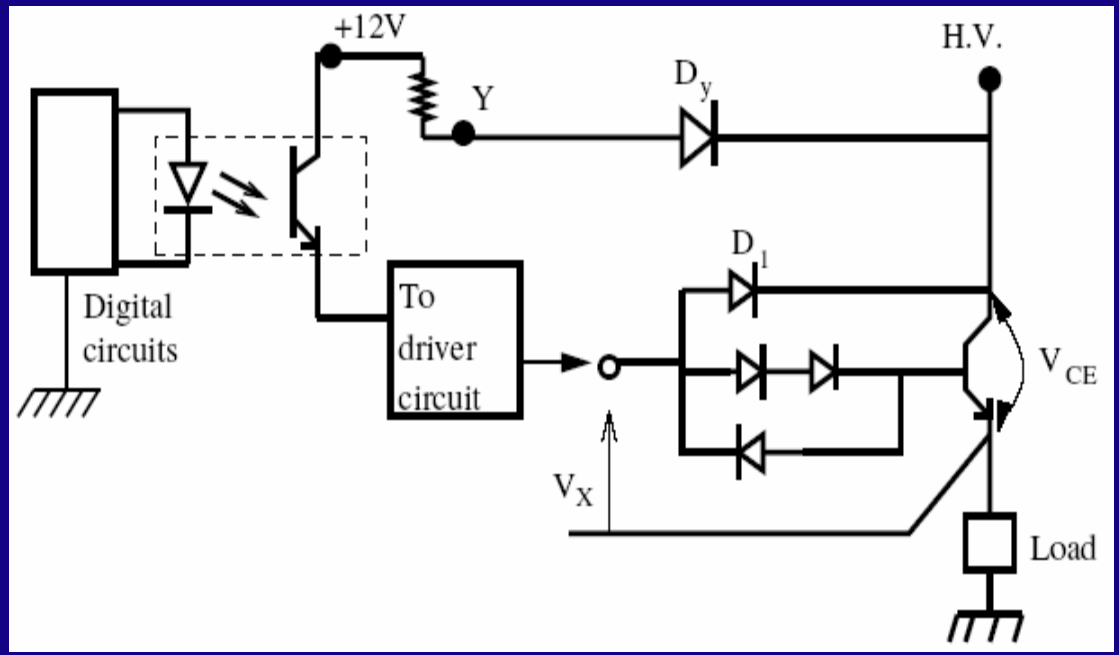
Overload protection :

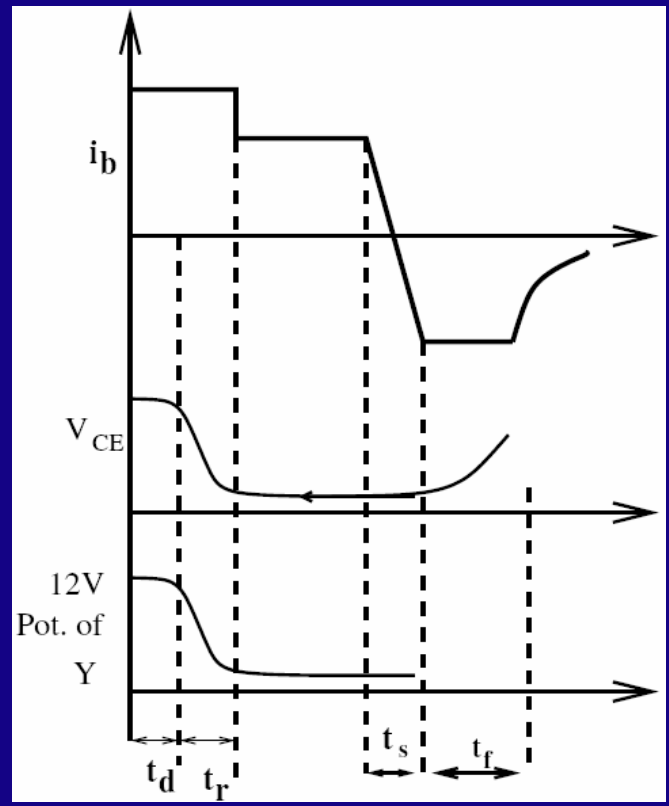
⇒ **Cannot be protected using a fuse.**

⇒ **Fuse is not fast enough**

⇒ **Overload capacity is not much higher than rated steady state capacity.**

⇒ **Necessary to detect an overcurrent condition & remove the base drive immediately.**


+12V
H.V.
Y
D_y
D_1
Digital
circuits
To
driver
circuit
V_{CE}
V_X
Load


i_b
V_{CE}
12V
Pot. of
Y
t_d
t_r
t_s
t_f

⇒ Sense V_{CE} during conduction.

⇒ V_{CE} drops to $V_X - V_{D1}$=Pot. of Y, after T_{ON}.

If pot. of Y ↑ above this limit during conduction period

→ Overload condition.

⇒ Withdraw +ve base drive & supply $-I_B$

⇒ Signals are apllied w.r.t emitter.

Pot. of emitter Pot. of collector, when ON.

When it is OFF = 0.

⇒ Reference point is floating.

Power MOSFET:

(1978 : 100V, 25A power MOSFET)

MOSFET : [200V, 500A – SEMIKRON],

[60V, 1000A - SEMIKRON]

⇒ Generally low V, high I devices

⇒ Very popular in DC-DC conversion.

⇒ Metal – Oxide – Semiconductor Field Effect Transistor

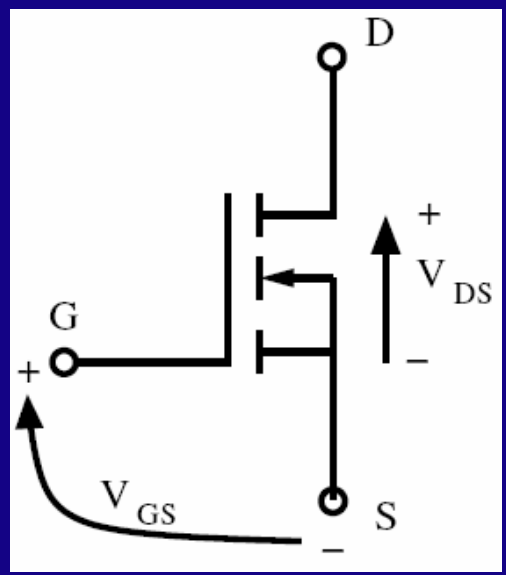
⇒ Fast device

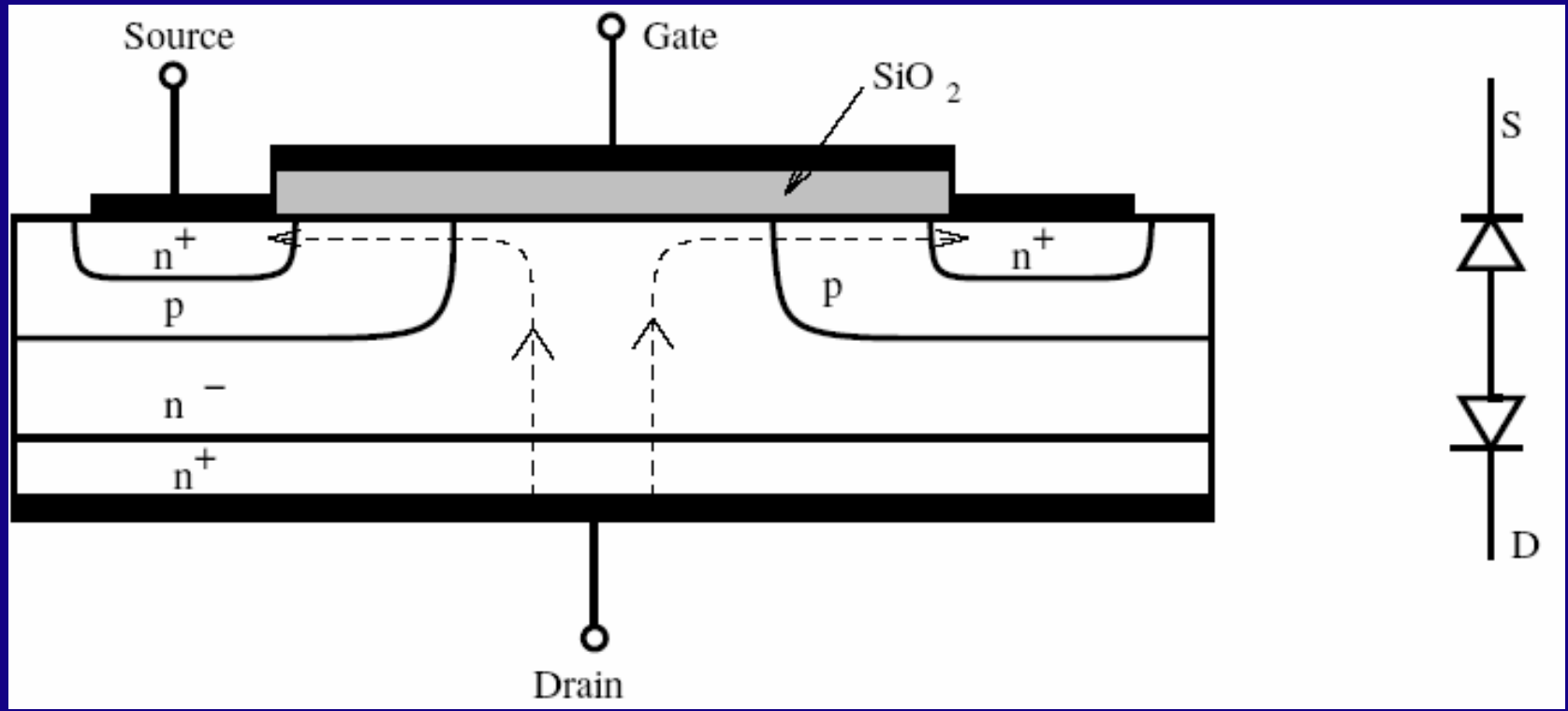
⇒ Majority carrier device

⇒ Unipolar device

⇒ Non-latching device

D → Drain G → Gate S → Source





Appears as though there cannot be any I flow between D & S.

Gate is insulated from the rest of the device

⇒ No steady I

⇒ Only displacement current (like in a parallel plate capacitor).

MOSFET is in cut-off when V_{GS} < threshold value.

When V_{GS} > threshold value,

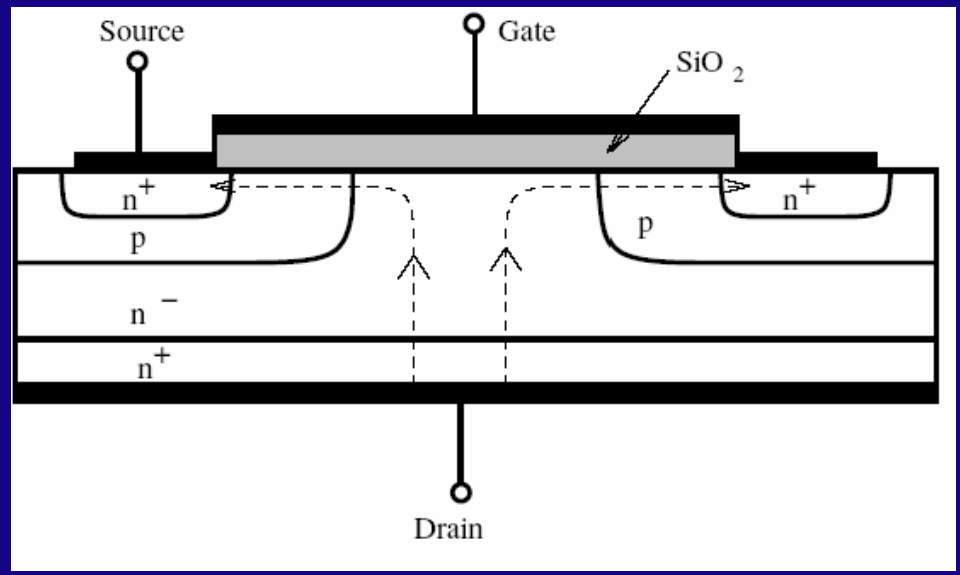
⇒ Converts silicon surface below the gate into an N-type channel

⇒ Connects source to drain

⇒ I starts flowing.

⇒ Threshold value V_{TH} depends on thickness of oxide layer

⇒ V_{TH} can be reduced by ↓ the thickness



⇒ when $V_{GS} > V_{GS(Th)}$;

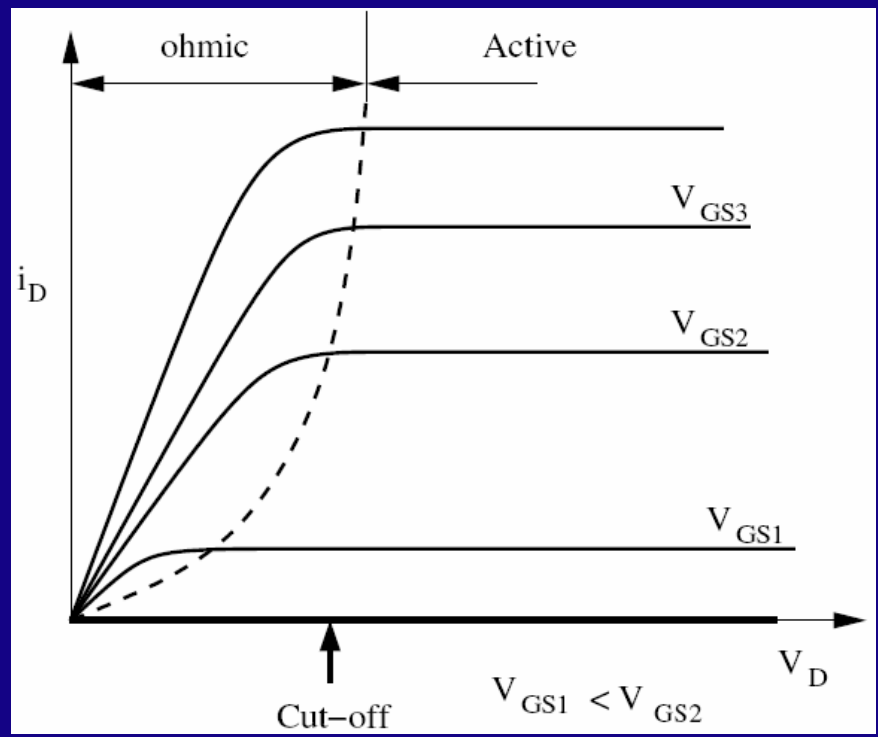
⇒ Device is driven into ohmic region

$V_{GS} - V_{GS(Th)} > V_{DS} > 0$

⇒ Power loss is low

⇒ In the active region, I_D depends only on V_{GS}

; Current is said to have saturated (saturation region).



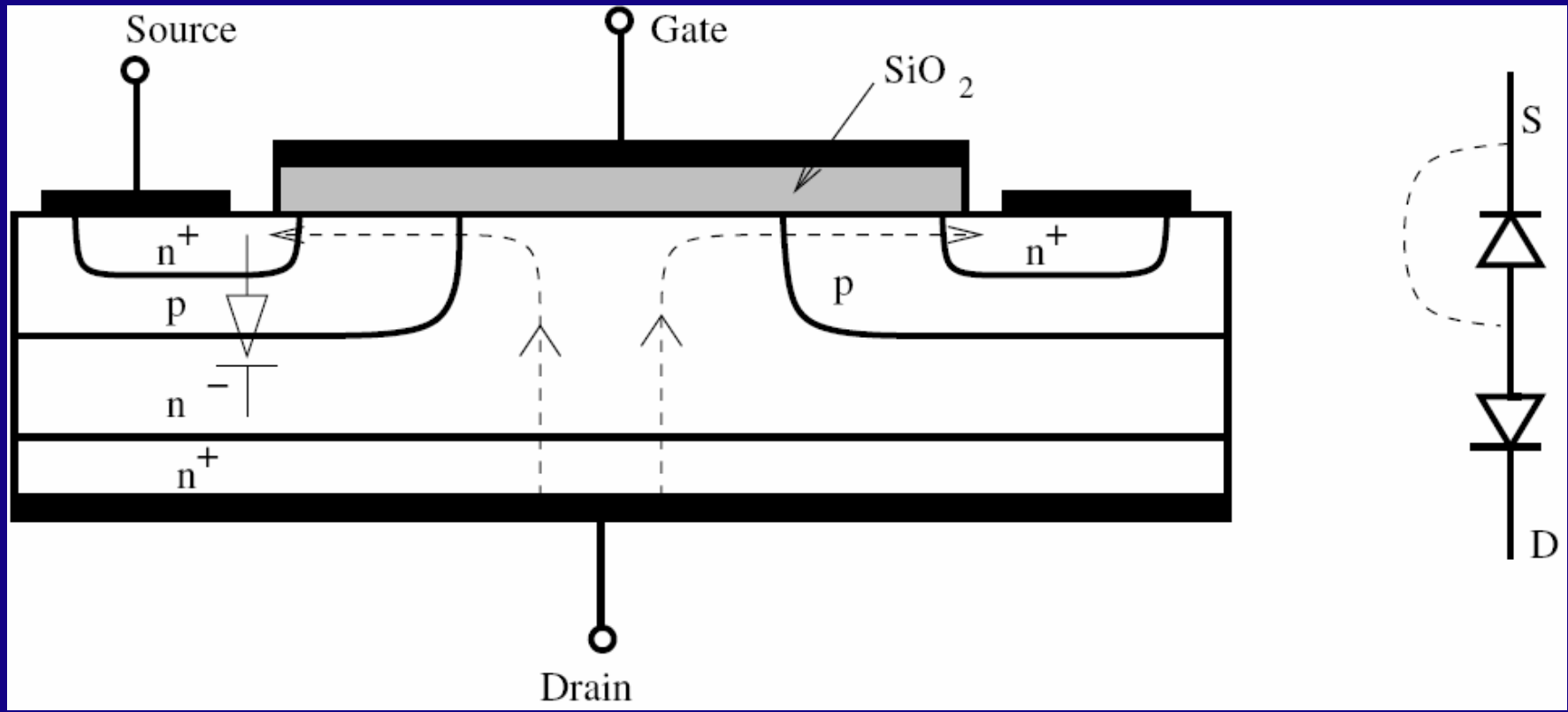
In ON state the 'channel' of the device behaves like a resistance $R_{DS(ON)}$

$$R_{DS(ON)} = \left.\frac{\partial V_{DS}}{\partial i_D}\right|_{V_{GS\ (constant)}}$$

$\Rightarrow$ Conduction power loss= $I_D^2\ R_{DS(ON)}$

BJT requires a base current for I_C to flow

$\Rightarrow$ BJT has substantially lower voltage drop than MOSFET


Source
Gate
SiO 2
n+
p
n−
n+
n+
p
Drain
S
D

Internal Body Diode

Has a internal Body Diode

Connected between source & drain

→ MOS can block +ve 'V'

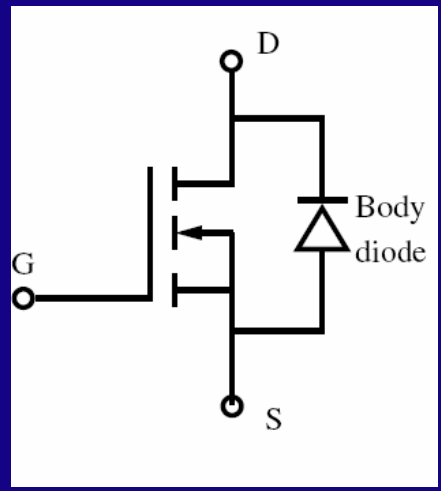
(junction P-N^- determines this V)

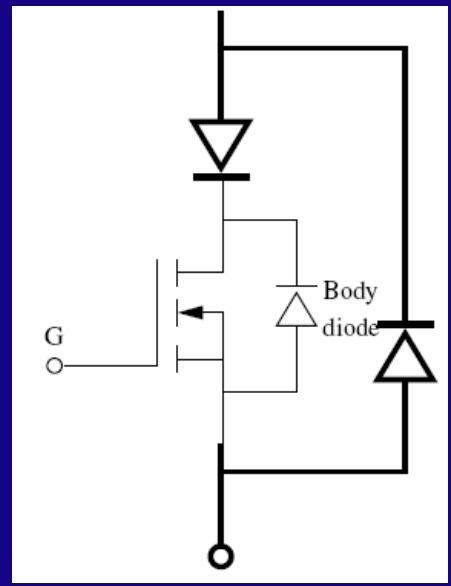
→ 'i' can be either +ve or -ve.

→ -ve I through diode

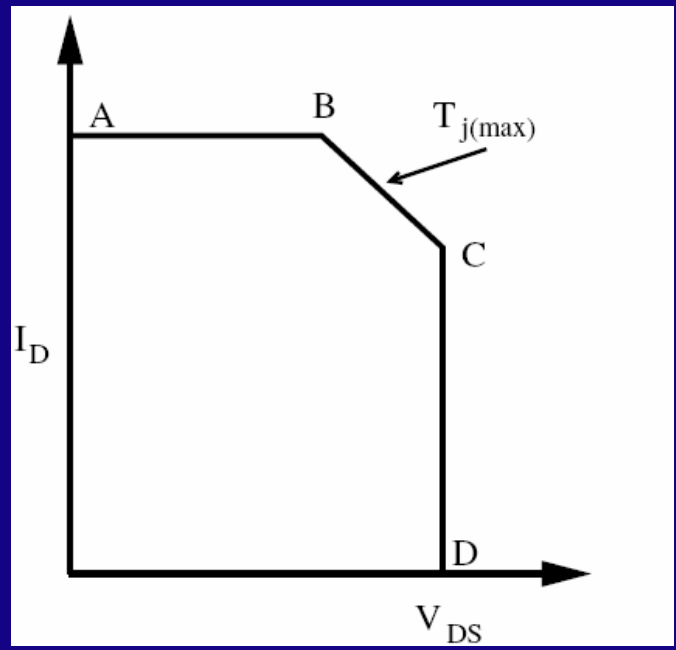
→ This diode has adequate I & switching speed rating

→ Some applications require fast diode





Safe Operating Area



No secondary breakdown region

SOA is limited by

AB-maximum drain I at steady state

CD-Maximum V_{DS} that the device can sustain

BC-Maximum power dissipation

⇒ Imposed by $R_{DS(ON)}$

⇒ Has +ve resistance coefficient.

⇒ Paralleling is easy

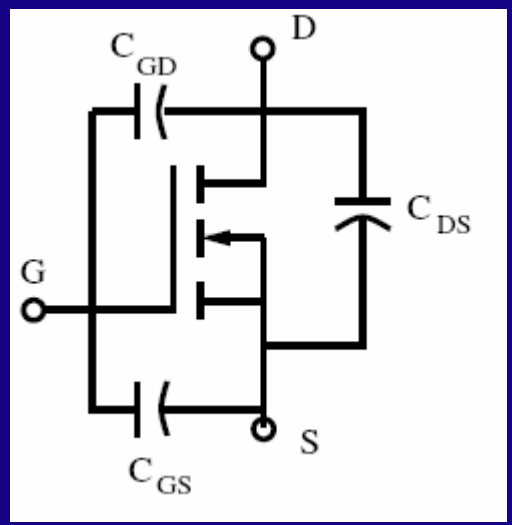
Internal Capacitor (Parasitic capacitance)

$\Rightarrow$ limits the switching speed

3 types

C_{GS} $\rightarrow$ Dielectric is the oxide layer isolating G & source

Almost independent of variation in V_{DS}



Gate – Drain capacitance : (C_{GD})

Varies considerably with V_{DS}

$\Rightarrow$; C_{GS} when V_{DS} is low

$\Rightarrow$ Negligible when V_{DS} is high

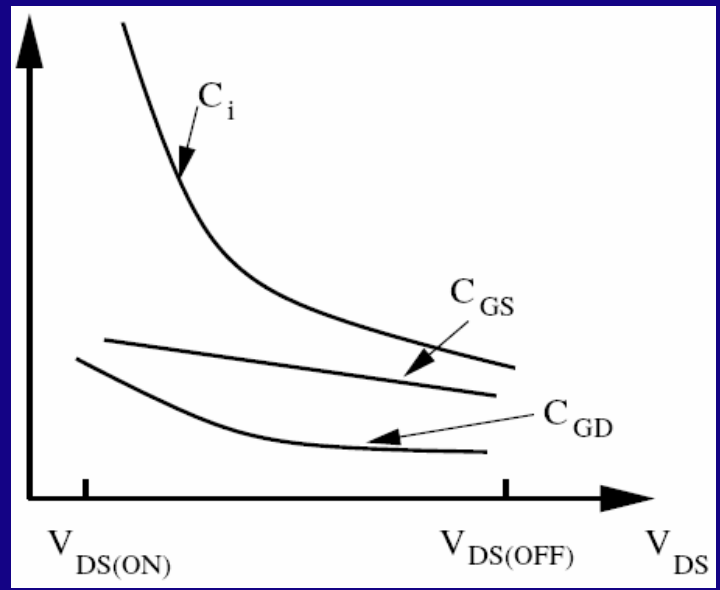
$\Rightarrow C_{DS} \rightarrow$ Less important

$\Rightarrow C_{GD} + C_{GS} \rightarrow C_i$

$\Rightarrow C_i \rightarrow$ Input capacitance

in pico Farads

$\Rightarrow$ During turn-ON, C_{GD} & C_{GS} must be charged through gate



Review :

1) Power MOSFET

Metal Oxide Semiconductor Field Effect Transistor

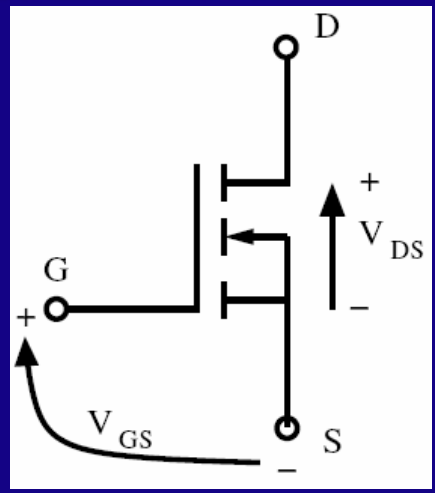
⇒ Fast Device

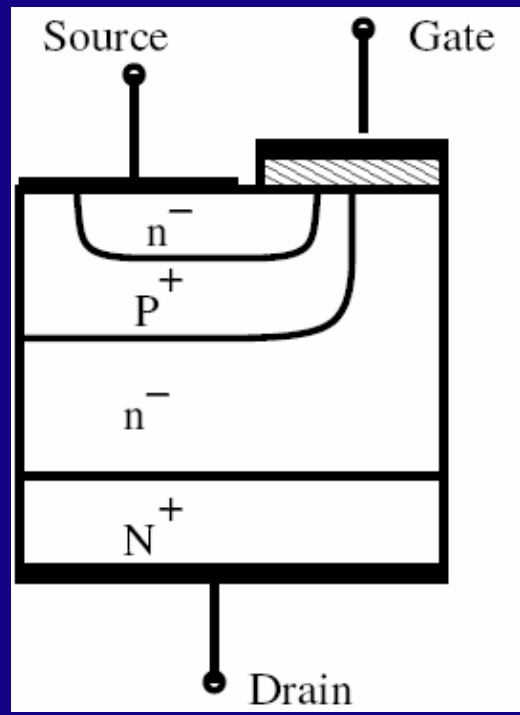
⇒ Gate is insulated from source

⇒ Input I ; 0

⇒ Input Z → ∞ ; it is capacitive.

⇒ If $V_{GS} > V_{TH}$, a n channel is formed, which connects drain and source.



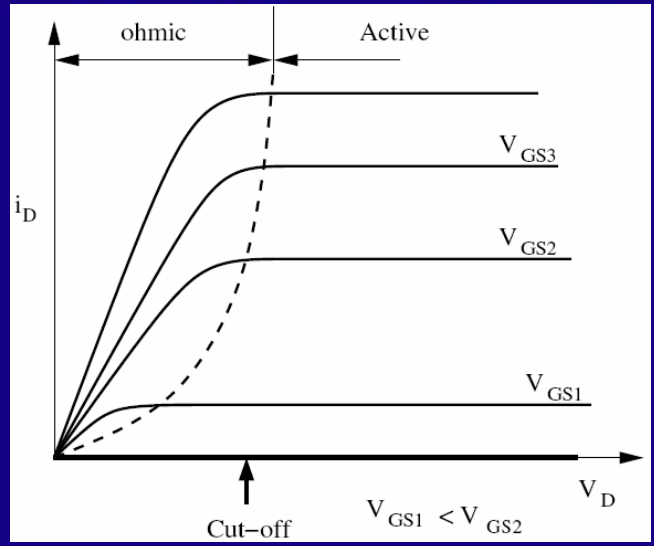


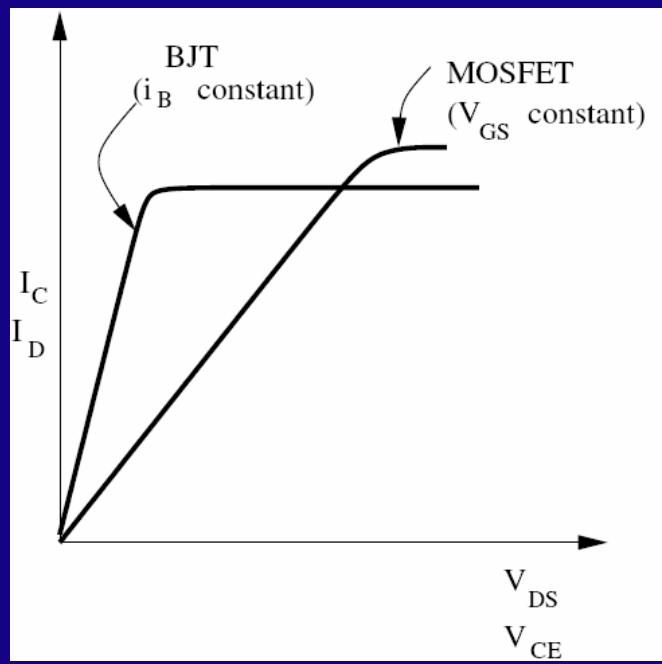
V-I characterisitcs

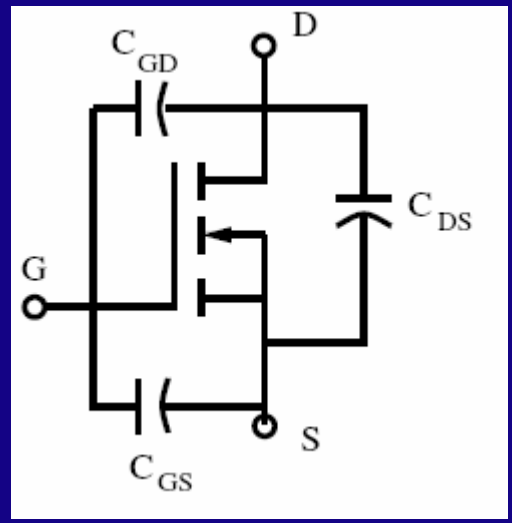
⇒ **In ohmic region MOS can be represented by Resistance (R_{DS})**

⇒ **BJT has substantially lower voltage drop than MOSFET.**

⇒ **One of the drawbacks of MOSFET.**







⇒ Input $C_i = C_{GD} + C_{GS}$

$C_{GD} \rightarrow$ varies with V_{DS}

C_{GD} ; C_{GS} when $V_{DS} = V_{DS(ON)}$

C_{GD} is very low when V_{DS} is high

$C_{GS} \rightarrow$ almost independent of V_{DS}

⇒ majority carrier device.

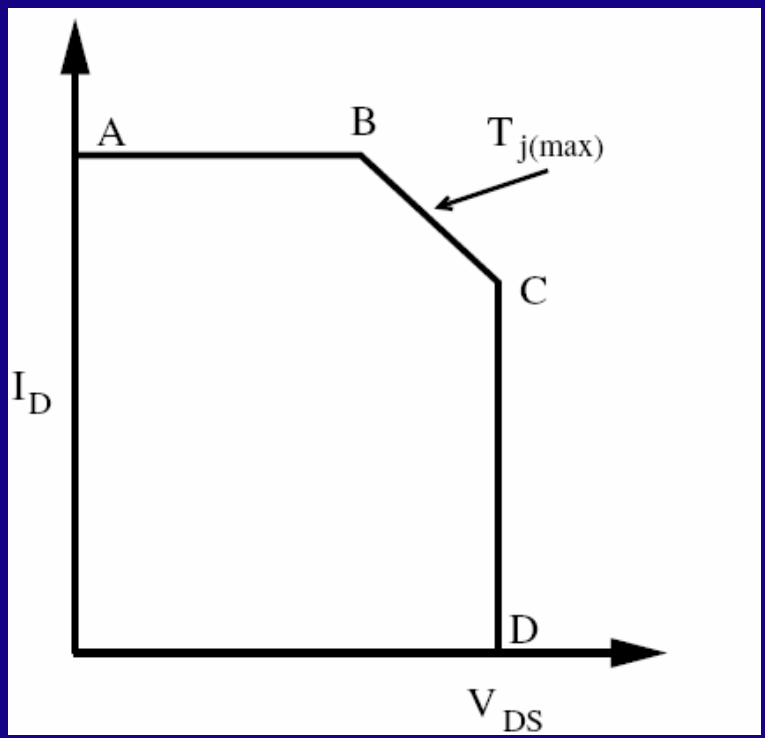
⇒ +ve temperature coefficient

⇒ paralleling is easy

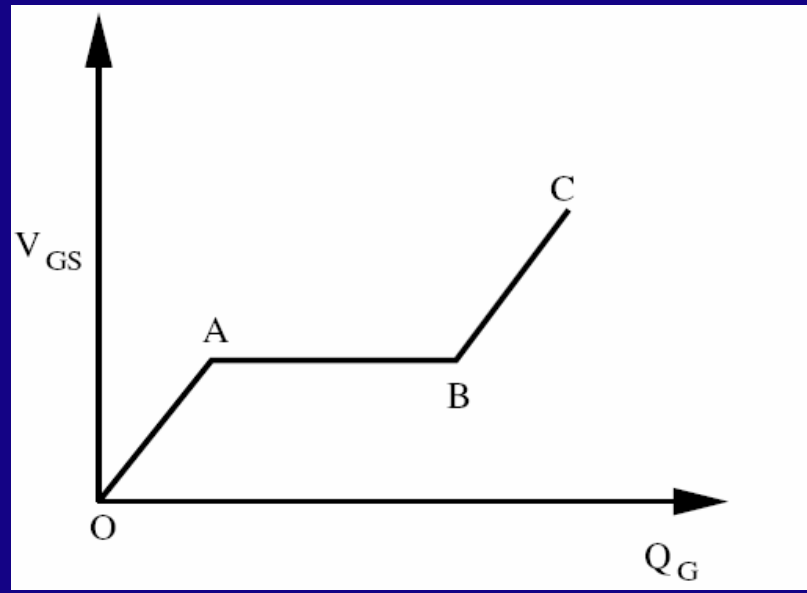
SOA has

→ I_D limit, V_{DS} limit.

→ Max. power dissipation limits.



Increase in V_{GS} as a function of charge carried to the Gate:



$Q_G \rightarrow$ Charge carried to the gate by current i_G during turn-ON

$OA \rightarrow$ Corresponding to the charging of C_i under full V_{DS}

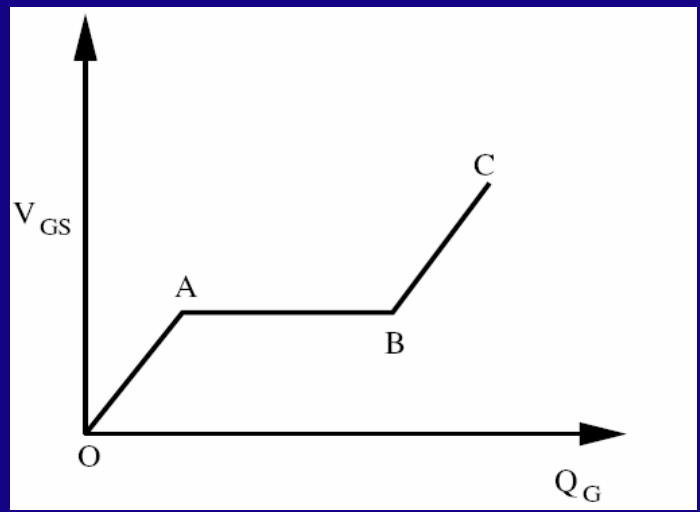
C_i ; C_{GS}

$\rightarrow$ Charge supplied depends on drain I .

AB $\rightarrow$ Corresponds to V_{DS} decrease from the supply voltage to $V_{DS(ON)}$. V_{GS} remains constant. Charge supplied is used to vary the 'V' across C_{GD}.

BC $\rightarrow$ Corresponds to input capacitance charge when the device is ON

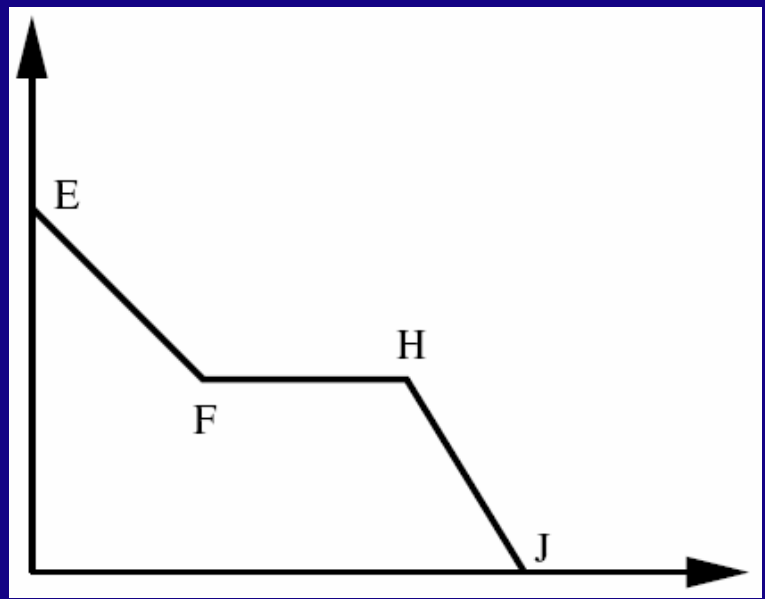
$C_i = C_{Gs} + C_{GD(ON)}$



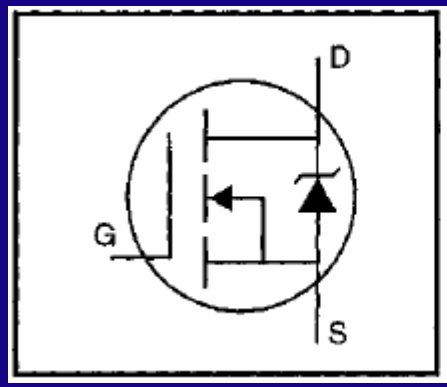
During turn-OFF

Removal of excess charge (EF), discharge of C_{GD} during voltage rise (FH), &

C_{GS} discharge during current fall (HJ).



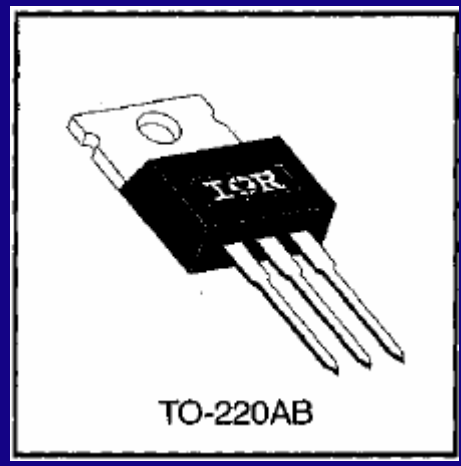
IRF640



$V_{DSS} = 200V$

$R_{DS(on)} = 0.18\Omega$

$I_D = 18A$



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	18	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	11	
V_{GS}	Gate-to-Source Voltage	±20	V

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS}=0V, I_D= 250μA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	V_{GS}=10V, I_D=11A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
Q_{gs}	Gate-to-Source Charge	—	—	13	nC	V_{DS}=160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	39		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD}=100V
t_r	Rise Time	—	51	—		I_D=18A
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		R_G=9.1Ω
t_f	Fall Time	—	36	—		R_D=5.4Ω See Figure 10 ④

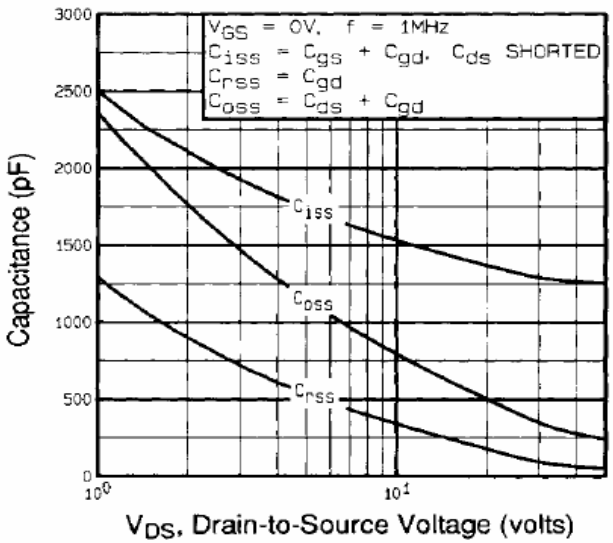


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

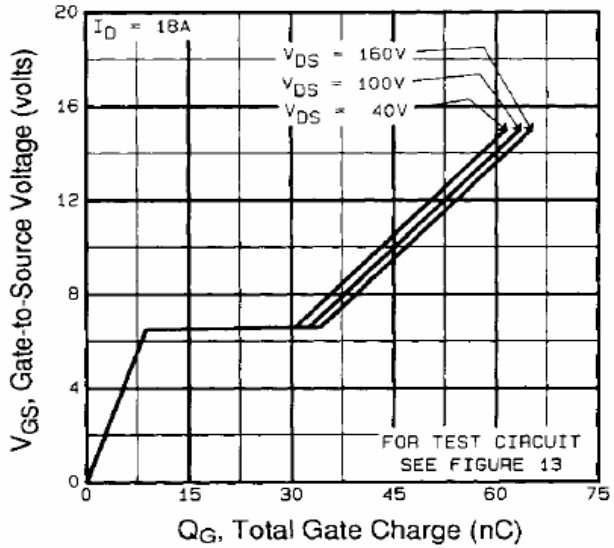
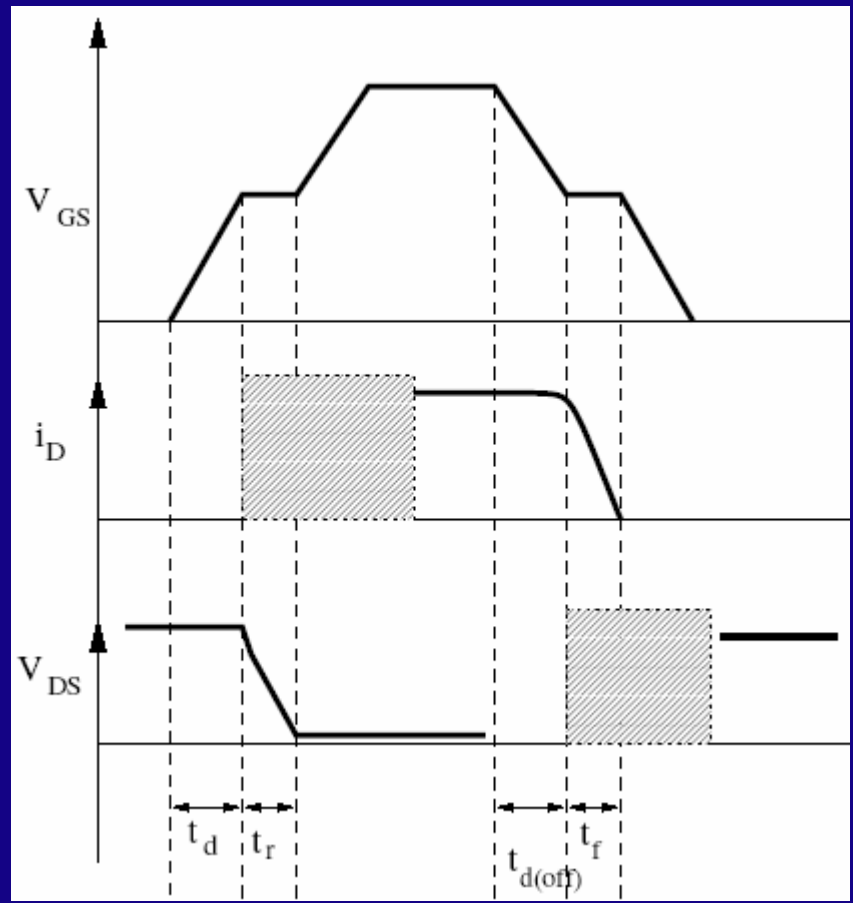


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

Switching characteristics :

$t_d \rightarrow$ time required to charge C_{GS} to V_{Th}

$t_r \rightarrow$ Charging time to drive the gate for full conduction of the device



Rise in i_D with time (hatched area) is decided by internal circuit

$t_{d(off)} \rightarrow$ Time required for the gate to discharge from the overdriven voltage to the threshold voltage corresponding to active region.

$t_f \rightarrow$ Time required for the gate voltage to move through the active region before entering cut-off.

Difference between BJT & MOSFET

BJT	MOSFET
1) Current controlled device	1) Voltage controlled device
2) Minority carrier device ∴ has -ve resistance co-efficient.	2) Majority carrier device has +ve resistance co-efficient.
3) Has secondary breakdown	3) No secondary breakdown
4) Paralleling device is difficult	4) Easy
5) On state power loss ($V_{CS(sat)} I_c$) is low	5) $I_D^2 R_{DS(ON)}$ is higher than on state losses of BJT
6) Turn-off time is higher	6) Very fast device

COOLMOS: On state resistance is low.

∴ conduction losses are low.

IGBT (1983-by Jayant Baliga)

(Insulated Gate Bipolar Transistor)

⇒ Prior to advent of IGBT,

⇒ BJTs & MOSFET were used in high frequency application

⇒ BJT has excellent on-state characteristics

⇒ Current controlled device

MOSFET : – Requires very small gate current.

Is it possible to use both?

$\Rightarrow$ BJT & MOSFET have charcteristics that compliment each other is some respects.

IGBT $\Rightarrow$ Insulated gate $\rightarrow$ similar to MOS

$\rightarrow$ control stage

BJT $\Rightarrow$ Power stage

Modify the structure

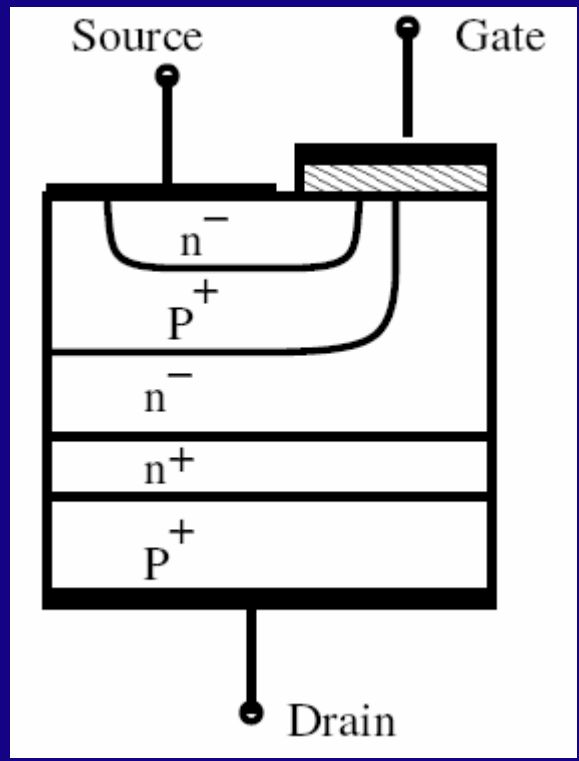
P^+ layer forms the drain.

When +ve potential applied to the gate & exceeds threshold voltage

n channel is formed $\rightarrow$ similar to MOS

$\Rightarrow$ Electron flow into N^- region

N^- layer receives electrons from source (N^+) & holes from drain (P^+)



If P^+ N^+ (J_1) junction is forward biased

holes are injected into the n^- region

$\Rightarrow$ Some electrons recombine with holes

$\Rightarrow$ Remaining holes are collected at source

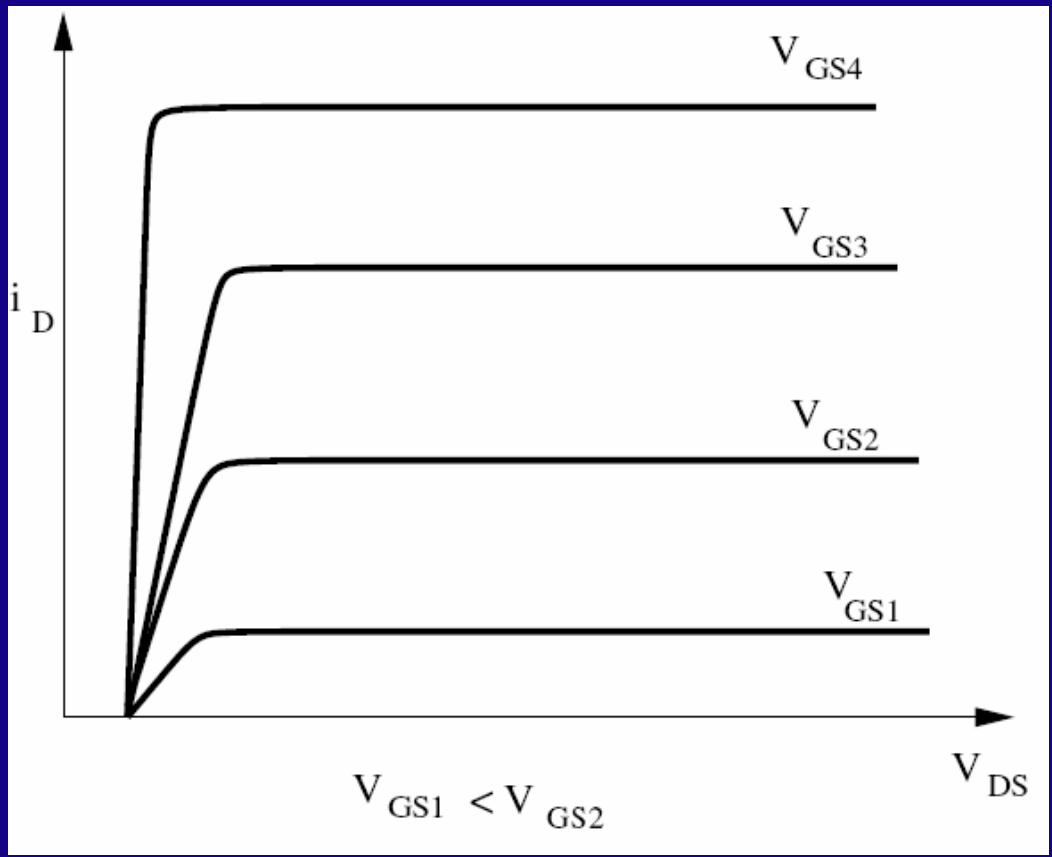
$\Rightarrow$ J_1 can now block -ve V.

In comparison to MOSFET, IGBT has no inverse body diode.

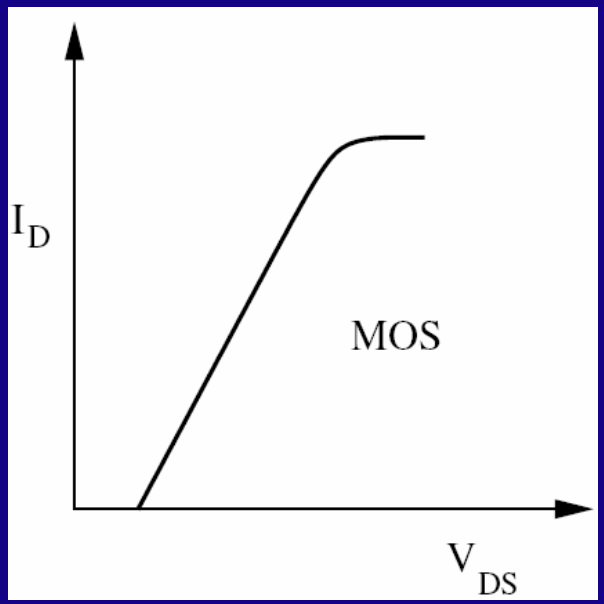
⇒ Most IGBTs contain inverse diode

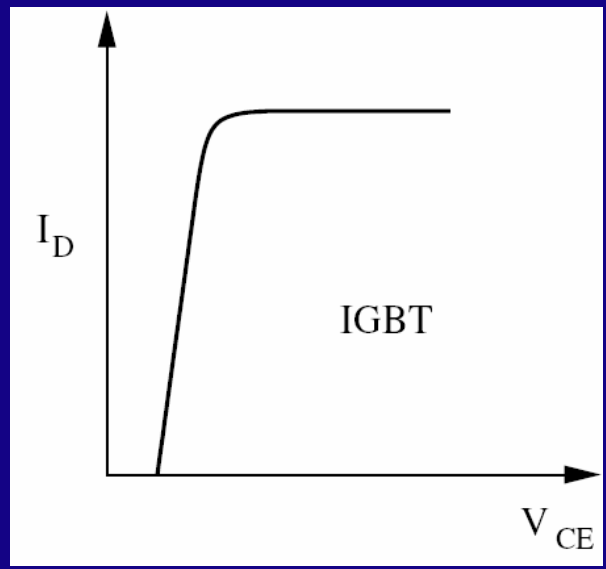
⇒ Built-in which is optimized to match the IGBT switching operation.

V-I charcteristics look similar to BJT except control parameter is V_{GS}



During conduction, R_{DS} is lower.





⇒ N^+ layer between P^+ (drain) N^- drift layer is not essential for operation of IGBT

⇒ Some have just $\underline{N^-}$ layer

⇒ Non punch through (NPT) IGBT

If both are present, is known as punch through IGBT (PT-IGBT)

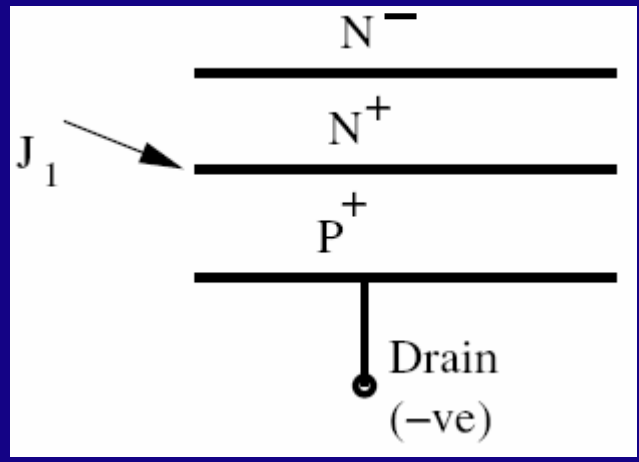
When reverse voltage is applied J_1 should block -ve

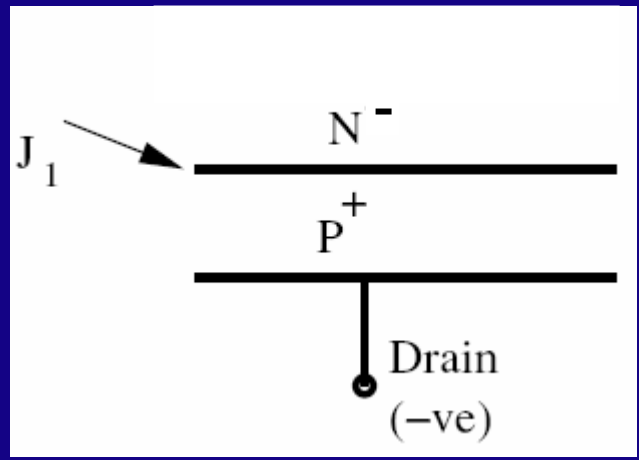
Due to heavy doping on both sides this V ↓

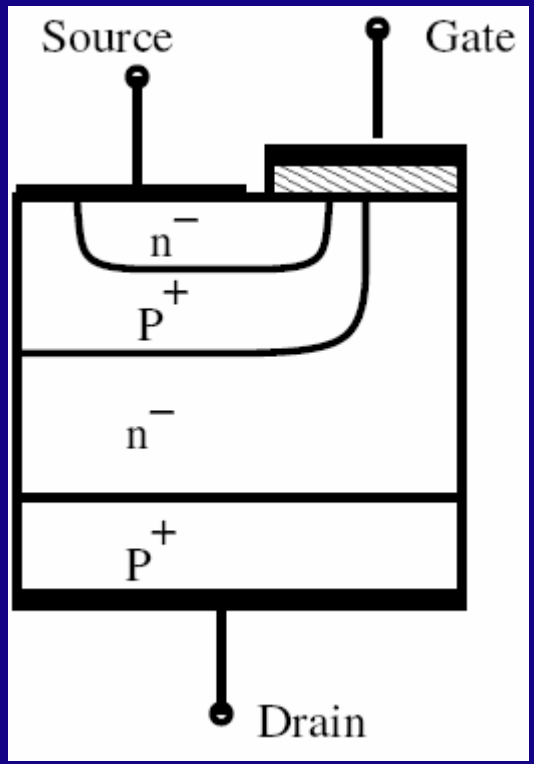
⇒ PT IGBT has low -ve V blocking capability (Non-symmetrical IGBT)

⇒ Non-punch through IGBT

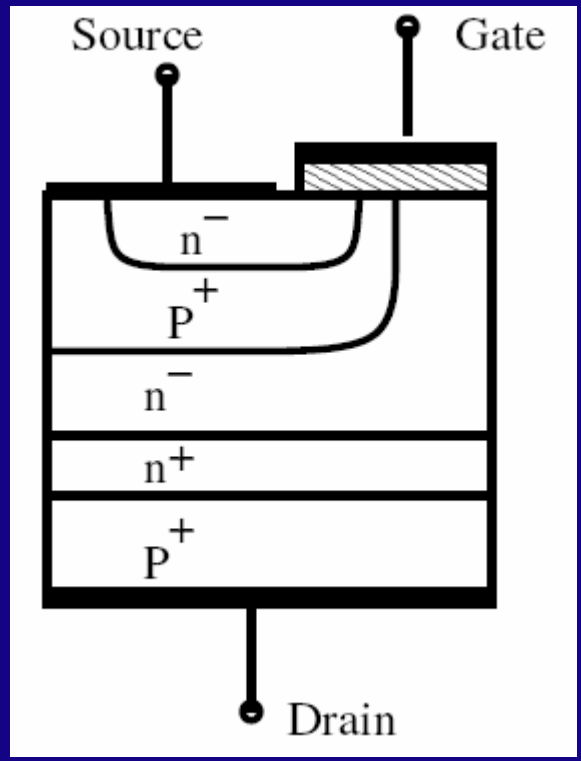
→ symmetrical IGBT







NPT



PT

Turn – ON of IGBT is ; same as that of power MOS

Turn-off :-

There are two distinct time interval during turn off:

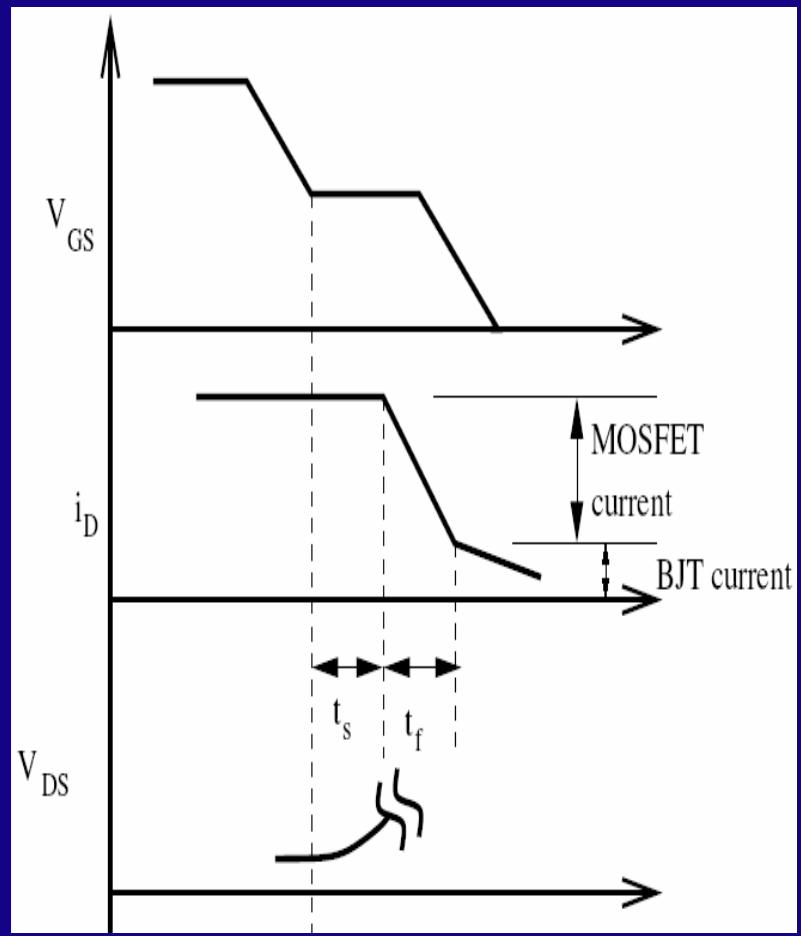
1) The channel disappears & MOSFET blocks quickly

$\Rightarrow i_D$ drops

$\Rightarrow$ Minority carriers in N^- layer gradually recombine.

$i_D \downarrow$ relatively slowly

(Tail current)



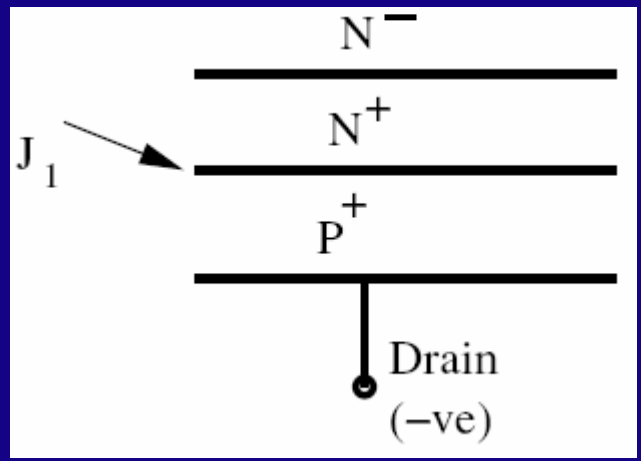
This period should be small since V_{DS} has attained reasonably a high value

$\Rightarrow$ Losses high

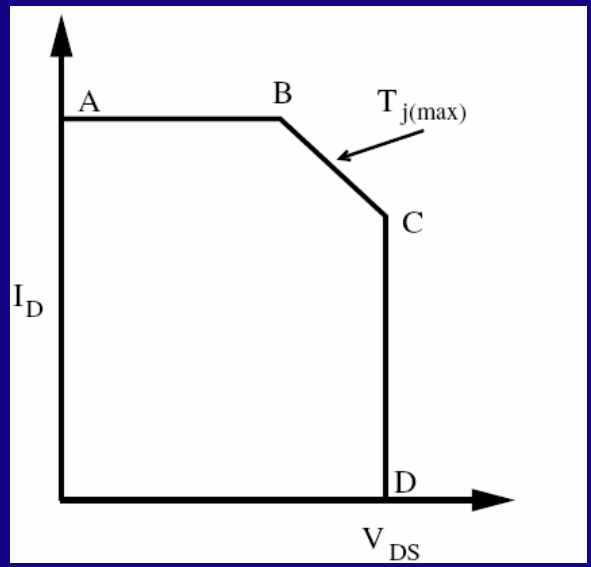
$\Rightarrow$ Punch through IGBT has smaller tail time

$\Rightarrow$ Has N^+ layer

(Almost similar to N^+ layer in GTO anode short structure)



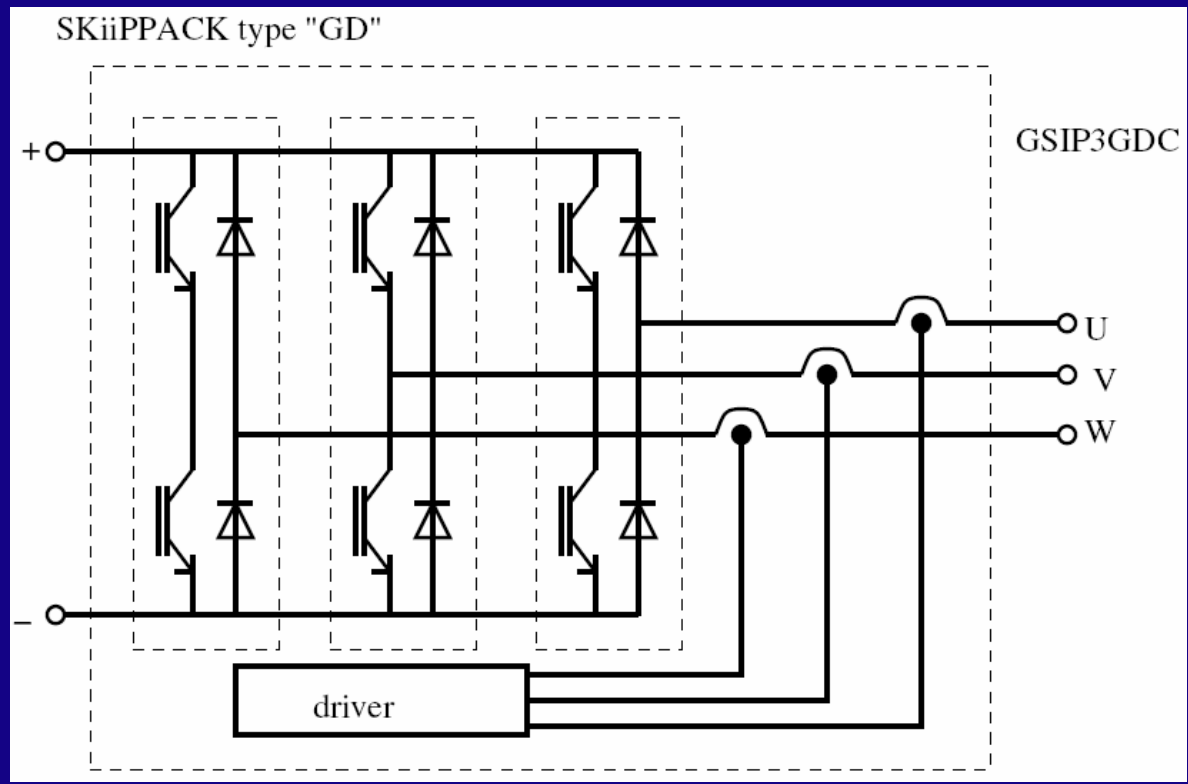
SOA of IGBT

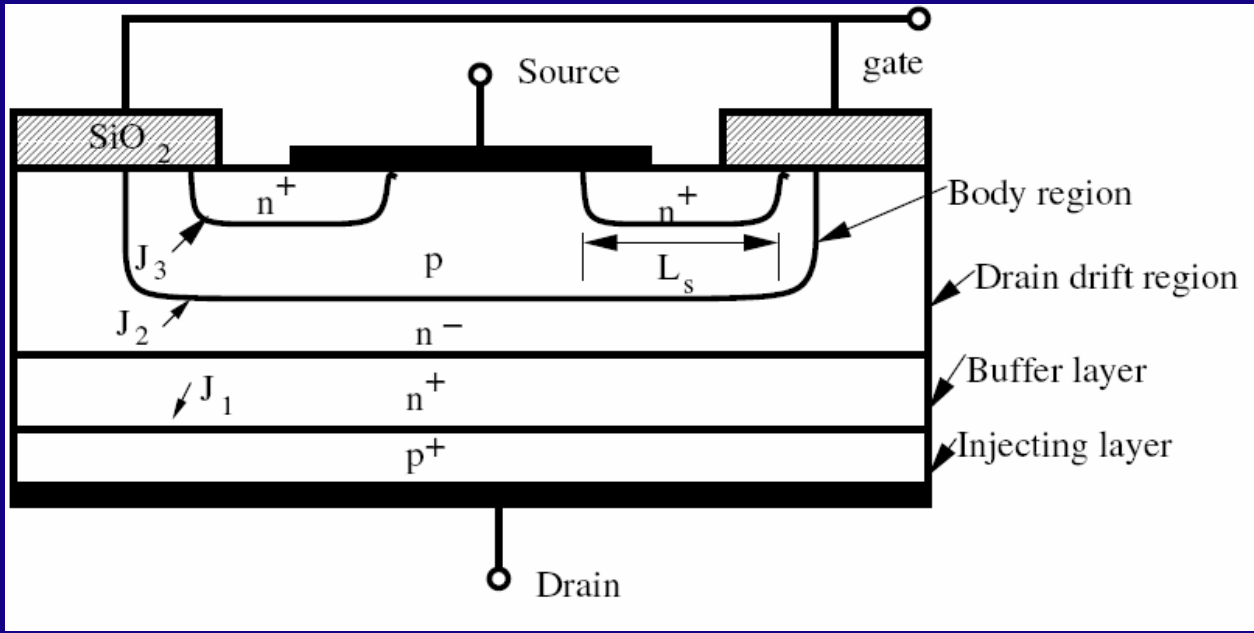


Smart Power Module:

⇒ **Power module + Driver circuit + Protection circuit**

- **Over temperature protection**
- **Over current protection**
- **Over voltage protection**




Source
gate
SiO 2
n+
n+
Body region
J 3
p
L s
Drain drift region
J 2
n −
J 1
n+
Buffer layer
p+
Injecting layer
Drain