Design of MOSFET Differential Amplifiers

Wadhwani Electronics Lab

Department of Electrical Engineering
Indian Institute of Technology Bombay
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Aim

* In this experiment,we wish to design and test Simple Current Mirror.
* We will also design and test MOSFET Differential Amplifiers with resistive and active loads.(Using ALD1106 and ALD1107).
* This experiment mainly aims at understanding the internal working of OPAMP.

Simple Current Mirror

Current sources are extensively designed and used to bias different kinds of circuits. An ideal current source supplies a constant current irrespective of the voltage supplied across it. In this experiment, we study two such current sources which are designed using MOSFETs.

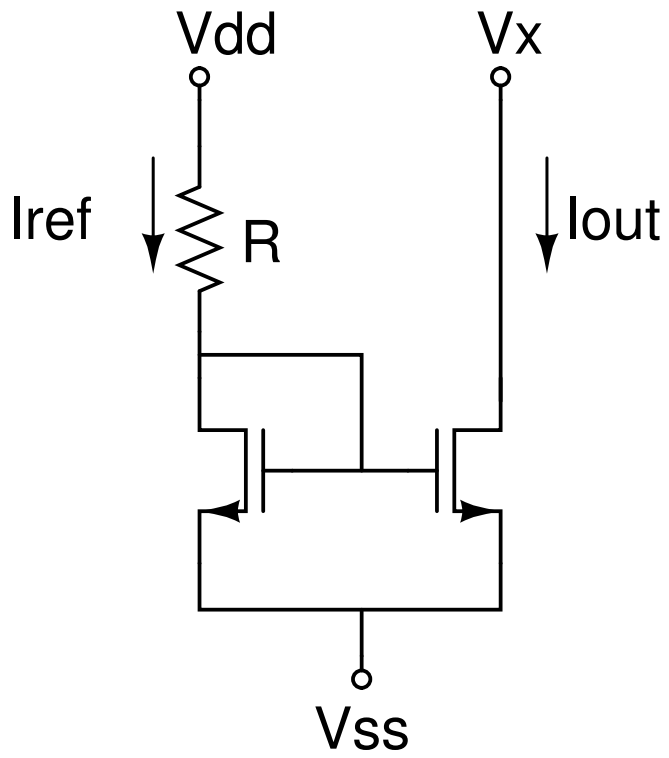

Figure: 2

Theory and Design Procedure

Figure 1 shows a Differential Amplifier which you have already studied in class.Analyse the circuit and find the expression for gain.Write the derivation of gain in postlab report.

Theory and Design Procedure

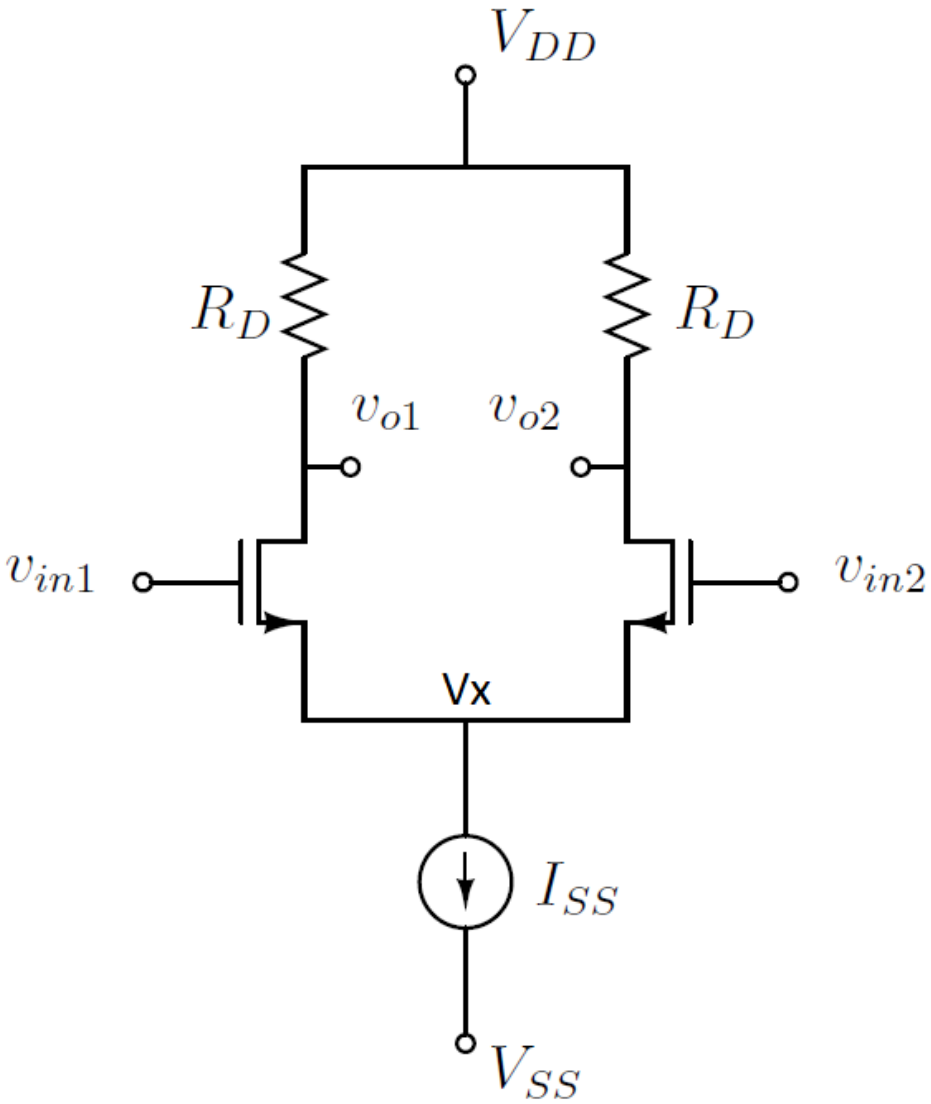

Figure 1: Simple MOSFET Differential Amplifier

Theory and Design Procedure

Small signal model of the above circuit is as follows:

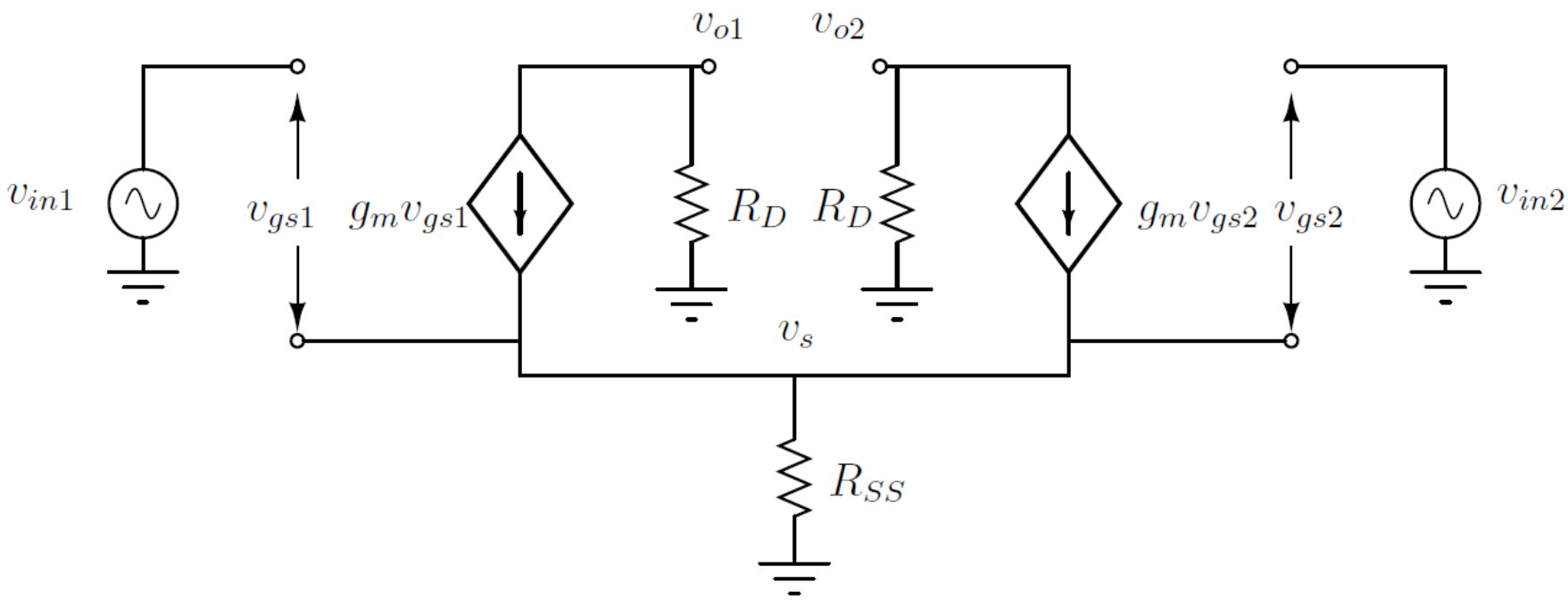

Figure 3: Small signal model of MOS Differential Amplifier

Theory and Design Procedure

Suppose we wish to design a differential amplifier as in Figure 1, with a gain of 5, given supply voltages of 3.3V and $-3.3V$.
Let us assume $I_D = 0.4mA$ through each transistor, which gives
$V_{GS} - V_{TN} = 1.24V$.
Substituting in Equation 8, we obtain $R_D = 7.76$ k.
Since the drain current for each transistor is 0.4 mA, we need a biasing current source $I_{SS} = 0.8mA$.
Read "Microelectronic Circuits" by Sedra and Smith for more information.

Pre Lab Work

1. Read up on differential amplifiers. Familiarize yourself with the terms "Common Mode Gain" and common mode rejection ratio (CMRR).

2. Similar to the way we derived the differential small signal gain expression, derive the expression for common mode gain.(Hint: You may have to assume that there is a slight mismatch between the transistors, and also the two drain resistors- say R_D and $R_D+\Delta R$)

3. Design the circuits to be used in each of the three parts of the experiment.

4. Simulate your designs in SPICE.

Part 1- Simple MOSFET Differential Amplifier

In this part, we will use the same circuit as shown in Figure 1. Instead of current source, use current mirror as given in Figure 2 (Precaution: Set the supply voltages properly before connecting them to the circuit. The maximum supply the device can tolerate is roughly $-5.5V$ - 5.5V)

1. Assemble the circuit, to get I_{out} of 1mA. Calculate the value of Kn or Kp with the help of the values tabulated in the datasheet.

2. For supply voltages $V_{DD} = 4.5V$ and $V_{SS} = -4.5V$, find the value of R_D required for a gain of 7. Will the output voltage swing be symmetric?

3. Wire up your circuit and apply a 50 mV peak, 1 kHz sine wave to (i) v_{in1} and (ii) v_{in2}.While applying a signal to one input, keep the other input grounded. Ensure that there is no distortion in the output. Measure the differential voltage gain A_d in each case. (How will you observe differential signals on the CRO?)

4. Find out the maximum symmetrical output swing of your circuit at 1 kHz.

Part 1- Simple MOSFET Differential Amplifier

5 Repeat step 3 for frequencies 10 kHz, 100 kHz and 500 kHz and 1 MHz.

6 Now short both the input terminals and apply a common-mode signal. Measure the common- mode voltage gain Ac at the above frequencies. Calculate the CMRR (in dB) for each frequency.

7 Measure the input offset voltage of your differential amplifier (you may neglect the effects of input bias current).

8 Compare your results (differential gain, CMRR, offset voltage) with two other groups and tabulate them.

Part 2-Differential Amplifier with Active Load

We will now replace the two drain resistors R_D in Figure 1 by a PMOS current mirror, as in Figure 4, and take a single-ended output.

Why do we use this configuration over resistive load?,Mention reasons in postlab report.

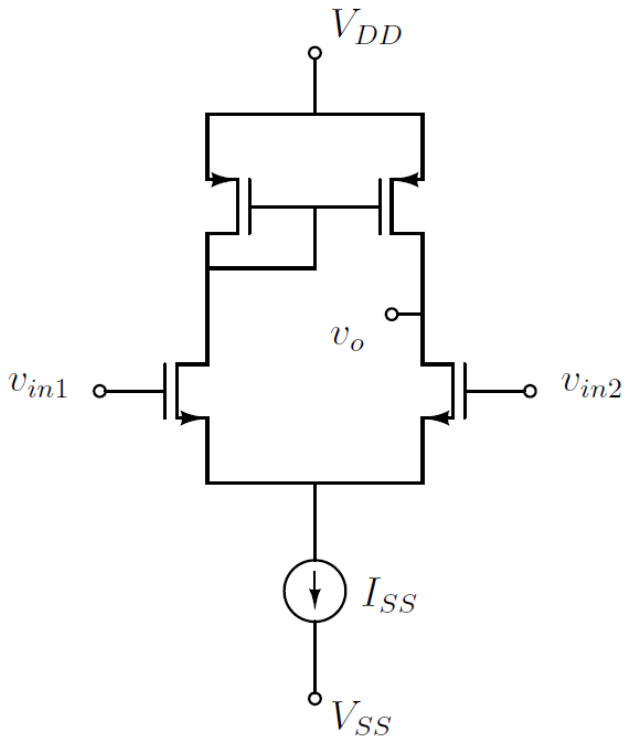

Figure 4 : Differential Amplifier with Active Load

Part 2-Differential Amplifier with Active Load

1. Use supply voltages $V_{DD} = 4.5V$ and $V_{SS} = -4.5V$,find the expression for gain, find the value of I_{SS} required for a gain of 50. (Hint: This time, the drain-source resistance r_o of the transistors need to be considered.Given the channel length modulation parameter λ for the NMOS and PMOS are approximately 0.036).

2. Use an appropriately designed current mirror for I_{SS}.(Keep the value of I_{SS} less than 100uA).

3. You may have to vary the potentiometer in current mirror to adjust the I_{SS} which in turn adjusts the gain of the amplifier.

4. Wire up your circuit and apply a 20 mV peak, 1 kHz sine wave to (i) v_{in1} and (ii) v_{in2}. Measure A_d in each case.

Part 3-Differential Amplifier with Active Load

5. Draw the small signal model of above circuit in postlab report.

6. Report the dependence of Gain on I_{SS}.Mention all the challenges you face in designing and explain why?.

7. Find out the maximum symmetrical output swing of your circuit at 1 kHz.

8. Repeat step 3 for frequencies 10 kHz, 100 kHz and 500 kHz and 1 MHz.

9. Measure the common-mode voltage gain Ac and the CMRR (in dB) at the above frequencies.

10. Measure the input offset voltage of your differential amplifier.

11. Compare your results with two other groups and tabulate them.