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Design of a flexible analog signal conditioning circuit for DSP-based systems

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Abstract

This paper presents the design of a flexible analog signal conditioning circuit (SCC) able to be reconfigured depending on user requirements. The SCC can be employed with DSP-based systems. The design is aimed to be used in power electronics applications where a wide range of signals types are present. In order to guarantee reconfiguration, the design is constituted of interconnected stages that can be activated depending on the characteristics of the input signal. The proposed circuit is a simple and a low cost solution because it employs off-the-shelf components.

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Keywords: measurement instrumentation, signal conditioning, power measurement

1. Introduction

The obtaining of information on power electronics applications, such as DC/DC converters, inverters, active filters, among many others [1]-[6] in order to monitor and control them has been representing a permanent concern of engineers. Voltage and current signals provided by power electronics systems have to be adapted to the analog-to-digital converter (ADC) range of data acquisition boards, digital signal processors (DSP), field programmable gate arrays (FPGA) or microcontrollers. The ADCs are used for the digitalizing of the conditioned signals. Usually, the ADCs of DSPs, FPGAs or microcontrollers are powered by low voltages (3.3V), if the measured signal exceeds this value, it must be conditioned.

Even if signal conditioning circuits are an essential stage in the measurement system, usually less attention is paid to them and often, they suffer of low design effort. Processes involved in signal conditioning highly depend on the application. Typical processes include galvanic isolation, impedance transformation, level translation and amplification, and linearization among others.

Amplification and filtering stages can be performed in commercial boards available today [7], [8]. Nevertheless, these boards does not have attenuation, DC level shift or isolation.

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In this paper, a multipurpose and reconfigurable SCC that can be connected either to an ADC of a DSP or FPGA is presented. In the design of the proposed reconfigurable circuit, a low-power consumption, low component count, and low cost requirements have been taken into consideration. The SCC is constituted of interconnected stages that include attenuation, isolation, low-pass filtering (LPF), DC level shift and voltage limitation. The advantages of this SCC in comparison with other circuits proposed in the literature [9], [10], [11] are: a high compatibility with different types of ADC, reconfigurable architecture, easy implementation, low-power consumption, low component count and low cost.

This paper is organized as follows. Section 2 presents the description, design specifications and requirements of every stage of the proposed SCC. Section 3 presents the circuit implementation and shows experimental evidence of the circuit performance. Finally in Section 4, some concluding remarks are presented.

2. Description and operation

In Fig. 1 the block diagram of the proposed signal conditioning circuit is shown. The design consists of five stages: i) attenuation, ii) isolation, iii) antialiasing filter, iv) DC level shift and v) voltage limitation. Usually, the analog inputs to be converted do not belong to the input range of the ADC. The attenuator is in charge to reduce the amplitude of the input signal. The isolator provides protection to the electronic circuits in case of transients or ground loops (when passive resistive elements such a shunt resistors are used). The antialiasing filter prevents the aliasing by limiting the bandwidth, thus the signal can be properly sampled. Specifically, the DC level shift adequate AC signals (that have positive and negative voltage values) to be acquired by devices such as DSPs or FPGAs. Finally, the limiter prevents that over-voltages saturate the A/D converter.

Fig. 1. Block diagram of the signal conditioning circuit.

The proposed architecture of the circuit is shown in Fig. 2.

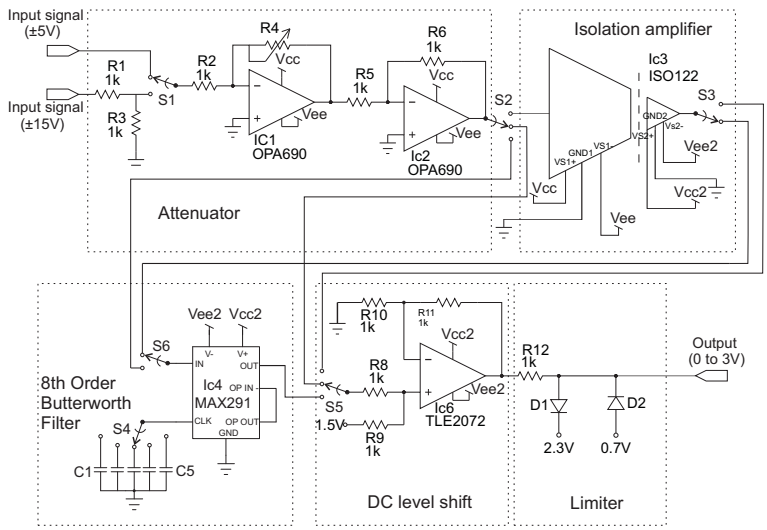

Fig. 2. Schematic diagram of the signal conditioning circuit.

2.1. Attenuator

For input voltages from 0–5V the attenuation is implemented using an inverter amplifier, as it can be seen from Fig. 2. Two possible attenuation scales can be selected using S1. For a scale of ±5V, the attenuation is given by:

$$G = -\frac{R_4}{R_3} \tag{1}$$

while for higher input signals (up to ±15V), a voltage divider with attenuation of 2 is added to the input of the inverter amplifier. Choosing $R_1 = R_2 = R_3$ the attenuation is given by:

$$G = -\frac{R_4}{3R_1} \tag{2}$$

2.2. Isolation amplifier

The output signal of the attenuator is galvanically isolated using an ISO122JP isolation amplifier (IA). The IA is supplied by two isolated DC/DC converters TEL 2-0521 (Traco Power) with input voltage range of 4.5–9V and output voltages of ±5V.

2.3. Antialiasing filter

To prevent aliasing, an 8th order low-pass Butterworth switched-capacitors filter is used. The cut-off frequency can be selected by an external capacitor. Its value is calculated according to:

$$C_{OSC}(pF) = \frac{10^5}{300 f_c(kHz)} \tag{3}$$

Five possible corner frequencies (5, 10, 15 25 and 50 kHz) can be selected via jumpers with five on board capacitors. According to [12] a cut-off frequency of 5 and 10 kHz allows sampling of electric power line signals to perform on-line voltage and current distortion analysis (harmonic and interharmonic). Cut-off frequencies of 15 and 25 kHz allow sampling signals from inverters. A cut-off frequency of 50 kHz allows adequate sampling of inductor currents from typical DC/DC converters.

2.4. DC level shift

The fourth stage is a DC level shifter. Any DSP imposes the analog input range of its ADC, (the recommended operation conditions are V_{in}= 0–3V [13]), typically:

$$0 \leq V_{in} \leq V_{DDA} \tag{4}$$

where V_{in} is the input voltage in the ADC and V_{DDA} is the supply voltage of the DSP.

For bipolar analog signals, a $V_{DDA}/2$ voltage shift must be performed. A schematic for the DC level shifter is shown in Fig. 3. A well know configuration of a summing amplifier, allow us to add an offset voltage of +1.5V to the input signal.

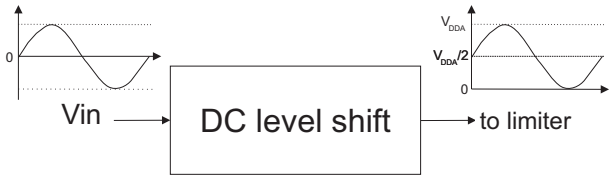

Fig. 3. DC level shifter.

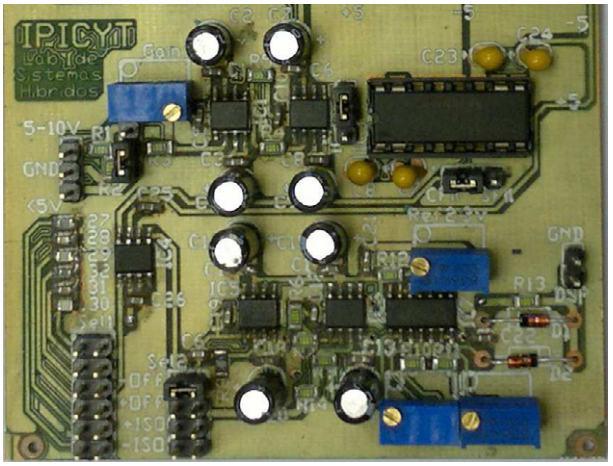

Fig. 4. Prototype of the SCC.

2.5. Limiter

As in the case above, the design of voltage limiters for DSPs or FPGAs devices has to be carefully analyzed. For example, the ADC in the DSP TMS320F2812 has an input voltage range of $0 - 3V$ and requires a supply voltage of 3.3V (V_{DDA}). Voltages above $V = V_{DDA} + 0.3V$ or below $-0.3V$ applied to an analog input pin, may temporarily affect the conversion [13]. To avoid this, a double shunt limiter is used to keep the analogue input within these limits. If the input voltage satisfies $0 \leq V_i \leq 3V$, both D_1 and D_2 are nonconducting and the output voltage follows the input (*i.e.* $V_i = V_o$).

3. Realization and testing of the SCC

In this section, the SCC prototype is presented and the frequency response of the SCC is obtained in order to verify that the design objectives are met; also the performance of the proposed SCC is evaluated in the laboratory. A picture of the designed SCC prototype, is shown in Fig. 4.

The following configurations are possible in the proposed circuit:

- Attenuator-isolation-antialiasing-DC level shift-Limiter
- Attenuator-antialiasing-DC level shift-Limiter
- Attenuator-DC level shift-Limiter
- Attenuator-isolation-DC level shift-Limiter

Hence the SCC can operate in four configurations, according to the application the required configuration can be selected (*e.g.* inverters, DC/DC converters, smart meters, power quality measurement, etc.). It is noteworthy that the proposed SCC has a power demand of less than 0.5W with a total cost of about US$60.

The frequency response of the prototype is performed using a personal computer (Pentium IV with Windows 2000), a National Instruments acquisition board (CompactRIO), and a Tektronix AFG3022B function generator. Since our instrument has been designed for five frequency ranges (see Section 2) a linear frequency sweep with the generator is performed (using a chirp signal) from 1Hz to 500kHz. Acquisitions in the input and in the output of the instrument are done by the CompactRIO board using 2 ADCs of 16 bits to get the frequency response. Once the data was acquired, the response was plotted in Matlab and a suitable software has been used to identify the system. Table 1 shows the comparison of the experimental cut-off

Table 1. Comparison of the theoretical and experimental cut-off frequencies of the SCC.

Cut-off frequency	
Theoretical (kHz)	Experimental (kHz)
5	4.98
10	9.98
15	15.10
25	25.25
50	49.80

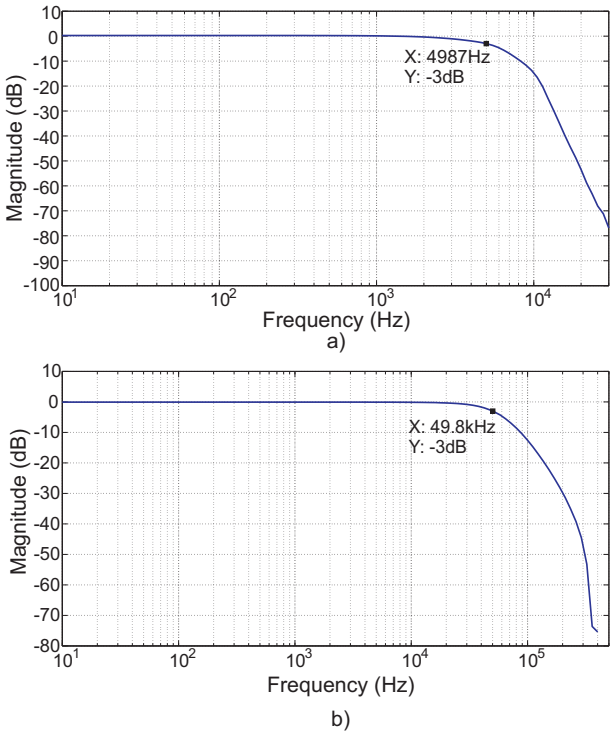

Fig. 5. Frequency response of the SCC for cut-off frequencies of a) 5 kHz and b) 50 kHz.

frequencies and the proposed ones. As can be observed, the experimental values are close to the theoretical ones, the small deviations are due to the tolerance of the capacitors and other inaccuracies.

The frequency response of the system for cut-off frequencies of 5kHz and 50kHz are shown in Figure 5 a) and b) respectively. As can be seen, the frequency response of the SCC is plain before the cut-off frequency.

The SCC was also submitted to test in order to verify their operational features. The peak to peak values of voltage as input an the corresponding output was measured. The result obtained with the SCC using each one of its stages for a sinusoidal signal is shown in Fig. 6. As we can see the input signal is attenuated and a DC level shift of 1.5V has been added to it, the phase shift is due to the antialiasing filter.

Moreover, the performance of the proposed SCC was evaluated using an AC signal from a hammer drill. To this end and for comparison purposes, the input current of a hammer drill was measured and conditioned using the proposed SCC. The current was measured using two methods: a hall effect sensor (LEM55-P) and the Tektronix AC/DC current probe model A622 with a scale of 100mV/A. Fig. 7 a) shows the measured signals and the signal from the SCC. As can be seen, the signal from the SCC has the same shape than the measured signals; however the conditioning can successfully adequate the voltage from 0 to 3V.

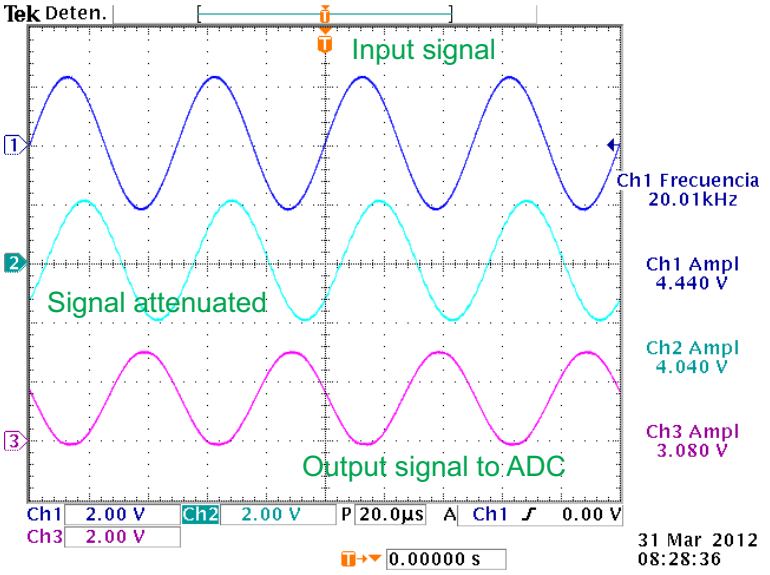

Fig. 6. Test with sinusoidal input.

In order to evaluate the limiter, a perturbation is applied to the hammer drill. An increment of its current consumption results as can be seen in (Fig. 7 b)). It can be observed that the SCC limits the output signal avoiding the saturation the ADC.

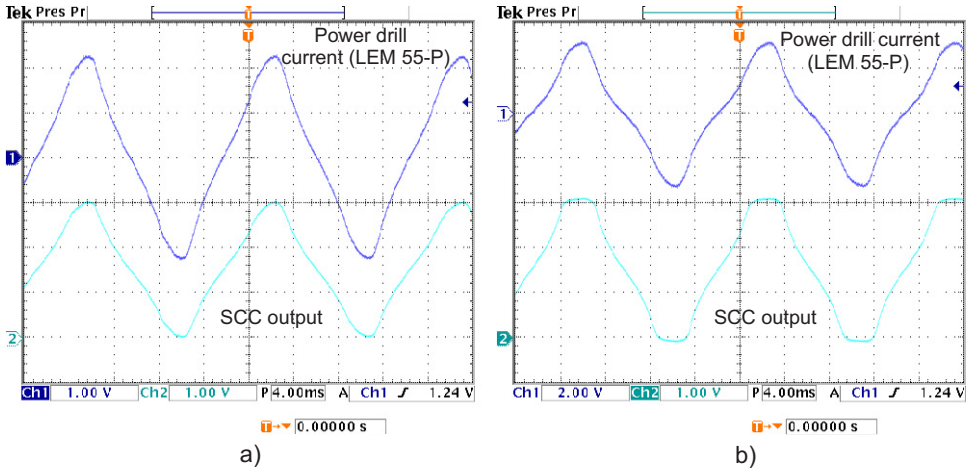

Fig. 7. Time evolution of a hammer drill current. Comparison of SCC with measurement devices a) normal operation, b) disturbed operation.

4. Conclusion

In this work a simple, reconfigurable architecture for SCC has been proposed. The card has been designed under the requirement of having low-power consumption and low cost. It is shown that the SCC is able to attenuate signals up to ± 15V and filter effectively frequencies above 5k, 10k, 15k, 25 and 50kHz

using a reconfigurable antialiasing filter. The SCC limits the output signal between 0–3V and an isolated stage can be included for power electronics applications. The SCC is made with off-the-shelf components.

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