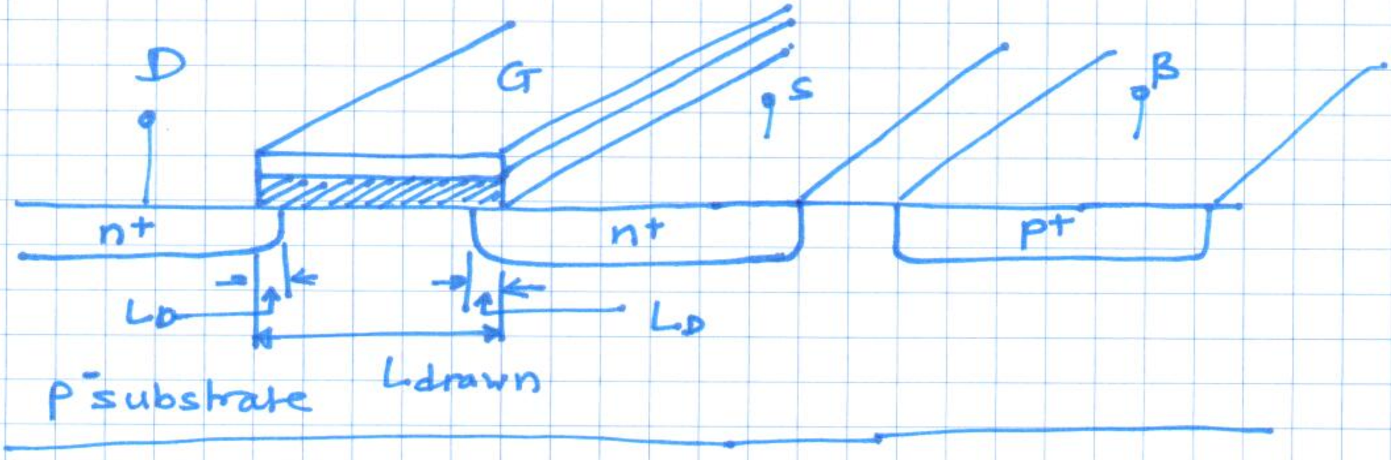
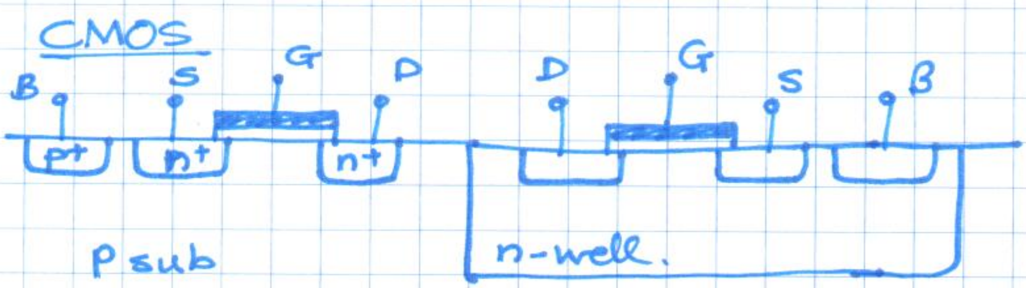
2AUG2019

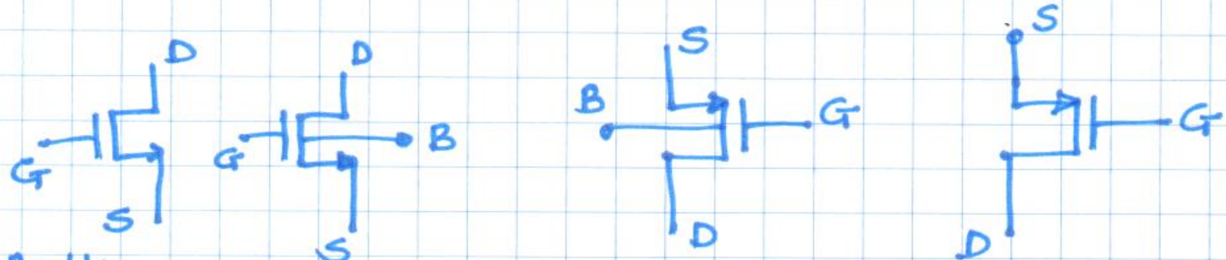
NMOS transistor



* LD due to side diffusion
* $L_{eff} = L_{drawn} - 2 \cdot L_D$.
* S - D interchangable
* S - source of charge carriers
  D - drain - collects charge carriers & removes them.

CMOS





Bulk implicit gnd.

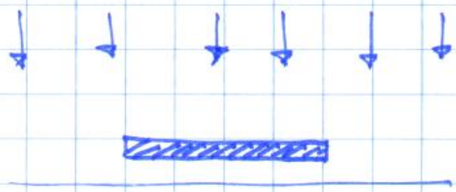
Bulk connection implicit vdd.

* Why polysilicon instead of Metal for gate

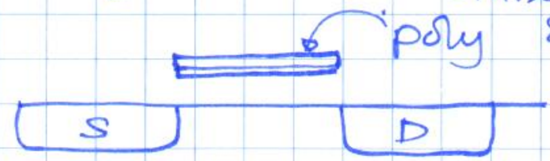
with poly Si we first put the gate & then doping as it can withstand high temp of anneling

→ Polysilicon – allows transistor gate definition very accurately – self aligned process. → smaller & faster transistor.

This helps to to reduce overlap



→ doping process – high temp annealing 8000°c



→ poly can withstand high temp. Metal/AL melt

→ V_T reduction ϕ_{ms} poly to s work function.

with Metal. – high V_T.

$$\phi_{ms} = \phi_{F_{sub}} - \phi_{F_{gate}}$$

n type poly.

$$= \frac{kT}{q} \ln\left(\frac{n_i}{N_A}\right) - \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right)$$

N_A – psub

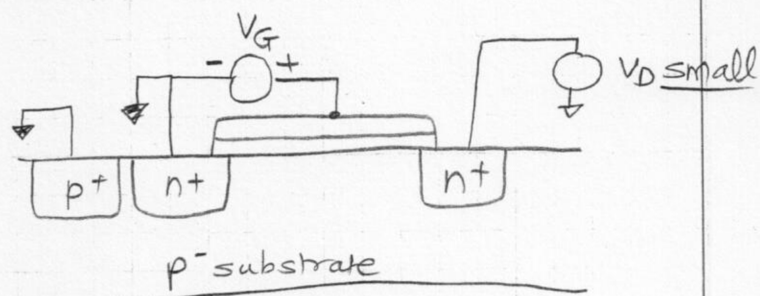
$$= \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

⇐ can be changed.

ANALOG CMOS IC DESIGN

MOS DEVICE PHYSICS BASICS

NMOS crosssection



As $V_G \uparrow$, holes in p-substrate repelled leaving behind -ve ions. (depletion region). As $V_G \uparrow$ further width of depletion region increases. Cap divider effect between gate - interface (oxide) - substrate. When V_G increases beyond sufficient positive value (V_{TH}), e^- flow from source to the interface & drain - channel formed. (Inversion)

V_{TH} - Threshold voltage $= \Phi_{MS} + 2\Phi_F + \dfrac{Q_{dep}}{C_{ox}}$

Φ_{MS} - work function difference betn gate & sub

Surface potential $\Phi_F = \dfrac{KT}{q} \ln\left(\dfrac{N_{sub}}{N_i}\right)$ — N_{sub} → doping density; N_i → e^- density in undoped Si

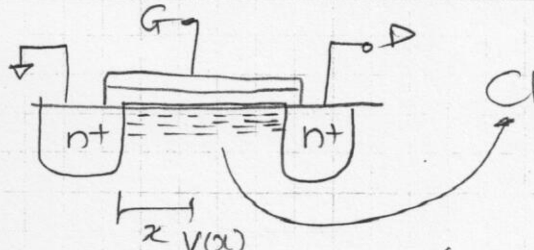
Q_{dep} = Charge in depletion region

$= \sqrt{4q\,\underbrace{\epsilon_{si}}_{\text{dielectric constant}}\,|\Phi_F|\,N_{sub}}$

C_{ox} - Gate Oxide cap.

$\epsilon_{si} = 11.68$

$\epsilon_{SiO_2} = 3.97$



Channel Charge Q_d density

@ $V_{GS} = V_{TH}$ Channel Begins to form.

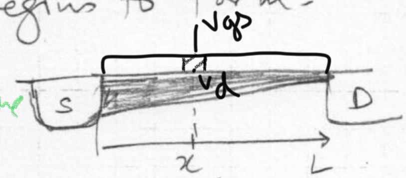
$$Q_d = W\, C_{ox} (V_{GS} - V_{TH})$$

per unit length

excess gate V

$$((V_{gs} - V_T) - V(x))$$

V at the surface at x distance



$$Q_d(x) = W\, C_{ox} [V_{GS} - V(x) - V_{TH}]$$

After formation of inversion layer the excess V_{gs} is used to build Q_d

Channel potential @ position x from source.

$$I_{DS}(x) = -W\, C_{ox} [V_{GS} - V(x) - V_{TH}]\, v$$

Charge velocity

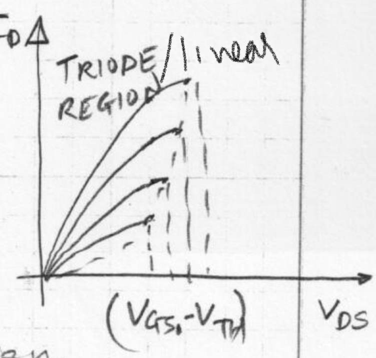
$$v = \mu_n E = \mu_n \frac{dV(x)}{dx}$$

$$I_{DS}(x) = W\, C_{ox} [V_{GS} - V(x) - V_{TH}]\, \mu_n \frac{dV(x)}{dx}$$

$$\int_0^L I_{DS}(x)\, dx = \int_0^{V_{DS}} \mu_n W\, C_{ox} [V_{GS} - V(x) - V_{TH}]\, dV(x)$$

$$L \cdot I_{DS} = \mu_n C_{ox} W \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2\right]$$



TRIODE Region

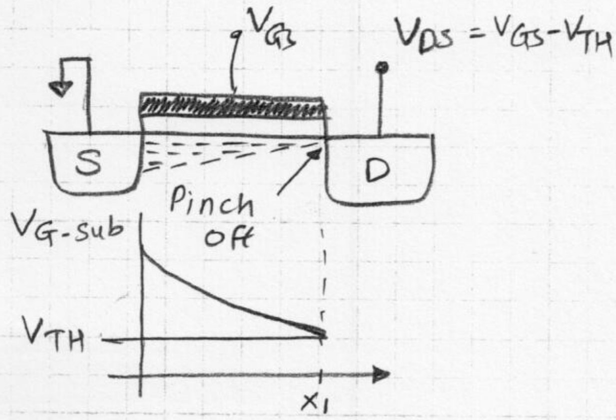
for $V_{DS} \ll 2(V_{GS} - V_{TH})$

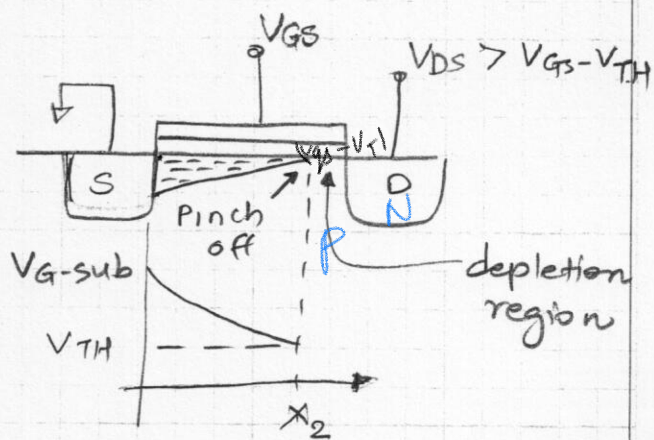
$$I_{DS} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$R_{ON} = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})}$$

Linear Region

When $V_{DS} > V_{GS} - V_{TH}$





$V(x_1) = V_{GS} - V_{TH}$

Remember $Q_d(x) = W C_{ox} [V_{GS} - V(x) - V_{TH}]$

@ pinch off point $Q_d(x) = 0$ $V(x) = V_{GS} - V_{TH}$

As e^- (carriers) approach pinch-off point, their velocity rises big time. ($v = I/Q_d$) → electrons shoot through the depletion region. & arrive @ drain.

After pinch-off - device is in saturation region.

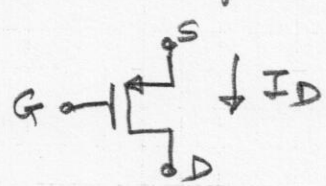
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$$ { integration from $V(x) = 0 \rightarrow (V_{GS} - V_{TH})$

L' where channel pinches off

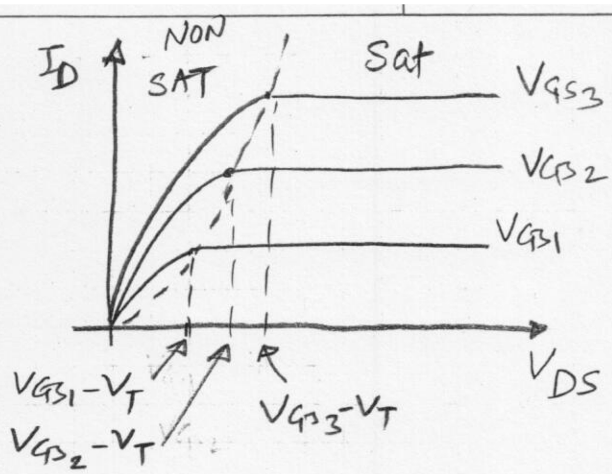
$V_{GS} - V_{TH}$ ⇒ called V_{dsat}

$V_{DS} > V_{dsat}$ Required for Saturation region op.

✱ PMOS devices

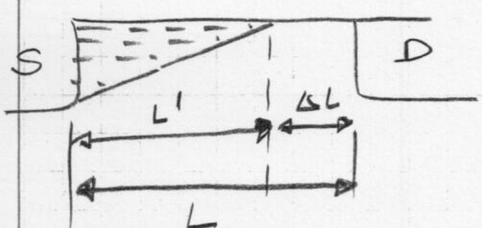


$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L'} (V_{SG} - |V_{THp}|)^2$$



Channel length Modulation

Recall pinch-off in saturation



L' is function of V_{DS}

$$\frac{\Delta L}{L} = \lambda V_{DS} \quad \text{(in saturation)}$$

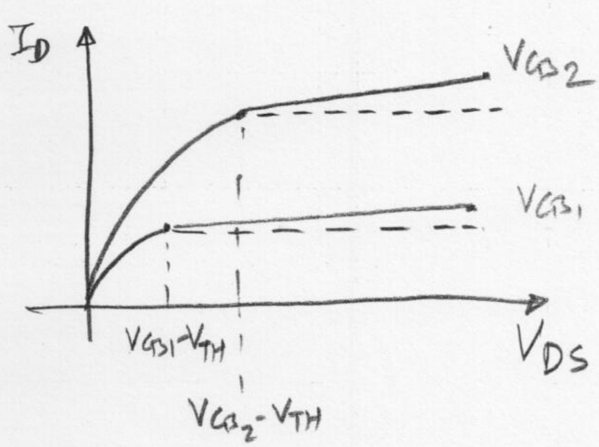
$$\frac{L'}{L} = \frac{L - \Delta L}{L} = (1 - \lambda V_{DS})$$

$$\frac{1}{L'} = (1 + \lambda V_{DS})\frac{1}{L}$$

$\lambda \rightarrow$ Channel length modulation Coeff.

substituting in sat equation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

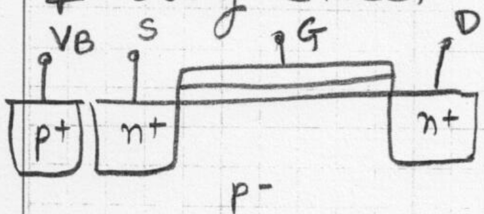


$$\underbrace{\frac{\Delta L}{L}}_{} = \lambda V_{DS}$$

Relative variation in length, due to V_{DS}

Longer L
Smaller λ

★ Body Effect



$\boxed{\text{Body - back gate}}$ acts like another gate affecting channel

$\uparrow V_{SB} \rightarrow \uparrow V_T$

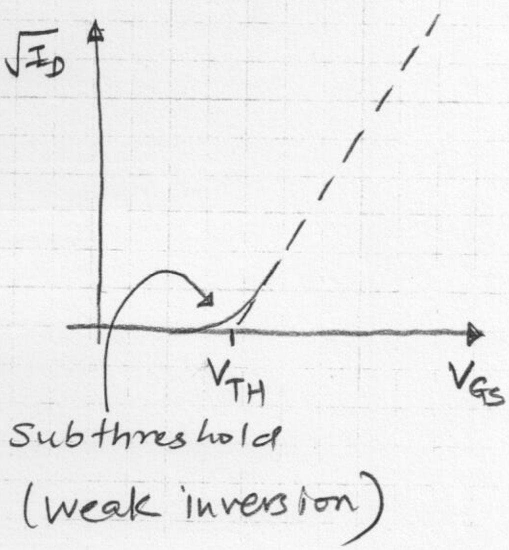
$$V_{TH} = V_{TH_0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

Body Effect Coefficient $\quad \gamma = \dfrac{\sqrt{2q\,\epsilon_{si} N_{sub}}}{C_{ox}} \sim 0.3 - 0.4\ \sqrt{V}$

$\uparrow V_{BS} \quad \downarrow V_T \quad$ Can be used to reduce V_T by forward biasing V_{BS}.

→ make sure current is limited after forward biasing.

★ Subthreshold Conduction.



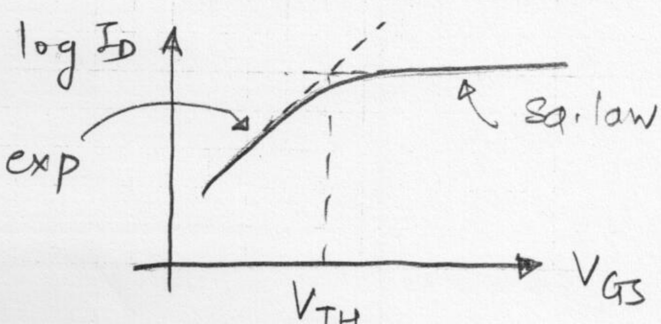
Even for $V_{GS} < V_{TH}$

— finite I_D - exponential dependence on V_{GS}

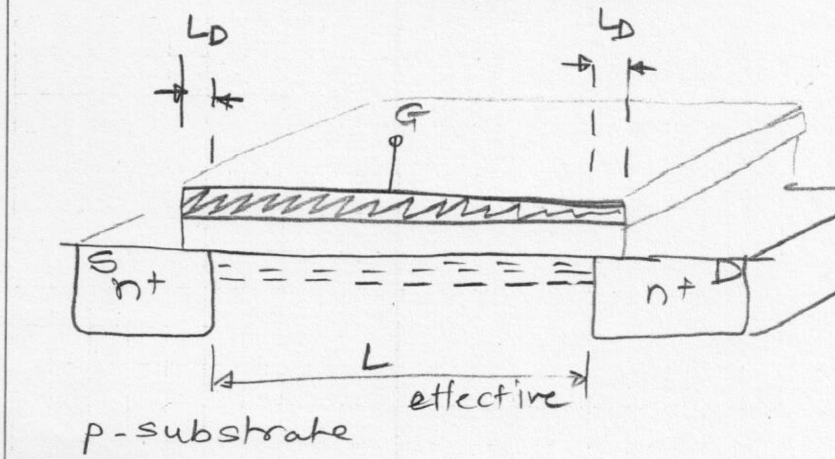
$$I_D = I_0 \exp \frac{V_{GS}}{\xi V_T}$$

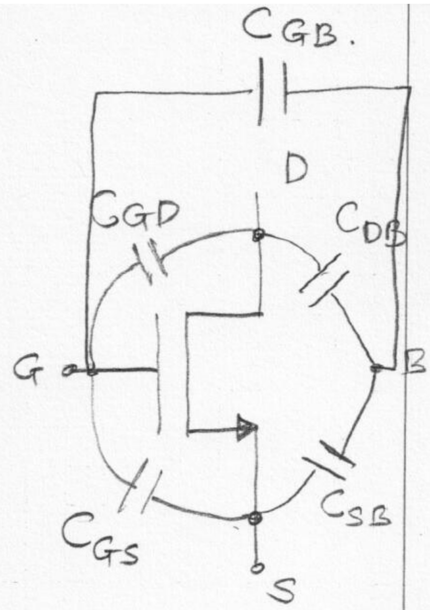
$\xi > 1 \ ; \ V_T = \dfrac{kT}{q}$

Similar to $I_C - V_{BE}$ of bipolar transistor



MOS device Capacitances





Device is off

$C_{GD} = C_{GS} = C_{ov} \cdot W$ ← $C_{ov} \to L_D \cdot C_{ox}$

$C_{GB} = C_{ox} WL$ series with C_d ← depletion sub. cap. $= WL\sqrt{q\epsilon_{si}\frac{N_{sub}}{4\phi_F}}$

Device is in triode region — $WL\,C_{ox}$ equally divided beth gate & source/drain term.

$$C_{GD} = C_{GS} = \frac{WL\,C_{ox}}{2} + W\,C_{ov}$$

$C_{ov} \to L_D \cdot C_{ox}$

$C_{GB} = 0$ Shielding

Device is in saturation region — pinch off channel

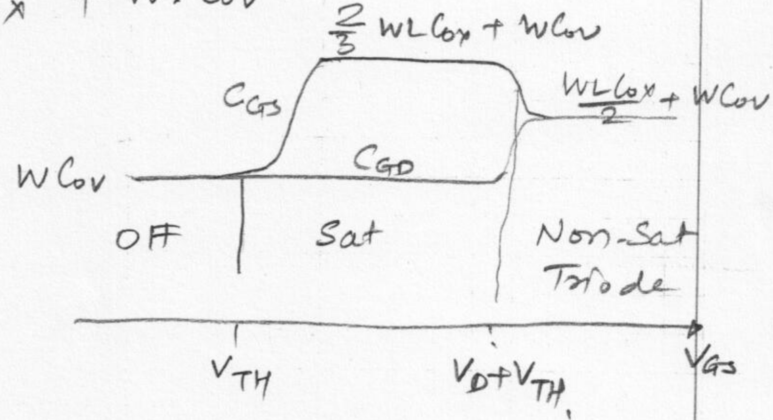
$$C_{GD} = C_{ov} \cdot W$$

$$C_{GS} = \frac{2}{3} WL\,C_{ox} + W \cdot C_{ov}$$

$C_{ov} \to L_D \cdot C_{ox}$

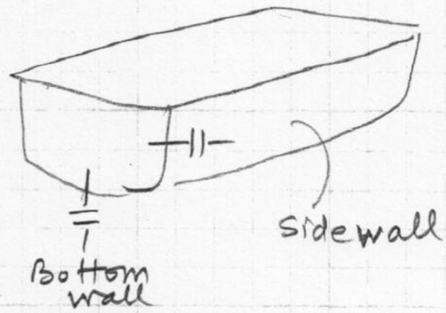
$C_{GB} \approx 0$

Muller Kamins proof



Drain / source → bulk cap.

$$C_{DB} = \underbrace{\frac{C_J \cdot A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{MJ}}}_{\text{Bottomwall}} + \underbrace{\frac{CJSW \cdot P_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{MJSW}}}_{\text{Sidewall}}$$



$$C_{SB} = \frac{C_J \cdot A_S}{\left(1 + \frac{V_{SB}}{P_B}\right)^{MJ}} + \frac{C_{JSW} \cdot P_S}{\left(1 + \frac{V_{SB}}{P_B}\right)^{MJSW}}$$

C_J → source/drain bottomplate j^n cap/area   F/m²

C_{JSW} → sidewall   F/m

P_B → source/drain junction built-in potential   V

MJ, MJSW → exponents (unitless)   0.3 to 0.4