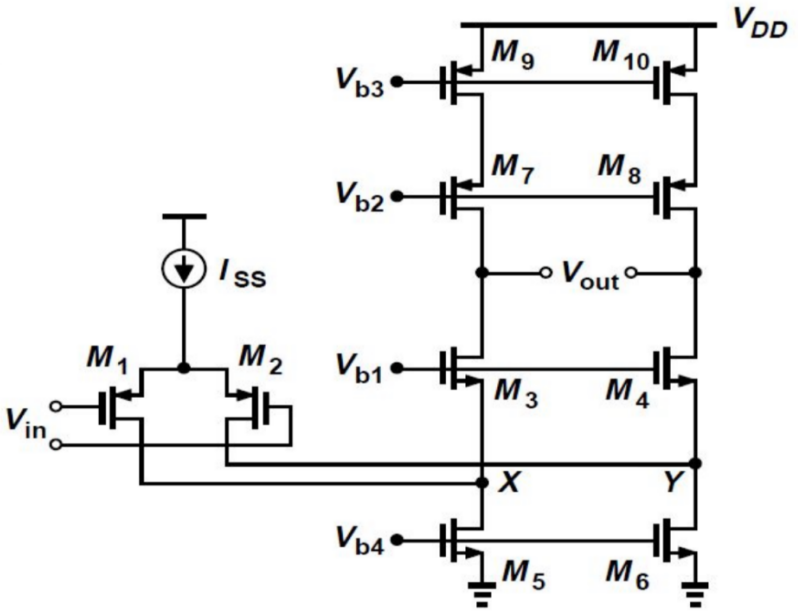
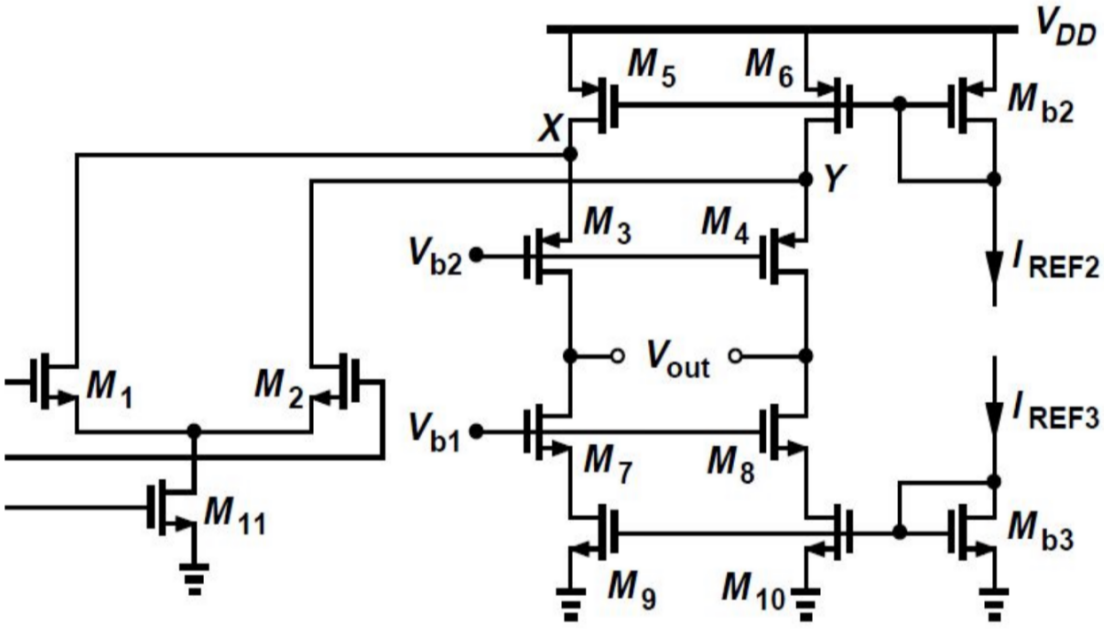
Folded cascode op amp with cascode PMOS load:



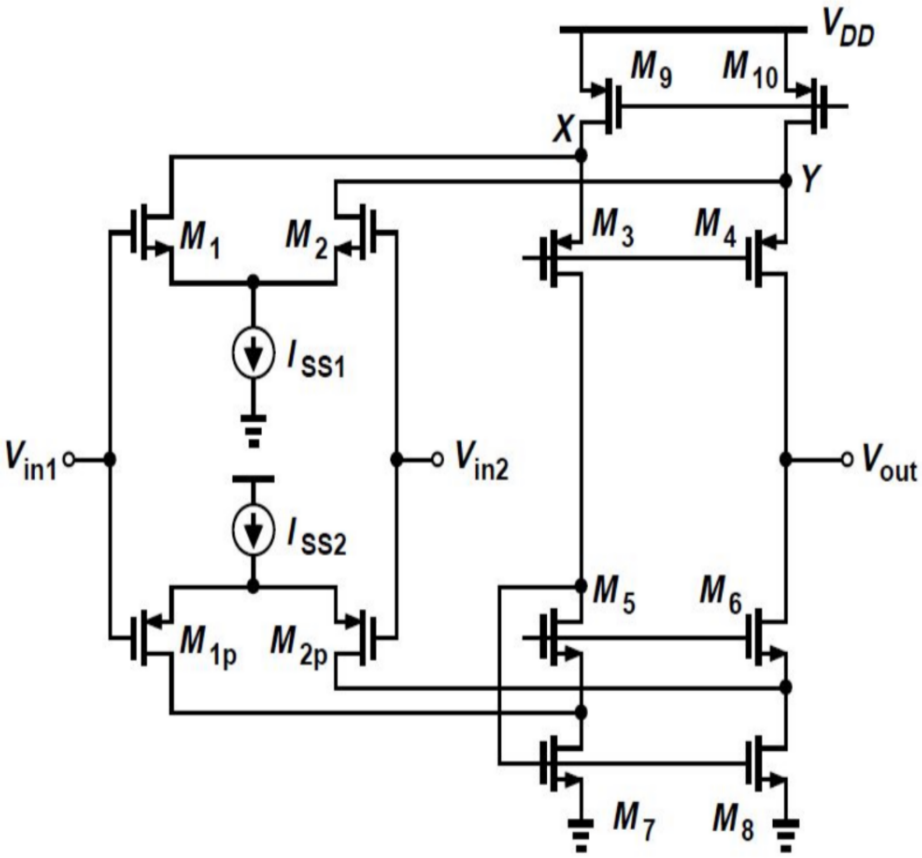
$V_{in,cm\ -\ range} => V_{DD}-(V_{Tp}+2V_{dsatp})$ to $V_{dsatn\ (previous\ stage)}$

Folded cascode op amp with cascode NMOS load:

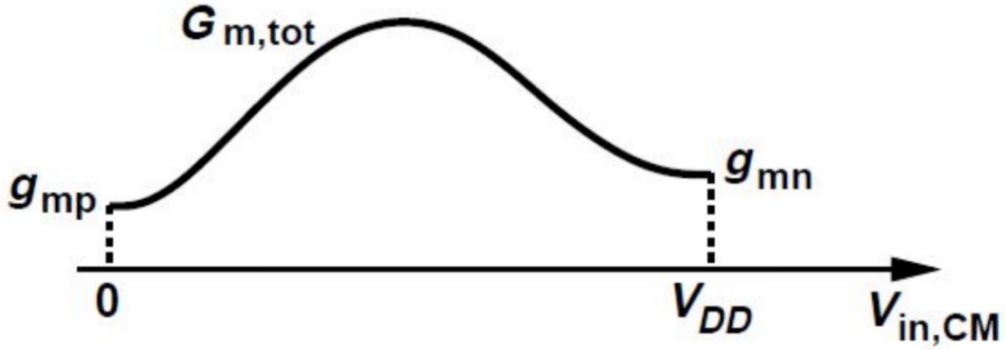


$V_{in,cm\ -\ range} => (V_{DD}- V_{dsatp\ (previous\ stage)})$ to $(V_{Tn}+2V_{dsatn})$

Extension of input common mode range:

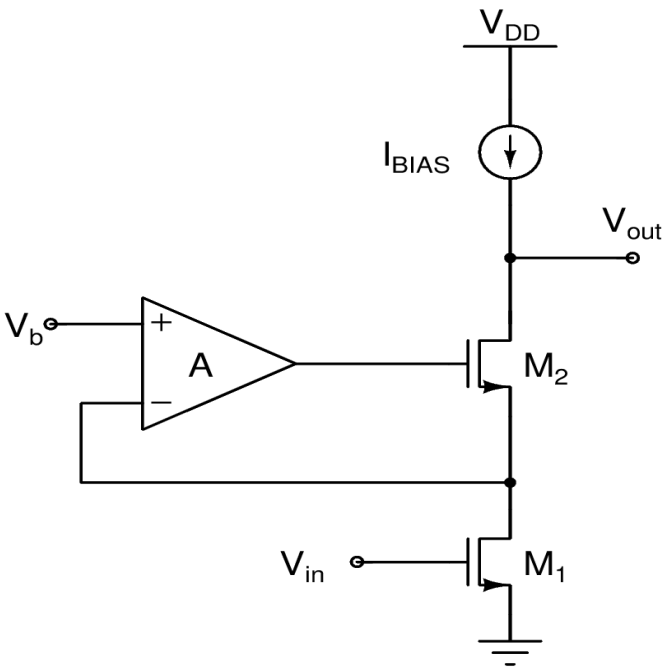


$$V_{\text{in, cm range}} = \sim V_{DD}$$



Reference: Design of Analog CMOS Integrated Circuits- B. Razavi. Chapter 9

Gain Boosting



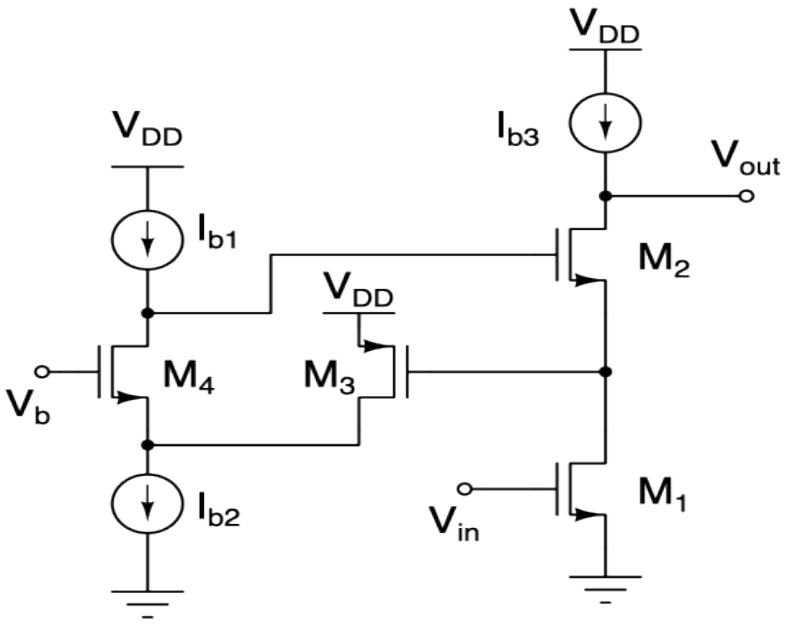
$$G_m = g_{m1}$$

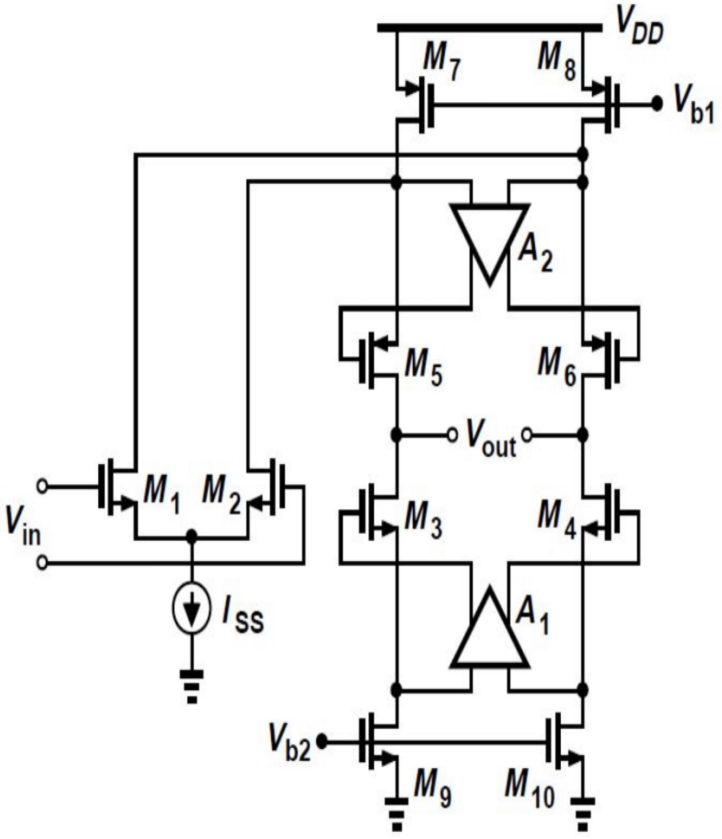
$$R_{out} = r_{o1} g_{m2} r_{o2} .(A+1)$$

$$\text{Gain} = g_{m1} r_{o1} g_{m2} r_{o2} .(A+1)$$

Reference: Klaas Bult JSSC – Dec 1990 pp. 1379 : Gain Boosting with Fast Settling

Implementation:





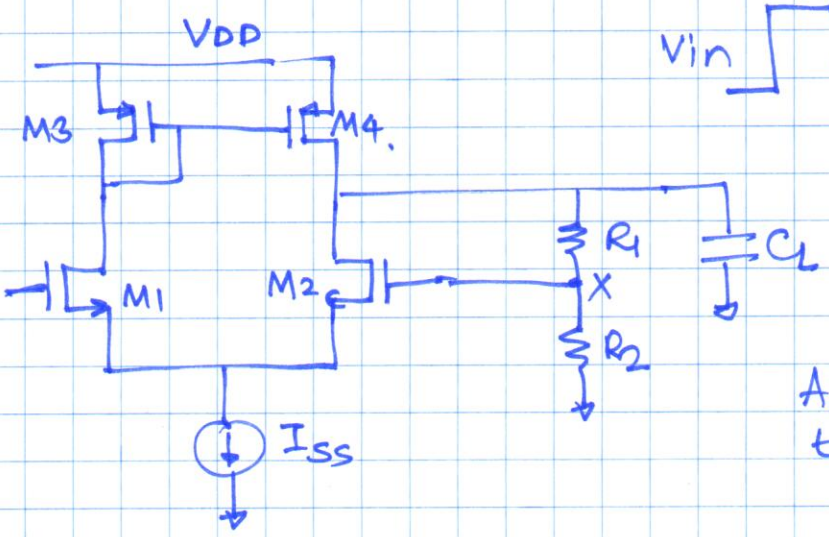
$$A = g_{m3} r_{o3} \frac{g_{m4} r_{o4}}{3}$$

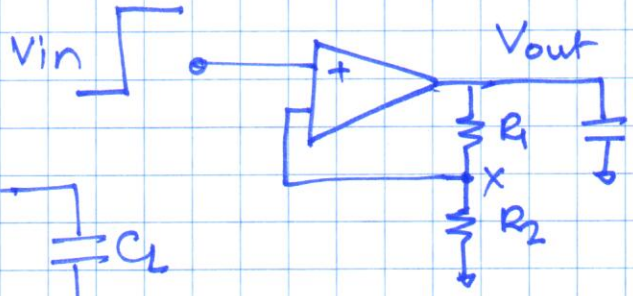
Slew Rate – Revisited

— large signal behavior Non-Linear

— fastest change in the node voltage.
decided by $\frac{I}{C} = \frac{dV}{dt}$

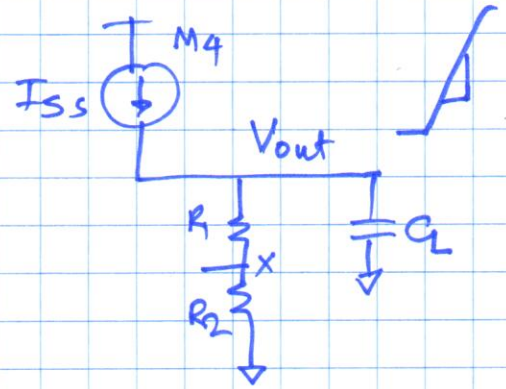
Consider single stage OTA





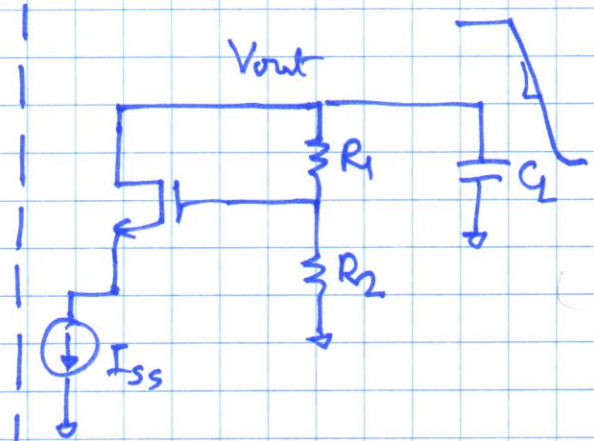
Assume $R_1 + R_2$ large to neglect current through

When ⌐ Vin step is applied,



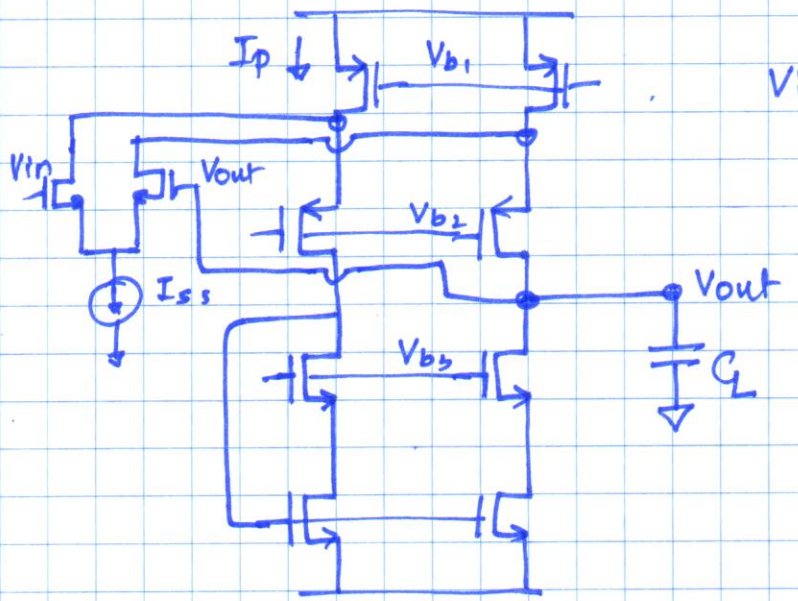
+ve slew rate = $\frac{I_{ss}}{C_L}$

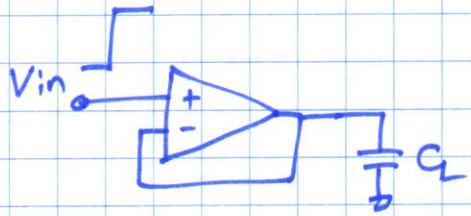
When ⌐ vin applied,



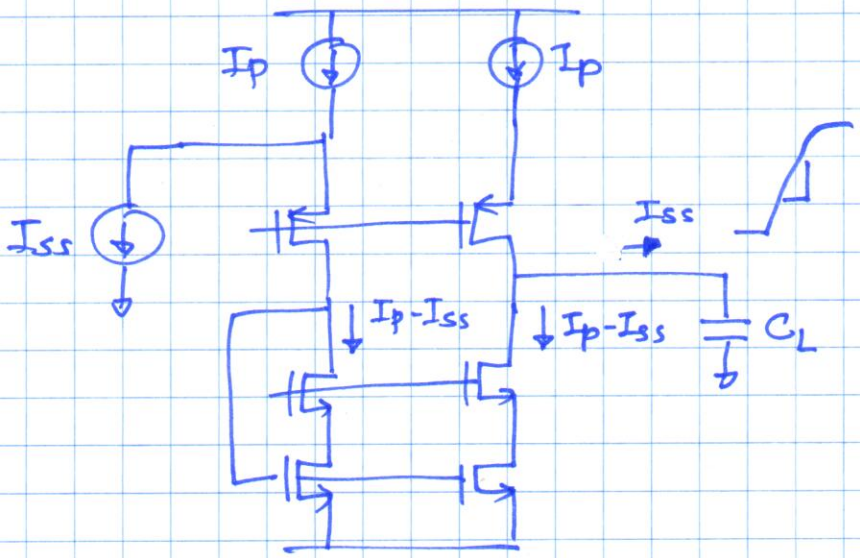
-ve slew rate = $\frac{I_{ss}}{C_L}$

Folded Cascode Opamp



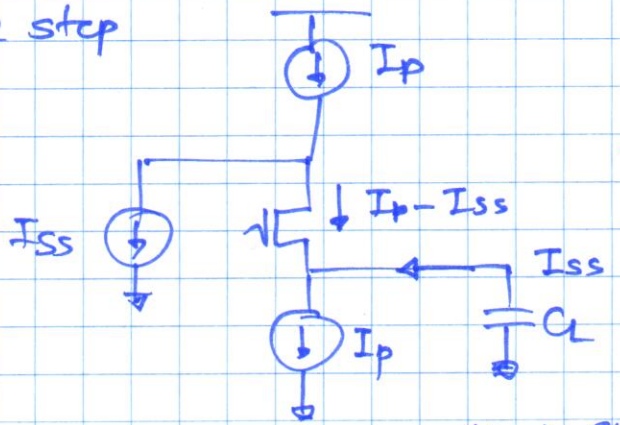


+ve step



+ve slew rate $= \frac{I_{ss}}{C_L}$

-ve step

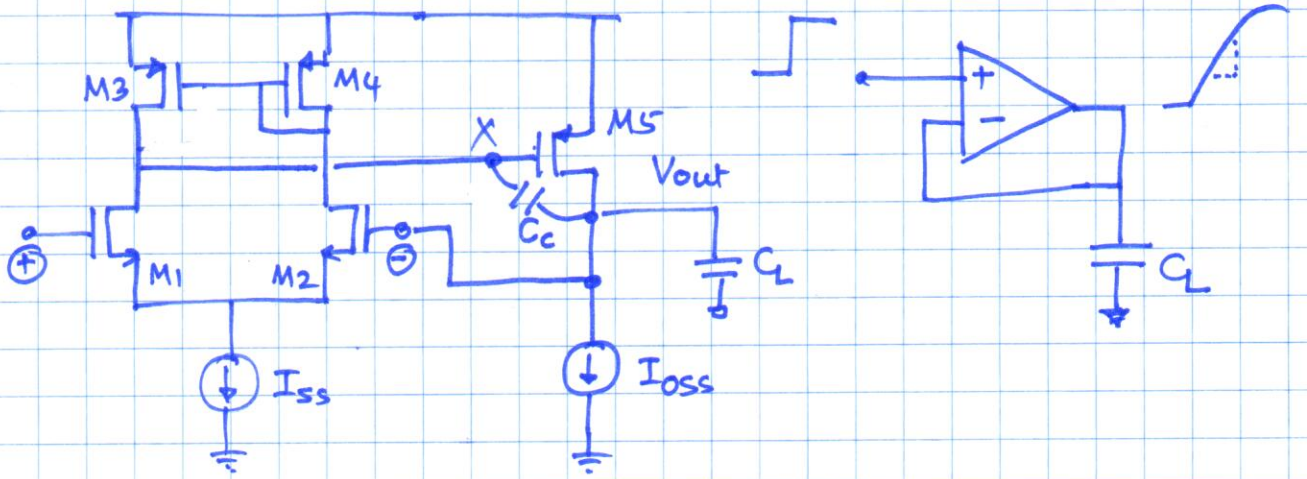


-ve slew rate $= \frac{I_{ss}}{C_L}$

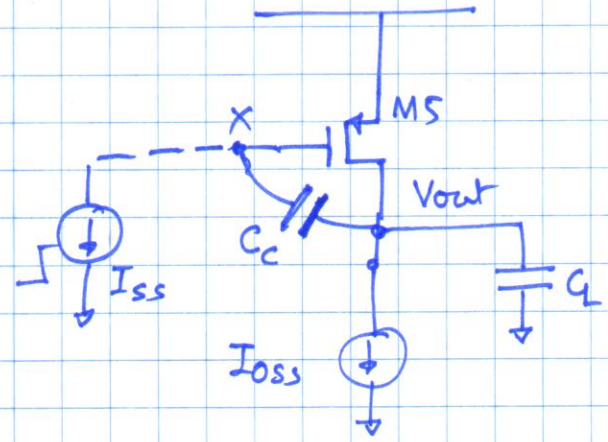
Keep $I_p = I_{ss}$ atleast

Else Slew rate limited to I_p/C_L I

Two stage op-amps slew rate.



+ve i/p step



Node x virtual gnd due to gain of M5.

$$\frac{dV_{out}}{dt} = \frac{I_{ss}}{C_c}$$

Current thru. $C_L = C_L \cdot \frac{dV_{out}}{dt}$

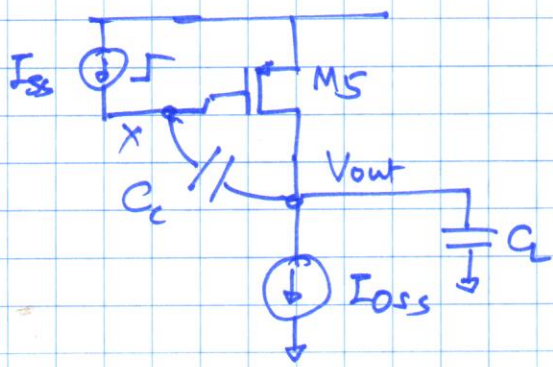
$$= \frac{C_L}{C_c} \cdot I_{ss}$$

M5 must support & stay in sat.

$$\left(I_{ss} + \frac{C_L}{C_c} I_{ss} + I_{oss}\right)$$

Slew rate = $\frac{I_{ss}}{C_c}$

-ve i/p step



$$\frac{dV_{out}}{dt} = \frac{I_{ss}}{C_c} \quad \text{(slew rate)}$$

if. $I_{oss} \geq I_{ss} + \frac{C_L}{C_c} I_{ss}$

Slew rate if $I_{oss} < I_{ss}\left(1 + \frac{C_L}{C_c}\right)$

$$= \frac{(I_{oss} - I_{ss})}{C_L}$$ | M5 off

How to increase slew rate?

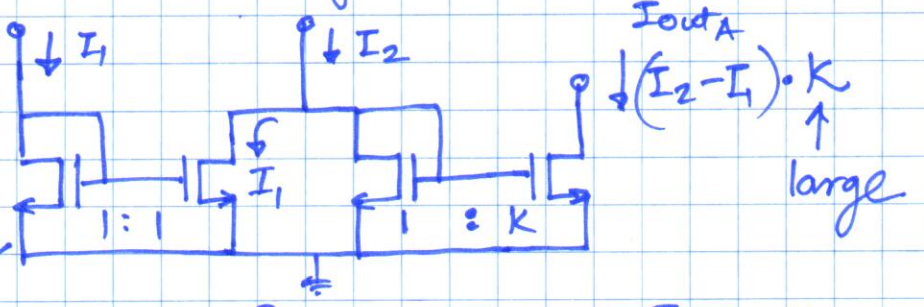
→ ↑ I_T → Increase in Quiescent Power

→ increase I_T only when large i/p voltage step applied.

→ Adaptively Biased opAMP. JSSC - JUNE 82

REFERENCE : ADAPTIVE BIASING CMOS AMP - DEGRAUWE

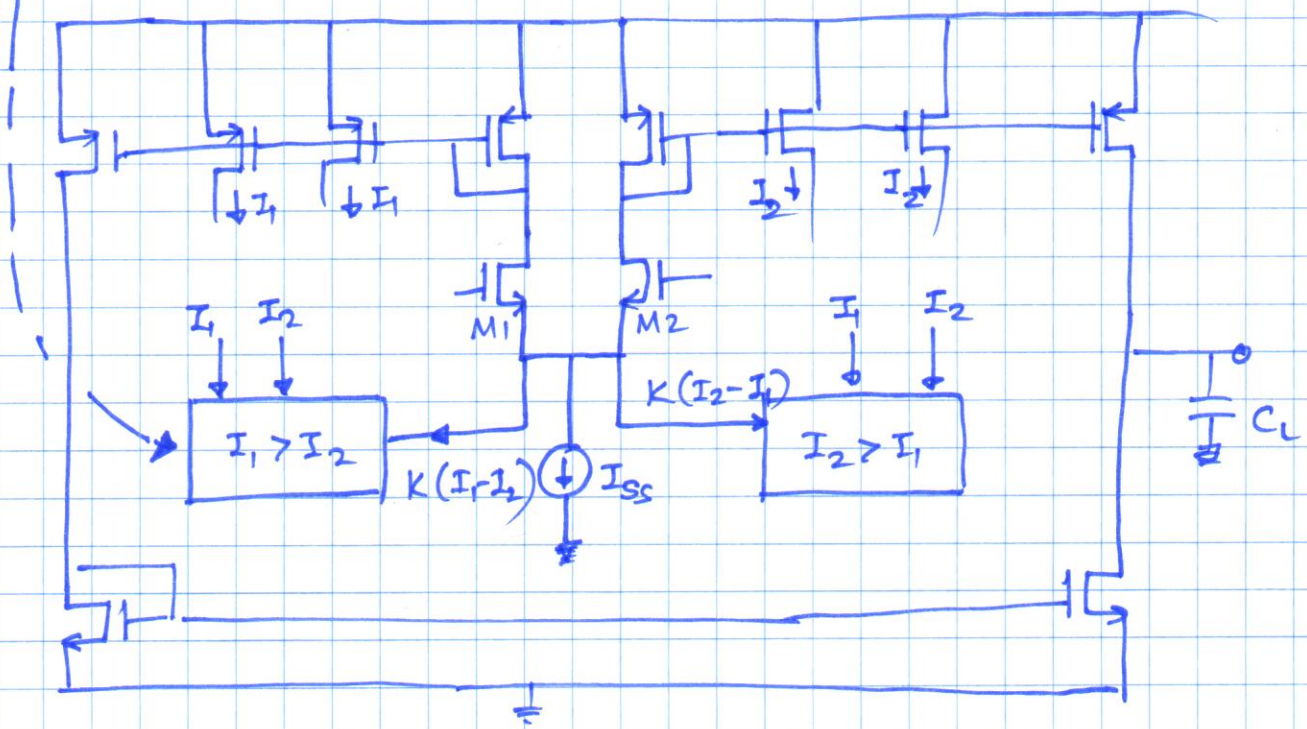
Consider following current mirror based circuit

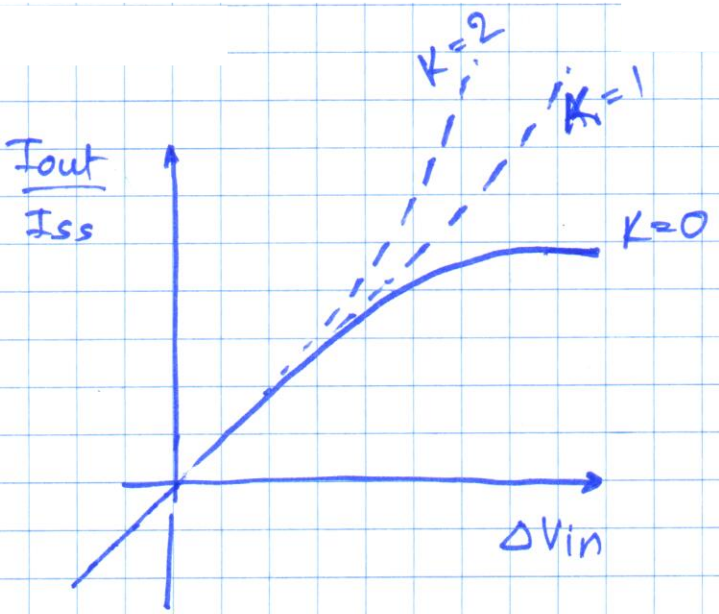


⇒ when $I_1 = I_2$ → $I_{out_A} \cong 0$

when $I_2 \gg I_1$ → $I_{out_A} = \underbrace{K(I_2 - I_1)}_{\text{large current}}$

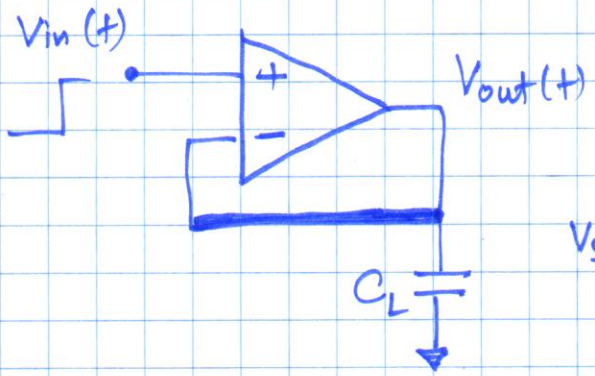
$I_2 < I_1$ → off. $I_{out_A} = 0$

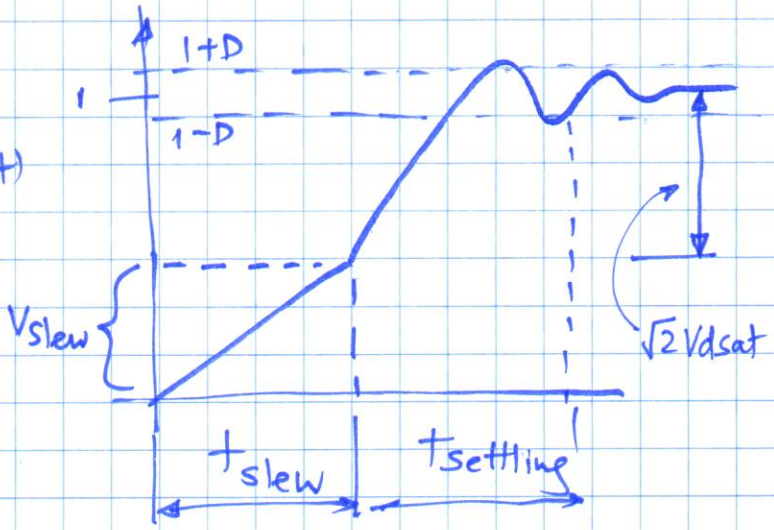




✡ Settling Time — Small-signal

Consider





Excellent Reference

Considerations for fast Settling Amplifiers

Howard Yang, Allstot —

IEEE Tran. CAS March 90

(from Allstot Notes)

Consider Opamp with single pole response. $a(s) = \frac{a_0}{\left(1+\frac{s}{p_1}\right)}$

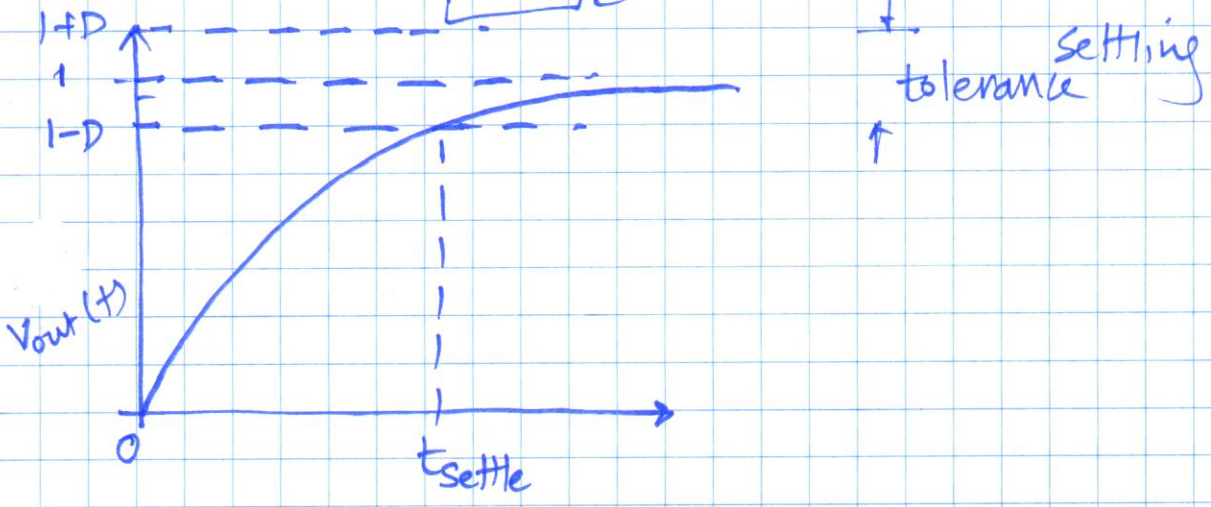
$$A(s) = \frac{a(s)}{1+a(s)} = \frac{a_0 p_1}{s + p_1(a_0+1)}$$

For unit step $V_{in}(s) = \frac{1}{s}$

$$V_{out}(s) = A(s) V_{in}(s) = \frac{a_0}{a_0+1}\left[\frac{1}{s} - \frac{1}{s+p_1(a_0+1)}\right]$$

Time domain ($\frac{a_0}{a_0+1} \to \sim 1$)

$$V_{out}(t) = \left[\frac{a_0}{a_0+1}\right]\left[u(t) - e^{-p_1(a_0+1)t}\right]$$



τ = small-signal settling time constant

$$= \frac{1}{p_1(a_0+1)} \simeq \frac{1}{p_1 a_0} \simeq \frac{1}{\omega_u} \leftarrow \underline{\text{GBW}}$$

D (%)	$t_s = -\tau \ln D$	f_u
1 (6.64 bits)	4.61τ	73.4 MHz
0.01 (13.3 bits)	9.21τ	147 MHz
0.001 (16.6 bits)	11.51τ	183 MHz
0.0001 (20 bits)	13.82τ	220 MHz

for 100 MHz operation.

Example $D = 0.01\%$ $\quad 20\log(0.01/100)^{-1}$

$= 80\,dB$ SNR

$\Rightarrow \frac{80}{6} \Rightarrow$ 13.33 bits resolution

$t_s = -\tau \ln D = -\tau \ln(0.0001)$

$= 9.21\tau.$

we wish to settle in $\frac{1}{100MHz}$ time $= 10nS.$

$t_{settle} = 10ns = 9.21\tau.$

$\Rightarrow \tau = 1.0857\,nS.$

$f_u = \frac{1}{2\pi\tau} = 146.6\,MHz$

Yang paper describes Minimum Settling Time as a function of Phase margin. for two pole system

Note Phase Margin depends on relative positions of two poles.

$$a(s) = \frac{a_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$