Effects of Lateral Charge Spreading on the Reliability of TANOS (TaN/AlO/SiN/Oxide/Si) NAND Flash Memory

Changseok Kang, Jungdal Choi, Jaesung Sim, Changhyun Lee, Yoocheol Shin,
Jintaek Park, Jongsun Sel, Sanghun Jeon, Youngwoo Park, and Kinam Kim

Semiconductor R&D Center, Memory Business, Samsung Electronics Co., Ltd.
San #24, Nongseo-Dong, Kiheung-Gu, Yongin-City, Kyungki-Do, Korea, 449-711
Phone:+82-31-208-2690 Fax:+82-31-209-3274 E-mail:changs.kang @samsung.com

ABSTRACT

It was found that the charge loss behavior of TANOS (TaN-Al_2O_3-Nitride-Oxide-Silicon) cells for NAND Flash memory application is highly dependent on the gate structures for the first time. The gate structures with trap layers remained on source and drain regions showed increased charge loss compared to the one with trap layers separated between different gate lines. The improvement by removing the trap layers between gate lines suggests that the lateral charge spreading via trap layers from the programmed cells to the adjacent erased cells contributes to the charge loss of the TANOS cells.

[*Keywords:* NAND, Flash Memory, TANOS, Charge Spreading, Charge Loss, Endurance]

INTRODUCTION

A TANOS-based NAND cell has been studied as an alternative technology to replace floating gate (FG) Flash memory technology since it provides reduced cell-to-cell interference, superior vertical scalability, and simpler process steps compared to the FG devices beyond 50nm node [1]. We reported that the use of high-k blocking layer (Al_2O_3) and TaN gates with high work function (~4.8eV) enabled thicker tunneling oxide (~40Å) which results in the improvement of charge retention characteristics of the TANOS devices [2]. Recently, 32G NAND Flash has been successfully demonstrated using a 40nm TANOS cell technology [3].

On the other hand, further understanding of the charge retention characteristics is inevitable to meet product-level reliability requirement. Charge loss of the SiN-based memory is composed of two components: One is vertical charge loss of the trap layer via the tunnel oxide or the blocking layer and the other is lateral charge migration. Most studies on the reliability of the SONOS memories for NAND Flash applications have been focused on the vertical charge loss [4]. However, the lateral charge loss may restrict cell structure of the devices depending on the integration scheme. Therefore, charge retention characteristics depending cell structures need to be investigated.

In this work, charge retention behavior was studied for two different gate structures, where trap layers of adjacent gate lines are connected as case "Connected" and separated as case "Separated" in Fig.1. The difference in the retention characteristics between the two cases will be addressed and a model explaining the results will be discussed. In addition, the effect of erase voltage on the charge retention of the TANOS device will be described.

EXPERIMENTAL

A TANOS cell was fabricated using the same integration scheme reported in [2] as shown in Table 1. A dielectric composite of SiO_2(40Å)/SiN(60Å)/Al_2O_3(150Å) and 150Å–thick TaN electrode were adopted for the TANOS cells. As a SiN trap layer, Si rich nitride (SRN) layer with a refractive index of 2.07 was used as a trap layer to improve erase speed.

The pattern pitches of word line and bit line are 126nm and 130nm, respectively. To investigate the effect of lateral charge spreading, two different gate structures were devised as shown in Fig.1: SiN trap layer of adjacent cells are connected in "Connected" and separated in "Separated". The gate etch was stopped on the Al_2O_3 blocking layer in case "Connected", whereas Al_2O_3 and SiN layer were cut during the gate etch process in case "Separated".

• **Well formation in cell and peripheral region and gate oxide formation for high voltage transistor**
• **Shallow Trench Isolation (STI) formation**
• **STI fill and planarization/Silicon nitride removal**
• **Gate oxide formation for low voltage transistor**
• **Poly-silicon deposition for peripheral region**
• **SiO_2-SiN-Al_2O_3-TaN formation for cell region**
• **WN/W material deposition for cell and peripheral region**
• **Gate definition (lithography and etching)** **(Two splits: "Connected" and "Separated" Trap Layers)**

Table 1. FEOL process flow of the TANOS-NAND Flash memory.

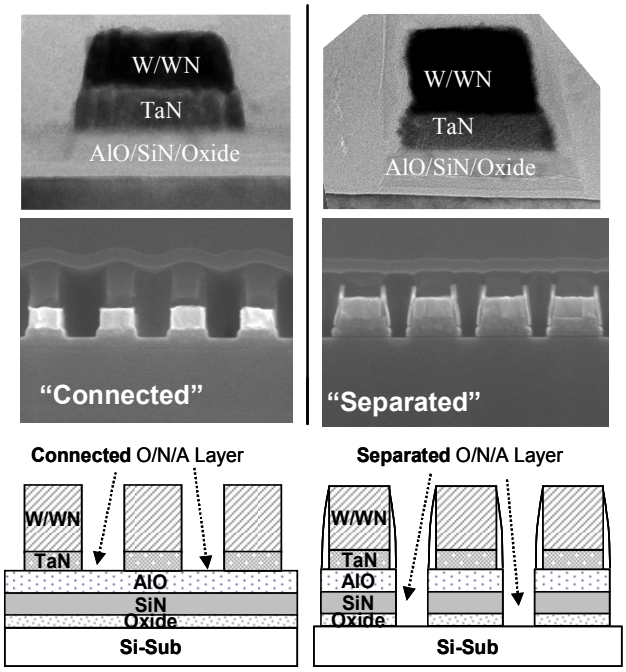


Fig.1. SEM and TEM photographs for "Connected"(left) and "Separated"(right) gate structures.

In the case of "Separated", it is desirable that Al_2O_3 and SiN layer are etched with sidewall spacers during gate etch process which contributes to the increase of O/N/A breakdown voltage (BV). BV distribution of O/N/A stacks with a 63nm gate node was compared for two cases: O/N/A gate stacks formed with and without gate spacers in Fig.2. BV of the O/N/A stacks with gate spacers shows ~ 5V higher BV and much narrower distribution compared to the other one. The improvement of the BV by the use of the gate spacers may be attributed to alleviation of damages induced during gate etching process or N- source/drain ion implantation.

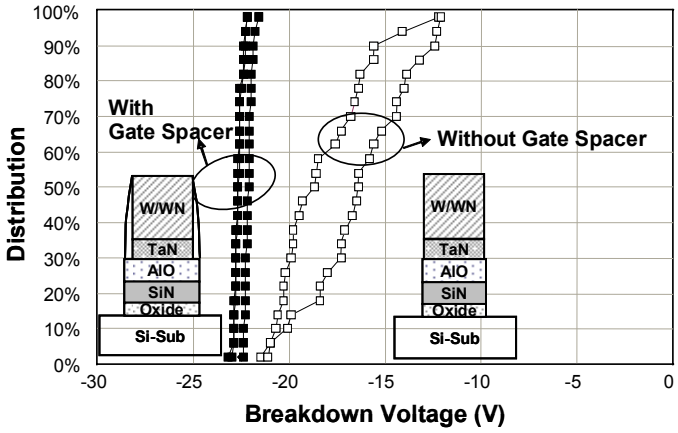


Fig.2. Comparison of hard breakdown voltage distribution for "Separated" gate structures patterned with and without sidewall spacers on the gate during gate etching process.

After patterning the gate structures, subsequent BEOL processes were performed by the conventional NAND Flash integration scheme.

RESULTS AND DISCUSSION

Fig.3 shows the programmed/erased cell pattern dependency of charge loss behavior in the "Connected" devices. In the pattern dependency test, 384 cells were used. In Fig.3 (A), initially, solid patterns were obtained by programming or erasing all cells at an average V_{TH} of 2.4V or -0.5V, respectively. Cells were erased by use of an erase voltage of 19V and an erase time of 10ms, and programmed by use of a program voltage of 17V and a program time of 200μs.

Then, V_{TH} distribution was measured for the programmed and erased cells after high temperature baking at 200℃ for 2 hours. After the baking, V_{TH}'s of the programmed cells decreases ~1V, and those of the erased cells increases ~0.5V as shown in Fig.3 (A). By comparison, in Fig.3 (B), half of the total cells were programmed and the other half of the cells were erased with a check-board pattern. Relatively increased V_{TH} shift is observed in the check-board pattern which has more chance for stored charges in the trap layer to spread laterally compared to the solid pattern. This result suggests lateral charge spreading occurs thorough the SiN trap layers.

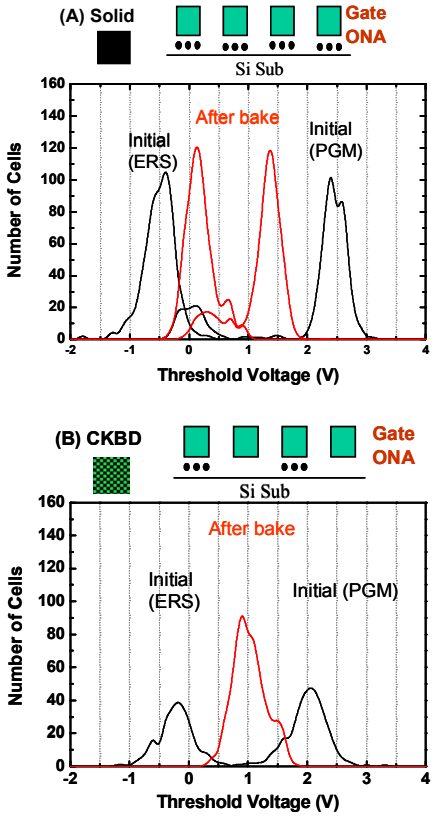
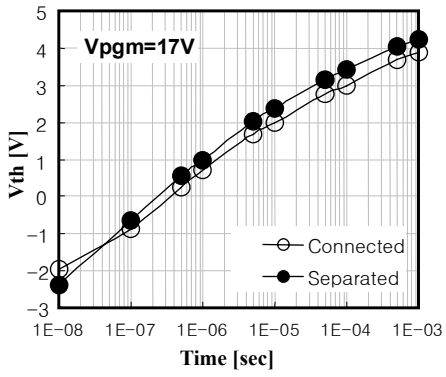


Fig.3. V_{TH} shift after bake at 200℃ and 2 hours for programmed and erased cells in solid (A) and check board (B) pattern in the case of "Connected" gate structure.

As shown in Fig. 4, two gate structures have similar program speed measured at Vpgm=17V while "Separated" shows 1V slower erase speed at 10ms of duration time and 19V of erase voltage than "Connected". Relatively slower erase speed of the "Separated" devices appears to come from the change of SiN composition during gate re-oxidation process since SiN layer of the "Separated" device have more probability to be oxidized during the re-oxidation process compared to the "Connected" ones. Although "Separated" device shows very similar program speed and a little slower erase speed compared to "Connected" one, V_{TH} window of the both structures are ~6V large enough for multi-level cell (MLC) operation.



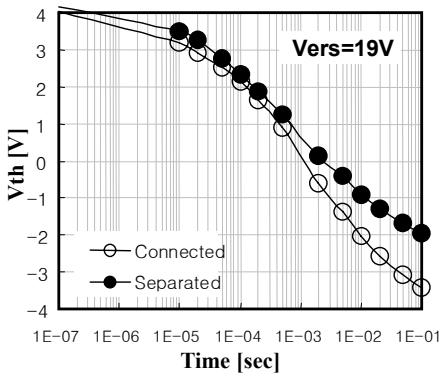


Fig.4. Comparison of program (top) and erase (bottom) speed between "Connected" and "Separated".

High temperature baking characteristics of the TANOS NAND cells with 16 Mb density were investigated for the "Separate" and "Connected" cases as shown in Fig. 5. "Separated" devices show approximately 2 times smaller shift from the initial V_{TH}'s after 200℃ baking for 2 hours compared to "Connected" ones. The suppression of charge loss in the "Separated" devices can be explained by a lateral charge spreading model depicted in Fig.6

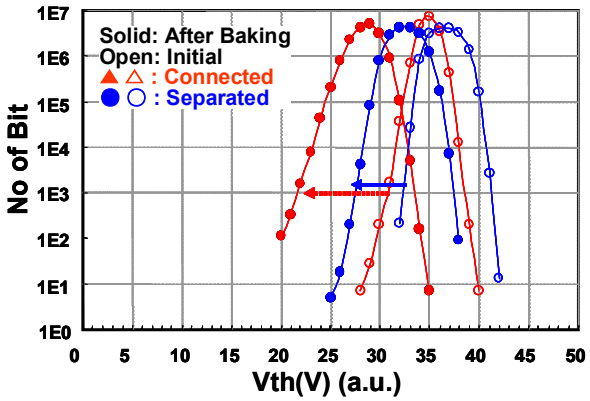


Fig.5. Comparison of high temperature baking (no program/erase cycling) characteristics between "Connected" and "Separated".

Holes injected to the trap layer on the channel region during the erase operation spread out to the trap layer extended on the source and drain region or field regions due to the relatively longer erase time (~10ms) and high diffusivity of holes [5]. The holes trapped in the SiN layer outside of channel area appear to remain after programming and aggravate the charge loss of the programmed cells.

Although charge migration from a programmed cell to an adjacent erased cell through the connected trap layers can be reduced in the "Separated" case, there still remains a probability of lateral spreading since the stored charge can be spread out to the SiN trap layers under a gate spacer regions. From this respect, charge loss can be alleviated by reducing the spacer length of "Separated" devices.

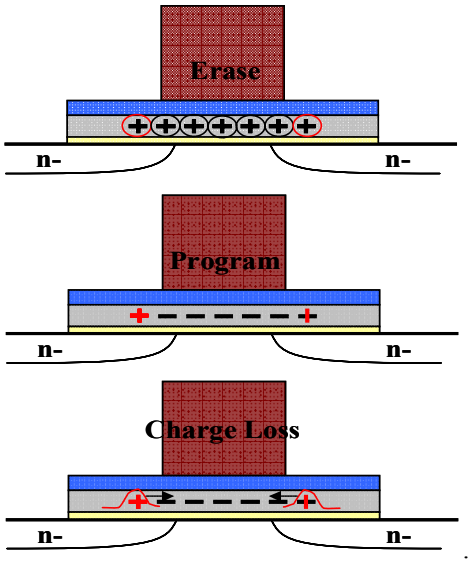


Fig.6. Schematics explaining lateral charge spreading.

To investigate the effects of the SiN trap layer extended outside of the channel area in the "Separated" devices, charge loss characteristics were measured for cells with different spacer length (Ls in Fig. 7) of 200Å and 130Å.

The spacer was formed by deposition of oxide layer and etch-back process. As shown in Fig.7, "Separated" device with a smaller spacer length (130Å) shows a ~20% reduced V_{TH} shift compared to a device with a longer spacer (200Å). This result supports the charge spreading model proposed in this article since smaller spacer length has a reduced chance for charges to spread laterally.

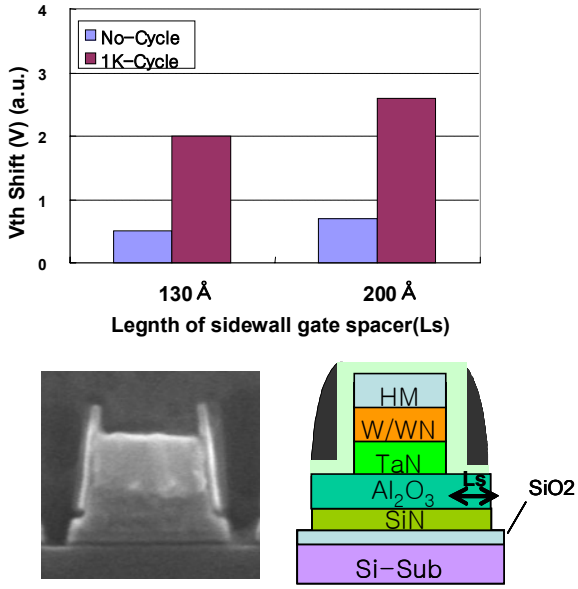


Fig.7. Dependence of V_{TH} shift on the gate spacer length which determines the SiN trap layer extended on the source and drain regions.

CONCLUSION

The gate structure with trap layers separated between different gate lines is desirable to suppress charge loss in the TANOS-NAND Flash devices since lateral charge spreading severely contributes to the charge retention of the devices. Charge spreading was suppressed as the gate spacer length decreased.

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