

## CMOS Analog VLSI Design

Natural

Can you think of a digital signal in the world?

World around you is analog.

Sound

Light

Color

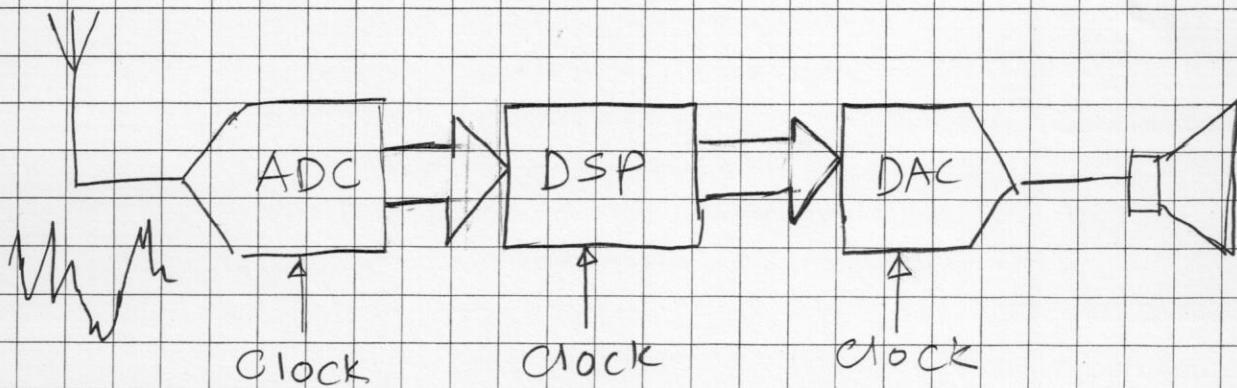
Signal processing in Analog is very difficult.

Digital Signal processing - Bits - Code.

— Repeatable — Reliable.

— Convert to digital as soon as possible

### Example



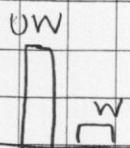
### Example - 2.4GHz WiFi

→ At least 10G clock frequency

→ Huge # of bits Needed to capture  
Strongest & weakest signal.

→ Impractical

## Analog Design



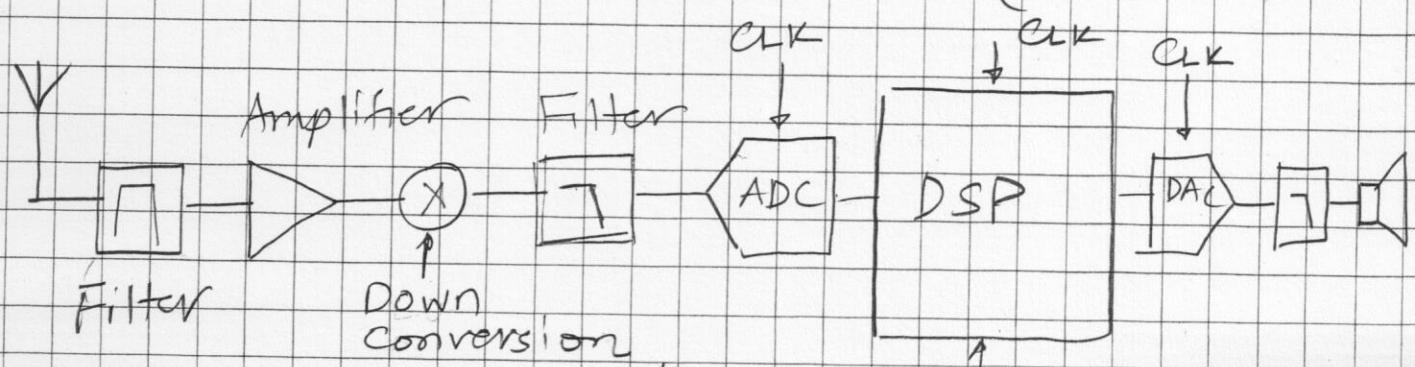
- Take continuous-time signal (from sensor)
- Remove unwanted signals.
- Sift out only desired signals.
- May be shift them to lower frequency
- Amplify and condition the signals.
- ADC with lowest sampling rate
  - Save power-area

Then DSP takes over

## On the Other Side

Take digital signal.

- Convert to analog
- Remove digital artifacts.
- Amplify / condition signal
- Drive speakers - other devices.  
(Actuators)

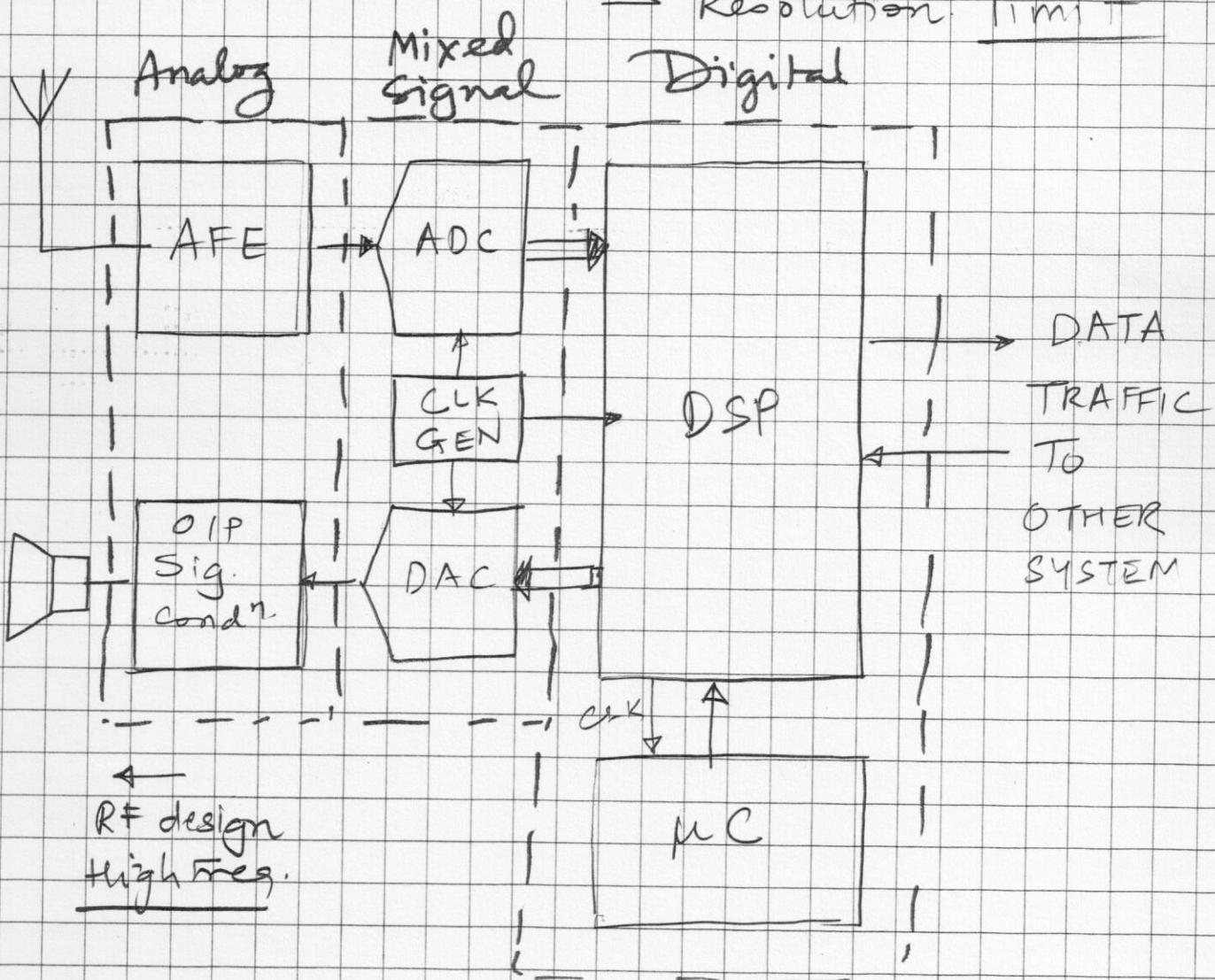


Analog TV example - Gradual Degradation of SNR

Digital TV - Near perfect picture till just it dies.

Analog signal - Susceptible to Noise

Digital signal - # of bits you process → Resolution limit



All together System-on-chip.

→ Implications Noise coupling

## ANALOG DESIGN CHALLENGES

- ① Device  $\xrightarrow[\text{LINEARITY}]{\text{NOISE}}$  Performance Degradation  
Feature size  $\rightarrow$  (Bad analog beh)
- ② Digital drives supply voltage downwards.  
 $\hookrightarrow$  Analog dynamic range ↓

③ Circuit complexity high . to make analog performance independent  $\left\{ \begin{array}{l} \text{PVT} \\ \text{process variations} \end{array} \right.$

$\xrightarrow{\text{Supply Voltage Variation}}$  Operating Temperature



④ 65nm Technology  $\rightarrow$  28nm Technology

Digital will scale - Automated to most extent

Analog Handcrafted artwork

$\rightarrow$  Redo

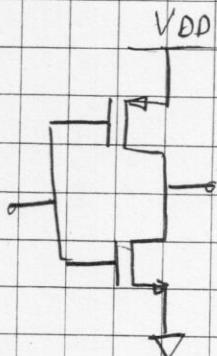
Analog-Mixed-Signal - RF designers always in high demand.

— commanding in job prospect

— Experience imm if you are good

## CMOS Technology

① Show crosssection here



### Main Driver

- 2 devices for inverter
- zero static power
- scalable (dimensions)
- minimum # of mask
- $V_{DD} \downarrow$  lower power  
 $CV^2f$

Bipolar - vertical devices - supersmall base width region  
superfast - HF

$$V_{BE} = 0.7V$$

$$V_{DD} = \sim 2V \text{ min}$$

CMOS - action happens laterally - gate length

- slower compared to Bipolar.

- with scaling  $L_{min} 28\text{nm} - \text{going down to } 5\text{nm}$

- speed matches Bipolars.  $f_T 100\text{GHz} +$

- analog performance of transistors suffers with scaling

- Digital free - use to compensate analog ckt imperfections.

$V_{DD} \downarrow$   
lower power designs

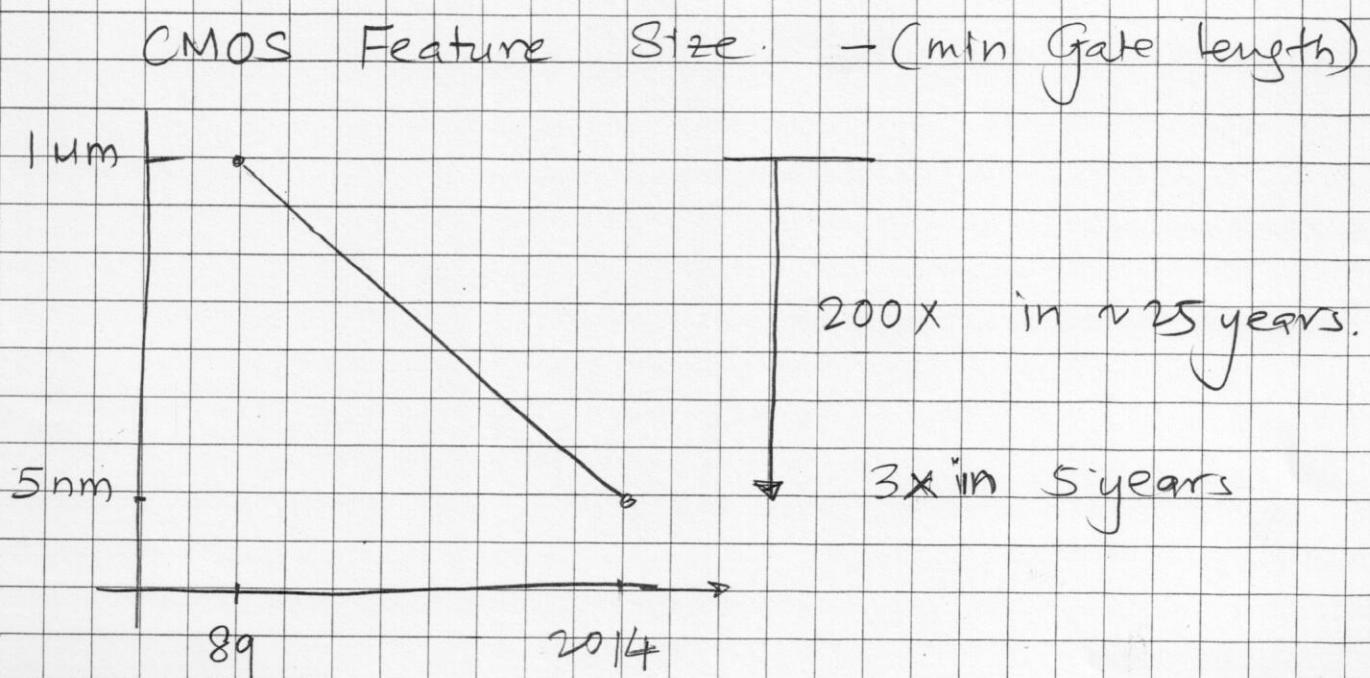
Analog + digital integration advantage.



→ process complexity

→ Models accuracy

→ supply voltage. - challenge to do HV design



As Analog Girl / Guy

- Creativity must to solve tough problems due to reducing supply voltage & transistor dimensions
- In SOC (System-on-chip) - Sensitive Analog must co-exist with very Noisy digital.
  - Noise insensitive architecture (diff ckt)
  - Effect of Substrate / bondwire / magnetic coupling
  - Effect of Packaging - must take into account at beginning
  - Floorplanning, very important

Analog parts - often run on high voltage

→ Device reliability - Important

- Device modeling
- Layout dependent effects.

Transistor matching

Layout parasitics

Electro-migration in metals

A lot of Neurons

EFForts

$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3}$
Schematic design	Layout effects	Measurement & debug

SHOW & TELL

—

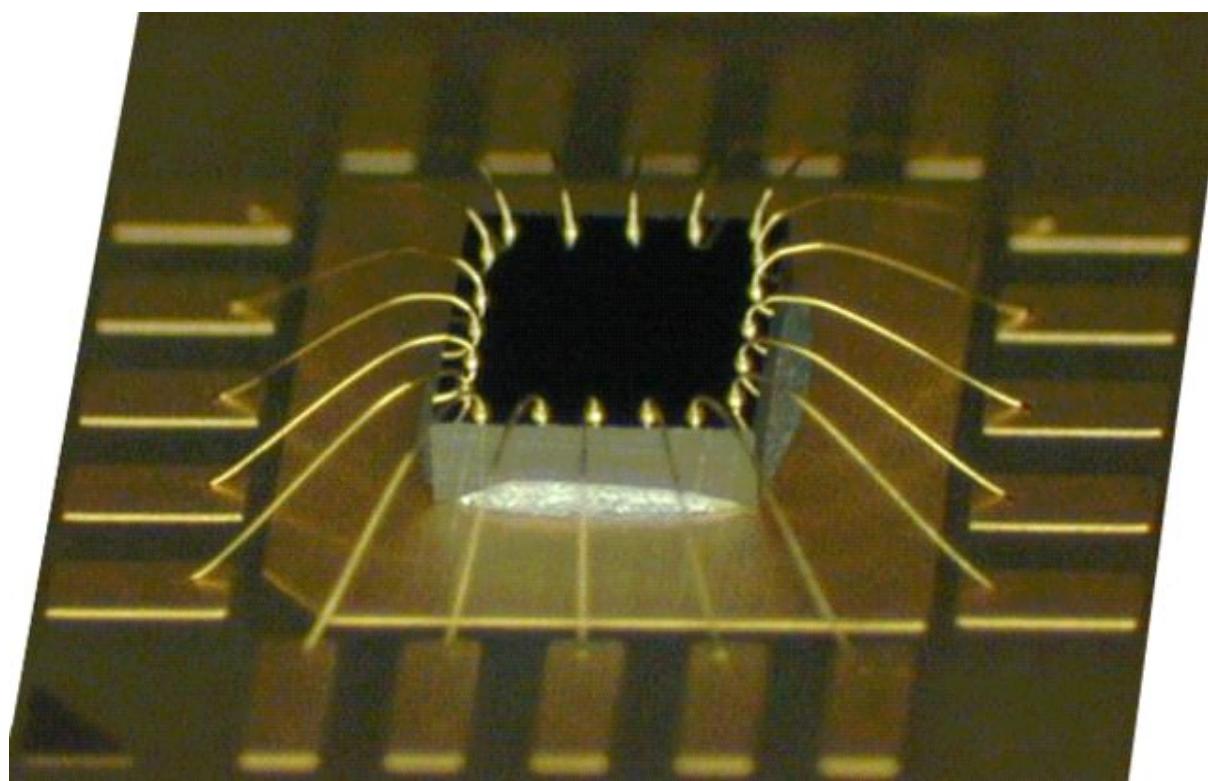
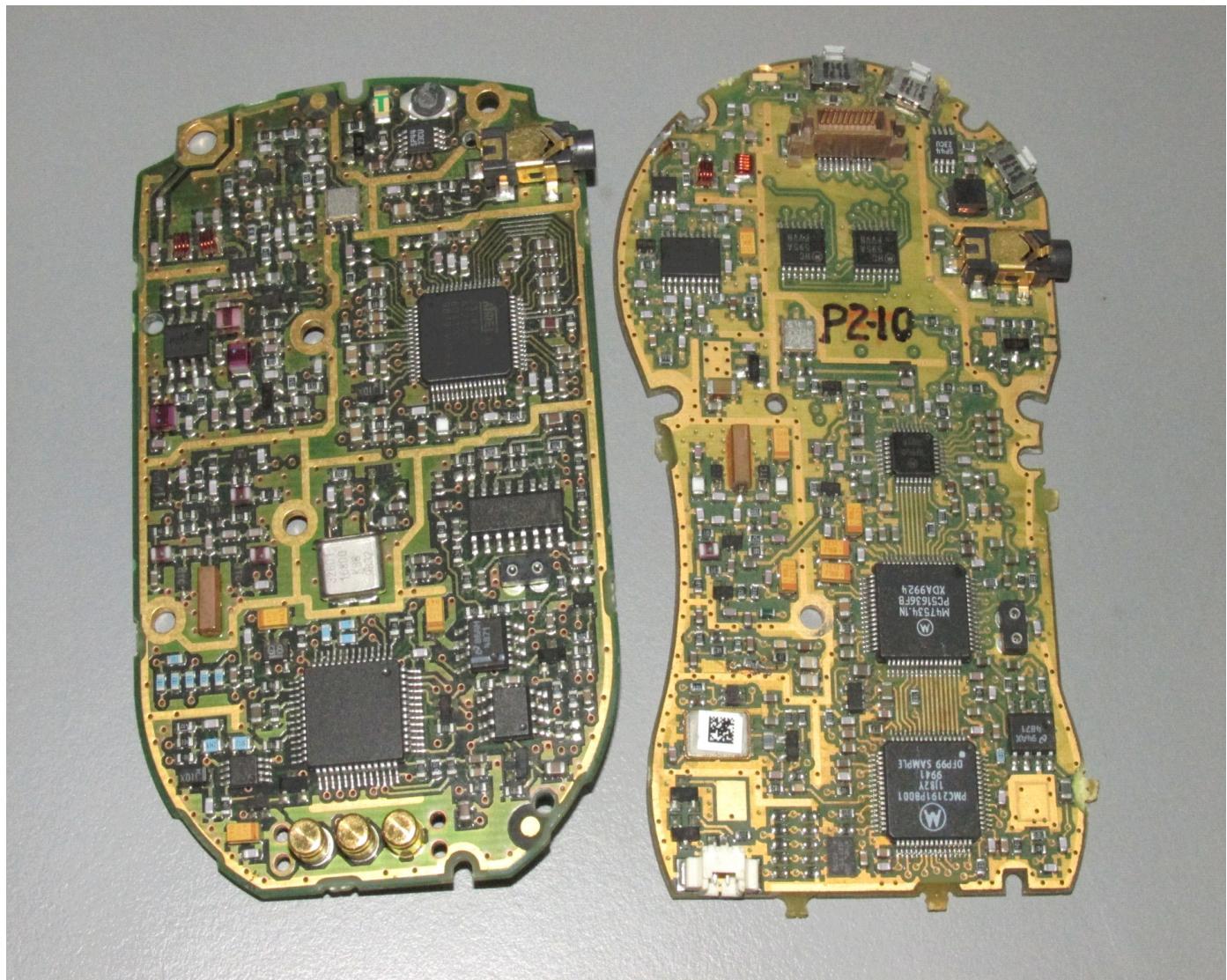
TEXT BOOK

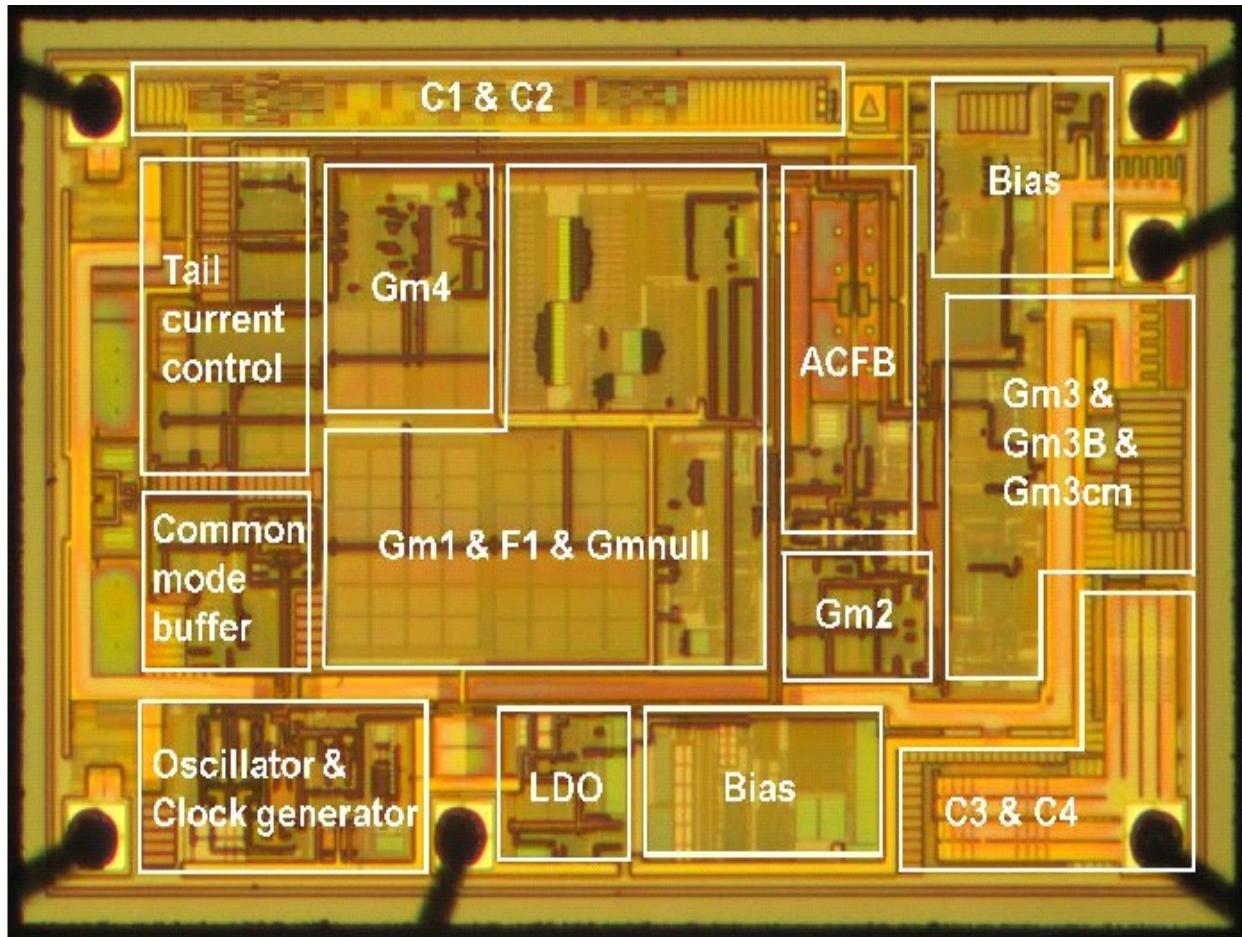
- Design of Analog CMOS ICs

— B. Razavi

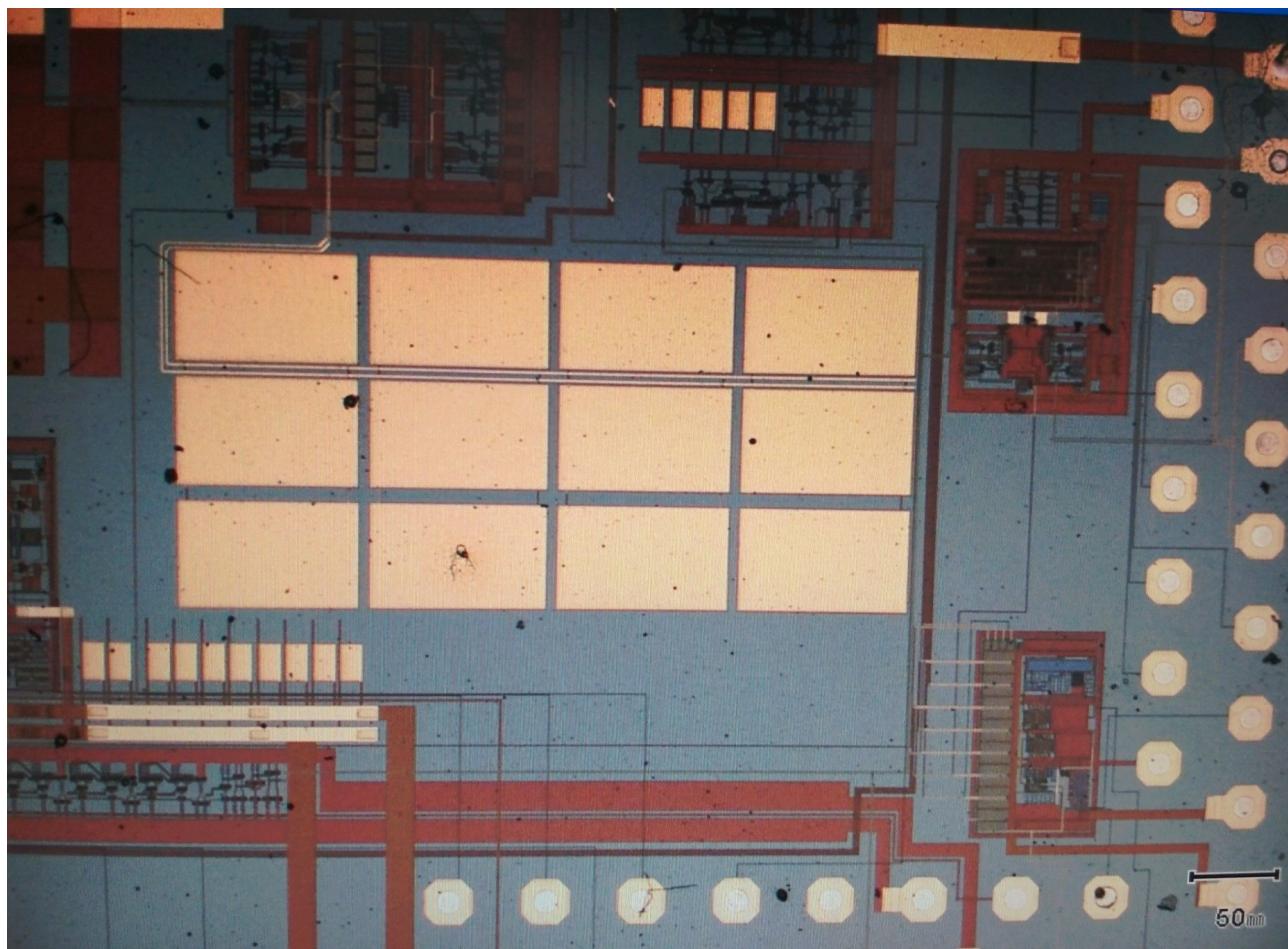
(1st or 2nd Edition)

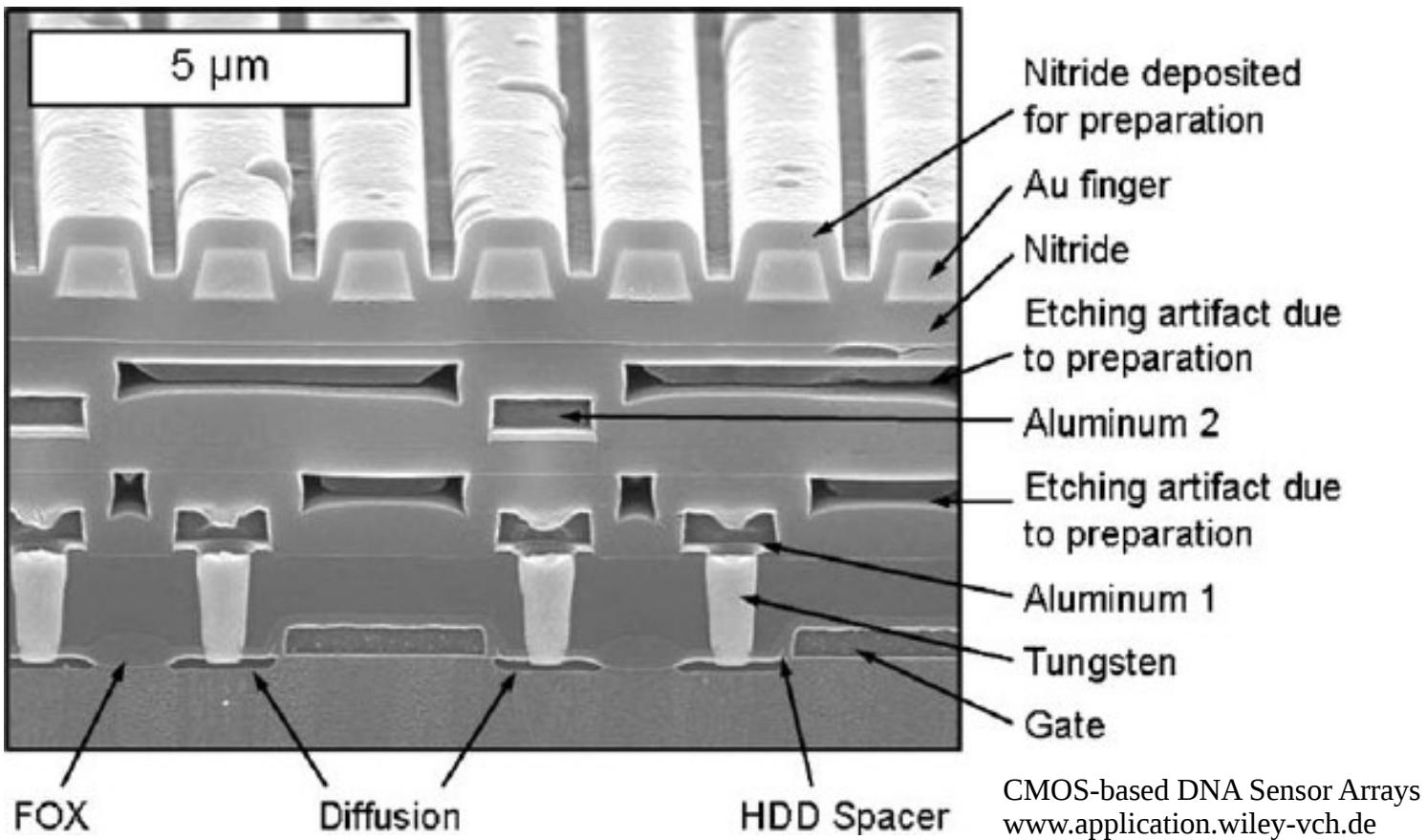
- Various papers for specific topics.





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CMOS-based DNA Sensor Arrays  
[www.application.wiley-vch.de](http://www.application.wiley-vch.de)

