# Logic Design Styles

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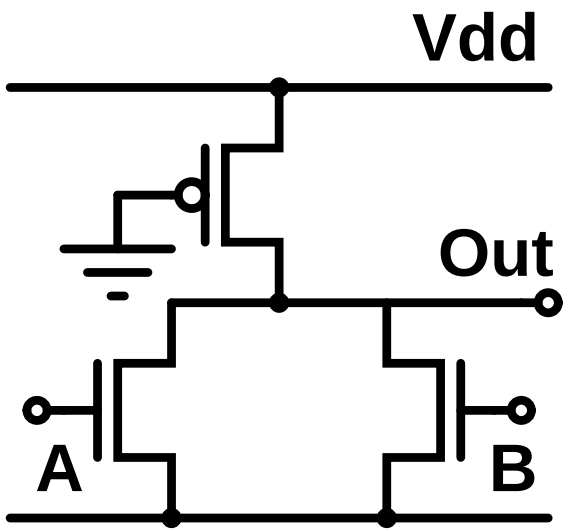
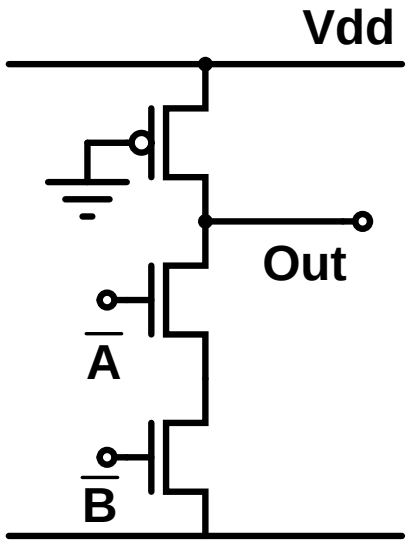
July 26, 2016

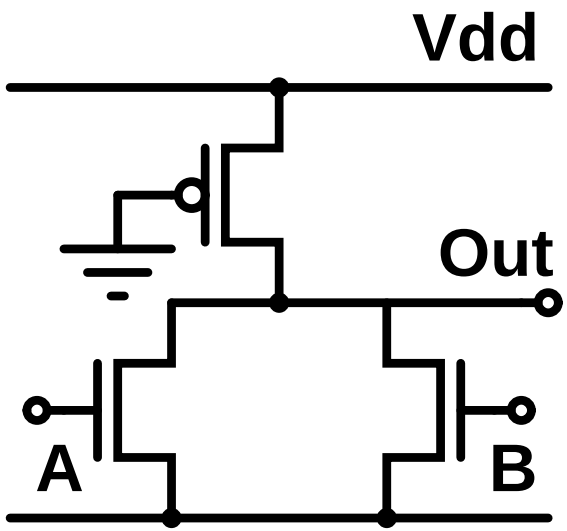
# Improving Pseudo nMOS

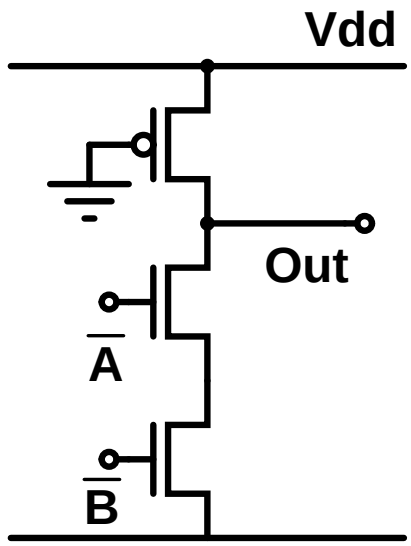



- In the pseudo-nMOS NOR circuit on the left, static power is consumed when the output is 'LOW'
- We would like to turn the pMOS off when A OR B is TRUE.
- The OR logic can be constructed by using a Pseudo-nMOS NAND of $\overline{A}$ and $\overline{B}$ as in the circuit on the right.
- But then what about the pMOS drive of this circuit?

# Improving Pseudo nMOS

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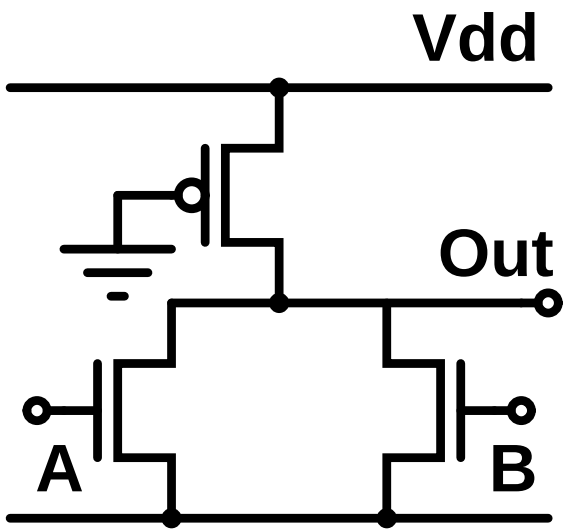
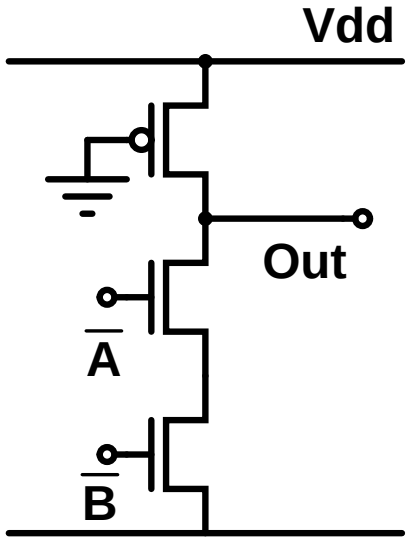
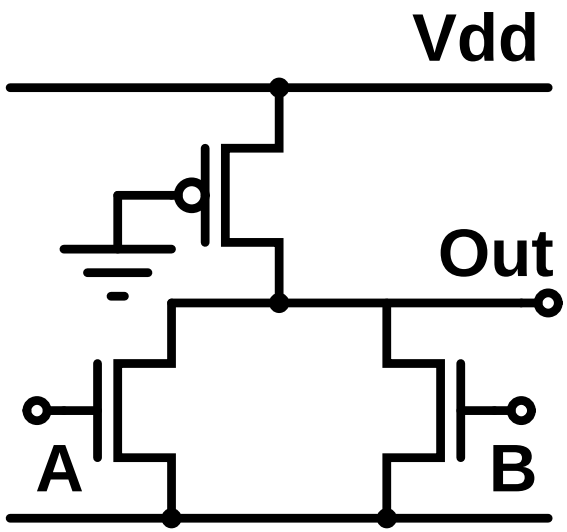
# Pseudo nMOS without Static Power

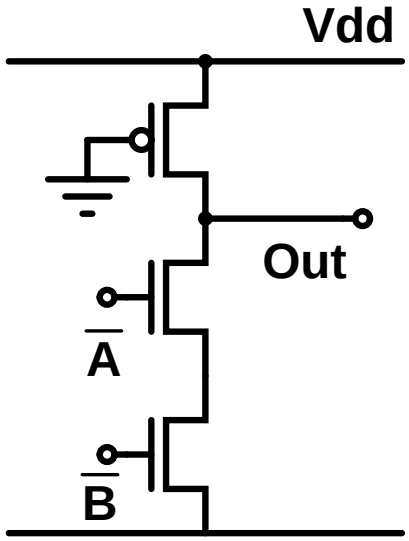



- The output of the circuit on the right is 'LOW' when both $\overline{A}$ and $\overline{B}$ are 'HIGH' (A = B = 0).
- We would like to turn *its* pMOS off when NOR of A and B is 'TRUE'
- But this can be provided by the circuit on the left!
- So the two circuits can drive each other's pMOS transistors and avoid static power consumption.

# Pseudo nMOS without Static Power

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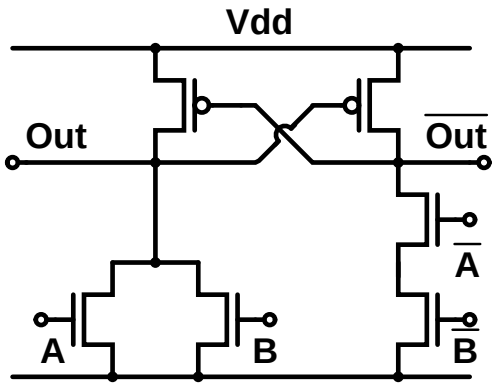
# Cascade Voltage Switch Logic




This kind of logic is called Cascade Voltage Switch Logic (CVSL).
It can use any network $f$ and its complementary network $\overline{f}$ in the two cross-coupled branches.

- Like CMOS static logic, there is no static power consumption.
- Like CPL, this logic requires both True and Complement signals. It also provides both True and complement outputs. (Dual Rail Logic).
- Like pseudo nMOS, the inputs present a single transistor load to the driving stage.
- The circuit is self latching. This reduces ratioing requirements.