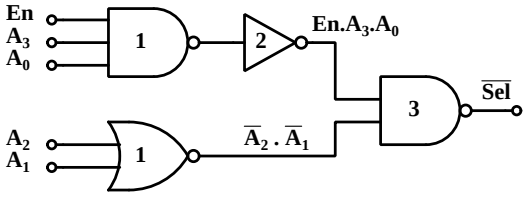
Solution to Midsem question paper for EE 671: VLSI Design, Autumn Semester 2017

Q–1 A 4 bit decoder needs to be designed using 4 phase dynamic logic. Inputs to the decoder are an Enable signal En and a 4 bit address $A_3A_2A_1A_0$. These input signals are valid only in phase $\phi 1$. (Complemented address bits are not available and should be generated when required). Design a decoding circuit which will produce an output signal $\overline{\text{Sel}}$ which becomes '0' only when En is '1' and the address bits have the value '1001'. The output should be available in as early a phase as possible. You are allowed to use only NAND, NOR and Inverter circuits with a maximum of 3 logic inputs (not counting clock). Give the logic diagram and the 'type' of each gate which specifies in which phase it evaluates.
(Slow and unnecessarily complex circuits will get no credit).

Soln.: We need to decode $\overline{En \cdot A_3 \cdot \overline{A_2} \cdot \overline{A_1} \cdot A_0}$.
To do as much work as possible in phase $\phi 1$ itself, we can feed En, A_3 and A_0 to a 3 input NAND and A_2 and A_1 to a 2 input NOR gate. The output of the 3 input NAND is valid in phases $\phi 2$ and $\phi 3$. This output can be inverted in phase $\phi 2$, so that $En \cdot A_3 \cdot A_0$ is available in phases $\phi 3$ and $\phi 4$.

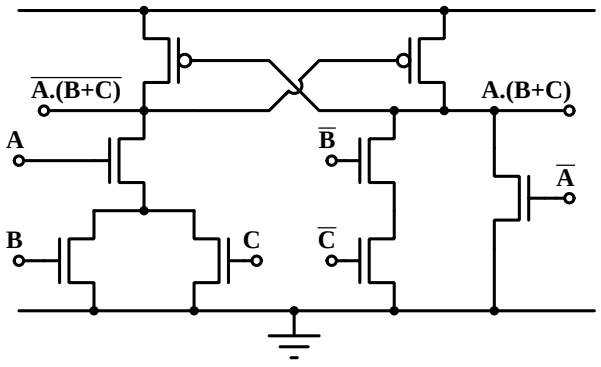
The output of the 2 input NOR gate is $\overline{A_2} \cdot \overline{A_1}$, valid in phases $\phi 2$ and $\phi 3$. Thus we have two intermediate products which are both valid in phase $\phi 3$. These can be combined with a 2-input NAND gate of type 3 to produce the desired $\overline{Sel}$ output.



– **[Q1: 2 marks]**

Q–2 Give the transistor level circuit diagram of a static Cascade Voltage Switch logic (CVSL) gate which implements the logic function $A.(B+C)$ and its complement, given A, B, C and their complements as inputs. How does this logic style avoid static current when the output is '0' while still needing to drive mostly n type transistors?

Soln.: The figure below shows the logic function $A.(B+C)$ implemented in CVSL logic style.



– **P.T.O.**

The nMOS network on the left is ON and pulls the left side output low when $A = 1$ AND either B or C or both are 1. Thus the left side output is $\overline{A.(B + C)}$ provided the pMOS load is 'ON' when $\overline{A.(B + C)}$ is '0'.

Similarly, the right side nMOS network is ON and will pull the right side output low when either $\overline{A} = 1$ or $\overline{B}$ as well as $\overline{C}$ are '1'. Thus the right side output is $\overline{\overline{A} + \overline{B} \cdot \overline{C}} = A.(B + C)$ provided the right side pMOS is on when $A.(B + C)$ is '1'

Whenever $A.(B + C) = 1$, the nMOS transistors on the left side pull the output LOW, turning the pMOS on the right ON as required. At the same time, the nMOS switch combination on the right is OFF and the right side output is '1', which turns the left side pMOS OFF.

Whenever $A.(B+C) = 0$, $\overline{A}+\overline{B}\cdot\overline{C} = 1$. This turns on the nMOS swich network on the right, pulling this output low. A low output on the right turns on the pMOS transistor on the left. At the same time, the nMOS switch combination on the left is OFF, and hence the left output is '1'.

Thre is no static power consumption in either state because the nMOS switch combinations and their pMOS loads are complementary. When $A.(B + C) = 1$, the left nMOS switch combination is ON, but its pMOS is OFF. At the same time, since $\overline{A}+\overline{B}\cdot\overline{C} = 0$, the nMOS combination on the right is OFF, while its pMOS is ON.

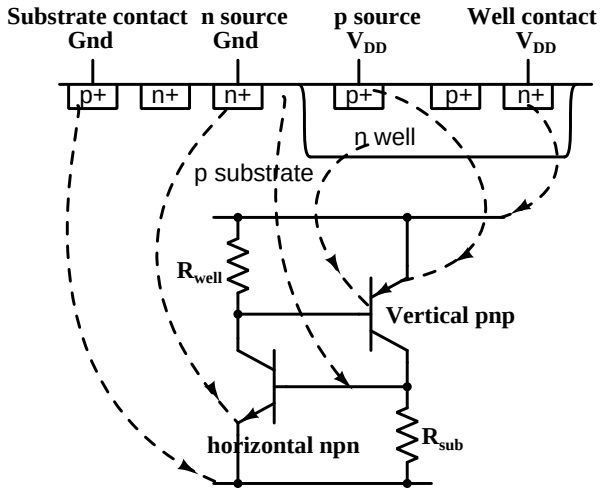
When $A.(B+C) = 0$, $\overline{A}+\overline{B}\cdot\overline{C} = 1$ and the right side nMOS switch combination is ON, but its pMOS is OFF. At the same time, since $A.(B + C) = 0$, the nMOS combination on the left is OFF, while its pMOS is ON.

In this way, even though we are driving only nMOS transistors, there is no static power consumption unlike the case for pseudo nMOS logic. – **[Q2: 2 marks]**

Q–3 Show how latch up occurs in CMOS circuits. Give a cross section diagram and the equivalent circuit, showing the correspondence between the regions in the cross section and the nodes of the equivalent circuit.

What are the suggested methods for avoiding latch up in the process (doping profile) and layout (design rules).

Soln.: The figure below shows a cross section of a CMOS circuit and the parasitic bipolar transistors which form the latchup structure.



The vertical pnp transistor is formed by the p+ source of a pMOS transistor connected to V_{DD} (which becomes the emitter), the n well (which becomes the base) and the p substrate (which becomes the collector of this transistor). The n well is connected to V_{DD} through a resistive path, which represents the resistance of the n well to the well contact.

The horizontal npn transistor is formed by the n+ source of an nMOS transistor connected to ground (which becomes the emitter), the p substrate, (which becomes the base) and the n well, (which becomes the collector).

Since the collector of the npn and the base of the pnp are both formed by the n well, these two are connected. Similarly, the collector of the pnp and the base of the npn are formed by the p substrate, so these are connected too.

Looking at the equivalent circuit, one can see that it forms a positive feedback system. An increase in the base current of the pnp will be amplified by its β_p and a large part of it will flow through the base emitter junction of the npn transistor. This part will be amplified by the β_n of the npn and a substantial part of it will go through the base emitter junction of the pnp. If the product of the two amplification factors β_p and β_n and the current division ratios between the resistors and the base emitter junctions exceeds 1, the currents will keep increasing due to this feedback, till there is a dead short between V_{DD} and ground. This is called latch up.

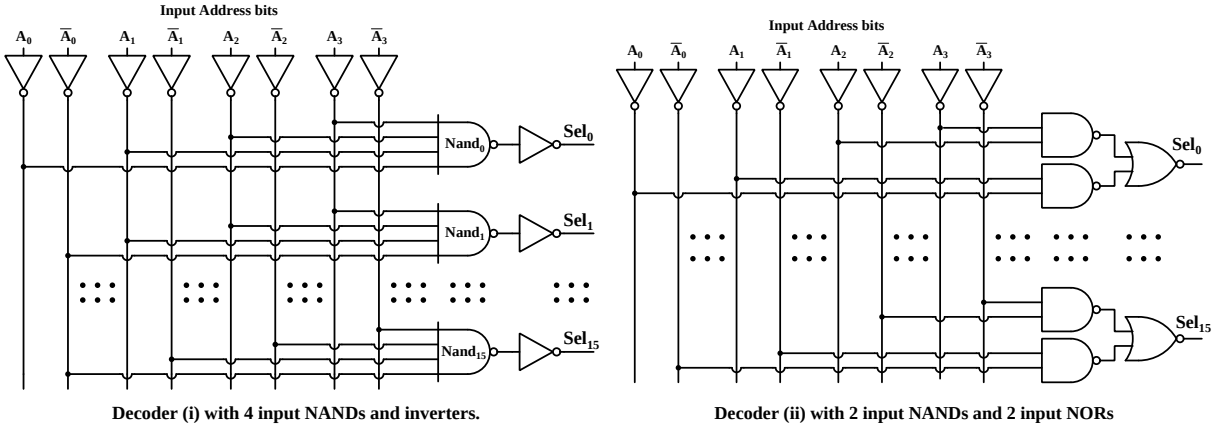
To prevent latch up, we must reduce the β of the parasitic bipolar transistors and make sure that most of the collector current of either transistor is directed to the resistor and not to the base-emitter junction of the other transistor. This can be done through process steps as well as through design rules.

1. The doping gradient of the n well should be made retrograde. (Doping should increase as we go deeper). This kills the current gain β_p of the pnp transistor.
2. The n well should have a guard ring connected to V_{DD}, which will collect any current which could form the base current of the pnp.
3. In layout, substrate and well contacts should be placed frequently, to reduce the value of R_{well} and $R_{substrate}$.
4. n channel transistors should be placed far from the edge of the n well. This increase the base width of the npn transistor and kills its current gain.
5. p channel transistors should also be placed far from the well edge and the p well should be deep to kill the gain of the npn transistor.

– **[Q3: 3 marks]**

Q–4 For a given CMOS process, the mobility correction factor γ for PMOS transistor widths is 2.5. The parasitic delay of gates may be taken to be proportional to the sum of the widths of transistors directly connected to the output terminal in a minimum sized gate. The parasitic delay of an inverter (p_{inv}) is 2 in units of τ, the propagation delay of a minimum sized inverter driving another minimum sized inverter without including the parasitic delay.

We want to compare two circuits to implement a 4 to 16 decoder. In circuit (i), appropriate combinations of address bits and their complements are given to 4-input-NAND gates, and their outputs are connected to inverters. In circuit (ii), combinations of address bits and their complements go to 2-input-NAND gates and their outputs are combined pair wise by 2-input-NOR gates to generate the select outputs as shown.



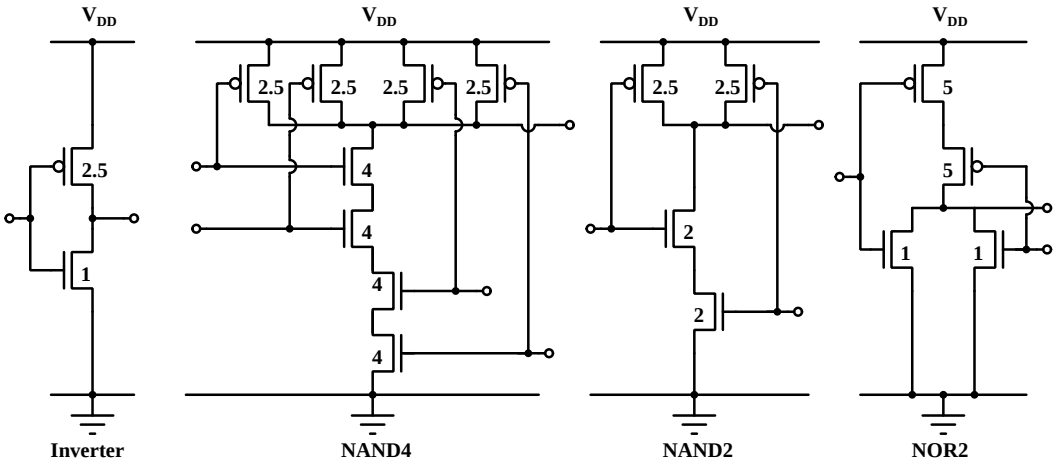
Decoder (i) with 4 input NANDs and inverters.

Decoder (ii) with 2 input NANDs and 2 input NORs

In both circuits, the inverters at the input are minimum sized and each select output is loaded with capacitance equivalent to 128 minimum sized inverters. All transistors use minimum channel length.

a) Compute the logical effort and parasitic delay for all the types of gates involved in the above circuits.

Soln.: The figure below shows the gates with transistor widths to be used for providing the same output drive as a minimum inverter.



In case of 4 input NAND, there are 4 n channel transistors in series. So each must be sized to 4 times the width of the n channel transistor used in the minimum inverter. 4 p channel transistors are in parallel, so each has the same size as the p

channel transistor in the minimum inverter – that is, 2.5 times the width of the n channel transistor in the minimum inverter.

Similarly, the 2 input NAND has two n channel transistors in series with a size of 2 and two p channel transistor with a size of 2.5 in parallel. The 2 input NOR has two n channel transistors in parallel, so each is the same size as the n channel transistor in the minimum inverter. The p channel transistors are in series, so each must be sized to 5.

The logical effort of an inverter is 1 by definition and its parasitic delay has been given to be 2. The logical effort for a gate is proportional to the input capacitance (and hence, total transistor width) connected to a given input. Therefore

$$g = \frac{1}{3.5} \times \text{sum of transistor widths connected to the input.}$$

The parasitic delay can be estimated to be proportional to the total transistor width connected to the output terminal. Therefore,

$$p = \frac{2}{3.5} \times \text{sum of transistor widths connected to the output}$$

This gives:

Gate	Width of n Trans.	Width of p Trans.	Total W at input	Total W at output	Logical Effort	Parasitic Delay
Inverter	1	2.5	3.5	3.5	1	2
4 input NAND	4	2.5	6.5	14	13/7	8
2 input NAND	2	2.5	4.5	7	9/7	4
2 input NOR	1	5	6	7	12/7	4

– **[1]**

b) Find the widths for n and p channel transistors in all the gates of both circuits to minimize the total delay. (Specify the widths in units of the width of the n channel transistor in a minimum inverter).

Soln.: Circuit (i) with NAND4 gates

The output of each input inverter goes to 8 NAND inputs. (There are 8 inverter outputs and 64 NAND inputs and these are equally divided). the logical effort g for 4-input-NAND gates is 13/7. Therefor the path effort for this circuit is given by

$$F = GBH = (1 \times \frac{13}{7} \times 1) \times 8 \times \frac{128}{1} = 1901.714$$

Since the circuit has 3 stages, the optimum stage effort is

$$\hat{f} = 1901.714^{1/3} = 12.38935$$

For the final inverters,

$$gbh = 1 \times 1 \times \frac{128}{C_{in}} = 12.38935, \quad \text{which gives} \quad C_{in} = 10.33146$$

For NAND gates with 4 inputs,

$$gbh = \frac{13}{7} \times 1 \times 10.33146/C_{in} = 12.38935, \quad \text{which gives} \quad C_{in} = 1.548668$$

For the input inverters,

$$gbh = 1 \times 8 \times 1.548668/C_{in} = 12.38935, \quad \text{which gives} \quad C_{in} = 1 \quad \text{as expected}$$

The final inverter is 10.33146 times the size of the minimum inverter. Therefore the n channel transistor width is 10.33146, while the p channel transistor width is $10.33146 \times 2.5 = 25.829$.

The input capacitance is in units of input capacitance of a minimum inverter. Thus, each capacitance unit represents 3.5 units of transistor width. The total transistor width at each input of the 4-input-NAND should be $3.5 \times 1.548668 = 5.420339$ width units. This width is divided in the ratio of $4 : 2.5$ between the n and p channel transistors. Therefore the n channel transistor width is $5.420339 \times 4/6.5 = 3.3356$ and the p channel transistor width is $5.420339 \times 2.5/6.5 = 2.0847$.

The input inverter is of course unit sized, and therefor n and p channel transistor widths are 1 and 2.5 respectively.

Circuit (ii) with NAND2 and NOR2 gates

The output of each input inverter again goes to 8 NAND inputs. (There are a total of 64 AND gate inputs fed by 8 inverter outputs and these are divided equally). Therefore the branch factor for the input inverters is 8 again.

The logical effort for 2-input-NAND gates is 9/7, while that for 2-input-NOR Gates is 12/7. Therefor the path effort for this circuit is given by

$$F = GBH = (1 \times \frac{9}{7} \times \frac{12}{7}) \times 8 \times \frac{128}{1} = 2256.98$$

Since the circuit has 3 stages, the optimum stage effort is

$$\hat{f} = 2256.98^{1/3} = 13.11724$$

For the last stage with NOR gates,

$$gbh = 127 \times 1 \times \frac{128}{C_{in}} = 13.11724 \quad \text{which gives} \quad C_{in} = 16.72825$$

For 2-input-NAND gates

$$gbh = \frac{9}{7} \times 1 \times 16.72825/C_{in} = 13.11724 \quad \text{which gives} \quad C_{in} = 1.639655$$

For the input inverters,

$$gbh = 1 \times 8 \times 1.639655/C_{in} = 13.11724 \quad \text{which gives} \quad C_{in} = 1 \quad \text{as expected}$$

Again, each capacitance unit represents 3.5 units of transistor width. Therefore the total input transistor width for NOR gates is $16.72825 \times 3.5 = 58.54889$. This is divided in the ratio 1 : 5 between n and p channel transistors. Therefore, n channel transistor width is $58.54889/6 = 9.758149$ and the p channel transistor width is $58.54889 \times 5/6 = 48.79074$.

The total input transistor width for 2-input-NAND gates is $1.639655 \times 3.5 = 5.738794$. This is divided in the ratio 2 : 2.5 between the n and p channel transistors. Therefore the n channel transistor width is $5.738794 \times 2/4.5 = 2.550574$ and the p channel transistor width is $5.738794 \times 2.5/4.5 = 3.188219$.

The input inverters are of course unit sized and so the n and p channel transistors have widths of 1 and 2.5 respectively.

The transistor sizes for all gates may be summarized as:

Circuit	gate	n width	p width
With NAND4	Input Inv.	1	2.5
	NAND 4	3.33	2.08
	Final Inv.	10.33	25.83
With NAND-NOR	Input Inv.	1	2.5
	NAND2	2.55	3.19
	NOR2	9.76	48.79

– [8]

c) Compute the total delay in units of τ for both circuits.

Soln.: In case of the first circuit, $\hat{f} = 12.39$. Therefore

$$D_{total} = 3\hat{f} + p_{inv} + p_{NAND4} + p_{inv} = 3 \times 12.39 + 2 + 8 + 2 = 49.17$$

For the second circuit, $\hat{f} = 13.12$. Therefore,

$$D_{total} = 3\hat{f} + p_{inv} + p_{NAND2} + p_{NOR2} = 3 \times 13.12 + 2 + 4 + 4 = 49.36$$

So the total delay is about the same in the two cases. – **[2]**

d) The optimum stage ratio ρ is a solution to the equation $\rho(1 - \ln \rho) + p_{inv} = 0$. Find the value of ρ and the optimum logic depth for the two decoders for the specified loading. What is the total delay for the two circuits if the logic depth is made optimum by adding inverters?

Soln.: p_{inv} is given to be 2. So the equation to be solved is:

$$f \equiv \rho - \rho \ln \rho + 2 = 0$$

We have

$$f' = 1 - \ln \rho - \rho \frac{1}{\rho} = -\ln \rho$$

Therefore given a guess g, the next improved guess is

$$g - \frac{f(g)}{f'(g)} = g + \frac{g - g \ln g + 2}{\ln g} = \frac{g + 2}{\ln g}$$

Starting with a guess value of 4, the successive guesses for ρ are: 4.328085, 4.319143, 4.319137, 4.319137 ....

Therefore the optimum number of stages is $\ln F / \ln \rho$.

For the circuit with NAND4, this is

$$\frac{\ln 1901.714}{\ln 4.319137} = 5.16$$

The optimum number of stages is 5, though one should also evaluate the delay for 6 stages to see which is better. The stage effort for a 5 stage design is $1901.714^{1/5} = 4.527193$. This design will add two additional inverters to the existing 2 inverters. So the parasitic delay will be $4p_{inv} + p_{NAND4} = 8 + 8 = 16$. Thus the total delay is $5 \times 4.527193 + 16 = 38.64$.

In case of a 6 stage design, 3 additional inverters will be inserted, so the parasitic delay will be $5p_{inv} + p_{NAND4} = 10 + 8 = 18$. The stage effort is $1901.714^{1/6} = 3.51985$ and so the total delay is $6 \times 3.51985 + 18 = 39.12$. Thus a 5 stage delay is optimum, with a total delay of 38.64.

For the circuits with NAND2 and NOR2, the optimum number of stages is

$$\frac{\ln 2256.98}{\ln 4.319137} = 5.28$$

Again, 5 stages should be optimum, though one should also evaluate the delay for 6 stages to see which is better. For a 5 stage design, two additional inverters will be inserted, so the parasitic delay will be $3 \times p_{inv} + p_{NAND2} + p_{NOR2} = 6 + 4 + 4 = 14$. The stage effort in this case is $2256.98^{1/5} = 4.684956$ and so the total delay is $5 \times 4.684956 + 14 = 37.42$.

For a six stage design, three inverters will be inserted, so the parasitic delay will be $4 \times p_{inv} + p_{NAND2} + p_{NOR2} = 8 + 4 + 4 = 16$. The stage effort is $2256.98^{1/6} = 3.621773$, so the total delay will be $6 \times 3.621773 + 16 = 37.73$.
In this case, the delay is about the same for a 5 stage or 6 stage design. However 5 stage design will be optimum because it has lower complexity (and marginally lower delay). – **[2]**

– **[Q3: 1 + 8 + 2 + 2 = 13 marks]**

Paper Ends