Modeling NAND Flash Memories for IC Design

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***Abstract*—In this letter, we present a compact model of NAND Flash memory strings for circuit simulation purposes. This model is modular and easy to be implemented, and its parameters can be extracted through a simple procedure. It allows accurate simulation of NAND Flash memories with a limited computational effort, taking into account capacitive coupling effects which will become extremely important in future technology generations. This model is a very valuable tool for IC designers to optimize NVM circuits, particularly in multilevel applications.**

***Index Terms*—Compact modeling, Flash memories, semiconductor devices.**

I. Introduction

THE INCREASE of NAND Flash memory market has been exponential in the last years, pushed by digital camera, MP3 player, and USB stick applications. In order to enable the designer's community to effectively explore optimized algorithms for read and program/erase (P/E) operations, an accurate Spice-like model is needed [1]. This becomes an indispensable requirement to design advanced multilevel memories, where the margins between different threshold voltage levels are very tight [2]. In addition, the continuous shrinking of NAND memory sizes enhances the capacitance coupling between adjacent cells, significantly increasing the lateral fringing field disturbing NAND operations [3]. Three-dimensional TCAD simulations show that threshold voltage shift (ΔV_T) induced by adjacent cells on the same bitline (BL) and wordline (WL) increases exponentially with technology scaling, tripling moving from the 57- to the 32-nm technology node. Therefore, effects due to adjacent cell capacitive coupling must be properly taken into account for a robust and accurate design, strongly motivating this work.

In this scenario, we present in this letter a compact model of a NAND string suitable for circuit simulations of present and future Flash memory generations. We focused on a simple parameter extraction procedure, which is crucial to make the model application easy. The basic structure of the model, along with its parameter extraction procedure, is described in Section II. Results are presented in Section III.

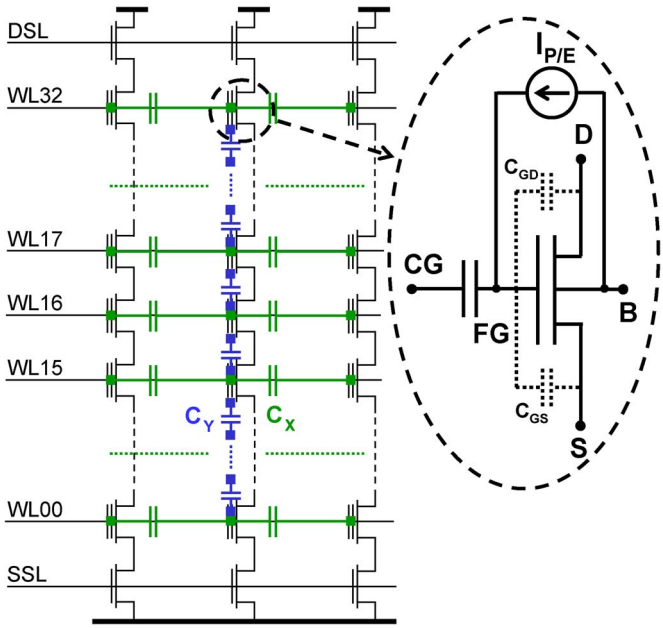

Fig. 1. Schematic of the basic structure of NAND Flash string macromodel. Notice the coupling capacitance between adjacent cells in the same WL (C_X) and BL (C_Y). The explosion shows the description of a single cell in terms of the equivalent transistor, ONO capacitor (C_{PP}), parasitic capacitances, and voltage-controlled current source for the P/E operations. C_{GS} and C_{GD} are bias independent FGs to source and drain capacitances, respectively, included into the BSIM 3v3.2 transistor model.

II. Compact Model

NAND Flash memories are organized in strings of 32 cells, connected by two selector transistors to drain (DSL) and source (SSL) lines. The building block of the macromodel we proposed in order to reproduce real device behavior is shown in Fig. 1. This is comprised of three strings. The central string is the one to be analyzed, whereas the two lateral ones are inserted to account for coupling capacitive effects. Each cell is composed of a stacked oxide/nitride/oxide (ONO) capacitor and an equivalent transistor, as shown in Fig. 1. Capacitive coupling effects are taken into account by an array of capacitors modeling the floating gate (FG) couplings to adjacent cells on the same WLs and BLs (C_X and C_Y, respectively, in Fig. 1). To model P/E operations, some voltage-controlled current sources can be inserted between FG and S, B, and D nodes to model tunneling currents flowing through the bottom oxide during program and erase operations [4].

For the compact model to be effective and easy to use, we developed a simple parameter extraction procedure to extract

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model parameters. This procedure is comprised of two steps, which allows one to derive both cell and selector parameters, and cell and coupling capacitances.

The first step of the parameter extraction procedure is the calculation of coupling (C_X and C_Y) and cell (C_{PP}, C_{GS}, and C_{GD}) capacitances through 3-D TCAD simulations (see Fig. 1). We obtained geometry and doping information from process simulations, SEM/TEM measurements, and SIMS doping profiles. The coupling and cell capacitances are calculated, running ac device simulations. Noticeably, TCAD simulations are very effective in modeling geometry dependent electrostatic effects; hence, they allow the accurate calculation of capacitances in Flash memory strings [5]. In order to limit the computational effort requested by the numerical approach, coupling capacitances are calculated, considering a 3-D 3×3 cell structure to reproduce the whole NAND array behavior. This approach does not affect the accuracy of extracted capacitances, since coupling effects to both second neighbor and oblique cells are negligible for the technology nodes and cell morphologies we considered.

The second step of the procedure is dedicated to the extraction of the parameters of selector and equivalent cell transistors, which are standard parameters of BSIM 3v3.2 transistor model [6]. Differently from [6], where special test structures (i.e., strings of equivalent transistors) that are not anymore available in future technology nodes were required, we used here a string of standard memory cells, easing parameter extraction. Selector and equivalent cell transistor parameters are extracted by applying a modified BSIM 3v3.2 parameter extraction procedure. We considered the bias dependence of every MOSFET parameters except capacitances [6]. In fact, cell FGs cannot be accessed directly; hence, FG voltages (that are gate voltages of cell equivalent transistors) are calculated by simulating the whole string in ac conditions, considering coupling and cell capacitances estimated through TCAD simulations. Thus, we extracted the same initial set of model parameters for both selectors and equivalent cell transistors, considering the electrical characteristics measured on DSL, SSL, and the first, the sixteenth, and the thirty-second cells. Then, scaling dependent parameters have been adjusted, considering cell and selector channel lengths derived from SEM measurements. When measuring cell transistors and selectors, other cells within the string were erased and then biased at a relatively high voltage to lower their equivalent resistance due to channel and source/drain diffusions. This resistance has to be taken into account for an accurate parameter extraction, particularly considering the typically low channel and source/drain doping of NAND Flash memories.

III. Simulation Results

We performed several measurements to test the simulation capabilities of the developed NAND Flash model. Fig. 2 shows the measurements and simulations of transfer curves of both source and drain selector MOSFETs with the BL biased at reading conditions ($\sim$1 V). Simulations are performed under transient conditions to avoid using a voltage-controlled voltage source to force the FG node to its correct voltage in dc conditions as in [4], setting up the initial charge in the FG

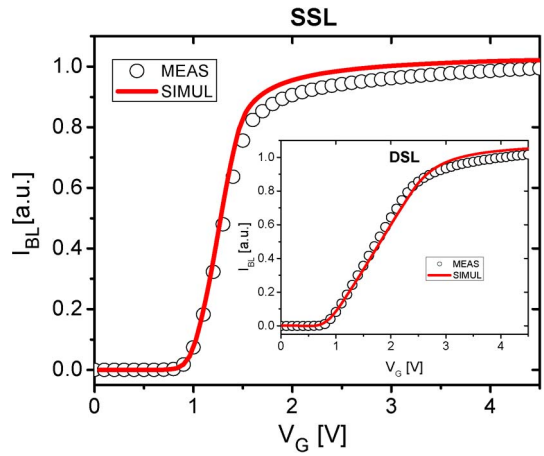

Fig. 2. Normalized transfer curves (symbols) measured and (solid lines) simulated on source (SSL) and drain (DSL) select transistors of a NAND Flash memory cell manufactured in 57-nm technology.

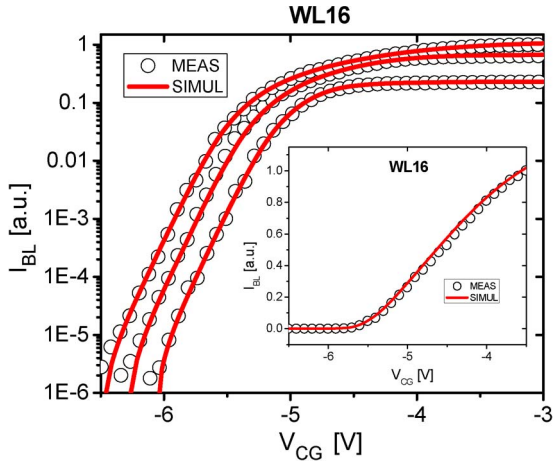

Fig. 3. Transfer curves (symbols) measured and (continuous lines) simulated on the sixteenth cell in the string manufactured in 57-nm technology with the gate of the other cells in the string biased at $\sim$5 V. The cell current normalized to its maximum saturation value is plotted in logarithmic scale considering three BL voltages (0.25, 0.75, and 1.25 V). The inset shows the transfer curve simulated and measured at the highest BL voltage, plotted in linear scale.

node. Measurements have been performed, biasing the cell gates at $\sim$5 V to minimize the effect of unselected cell channel resistance. As shown, the agreement between measurements is very good. Noticeably, the model also reproduces accurately the difference between the slopes of the linear portion of the transfer curves observed on source and drain selectors, ascribed to their different series resistances, i.e., to the position within the string.

Fig. 3 shows the transfer curves simulated and measured on the sixteenth cell of the string at three different BL voltages (0.25, 0.75, and 1.25 V), while biasing at 5 V the gates of other cells in the string. Interestingly, the model reproduces accurately the threshold voltage lowering observed when increasing the BL voltage, due to both DIBL effect and series resistance of cells in the string. The excellent agreement between measurements and simulations demonstrates the accuracy of the extraction procedure we proposed. The inset in Fig. 3 shows, in linear scale, the transfer curve measured and simulated at the higher BL voltage, which emphasizes the very good fitting

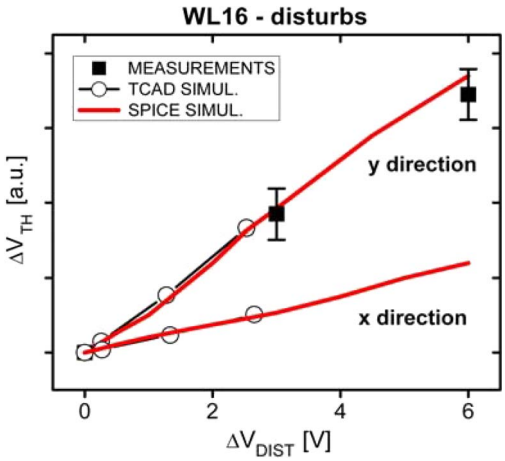

Fig. 4. (Full symbols) V_T shift measured on the sixteenth cell in the string manufactured in 5-nm technology as a function of the threshold voltage shift of the adjacent disturbing cell (ΔV_{DIST}) in the same BL (x-direction) and WL (y-direction; see the inset). Empty symbols represent TCAD simulation results, whereas the solid line represents the Spice simulation results obtained with the model we have developed. The V_T shift of the adjacent cell has been generated by reproducing the whole experiment: 1) the cell is read; 2) the adjacent cell is programmed; and 3) the original cell is read again.

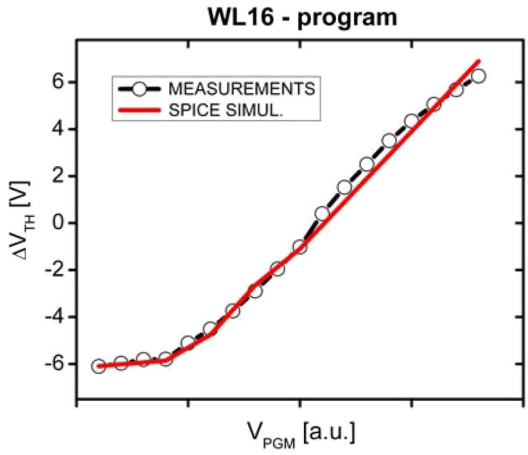

Fig. 5. Typical programming curve showing the cell threshold voltage shift (ΔV_{TH}) measured and simulated on a 57-nm NAND memory cell plotted versus the increasing boxlike control gate programming pulse (V_{PGM}) with a fixed duration, while grounding the source, body, and drain.

obtained also at high current. Such a result demonstrates the accuracy of the coupling and interpoly capacitances calculated through TCAD simulations.

To demonstrate the model application to future Flash memory generations, we tested its capabilities to reproduce the crosstalk between adjacent cells. Fig. 4 shows the measured and simulated threshold voltage shift ΔV_{TH} of a cell in the string, due to capacitive coupling between adjacent FGs on the same BL (y-direction) and WL (x-direction). As shown, the model accurately reproduces both TCAD simulations and measurements, demonstrating that it is a valuable tool for circuit simulations of present and future NAND Flash memories, essential to optimize the program algorithms of multilevel design where sensing margins become a strong concern. At this regard, we want to emphasize that the model can also simulate threshold voltage shifts due to program and erase operations, provided that current sources modeling tunneling currents through the bottom oxide are inserted [4]. The bottom oxide field is calculated, neglecting charge quantization effects. Results shown in Fig. 5 show the accurate agreement between measurements and simulations of the threshold voltage shift occurring during the program of a 57-nm memory cell, proving that the model can be effectively used to test programming algorithms of future NAND Flash.

IV. Conclusion

We proposed a compact model of NAND Flash strings for circuit simulation purposes. The model correctly reproduces the electrical behavior of a NAND Flash string, taking correctly into account the capacitive coupling effects between adjacent cells. The model is modular and easy to implement, and its parameters can be extracted by following a straightforward procedure. This model provides a very valuable aid to design present- and next-generation multilevel NAND Flash memories.

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