

## REFERENCE CIRCUIT DESIGN.

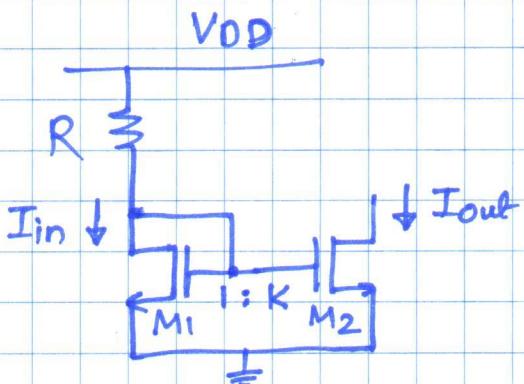
\* Voltage or Current Reference

\* Process, Temperature or Supply independent

\* Or. well-defined (predictable) dependence on Temp.

⇒ Goal - Overall Chip performance predictable / consistent over PVT. Yield. - Meet Specs over PVT.

### I. Supply Independent Current-source



$$\Delta I_{out} = K \frac{\Delta V_{DD}}{R + \frac{1}{g_m}}$$

$$I_{in} = \frac{V_{DD} - V_{GS}}{R}$$

$$\Delta I_{in} = \frac{\Delta V_{DD} - \Delta V_{GS}}{R}$$

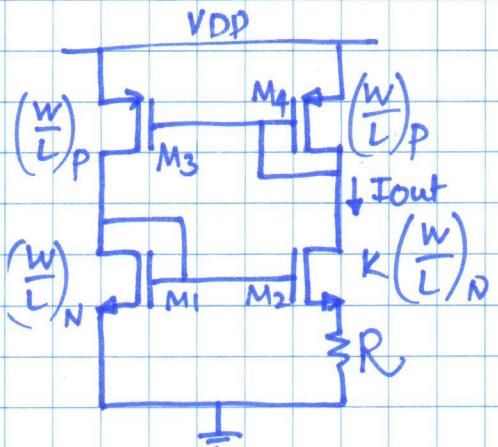
$$\Delta V_{GS1} = \frac{\Delta I_{in}}{g_{m1}}$$

$$\Delta I_{in} = \frac{\Delta V_{DD}}{R + \frac{1}{g_{m1}}}$$

No good.

I & hence VDD

Consider



$$V_{GS1} = V_{GS2} + I_{out} R$$

$$K_n = \mu_n C_{ox}$$

$$V_T + \sqrt{2 I_{out} \frac{1}{K_n (w/l)_N}} = V_T + \sqrt{\frac{2 I_{out}}{K_n K_n (w/l)_N}} + I_{out} R$$

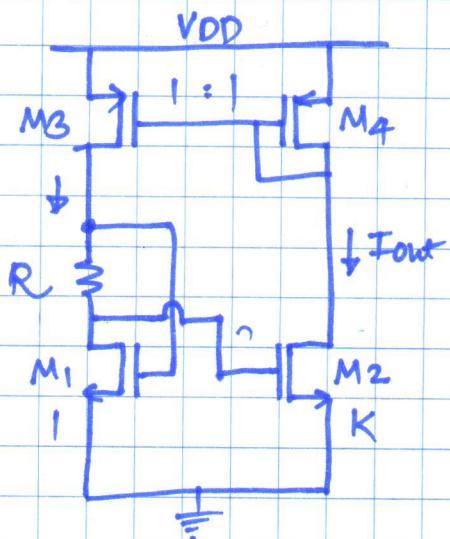
$$\sqrt{I_{out}} = \frac{1}{R} \left[ \sqrt{\frac{2}{K_n (w/l)_N}} \left( 1 - \frac{1}{\sqrt{K}} \right) \right]$$

$$I_{out} = \frac{1}{R^2} \cdot \frac{2}{K_n (w/l)_N} \left( 1 - \frac{1}{\sqrt{K}} \right)^2$$

→ indep of VDD - depends on process & T & R value.

⊕ Body effect of M2.

Improved circuit



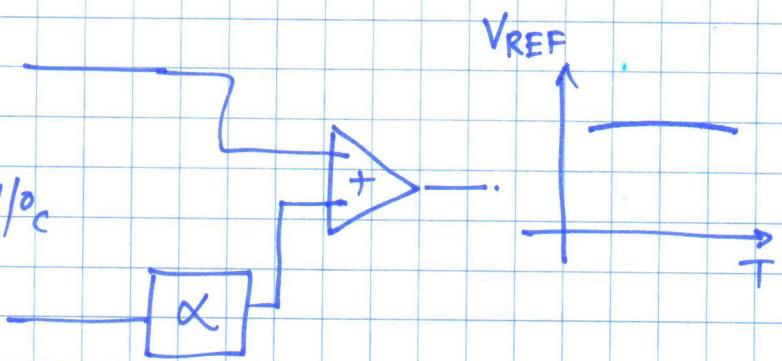
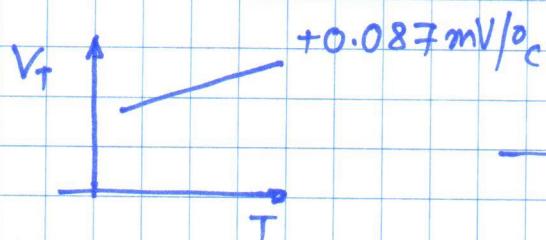
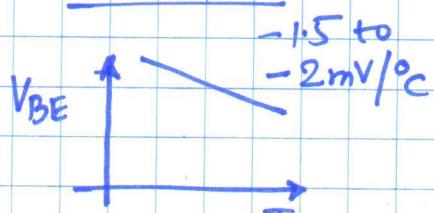
No Body effect for M<sub>2</sub>.

Same I<sub>out</sub> equation.

Use long channel devices to reduce Ch. length modulation.

### Temperature Independent Reference

Concept



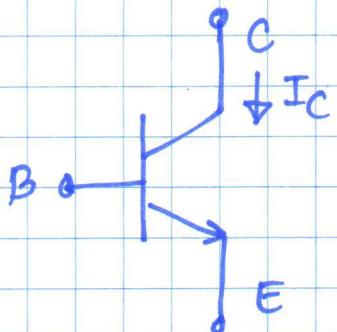
$$V_{\text{REF}} = V_{\text{BE}} + \alpha V_T$$

-ve Temp Co      +ve Temp Co  
Temp Co

→ Process, Supply & Temp Independent

→ Need to use Bipolar Transistors

## Bipolar Basics.



$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \quad \frac{kT}{q}$$

Saturation current  $\propto \mu k T n_i^2$

$$\mu k T n_i^2 \quad \text{(intrinsic carrier conc)} \quad \text{Bandgap} \rightarrow 1.12 \text{ eV}$$

mobility

$$\propto \mu_0 T^m \cdot 2^{-\frac{n}{2}} \left(\frac{3}{2}\right)$$

$$\propto T^3 \exp[-E_g/kT]$$

Overall  $I_S = b T^{4+m} \exp \frac{-E_g}{kT}$   
constant. indep. of  $T \uparrow$

$$V_{BE} = V_T \ln \left( \frac{I_C}{I_S} \right)$$

$$\frac{\partial V_{BE}}{\partial T} = \underbrace{\frac{\partial V_T}{\partial T} \cdot \ln \left( \frac{I_C}{I_S} \right)}_{\frac{V_{BE}}{T}} - \underbrace{\frac{V_T}{I_S} \frac{\partial I_S}{\partial T}}_{(4+m) \frac{V_T}{T} + \frac{E_g}{kT^2} V_T}$$

Simplification  
{  $I_C$  held constant }

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

Older Tech  $V_{BE} = 0.7 \text{ V}$   $T = 300^\circ \text{K}$   $\Rightarrow \frac{\partial V_{BE}}{\partial T} \approx -1.9 \text{ mV}/\text{K}$

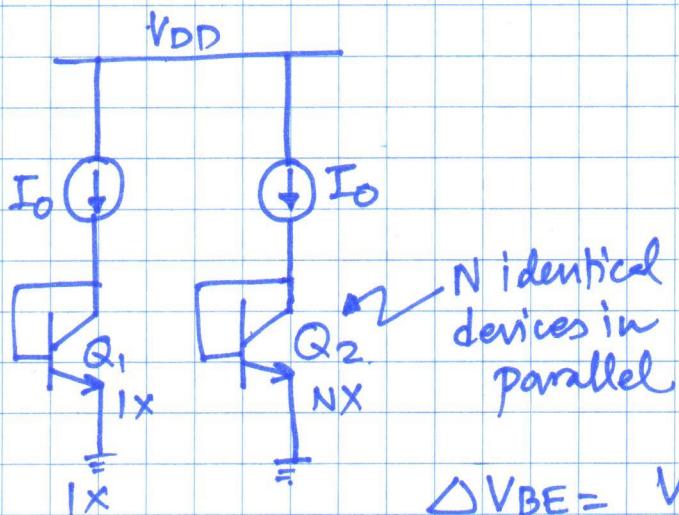
Modern Tech.  $V_{BE} = 0.8 \text{ V}$   $T = 300^\circ \text{K}$   $\Rightarrow \frac{\partial V_{BE}}{\partial T} \approx -1.5 \text{ mV}/\text{K}$

NOTE: If you take into account collector current var<sup>n</sup> ( $I_C = \frac{V_T \ln N}{R}$ ), then equation modified as  $(3+m)$  instead of  $(4+m)$  (Razavi pp.517)

How to generate the TC voltage?

PTAT Proportional to Absolute Temperature.

→ Hilbiber 1964



$$V_{BE1} = V_T \ln \left( \frac{I_o}{I_s} \right)$$

$$V_{BE2} = V_T \ln \left( \frac{I_o/N}{I_s} \right)$$

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= V_T \ln \left( \frac{I_o}{I_s} \right) - V_T \ln \left( \frac{I_o/N}{I_s} \right)$$

$$= V_T \ln(N) = \frac{kT}{q} \ln(N)$$

$k, q$  constants  $N \rightarrow$  scaling ratio

$\Delta V_{BE} \propto T$  indep of P.V.

$$V_{REF} = V_{BE} + \alpha V_T$$

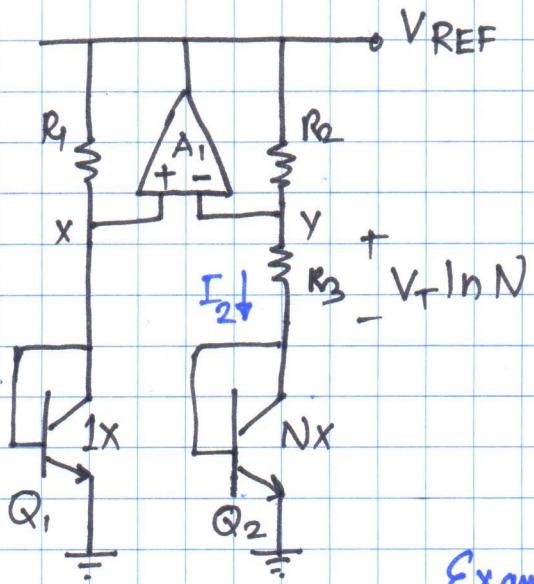
$$-1.5 \text{ mV}/^\circ\text{K} \quad 0.087 \text{ mV}/^\circ\text{K}$$

$$\alpha = 17.2$$

$$V_{REF} = 800 \text{ mV} + (17.2 \times 26 \text{ mV})$$

$$\approx 1.25 \text{ V} \quad (\text{nBandgap Voltage})$$

## Circuit Implementation

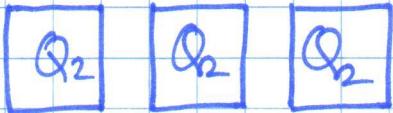


$$V_{REF} = (R_2 + R_3) I_2 + V_{BE}$$

$$= V_{BE} + (R_2 + R_3) \left( \frac{V_T \ln N}{R_3} \right)$$

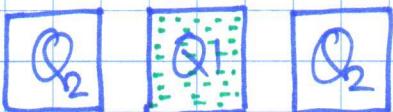
$$= V_{BE} + \left( 1 + \frac{R_2}{R_3} \right) V_T \ln n.$$

Example  $m = 8 \quad \frac{R_2}{R_3} = 7.3$

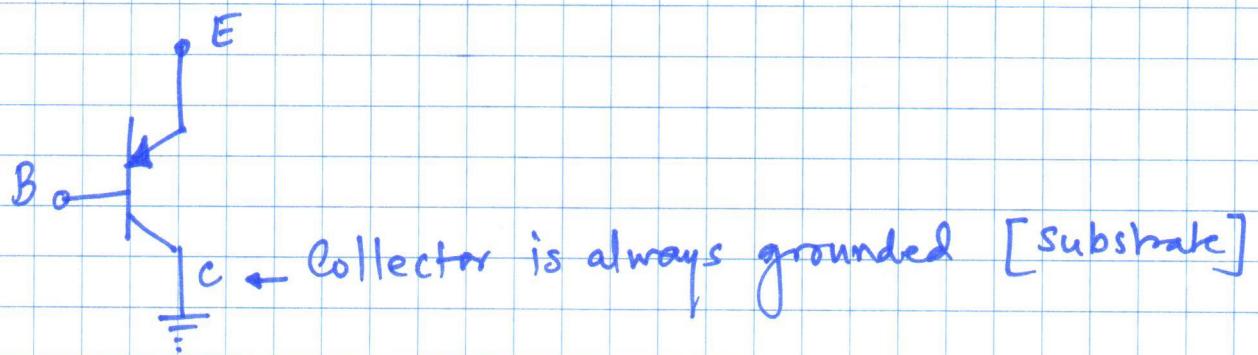
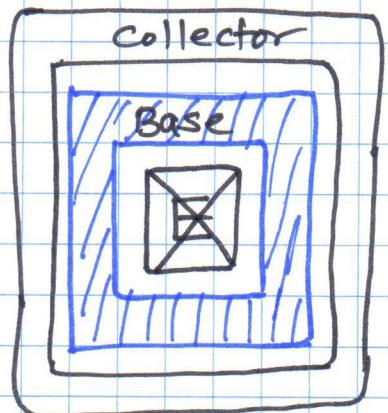
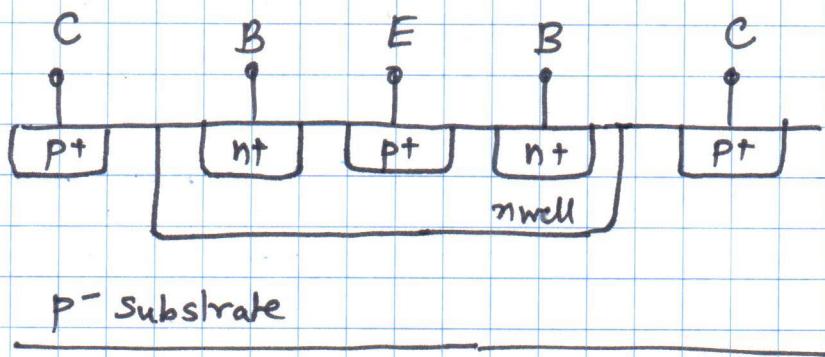


Common. Centroid layout

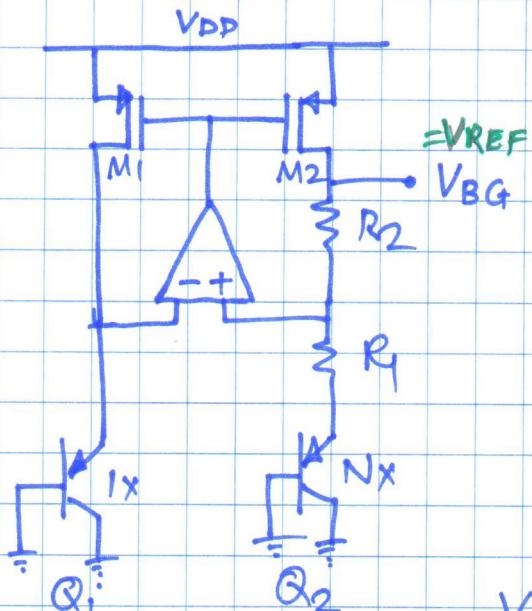
— matching between  $Q_1$  &  $Q_2$



## Bipolar Transistors in CMOS Technology



### CMOS implementation



$$V_{REF} = V_{BE} + \frac{2}{3} kT \ln N$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{2}{3} \frac{kT}{T} \ln N = 0$$

for flat response...

$$-\frac{2kT \ln N}{T} = \frac{V_{BE} - (4+m)V_T - Eg/q}{T}$$

$$\Rightarrow 2kT \ln N = (4+m)V_T + \frac{Eg}{q} - V_{BE}$$

$$V_{REF} = \frac{Eg}{q} + (4+m)V_T$$

$\mu$  Temp exponent

$$\text{as } T \rightarrow 0 \quad V_{REF} = \frac{Eg}{q} \quad (\text{Bandgap voltage})$$

Explain opamp +/- connection.