

VT Modeling In Nand Flash Memory

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16D070044**

PAPER REVIEWED

- A Behavioral Compact Model of 3D NAND Flash Memory. Author: Shubham Sahay and Dmitri Strukov
- Reviewing the Evolution of the nand Flash Technology. Author: Christian Monzio CoMpagnoni, Senior Member IEEE, akira goda, alessandro s. spinelli, Senior Member IEEE, peter Feeley, andrea I. laCaia, Fellow IEEE, and angelo VisConti, Member IEEE
- Modeling NAND Flash Memories for IC Design. Author: L. Larcher, A. Padovani, P. Pavan P. Fantini, A. Calderoni, A. Mauri, and A. Benvenuti
- Multi-Level NAND Flash Memory. Author: Chang-Hyun Lee, Jungdal Choi, Changseok Kang, Yoocheol Shin, Jang-Sik Lee, Jongsun Sel, Jaesung Sim, Sanghun Jeon, Byeong-In Choe, Dukwon Bae , Kitae Park, and Kinam Kim

Nand flash memory

- Nand flash memory is a type of non-volatile storage used to store large amount of data.
- Each transistor stores the information form of charge in the floating gate.
- The stored charges change the threshold voltage of the transistor.
- It has a vertical structures with orthogonal wordlines. It is more compact than nor memory.
- It has basically three operations: Program, read and erase.
- **Program:** To program the nand flash memory uses Fowler–Nordheim tunnelings. High voltage is applied at WL with substrate grounded. This creates electric field and electron tunnel to the floating gate. This changes the V_t of that transistor.
- **Read:** We apply V_{rx} in the word line of the selected row and V_{pass} at every other transistor. If V_{rx} is lower than V_t then current will conduct and sense amplifier will be able to detect. For MLC it may require multiple read.
- **Erase:** A high positive voltage V_e is applied to the substrate with all wordline grounded. This lead to running of electrons from the floating gate to the substrate. This is bulk erase. Erase happens in one cycle whether it is a MLC(multiple level cell) or SLC (single level cell)

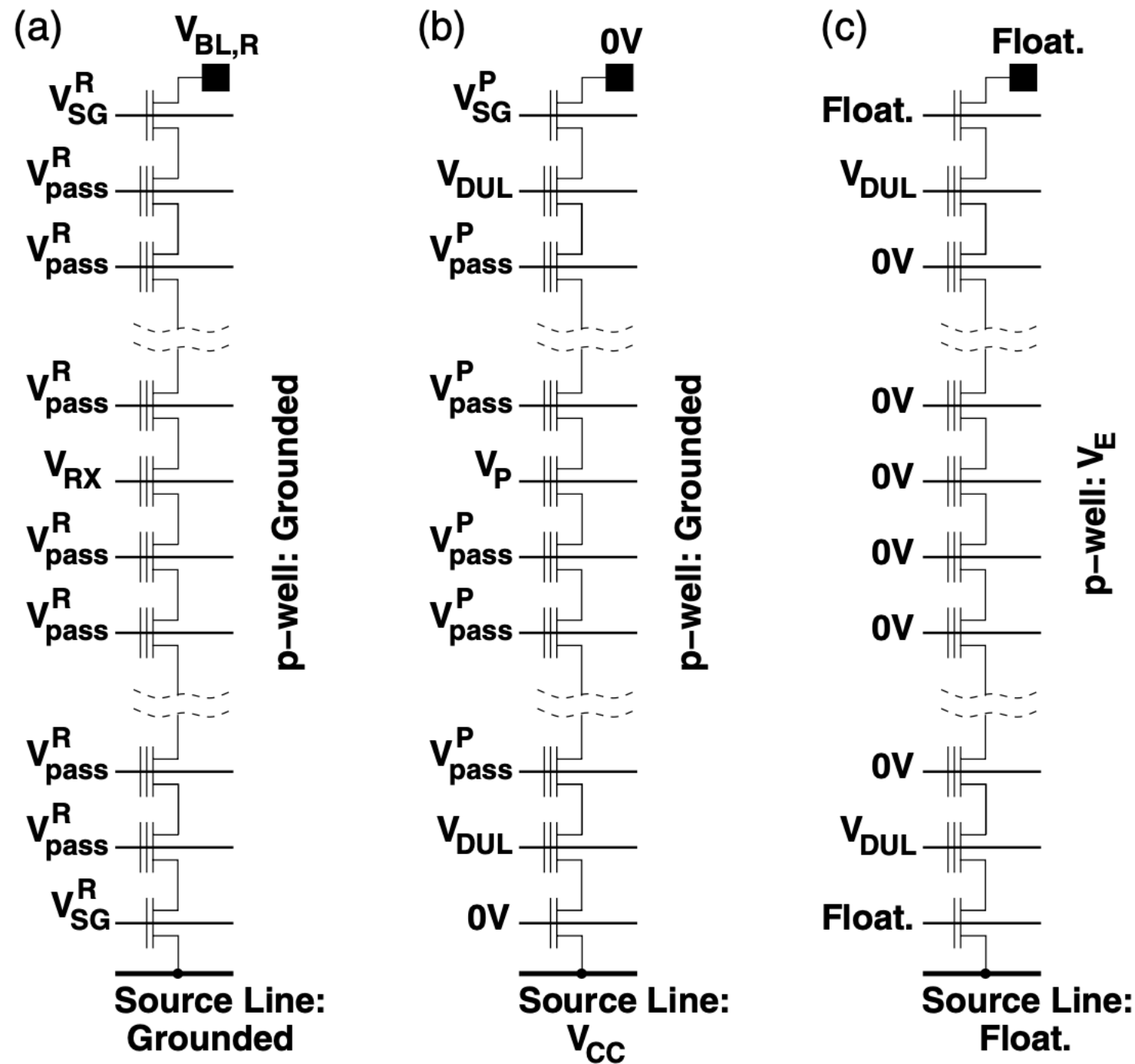


Fig. 5. Schematic description of the voltages applied to the *NAND* string to (a) read and (b) program a selected memory cell in the string (the selected cell is that whose WL voltage is V_{RX} and V_P during read and program, respectively). (c) Voltage scheme to erase the entire *NAND* block. V_{SG}^R and V_{SG}^P are the voltages applied to the gates of the biased select transistors during read and program, respectively.

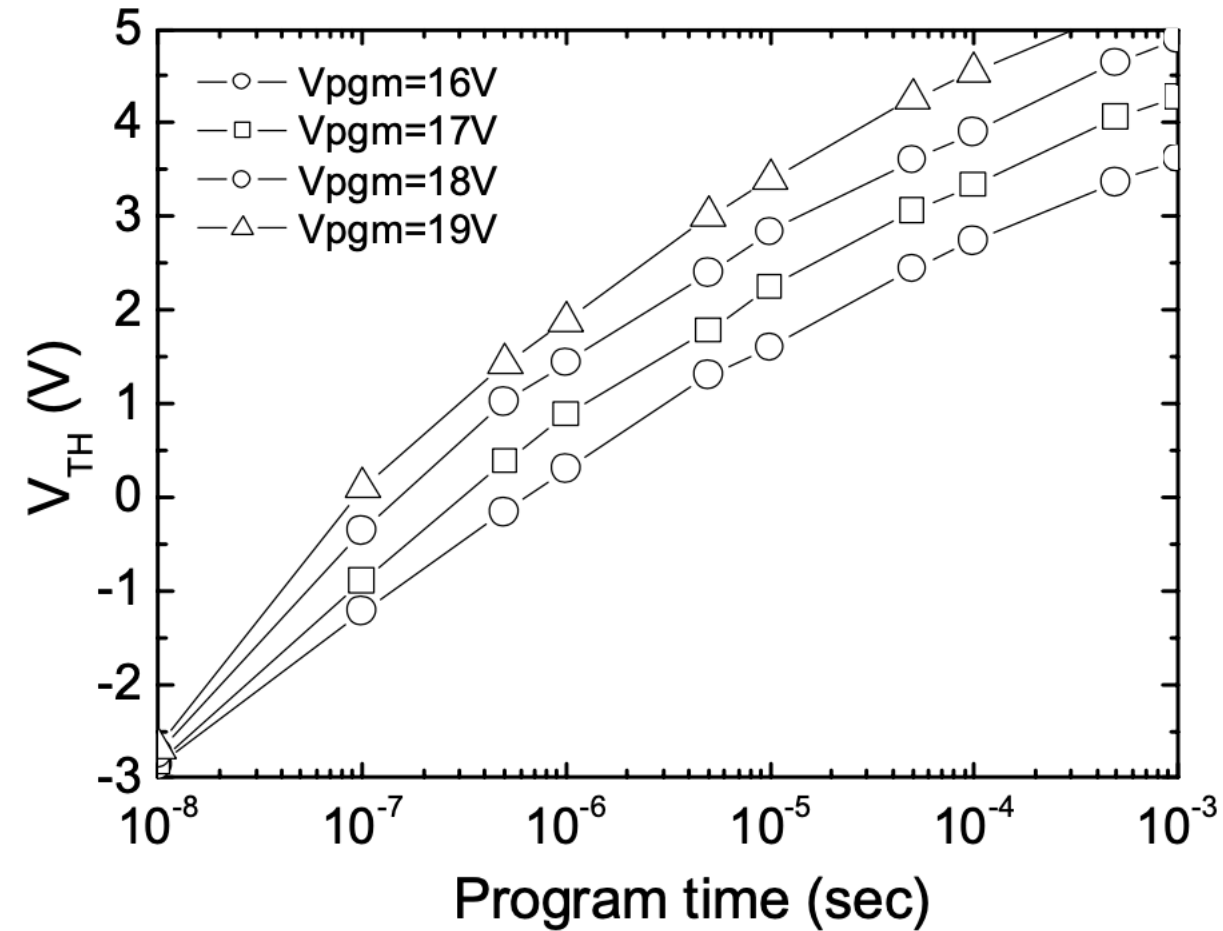
Program time

- I referred to paper(4) and extracted their data with WebPlotDigitizer (online tool).
- Only the change in V_t matters therefore I tried to model the change in V_t with the exponential function.
- I used Cftool of Matlab to do the estimation. Which uses Trust-Region and Levenberg-Marquardt algorithm to estimate coefficient

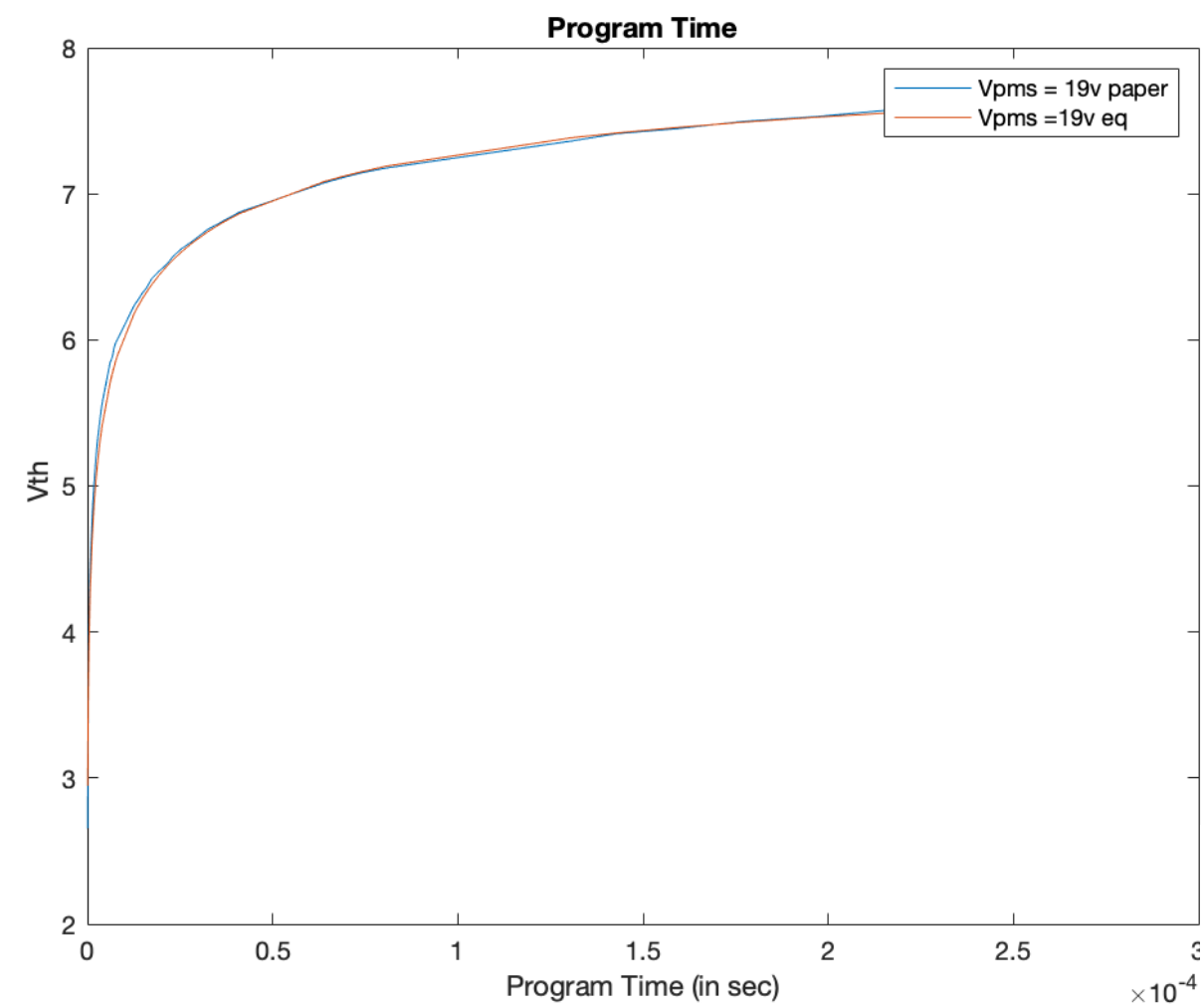
$$V_{th} = A * (1 - \exp(-1 * (\frac{t}{tou})^D)) \quad A = 8V$$

$$tou = a * \exp(b * V_{pms}), a = 7.3153e - 06, b = -1.304$$

$$D = a * \exp(b * V_{pms}); a = 0.03376, b = 0.1021$$



Ref : Multi-Level NAND Flash Memory.



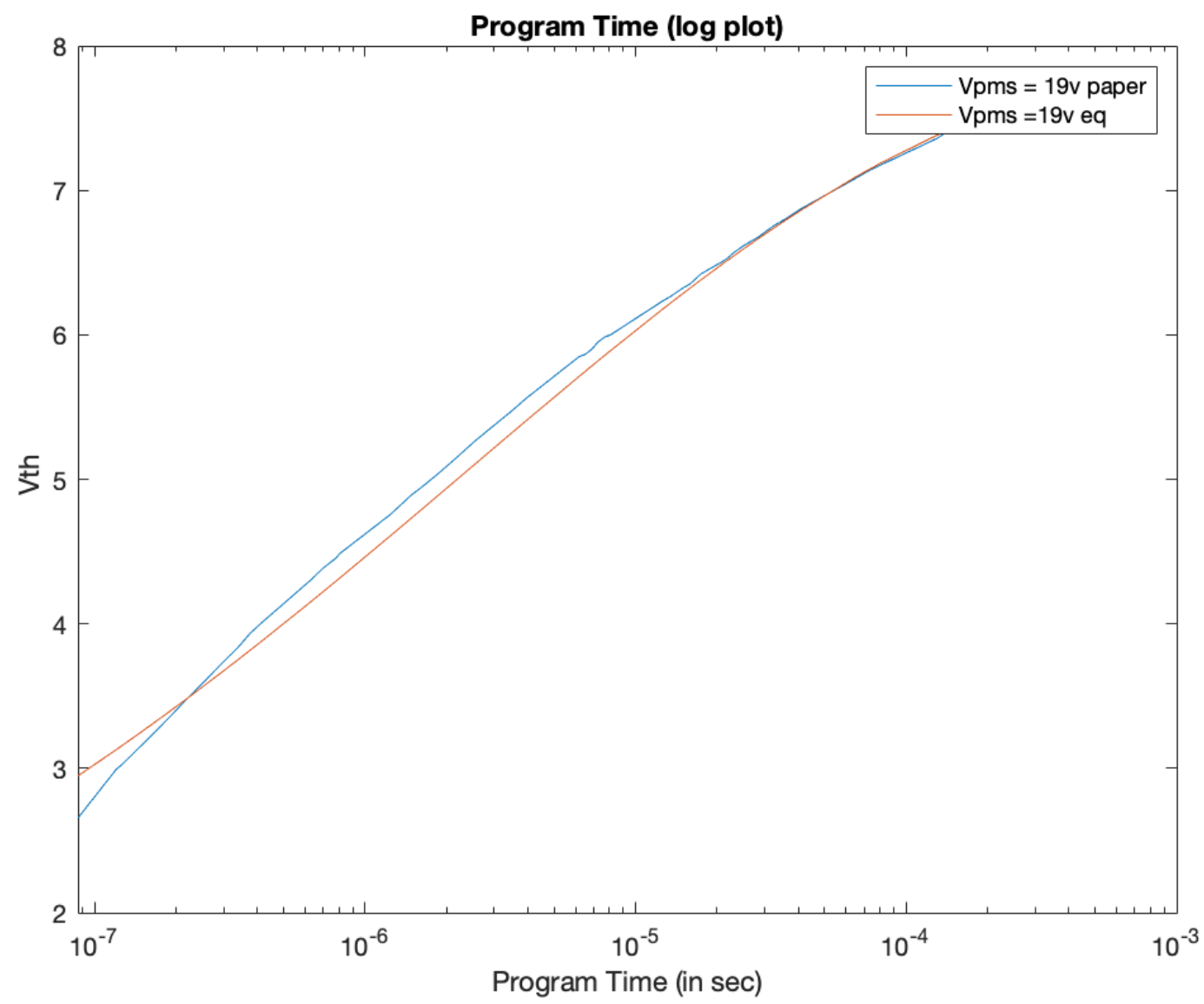
$$V_{wl} = 19V$$

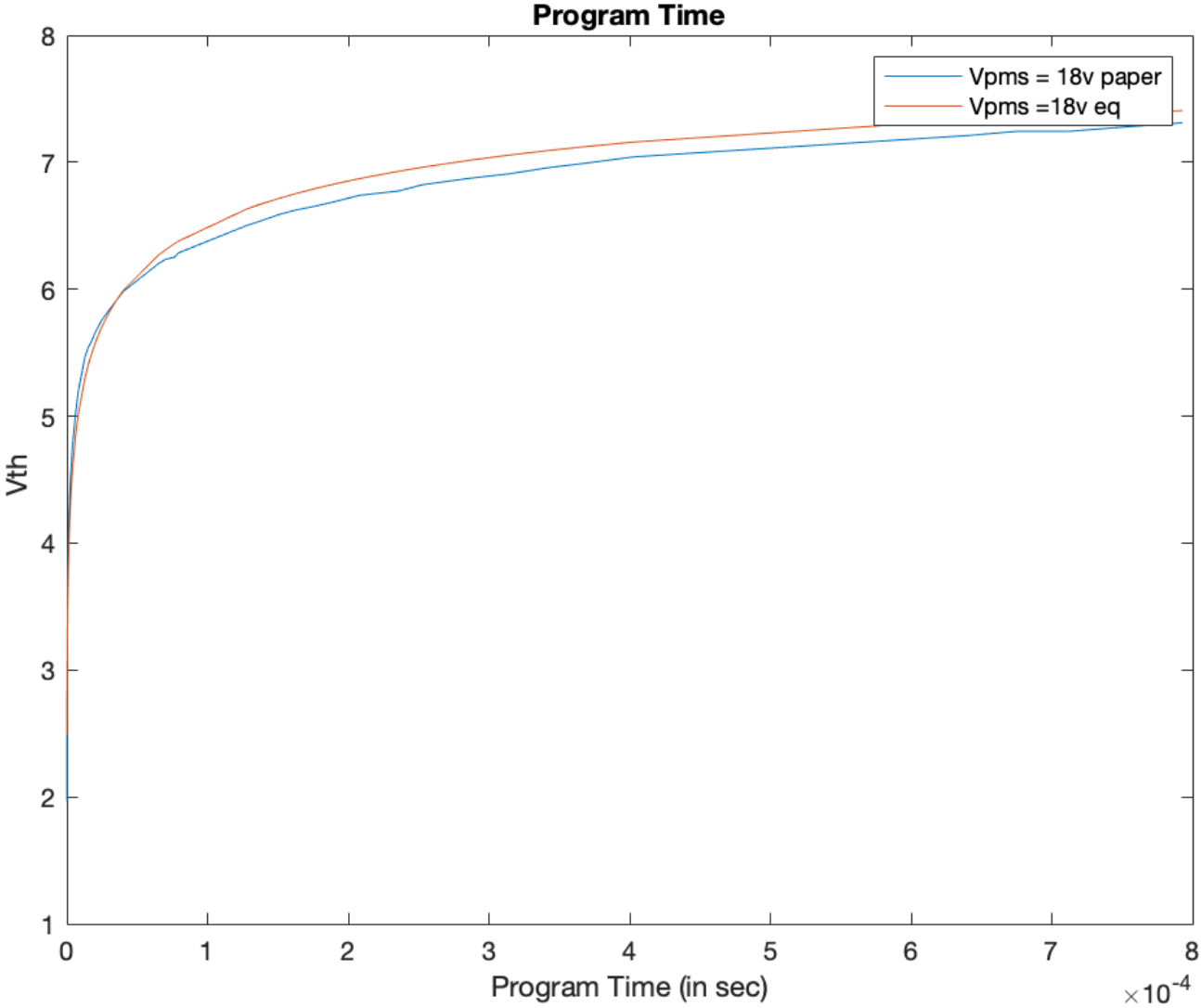
Goodness of fit:

R-square: 0.996

Adjusted R-square: 0.996

RMSE: 0.09262





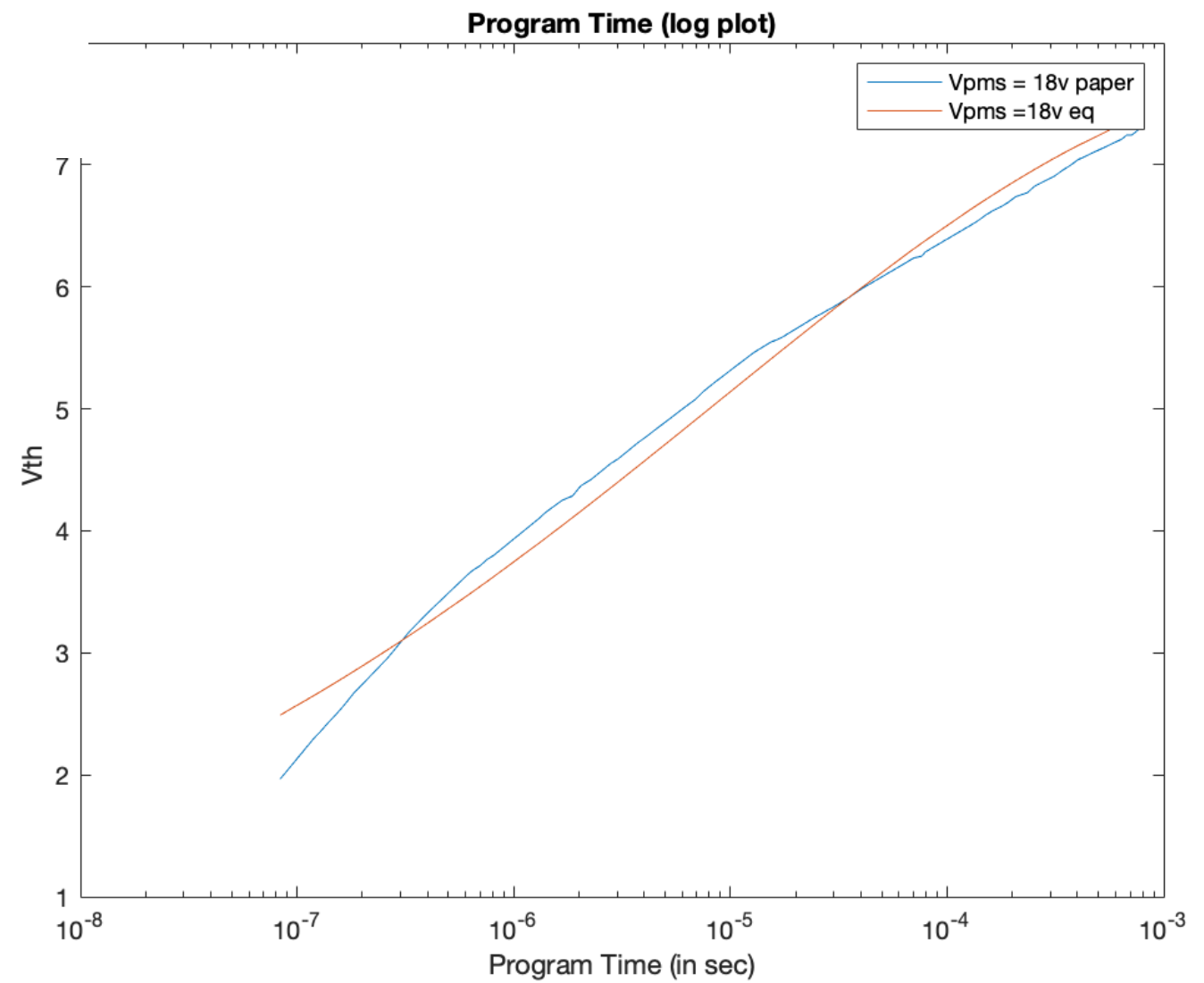
$$V_{wl} = 18V$$

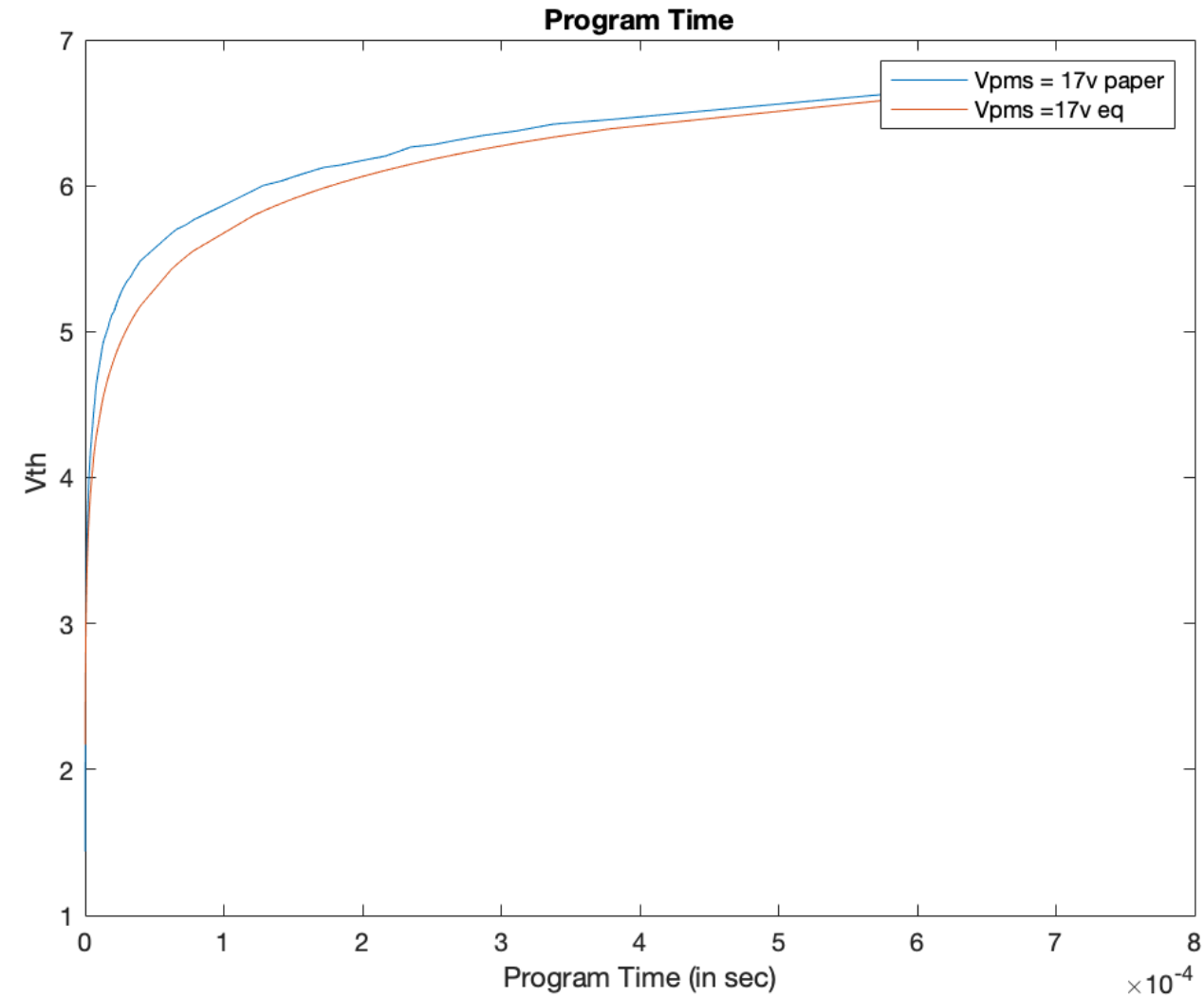
Goodness of fit:

R-square: 0.9882

Adjusted R-square: 0.9882

RMSE: 0.1732





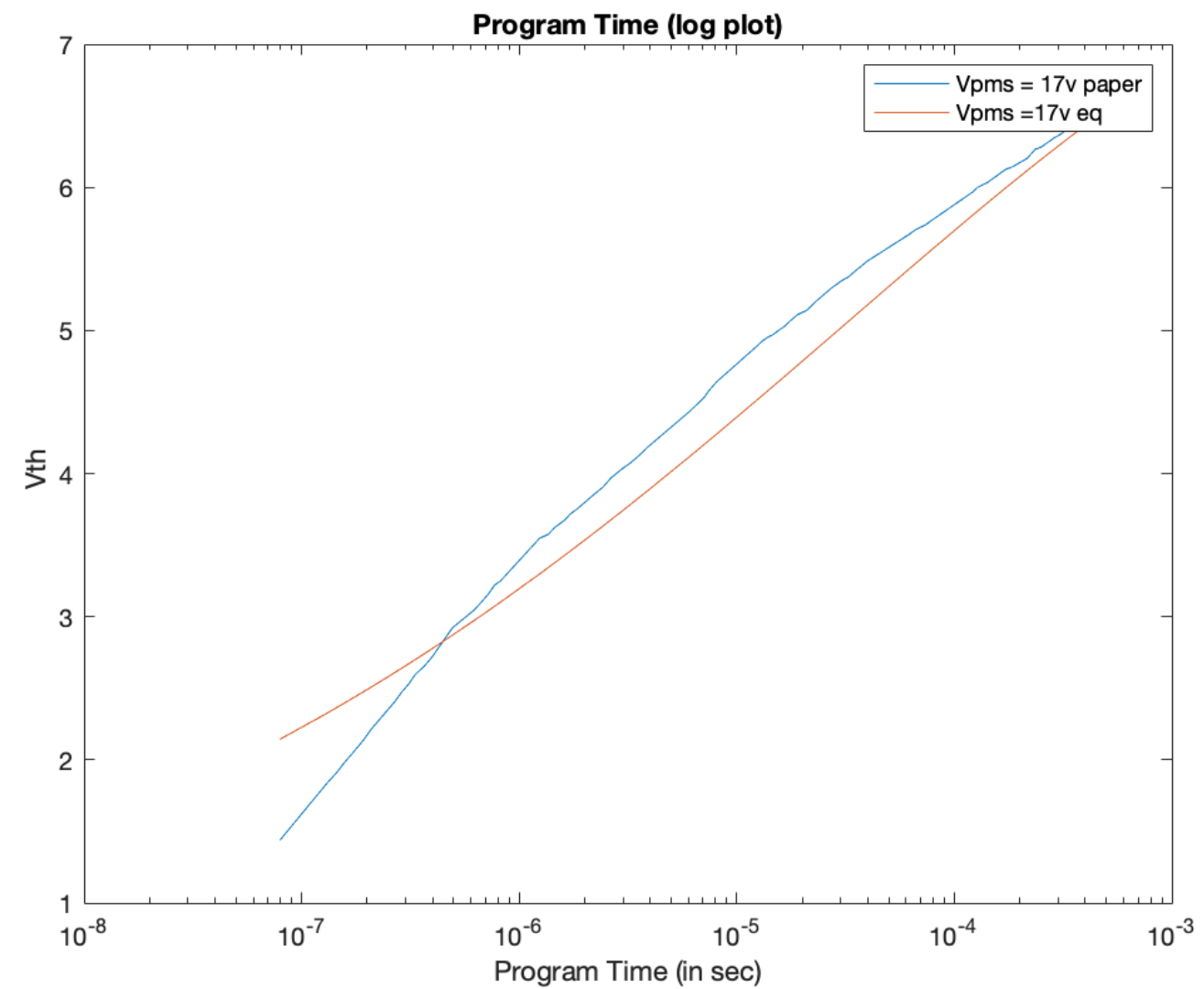
$$V_{wl} = 17V$$

Goodness of fit:

R-square: 0.9767

Adjusted R-square: 0.9767

RMSE: 0.2297



Erase time

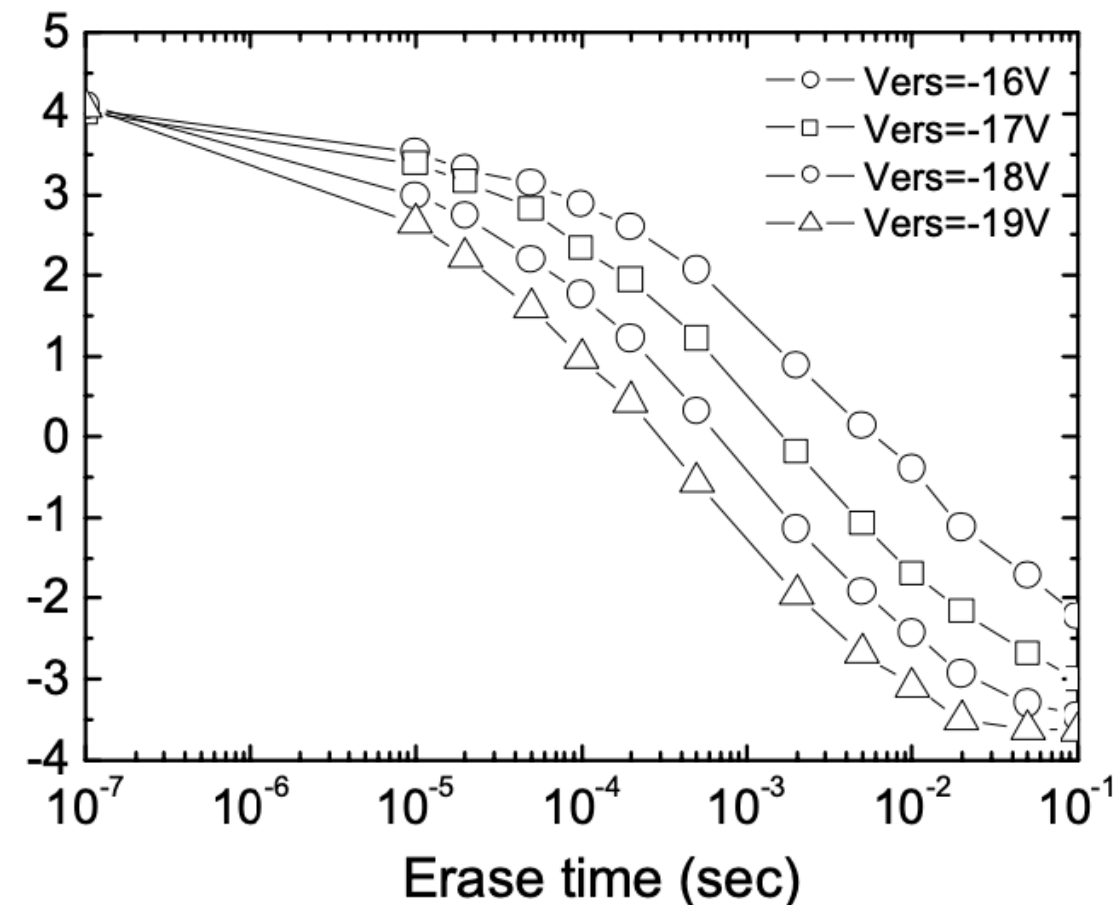
- I referred to paper(4) and extracted their data with WebPlotDigitizer (online tool).
- Only the change in V_t matters therefore I tried to model the change in V_t with the exponential function.
- I used Cftool of Matlab to do the estimation. Which uses Trust-Region and Levenberg-Marquardt algorithm to estimate coefficient

$$V_{th} = A * (\exp(-1 * (\frac{t}{tou})^D)) + C$$

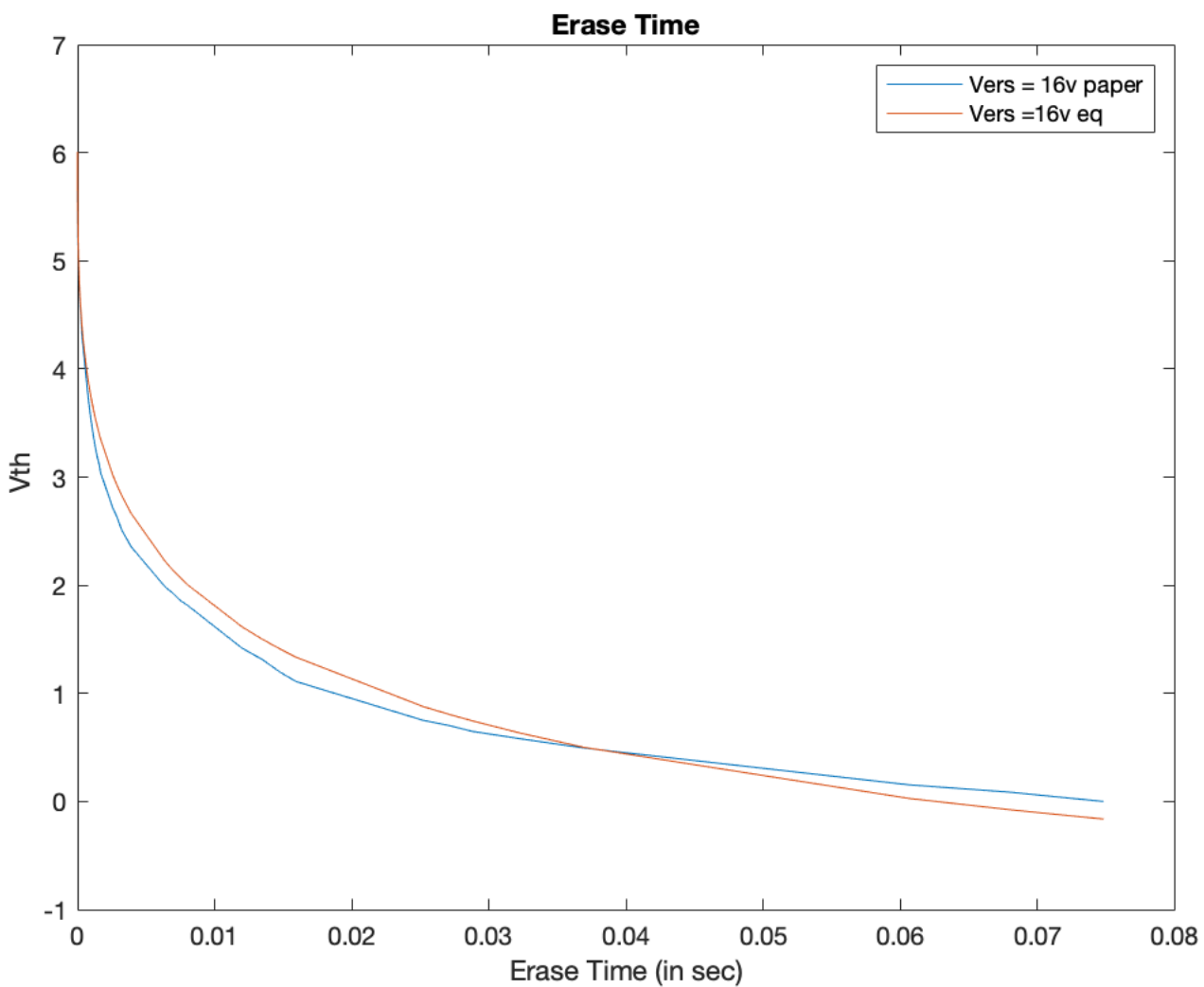
$$A = 8V, D = 0.3389$$

$$tou = a * \exp(b * V_{ers}), a = 2.856e + 08, b = -1.46$$

$$C = a * \exp(b * V_{ers}); a = -7.827e + 06, b = -0.9534$$



Ref : Multi-Level NAND Flash Memory.



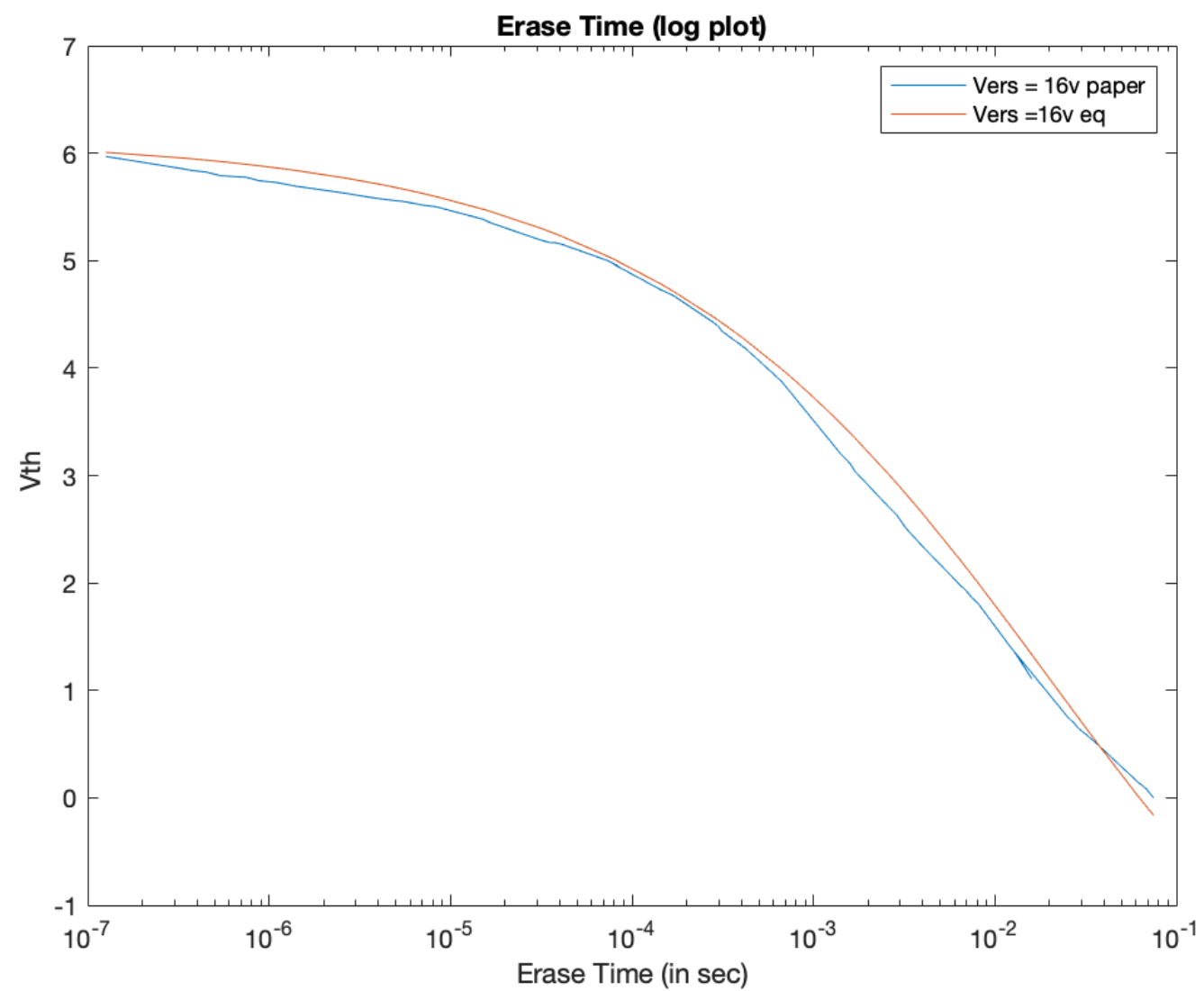
$$V_{ers} = 16V$$

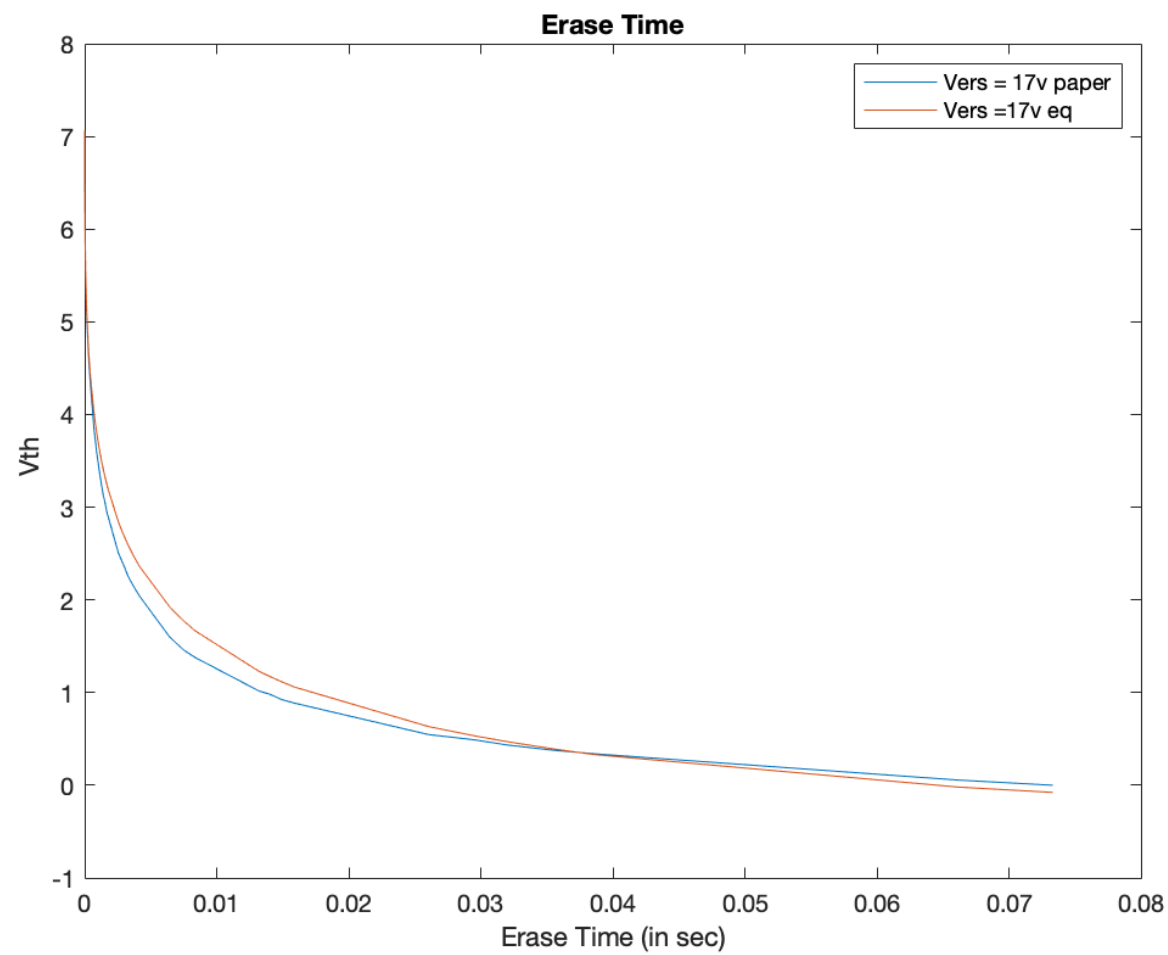
Goodness of fit:

R-square: 0.9971

Adjusted R-square: 0.9971

RMSE: 0.1011





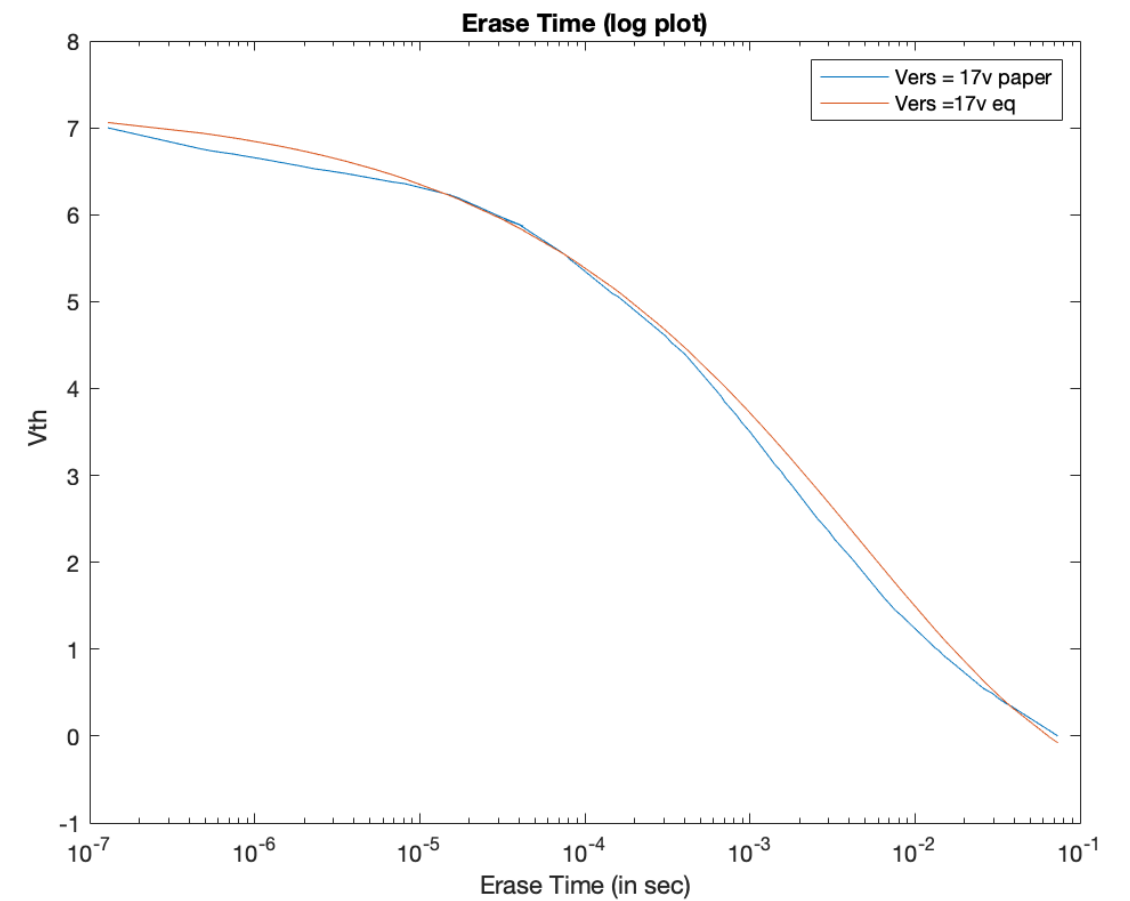
$$V_{ers} = 17V$$

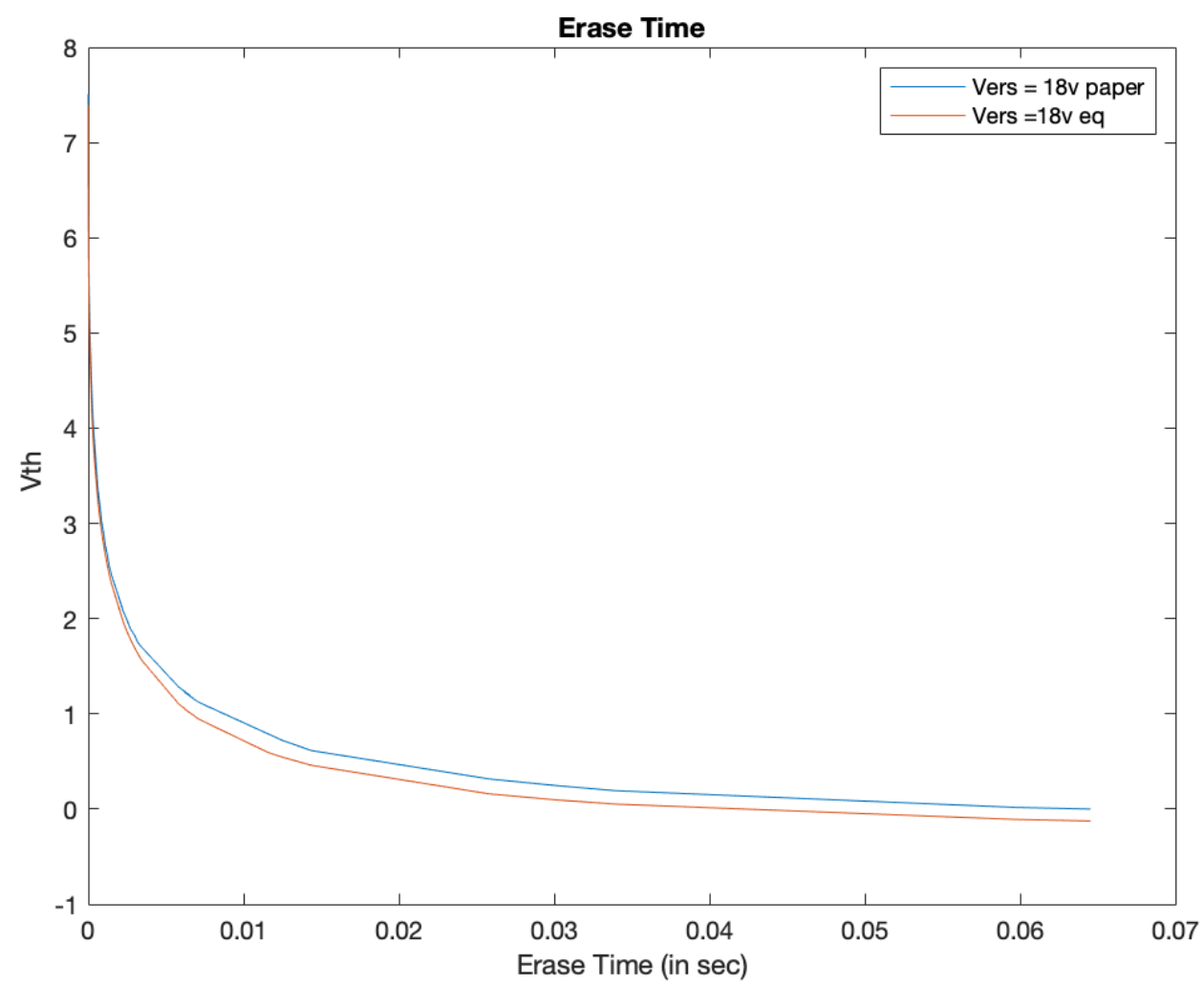
Goodness of fit:

R-square: 0.9969

Adjusted R-square: 0.9969

RMSE: 0.122





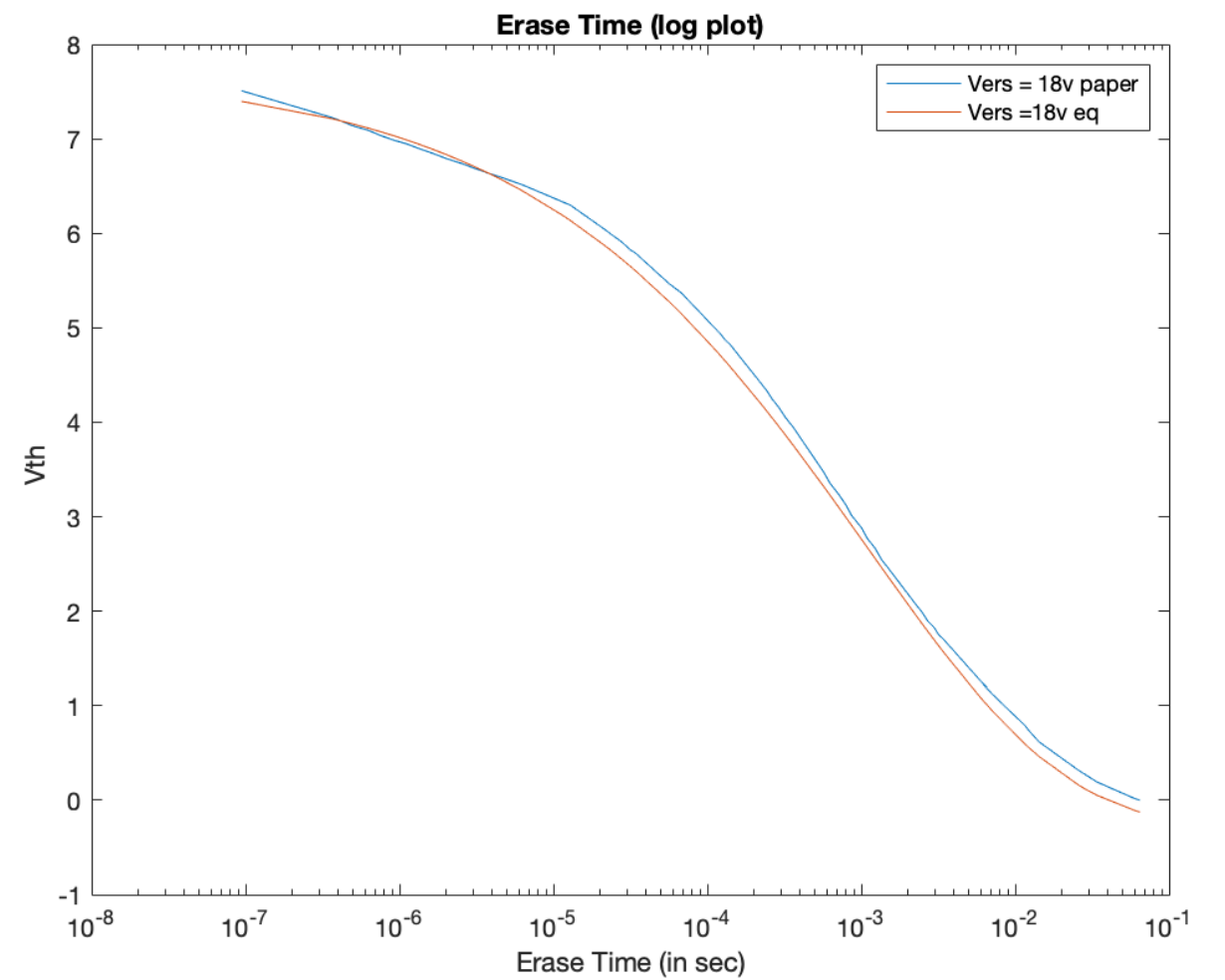
$$V_{ers} = 18V$$

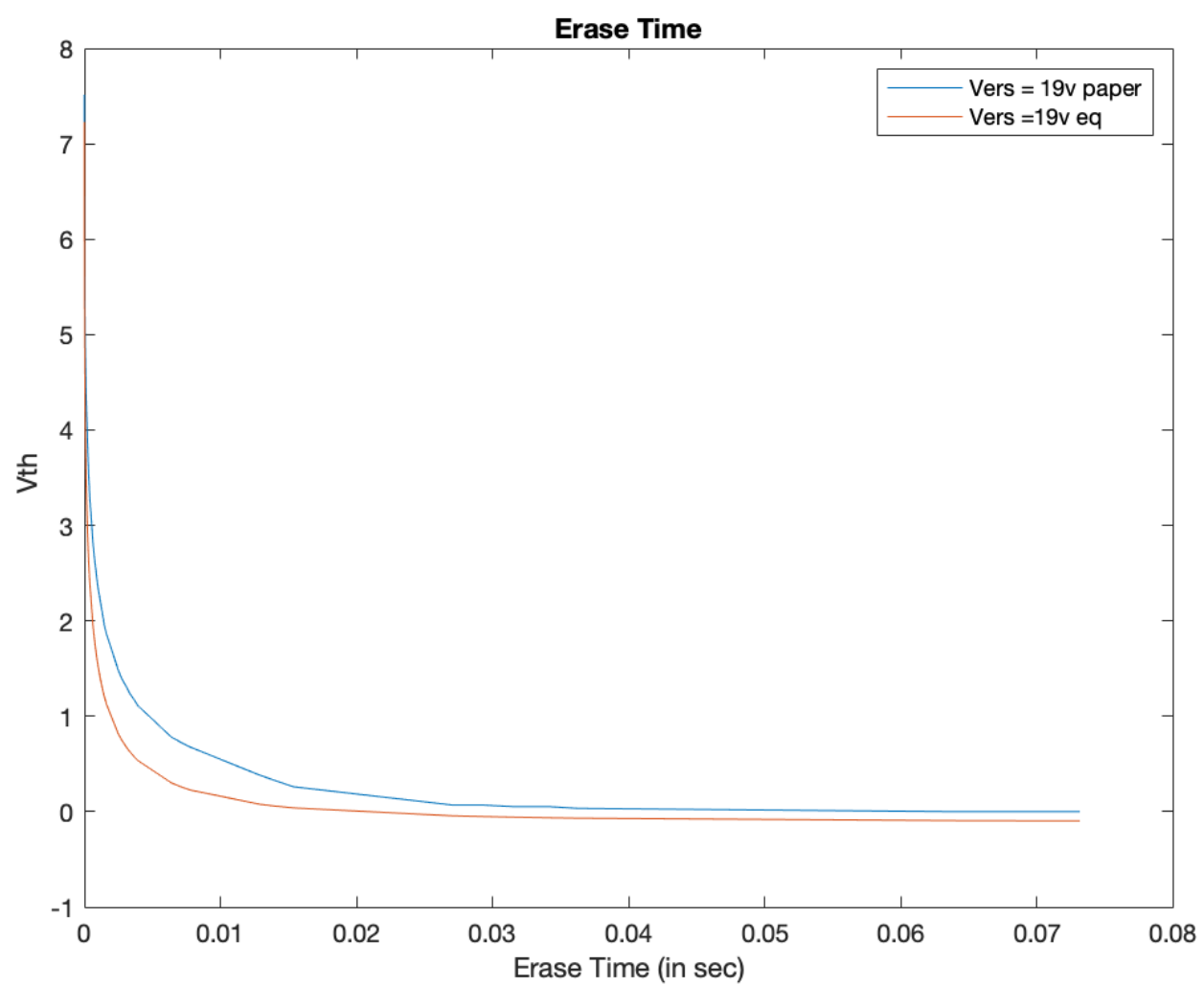
Goodness of fit:

R-square: 0.9987

Adjusted R-square: 0.9987

RMSE: 0.0851





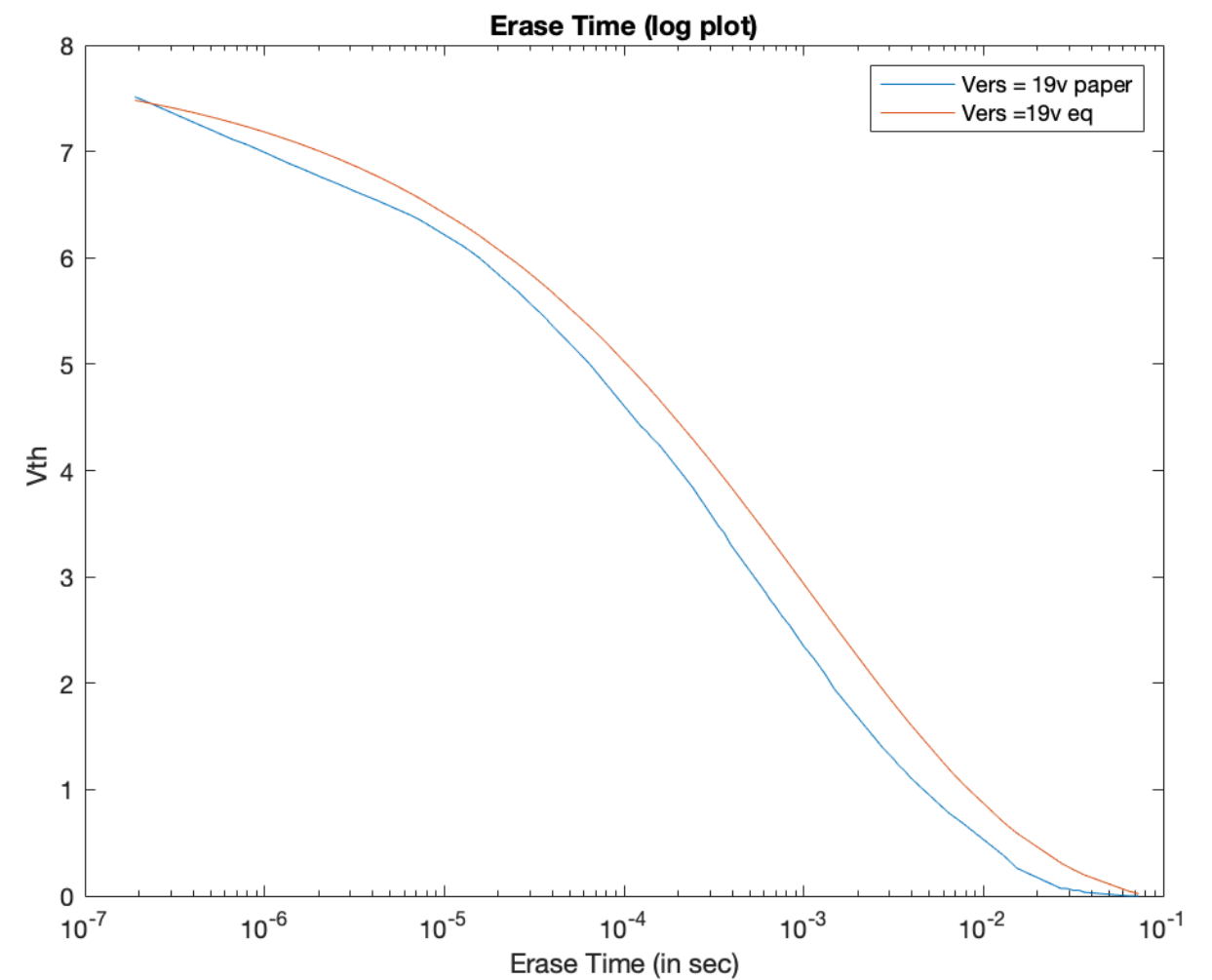
$$V_{ers} = 19V$$

Goodness of fit:

R-square: 0.995

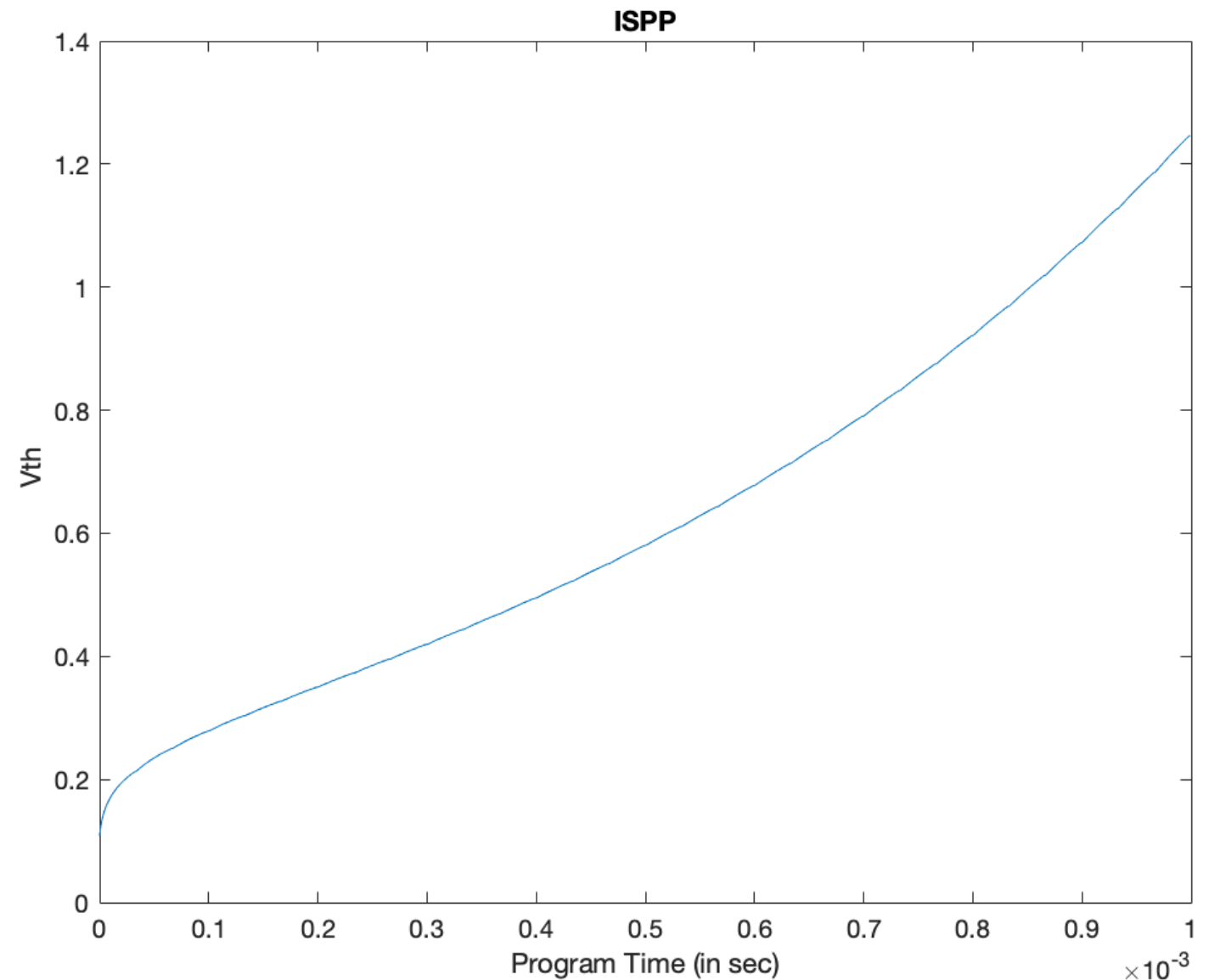
Adjusted R-square: 0.995

RMSE: 0.1803

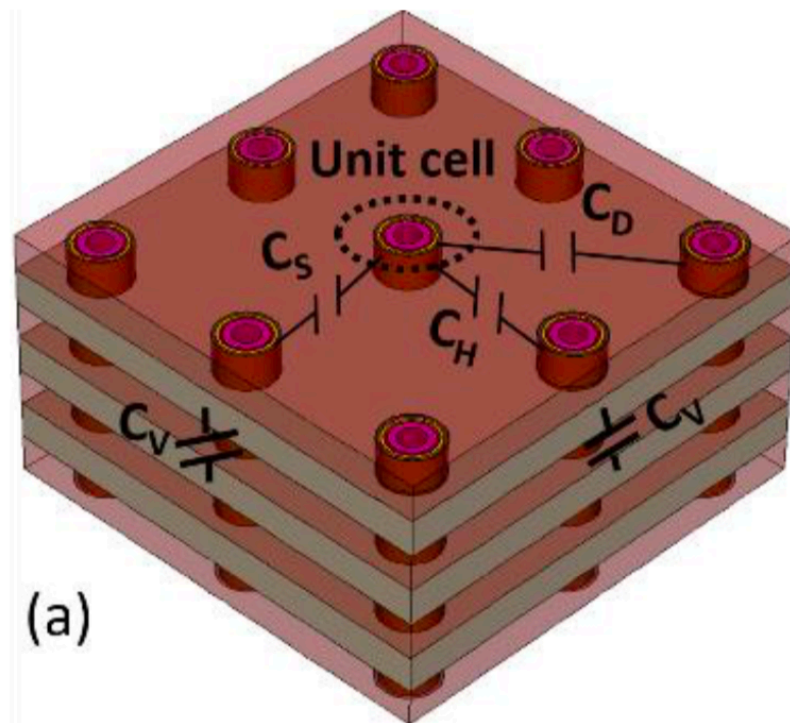


ISPP: Incremental-step-pulse programming

- During program, in case of MLC cells, we usually do not apply v_p directly.
- We apply Incremental V_p . The amplitude of v_p of applied to the cell is increased by a constant step V_s . This is called Incremental-step-pulse programming(ISPP). ISPP also allows to keep a nearly constant electric field in the cell tunnel oxide



MODELING NAND FLASH MEMORIES



C_H : The cell-cell coupling between adjacent cells sharing the same WL

C_v : the vertical coupling between the cells on the same string is taken into account via a vertical capacitance

C_D : the coupling between diagonal cells and the neighboring cells is considered using C_D the diagonal capacitance and the side capacitance C_s

Ref : A Behavioral Compact Model of 3D
NAND Flash Memory by Shubham Sahay,
Dmitri Strukov

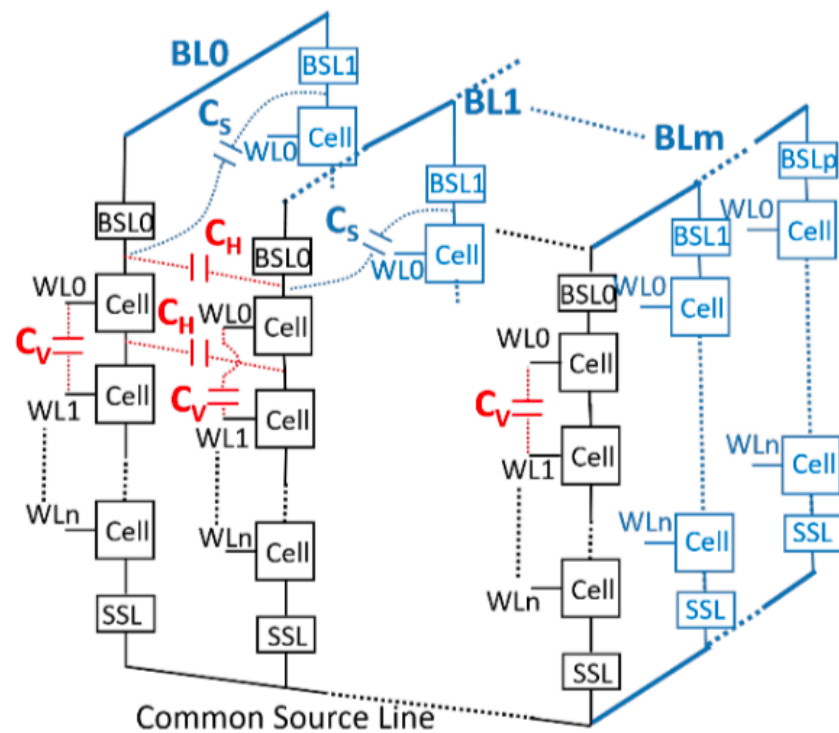


Fig. 3. Representation of a generalized 3D NAND flash memory array utilizing the compact model approach.

Ref : A Behavioral Compact Model of 3D NAND Flash Memory by Shubham Sahay, Dmitri Strukov

Here to model every string we need eight other strings
 To calculate the coupling capacitance (C_V , C_H , C_S and C_D) they have used mixed-mode Tcad simulations. For the basic mos the BSIM-CMG 110.0.0 compact model was used by them
 They have done simulation on 10 WLS