EE 671: VLSI DESIGN
Assignment-2

We shall use VHDL for carrying out this assignment.

Q–1 Assume that the delay of some common gates (inclusive of parasitic delay) is as given below:

Inverter	100 ps
NAND gate	150 ps
NOR gate	150 ps
$\overline{A+B.C}$	200 ps
Tiny XOR	200 ps

a) Design a logarithmic adder using Brent Kung architecture for adding 32 bit operands. Write its hardware description in synthesizable VHDL and show its correct working using a test bench with appropriate test vectors.

b) What is its critical path? In how much time can we guarantee that the addition will be complete?

We shall use this adder later for designing a 16x16 bit multiplier.