generate resistor.va
generate .sp file
hspice -i hello.sp -o out
use 13

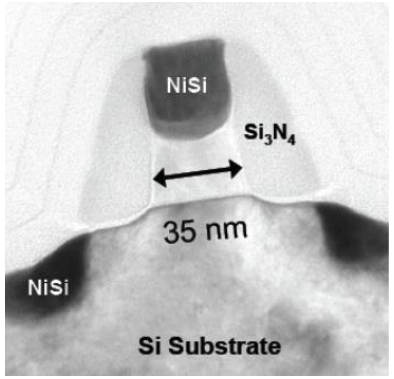
# COMPACT MODELLING USING VERILOG-A
# AND
# INTEGRATION WITH HSPICE

# COMPACT MODEL ??

- COMPUTATIONALLY EFFICIENT description of TERMINAL PROPERTIES of a device as a function of TERMINAL VOLTAGES

$$[\{I\},\{Q\}] = f(V1,V2,V3.....Vn)$$

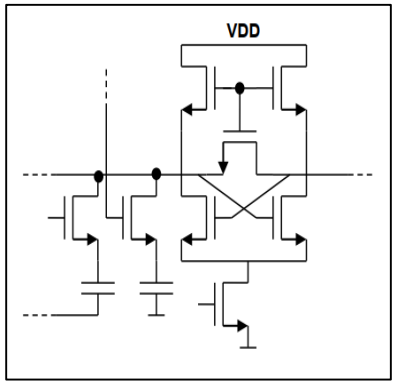
**PROCESS/TECHNOLOGY Development**




Bridge

**COMPACT MODEL**

**CIRCUIT Designing**




- It is implemented inside a CIRCUIT SIMULATION Engine
- How to make a **COMPACT MODEL** ?

*ref-https://nanohub.org/resources/21367/*

# Compact model classification and requirements

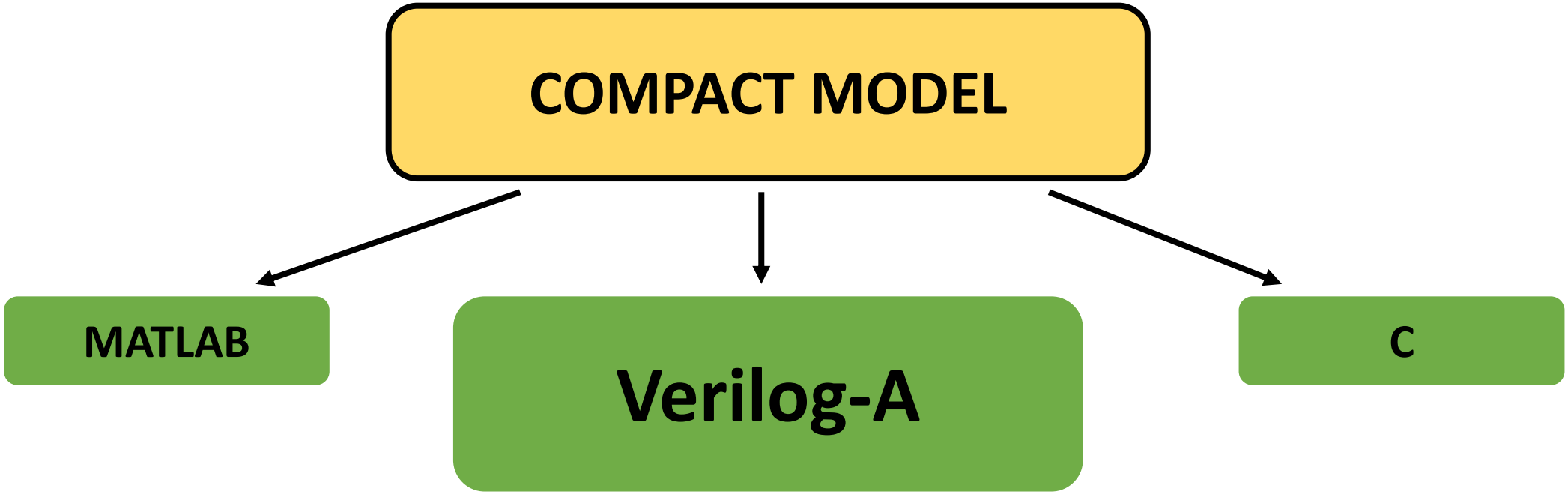
## Classification of Transistor Model

- **Physics based**
  - All parameters have physical significance.
  - Computationally efficient and technology independent.
- **Empirical**
  - Set of equations with fitting parameters.
- **Lookup table based**
  - Limited to characterized data present in lookup table.
- **Macromodels**
  - Present in the form of equivalent circuit representation.
- **Semi-empirical model**
  - Introduced fitting parameters in Physics based model to capture device behaviour.
  - Empirical lookup table based model.

## Compact Model Requirements

- **Model stability and convergence**
  - Functions and their derivatives must be continuous
  - No evaluation resulting 0/0 (i.e. physical limit must be accurately set)
- **Speed of evaluation**
  - Expensive math functions must be avoided.
  - Reusability of internal variables to reduce computation time.
- **Accuracy**
  - Must be accurate up to required RMS error.

Ref: Tutorial on “Basics of Compact Model Development”, by Sivakumar P Mudanai (*Intel Corporation, Santa Clara, CA*).
Web: https://nanohub.org/resources/21367/




**‘Hardware Description Language’**

**Can be easily integrated with SPICE-Simulators**

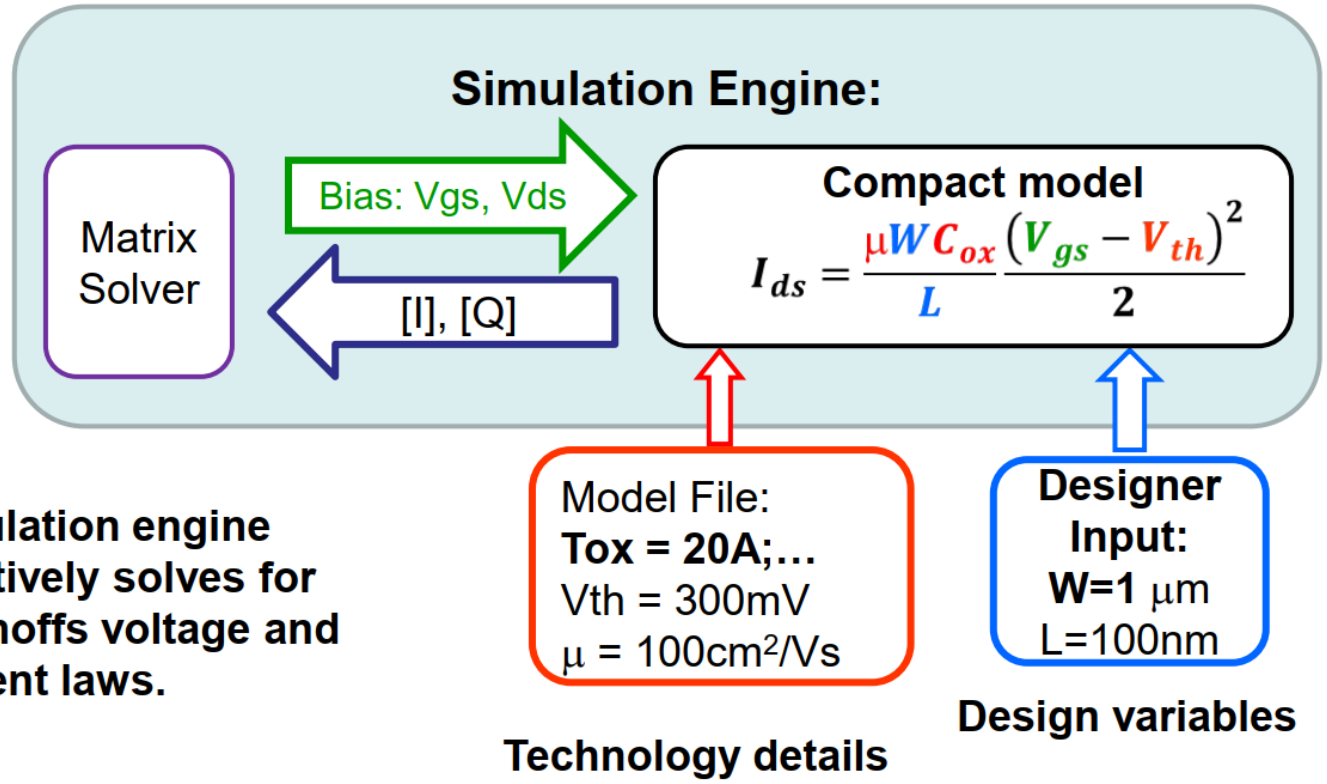
https://nanohub.org/resources/20580/download/2014.02.21-Coram-NEEDS.pdf

# CIRCUIT SIMULATORS ??

- NgSpice
- HSpice
- PSpice
- MultiSim
- Cadence-Spectre

.....

## SIMPLIFIED VIEW OF A CIRCUIT SIMULATION




**Simulation engine iteratively solves for Kirchoffs voltage and current laws.**

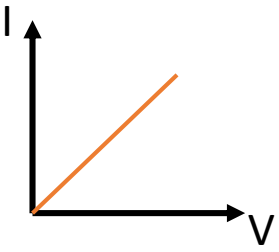
# Verilog-A Model for a Simple Resistor

Defines "electrical" discipline and access functions V and I

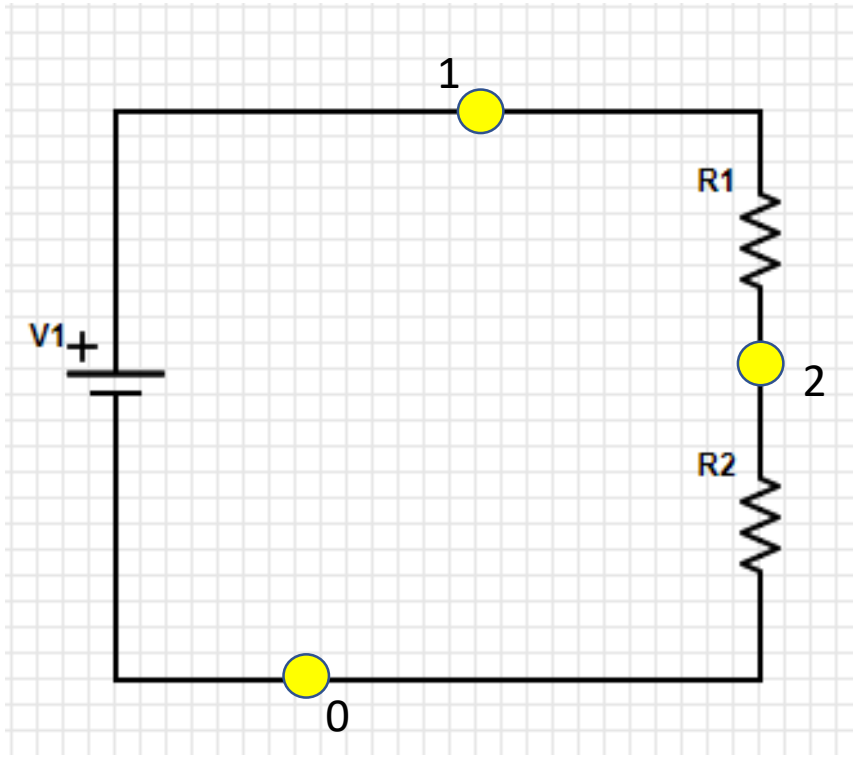
```
`include "disciplines.vams"

module resistor(p,n) ;
inout p,n;

parameter real resistance = 1000.0 from (0.0:inf) ;

electrical p, n ;
analog
begin
I(p,n) <+ V(p,n)/resistance ;
end
endmodule
```

V(p,n) and I(p,n) can be used


**resistance** = 1000.0 Ω



```
`include "disciplines.vams"

module resistor(p,n) ;
inout p,n;

parameter real resistance = 1000.0 from (0.0:inf) ;

electrical p, n ;
analog
begin
I(p,n) <+ V(p,n)/resistance ;
end
endmodule
```




# Circuit Netlist

```
R1  1  2  5k
R2  2  0  5k
```

Standard RESISTOR model

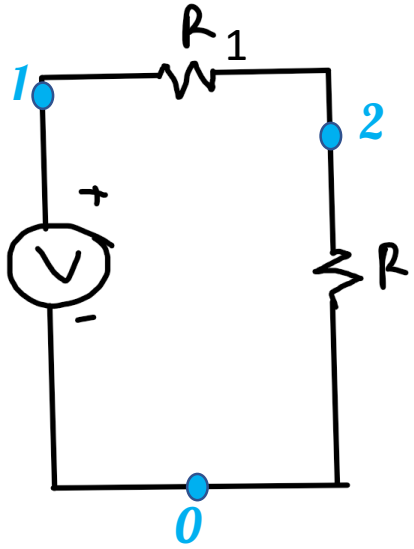
```
Vs  1  0  DC 5V
```

# HSPICE NETLIST FOR A BASIC RESISTOR-DIVIDER

Your Nickname for the model

Same name as module

```
1   * Basic resistor
2   ********************************************************************************
3   *                              Include Files
4   ********************************************************************************
5   .OPTION POST=2
6   .hdl "resistor.va"
7   .model res resistor
8   $.param GND = 0
9   ********************************************************************************
10  *                                Netlist
11  ********************************************************************************
12  $Xn1 2 1 0 0 nmos1 $NFIN=3
13  X1 1 2 res resistance=5000
14  X2 2 0 res resistance=10000
15  Vs 1 0 DC 0.8
16  $Vin IP GND PULSE(0 0.8 0 2p 2p 1n 2n)
17  ********************************************************************************
18  .dc Vs 0 2 0.1
19  .end
20
```




!! ERROR !!

https://cseweb.ucsd.edu/classes/wi10/cse241a/assign/hspice_sa.pdf

# How to Include model parameters from a text file??

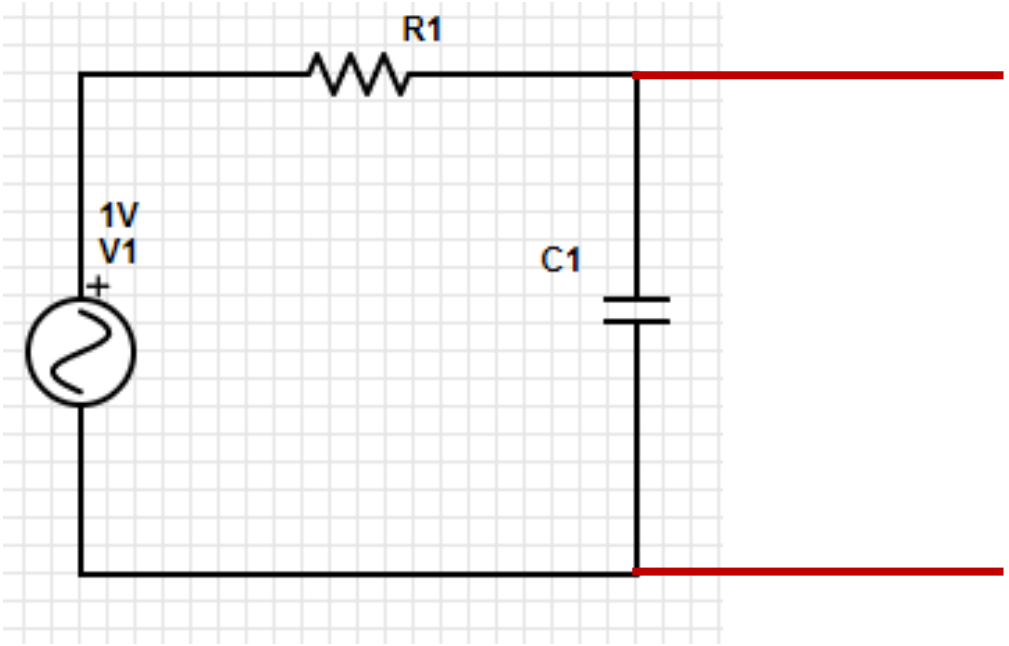
```
* Basic Resistor with Include Parameter file
*********************************************************************
***
*                            Include Files
*********************************************************************
***
.OPTION POST=2

.hdl "resistor.va"
.include 'param.txt'
* .model res resistor
$.param GND = 0
*********************************************************************
***
*                              Netlist
*********************************************************************
***
X1 1 2 res $resistance=10
X2 2 0 res $resistance=10

Vs 1 0 DC 0.8

*********************************************************************
***
.dc Vs 0 4 0.1
.print V(1) V(2)

.end
```

```
.model res resistor
+resistance = 200
+
+
....
```

# Verilog-A model of a Capacitor

```
`include "disciplines.vams"

module simplecap(p,n);

inout p,n;
electrical p,n;

parameter real C=1e-6 from [0.0:inf);  //default value
real q;

analog begin
    q=C*V(p,n);
    I(p,n)<+ ddt(q);
                end

endmodule
```

**Ques - Use your customized models for resistor and capacitor to design RC-Low Pass Filter with 3-dB Bandwidth of 10KHz. Perform AC analysis to verify the result. Overwrite appropriate values in place of default values for R and C.**



```
*RC-Check
*********************************************************************
*                              Include Files
*********************************************************************
.OPTION POST=2

.hdl "resistor.va"
.hdl "simplecap.va"
.model cap simplecap
.model res resistor

*********************************************************************
*                                Netlist
*********************************************************************
X1 1 2 res   $What value?
X2 2 0 cap   $What value?
Vs 1 0 AC 1V

*********************************************************************

$.dc Vs 0 2 0.1
.AC DEC 10 1 1MEG
.print V(2)

.end
```

# Ques1 –

a) **Make a Verilog-A model for a simple MOSFET by defining current equations in linear and saturation regions. Verify by plotting INPUT and OUTPUT characteristics in HSPICE. Consider Vth=0.4V.**

## Ques2 –

**Include the effect of Channel Length Modulation(CLM) in the Verilog-A model and find a suitable value of '$\lambda$' to approximately match $I_d$-$V_d$ of the designed model with given data.**

**Use $L_1$=100µm and W=L**

$$I_{dsat} = I_d'[1 + \lambda(V_{DS} - (V_{GS} - VTH))]$$

# Ques3 –

**Instead of using Vth as a constant, use these equations :**

$$V_T = VT_0 + \Upsilon(\sqrt{2\Phi_f + Vsb} - \sqrt{2\Phi_f})$$

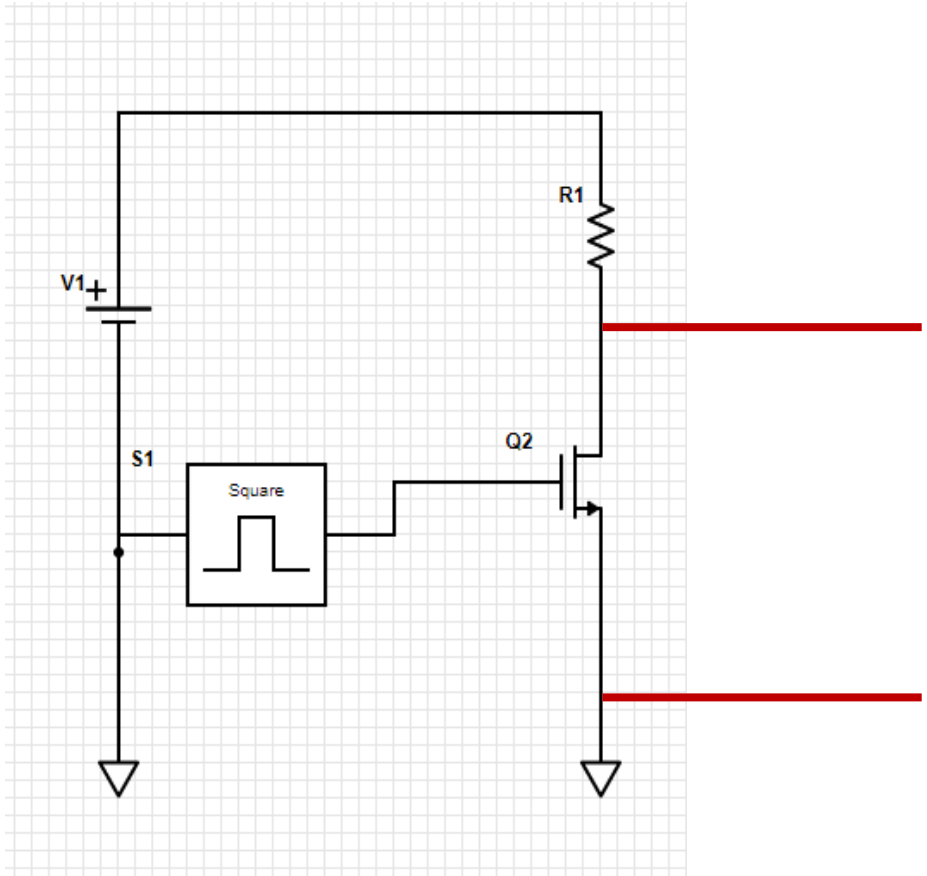
$$\Upsilon = \frac{\sqrt{2\varepsilon_0 q N_a}}{C_{ox}}$$

$V_{T0}$ **= 0.4V**
$\Phi_f$ **= $V_T$ln(Na/Ni) , $V_T$ = 0.026V , Ni=1e10 /cm$^3$**

**to study the effect of Body-Bias on the Threshold Voltage. Symbols have their usual meanings.**

**Verify for : $V_{SB}$ = 0.5V, 1V and 1.5V**

# Ques4 – Design a basic INVERTER using the nmos and verify by applying a square pulse at Gate.




```
.. .. ..

Vg 2 0 PULSE(0 1.8 0 10p 10p 1n 2n)

.. .. ..

.tran 10p 10n
.print V(2) V(3) I(Vdum)
```

# Reference Code – Verilog-A

```
`include "disciplines.vams"
`include "constants.vams"

module simple_mos (d,g,s,b);

inout d,g,s,b;                                          // inout TERMINALS
electrical d ,g ,s ,b ;                                 //input-output nodes

parameter real W=1e-5 from [0:inf];                     // width of MOSFET
parameter real L=1e-5 from [0:inf];                     // Length of MOSFET
….
….
parameter real VTO=0.4 from [0:inf];                    // Initial Threshold voltage
parameter real mu=0.4 from [0:inf];
parameter real NA=1e17 from [1e13:1e22];                // Doping
parameter real TOX=20e-7;                               // Oxide Thickness
parameter real VSB=0.0;                                 //Body-Bias
real P_EPSOX=3.9*8.85e-14;
real P_EPSSI=11.7*8.85e-14;
real PHI,GAMMA,COX,PHI_F,VT;                            // You can choose your own variables
real Ni=1e10;
real q=1.6e-19;

analog
begin
  // ……. Real variables calculations using the provided equations……
   if (V(g,s) > VT)                  //ensuring conduction after threshold
      begin
         if(……)
                  ……

         else
                  ……
      end
   end
endmodule
```

# Reference Code - HSPICE

```
* Basic mos_test
*****************************************************************************
*                              Include Files
*****************************************************************************
.OPTION POST=2
.hdl "MOS_adv.va"
* .hdl "simple_MOS.va“   $ change the names according to your file_names
* .model mos simple_mos
.include 'model_var.txt'

*****************************************************************************
*                                Netlist
*****************************************************************************

X1 3 2 0 0 mos
Vdum 4 3 DC 0
$R 4 3 1K   $ Uncomment for INVERTER problem
$Vg 2 0 DC 1
Vd 4 0 DC 1.8V
$Vg 2 0 PULSE(0 1.8 0 20p 20p 1n 2n)
Vg 2 0 DC 1
*****************************************************************************
.dc Vd 0 2 0.001 $ to plot Output Characteristics
.dc Vg 0 2 0.001 $ to plot Input Characteristics
* .tran 10p 6n
$ .print – to get data in the .lis file
.end
```