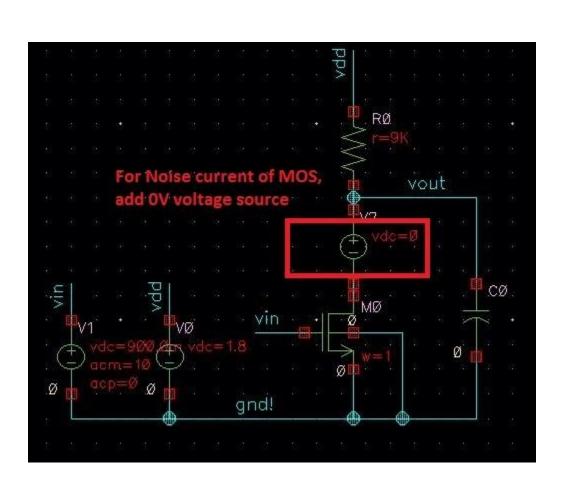
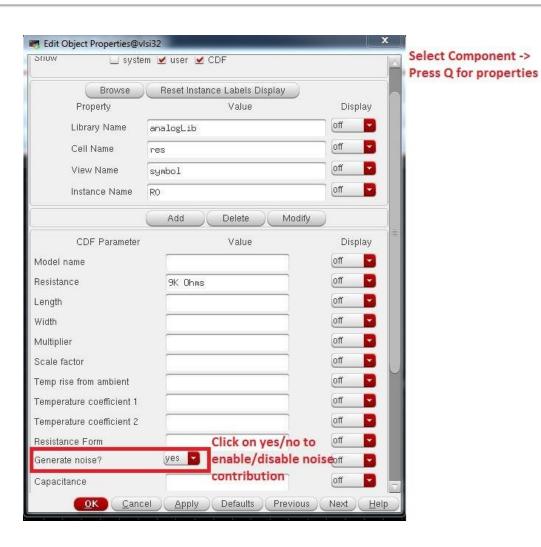
EE618 CMOS ANALOG IC DESIGN

Noise Simulation In cadence Spectre

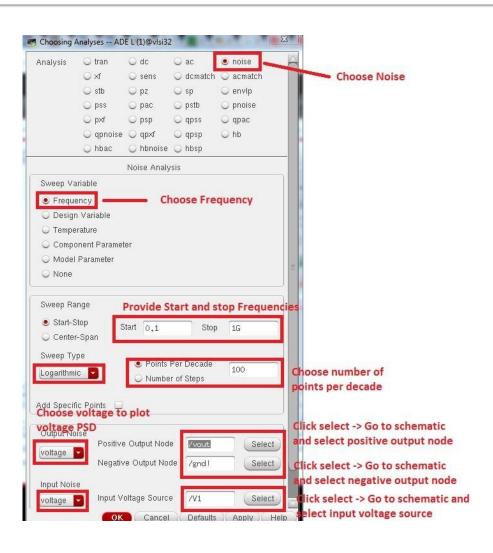
Set up the circuit



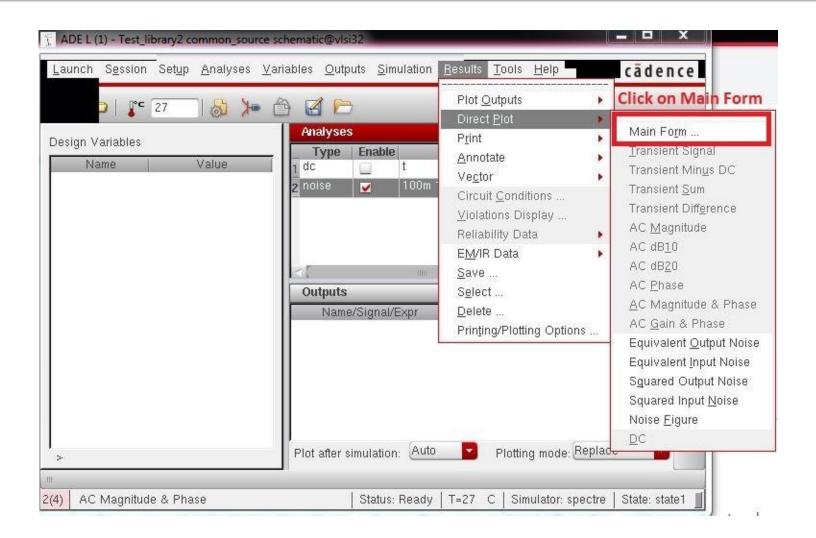
Enable/Disable Resistor Noise



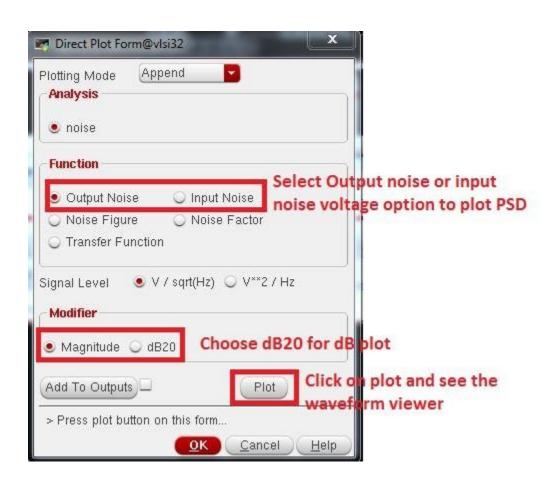
Analysis Selection in ADE for voltage PSD



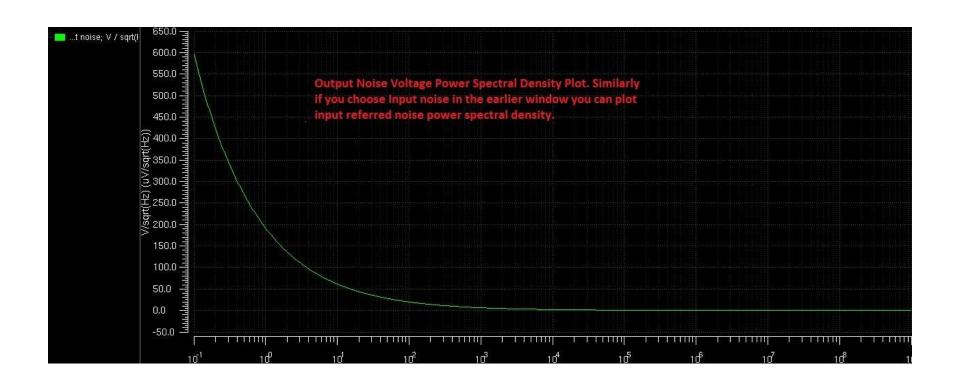
After Running Simulation



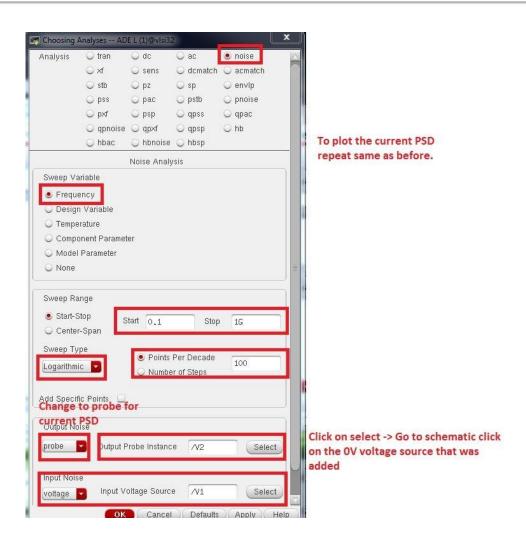
Plotting Options for Voltage PSD



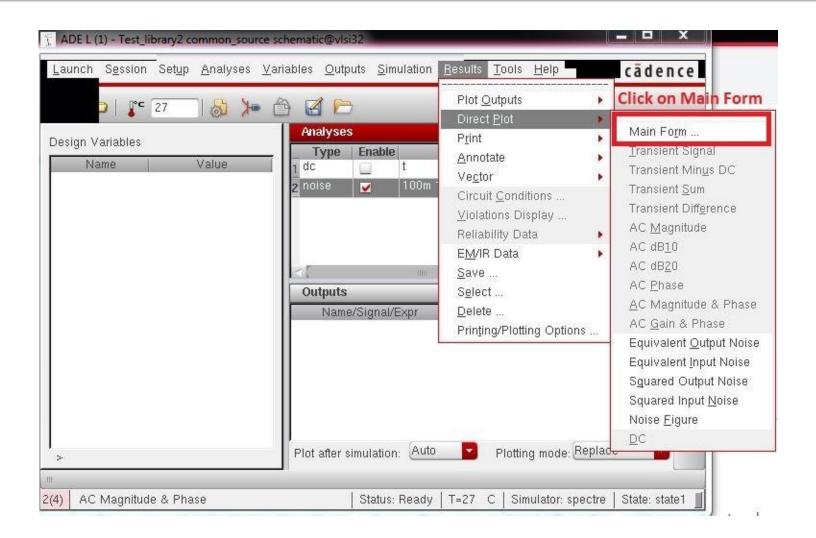
Example Voltage PSD plot



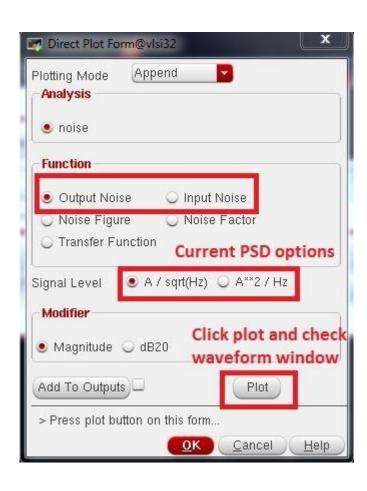
Analysis Selection in ADE for Current PSD



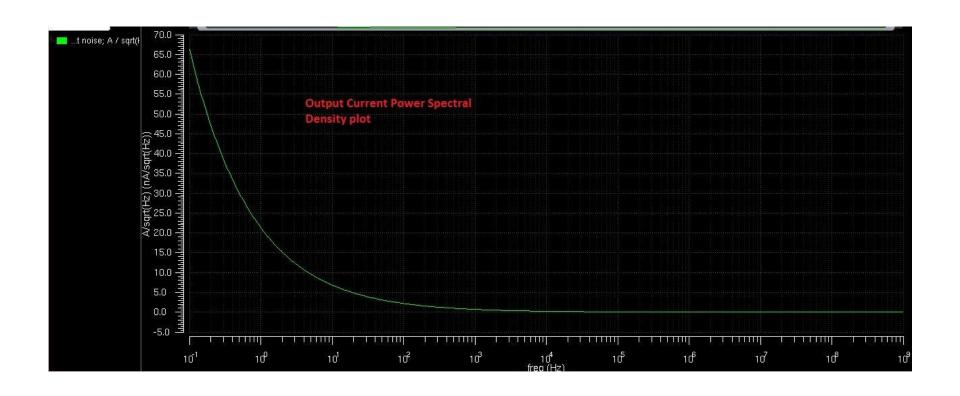
After Running Simulation



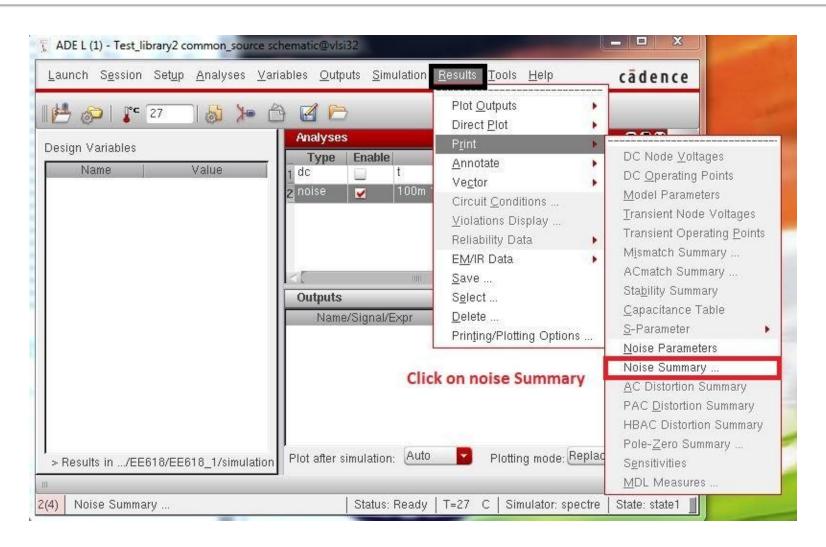
Plotting Options for Current PSD



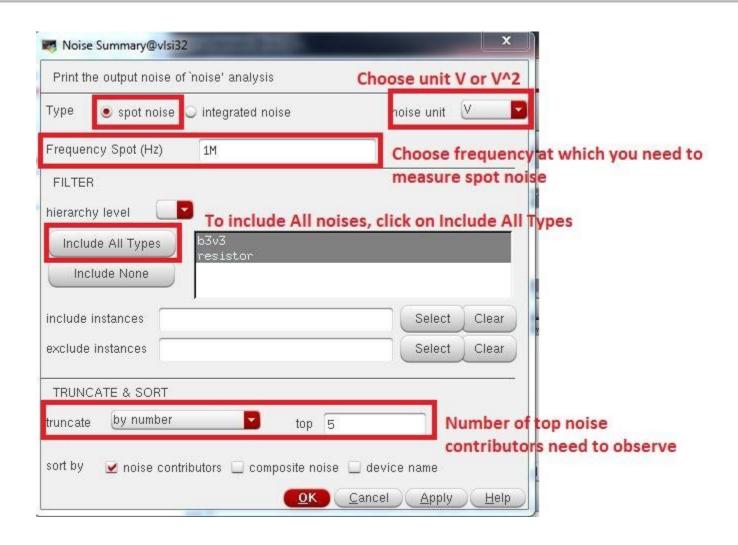
Example Current PSD plot



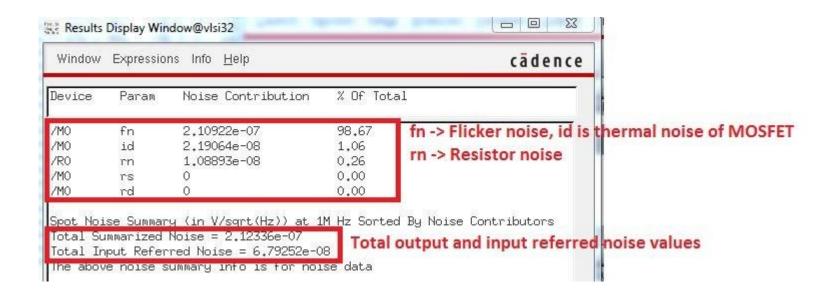
For Spot Noise Calculation (After Running simulation)



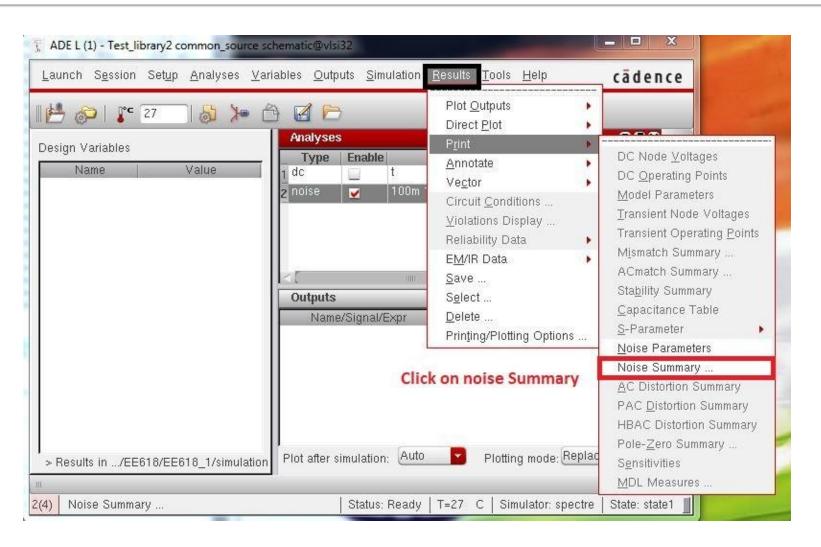
Spot noise Settings



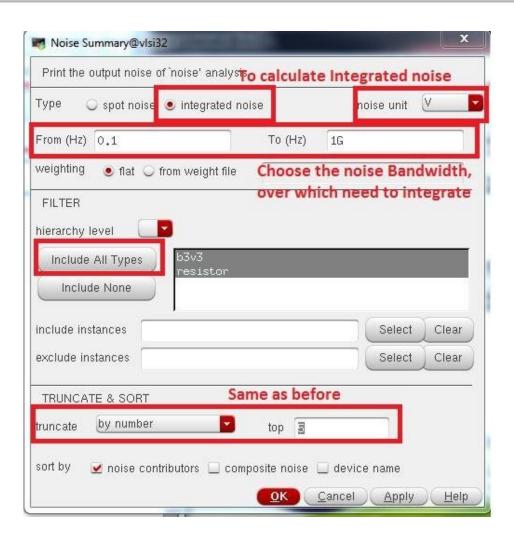
Spot Noise Result Summary



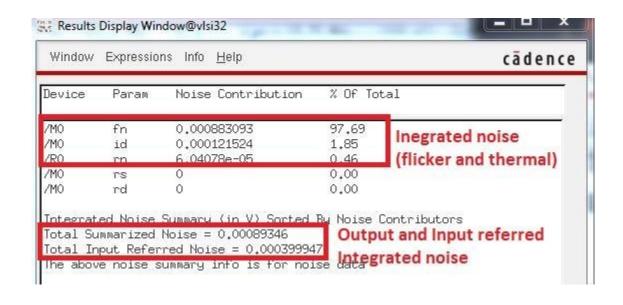
For Integrated Noise Calculation (After Running simulation)



Settings for Integrated Noise



Integrated Noise Result Summary



END