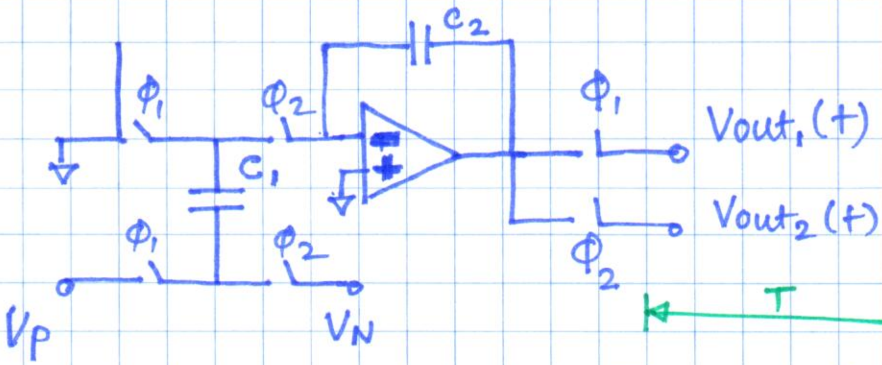
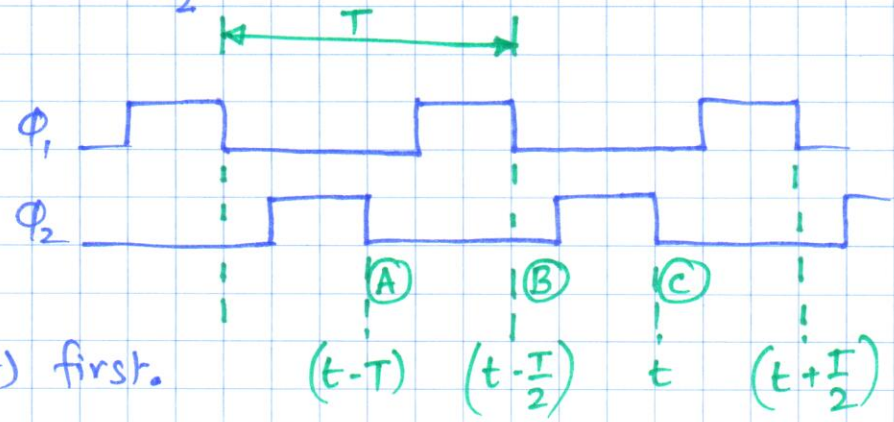
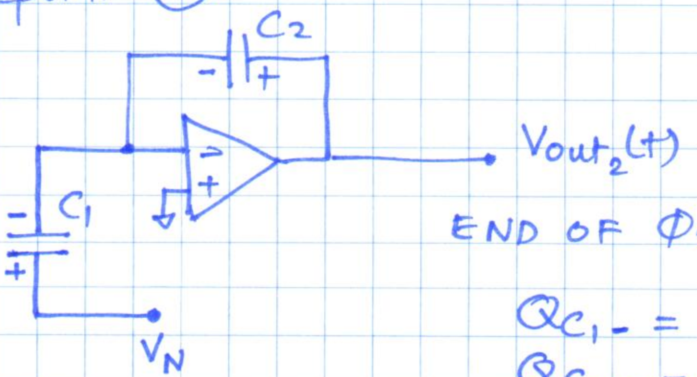
Parasitic Insensitive Switched-Capacitor Integrator





Lets figure out $V_{out_2}(t)$ first.

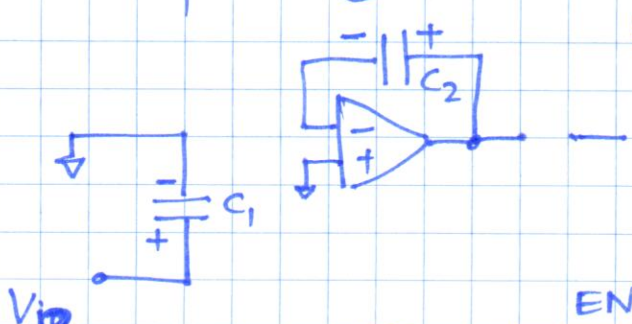
@ Timepoint A



END OF Φ_2

$$Q_{C_1-} = -C_1 V_N(t-T)$$
$$Q_{C_2-} = -C_2 V_{out_2}(t-T)$$

@ Timepoint B

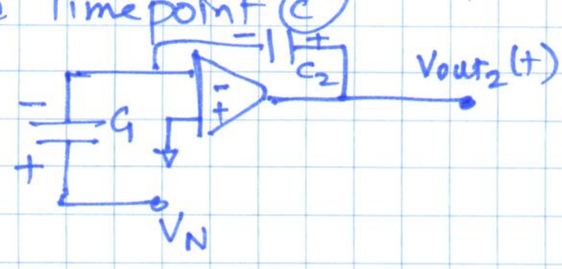


END OF Φ_1

$$Q_{C_1-} = -C_1 V_P(t-\tfrac{T}{2})$$
$$Q_{C_2-} = -C_2 V_{out_2}(t-T)$$

END OF Φ_2 - charge redistribution

@ Timepoint C



$$Q_{C_1-} = -C_1 V_N(t)$$
$$Q_{C_2-} = -C_2 V_{out_2}(t)$$

From Ⓑ to Ⓒ – Charge conserved on capacitor plates connected to opAMP. -ve i/p

$$\underbrace{Q_{C_1-} + Q_{C_2-}}_{B} = \underbrace{Q_{C_1-} + Q_{C_2-}}_{C}$$

$$-C_1 V_p\left(t-\frac{T}{2}\right) - C_2 V_{out_2}(t-T) = -C_1 V_N(t) - C_2 V_{out_2}(t)$$

Div by $-C_2$

$$\frac{C_1}{C_2} V_p\left(t-\frac{T}{2}\right) + V_{out_2}(t-T) = \frac{C_1}{C_2} V_N(t) + V_{out_2}(t)$$

Z - Xform

$$\frac{C_1}{C_2} z^{-1/2} V_p(z) + z^{-1} V_{out_2}(z) = \frac{C_1}{C_2} V_N(z) + V_{out_2}(z)$$

$$V_{out_2}(z) = \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1 - z^{-1}}}_{\text{(Half Delay)}} V_p(z) - \underbrace{\frac{\left(\frac{C_1}{C_2}\right)}{1 - z^{-1}}}_{\text{(Zero Delay)}} V_N(z)$$

$$V_{out_1}(z) = z^{-1/2} V_{out_2}(z)$$

$$V_{out_1}(z) = \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1}}{1 - z^{-1}}}_{\text{(Unit Delay)}} V_p(z) - \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1 - z^{-1}}}_{\text{(Half Delay)}} V_N(z)$$

$\left(\frac{C_1}{C_2}\right) \rightarrow$ Integrator constant

$\frac{1}{1-z^{-1}} \rightarrow$ Integrator function

Both (+ve) & (-ve) i/ps. achieved

Recap Integrator XF $H(s) = -\frac{1}{sCR} = -\frac{\omega_0}{s}$

$|H(j\omega)| = \omega_0/\omega \qquad \angle H(j\omega) = 90^\circ$

Lets compare with discrete-time integrators.

$z = e^{j\omega T}$

Zero delay Integrator $\frac{\left(\frac{C_1}{C_2}\right)}{1 - z^{-1}} = \frac{\left(\frac{C_1}{C_2}\right)}{1 - e^{-j\omega T}} \left(\frac{* \, e^{j\omega \frac{T}{2}}}{* \, e^{j\omega T/2}}\right)$

$$\frac{\left(\frac{C_1}{C_2}\right)}{1 - z^{-1}} = \frac{\left(\frac{C_1}{C_2}\right) e^{j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}$$

$$= \frac{\left(\frac{C_1}{C_2}\right) e^{j\omega T/2}}{2j \sin\left(\frac{\omega T}{2}\right)} \cdot \left(\frac{* \, \omega T}{* \, \omega T}\right)$$

$$= \underbrace{\frac{1}{j\omega}}_{1/s} \cdot \underbrace{\left(\frac{C_1}{C_2 \cdot T}\right)}_{\omega_0 = f_s\left(\frac{C_1}{C_2}\right)} \underbrace{\frac{(\omega T/2)}{\sin(\omega T/2)}}_{\text{Magnitude Error}} \underbrace{e^{j\omega T/2}}_{\text{phase error}}$$

Similarly

One Delay Integrator $= \frac{\left(\frac{C_1}{C_2}\right) z^{-1}}{1 - z^{-1}}$

$$= \underbrace{\frac{1}{j\omega}}_{\frac{1}{S}} \cdot \underbrace{\left(\frac{C_1}{C_2 \, T}\right)}_{\omega_0 = f_S\left(\frac{C_1}{C_2}\right)} \cdot \underbrace{\frac{(\omega T/2)}{\sin\left(\frac{\omega T}{2}\right)}}_{\text{Magnitude Error}} \underbrace{e^{-j\omega T/2}}_{\text{phase Error}}$$

$$\underline{\text{Half Delay Integrator}} = \frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1 - z^{-1}}$$

$$= \frac{\left(\frac{C_1}{C_2}\right) e^{-j\omega T/2}}{1 - e^{-j\omega T}} = \frac{\left(\frac{C_1}{C_2}\right)}{e^{j\omega T/2} - e^{-j\omega T/2}}$$

$$= \frac{(C_1/C_2)}{2j \sin\left(\frac{\omega T}{2}\right)} = \frac{\left(\frac{C_1}{C_2}\right) \omega T}{2j\omega T \sin\left(\frac{\omega T}{2}\right)}$$

$$= \underbrace{\frac{1}{j\omega}}_{\frac{1}{s}} \cdot \underbrace{\left(\frac{C_1}{C_2 \cdot T}\right)}_{\omega_o = f_s\left(\frac{C_1}{C_2}\right)} \underbrace{\frac{(\omega T/2)}{\sin\left(\frac{\omega T}{2}\right)}}_{\text{Magnitude Error}} \cdot \underbrace{}_{\text{NO PHASE ERROR!}}$$

Half-Delay Integrator — Lossless Discrete Integrator

Quality $\quad Q \to \infty \quad$ [Since expression is imaginary) No real part.

$$\underline{\text{Zero Delay}} \quad \frac{1}{1 - z^{-1}} = \frac{1}{1 - e^{-j\omega T}} = \frac{1}{(1 - \cos\omega T) + j\sin\omega T}$$

$$\underline{\text{Quality}} \quad Q = \frac{\text{Imag}}{\text{Real}} = \frac{\sin\omega T}{1 - \cos\omega T} \qquad (+ve)\ Q$$

$$\underline{\text{One Delay}} = \frac{z^{-1}}{1 - z^{-1}} = \frac{e^{-j\omega T}}{1 - e^{-j\omega T}} = \frac{1}{e^{j\omega T} - 1} = \frac{1}{(\cos\omega T - 1) + j\sin\omega T}$$

$$Q = \frac{\text{Imag}}{\text{Real}} = \frac{\sin\omega T}{\cos\omega T - 1} \qquad (-ve)\ Q.$$

Reference: Design Tech. for MOS SC ladder filters. G.M. Jacobs et.al. / CAS Dec 1978

Magnitude Error $= \dfrac{\left(\frac{\omega T}{2}\right)}{\sin\left(\frac{\omega T}{2}\right)}$

$$= \frac{\frac{2\pi f}{2 \cdot f_s}}{\sin\left(\frac{2\pi f}{2 \cdot f_s}\right)} = \frac{\pi f/f_s}{\sin(\pi f/f_s)}$$

$f_s = \frac{1}{T}$ Sample rate

$f \rightarrow$ max freq of interest in filter

$(f/f_s)^{-1}$	Mag Error
5	1.0689
10	1.0166
15	1.0073
20	1.004124
25	1.002637

Better than cap matching error of 0.1%

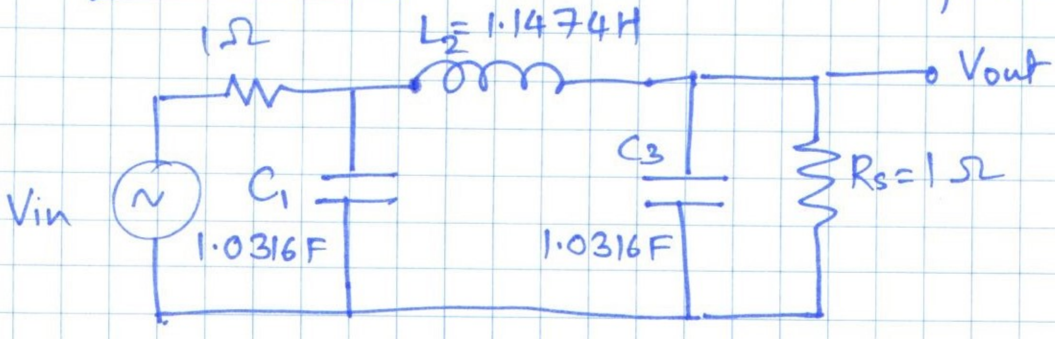
S.C. Filter Design Example.

Design a Chebyshev filter to meet following requrement

* 0.1 dB ripple
* 10 MHz ripple BW
* Stopband Atten. 40 dB
* Stopband 60 MHz

3rd order

RLC filter based on tables provided in lect 19

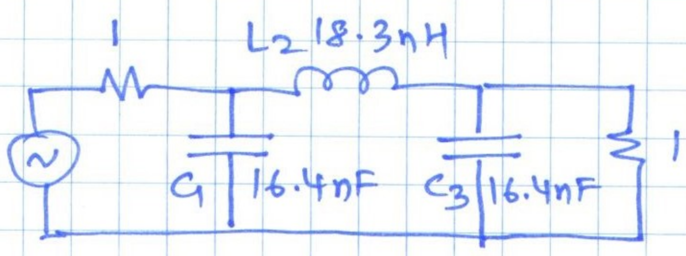


$\omega_{ripple\,bw} = 1\,rad/s$ Desired $\omega_{rippleb} = 2\pi \times 10\,MHz$

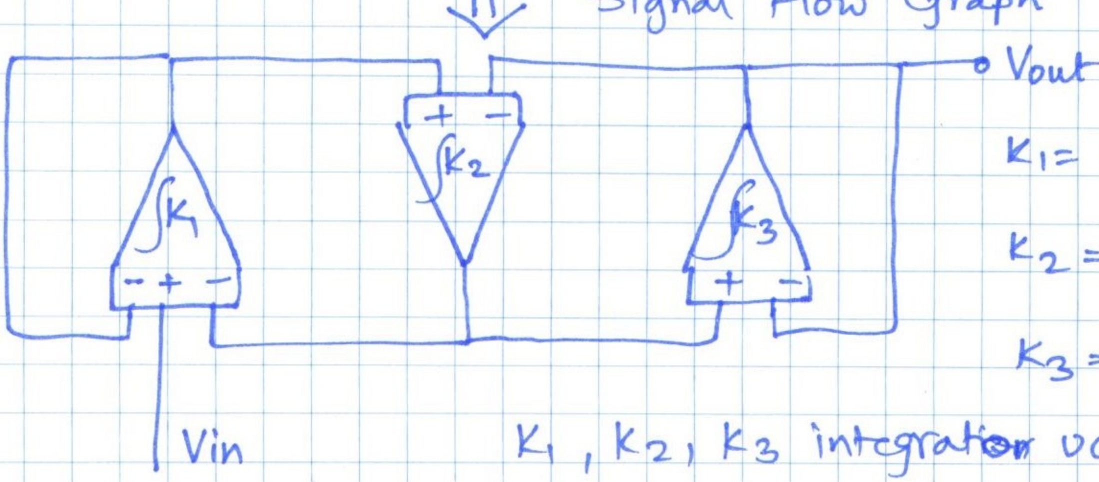
$= 62.8\,Mrad/s.$

$$C_3 = C_1 = \frac{1.0316F}{62.8M} = 16.4nF$$

$$L_2 = \frac{1.1474H}{62.8M} = 18.3nH.$$



⇓ Signal Flow Graph



$K_1 = \frac{1}{C_1}$

$K_2 = \frac{1}{L_2}$

$K_3 = \frac{1}{C_3}$

K_1, K_2, K_3 integration UGF

Connecting to switched-cap integrators

* 10MHz ripple BW → 200MHz = f_s (20x)

$$\boxed{\omega_0 = f_s \cdot \left(\frac{C_1}{C_2}\right)}$$

For integrator 1 & 3.

$$\omega_0 = f_s\left(\frac{C_1}{C_2}\right) = \frac{1}{16.4n}$$

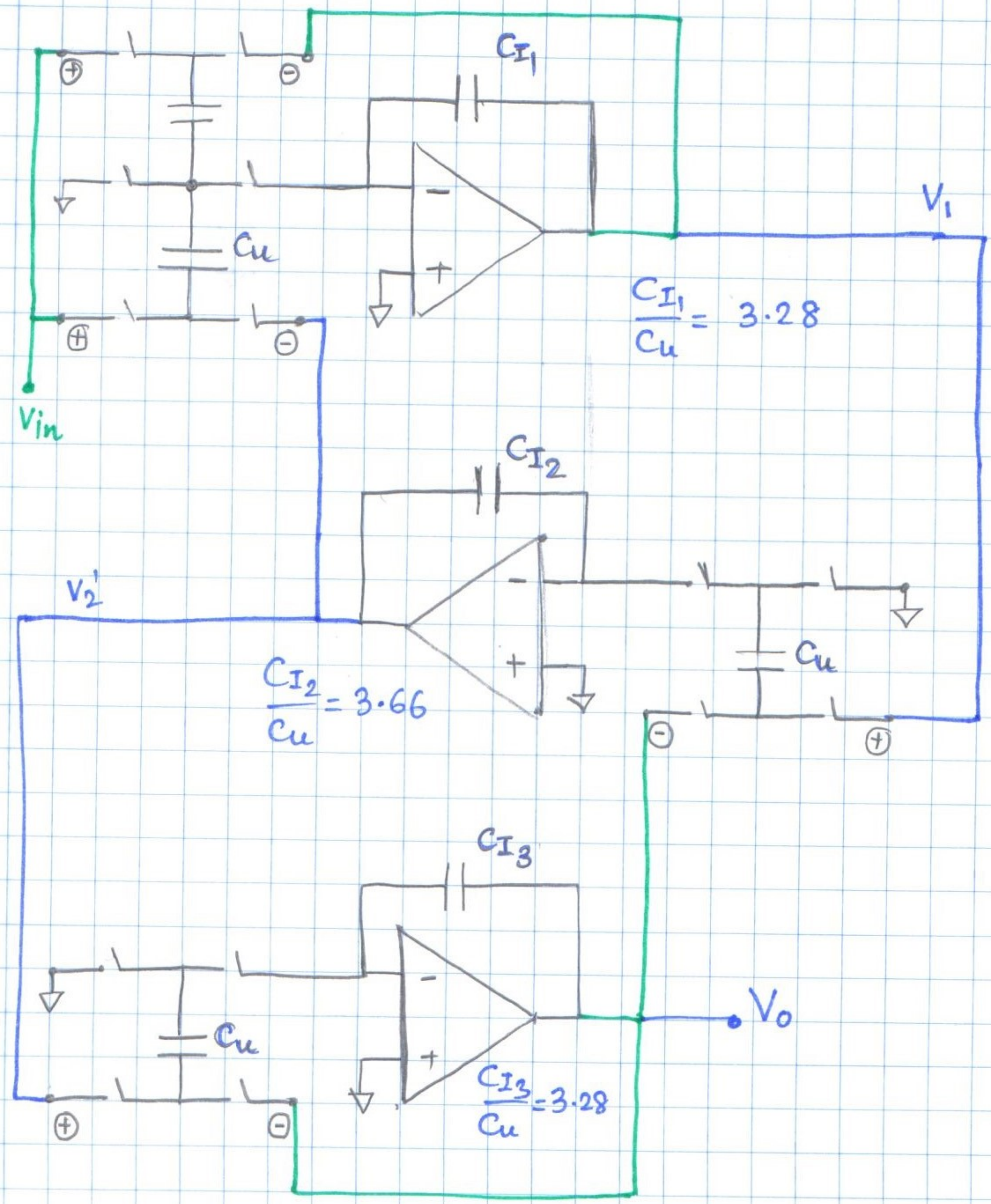
$$\frac{C_2}{C_1} = f_s \times 16.4n = 200 \times 10^6 \times 16.4 \times 10^{-9}$$

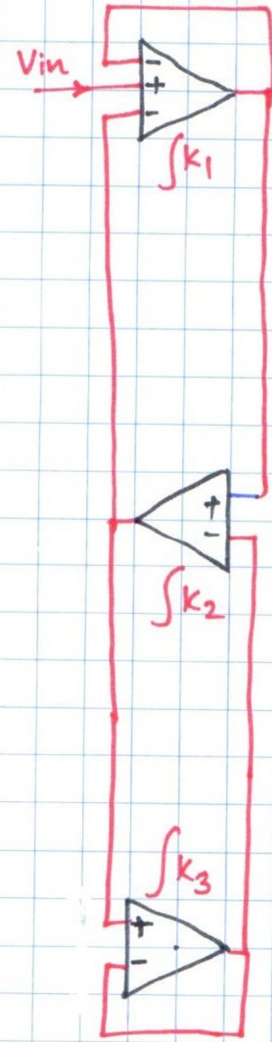
$$\boxed{= 3.28}$$

For integrator 2

$$\omega_0 = f_s\left(\frac{C_1}{C_2}\right) = \frac{1}{18.3n}$$

$$\boxed{\frac{C_2}{C_1} = 3.66}$$

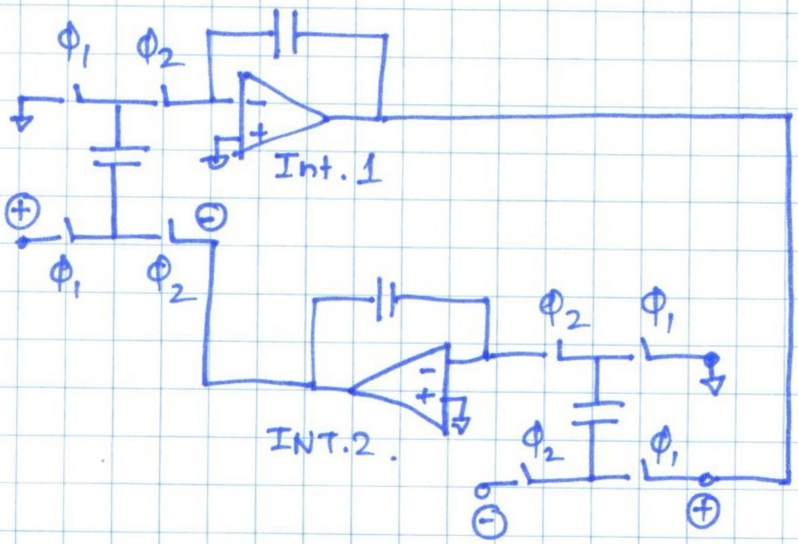




clocking – To avoid phase errors (from integrator)
→ half delay from each integrator.
→ One delay per loop of two integrators.

→ LDI (Lossless Discrete Integrator) Clocking.

LDI Clocking — ① Same Phase Clocking



INT 1 – half delay

INT 2 – half delay

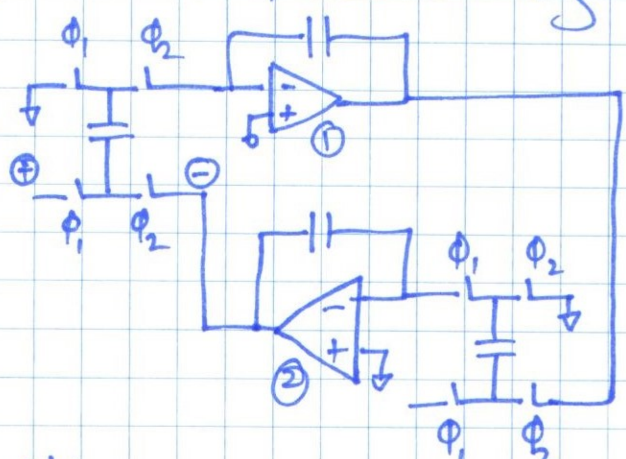
→ One clock period delay around the loop

→ LDI clocking

→ Opamp 1 & 2 both settle in ϕ_2
— idling in phase ϕ_1

→ series settling of two opamps – BW shrinkage effect

② Alternate Phase Clocking



INT 1 → Zero delay

INT 2 → One delay

Total One delay around loop

LDI Clocking

opamp 1 settles during ϕ_2

opamp 2 settles during ϕ_1