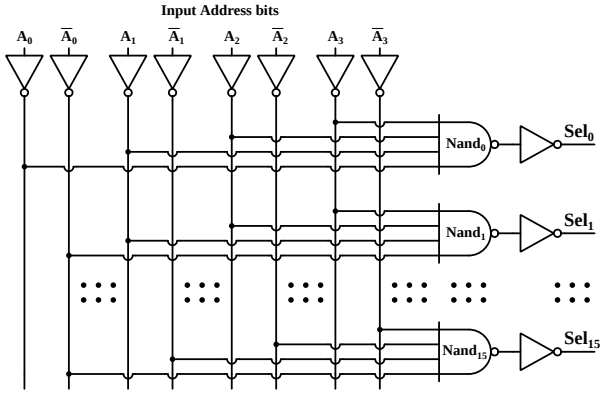
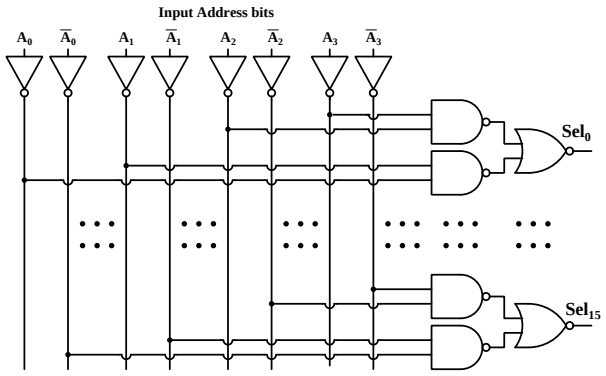
For a given CMOS process, the mobility correction factor γ for PMOS transistor widths is 2.5. The parasitic delay of gates may be taken to be proportional to the sum of the widths of transistors directly connected to the output terminal in a minimum sized gate. The parasitic delay of an inverter (p_{inv}) is 2 in units of τ, the propagation delay of a minimum sized inverter driving another minimum sized inverter without including the parasitic delay.

We want to compare two circuits to implement a 4 to 16 decoder. In circuit (i), appropriate combinations of address bits and their complements are given to 4-input-NAND gates, and their outputs are connected to inverters. In circuit (ii), combinations of address bits and their complements go to 2-input-NAND gates and their outputs are combined pair wise by 2-input-NOR gates to generate the select outputs as shown.



Decoder (i) with 4 input NANDs and inverters.

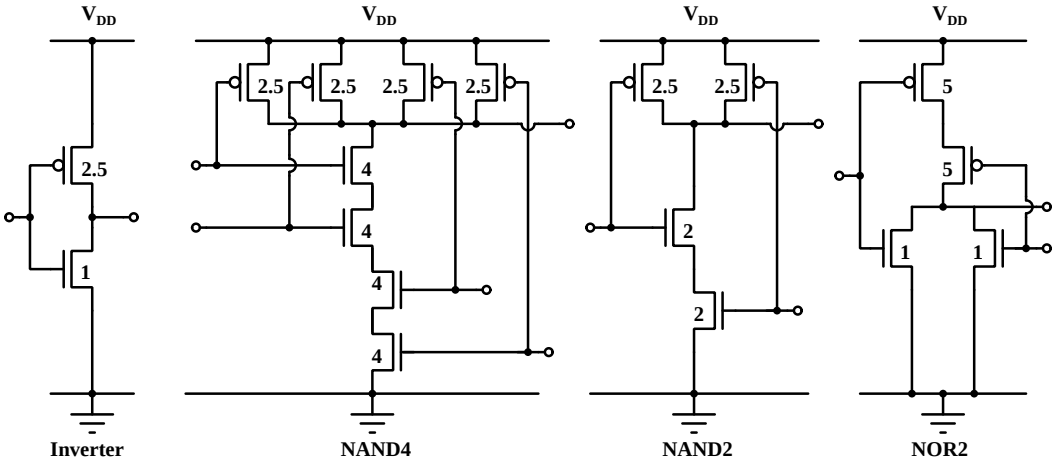


Decoder (ii) with 2 input NANDs and 2 input NORs

In both circuits, the inverters at the input are minimum sized and each select output is loaded with capacitance equivalent to 128 minimum sized inverters. All transistors use minimum channel length.

Compute the logical effort and parasitic delay for all the types of gates involved in the above circuits.

The figure below shows the gates with transistor widths to be used for providing the same output drive as a minimum inverter.



In case of 4 input NAND, there are 4 n channel transistors in series. So each must be sized to 4 times the width of the n channel transistor used in the minimum inverter. 4 p channel transistors are in parallel, so each has the same size as the p channel transistor in the minimum inverter – that is, 2.5 times the width of the n channel transistor in the minimum inverter.

Similarly, the 2 input NAND has two n channel transistors in series with a size of 2 and two p channel transistor with a size of 2.5 in parallel. The 2 input NOR has two n channel transistors in parallel, so each is the same size as the n channel transistor in the minimum inverter. The p channel transistors are in series, so each must be sized to 5.

The logical effort of an inverter is 1 by definition and its parasitic delay has been given to be 2. The logical effort for a gate is proportional to the input capacitance (and hence, total transistor width) connected to a given input. Therefore

$$g = \frac{1}{3.5} \times \text{sum of transistor widths connected to the input.}$$

The parasitic delay can be estimated to be proportional to the total transistor width connected to the output terminal. Therefore,

$$p = \frac{2}{3.5} \times \text{sum of transistor widths connected to the output}$$

This gives:

Gate	Width of n Trans.	Width of p Trans.	Total W at input	Total W at output	Logical Effort	Parasitic Delay
Inverter	1	2.5	3.5	3.5	1	2
4 input NAND	4	2.5	6.5	14	13/7	8
2 input NAND	2	2.5	4.5	7	9/7	4
2 input NOR	1	5	6	7	12/7	4

Find the widths for n and p channel transistors in all the gates of both circuits to minimize the total delay. (Specify the widths in units of the width of the n channel transistor in a minimum inverter).

Circuit (i) with NAND4 gates

The output of each input inverter goes to 8 NAND inputs. (There are 8 inverter outputs and 64 NAND inputs and these are equally divided). the logical effort g for 4-input-NAND gates is 13/7. Therefor the path effort for this circuit is given by

$$F = GBH = (1 \times \frac{13}{7} \times 1) \times 8 \times \frac{128}{1} = 1901.714$$

Since the circuit has 3 stages, the optimum stage effort is

$$\hat{f} = 1901.714^{1/3} = 12.38935$$

For the final inverters,

$$gbh = 1 \times 1 \times \frac{128}{C_{in}} = 12.38935, \quad \text{which gives} \quad C_{in} = 10.33146$$

For NAND gates with 4 inputs,

$$gbh = \frac{13}{7} \times 1 \times 10.33146/C_{in} = 12.38935, \quad \text{which gives} \quad C_{in} = 1.548668$$

For the input inverters,

$$gbh = 1 \times 8 \times 1.548668/C_{in} = 12.38935, \quad \text{which gives} \quad C_{in} = 1 \quad \text{as expected}$$

The final inverter is 10.33146 times the size of the minimum inverter. Therefore the n channel transistor width is 10.33146, while the p channel transistor width is $10.33146 \times 2.5 = 25.829$.

The input capacitance is in units of input capacitance of a minimum inverter. Thus, each capacitance unit represents 3.5 units of transistor width. The total transistor width at each input of the 4-input-NAND should be $3.5 \times 1.548668 = 5.420339$ width units. This width is divided in the ratio of $4 : 2.5$ between the n and p channel transistors. Therefore the n channel transistor width is $5.420339 \times 4/6.5 = 3.3356$ and the p channel transistor width is $5.420339 \times 2.5/6.5 = 2.0847$.

The input inverter is of course unit sized, and therefor n and p channel transistor widths are 1 and 2.5 respectively.

Circuit (ii) with NAND2 and NOR2 gates

The output of each input inverter again goes to 8 NAND inputs. (There are a total of 64 AND gate inputs fed by 8 inverter outputs and these are divided equally). Therefore the branch factor for the input inverters is 8 again.

The logical effort for 2-input-NAND gates is 9/7, while that for 2-input-NOR Gates is 12/7. Therefor the path effort for this circuit is given by

$$F = GBH = (1 \times \frac{9}{7} \times \frac{12}{7}) \times 8 \times \frac{128}{1} = 2256.98$$

Since the circuit has 3 stages, the optimum stage effort is

$$\hat{f} = 2256.98^{1/3} = 13.11724$$

For the last stage with NOR gates,

$$gbh = \frac{12}{7} \times 1 \times \frac{128}{C_{in}} = 13.11724 \quad \text{which gives} \quad C_{in} = 16.72825$$

For 2-input-NAND gates

$$gbh = \frac{9}{7} \times 1 \times 16.72825/C_{in} = 13.11724 \quad \text{which gives} \quad C_{in} = 1.639655$$

For the input inverters,

$$gbh = 1 \times 8 \times 1.639655/C_{in} = 13.11724 \quad \text{which gives} \quad C_{in} = 1 \quad \text{as expected}$$

Again, each capacitance unit represents 3.5 units of transistor width. Therefore the total input transistor width for NOR gates is $16.72825 \times 3.5 = 58.54889$. This is divided in the ratio $1 : 5$ between n and p channel transistors. Therefore, n channel transistor width is $58.54889/6 = 9.758149$ and the p channel transistor width is $58.54889 \times 5/6 = 48.79074$.

The total input transistor width for 2-input-NAND gates is $1.639655 \times 3.5 = 5.738794$. This is divided in the ratio $2 : 2.5$ between the n and p channel transistors. Therefore the n channel transistor width is $5.738794 \times 2/4.5 = 2.550574$ and the p channel transistor width is $5.738794 \times 2.5/4.5 = 3.188219$.

The input inverters are of course unit sized and so the n and p channel transistors have widths of 1 and 2.5 respectively.

The transistor sizes for all gates may be summarized as:

Circuit	gate	n width	p width
With NAND4	Input Inv.	1	2.5
	NAND 4	3.33	2.08
	Final Inv.	10.33	25.83
With NAND-NOR	Input Inv.	1	2.5
	NAND2	2.55	3.19
	NOR2	9.76	48.79

Compute the total delay in units of τ for both circuits.

In case of the first circuit, $\hat{f} = 12.39$. Therefore

$$D_{total} = 3\hat{f} + p_{inv} + p_{\text{NAND4}} + p_{inv} = 3 \times 12.39 + 2 + 8 + 2 = 49.17$$

For the second circuit, $\hat{f} = 13.12$. Therefore,

$$D_{total} = 3\hat{f} + p_{inv} + p_{\text{NAND2}} + p_{\text{NOR2}} = 3 \times 13.12 + 2 + 4 + 4 = 49.36$$

So the total delay is about the same in the two cases.

The optimum stage ratio ρ is a solution to the equation $\rho(1 - \ln \rho) + p_{inv} = 0$.
Find the value of ρ and the optimum logic depth for the two decoders for the specified loading. What is the total delay for the two circuits if the logic depth is made optimum by adding inverters?

p_{inv} is given to be 2. So the equation to be solved is:

$$f \equiv \rho - \rho \ln \rho + 2 = 0$$

We have

$$f' = 1 - \ln \rho - \rho \frac{1}{\rho} = -\ln \rho$$

Therefore given a guess g, the next improved guess is

$$g - \frac{f(g)}{f'(g)} = g + \frac{g - g \ln g + 2}{\ln g} = \frac{g + 2}{\ln g}$$

Starting with a guess value of 4, the successive guesses for ρ are: 4.328085, 4.319143, 4.319137, 4.319137 ....

Therefore the optimum number of stages is $\ln F / \ln \rho$.

For the circuit with NAND4, this is

$$\frac{\ln 1901.714}{\ln 4.319137} = 5.16$$

The optimum number of stages is 5, though one should also evaluate the delay for 6 stages to see which is better. The stage effort for a 5 stage design is $1901.714^{1/5} = 4.527193$. This design will add two additional inverters to the existing 2 inverters. So the parasitic delay will be $4p_{inv} + p_{\text{NAND4}} = 8 + 8 = 16$. Thus the total delay is $5 \times 4.527193 + 16 = 38.64$.

In case of a 6 stage design, 3 additional inverters will be inserted, so the parasitic delay will be $5p_{inv} + p_{\text{NAND4}} = 10 + 8 = 18$. The stage effort is $1901.714^{1/6} = 3.51985$ and so the total delay is $6 \times 3.51985 + 18 = 39.12$. Thus a 5 stage delay is optimum, with a total delay of 38.64.

For the circuits with NAND2 and NOR2, the optimum number of stages is

$$\frac{\ln 2256.98}{\ln 4.319137} = 5.28$$

Again, 5 stages should be optimum, though one should also evaluate the delay for 6 stages to see which is better. For a 5 stage design, two additional inverters will be inserted, so the parasitic delay will be $3 \times p_{inv} + p_{\text{NAND2}} + p_{\text{NOR2}} = 6 + 4 + 4 = 14$. The stage effort in this case is $2256.98^{1/5} = 4.684956$ and so the total delay is $5 \times 4.684956 + 14 = 37.42$.

For a six stage design, three inverters will be inserted, so the parasitic delay will be $4 \times p_{inv} + p_{\text{NAND2}} + p_{\text{NOR2}} = 8 + 4 + 4 = 16$. The stage effort is $2256.98^{1/6} = 3.621773$, so the total delay will be $6 \times 3.621773 + 16 = 37.73$.
In this case, the delay is about the same for a 5 stage or 6 stage design. However 5 stage design will be optimum because it has lower complexity (and marginally lower delay).