Multi-Level NAND Flash Memory with 63 nm-node TANOS (Si-Oxide-SiN-Al_2O_3-TaN) Cell Structure

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Abstract

For the first time, multi-level NAND flash memories with a 63 nm design rule are developed successfully using charge trapping memory cells of Si/SiO_2/SiN/Al_2O_3/TaN (TANOS). We successfully integrated TANOS cells into multi-gigabit multi-level NAND flash memory without changing the memory window and circuit design of the conventional floating-gate type NAND flash memories by improving erase speed. The evolved TANOS cells show four-level cell distribution which is free from program disturbance and a charge loss of less than 0.4 V at high temperature bake test.

Introduction

Charge trapping memory cells have the advantage over floating gate cells in terms of multi-level cell operation because the floating-gate interference effect hurts the cell distribution severely in sub-50nm regime [1]. However, the conventional SONOS cell programmed and erased by Fowler-Nordheim (FN) tunneling cannot be applied for high-density NAND flash memory for its poor data retention characteristics.

The use of thicker (>30Å) tunnel oxide is indispensable for improving data retention without losing erase speed. We reported previously the TANOS (Si/SiO_2/SiN/A_2O_3/TaN) device structure with high-k dielectrics as a blocking layer and higher work function metal gate for employing thicker tunnel oxide [2]. Furthermore, we presented 4 Gb single-level NAND flash memory with TANOS cells using 63 nm process technology [3]. We have designed erase threshold to be positive for the single-level NAND flash memory.

In this work, we have developed the multi-level TANOS-NAND flash memory successfully without changing a circuit design of multi-level NAND flash memory with 63nm-node floating-gate cells for the first time.

To realize the multi-level TANOS-NAND flash memory, key requirements such as program/erase speed, read retention, and program disturb window should be satisfied. Specially, the cell should have similar erase speed to the floating-gate cells in order to accept the old window gap design which was determined by the multi-level cell (MLC) window of the floating- gate cells.

Results and Discussions

The fabricated NAND string has TANOS cell structure with 35Å-thick SiO_2/60Å-thick SiN/100Å-thick Al_2O_3/TaN/WN/W. The NAND string was integrated by the process flow shown in table 1. The W/WN metal gate is deposited onto TaN of the cell and poly-silicon of peripheral transistors simultaneously. The two select transistors (SSL and GSL TR) to control signals of bit-line and common source line have the same device structure as the cell transistors.

Figures 3 and 4 show the program and erase characteristics of the fabricated 63 nm TANOS-NAND cells. For achieving the program threshold voltage (V_{TH}) of +3 V, program voltage of 17 V with time of 100 μsec is needed and for the erase V_{TH} of -3 V, erase voltage of -19 V with time of 10 msec is needed. The program and erase V_{TH} for TANOS cells is identical to that of 63 nm-NAND flash memory with floating-gate cells. The erase speed was improved through suppressing back-tunneling from a blocking oxide of Al_2O_3. For read operation of NAND string cell, the gate of unselected cell should be biased at high voltage enough to pass the program cell. The requirement is characterized by read retention measurement. Figure 5 shows read retention of 63 nm NAND-type TANOS cells. The life time is defined by read-stress time required the unselected erase cell V_{TH} to reach 0 V by read voltage stress. To satisfy 100 k read retention, the read voltage should be kept to be lower than 6.0 V for TANOS stack of 35Å/60Å/100Å.

Figure 6 shows the change of the cell V_{TH} as neighboring cells are programmed. As expected, the cell threshold is not influenced by the V_{TH} change of neighboring cells. It is the first demonstration that there is no interference effect with neighboring cells for TANOS-NAND flash memory.

For multi-level cell operation, the cell current in worst condition is 130 nA for read voltage of 5.5 V and 1.0 V bit-line voltage when the sensing gate voltage is higher of 0.2 V than the V_{TH} of On-cell as shown in Fig. 7. The value is sufficient for read operation in multi-level NAND flash memories.

Figures 8 and 9 show data retention characteristics in case of fresh and 1.2 k-cycled cells. Bake retention test was performed at 200 °C for 2 hours. There was charge loss of 0.2 V in program V_{TH} of 3.0 V for the fresh cells. The 1.2 k-cycled cells show a charge loss of less than 0.4 V. The value is comparable to that of floating-gate cells. The small difference of charge loss in the fresh and cycled cells comes from the use of thinner tunnel oxide for TANOS which is accompanied with less oxide trap generation than floating-gate cell.

Figure 10 shows program sequence for multi-level cell programming. The 2 bit per cell information is programmed by first "phase I" from the "11" state to the "10" state. In turn, at second "phase II" programming, the cells in the "11" state and the "10" state are programmed at the same time to the "01" state and "00" state, respectively.

We achieve the multi-level cell distribution by using the programming method and the self-boosting scheme for program inhibit. The cells in the "00" state keep erased state without fail bits when the cells are programmed to the "10" or "00" or "01" states by "phase I" and "phase II" programming as shown in Fig. 11. From the results, the program disturbance-free windows can be obtained for the evolved TANOS cells because the erase threshold is negative one enough to overcome program disturbance.

Conclusion

We developed successfully the multi-level NAND flash memory which consists of TANOS cells with 35Å-thick tunnel oxide using 63-nm technology for the first time. The TANOS cells show fast erase speed comparable to that of the conventional floating-gate cells even at 35Å-thick tunnel oxide and an excellent data retention. We can define the cell V_{TH} windows of four states which are same as the 63 nm-MLC NAND flash memory with floating-gate cells.

References

[1] K. Kim, et al, VLSI-TSA-TECH., pp. 88-94, 2005.
[2] C. H. Lee, et al, IEDM Tech. Dig., pp. 613-616, 2003.
[3] Y. C. Shin, et al, IEDM Tech. Dig., pp. 337-340, 2005.

- Well formation in cell and peripheral region and gate oxide formation for high voltage transistor
- Shallow Trench Isolation (STI) formation
- STI fill and planarization/Silicon nitride removal
- Gate oxide formation for low voltage transistor
- Poly-silicon deposition for peripheral region
- SiO_2-SiN-Al_2O_3-TaN formation for cell region
- WN/W material deposition for cell and peripheral region
- Gate definition (lithography and etching)

Table 1. Fabrication process flow of TANOS-NAND flash memory.

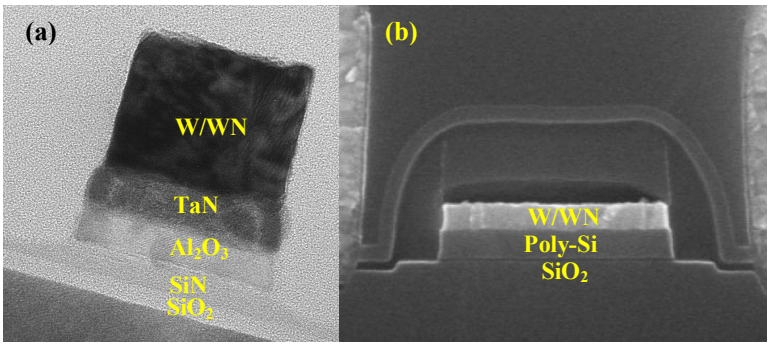

Fig. 1(a). Cross-sectional TEM image of TANOS cell (O/N/Al_2O_3=35 Å/60 Å/100 Å) and (b) cross-sectional SEM image of peripheral transistor.

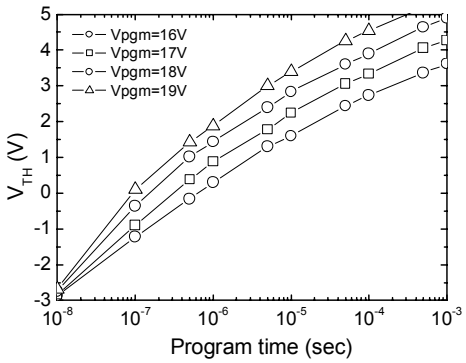

Fig. 3. Program characteristics of TANOS cells (O/N/Al_2O_3=35 Å/60 Å/100 Å).

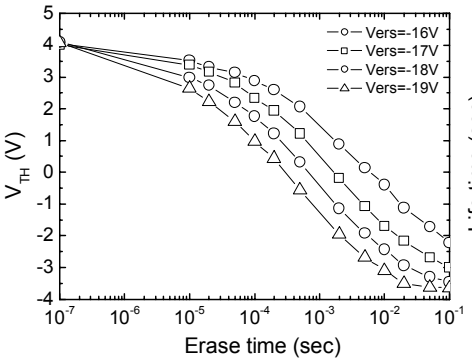

Fig. 4. Erase characteristics of TANOS cells (O/N/Al_2O_3=35 Å/60 Å/100 Å).

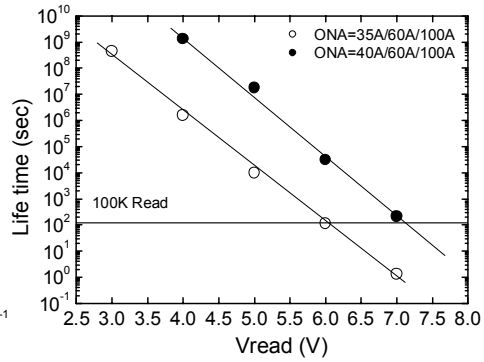

Fig. 5. Read retention of TANOS cells.

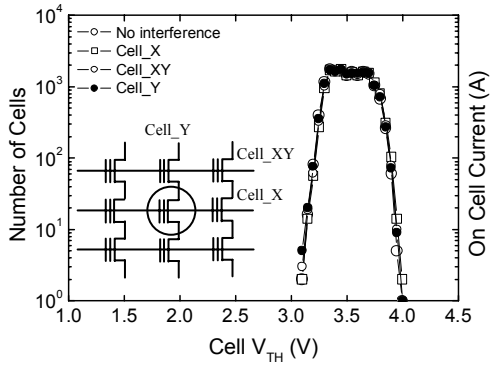

Fig. 6. Variation of cell V_{TH} distribution as adjacent cells are programmed for TANOS-NAND flash memory.

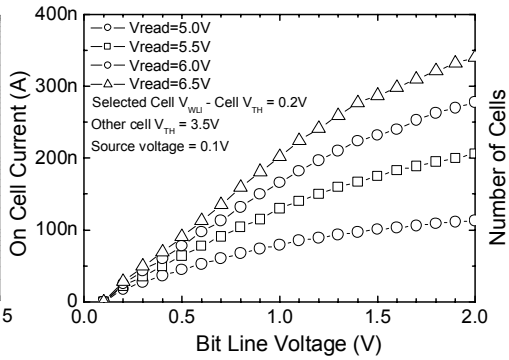

Fig. 7. "On" cell current characteristics for MLC operation in worst case situations (O/N/Al_2O_3=35 Å/60 Å/100 Å).

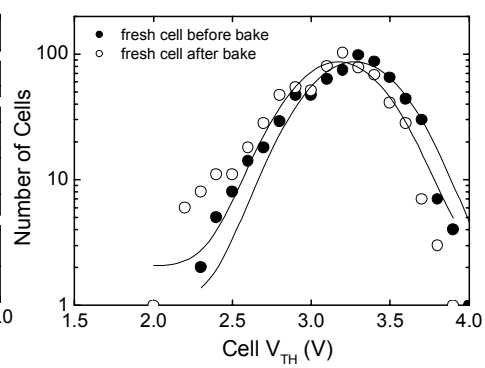

Fig. 8. Cell V_{TH} distribution after baking at 200 °C for 2 hrs. The cells are fresh state.

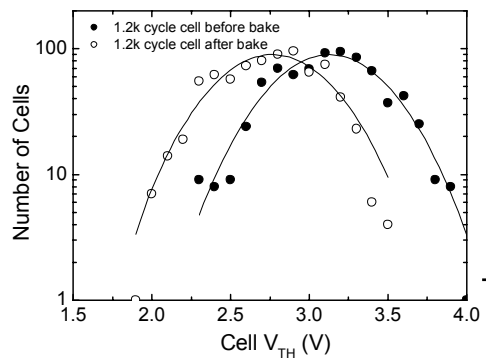

Fig. 9. Cell V_{TH} distribution after baking at 200 °C for 2 hrs. The cells are stressed by 1.2 k-cycling.

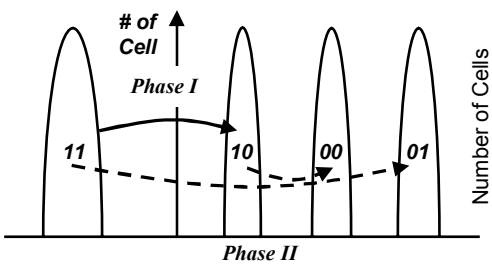

Fig. 10. Program sequence for multi-level cell operation. Phase I programming is followed by phase II programming.

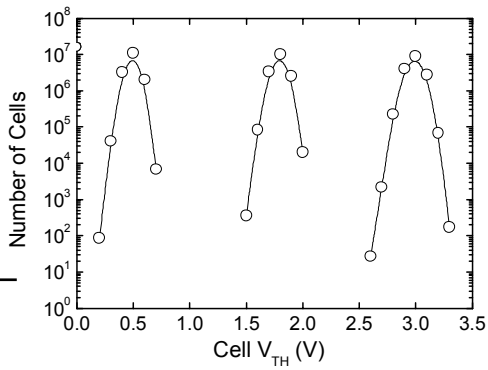

Fig. 11. Cell V_{TH} distribution of 64 M cells by multi-level cell programming.