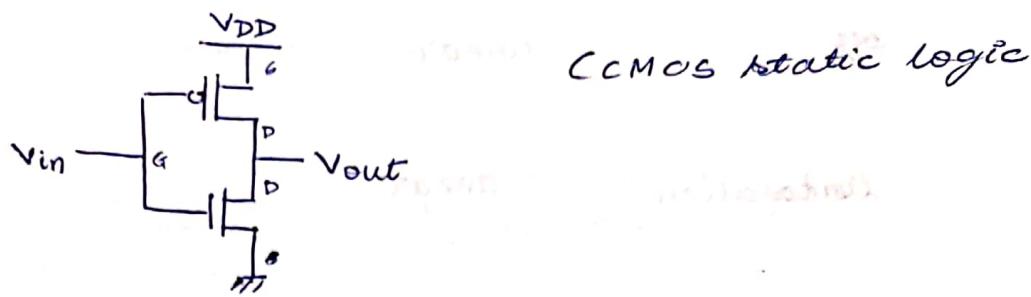


30/7

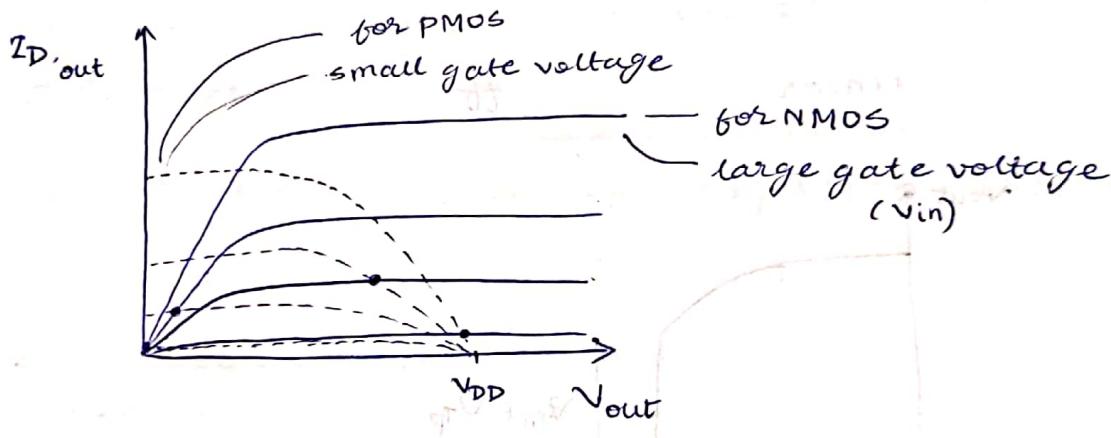
CMOS Inverter

11



- both shouldn't be on/off at the same time

↳ indeterminate output



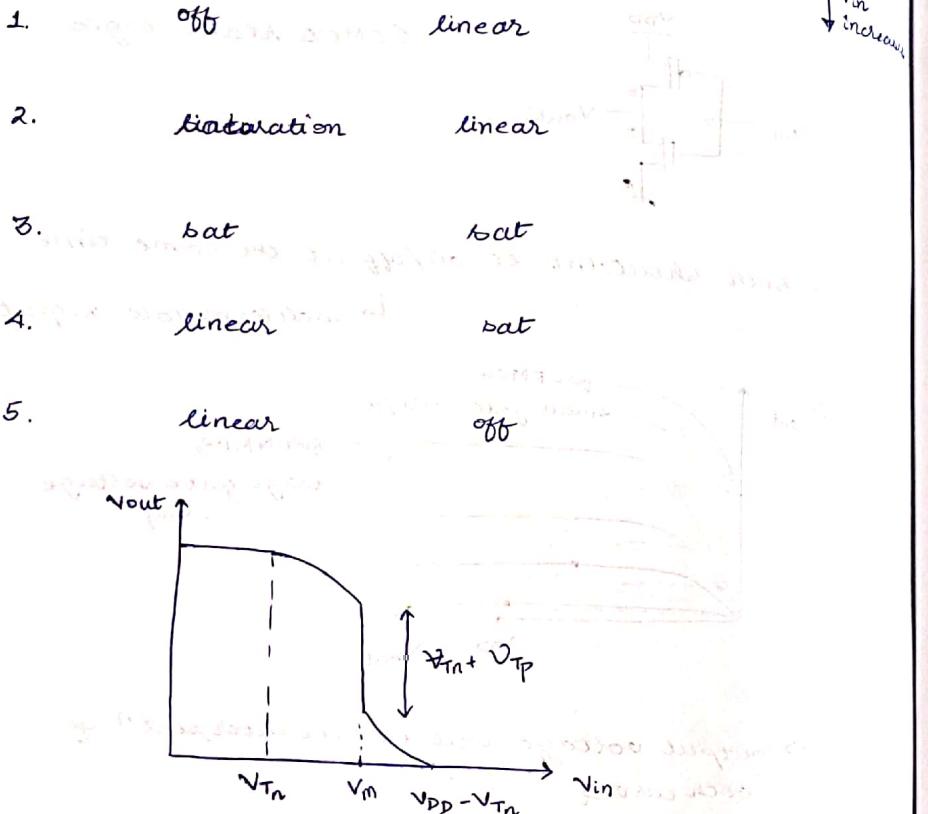
→ output voltage will be the intersection of both curves

→ for small input voltage

$$NMOS = off$$

PMOS = linear (since VDD appears at $V_{GS} - V_T > V_D$)

→ since NMOS off so current should be zero
To make current to be zero through PMOS
Drain should rise to VDD



Currents

① zero current

$$② K_n \frac{(V_i - V_{Tn})^2}{2} = K_p [(V_{Dd} - V_i - V_{Tp})(V_{Dd} - V_o) - \frac{(V_{Dd} - V_o)^2}{2}]$$

Let $\beta = \frac{K_n}{K_p}$ (if $\beta = 1$, symmetric inverter, both N & P are equally powerful)
 \Rightarrow charge & discharge time becomes equal

$$\frac{\beta}{2} (V_i - V_{Tn})^2 = (V_{Dd} - V_i - V_{Tp}) V_{Dd} - \frac{V_{Dd}^2}{2}$$

$$\frac{\beta}{2} (V_i^2 + V_{Tn}^2 - 2V_i V_{Tn}) = (V_{Dd} - V_{Tp}) V_{Dd} - V_i V_{Dd} - \frac{V_{Dd}^2}{2}$$

$$\frac{\beta}{2} V_i^2 - (2V_{Tn} + V_{Dd}) V_i + \frac{\beta V_{Tn}^2}{2} - (V_{Dd} - V_{Tp}) V_{Dd} + \frac{V_{Dd}^2}{2} = 0$$

$$V_i = \frac{1}{\beta} \left[\frac{2V_{Tn} - V_{Dd}}{2} \pm \sqrt{\left(2V_{Tn} - V_{Dd}\right)^2 - 2\beta \left(\frac{\beta V_{Tn}^2}{2} - (V_{Dd} - V_{Tp}) V_{Dd} + \frac{V_{Dd}^2}{2} \right)} \right]$$

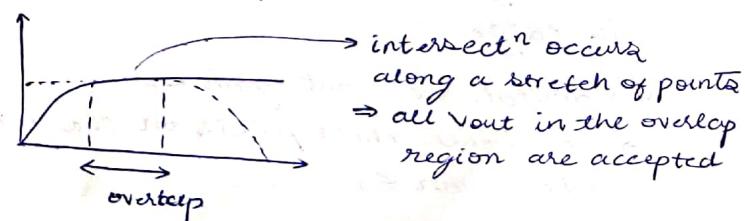
\Rightarrow we choose the sign based on which region it belongs to:

$$V_o = V_i + V_{Tn} \pm \sqrt{\left(2V_{Tn} - V_{Dd}\right)^2 - 2\beta \left(\frac{\beta V_{Tn}^2}{2} - (V_{Dd} - V_{Tp}) V_{Dd} + \frac{V_{Dd}^2}{2} \right)}$$

\rightarrow the turn on voltage puts a lower limit on our power supply

\rightarrow when $V_o = V_i + V_{Tp}$, the transistor is at the end of saturation

\rightarrow when $\beta = 1$ & $V_{Tn} = V_{Tp}$



$$\rightarrow V_{Dd} - V_{Tp} - V_i = \sqrt{\beta} (V_i - V_{Dd})$$

$$V_{Dd} - V_{Tp} + \sqrt{\beta} V_{Dd} = (1 + \sqrt{\beta}) V_i$$

$$V_i = \frac{V_{Dd} - V_{Tp} + \sqrt{\beta} V_{Dd}}{1 + \sqrt{\beta}}$$

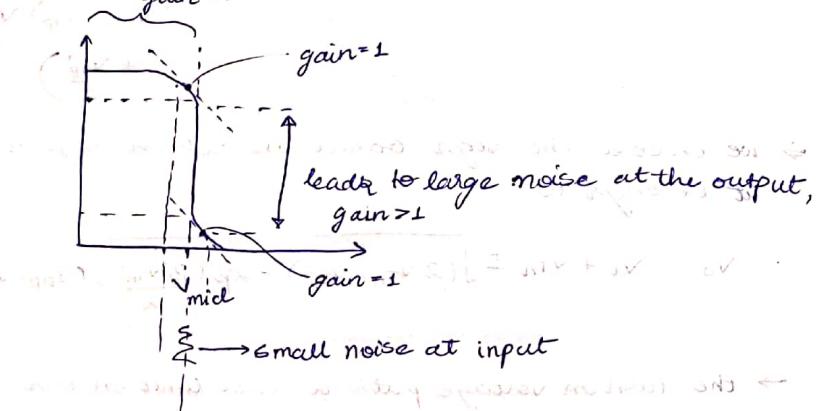
\rightarrow for this value discriminant = 0
(determines the flip point of the

$$V_{dd} - V_i - V_{Tp} = \text{effective forward bias on PMOS}$$

$$V_i - V_{dd} - V_{Tn} = \text{effective forward bias on NMOS}$$

\rightarrow when $\beta = 1$

$$V_o = V_i - V_{Tn} - \frac{\sqrt{(V_{dd} - V_i - V_{Tp})^2 - (V_{dd} - V_i - V_{Tn})^2}}{\beta}$$



- threshold should be such that it is insensitive to noise (for digital)
- Also amplification should be low (digital)
- In analog we operate in a regime, amplification is large

- For digital we want gain < 1
 \Rightarrow we choose those points on the curve where gain ≤ 1

- $\Rightarrow V_{iL}$ = input corresponding to 1st tangent
- \Rightarrow Range between V_{iL} & V_{iH} is forbidden range
- $\Rightarrow V_{iL} \leftrightarrow V_{OH}$; $V_{iH} \leftrightarrow V_{OL}$

$\rightarrow V_{OH} - V_{OL} = V_H$: if noise higher than this the noise is higher
 $V_{iL} - V_{iH} = V_L$: if noise less than this then noise is considered

$$V_H = \text{high noise margin} \quad \left. \begin{array}{l} \text{static noise margin} \\ \text{ } \end{array} \right\}$$

$$V_L =$$

$$\bullet V_o = V_i + V_{Tp} + \sqrt{(V_{dd} - V_i - V_{Tp})^2 - (V_{dd} - V_i - V_{Tn})^2}, \text{ at } \beta = 1$$

$$= V_i + V_{Tp} + \sqrt{(V_{dd} - V_{Tn} - V_{Tp})^2 - (V_{dd} - V_{Tp} + V_{Tn} - 2V_i)^2}$$

how much higher
am. I than the
minm possible value

differentiating w.r.t. V_i

$$-1 = 1 + \sqrt{V_{dd} - V_{Tn} - V_{Tp}} \left(\frac{1}{2} \right) \frac{(-2)}{\sqrt{V_{dd} - V_{Tp} + V_{Tn} - 2V_i}}$$

$$2 = \frac{V_{dd} - V_{Tn} - V_{Tp}}{V_{dd} - V_{Tp} + V_{Tn} - 2V_i}$$

$$\Rightarrow 4(V_{dd} - V_{Tp} + V_{Tn} - 2V_i) = V_{dd} - V_{Tn} - V_{Tp}$$

$$V_i = \frac{3V_{dd} - 3V_{Tp} + 5V_{Tn}}{8} = V_{iL}$$

If we assume V_{dd} , V_{Tn} , V_{Tp} to be vectors

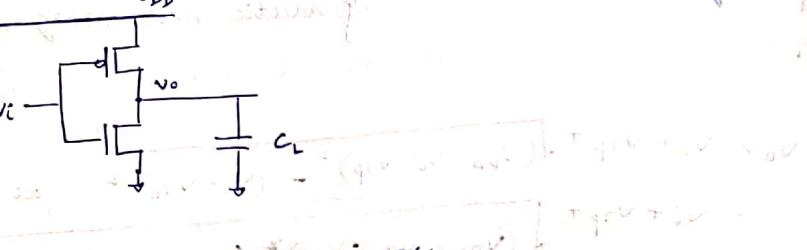
$$V_{iL} = \frac{3, 5, -3}{8}$$

corresponding $V_o = V_{OH}$

$$\Rightarrow V_{dd} - V_{Tp} + V_{Tn} - 2V_i = (1, 1, -1) - \frac{2}{8} (3, 5, -3)$$

$$= \frac{1, -1, -1}{4}$$

$$\Rightarrow V_o = \frac{(3, 5, -3)}{8} + (0, 0, 1) + \frac{(1, -1, -1)}{2}$$



a) when $V_i < V_{th}$, NMOS is off

$\Rightarrow C_L$ charges

$$I = C_L \frac{dV_o}{dt} = I_{drain, pmos} + I_{dp}$$

$$\frac{dt}{C_L} = \frac{dV_o}{I_{dp}} \quad \text{func. of time}$$

Want to find the time taken to go from

$0 \rightarrow V_{oh}$ (τ)

$$\Rightarrow \frac{\tau}{C_L} = \int_{\frac{V_i + V_{tp}}{2}}^{V_{oh}} \frac{dV_o}{K_p \left(\frac{V_{dd} - V_o - V_{tp}}{2} \right)^2} + \int_{V_{oh}}^{\frac{V_{dd} - V_{oh}}{2}} \frac{dV_o}{K_d [V_{dd} - V_o - V_{tp}] (V_{dd} - V_o)}$$

However from $0 \rightarrow V_{oh}$ expression for $I_{dp} \left| \frac{1}{2} (V_{dd} - V_o)^2 \right.$ charged at $V_i + V_{tp}$

Valid only when $V_{oh} > V_i + V_{tp}$

Let $V_1 = V_{dd} - V_o$

$$V_2 = V_{dd} - V_i - V_{tp}$$

$$\frac{\tau}{C_L} = \frac{V_i + V_{tp}}{\frac{K_p V_2^2}{2}} = \int_{V_2}^{\frac{V_{dd} - V_{oh}}{2}} \frac{dV_1}{K_p \left[V_2 V_1 - \frac{1}{2} V_1^2 \right]}$$

$$\frac{K_p \tau}{2 C_L} = \frac{V_i + V_{tp}}{V_2^2} + \int_{V_{dd} - V_{oh}}^{V_2} \frac{dV_1}{V_1 (2V_2 - V_1)}$$

partial fraction

$$= \frac{V_{in} - V_{tp}}{2} + \frac{1}{2V_2} \log \frac{V_1}{2V_2 - V_1}$$

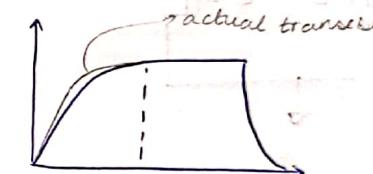
$$= \frac{V_{in} - V_{tp}}{2} + \frac{1}{2V_2} \log \frac{V_{dd} - V_{oh}}{2V_2 - V_{dd} + V_{oh}}$$

$$= \frac{V_{in} - V_{tp}}{2} + \frac{1}{2V_2} \log \frac{(2V_2 - V_{dd} + V_{oh})}{(V_{dd} - V_{oh})}$$

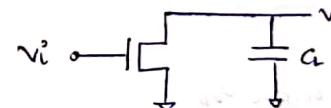
$(V_{oh} \text{ very close to } V_{dd})$
 $\Rightarrow V_{oh} = \text{const}, \text{ RHS} = \text{const}$

$\Rightarrow \tau \propto C_L$ (when $V_{oh} = \text{const}$)

\rightarrow we assume the non-linear transistor to be like a resistor and take its RC rise time value



b) when PMOS off (V_i high)



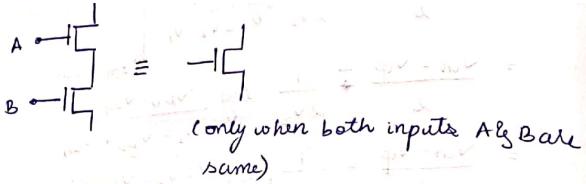
$$I_{dn} = -C_L \frac{dV_o}{dt} \quad (\text{discharging } C_L)$$

Here break-off point is $V_i - V_{tn}$

$$\tau_{\text{disch}} \propto C_L$$

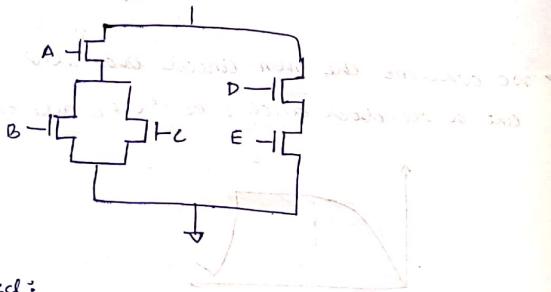
- To keep rise and fall time, $V_{tn} = V_{tp}$, $\beta = 1$ same

\Rightarrow Ratio less design



⇒ If NMOS are series then they are AND
If NMOS are parallel then they are OFF

$$A \cdot (B+c) + D \cdot E = \text{desired}$$



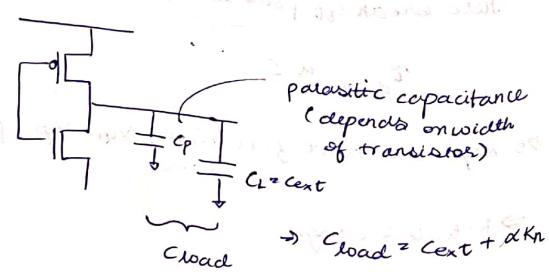
Desired:

low power
high speed
more robust

→ for more robustness need higher V_{DD}

$$V_{OH} - V_{IH} = \frac{V_{DD} + \Delta}{A}$$

→ current small → speed is low



$$\frac{C_{load}}{K_n^2} = \text{const}$$

$$\Rightarrow \frac{C_{ext} + \alpha K_n}{K_n^2} = \frac{C_{ext}}{K_n^2} + \frac{\alpha}{\tau} = \text{const}$$

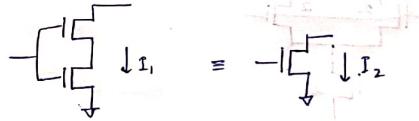
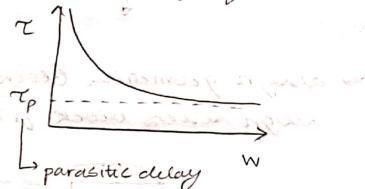
$$\begin{aligned} [\alpha_1 W_n + \alpha_2 W_p] \\ = \gamma_1 K_n + \gamma_2 K_p \\ \Rightarrow (\gamma_1 + \frac{\gamma_2}{P}) K_n \\ = \alpha K_n \end{aligned}$$

If this is large we can scale time

⇒ however if both terms are comparable, some delay associated

⇒ delay comparable to size

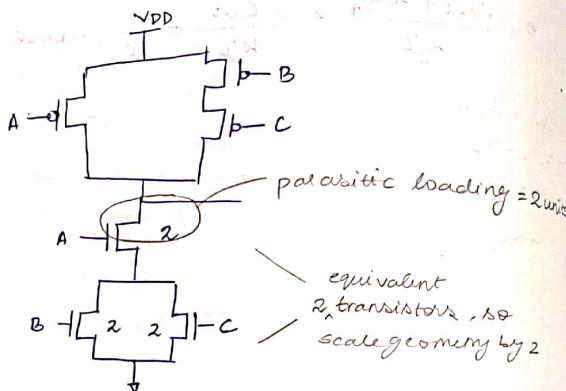
⇒ delay independent of geometry if geometry large



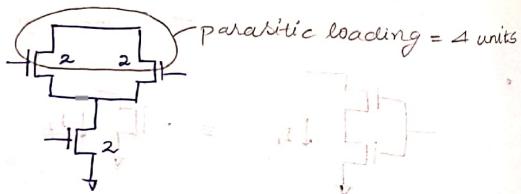
$I_1 = \frac{I_2}{2}$
→ To need to design the NMOS to draw twice the current as a single NMOS

⇒ for n transistors, make geometry of individual transistor such that current is n-times.

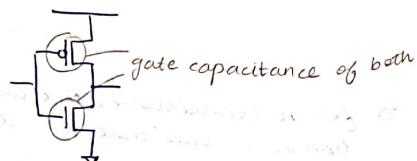
- 1) For transistors in series, multiply geometry of 1 transistor with total no. of transistors
- 2) For parallel transistors, leave geometries unchanged



→ assign geometries block wise.
assign series block first.

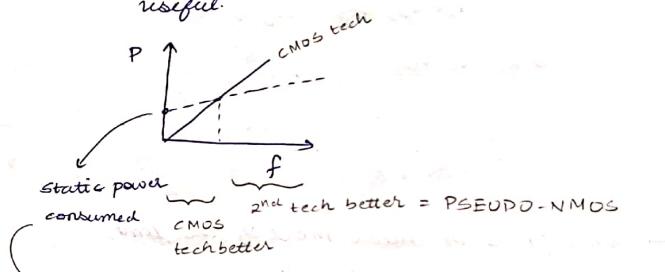


* Speed of gates determined by C_g



- Can't bring n & p channel transistor close else latch-up occurs
- But if don't bring them don't have a compact design

- capacitive loading becomes higher
- P-channel provides high loading but low current
- so we don't allow input to turn on p channel
- so we keep p channel permanently on
 - static power consumption ↑
 - But we gain dynamic power (since capacitance reduced)
 - as $C \propto f$
cap & dynamic power becomes $(\frac{1}{2})^{\text{rd}}$
- so need to see which power is dominant
- for high frequency (switching) config having dynamic power as dominant, this config. useful.



If we reduce static power, we can reduce the crossover frequency

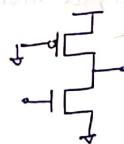
→ In CMOS tech:

if we reduce capacitance we can lower the slope, so prefer lower width transistor

→ In Pseudo-NMOS tech:

use PMOS which draws lower current

8/8



- we can connect pmos to CLK so that it is on only when clk enabled/high

- ⇒ for all $V_o < V_{tp}$, the pmos is unsaturated
- ⇒ $V_o > V_{tp}$, pmos is linear
- ⇒ $V_o \geq V_{tn} + V_{tp}$, nmos is saturated
- ⇒ $V_o \leq V_{tn} + V_{tp}$, nmos is linear

$n = p$ (out) \rightarrow voltage drop across the load is off lin $V_{DD} - V_o$

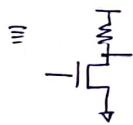
sat lin

$$V_2 = V_{DD} - V_{tp}, V_{DD} - V_o = V_1$$

$$\Rightarrow K_n \frac{(V_i - V_{tn})^2}{2} = K_p \left[V_2 V_1 - \frac{1}{2} V_1^2 \right]$$

$$\frac{B}{2} (V_i - V_{tn})^2 = V_1 V_2 - \frac{V_1^2}{2}$$

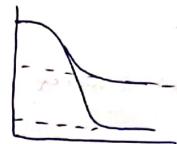
- Since pmos is linear most of the time, the $V_{tn} + V_{tp}$ drop won't occur



when β is of the order of V_{tp}

$$K_n \left[(V_i - V_{tn}) V_o - \frac{V_o^2}{2} \right] = K_p \left[V_{DD} - V_{tp} \right]^2$$

since pmos never turns off, the output never goes to zero



if β is not sufficiently high, the value settles earlier and is of no use
→ won't be able to discharge effectively

$$\beta = 4:1 \text{ (usually)}$$

- to reduce the cap (load) by $(\beta)^2$ we used only nmos, but to get a good settling value we need the β ratio to be high → nmos charac/geometry high
- dynamic power improvement limited

- If power is our concern then CMOS is preferred

$$V_{tn} \approx V_{tp} \approx \frac{V_{DD}}{5} \Rightarrow \beta = 4-6$$

- let's assume that pmos current is const at max value I_{osat} → helps to solve algebra
- we want to make the pmos weaker because the nmos has to constantly fight the current supplied by it and discharge the load
- we can make β such that V_o is low enough → fight discharge time after that

⇒ if requirements not met then solve for β using dynamic consideration

complementary Pass gate logic

2 \bar{x} readily present, however 2 wires running for each logic

$$\Rightarrow f(x_1, x_2, \dots, x_i, \dots, x_n)$$

$$f_1 = (x_1, x_2, \dots, 1, \dots, x_n)$$

$$f_0 = (x_1, x_2, \dots, 0, \dots, x_n)$$

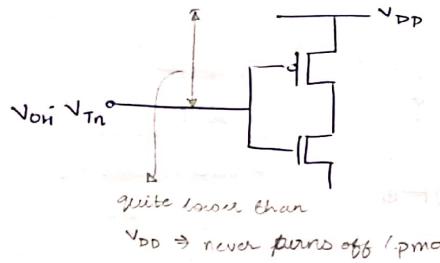
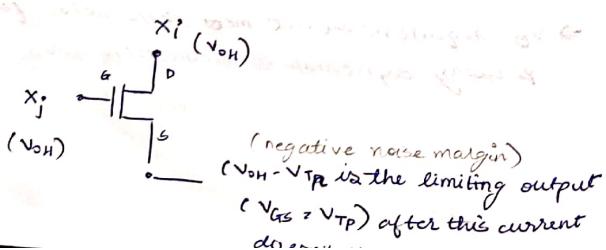
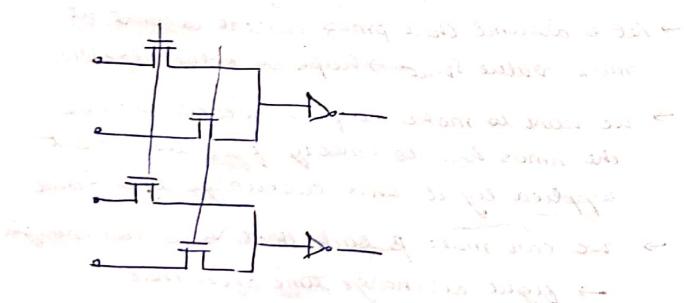
$$\Rightarrow x_i f_1 + \bar{x}_i f_0$$

[we put an inverter (static gate) at the end because the output before that has negative noise margin, so inverter helps restore the logic levels]

1/6

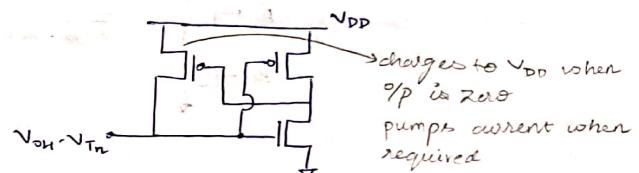
→ CPL allows compactness of structure

→ solve problem of \ominus noise margin by putting an inverter

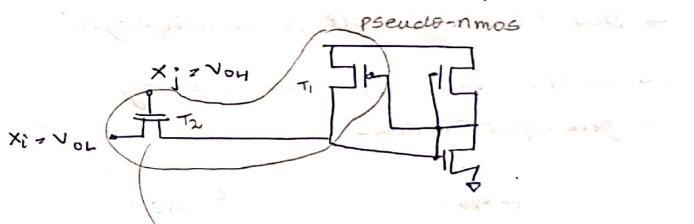


- we want the pmos to be off when gate is 1 and \bar{v}_p should be zero

- so we have problem while charging



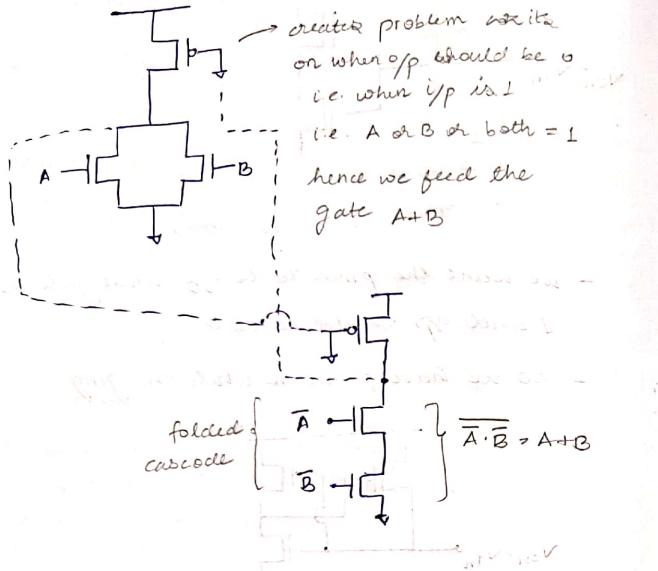
→ problem arises when we input V_{OL}



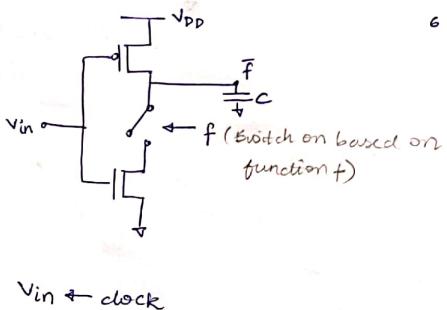
this has to stronger than T_1 to pull it down and turn it off (else T_1 will keep charging)
 T_1 doesn't have to do a lot of work hence we make it weak

consumes more power (more power in transition, less while in static)

- T_1 consumes while charging
- T_2 consumes while discharging



- This structure is a latch (cross-connection)
- In such a circuit, need to have PMOS weak
- This 'Cascade Voltage Switch logic'
- In CPL, CVSL, pseudo-nmos, we only give input to nmos



Vin ← clock

"CMOS Dynamic gate"

when clock = 0

C is charged

clock = 1

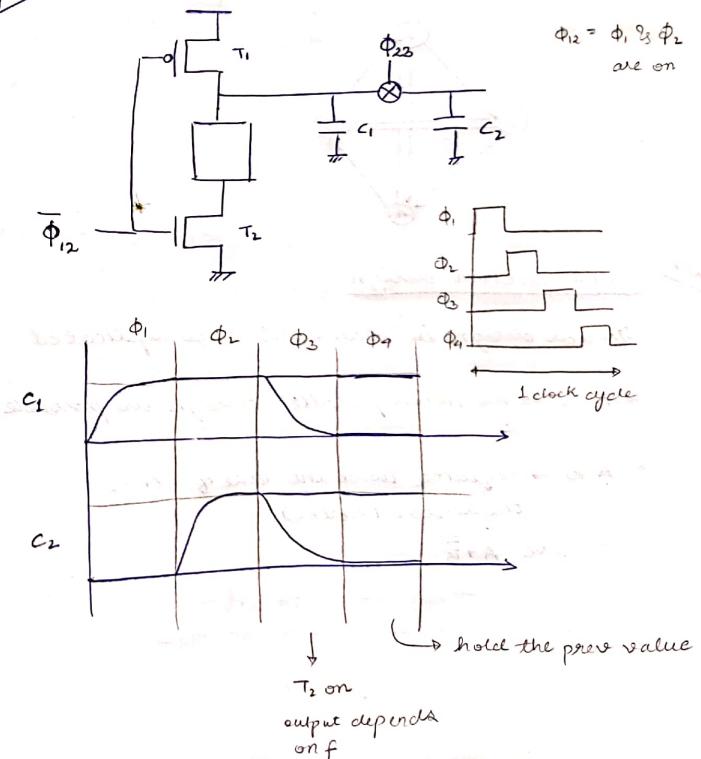
C is discharged

→ It is problematic when clock is too slow
else the cap charge would drain away (for long high clock)

→ Dynamic power ∝ clock freq.

→ when clock high, the cap charges & discharges when clock low, cap is already high

19/8



- C_2 isolated in $\phi_1 \& \phi_3$ hence o/p valid only in these cycles (phase)
- input needs to be valid in ϕ_3 (equivalent of noise margin in time)

\Rightarrow TYPE 3 GATE

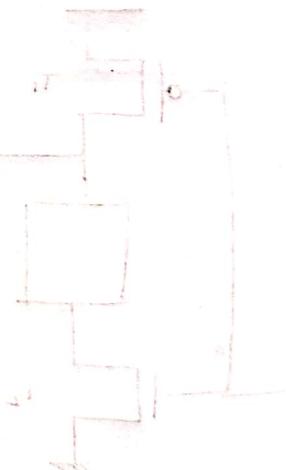
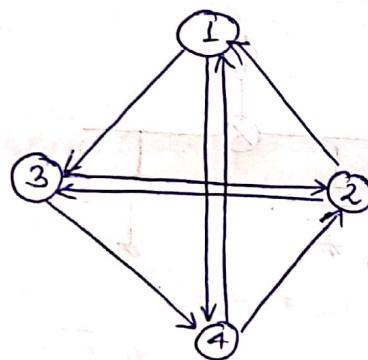
$$\text{if } \overline{\Phi_{12}} = \overline{\Phi_{23}}$$

$$\Phi_{23} = \Phi_{34}$$

then we shift by 1 phase

$$y_p = \Phi_4$$

o/p valid in $\phi_1 \& \phi_2$



22/8 Semi-custom design

Initial design is standard and replicated

\rightarrow Need to do much parallel design as possible

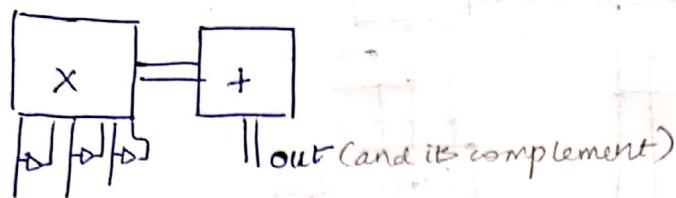
- $A \cdot B \rightarrow$ requires twice the size of other transistor (series)

\therefore use $\overline{A + B}$

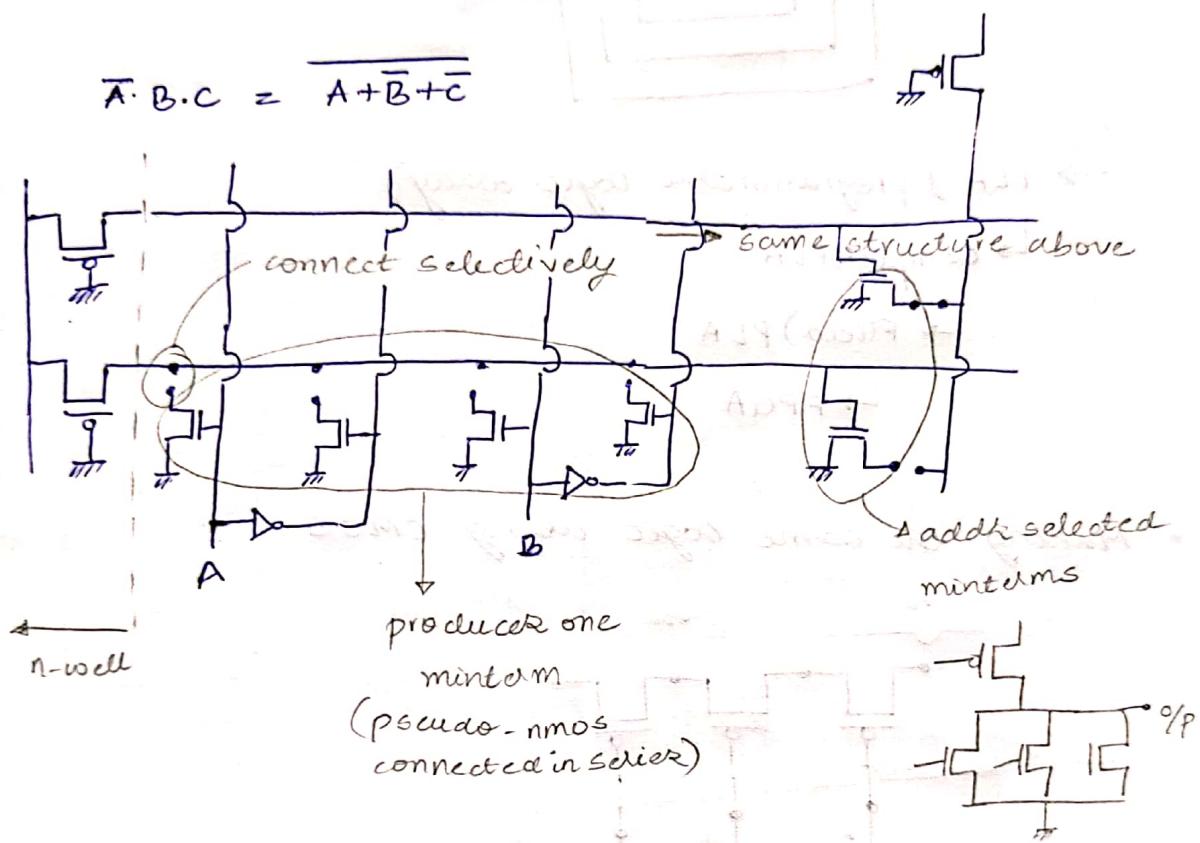
\hookrightarrow but now p-channel is series

\Rightarrow so use pseudo-nmos

- Divide logic to create several minterms and a programmable adder adds selected minterms

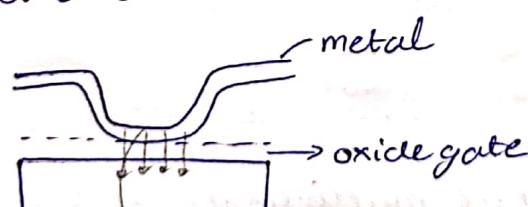


$$F \cdot B \cdot C = \overline{A + \overline{B} + \overline{C}}$$



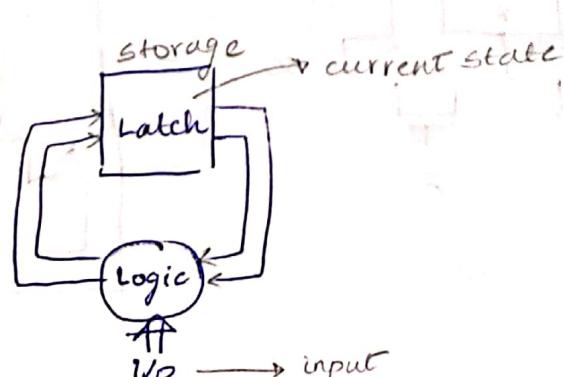
- Fuse technology (oxide fuse/anti-fuse)

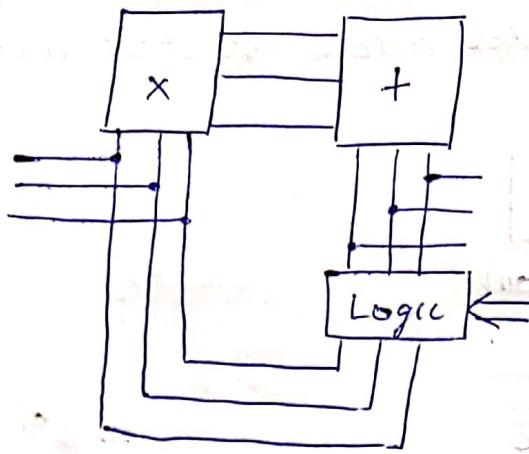
→ in order to create a switch



metal given a jolt of 100V to breakdown the oxide and connect the metals

- FSM





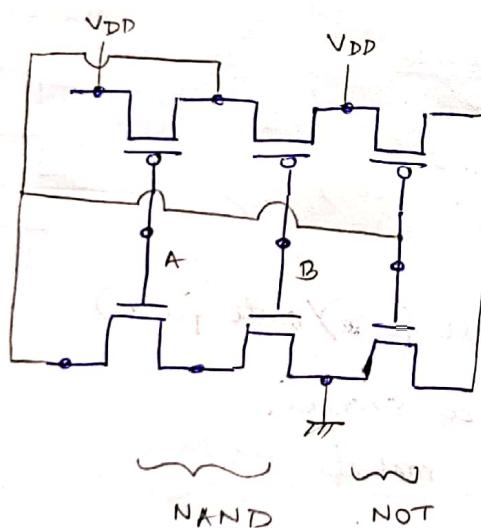
→ PLA (programmable logic array)

↳ (Complex) PLA

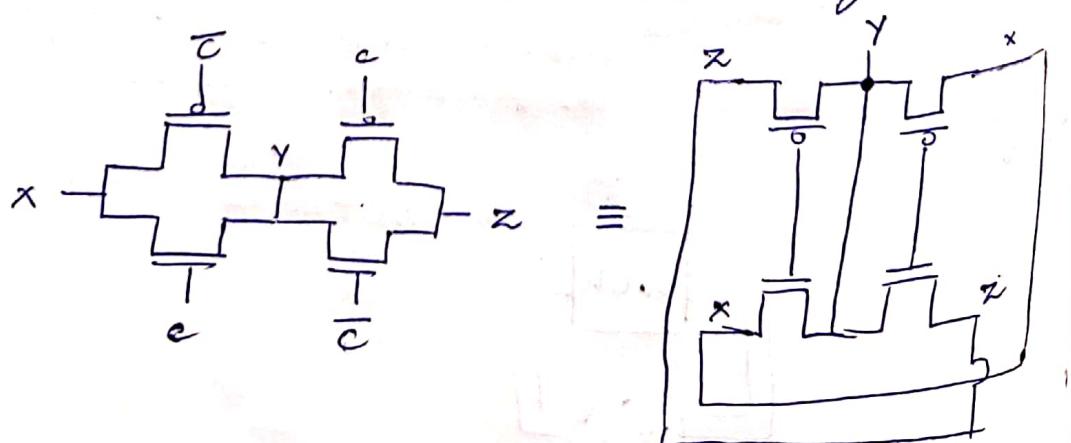
↳ F(ield) PLA

↳ FPGA

- Making the same logic using CMOS

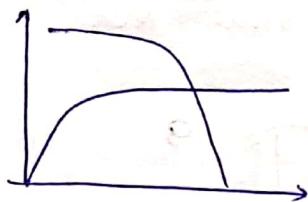


→ can't construct multiplexers this way



QUIZ solution

①



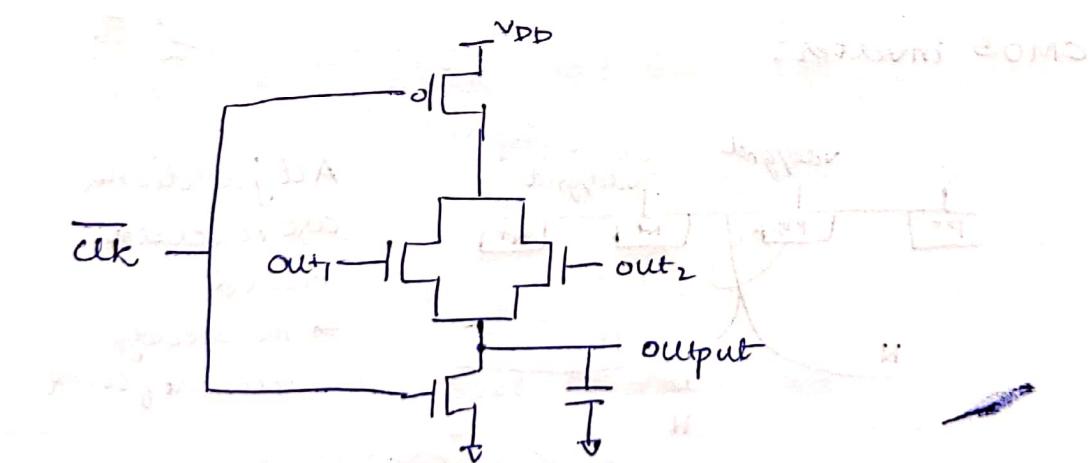
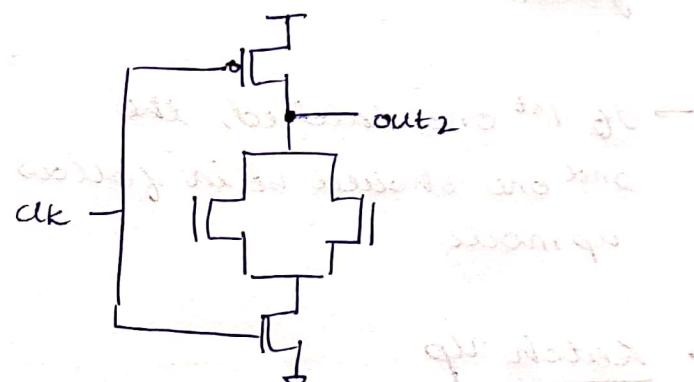
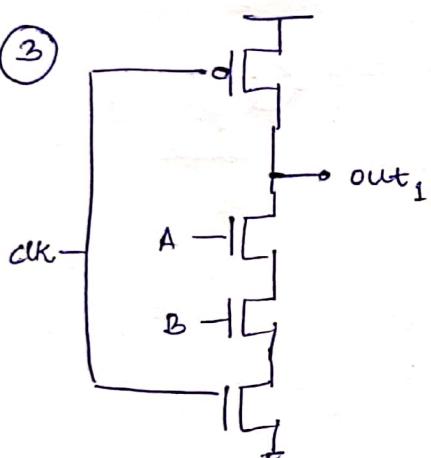
both are in sat^n

$$\frac{k_n}{2} (V_i - V_{th})^2 = \frac{k_p}{2} (V_{DD} - V_i - V_{tp})^2$$

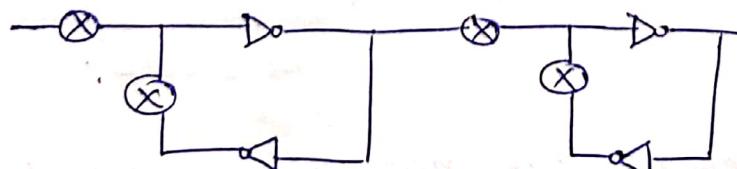
$$\sqrt{P} (V_i - V_{th}) = (V_{DD} - V_i - V_{tp})$$

$$V_i = \frac{V_{DD} - V_{tp} + \sqrt{P} V_{th}}{1 + \sqrt{P}}$$

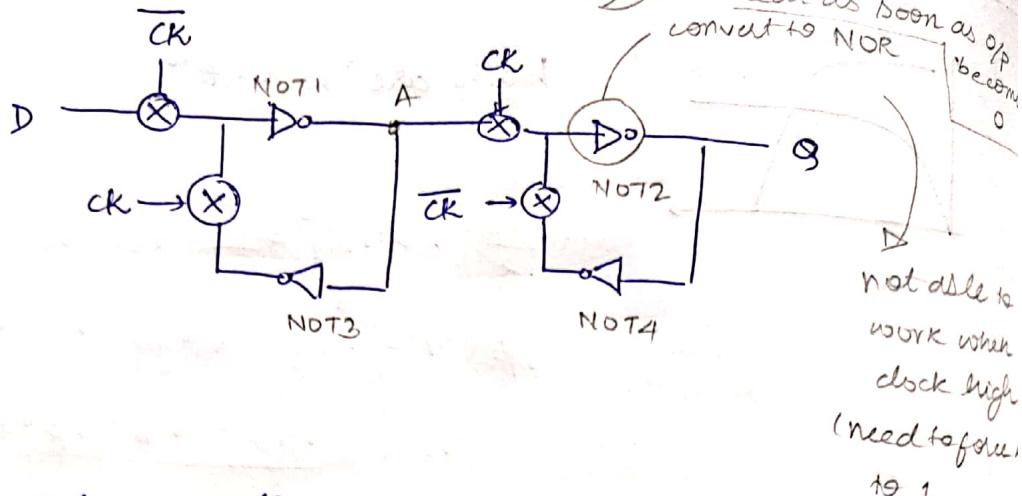
③



④



26/08

D - flipflop

To set, convert

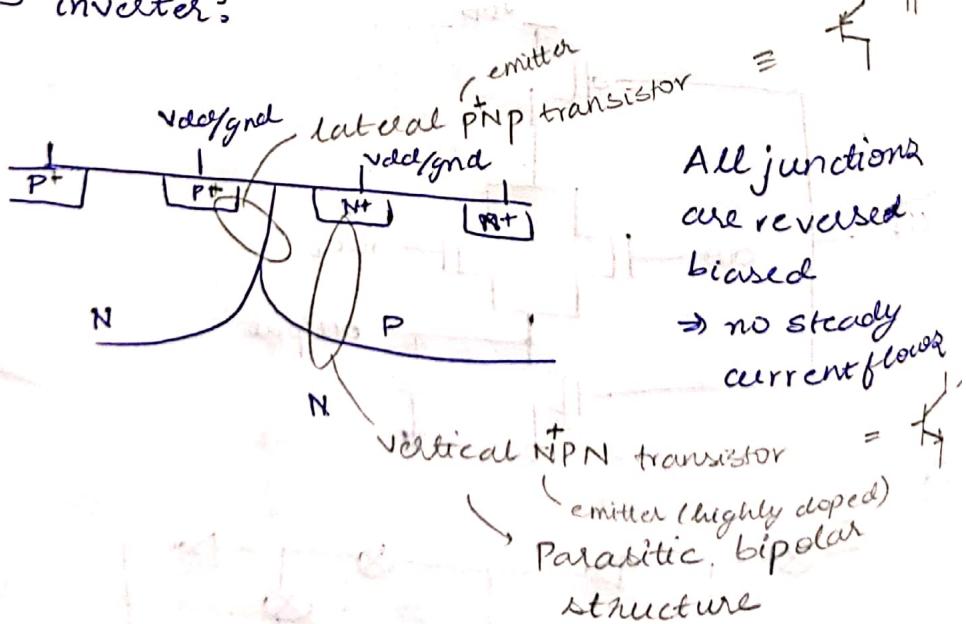
NOT1 & NOT4 to NOR gates.

→ NOT3 should become

→ If 1st one latched, the 2nd one should be in follow up mode

• Latch Up

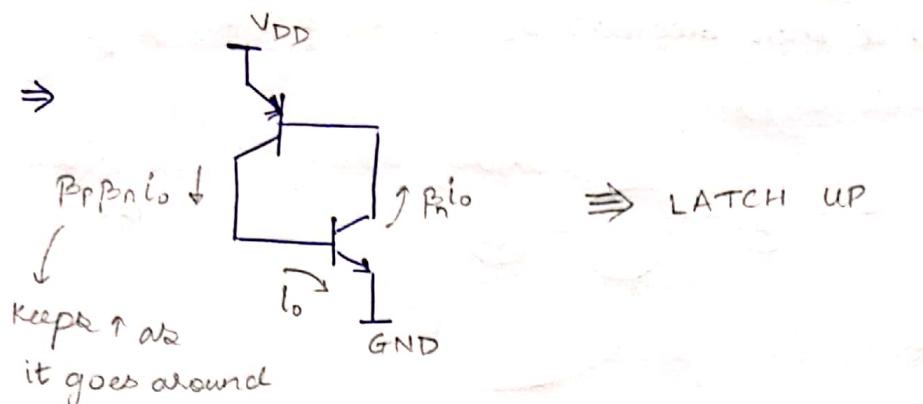
CMOS inverter:



- MOS regions are naturally reverse biased
- bipolar transistors need reverse bias isolation layer surrounding it

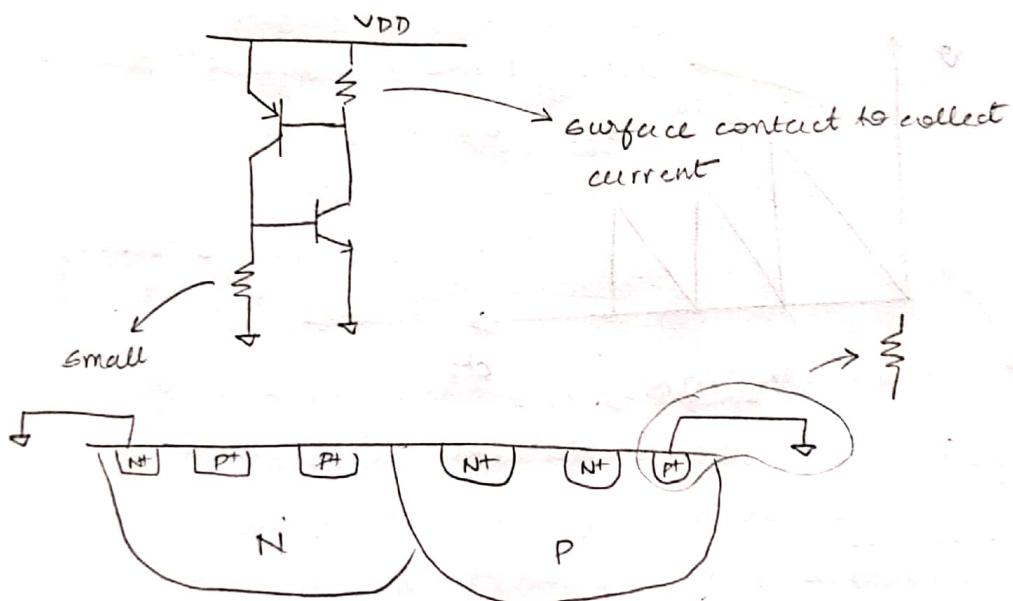
→ Collector of T_1 is the base of T_2

Collector of T_2 is the base of T_1



⇒ even a small current can magnify a lot
and melt the wires, heat up circuit

⇒ we provide an alternate path to the current



or make $\beta_{pPn} < 1$

⇒ make a bad bipolar transis.

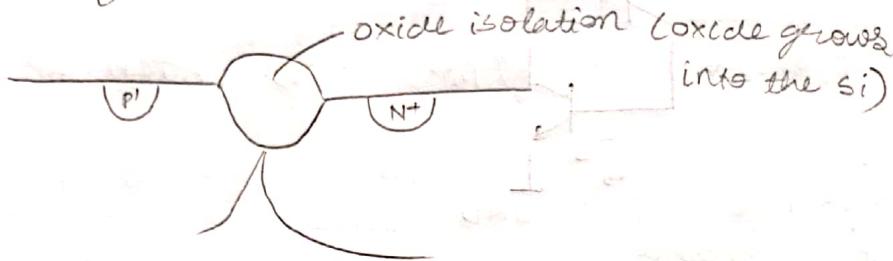
⇒ make base thicker

⇒ keep p^+ to n^+ as far away as possible

→ we usually have a graded doping so that e- reach collector as fast as possible

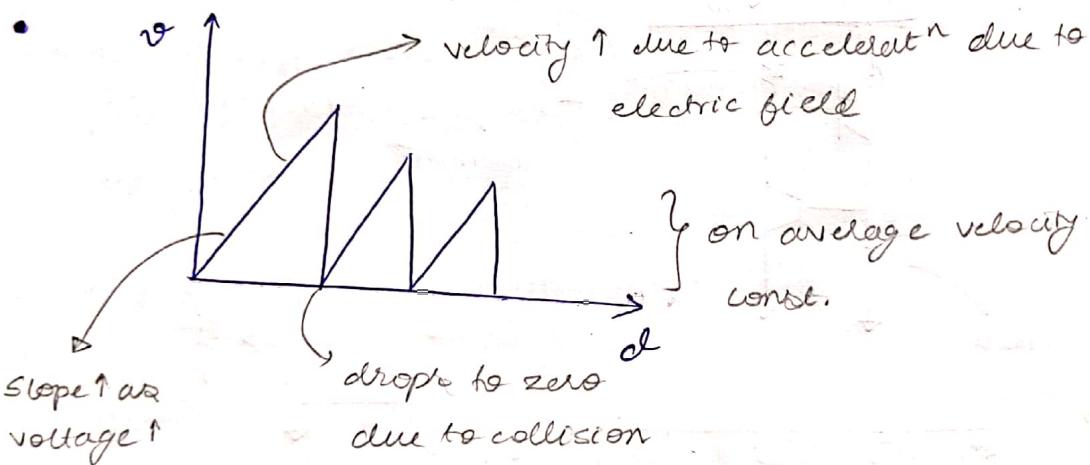
surface ————— gradient (high to low doping)

- so we make a retrograde implantation
- ⇒ doping concentration increases with depth and then decreases (can't have the doping increasing)



Latch up necessitates a min^m distance

b/w P+ & N+

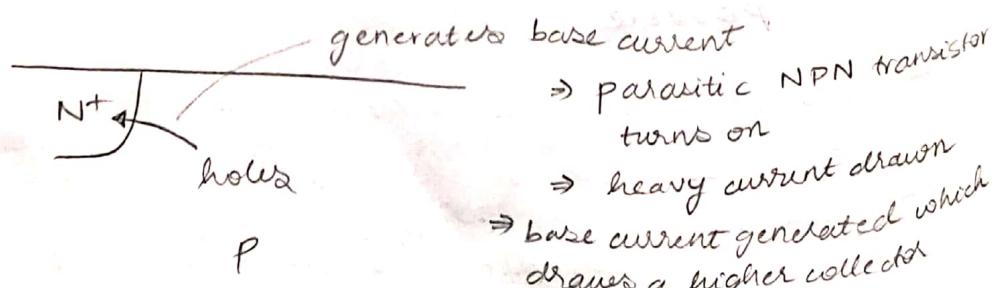


⇒ within the same distance we reach a higher velocity
⇒ more K.E.

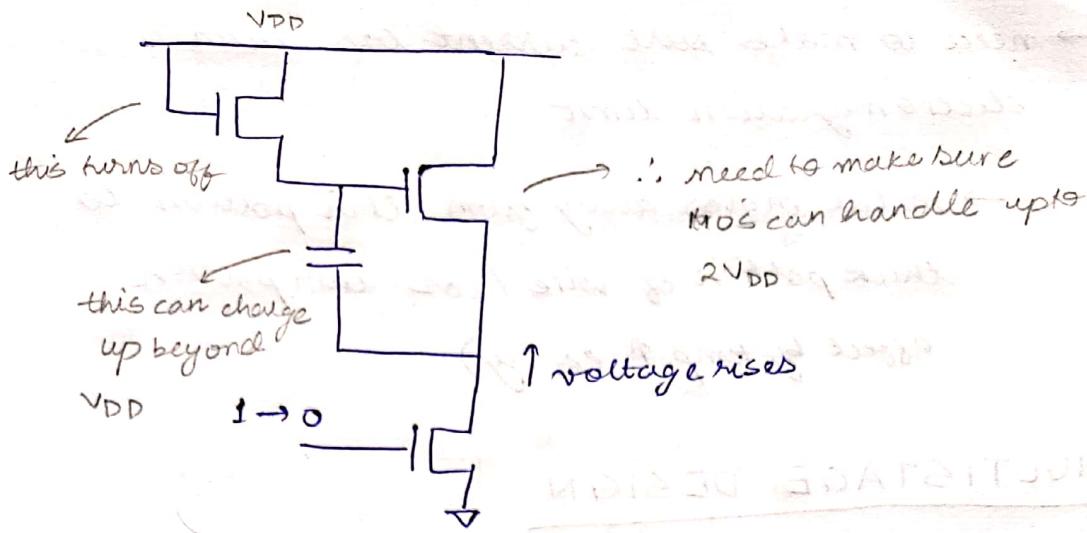
⇒ we can knock out an e⁻ from atom (ionization w/o doping);
Generation of e⁻ hole pair

⇒ new e⁻ does the same thing

⇒ avalanche process

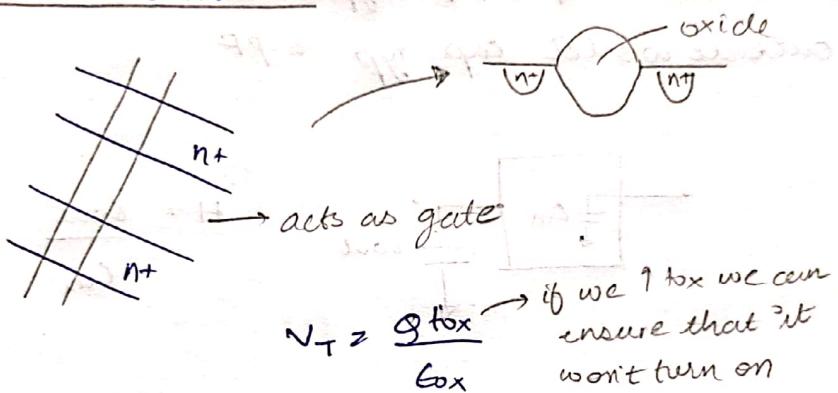


⇒ can't apply very high voltage



27/08

1) Field Turn On



2) Punch through

If we reduce channel length, the source comes close to field of drain.

→ drain field will inject e⁻ to source and it would turn on; can't control

3) Parasitic bipolar

A) latch up

B) drain (avalanche) breakdown

- Electromigration : movement of atoms due to collision from e⁻

(atoms keep moving about mean position due to thermal energy. If high energy e⁻ collides with an atom that is very much away from mean position, it is knocked out)

- need to make sure current less than electromigration limit
- metal moves away from thin portion to thick portion of wire (coz thin portion affect by temp ↑ easily)

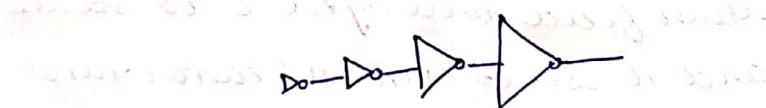
MULTISTAGE DESIGN

In silicon chip cap. typ. = f_F
outside world cap. typ. = P_F

$$\frac{1}{2} C_{in} \rightarrow H = \frac{C_{out}}{C_{in}}$$

$$\frac{K\tau}{C} = \text{const.}$$

we make the smallest inverter which meet the specification for our library.



Tapered Inverter

Need to scale the inverter such that it is able to run the bigger inverter

- also need to decide how many to put

$\tau \rightarrow$ time taken by minⁿ sized inverter (MSI) to drive another MSI

Now, of scaling of i^{th} inverter = s_i

$$\Rightarrow s_i \rightarrow s_{i+1}$$

(scaling of next stage)

$$\Rightarrow \gamma_i = \gamma \frac{s_{i+1}}{s_i}$$

$$\Rightarrow \text{total delay} = \gamma \sum_{i=1}^n \frac{s_{i+1}}{s_i} = D$$

s_{N+1} = load expressed as multiple of

(MSI expression)

$$\frac{\partial D}{\partial s_i} = 0$$

$$\Rightarrow \frac{\partial}{\partial s_i} \left[\frac{s_i}{s_{i-1}} + \frac{s_{i+1}}{s_i} \right] = 0$$

$$\frac{1}{s_{i-1}} - \frac{s_{i+1}}{s_i^2} = 0$$

$$s_i = \sqrt{s_{i+1}s_{i-1}}$$

$$\text{or } \frac{s_i}{s_{i-1}} = \frac{s_{i+1}}{s_i} = g = \text{"Scale Up Ratio"}$$

↳ const. scaling ratio for all inverters

Now, $s^n = H$ (accumulating inverters multiply their scaling)

$$\Rightarrow C' s^n = C_{\text{load}}$$

$$n \log g = \log H$$

$$n = \frac{\ln H}{\ln g}$$

Again, $D = n \tau$

$$D = \tau \ln H \frac{f}{ens}$$

$$\frac{\partial D}{\partial f} = \tau \ln H \left[\frac{ens - f(\frac{1}{f})}{(ens)^2} \right] = 0$$

$$\Rightarrow \frac{1}{ens} = \frac{1}{(ens)^2}$$

$$\ln f = 1$$

$$f = e$$

(But actually $f \sim 3-4$)

(we have ignored the parasitic capacitance)

Thus, need to include:

i) parasitic delay

ii) other logic (other than inverter)

iii) Branching

Incorporation of these 3 things into the simplistic model is called

"logical effort"

29/08 → we only have the flexibility to change the geometry in order to minimize the delay

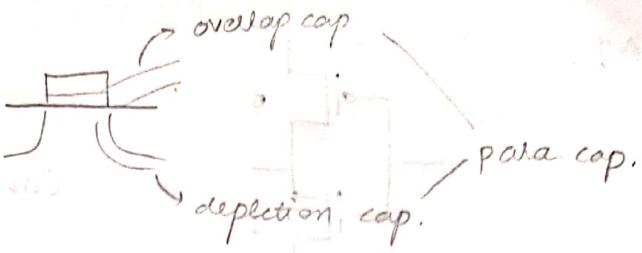
capacitance $\propto W$ ($L \rightarrow \text{const. at min^n value}$)
(even parasitic)

⇒ $W = \text{capacitance}$

$$\Rightarrow \frac{K\tau}{C} = \text{const.}$$

$$\Rightarrow \frac{WT}{C_L + \alpha W} = \text{const.}$$

para.
cap.



$$\Rightarrow \gamma \alpha \frac{C_L + \alpha W}{W}$$

$\gamma \alpha \frac{C_L}{W} + \alpha$

the minⁿ time taken to charge para cap is not zero (independent of width)

initial cap = $\frac{C_L}{C_{in}}$ (width)

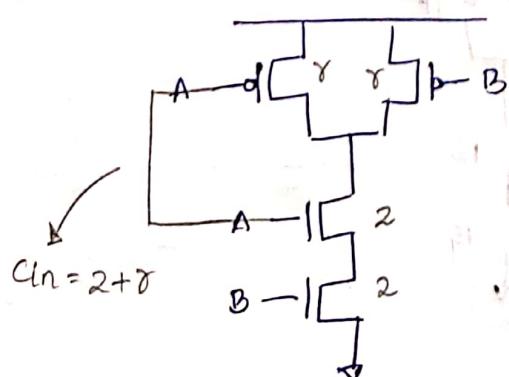
$$\Rightarrow d(\text{delay}) = f + p$$

(these quantities measured in terms of minⁿ size of minⁿ sized inv.)

→ C_{in} is a measure of driving capability
(to drive C_{out})

→ Any logic gate is basically an inverter which for the same current sees a different load

→ the relative size of pmos w.r.t. nmos in an inverter remains same for any scaling

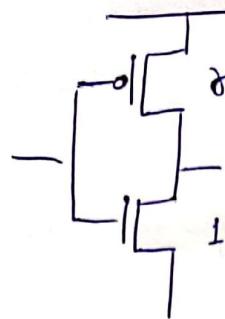


$$W_p = \gamma W_n$$

Drawing in terms of MSI taking a unit of 1

- width = width of n channel
- time = time taken by MSI to drive another MSI, not taking into account para. cap

MSI:



$$Cin = 1 + \delta$$

If we not compare out NAND on terms

If we want to make the NAND equivalent to MSI such that prev stage thinks the load is like an MSI

→ we scale it such that $\frac{2+\delta}{1+\delta}$

$$\Rightarrow \tau_{eff} = \frac{2+\delta}{1+\delta} \cdot \tau_{(NAND)}$$

scale geometry by $\frac{1+\delta}{2+\delta}$; ⇒ delay by $\frac{2+\delta}{1+\delta}$

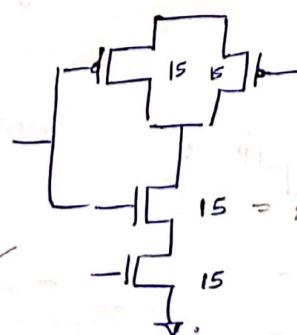
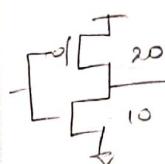
(these scaling factors depend on the construction of NAND rather than the geometry)

MSI scaled by 10

$$\Rightarrow Cin = (1+\delta)10$$

$$\text{if } \delta = 2$$

$$Cin = 30$$



This is like an inverter scaled by $\frac{3}{4} \times 10$

$$15 = 20 \left(\frac{3}{4}\right) = 2 \times \left(\frac{3}{4} \times 10\right)$$

Scaling of nmos in template NMOS

delay higher by a factor of $\frac{4}{3}$

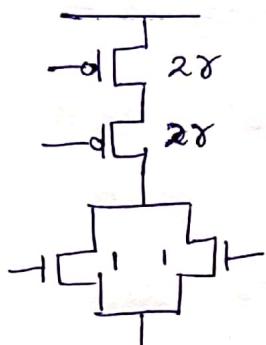
$$f = g \cdot h$$

$g \rightarrow$ correction factor (logical effort) (depends on type of gate (indep. of sizing))

$$h \rightarrow \frac{C_{load}}{C_{in}} = \frac{S_{in}}{S_i} \text{ (sizing dependant)}$$

$$\Rightarrow d = gh + P$$

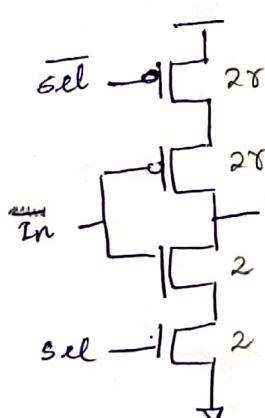
$$\text{eg: } g(n \text{ input NAND}) = \frac{n+\gamma}{1+\gamma}$$



$$g = \frac{2\gamma + 1}{\gamma + 1} \rightarrow \text{NOR is slower than NAND}$$

$$g(n \text{ input NOR}) = \frac{2n\gamma + 1}{\gamma + 1}$$

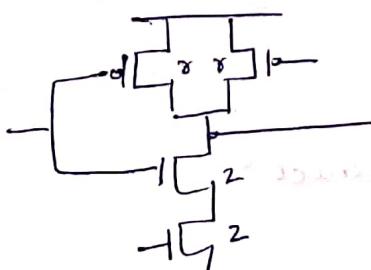
eg: MUX



$$g = \frac{2\gamma + 2}{\gamma + 1} = 2$$

• Delay of parasitic capacitance

→ only consider the gates connected to C_p

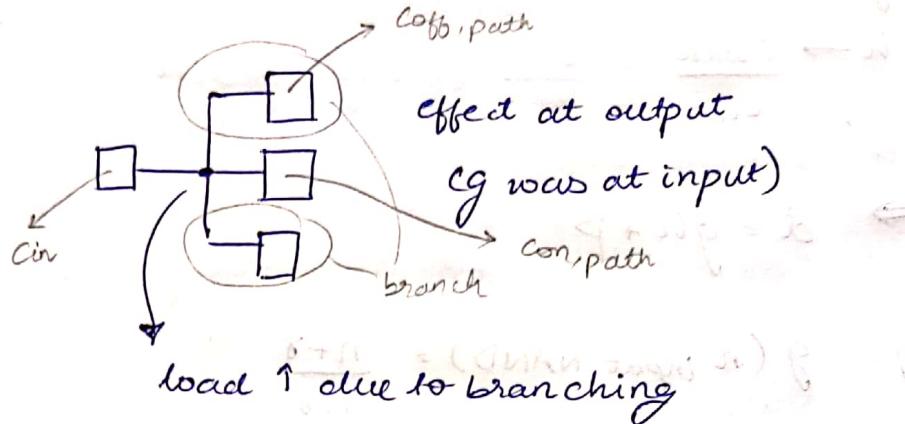


$$\frac{2+2\gamma}{1+\gamma} = 2$$

$$\Rightarrow P_{NAND} = 2P_{inv}$$

03/09

- we want a lower output hence larger delay



$b = \text{branching co-efficient}$

$$= \frac{\text{con. path} + \text{soft path}}{\text{con. path}}$$

we pretend as if branch not connected

if no branching then

$$\frac{\text{con. path}}{\text{Cin}} = \text{delay}$$

Now $\frac{\text{con. path}}{\text{Cin}} \times \frac{\text{Total}}{\text{con. path}}$

$\underbrace{\quad}_{h}$ $\underbrace{\quad}_{\text{con. path}}$

loading higher by this amount $= b$

→ when branching occurs, $b > 1$

when no branching, $\text{soft path} = 0$
 $\Rightarrow b = 1$

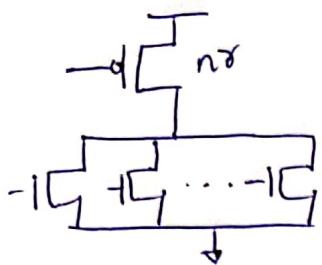
→ $b = \text{depends on fan out}$

$g = \text{depends on gate constructn}$

$h = \text{depends on sizing}$

$P = \text{const.}$

- g for inverter = 1
- $P_{inv} = (0.75 - 3)$ for inverter



$$P_{NOR} = \frac{n\tau + n}{\tau + 1} = n \frac{(\tau + 1)}{\tau + 1} = n P_{inv}$$

⇒ for any logic, parasitic delay is n times the inverter parasitic delay.

- $G = \prod g_i$

- $B = \prod b_i$

- $D = \sum d_i \rightarrow$ path delay (want to minimize)

$$D = \sum g_i b_i h_i + \underbrace{\sum p_i}_{\text{minimum delay}}$$

$$D = \sum g_i b_i \frac{c_{i+1}}{c_i} + \sum p_i$$

$$\frac{\partial D}{\partial c_i} = g_{i-1} b_{i-1} \cdot \frac{1}{c_{i+1}} + g_i b_i \frac{(-1) c_{i+1}}{c_i^2} = 0$$

$$g_{i-1} b_{i-1} h_{i-1} = \underbrace{g_i b_i h_i}_{f_i} = \hat{f}$$

h_i = electrical effort (size dependent)

f_i = stage effort

- all f_i 's should be equal

- product of all stages = $\hat{f}^N = \underbrace{GBH}_{\text{known}}$

⇒ $\underbrace{g_i b_i h_i}_{\text{known}} \rightarrow \text{known}$
 \rightarrow can calculate starting from stage 1