Welcome to

EE669: VLSI Technology

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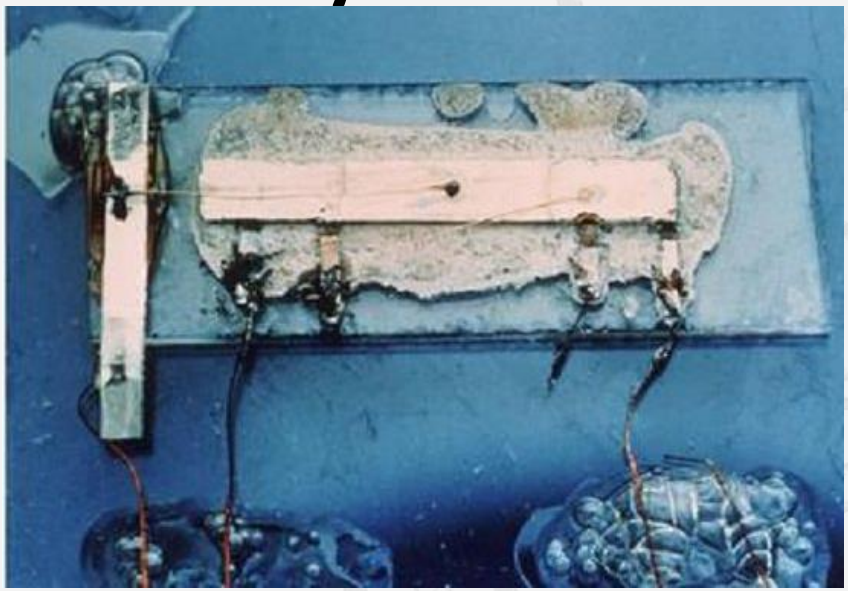
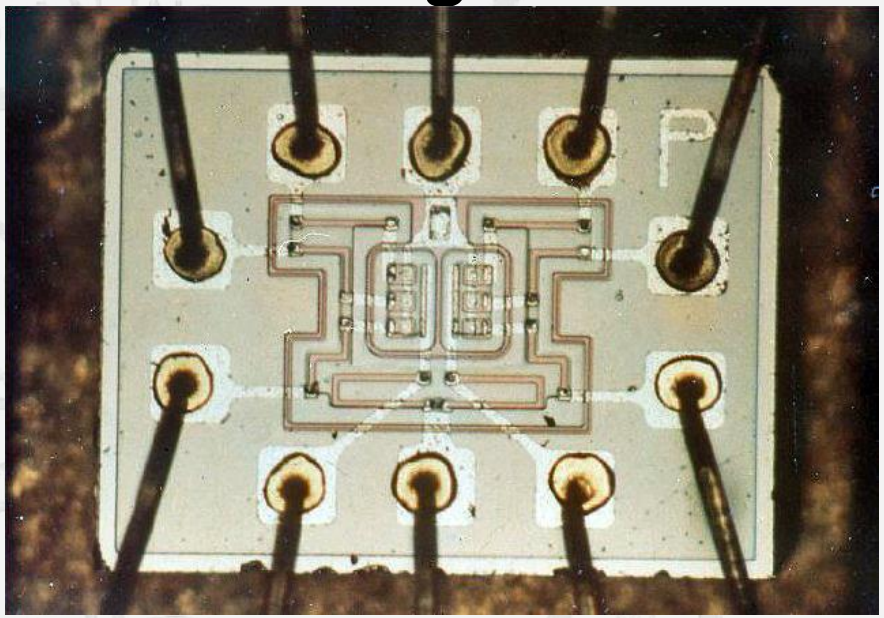
Office hour: Friday 10:00 – 11.00 AM, EE Annex, Room: 104

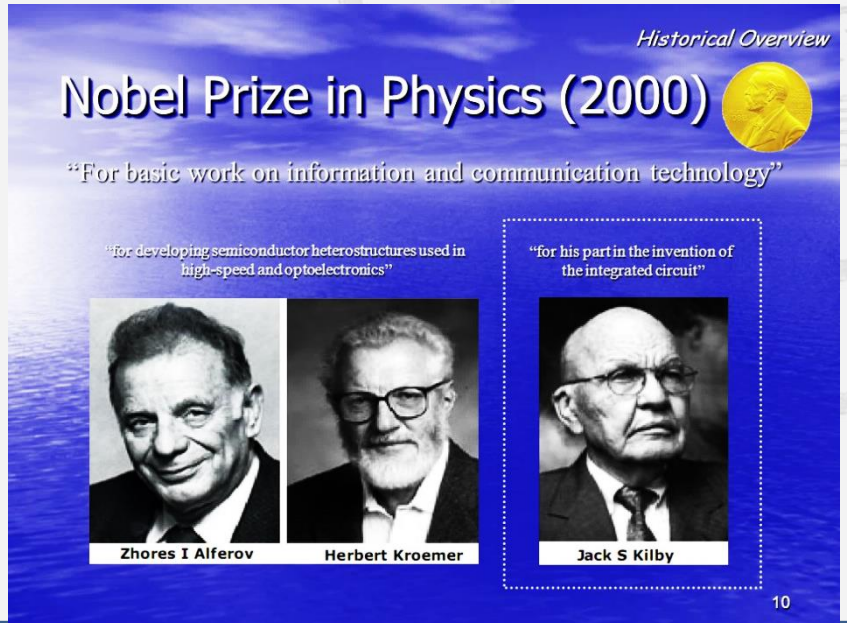
When and where did it start

Bardeen_Shockley_Brattain_1948 @ Bell Lab

Jack Kilby and the World's First Integrated Circuit







Logical NOR IC from the computer that controlled the Apollo spacecraft

Moore's Law and Technology Node?????

- *The number of transistors in an integrated circuit doubles about every 18 months*

- **What is the meaning of a technology node for the semiconductor manufacturing process ???**

- **"Node"** defined as average **half-pitch** (i.e., half the distance between **identical features**) of a **memory cell** at specific technology level.

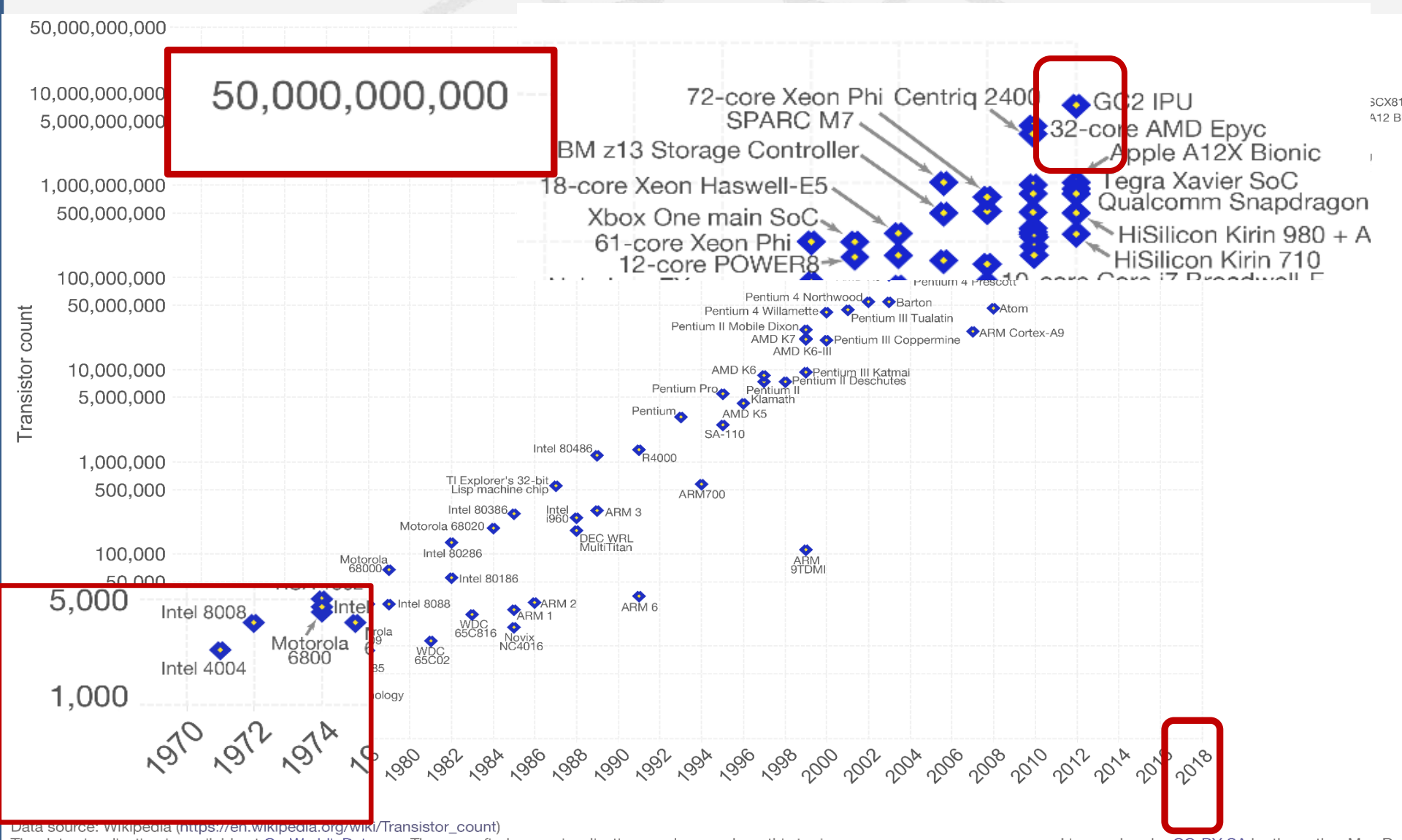
But this definition of technology node is NOT valid any more!!!!

Standard Node Value by Node

Company	16nm/14nm	10nm	7nm	5nm
Global Foundries	16.6nm	NA	8.2nm	NA
Intel	**13.4nm**	**9.5nm**	**6.7nm**	NA
Samsung	16.6nm	12.0nm	8.4nm	NA
TSMC	18.3nm	11.3nm	8.2nm	5.4nm

- ***This table is based on data available from GF/Intel/Samsung and TSMC***

Moore's Law and Scaling



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Technology Road Map: Who controls?

The International Technology Roadmap for Semiconductors

IEEE
ncing Technology
for Humanity

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

INTERNATIONAL
ROADMAP
FOR
DEVICES AND SYSTEMS™

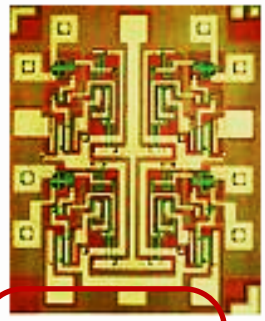
2018 EDITION

EXECUTIVE SUMMARY

THE IRDS™ IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

Intel's Path to 10nm: 2010 to 2019

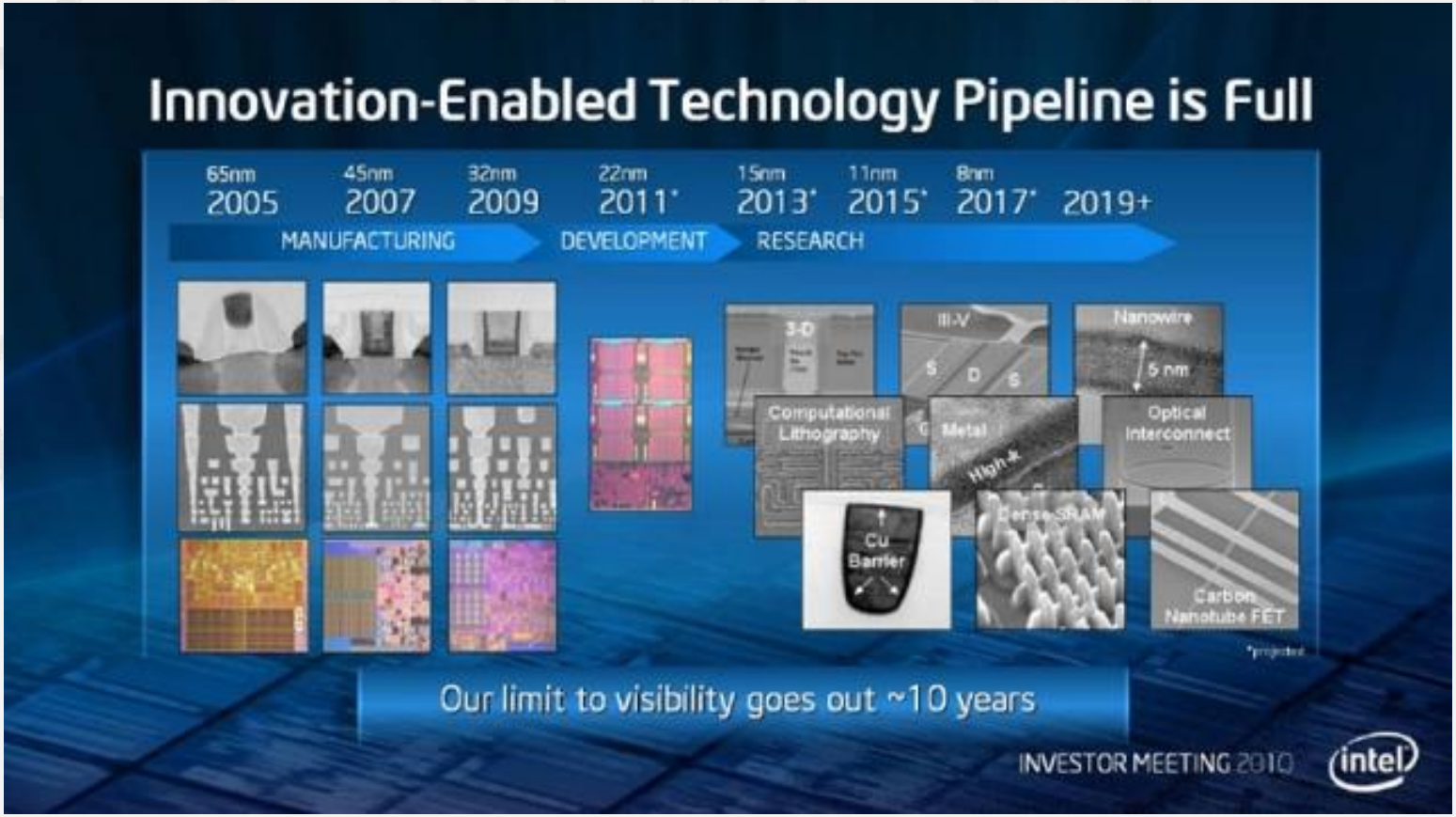
Semiconductor manufacturing processes



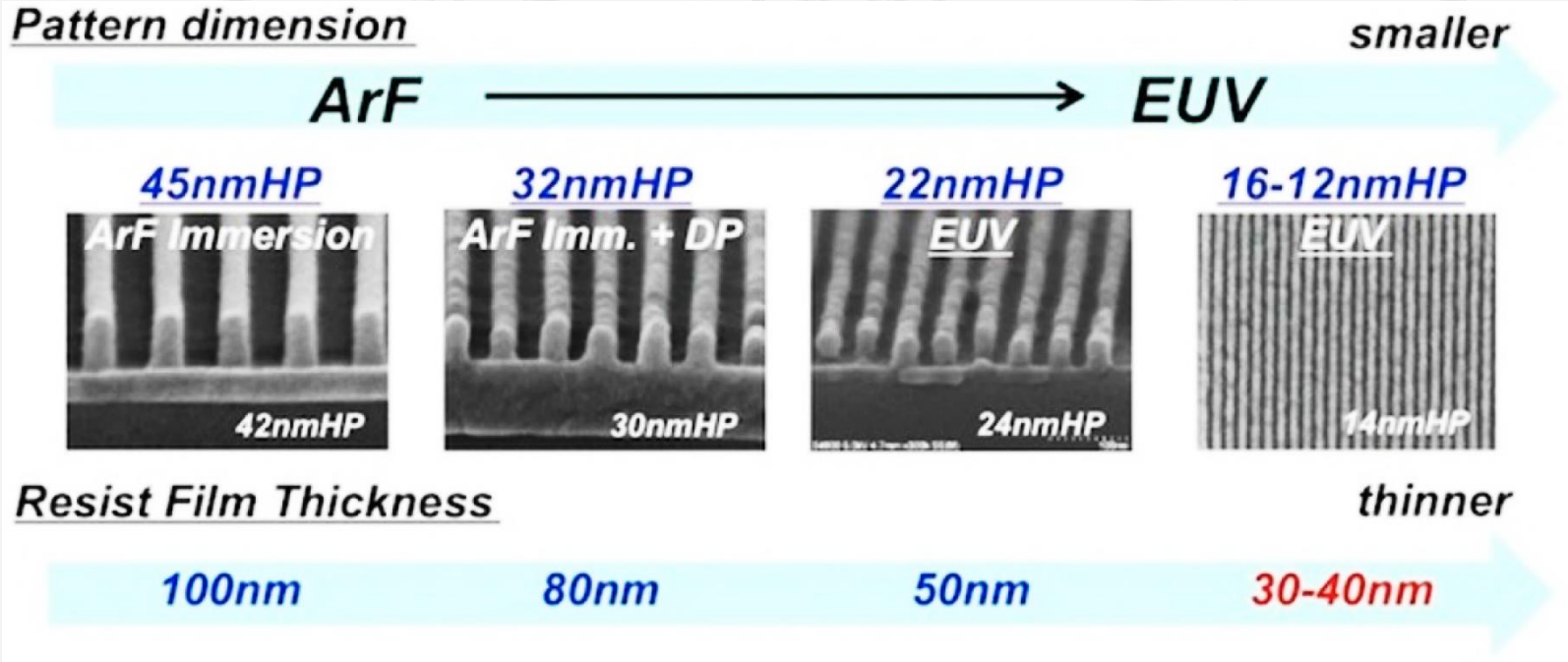
10 µm – 1971
6 µm – 1974
3 µm – 1977
1.5 µm – 1981
1 µm – 1984
800 nm – 1987
600 nm – 1990
350 nm – 1994
250 nm – 1996
180 nm – 1999
130 nm – 2001
90 nm – 2003
65 nm – 2005
45 nm – 2007
32 nm – 2009
22 nm – 2012
14 nm – 2014
10 nm – 2016
7 nm – 2018
5 nm – 2019
3 nm – ~2021

Intel Process Technology And Packaging Plans: 10nm in June, 7nm in 2021

David Schor Foundries, Interconnects, Packaging, Process Technologies May 11, 2019
Tagged 10nm, 3D packaging, 7nm, EMIB, HPC, Lakefield



Evolution of the lithography technique where the pattern becomes denser the (HP)



Process steps:

- Fin patterning vs. planar active region patterning
- Oxide filling, planarization, and recessing
- Doping to form well isolation
- Gate oxide growth, and dummy gate deposition, planarization and patterning
- Doping to form S/D extentions
- Spacer deposition and patterning
- Epitaxy forming S/D regions (embedded SiGe and raised Si)
- ILD0& CMP
- Dummy gate removal
- Replacement of high-k & metal gate stack
- Self-aligned contact formation
- Back end of line

Radamson, H.H.; Zhang, Y.B.; He, X.B.; Cui, H.S.; Li, J.J.; Xiang, J.J.; Liu, J.B.; Gu, S.H.; Wang, G.L. The Challenges of Advanced CMOS Process from 2D to 3D. Appl. Sci. **2017**, 7, 1047

Market Share

RESEARCHANDMARKETS
THE WORLD'S LARGEST MARKET RESEARCH STORE

Global $5+ Billion Silicon Germanium Materials & Devices Market 2017-2018 & 2021

Email | Print Friendly | Share

April 27, 2018 04:06 ET | **Source:** Research and Markets

Dublin, April 27, 2018 (GLOBE NEWSWIRE) -- The "Global Silicon Germanium Materials & Devices Market: Focus on Material Type (Source, Substrate & Epitaxial Wafer), Device Type (Wireless, Radio, FOT) & End-User (Telecommunication, Consumer Electronics, Automotive) - Analysis & Forecast 2017-2021 " report has been added to **ResearchAndMarkets.com's** offering.

Compound Semiconductor Market

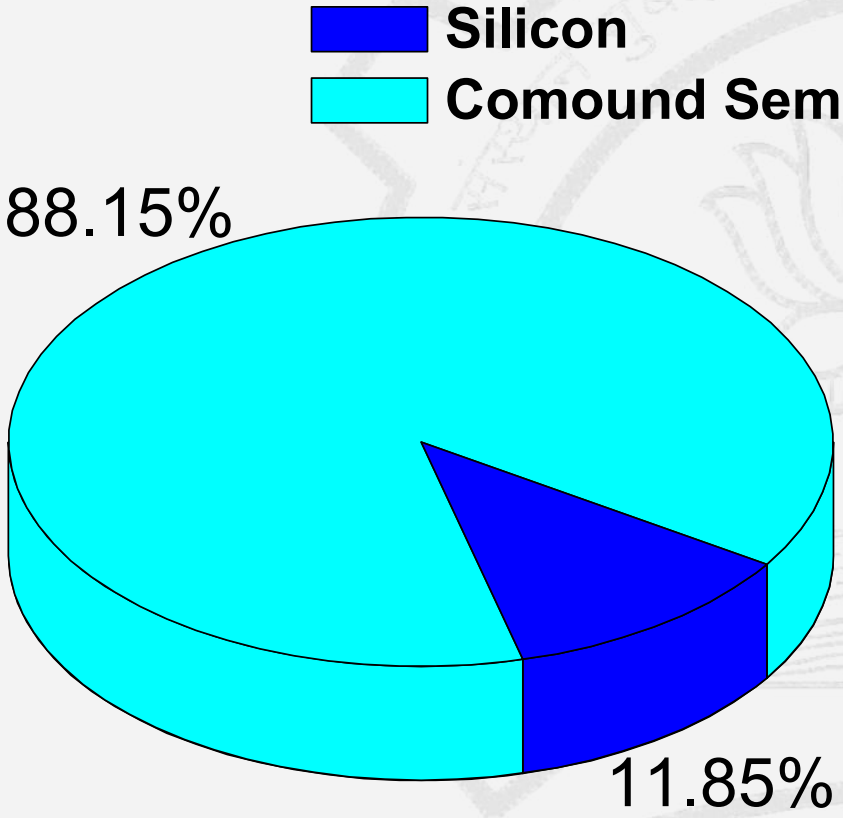
HOME › PRESS RELEASES › **Compound Semiconductor Market worth $53.0 billion by 2024**

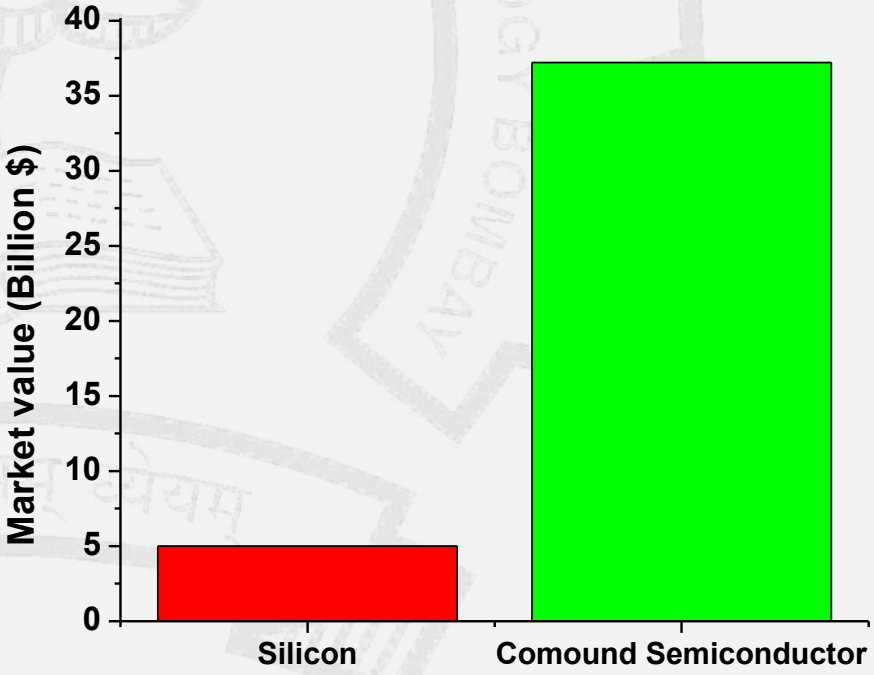
Compound Semiconductor Market worth $53.0 billion by 2024

VIEW FULL TABLE OF CONTENTS | METHODOLOGY | DOWNLOAD PDF

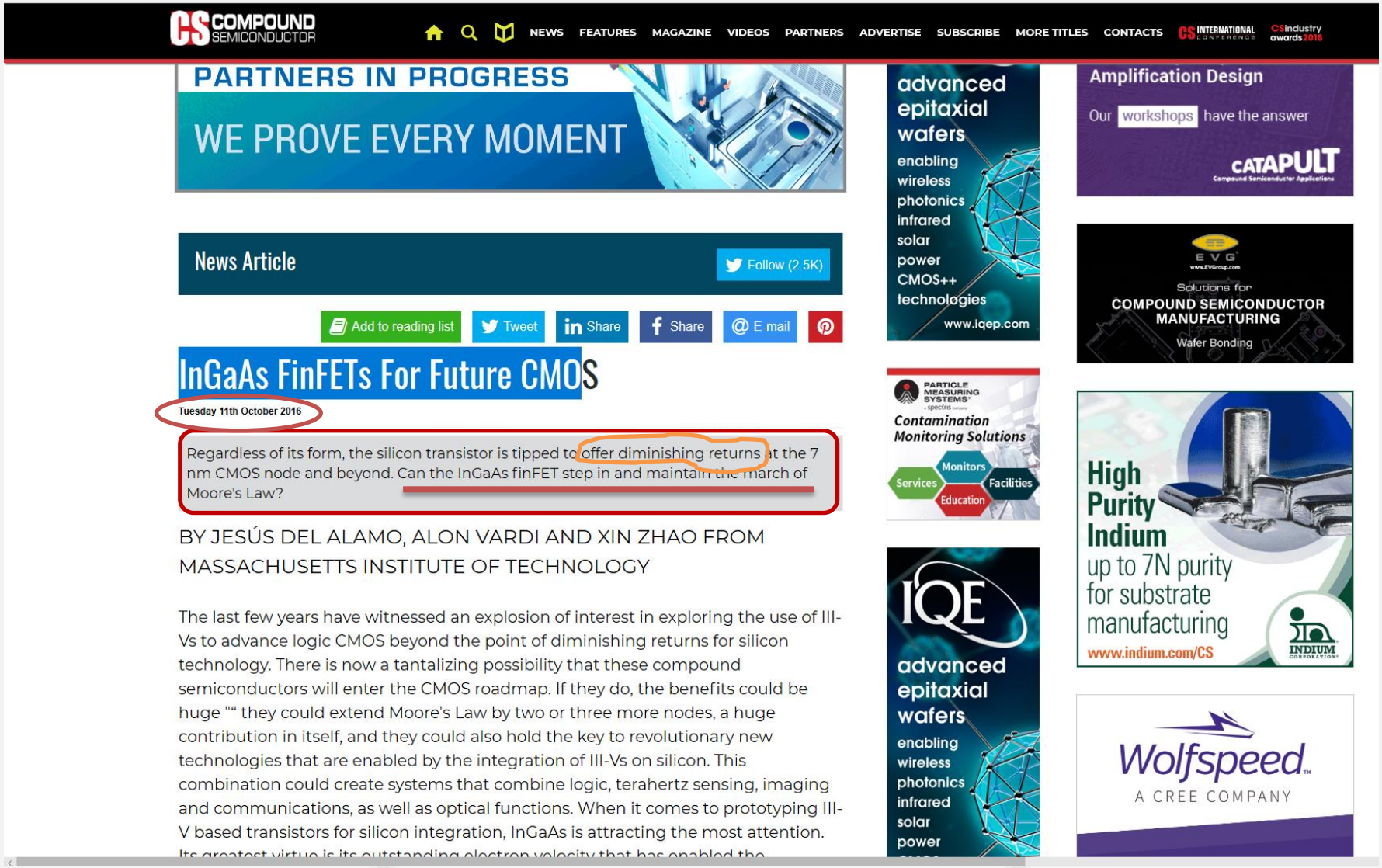
According to the new research report "**Compound Semiconductor Market by Type (GaN, GaAs, InP, SiGe, SiC, GaP), Product (LED, RF, Optoelectronics, Power Electronics), Application (Telecommunications, General Lighting, Military & Defense, Datacom, Automotive), Geography - Global Forecast to 2024**", The compound semiconductor market is expected to grow from USD 37.2 billion in 2019 to USD 53.0 billion by 2024, at a compound annual growth rate (CAGR) of 7.3%. Increasing adoption of compound semiconductors, including GaN, GaAs, and InP, is expected to drive the growth of the compound semiconductor market during the forecast period.

Market share: Si and Compound Semiconductor Technology

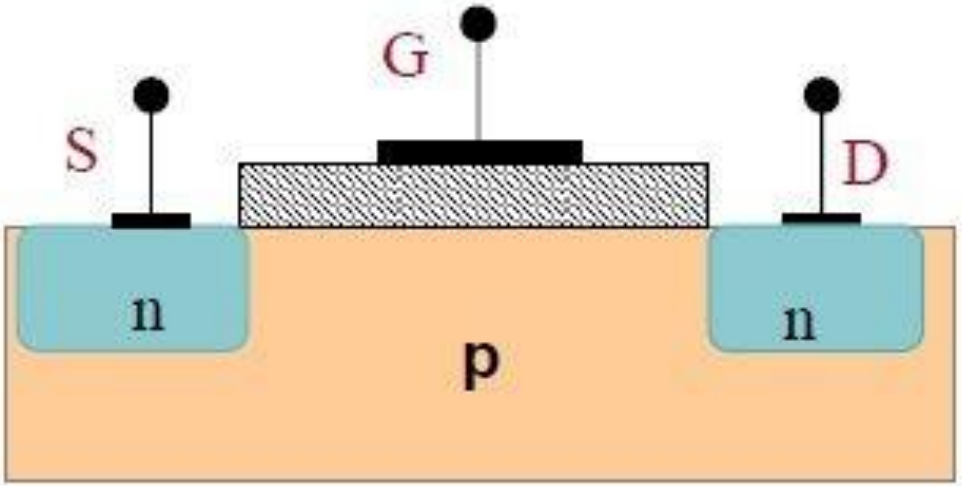




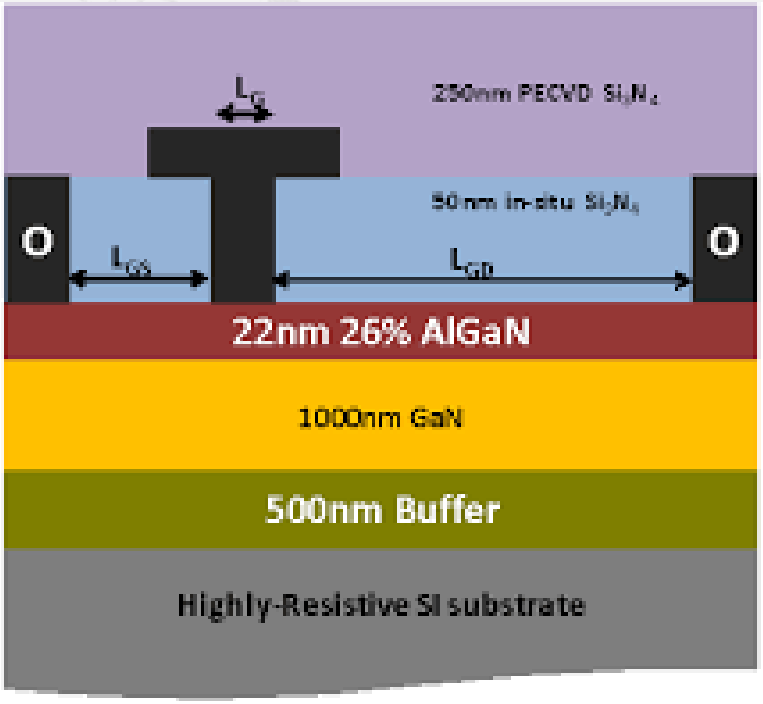
VLSI: What is it today?



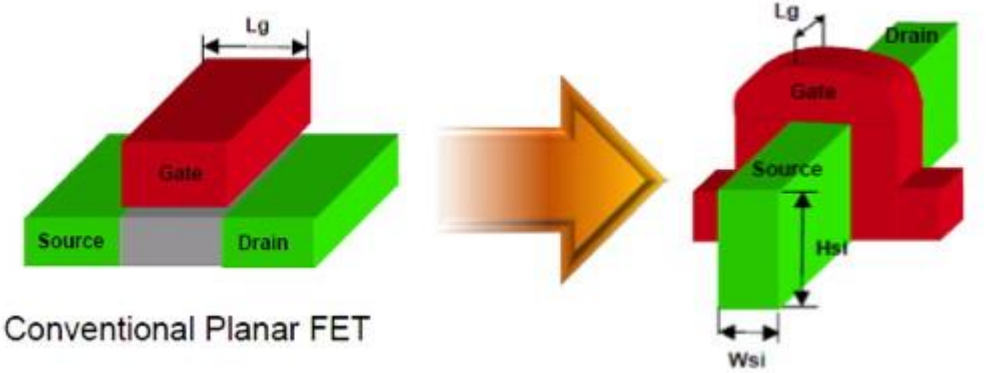
Example of Si and Compound semiconductor Devices



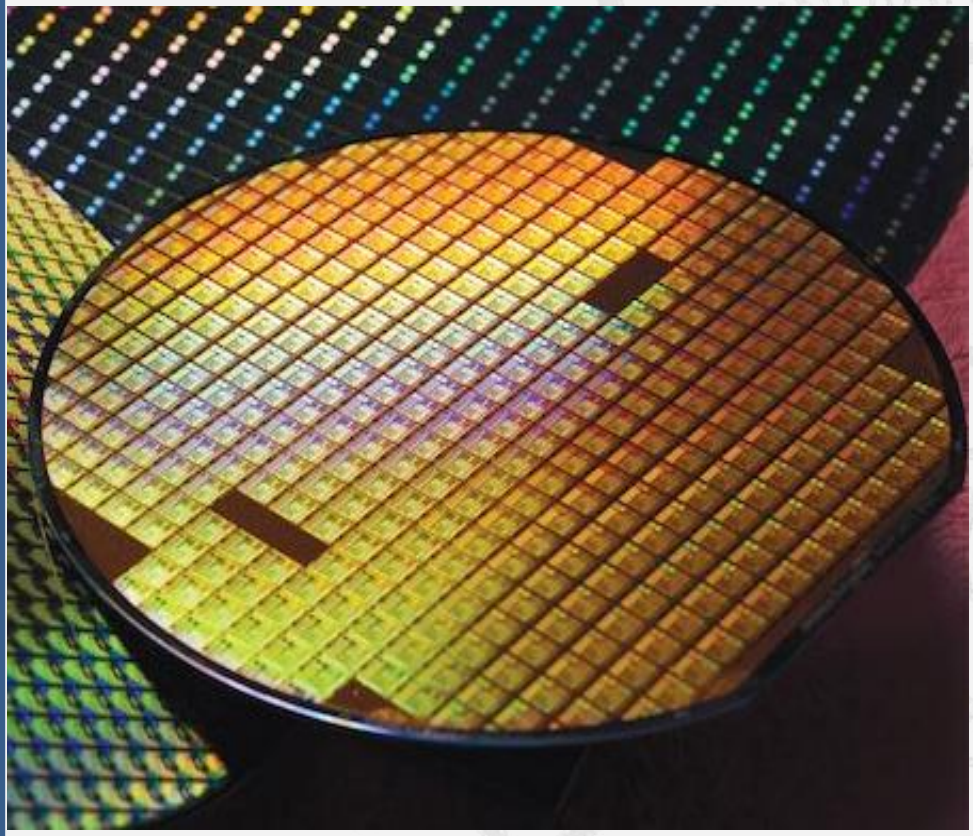
MOSFET Structure



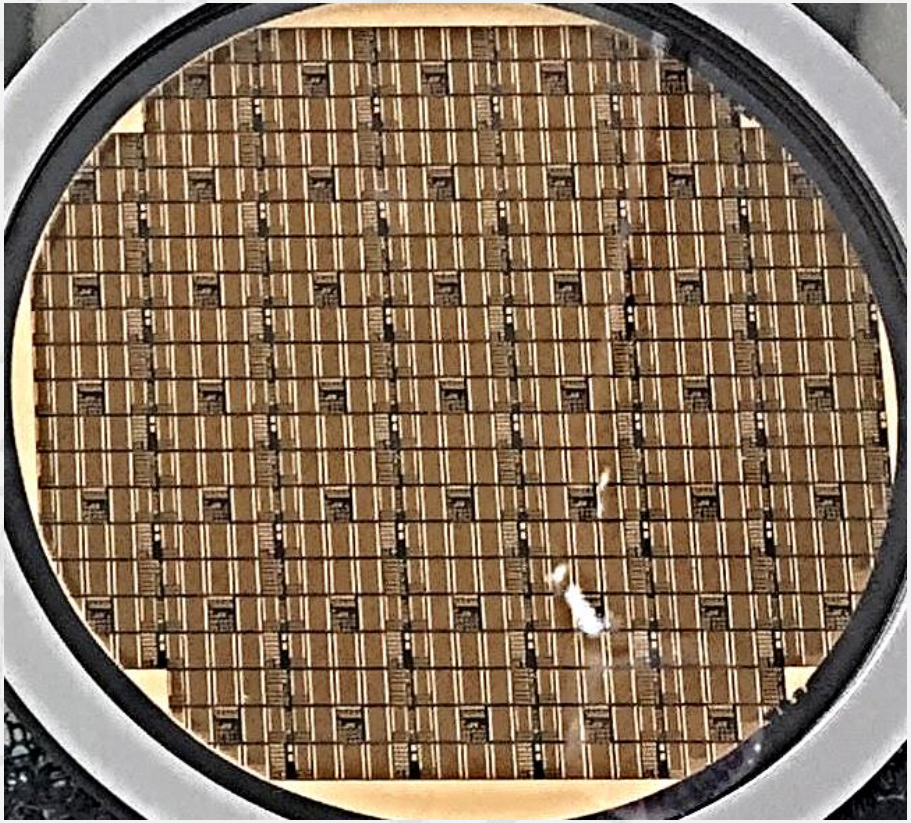
1: Schematic structure of the AlGaN/GaN epilaye



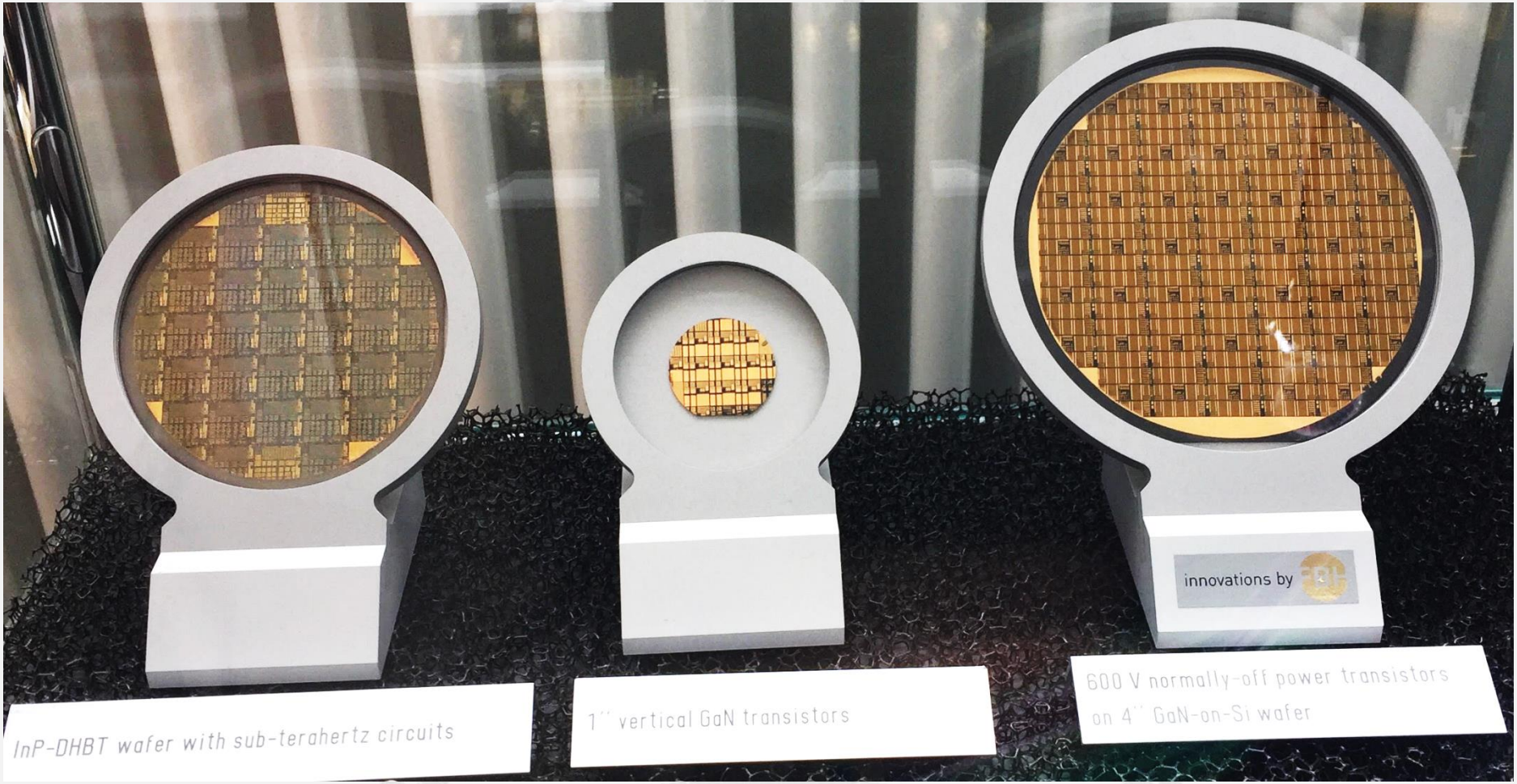
Si vs. Compound Semiconductor Devices



TSMC 7nm node Chip on 12” Si



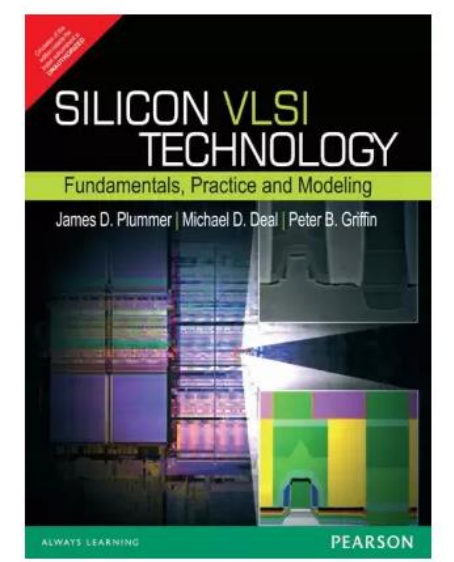
600V Normally OFF GaN power transistor on 4” Si wafer

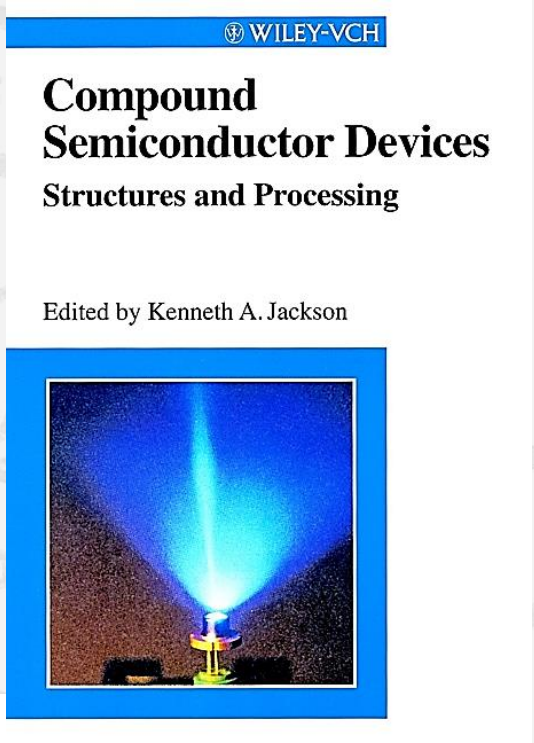

InP-DHBT wafer with sub-terahertz circuits
1'' vertical GaN transistors
innovations by
600 V normally-off power transistors
on 4'' GaN-on-Si wafer

Course content: Official description

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques. Impurity incorporation: Solid State diffusion modeling and technology, Ion Implantation modeling, technology and damage annealing, characterization of Impurity profiles. Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI, Characterization of oxide films, High k and low k dielectrics for ULSI. Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation. Chemical Vapor Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films, Epitaxial growth of silicon, modelling and technology. Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects, Multi-level metallization schemes. Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques, RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits, Advanced MOS technologies.

References





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Gallium Nitride Electronics

Authors: **Quay**, Rüdiger

Important: Grading

- Midsem: 35%
- Endsem: 40%
- Quizzes:15% (Best 6 out of 8)
- Assignments: 5%
- Attendance: 5%

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See you tomorrow