EE618(Zele)
CMOS Analog IC Design

Supporting Document for Course Project - I.

Note:
1)Use SCL 180nm Design Kit, with VDD = 1.8V.
2)Use λ_n, λ_p, μ_n, μ_p values provided in class.
3)For resistors use "rphpoly2t" from the SCL library.
4)For MIM capacitors use "cmim_sq" from the SCL library.
5)Use a single ideal current source to bias the OTA.

Note: Testbenches and other supporting documents (along with a report template) will be provided to students on moodle. A symbol needs to be created out of the design with the following pins : IN_P, IN_N, VDD, VSS, IBIAS, and VOUT. The individual testbenches for characterization will be provided under the library "OTA_CHARACTERIZATION" on moodle. The IBIAS value is 10μA and this current source will be provided in the testbench. The OTA IBIAS pin must take this current of 10μA and generate all necessary current/voltage internally. The design symbol needs to be placed on each of the test case to perform the characterization.

Details on the Simulations to be performed:

- **OPERATING POINT:** Perform the dc operating point analysis with the OTA in unity gain feedback mode. Clearly annotate and report the dc operating point voltages at every node on the schematic.
- **STB ANALYSIS:** Run the "stb" analysis and report the DC gain, unity gain frequency and the phase margin. Also show the magnitude and phase plot.
- **SLEW RATE:** With the OTA in unity gain feedback mode, apply a positive step from 0 to 1.8V with a rise time of 100ps. Measure the slew rate and clearly show the output plot in the slewing region with cursors.

- **SETTLING TIME:** With the OTA in unity gain feedback mode, apply the same step input as above. Measure and report the settling time, t_s for 1% accuracy.
- **SYSTEMATIC OFFSET:** With the OTA in unity gain feedback mode, measure and report the systematic offset value using dc analysis. Clearly show the output node voltage on the schematic.
- **NOISE:** Show the input referred noise PSD from 1Hz to 1GHz band. Clearly show the RMS thermal noise voltage in the plot (with cursor). Report the integrated noise voltage over the unity gain bandwidth.
- **CMRR:** Plot the open loop CM gain of the OTA with clear labels. Report the CMRR of the OTA.
- **PSRR:** Perform the PSRR simulation by adding a small signal component only on the voltage supply of the OTA. Plot and report the PSRR value with clear labels (Open loop).
- **INPUT COMMON MODE RANGE:** Sweep the input common mode voltage in the unity gain configuration and report the maximum Input common mode range of the OTA.
- **CLOSED LOOP GAIN:** With the OTA in unity gain feedback mode, perform ac analysis and report the DC gain and the -3dB frequency.
- **CLOSED LOOP TRANSIENT ANALYSIS:** With the OTA in unity gain feedback mode, apply a sinusoidal signal of 10KHz frequency for maximum signal swing at the output without distortion.
- **POWER CONSUMPTION:** Report the total current and power consumption of the OTA.
