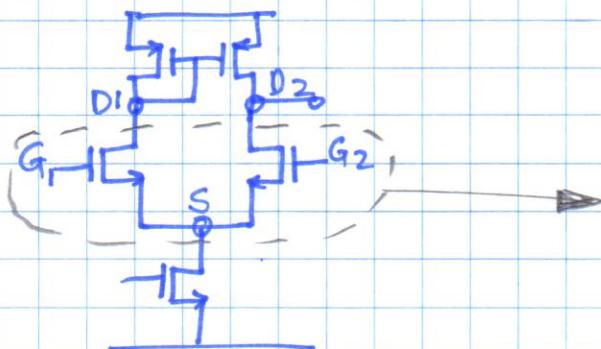
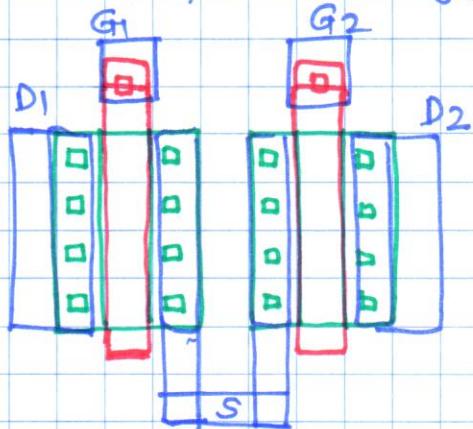


12 OCT 2019

ANALOG LAYOUT TECHNIQUESSchematic designLayout design

In schematic design, only internal device parasitics are modeled for purpose of simulation.

layout → Placement of all mask layers to create devices & interconnect. — New parasitics R, LC are added. When layout is created. — can degrade performance of your circuit.

Circuit Design Engineer → EE background

Layout Design Engineer → Artists., good Engineering drawing skills
3.D visualization

Overall responsibility → you. as design engineer

Layout Design

DRC Design Rule Checks

— Guarantee functional transistor & interconnects.
in presence of process variations.

* Min Width.

* Min. Enclosure

* Min Spacing

* Min Extension.

Caliber tools

LVS

Layout vs. Schematic Check.

→ Layout → Netlist
Schematic → Netlist \rightarrow identical check.
Device Sizes same.

ERC

Electrical Rule Check.

→ Electrical Connection of all wells, substrate
→ Devices connected to proper supply voltages
IV device \rightarrow IV supply.

Extraction

PEX, RCX.

parasitic

→ R - only Resistance extracted - IR drop.
→ C \rightarrow only p. Cap. extracted (to gnd)
→ CC \rightarrow coupled cap. extracted (to adjacent lines)
→ R+CC \rightarrow Final verdict for simulations

→ L extraction \rightarrow painful with std. tools

\rightarrow EMX used to model par. inductance

2-d Simulator — Ind. Standard.

Crosssection of CMOS Technology.

Reference: Chapter 18 - Razavi CMOS Proc. Tech.
 → Review -

Slides discussed in class -

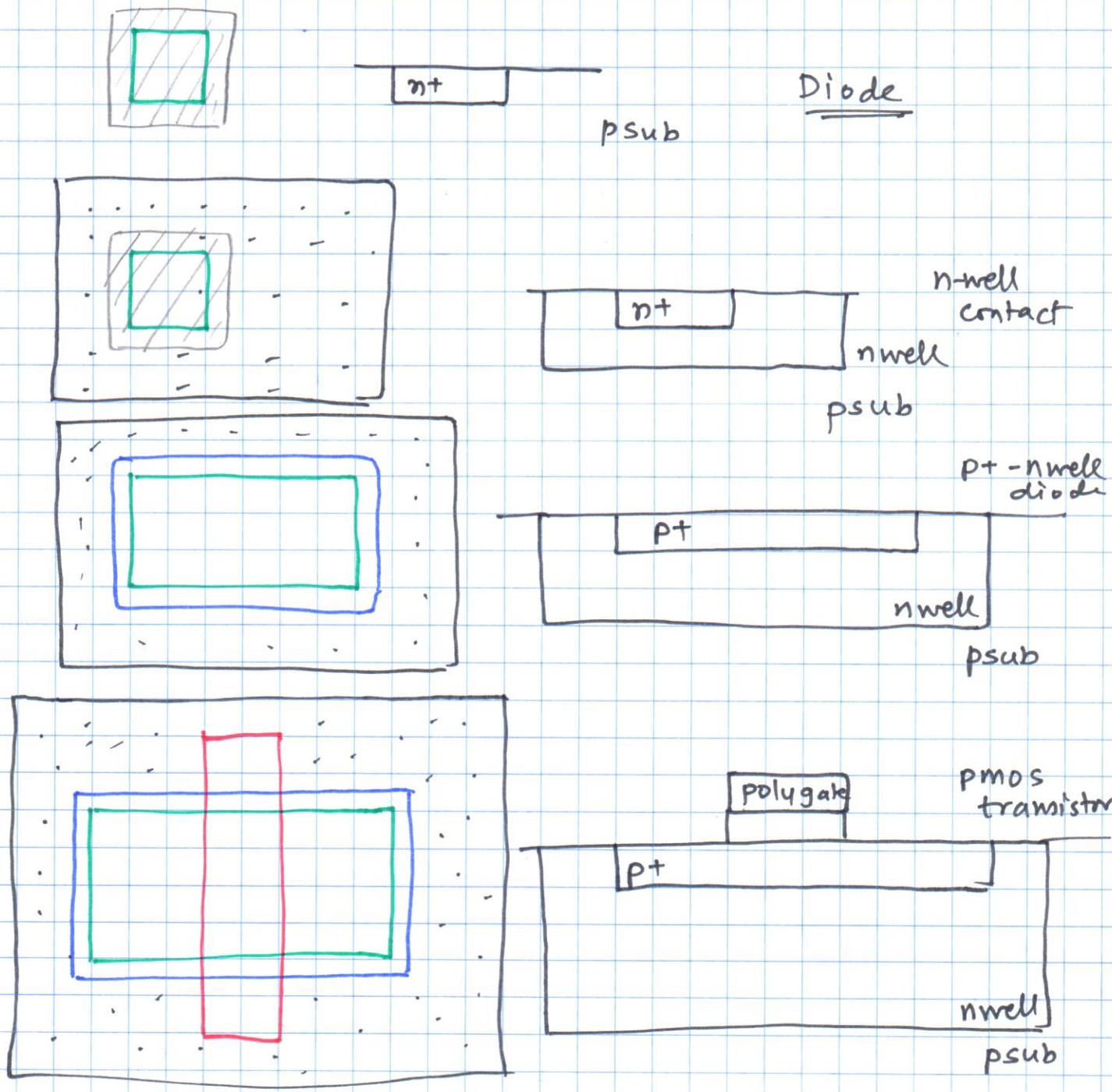
■ N well.

□ Poly

□ Diffusion

□ N type

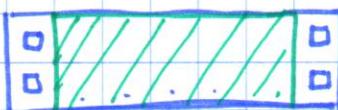
□ p-type



Device Parasitics

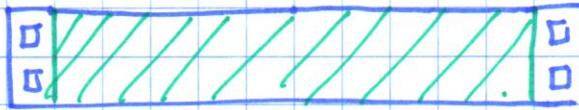
1. Resistor

$$R_1 = 500\Omega$$



R_c 500Ω R_c

$$R_2 = 1000\Omega$$



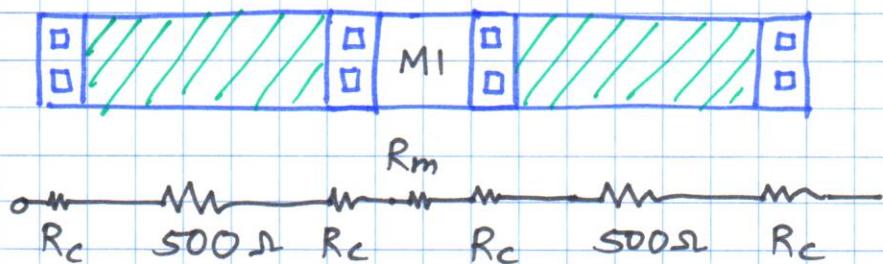
R_c 1000Ω R_c

R_c - contact Resistance
- parasitic -

Will NOT Match

generally much higher
than Metal R

Better implementation



R_m - metal R

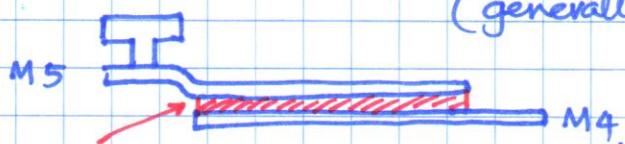
R_c - contact R

$R_m \ll R_c$

2. Capacitors

MIM — Metal Insulator Metal Cap

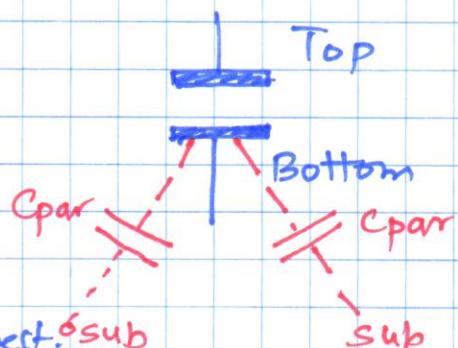
— Requires special mask layer to create thin oxide between two metals.
(generally top two metals)



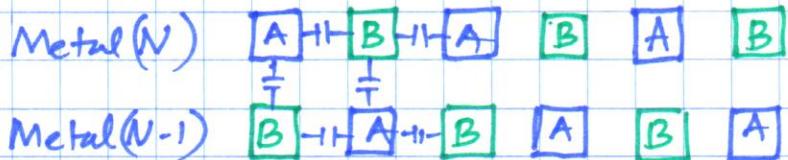
Thin ox - special mask layer

Bottom plate has large
parasitics

→ Try to use it as and connect δ_{sub}

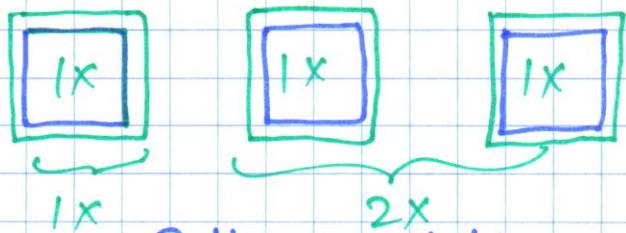
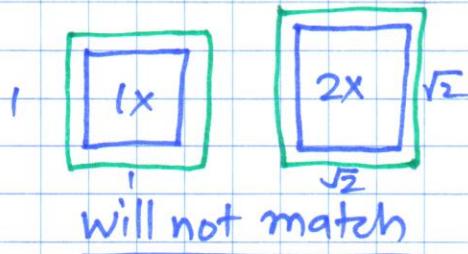


MOM capacitor Metal Oxide Metal
— No special Mask needed



Good density in high Metal layer count process.

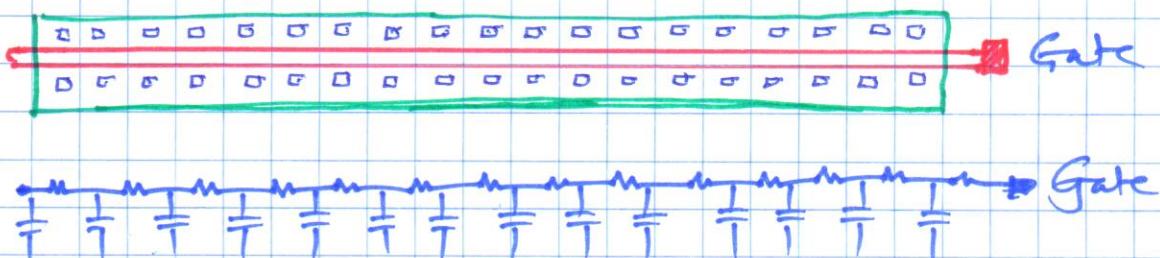
Cap Matching



- Make sure you watch out for fringe cap.
- Keep identical environment around matched caps.

3. Mos Devices

Consider Device size $W = 10 \mu\text{m}$ $L = 0.05 \mu\text{m}$.



Long poly - large parasitic R + distributed cap.

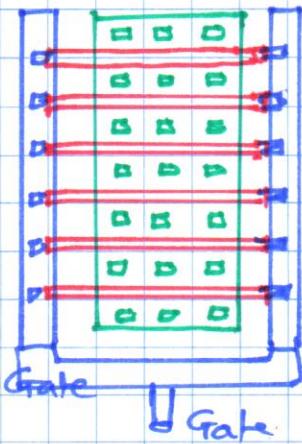
→ Bad idea. → ↑ Noise

→ RC delay

→ Cap Quality factor

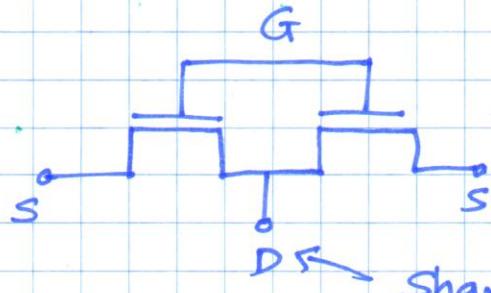
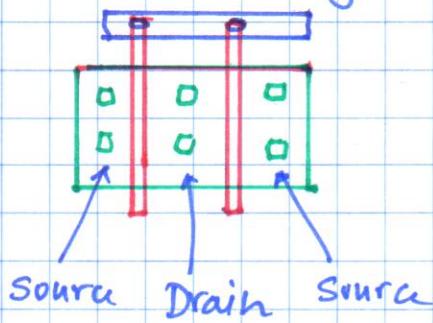
→ Increase number of fingers.

→ Connect gate with metal — poly resistance \gg metal R.



→ Minimize gate resistance - RF performance

Reducing Drain Parasitics — Shared drain



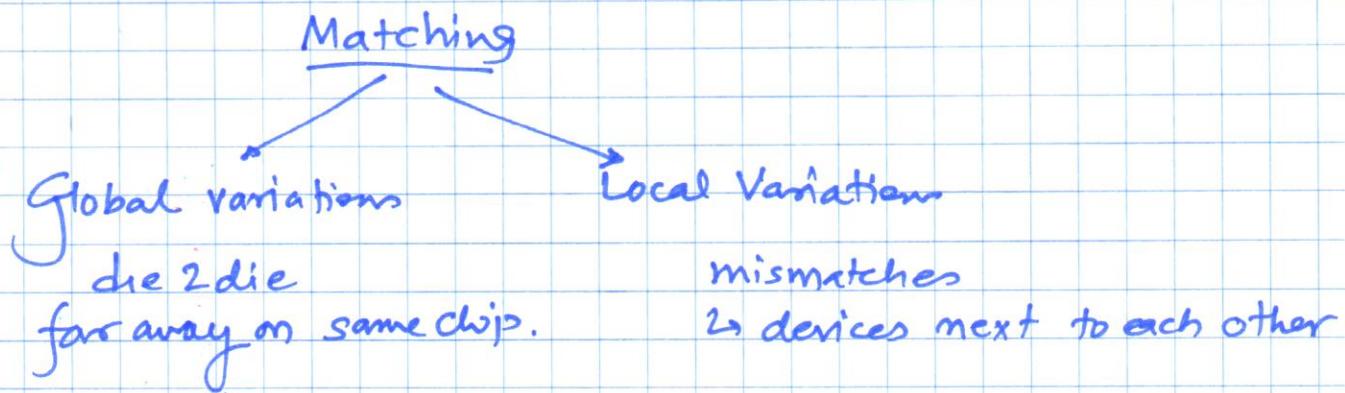
Shared drain
→ Reduced parasitics

Well or Substrate connection for NMOS / PMOS

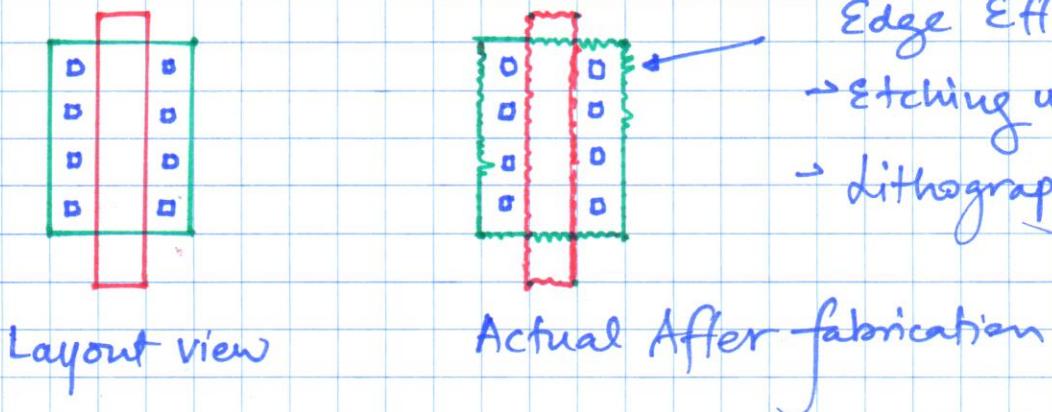
↳ Latchup considerations → Should have connection every $10 \times 10 \mu\text{m}$ space (for example)

→ Connect to indiv. transistor or @ block level

} judgement based on application



Random Mismatch



Matching Improves with increase in area (WL)
→ Edge effects get averaged.

Process Variations

→ Mask Alignment

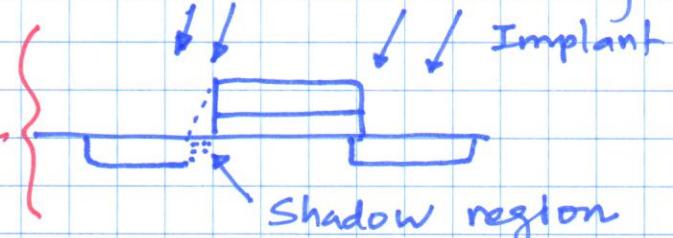
→ Shadowing effect

→ Proximity Effect

→ Gradient Effect

→ Lateral Diffusion.

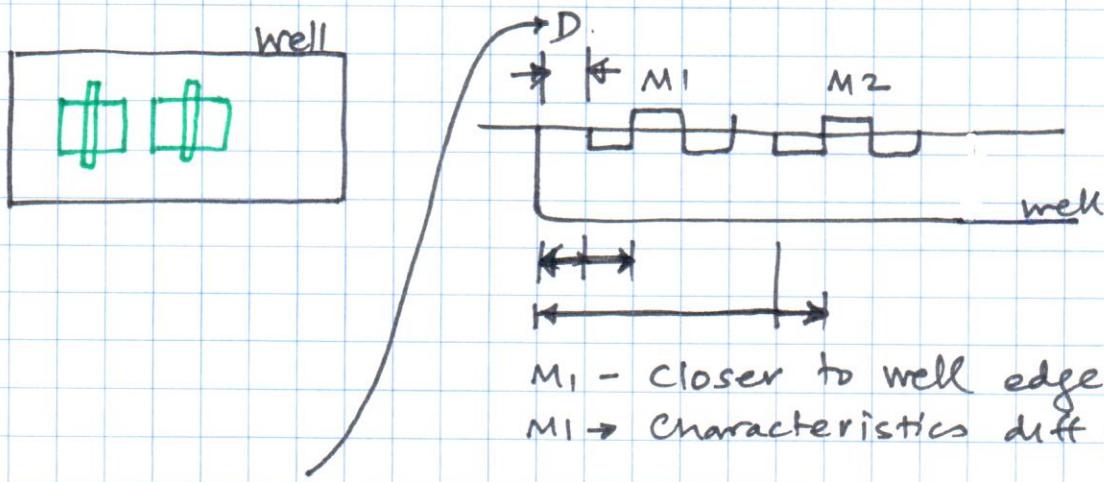
→ Due to inaccuracies in fab.



→ Well prox. WPE

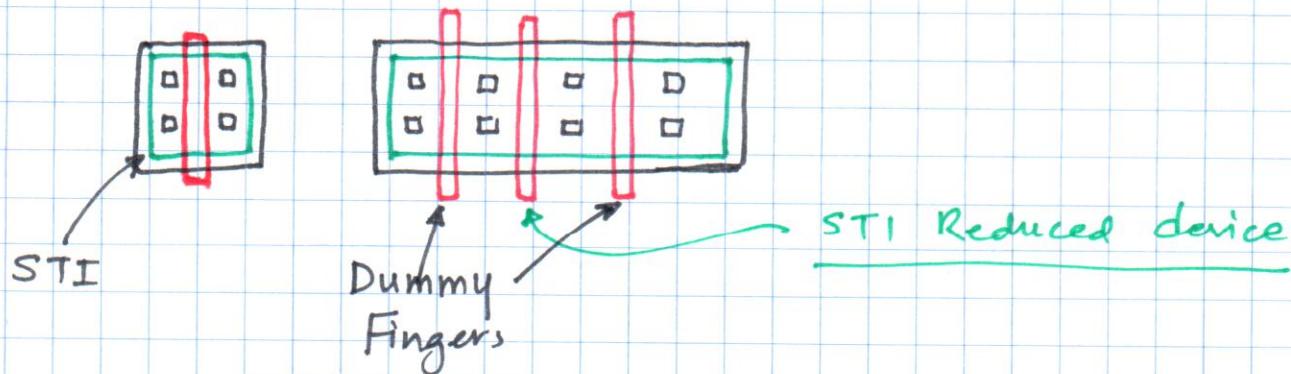
→ STI - Shallow Trench Isoln

* WPE Well proximity effect



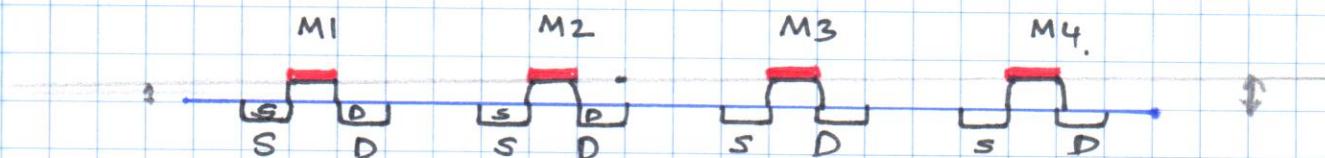
Increase D so that WPE is minimal.

* STI Shallow Trench Isolation effect



STI - to avoid formation of device between adjacent transistors. - Oxide trench. - Stress effect.

* Gradient Effect

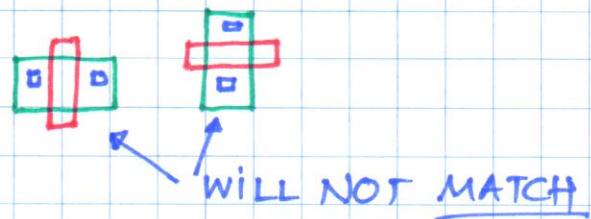


M₄ & M₁ will not match.

→ Common Centroid layout so that two dimensional gradient is cancelled out.

Critical Matching

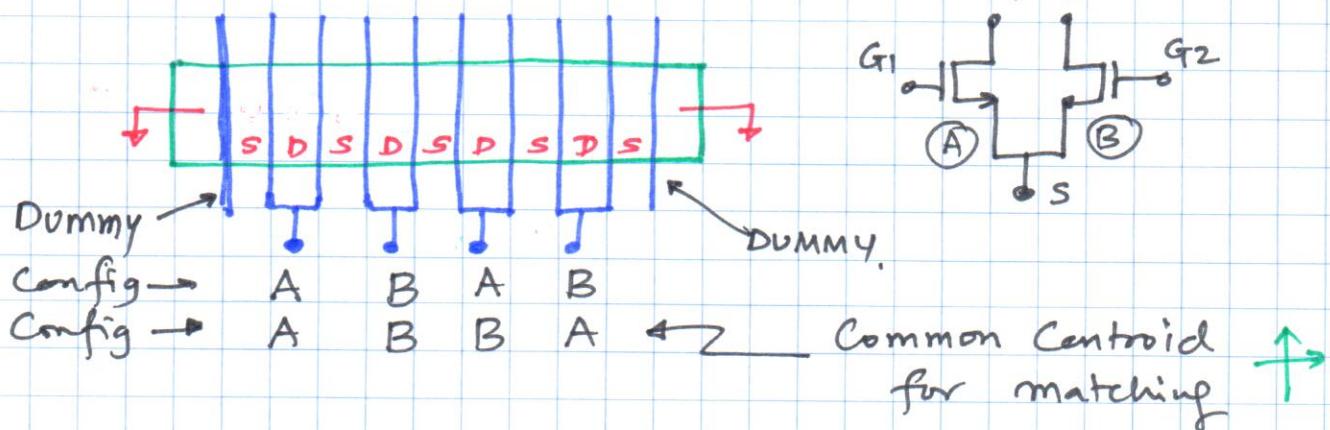
- * Unit cell layout
- * Device orientation



- * Direction of current flow



- * Interleave Devices



- * Common Centroid layout-



Gradient in
any direction
cancelled.

Keep dummy devices around matched
devices to reduce edge effects.

* INTERCONNECT

→ parasitics



MINIMIZE
SYMMETRICALIZE["]

High current lines - reduce $\cdot R \rightarrow IR$ drop ↓

High Frequency Signals → Reduce $C \rightarrow$ Loading ↓

General Guideline

Use M1-M3 (lower Metals) for DC bias signals
(Thin metals)

Use M4-M5-M6 (High Freq) Signal Lines

↳ Reduce parasitic cap to substrate

Use Top thick metals (very low R)
 $2x, 4x$ thickness

↳ for VDD, GND lines.

Make these fat.

DO NOT SKIMP ON Metal.
(avoid overlap with signal lines)

In 28nm & below → Electromigration concern.

→ Burnin Issue.

Metals can carry limited current (Metal Width Shrinking)

Strong Temperature Dependent

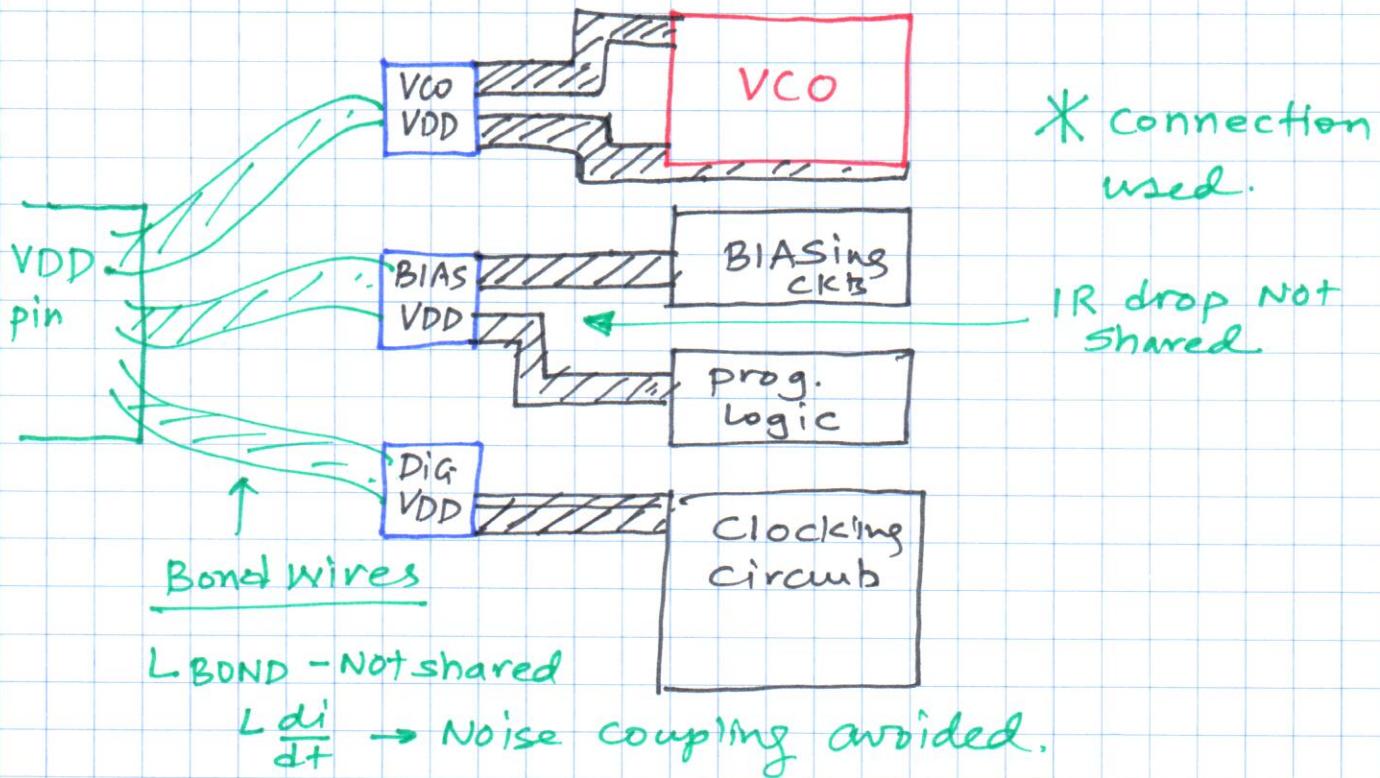
115°C

125°

1μm M1 XmA 0.7XmA 30% less.

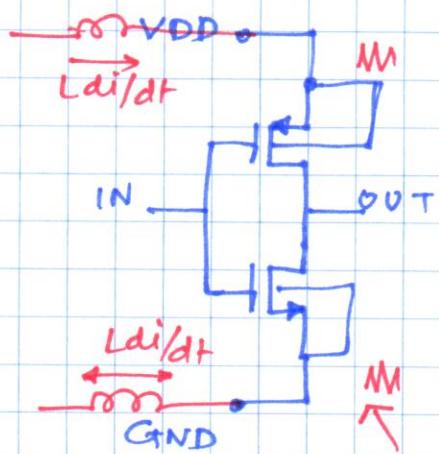
→ CAD tools can be utilized to identify violation.
VolthusFi

* Supply / Ground connections

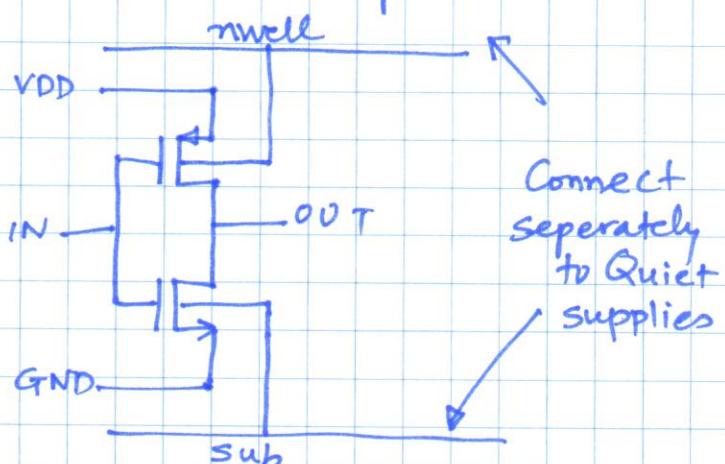


* Substrate & Well connection

→ Important to avoid latchup.

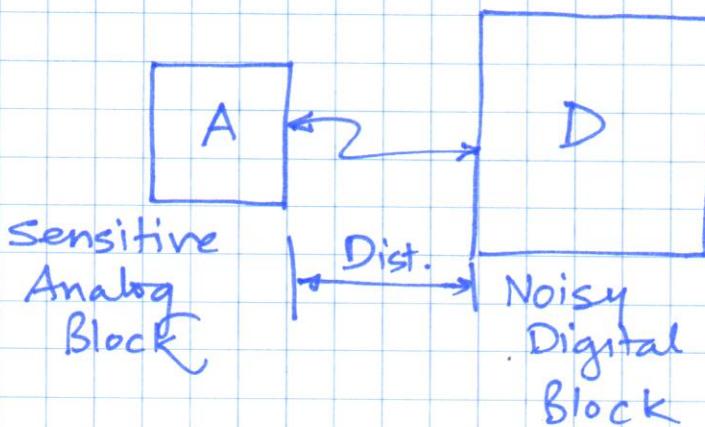


Noise coupled
to other ckt

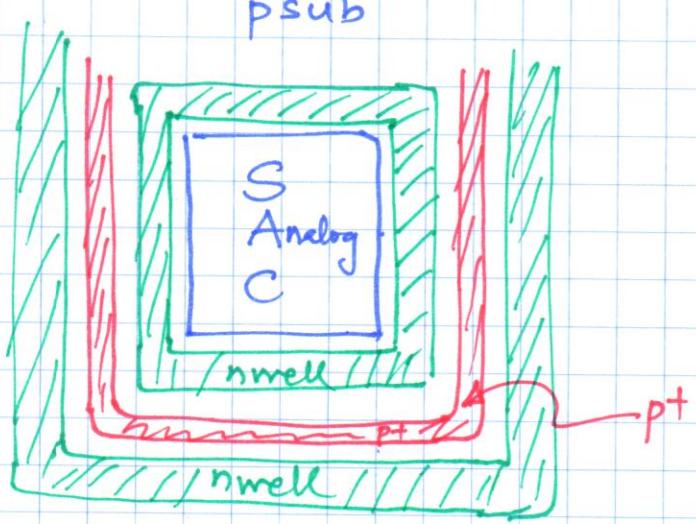
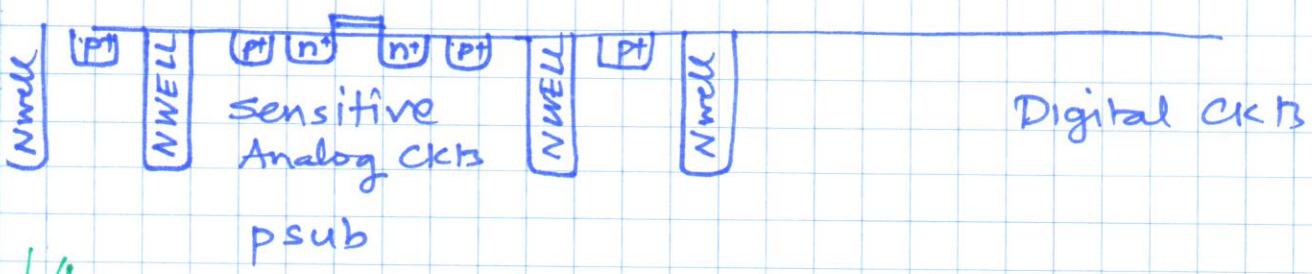


Locally generated noise (switching) is not transmitted to other (sensitive) circuit

* ISOLATION & COUPLING



- ① → Maximize Distance D - Die area issues.
- ② → Guard Rings.



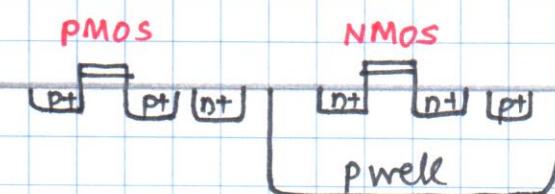
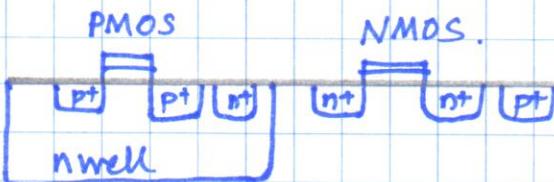
Like Moat around castle.

③ → Create isolated (Electrically) substrate

Deep-Nwell

→ Extra Mask Layer

Great for RF - Mixed Signal SOCs.

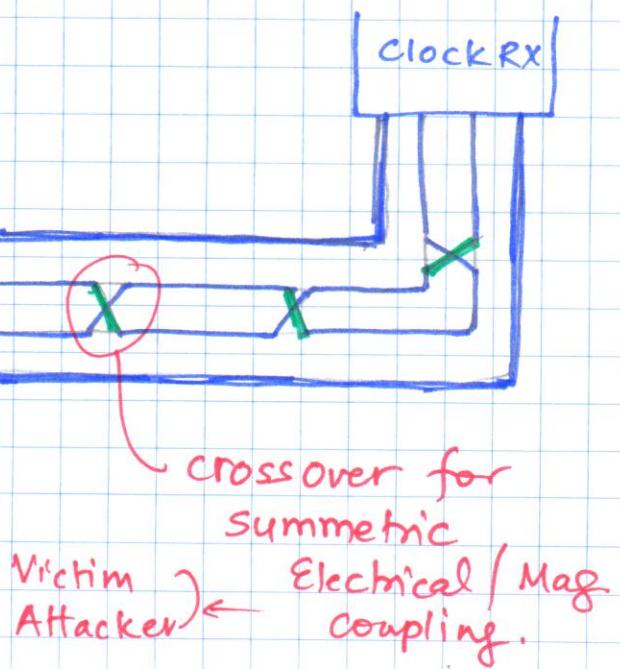
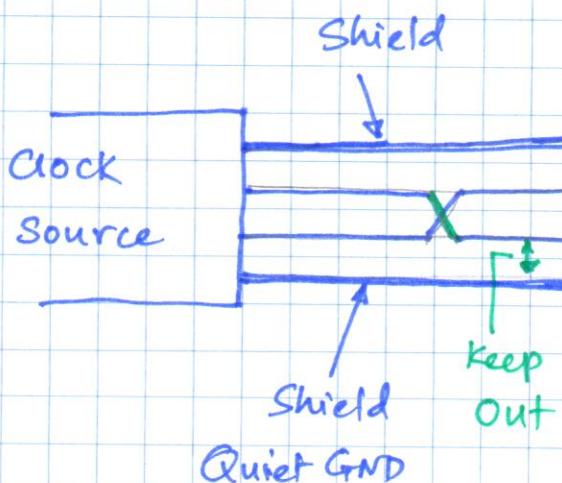


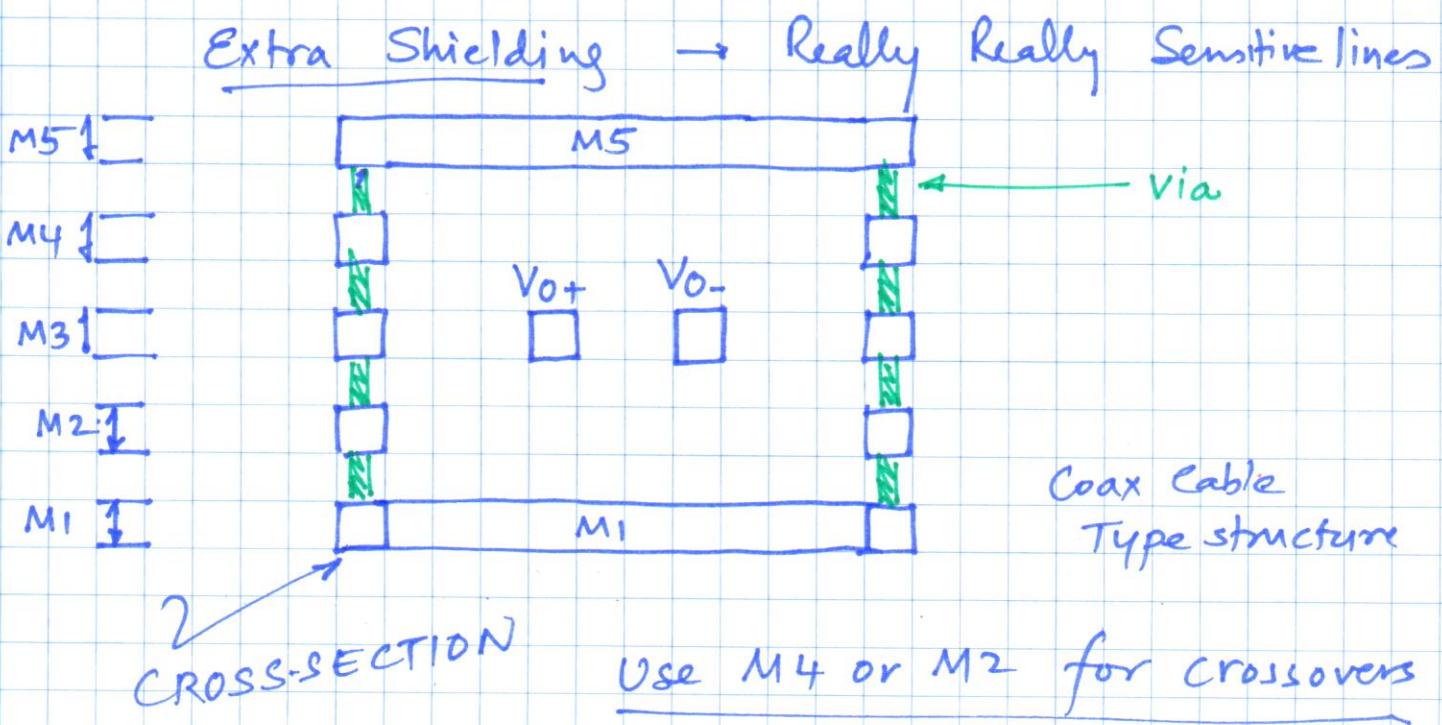
Deep Nwell

p-substrate
NMOS - in bare substrate
Body connection - sub
→ common ground

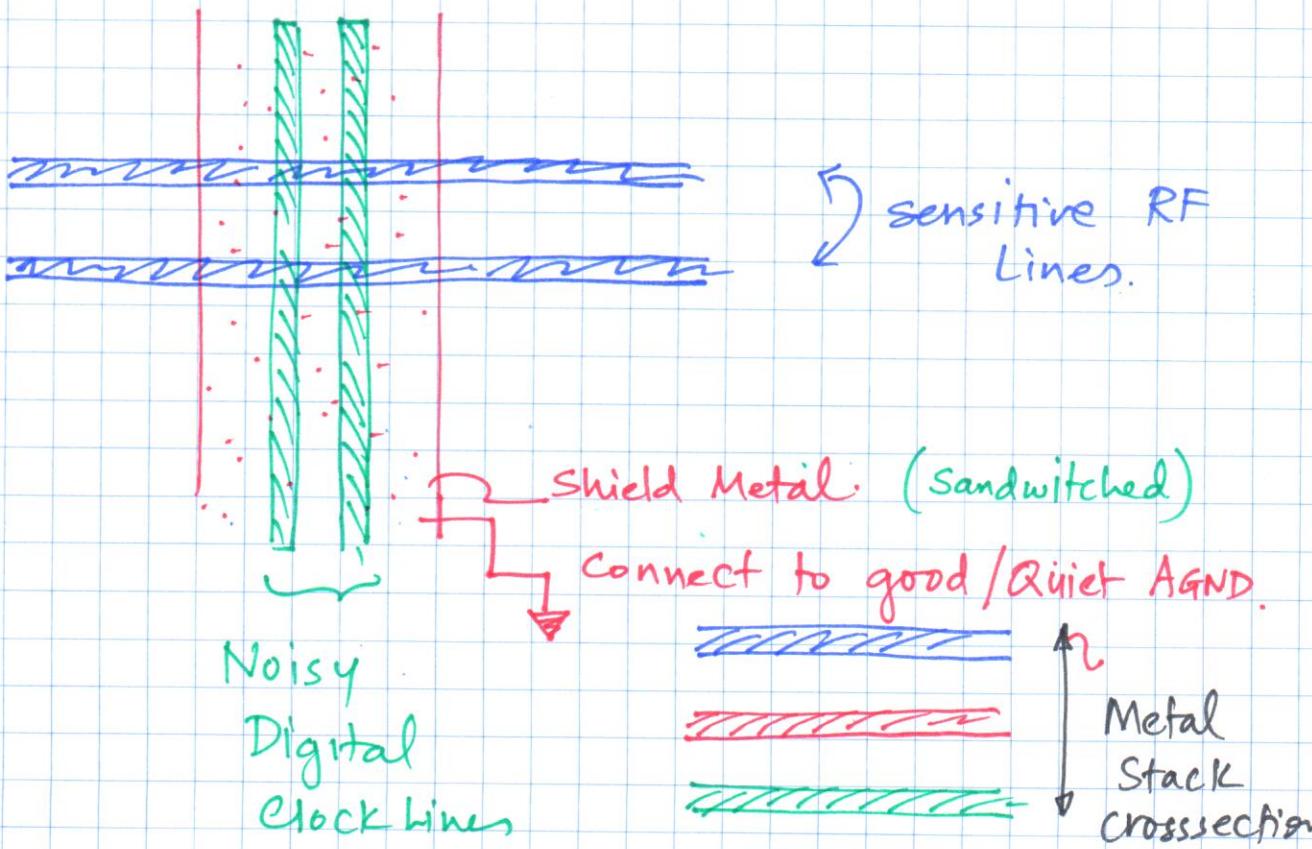
- NMOS in isolated pwell.
- Each NMOS can have separate well connection
- isolated from substrate noise.

④ Shielding Techniques



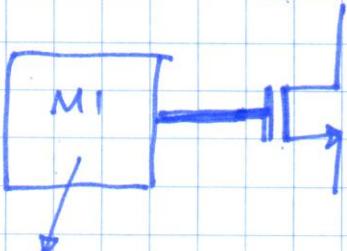


Connect Shield to good analog ground.
 ↳ Quiet with low ohmic ^{impedance} ~~resistance~~.
 @ frequency of operation.



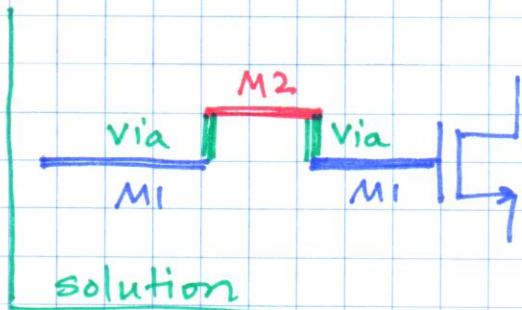
Other Important Issues

* Antenna Effect



large piece
of metal 1

Routing etc.



solution

Collects ions/charge during etching
+
damages gate oxide.

→ Checked during DRC

* Metal Fills

In advance CMOS processes, with high number of metal layers, metal density needs to be carefully controlled within certain range.

→ depends on Fab requirement

→ Driven by Chemical Mechanical Polishing

→ planarization of all metal layers

→ Design for manufacturability

→ After all chip layout done

+ auto tool adds/sprays spangles of metal pieces to meet foundry requirement-

→ Pieces of metal over sensitive circuits

can mess up symmetry, added coupling etc.

- Do metal fills @ block level
- RF/analog sensitive blocks - do manual fill & then extracted sims with fills
- Can be a show-stopper if done @ last min.

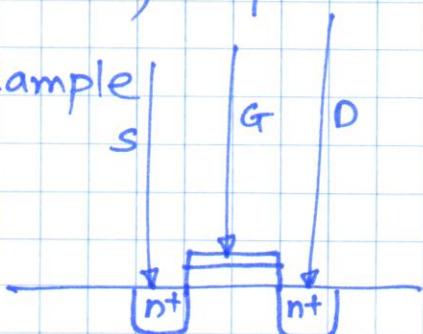
* Planning For Metal Mask Changes

- Assume you will have bugs
- Add programmability / flexibility (digital)
- Observability (test o/p's)
- Add Cya-Cyb circuits
- Make sure you can use top metals to fix connections

Top metal mask 10K \$

M1 , Poly 50-60K \$.

- Example



Bring all S,G,D
on all metals.

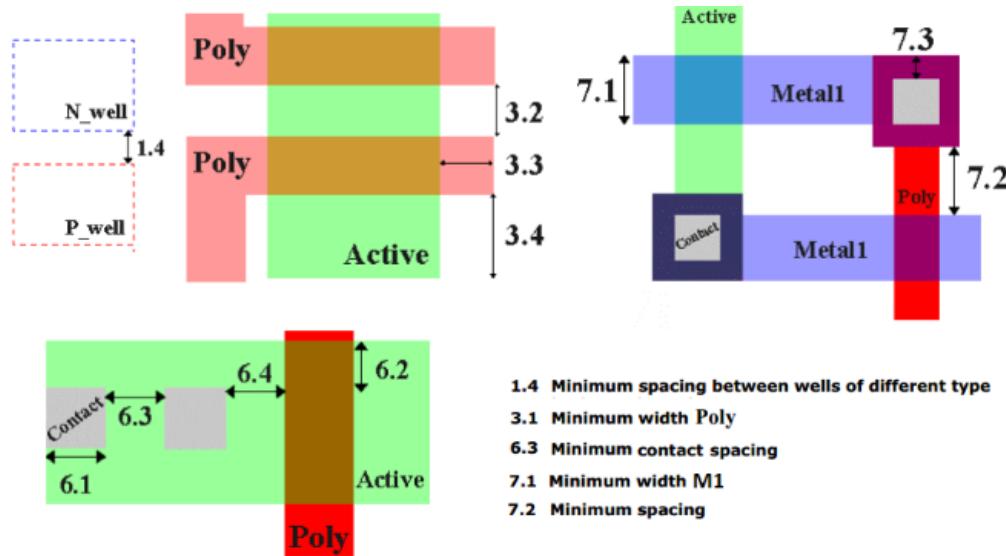
← Spare kit

→ Keep them as filters
in empty spaces.

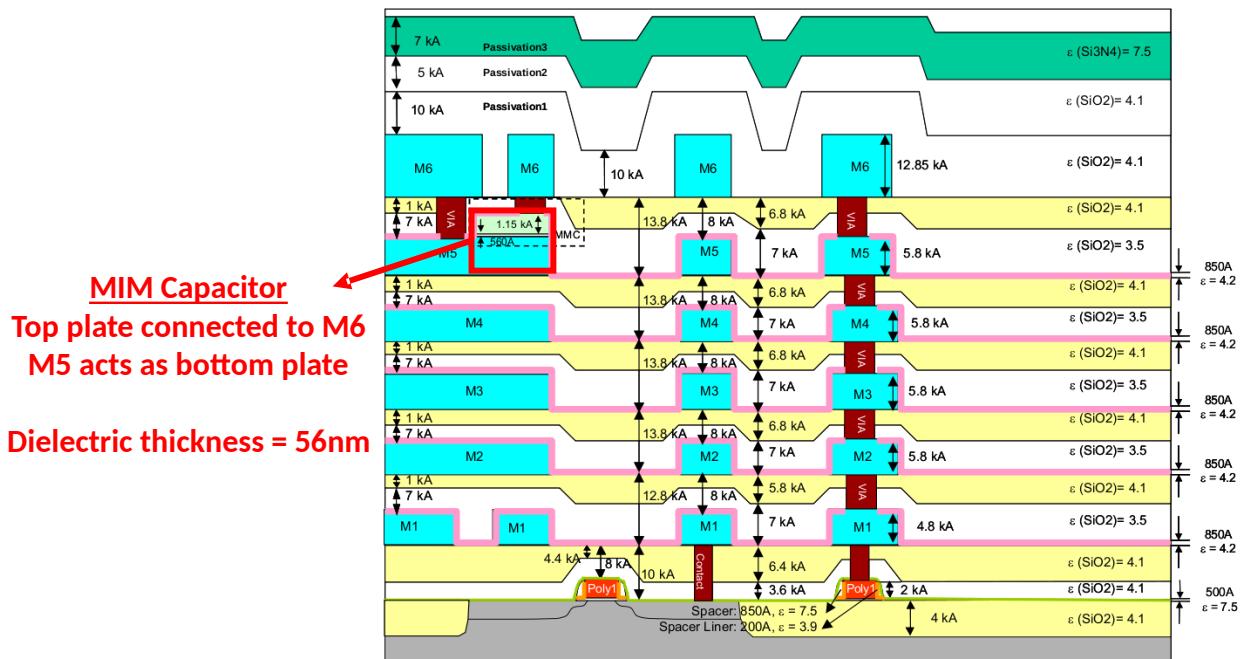
* Chip Planning

- City planning — architecture
 - Board level layout / parasitics
 - Supply / ground / Signal Routing @ board level
 - Define package pin-outs / bonding diagram.
 - Floorplan your chip
 - Signal / clocks / Vdd / gnd flow
 - Isolation between sensitive circuits
 - Digital Circuits can also fail due to IR drops. Check VDD / GND IR drops
 - Top level (chip level) connectivity check
 - Simulate power up / down
 - Reliability Checks.
 - Electro-migration checks.
 - make sure circuit somewhere else is not interacting with your ckt.
 - Sensitive Routing R/L/C extraction to gain confidence
 - Just Maskset for 28nm CMOS can cost ~ 1 million \$.
 - + 4-6 K\$ per wafer processed.
- ① Use all neurons / compute power before tape-out.

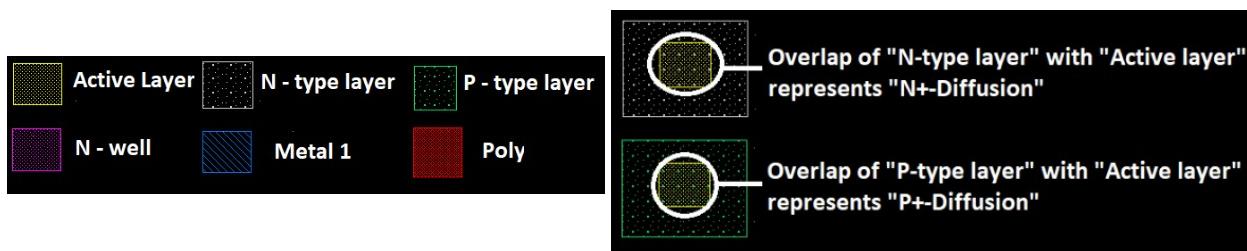
Sample of Design Rules provided by the foundry
 (Below shown rules doesn't correspond to SCL process)



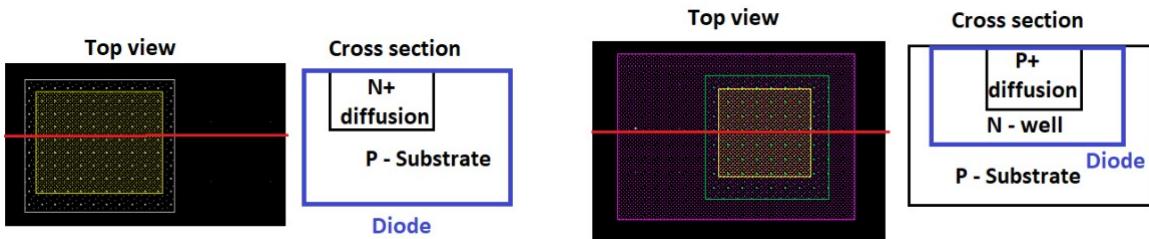
Interconnect layers (Doesn't correspond to SCL process)



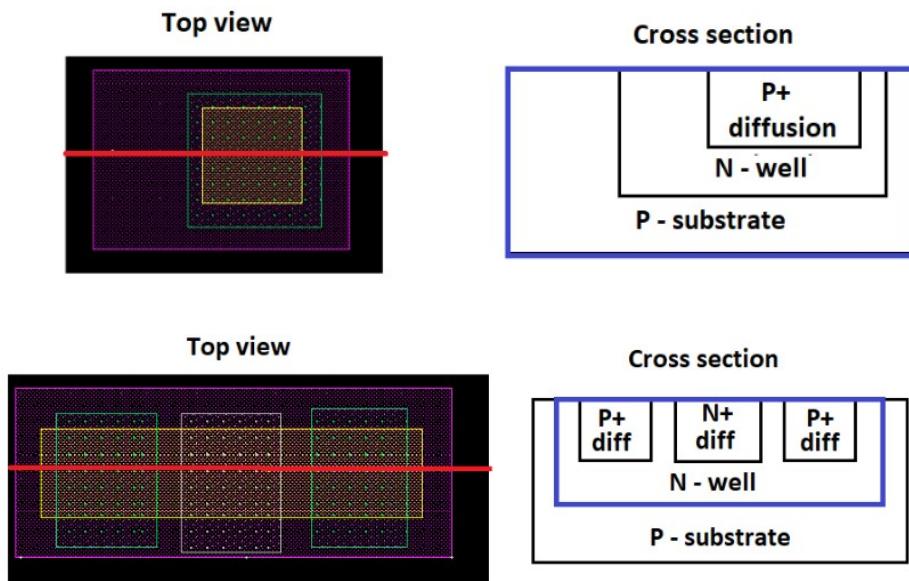
Basic Layers in SCL 180nm



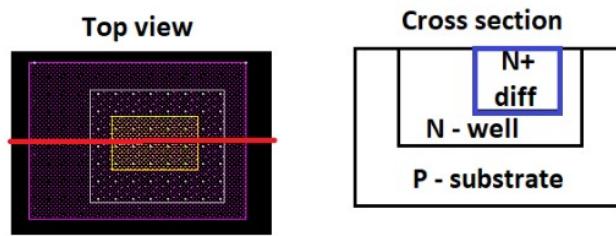
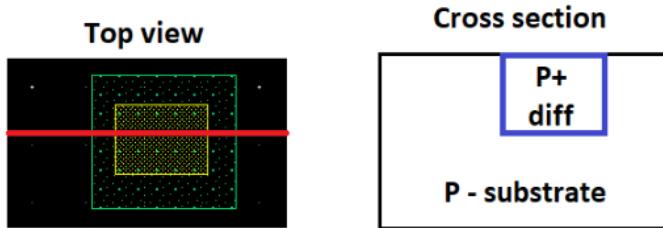
Different ways of forming Diode



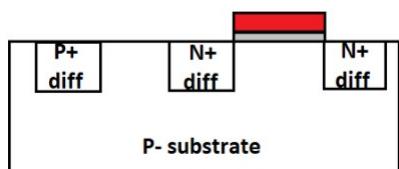
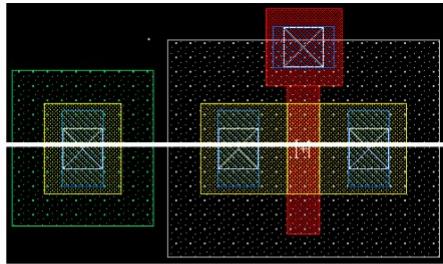
Different ways of forming BJT



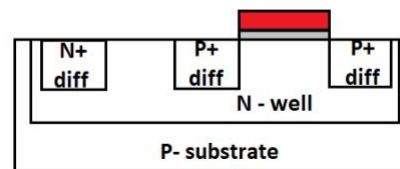
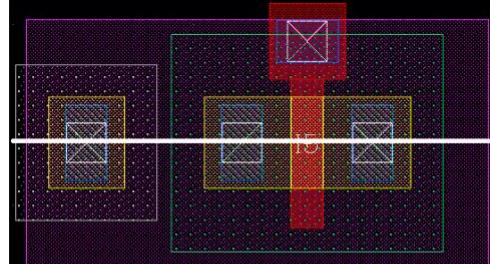
Contacts to regions



Top View of NMOS



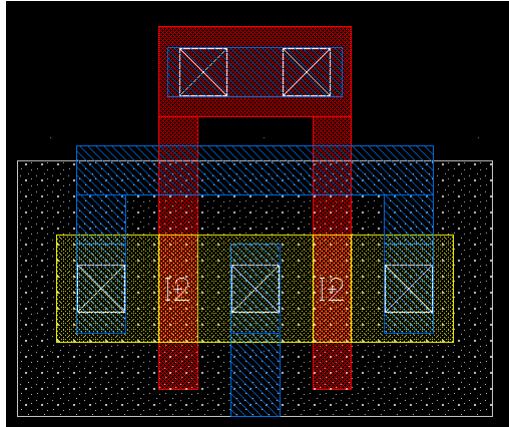
Top View of PMOS



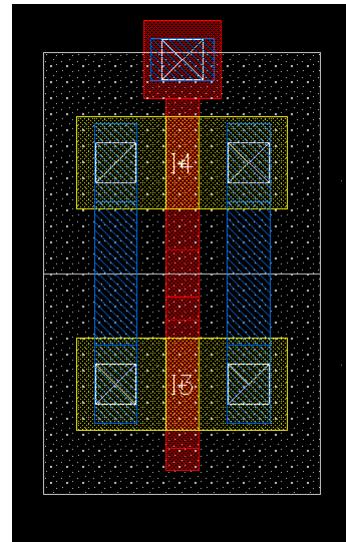
Cross sectional view of NMOS

Cross sectional view of PMOS

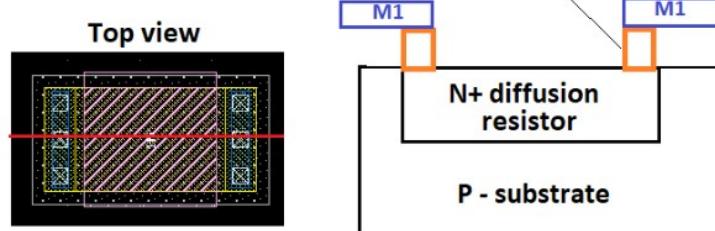
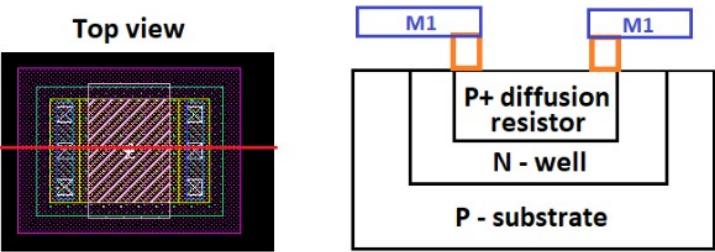
NMOS
 Total width = (0.5um) x 2 fingers = 1um
 Length= 0.18 um



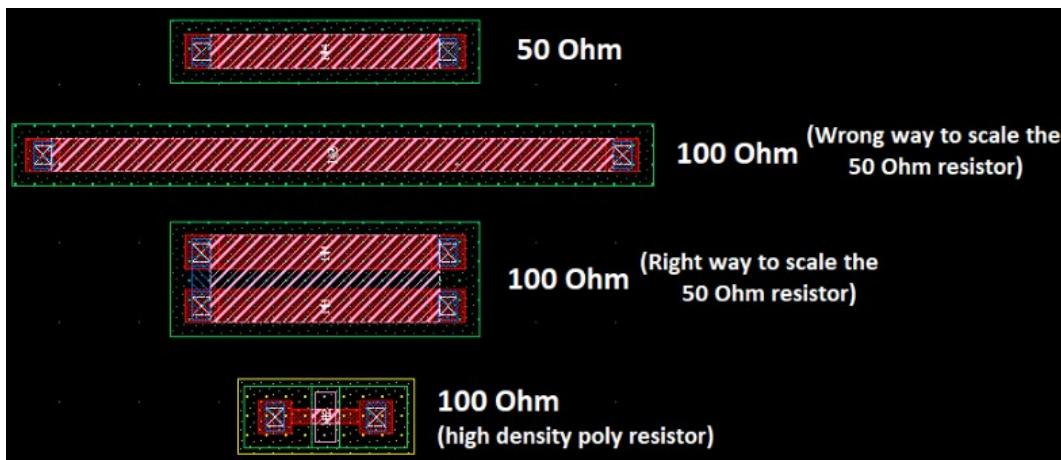
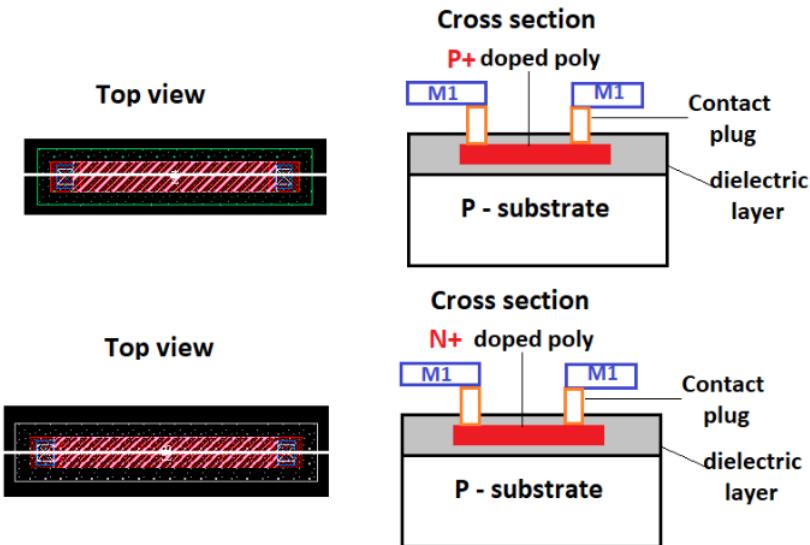
NMOS
 Total width = (0.5um) x 2 multiples = 1um
 Length= 0.18 um



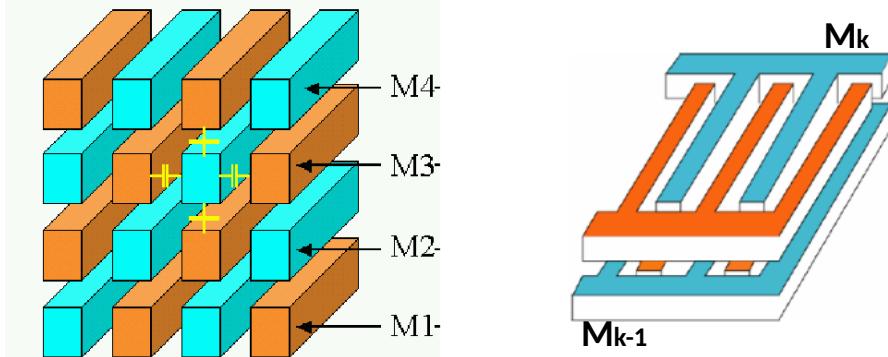
Diffusion resistors



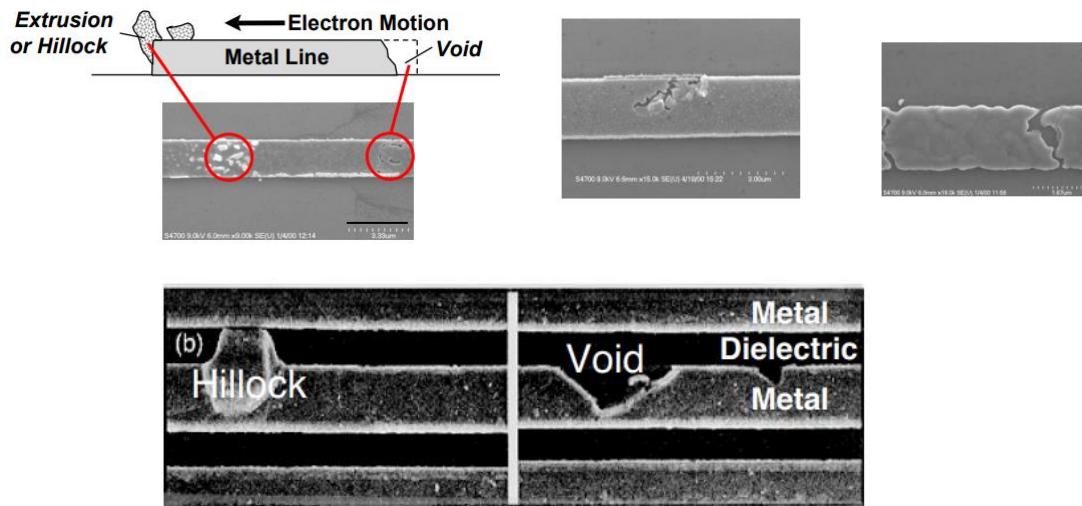
Poly resistors



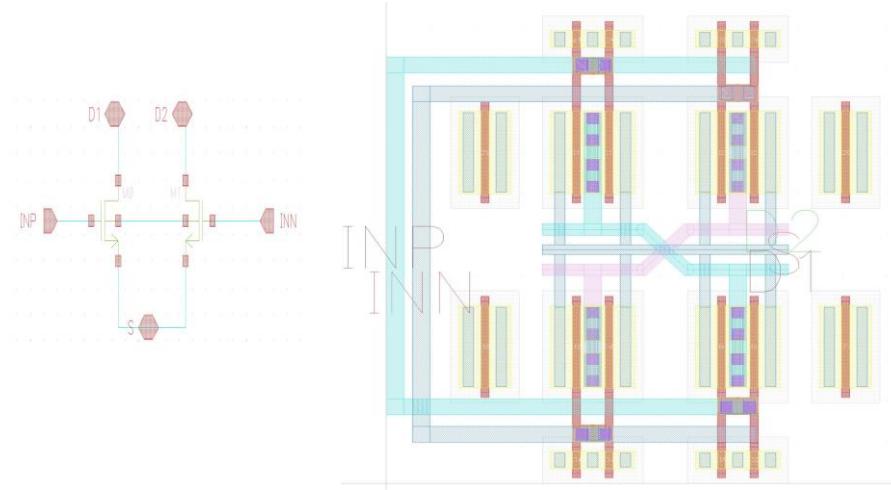
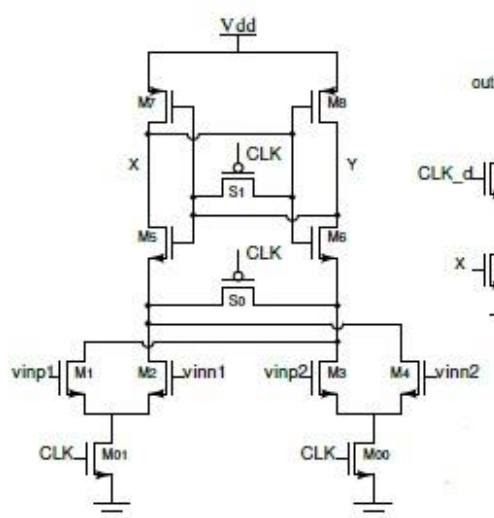
MOM Capacitors



Electromigration failure



https://web.stanford.edu/class/ee311/NOTES/Interconnect_A1.pdf

Layout of the Input Pair of OpAmp using Common-Centroid**Comparator Schematic****Layout**