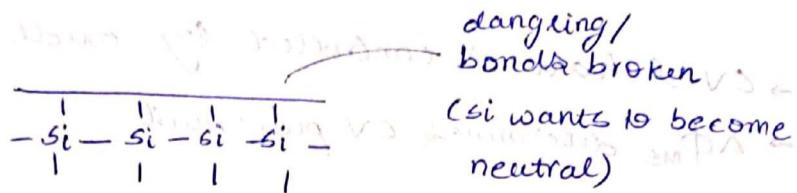
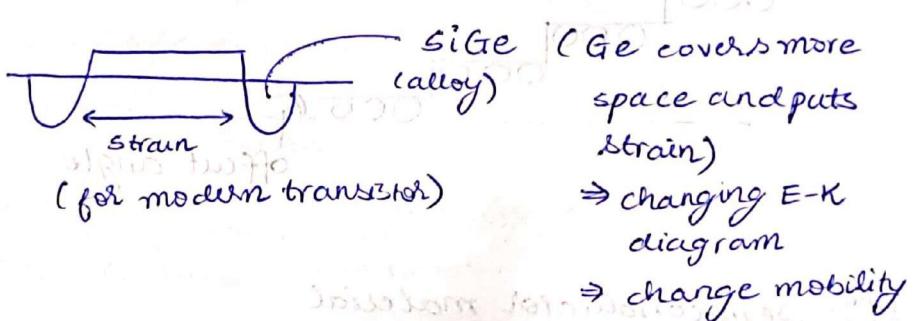


30/7

- Damage annealing:
for creating n/p type we want the impurity to replace the Si atom. so we bombard the Si with impurity
- oxide layer
 - i) can be directly deposited
 - ii) grown by exposing to such an environment (Si has good e affinity)



→ oxide passivates dangling bonds
 Also controls charge flow in the channel/interface



- clean room
 - yellow light colour is important (else photo sensitive reactn are triggered)

3/8

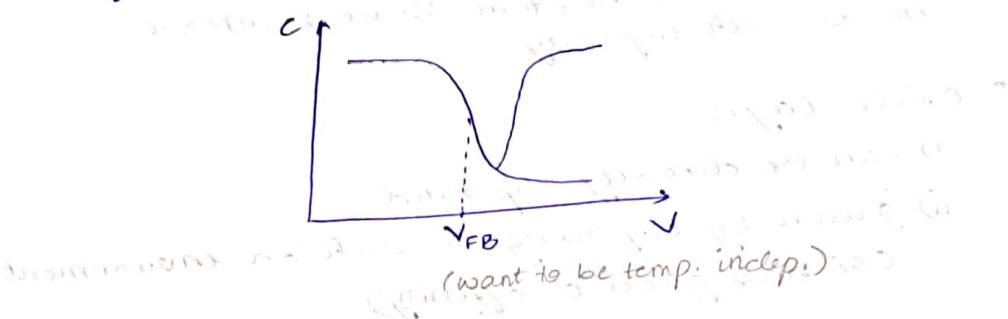
• WAFER CLEANING

$$C = \frac{EA}{d}$$

since A was shrinking, we were reducing d to keep C const.

$$\Rightarrow Q = CV = \text{const.}$$

- High K have higher ϵ , no need to reduce d

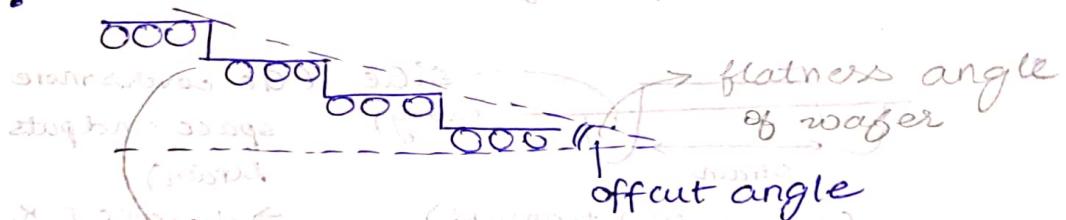


- CV behaviour controlled by oxide
- $\Delta\Phi_{MS}$ determines CV placement

→ For Si

III - lowest formation & surface energy

.



desired: to minimize no. of steps/terrace
(offset angle reduced)

Semiconductor material

A) group N (C, Si, Ge, Sn)

B) SiC (rectifier developed on it)

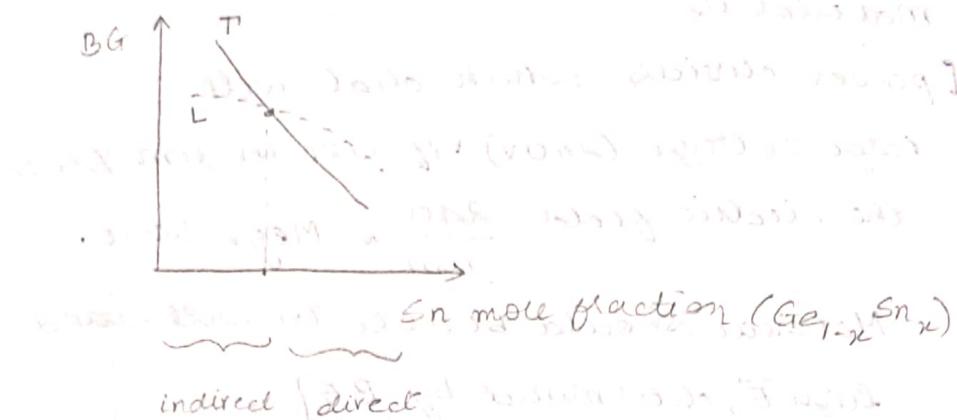
C) group VI (S, Se, Te)

D) III-V

E) II-VI (usually p-type)

- Hard to break bonds of large bandgap material
- silicone having indirect bandgap coz they carriers generated don't easily recombine and have high lifetime.
- getting p-type ZnO is diff.

- group 4 indirect BG hence we don't have opto electronic devices made from them
- T : direct transition
L : indirect transition whichever is lower is used for transition



6/8

- GaAs bond stronger than Ga-Ga & As-As

- ↳ to make need to combine a liquid & a gas
- Ga has low vapour pressure
- exact 50:50 composition requires high pressure environ.

- at 650°C As at vapour state
- shape of crystals determined by the thermodynamics
- Polycrystalline / multicrystalline have a single phase
- Boron trioxide is used to prevent the escape of gas
- getting reactive nitrogen is very difficult
 - nitrogen-nitrogen have triple bond
 - one of the strongest bond
- Hence don't get single substrate GaN in market

(blue light emission)

- Mobility: determines how fast we can turn a switch on/off
(e⁻ moving through crystals: bulk mobility)

Bandgap: decides how strong / robust the material is

[power devices which deal with large voltage (240V) ; if size in μm scale the electric field $\frac{240}{\mu\text{m}} \sim \text{Mega scale.}$

Material should be able to withstand high E , determined by BG]

\Rightarrow SiC, GaN used in power devices

T_{max}: max temp. at which material is stable

- Doping shouldn't change the intrinsic material structure else it surfaces as defects

3/8 complementary MOS

Adv: no static power leakage

since n & p present in one substrate

- choosing a substrate

\rightarrow when we break a Si plane it breaks at 60° (111 plane)

\rightarrow we desire a highly resistive wafer (but cost!)

\rightarrow large wafer size preferred however uniformity is a concern

\rightarrow can't be made using float-zone Tech

\rightarrow large wafer require special infra

\rightarrow flatness:

minimum step height = 1 atomic plane

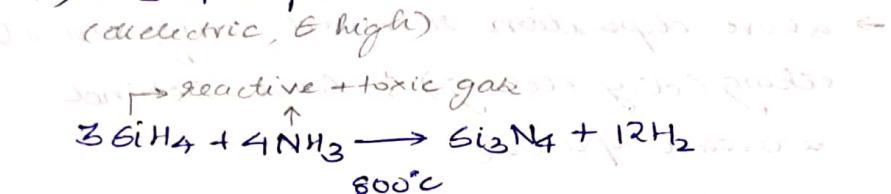
- Standard P-type wafers

- i) P-Si (100), S-20 μm
- ii) SiO_2 growth @ 900°C , H_2O

Need a source of oxygen (dry oxygen)

(otherwise H_2O from H_2 makes process slower)

- iii) Si_3N_4 deposition



Si_3N_4 deposited by LPCVD (low pressure chemical vapour deposition)

- iv) photo resist = soluble in water when exposed to some light
- photosensitive: resistance changes

→ SOI (silicon on insulator) used nowadays

Pg: 49 - 63

13/8

- replacement gate process used nowadays since SiO_2 not used currently (earlier process req. SiO_2 to be grown on Si)
- rather using poly silicon gate we used pure metal, mixed metal gates nowadays

In-situ: part of integrated process

- positive photoresist better: gives sharper edge
- negative photoresist - cheaper, however finer details not exactly met
- Thick field oxide: used to isolate h/w gate and source/drain
- conformal deposition: deposition thickness uniform all over
 - above deposition removed using anisotropic etching (dry etching); leave behind sidewall spacers
- Now a thin oxide layer deposited on the gate before exposing to Arsenic and forming source & drain
- even if we make source/drain beyond gate we would need to form the sidewall spacers since they are required for forming metal contacts
- RTA (rapid thermal annealing)
 - very fast process compared to standard

The graph illustrates the temperature profile for RTA compared to standard annealing. The y-axis represents Temperature (T) and the x-axis represents time.

 - RTA:** The temperature rises sharply from room temperature to 900°C, remains constant for a short duration (labeled "RTA"), then drops sharply to 500°C, and finally cools down to room temperature at a rate of 5/min.
 - Standard:** The temperature rises sharply from room temperature to 900°C, remains constant for a longer duration (labeled "standard"), then drops sharply to 500°C, and finally cools down to room temperature over 30 minutes.

- Dry etching preferred over wet
Anisotropic etching is usually dry etching
wet etching doesn't always give sharp edge
dry etching is orders of magnitude faster
- Ti has inherently better sticking property
 - also when it reacts with Nitrogen it forms a compound which is also sticking (TiN)
⇒ preferred for forming metal contact
- Al makes better contact however it has strong electronegativity, so it gets easily oxidized
 - hence capped with gold
 - however if we don't want gold so we cap it with Ti

⇒ Ti-Al + several contact layers make the structure stable, and prevents diffusion

* Device physics + etching (60-70%)

- Substances present on wafer that can act as impurities:

- i) surface films (SiO_2 , poly silicon, silicides, metals etc.)
- ii) oxides
- iii) photoresists
- iv) undesirable elements such as metals ($\text{Fe}, \text{Au}, \text{Cu}$ etc) and alkali ions (Na^+, K^+ etc)
(present in machines, chemicals and humans).

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2qEN_a(2\phi_F)}}{C_{ox}} - \frac{2\phi_M}{C_{ox}}$$

where, ϕ_M = mobile charge density
(number of charges per cm^2)
associated with Na^+ or K^+ in
the gate oxide

- In silicon devices, junction leakage current are dominated by SRH recombination

$$\tau_R = \frac{1}{\sigma D_{th} N_t}$$

τ_R = recombination lifetime

σ = capture cross section of the trap

V_{th} = minority carrier thermal velocity

N_t = density of traps

- $\text{Au}, \text{Cu}, \text{Fe}$ form deep-level traps. They are expensive to remove hence 'gettering' is used to remove them from critical areas.

- . levels of contamination control: wafer cleaning
 - i) clean factories
 - ii) wafer cleaning
 - iii) gettering

CLEAN FACTORIES

class X: in each cubic foot of air in the factory, less than X total particles have size greater than $0.5\mu\text{m}$

- particle size that are major concern in semiconductor plants are between 10nm and $10\mu\text{m}$ in size.
- particles smaller than 10nm tend to coagulate into larger sizes.
- those larger than $10\mu\text{m}$ tend to become heavier and precipitate.
- B/w 10nm to $10\mu\text{m}$ remain suspended in air for a long time.
- such particles deposit through 2 mechanisms:

(A) Brownian Motion

random motion in the air that occasionally brings them in contact with a surface

(B) Gravitational Force

particles settle due to gravitational force

HEPA filters

(High Efficiency Particulate Air)

- composed of thin porous sheets of ultrafine glass fibers ($<1\mu\text{m}$ diameter).
- room air is forced through with a velocity of 50 cm/sec .
- large particles are trapped; finer particles

stick to the fiber through electron forces. Even neutral particles stick due to difference in work function.

- water used is also cleaned
 - it is filtered to remove dissolved particles and organics
 - dissolved ions are removed through ion exchange or reverse osmosis.

WAFER CLEANING

i) Photoresist removal

- photoresists are organic compounds
- For front end (no metals on wafer)



Acid + strong oxidant decompose the resist in CO_2 & H_2O

ii) Oxygen Plasma

converts resist to CO_2 & H_2O

Advantage of reduced pollution & good selectivity

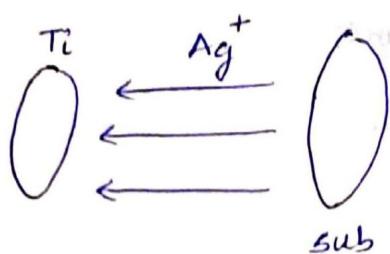
- For back end

i) Oxygen plasma

ii) Phenol based organic strippers

- Front end processes involve high temperature (oxidations, anneals, film deposition) while back-end occurs at low temp
- RCA CLEAN

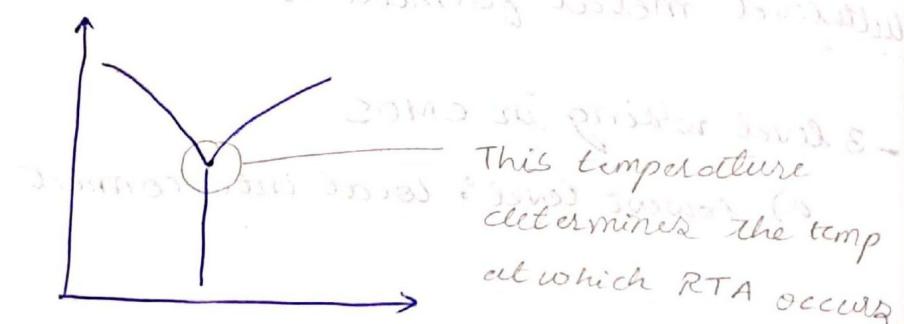
(GIA) Standard process after cleaning of acids, bases and deionizers (waterless wash) followed by rinsing and preliminary cleaning (dilute).



- CVD helps to get conformal (uniform thickness) deposition
- Sputtering = physical vapour deposition (PVD)
- TiS_2 (formed on annealing) molds the work function such that it forms an ohmic contact on both n & p

• Phase diagram

- useful when looking for new material



- TiN although conducting, isn't very good; not used for communication
- deposition rate in sputtering is low
- SiO_2 doped with P and B to protect against Na^+
- B also forms a liquid surface and hence helps in surface smoothening
- smooth surface needed for photolithography

gettering

- used to remove bulk defects
 - to remove stray ions, need to oxidize them
 - need oxygen source
 - prevent them from forming defects
- * Nucleation (atom + defect) \rightarrow atom + defect

CHAP 4 : FORMULAE

$$f = \frac{1}{q\mu_{nn} + q\mu_{pp}}$$

$$F(E) = \frac{1}{1 + \exp\left(\frac{(E - E_F)}{kT}\right)}$$

$$N(E) = \frac{4\pi}{h^3} (m_e^*)^{2/3} (E - E_c)^{1/2}, \quad E > E_c$$

$$N(E) = \frac{4\pi}{h^3} (m_n^*)^{2/3} (E_v - E)^{1/2}, \quad E < E_v$$

$$n_i = \int_{E_c}^{\infty} F(E) N(E) dE$$

$$\approx N_c \exp\left(-\frac{(E_c - E_F)}{kT}\right)$$

$$P \approx N_v \exp\left(-\frac{(E_F - E_v)}{kT}\right)$$

$$np = n_i^2$$

$$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

$$p = n_i \exp\left(\frac{E_i - E_F}{kT}\right)$$

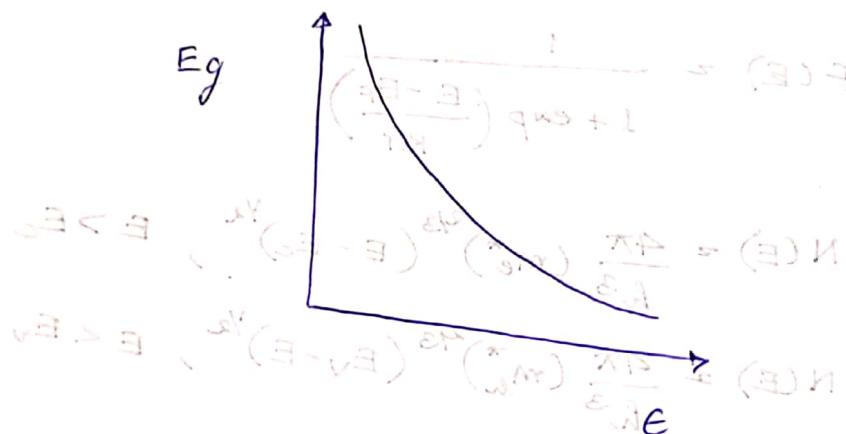
$$N_D^+ + P = N_A^- + n$$

$$n = \frac{1}{2} \left[(N_D^+ - N_A^-) + \sqrt{(N_D^+ - N_A^-) + 4n_i^2} \right]$$

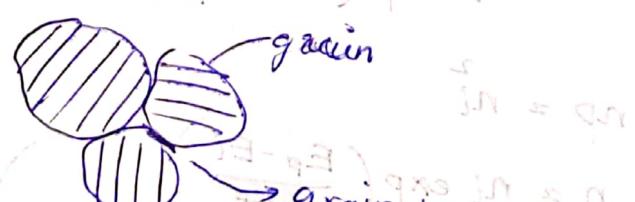
$$P = \frac{1}{2} \left[(N_A^- + N_D^+) + \sqrt{(N_A^- - N_D^+) + 4n_i^2} \right]$$

$$U = \frac{np - ni^2}{2 \left[p + n + 2ni \cosh \left(\frac{E_T - E_i}{kT} \right) \right]}$$

- 20/8
- Elements with high electronegativity are prone to getting oxidized
eg: Al, Si



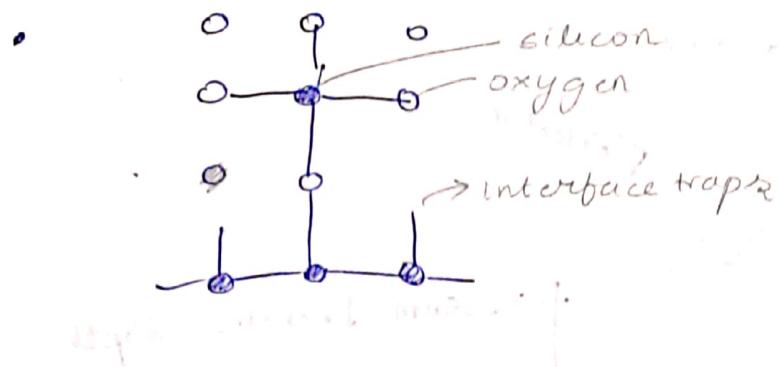
- Amorphous: no order present in structure
⇒ at interface no strain present
when we try to bring 2 material together



not ordered (Path for leakage current)

- Materials with high melting points have lower dielectric constant

- Atomically sharp \rightarrow no intermixing

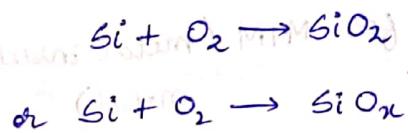


- Dry oxidation only used for ultra-thin oxide formation. electrically quality really good
- wet oxidation
 - faster
 - thicker oxide
 - quality not good (breakdown voltage not high)

\hookrightarrow dielectric const
 \hookrightarrow breakdown voltage

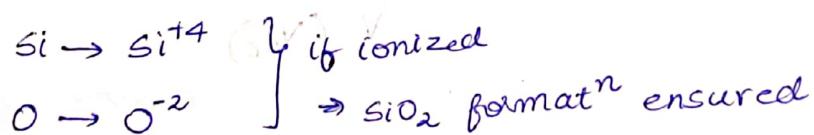


22/8

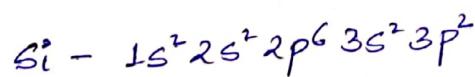


$$1 < n < 2$$

Y Pressure of
oxygen +
temp controlled



X-Ray Photoelectron Spectroscopy



core level e^-

$$E_i - E(e) = E_B(e)$$

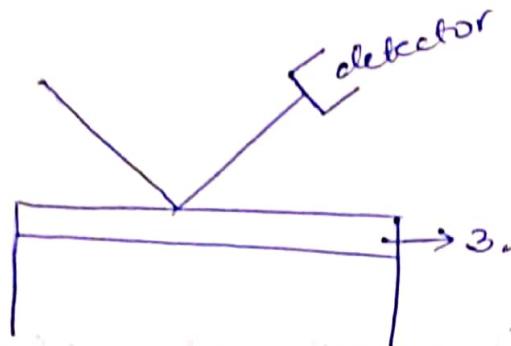
\hookrightarrow binding energy

if e^- comes from ion than atom, its binding energy will be higher

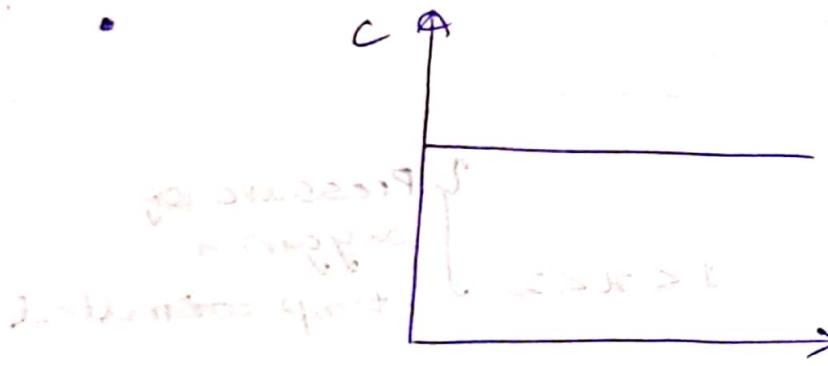
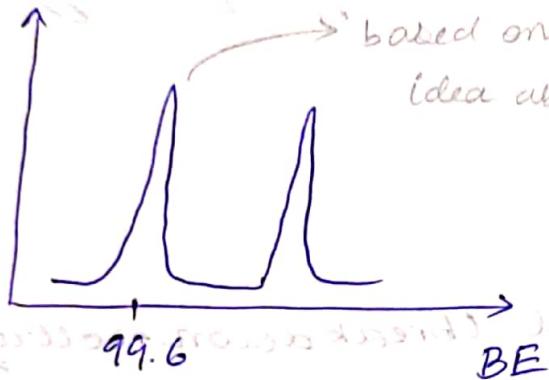
$$Si \ 2p \Rightarrow 99.6 \text{ eV}$$

$$Si^{+4} \ 2p \Rightarrow 104.2 \text{ eV}$$

$$Si^{+3} \ 2p \Rightarrow 102.5 \text{ eV}$$



Int

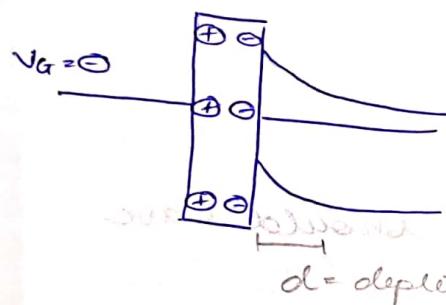
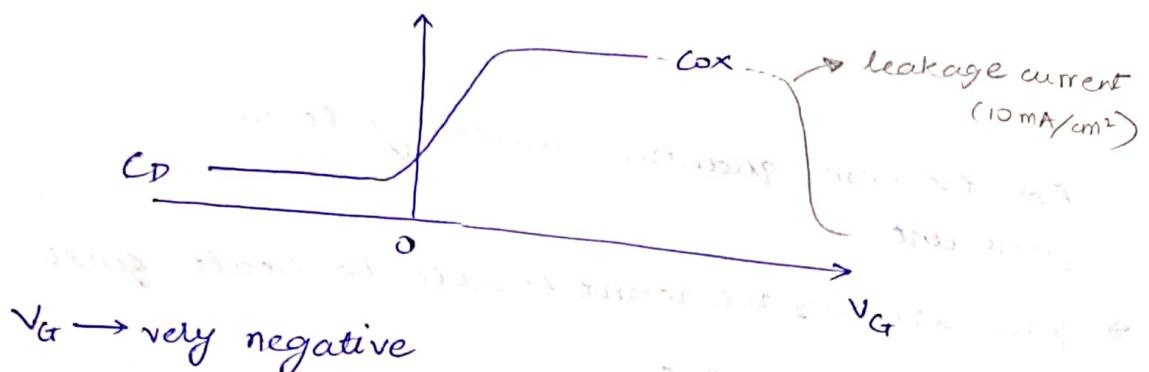


for MIM (metal insulator metal)

To measure capacitance we need to have an AC voltage riding on the bias



$$\frac{1}{C_{\text{Meas}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{Dep}}}$$



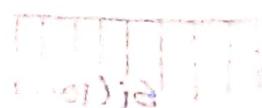
$$C_D = \frac{\epsilon_{Si} \epsilon_0}{d}$$

as V_G becomes more negative, $d \uparrow \Rightarrow C_D \downarrow$
 $\Rightarrow C_{\text{Meas}} \downarrow$ (from $C_{\text{Meas}} = C_{\text{ox}} + C_D$)

$$C_{\text{Meas}} \approx C_D$$

For $V_G = 1 \text{ V}$, $E = \frac{1}{10^{-8}} = 100 \text{ MV/m}$
 (for small thickness)

$$\frac{\phi_{MS}}{e} \pm \frac{Q_i}{C_{\text{ox}}} \pm \frac{Q_f}{C_{\text{ox}}} = V_{FB}$$



For $d < 2\text{nm}$, quantum tunneling becomes prevalent.

⇒ If we use SiO_2 we won't be able to scale further
so we need to ↑ ϵ_x

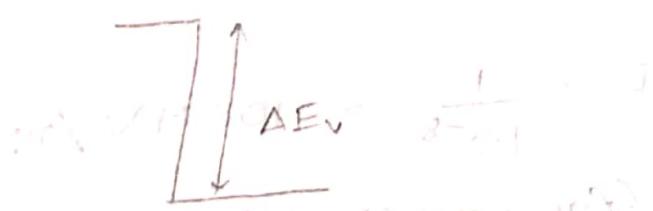
or at A↑, $\frac{\epsilon_r}{d} \uparrow$

Need $\epsilon_x > \epsilon_{\text{SiO}_2} = 3.9$

Thus our new material should have

- 1) ϵ_x large
- 2) High bandgap (\Rightarrow good insulator)
- 3) High thermal stability
- 4) good interface (\Rightarrow less traps)
- 5) Band offset (more important than BG)

$\sqrt{\Delta E_C}$ } eff. BG for ϵ_x not large



Band offset : Difference in the E_C of 2 material /

E_V of 2 material

Si and Si_{Ge}

SiGe: low BG \Rightarrow larger lattice const.
 $a_{\text{Ge}} \Rightarrow a_{\text{SiGe}} > a_{\text{Si}}$

\hookrightarrow decided by composition of Si & Ge

most of the stress/strain felt by SiGe

SiGe \rightarrow feels compressive strain

\Rightarrow as strain felt, the curvature of E-K diagram changes

\Rightarrow mobility changes

\Rightarrow \uparrow mobility (\leftarrow try for this cond?)

Equivalent Oxide Thickness (EOT)

$$C_{\text{HK}} = \frac{\epsilon_{\text{HK}} \epsilon_0 A}{d_{\text{HK}}} \approx \frac{\epsilon_{\text{SiO}_2} \epsilon_0 A}{d_{\text{SiO}_2}}$$

$$\Rightarrow \frac{\epsilon_{\text{HK}}}{d_{\text{HK}}} = \frac{\epsilon_{\text{SiO}_2}}{d_{\text{SiO}_2}}$$

$$d_{\text{SiO}_2} = \frac{\epsilon_{\text{HK}}}{\epsilon_{\text{SiO}_2}} \cdot d_{\text{HK}}$$

as we change this
we scale the EOT

\rightarrow also called 'Capacitance Equivalent Thickness' (CET)

\rightarrow By \uparrow thickness, we reduce leakage current
(due to tunneling)

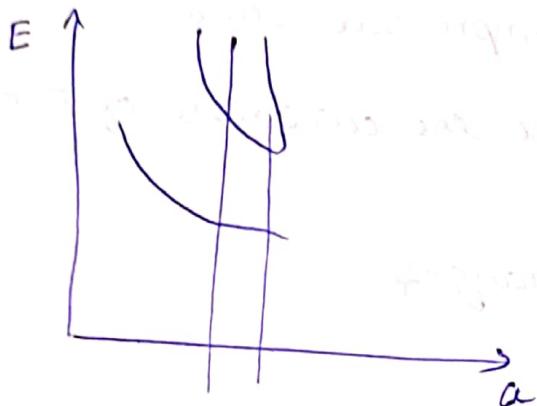
$$E_G \quad d \quad \frac{1}{a \text{ (lattice const.)}}$$

Band Gap

$$\text{eg: } E_{G,\text{ci}} = 1.1 \text{ eV}$$

$$E_{G,\text{ge}} = 0.42 \text{ eV}$$

$$\frac{a_{\text{Ge}} - a_{\text{Si}}}{a_{\text{Si}}} = 4\%$$



E_G smaller here

- Dipole moment $\approx e.d$ if atoms loosely packaged
 d high
- \Rightarrow small $a \Rightarrow$ high dipole moment \Rightarrow high E_G
- Make sure that no reacln occurs at the surface while growing

$$t_{\text{eq}} = \left[\frac{E_{\text{F102}}}{E_{\text{F10-K}}} \right] t_{\text{low-K}} + \left[\frac{E_{\text{F102}}}{E_{\text{F1high-K}}} \right] t_{\text{high-K}}$$

limits the t_{eq} regardless of how high $E_{\text{F1high-K}}$ is

- we get flatband when difference of workfunction is compensated

29/08 SOI : reduce active area

- Standby current becomes min^m
- on-current however reduced

- as para. cap reduces we can increase speed
- antenna \rightarrow radiation
(due to oscillation)
- epitaxy \rightarrow grow single crystal.

\rightarrow annealing ensures we get single crystal easily at high temp

\rightarrow std. plane of Sapphire is $\langle 0001 \rangle$ \rightarrow hexagonal which won't align with Si(100)

- Smart Cut Method

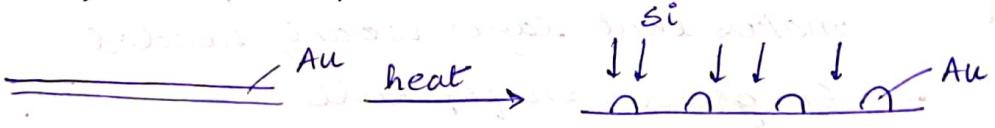
- deposit oxygen on Si
- H₂ implantation (it's density peaks underneath) makes that layer weakly bonded

- Si growth on flip side
 \rightarrow on annealing, the H₂ layer easily breaks
orientation maintained since it is cut parallel to wafer orientation

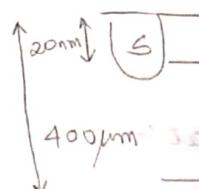
- SiO₂ \rightarrow amorphous (doesn't has exact alignment with structure of Si)

Gd₂O₃ \rightarrow crystalline struct. (struct. coherence with Si)

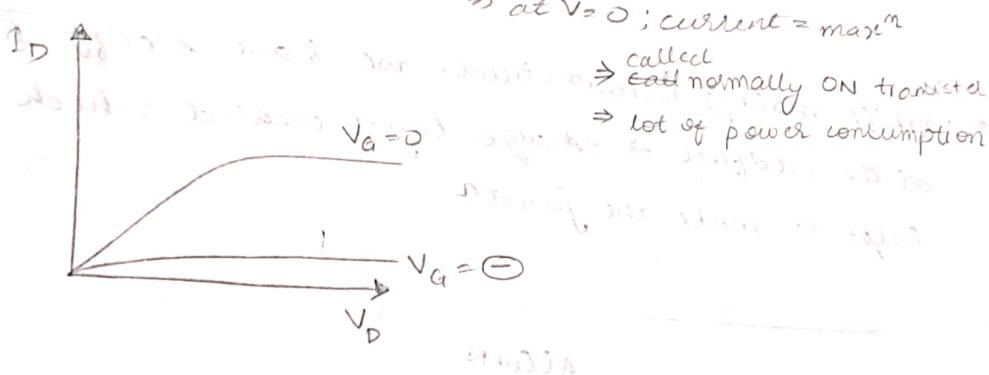
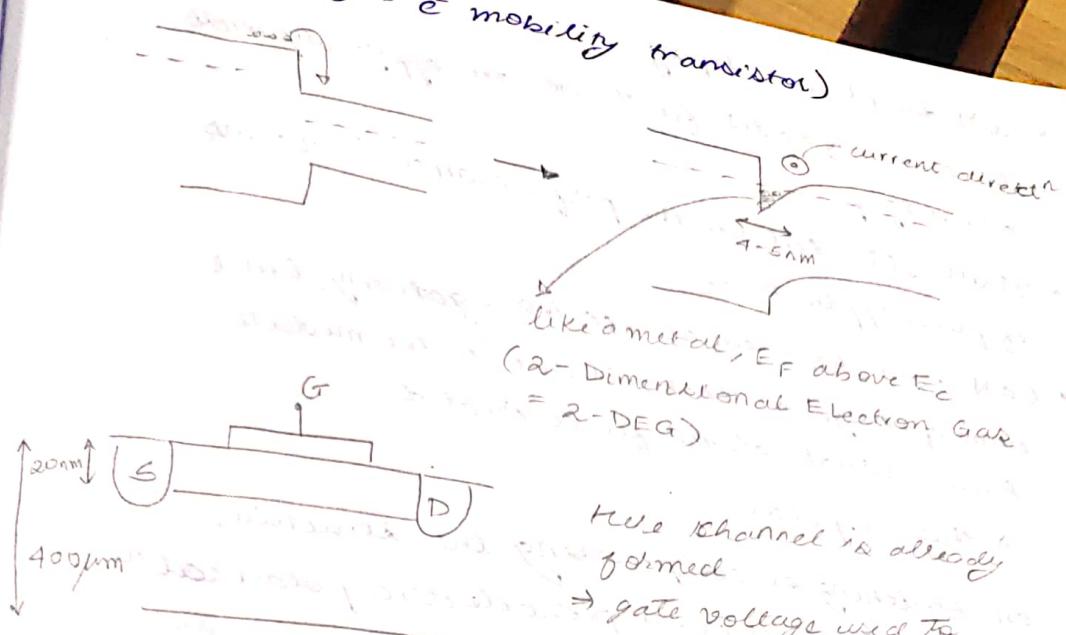
- 05/09
- In SOI, carrier generated through impact ionization
 - gate on both sides gives a greater control over channel
 - Double-gate
 - planar - difficult to fabricate bottom gate
 - fin - quantum mechanically controlled (4-5nm Silicon channel)
 - energy levels for carriers to stay is limited \Rightarrow quantum confinement
 - while making source drain we need to anneal at high temp; the High-K gate can't withstand high temp
 \Rightarrow soln: make gate afterwards

- VLS growth (Vapour Liquid Solid)
- Diagram: 
- gold nanowires grow at the gold nanoparticle
- (conditions like - at some composition melting point reached
- then Au + Si melt together - as Si. T, it melting point \Rightarrow it solidifies
- then Au float, and nanowire formed

• HEMT (High Electron Mobility Transistor)



- HEMT (high μ mobility transistor)



- since carrier not going through bulk, resistance is very low \Rightarrow high mobility (only interface)

05/09



2-DEG

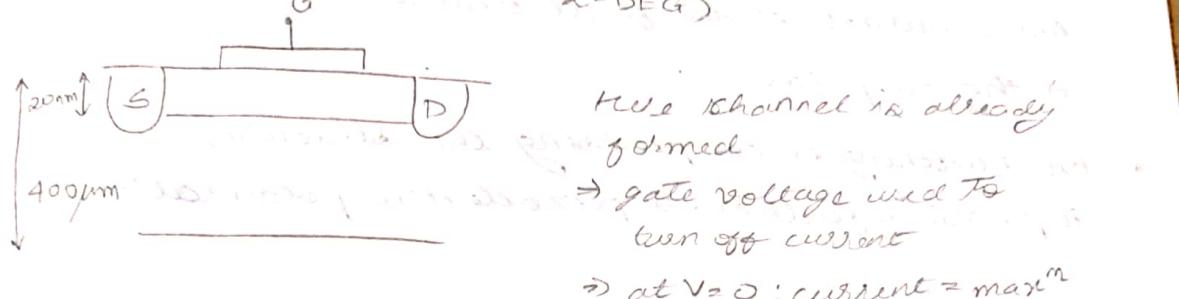
\hookrightarrow goes coz or follows Boltzmann statistics

- Tunneling possible in HEMT, however we don't need to apply high bias for operation

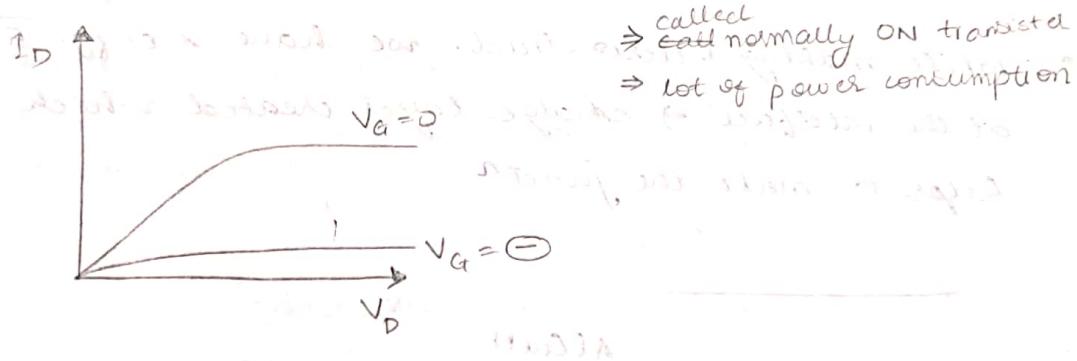
- HEMT (high μ mobility transistor)

band diagram: like a metal, E_F above E_C

2-DEG = (2-Dimensional Electron Gas) = 2-DEG



→ gate voltage used to turn off current
→ at $V_G = 0$; current = maxⁿ



- since carrier not going through bulk, resistance is very low \Rightarrow high mobility

(only interface)



2-DEG

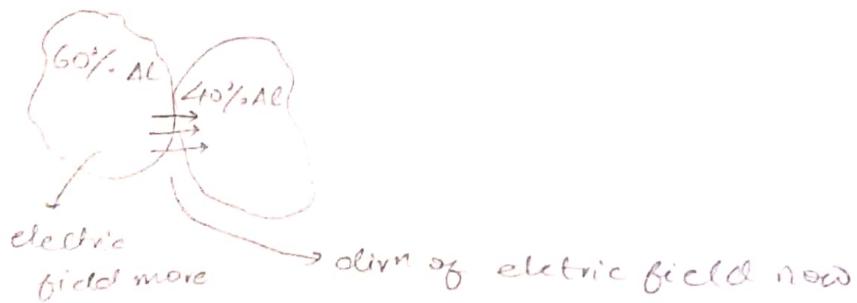
↳ goes coz or follow Boltzmann statistics

- Tunneling possible in HEMT, however we don't need to apply high bias for operation

- GaN doesn't need doping
- The amount of electric field we can apply depends on bandgap
- BFOM, JFM tell us the performance in terms of power applications
- GaN don't have equal electronegativity, hence centre of charge in the bond isn't in the middle, hence internal electric field created
→ they are polar
- on stretching or compressing the structure, it polarizes further → piezoelectric polarization
→ spontaneous polarization
- while making heterostruct. we have 2 diff. E at the interface → charge layer created which helps to make the junction
they come from surface (most) and anywhere else
mobile only along the layer
- AlGaN → should be very thin.

GaN

→ doesn't face piezo... polarization cos its width is thicker in comparison; acts as virtual substrate



- Better n
→ large e
→ Recr.
- ac

12/09 To n

23/09 []

- Better mobility = better switching speed
 - large EG material form shottky metal contact
 - Recrystallization

22/09

- To improve resolution, aperture becomes narrow so depth of focus reduces
- acetone evaporates on high vapor pressure hence it may evaporate before dissolving all the PR and is not always recommended

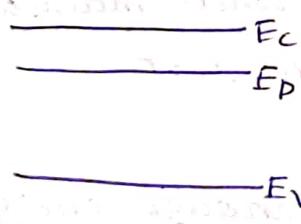
23/09

[Book: chap 7]

- Series resistance (due to mos interface) adds to delay.
- Doping: done through conc. difference
 - difficult to control depth (not sharp)
 - we do ion implantation now
 - before this we need to create vacancies all the while maintaining the uniformity of substrate
 - ⇒ temp imp.
 - giving dopant enough energy to diffuse w/o destroying crystal
 - "thermal budget" imp.
- The substrate atom shouldn't be too large (dopants feel more resistance) or too small (dopants can fit in anywhere)
 - we need substitutional replacement otherwise carriers not released

- $n = N_0 \exp \left[-\frac{E_C - E_F}{kT} \right]$ \rightarrow exp. temp. dependence
- Epitaxy: growing single crystal material on single crystal substrate \rightarrow Doped Epitaxial Layer
- Background doping decided by temperature and bandgap
- Beyond a certain temp. solid solubility \downarrow .
 - \rightarrow Avogadro number $= 10^{23}$
 - \rightarrow limit to solubility $\sim 10^{21}$
 - \rightarrow if working with large temp, choose high temp stable and soluble dopant
 - \rightarrow Phosphorous not a good dopant (in general)

24/09

- $N_A \neq P$ } for conc. of dopants
 $N_D \neq n$ } (~ 1 order difference)
- $d \downarrow$  if $d = 20 \text{ meV}$
 \rightarrow all dopant atoms are activated
- Sheet resistance - very thin layer

$$R_S = \frac{s}{n_j} \quad (\text{for square contact})$$

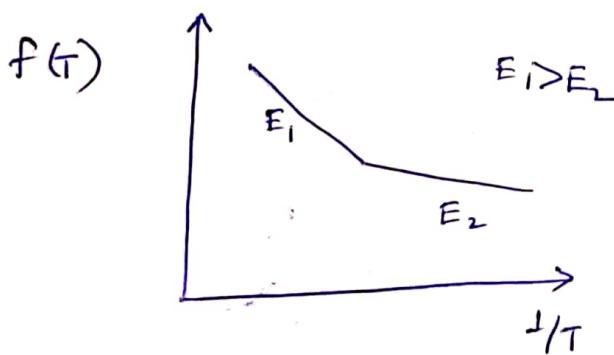
- Thermal velocity $\sim 10^7 \text{ cm/sec}$
 But thermal velocity is random
 \Rightarrow Drift velocity (due to electric field) leads to current ultimately

- $\sigma = q \left(n_{un} + p_{up} \right)$
- $\rightarrow \frac{\mu E}{cm^2 N sec}$
- becomes + since we consider the direction of $\frac{D_n}{E_n}$
- $\mu_n = \frac{v_{nun}}{E_n} \rightarrow$ dependence on material

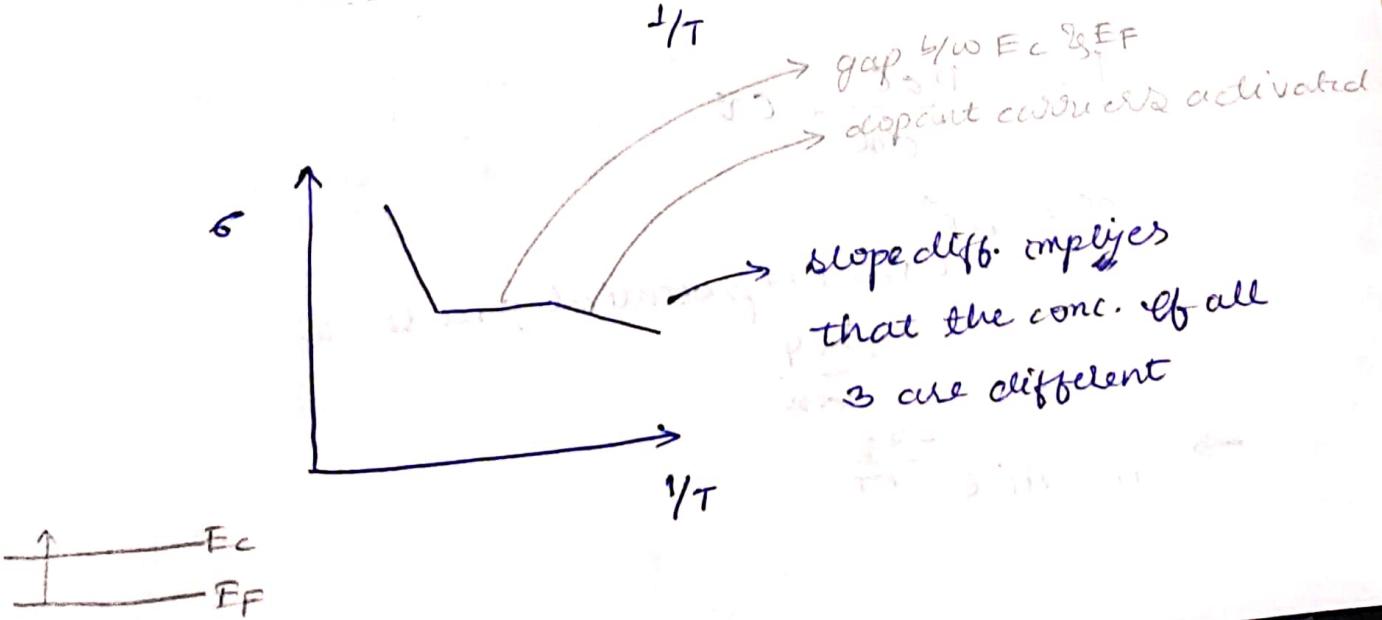
- $R_s = \frac{g}{n_j} = \frac{1}{\sigma n_j} = \frac{1}{q \mu n_j} = \frac{1}{q \mu_0}$
- As : $D^0 = 9.17 \Rightarrow$ slightly diffusive

24/09 • Hopping flag, $P_i = v_0 \exp \left(-\frac{E_i}{kT} \right)$ depends on material

→ as particle diffuses in crystal material it faces a periodic potential

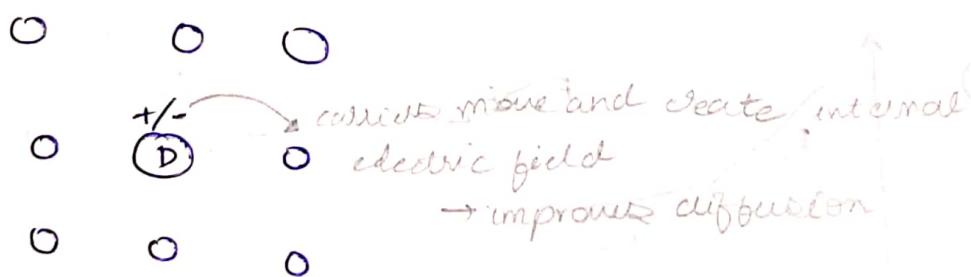


low slope
activation energy
is less



- 01/10
- at low temp we can excite the dopant carriers
 - Cu has high diffusion coefficient hence it is a major contaminant and needs to be taken care of
 - Vacancy = binding energy of Si to surrounding atoms
 - $\frac{N_v}{N} = \exp\left(\frac{-E_{vac}}{KT}\right)$
 - for small bandgap materials binding energy is less
 - $P_v = \exp\left(\frac{-E_{vac}}{KT}\right) \cdot v_0 \exp\left(\frac{-E_s}{KT}\right)$

v_0
creation of vacancies
energy for substitution of impurity
 - Ficks law valid only for low doping.



$$F = -D \frac{dc}{dx} + Cv \quad \begin{matrix} \rightarrow \\ \text{drift velocity due to diffusion} \end{matrix}$$

$$v = \mu E \quad \begin{matrix} \rightarrow \\ \text{due to potential gradient} \end{matrix}$$

$$= -\frac{d\psi}{dx}$$

$$\rightarrow n = n_i e^{-\frac{4q}{KT}}$$

(16)

02/10

Thin Film

d (thickness) =

e.g. of thin films: $300\text{ nm} - 3\mu\text{m}$

PR, Gate oxide, oxide, metal oxide
(PVD)

Requirement for thin film: want pure metal

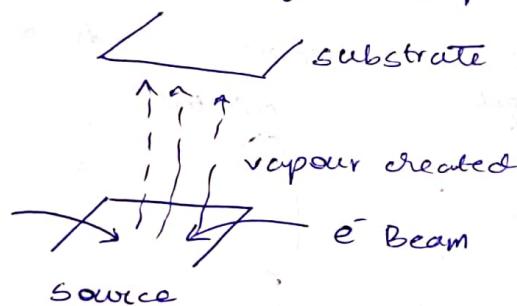
a) substrate

b) sources

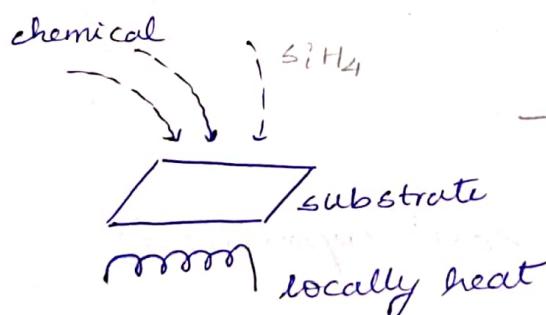
→ (i.e. Physical Vapour Deposition (PVD))

→ chemical vapour deposit (CVD)

{ Generating vapour for PVD:

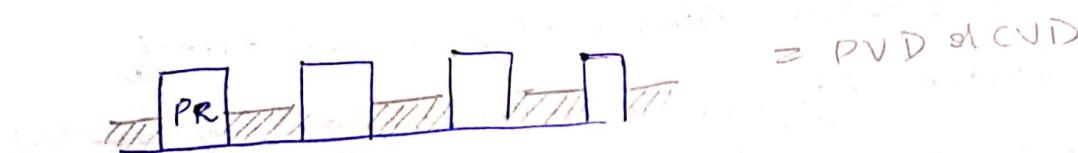


CVD:



chemical: in compound form
— called 'Precursor'

- If deposition is over



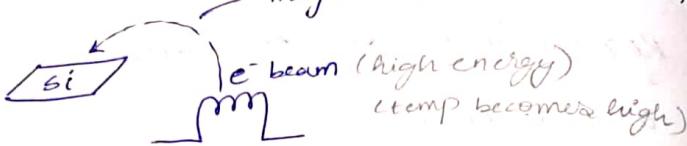
- PVD = sputtering

- PVD techniques

→ thermal evaporation

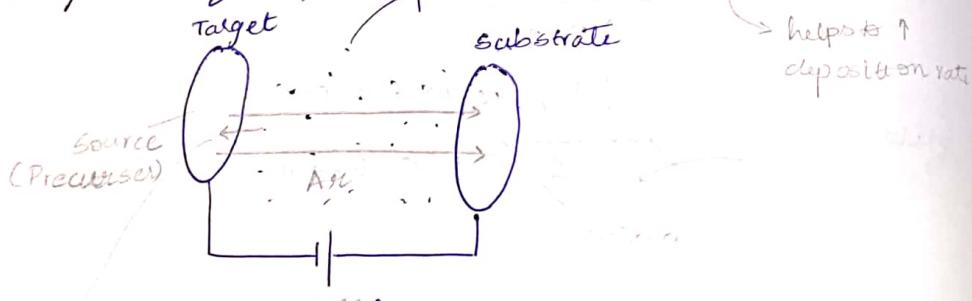
→ e-beam evaporation (better) (typ. used)

magnetic field bends it 270°



e-beam raised the temperature. It might hardens the PR. So in that case we use thermal evaporation

→ sputtering (typ. used)



heavy atom hit the target due to beam which releases source atoms that deposit on substrate

→ PLD (Pulse Laser Deposition)

- PVD needs vacuum, however CVD has no such req. mandatory
- Precursor present in liquid form so we need gaseous collid. Can't heat precursor directly otherwise they give uncontrolled gas expansion and might react before reaching substrate at such high temp.

03/10

- CVD class conditions

- atm

- low P (LPCVD)

- ultra (CVD)

common today

- MOCVD
metal org

- LPCVD

- pre

it

- co

• 96

- b) v • CVD classification based on operating conditions:

- atmospheric pressure
- low pressure (all reactions on substrate)
(LPCVD)
- ultra high vacuum (used to grow the LEDs)
(UHV CVD) HBD

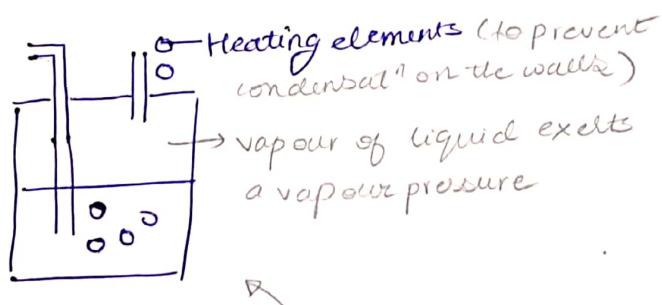
common today Low pressure \Rightarrow pure environment

• MOCVD

metal organic

• LPCVD

- prefer the precursor to be liquid so that it doesn't touch the reactor
- carrier gases (inert) when introduced in liquid form a bubble



$$\ln \frac{P}{P_0} = \frac{V}{RT} (P - P_0)$$

- very low VP \Rightarrow can't evaporate
very high VP \Rightarrow unstable and reacts with neighbours
- shower head reactor \rightarrow only one wafer at a time
- If we get powdered output \Rightarrow too much turbulence on wafer