Welcome to

EE669: VLSI Technology

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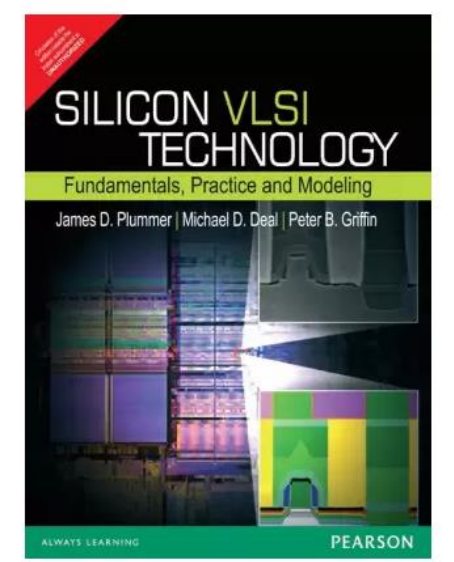
Office hour: Friday 10:00 – 11.00 AM, EE Annex, Room: 104

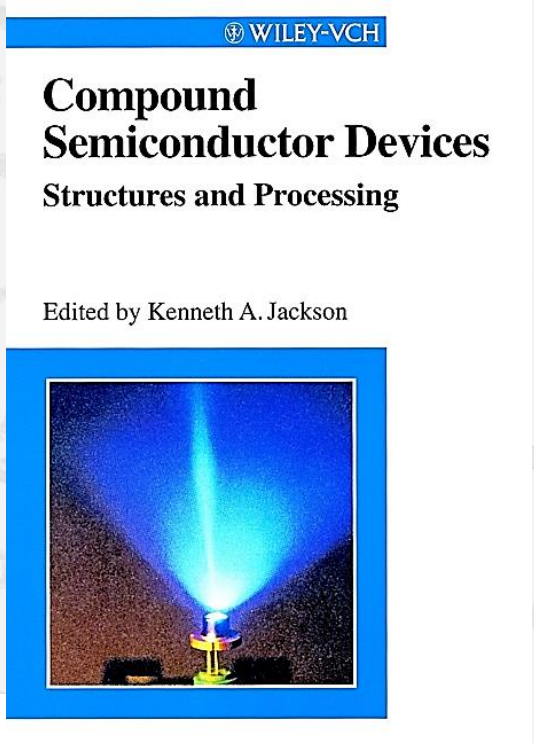
Important: Grading

- Midsem: 35%
- Endsem: 40%
- Quizzes:15% (Best 6 out of 8)
- Assignments: 5%
- Attendance: 5%

Please add your name in Moodle, IITB

References





Springer Series in Materials Science

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Gallium Nitride Electronics

Authors: **Quay**, Rüdiger

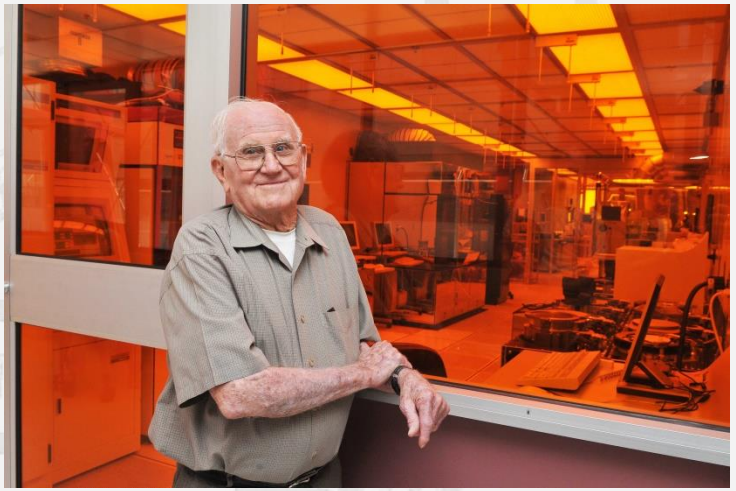
Course content: Official description

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques. Impurity incorporation: Solid State diffusion modeling and technology, Ion Implantation modeling, technology and damage annealing, characterization of Impurity profiles. Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI, Characterization of oxide films, High k and low k dielectrics for ULSI. Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation. Chemical Vapor Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films, Epitaxial growth of silicon, modelling and technology. Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects, Multi-level metallization schemes. Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques, RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits, Advanced MOS technologies.

Clean room: Who invented

1962, Willis Whitfield @ Sandia Lab

Sandia Lab, USA: When Willis Whitfield invented the laminar-flow cleanroom 50 years ago, researchers and industrialists didn't believe it at first. But within a few short years, $50 billion worth of laminar-flow cleanrooms were being built worldwide and the invention is still in use today.



50 years later at Sandia Lab

Clean room: **A controlled environment used for scientific research or for manufacturing of ICs.**

- **Protect from pollutants such as dust, chemical vapors etc.**
- **Controls the airborne particles in a specified limit based upon its specifications**
- **The contamination by people, fluids, tools, etc**

How do we control the environment?

- Flow rates of air, direction of flow, temperature humidity, and filtration
- It is filtered using an air filter HEPA (High Efficiency Particulate Arrestance).
- It can remove 99.97% of particles having a size of 0.3 micrometer
- **ULPA (Ultra Low Particulate Air)** can remove 99.99% of particles such as dust, bacteria etc having a size of 0.1 micrometer.

Environment for VLSI Technology: Clean room and safety requirements

What is a Clean Room?

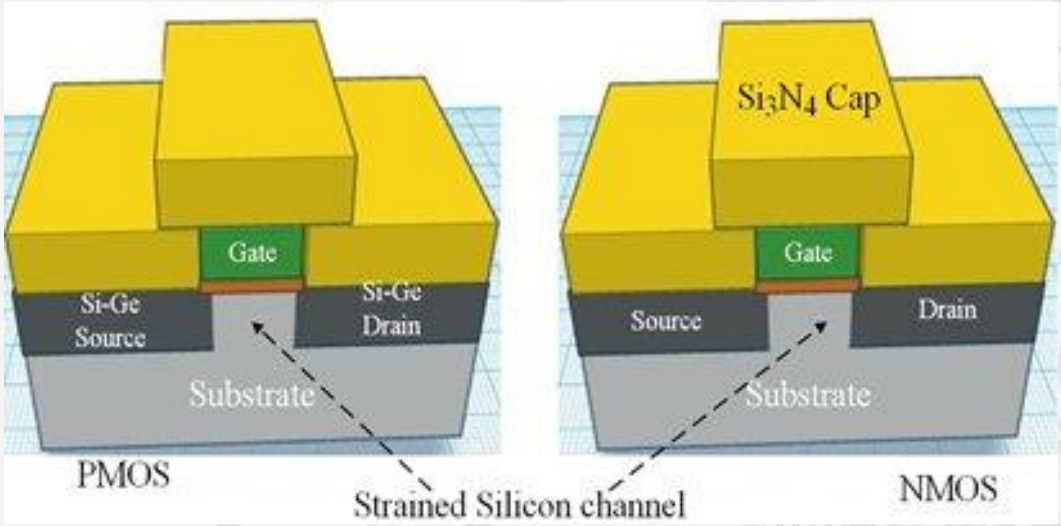
	≥0.1 µm	≥0.2 µm	≥0.3 µm	≥0.5 µm	≥1 µm	≥5 µm	
ISO 3	1,000	237	102	35[b]	[d]	[e]	Class 1
ISO 4	10,000	2,370	1,020	352	83[b]	[e]	Class 10
ISO 5	100,000	23,700	10,200	3,520	832	[d,e,f]	Class 100
ISO 6	1,000,000	237,000	102,000	35,200	8,320	293	Class 1,000
ISO 7	[c]	[c]	[c]	352,000	83,200	2,930	Class 10,000
ISO 8	[c]	[c]	[c]	3,520,000	832,000	29,300	Class 100,000

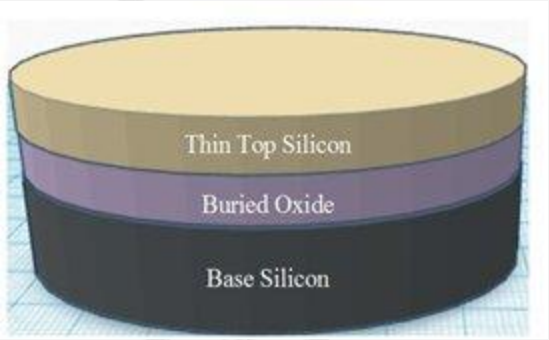
Source: https://en.wikipedia.org/wiki/Cleanroom

Entry to the clean room

- The person must pass through air showers before entering the room in order to clear off the dust particles from bodies.
- Air showers are specialized antechambers which spray wind speed about 25m/s or above via stainless steel nozzles.

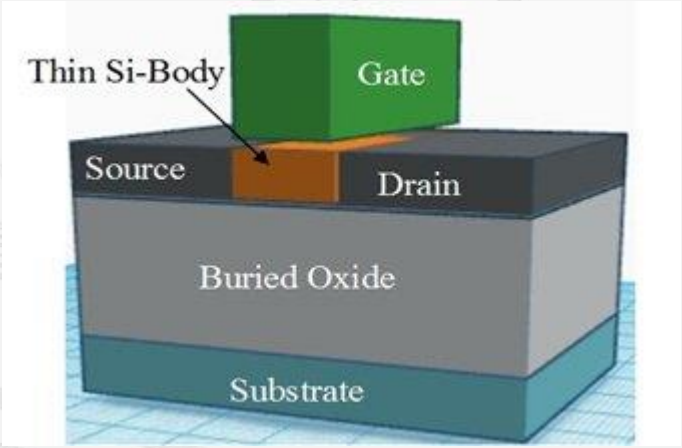
Example of Si and Compound semiconductor Devices

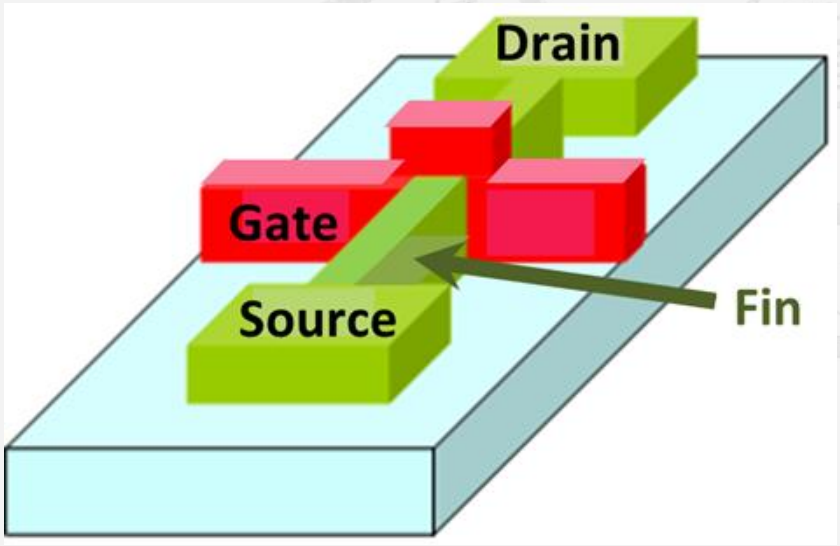




SOI Wafer

PMOS: Uniaxial Compressive Strain b) NMOS: Uniaxial Tensile Strain





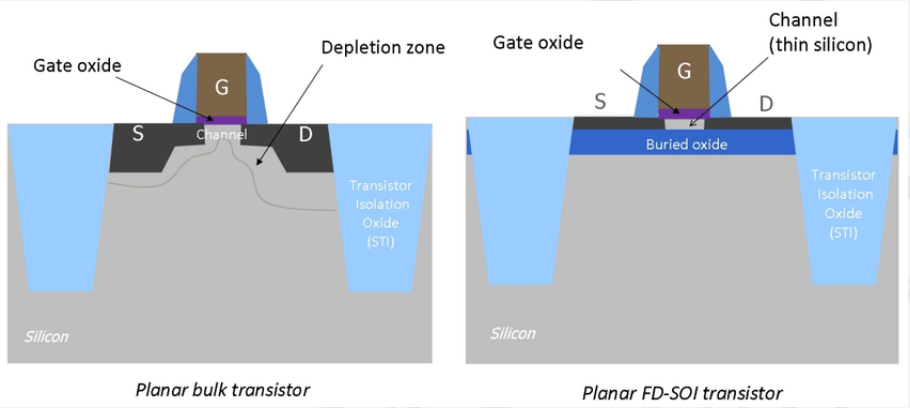
Structure of SOI FET

Process steps:

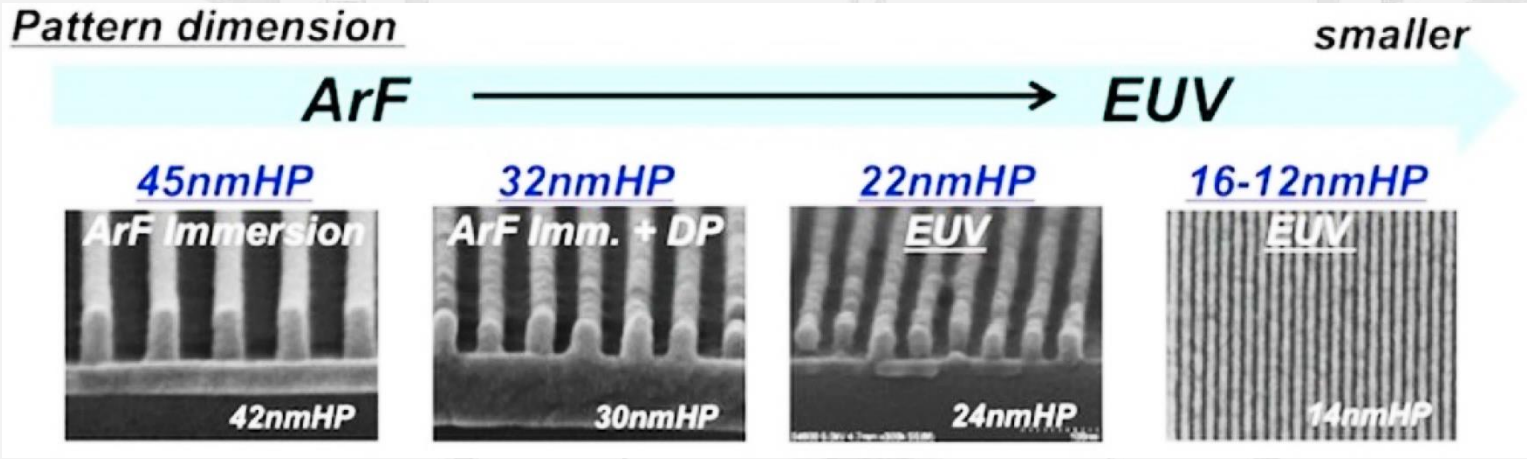
- Fin patterning vs. planar active region patterning
- Oxide filling, planarization, and recessing
- Doping to form well isolation
- Gate oxide growth, and dummy gate deposition, planarization and patterning
- Doping to form S/D extentions
- Spacer deposition and patterning
- Epitaxy forming S/D regions (embedded SiGe and raised Si)
- ILD0& CMP
- Dummy gate removal
- Replacement of high-k & metal gate stack
- Self-aligned contact formation
- Back end of line

Radamson, H.H.; Zhang, Y.B.; He, X.B.; Cui, H.S.; Li, J.J.; Xiang, J.J.; Liu, J.B.; Gu, S.H.; Wang, G.L. The Challenges of Advanced CMOS Process from 2D to 3D. Appl. Sci. **2017**, 7, 1047

Classical vs to Today's high performing

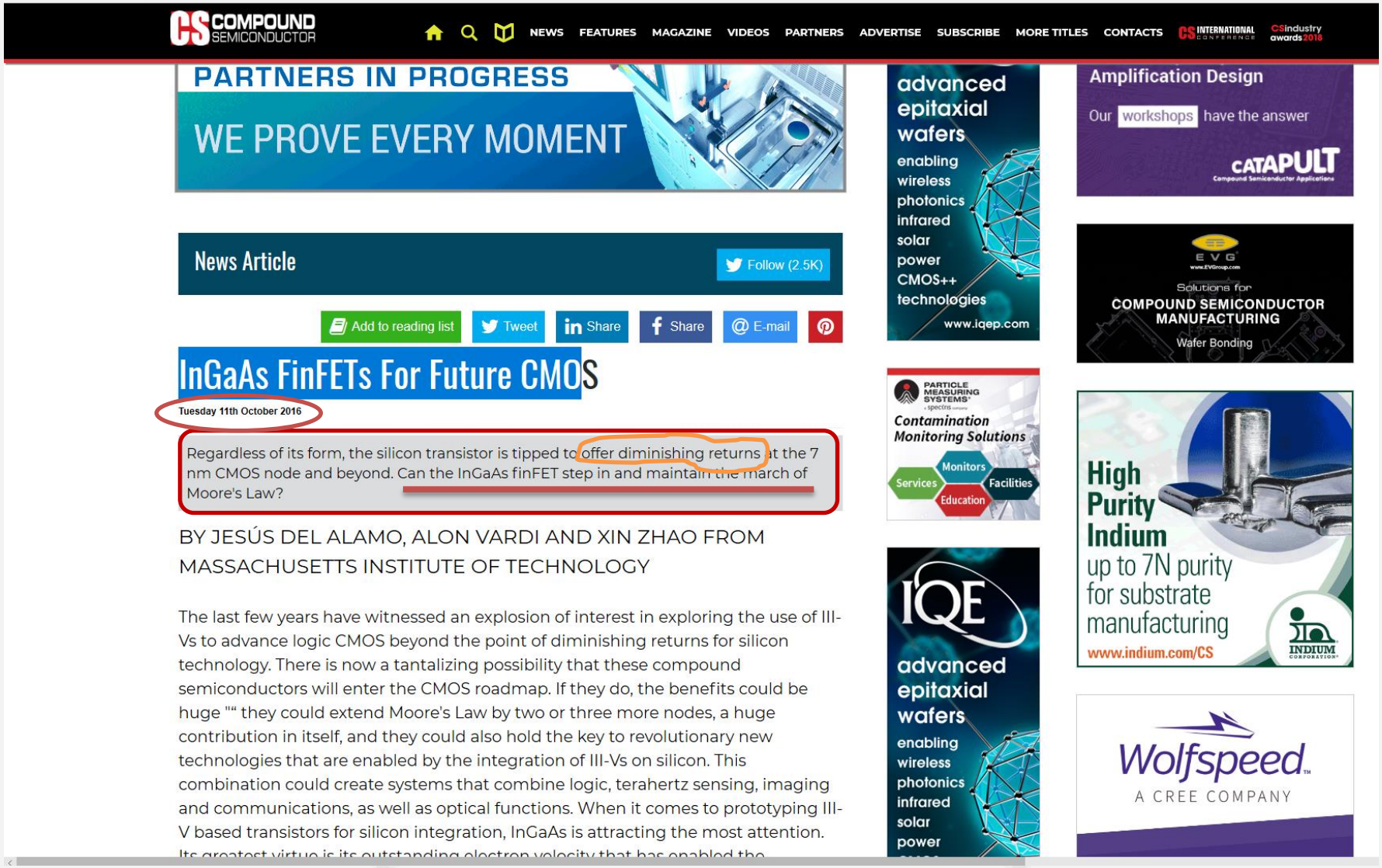


Evolution of the lithography technique where the pattern becomes denser and smaller in each new technology node

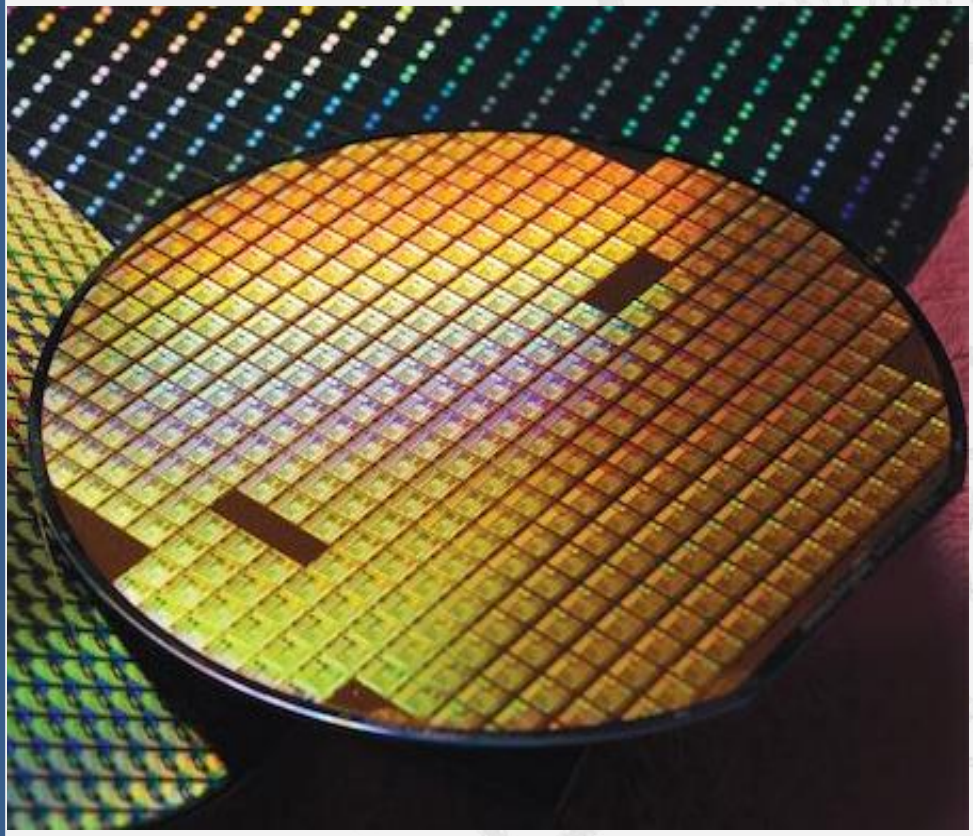


To prevent pattern collapse, the thickness of resist is reduced proportionally to the minimum half-pitch (HP) of lines/spaces.

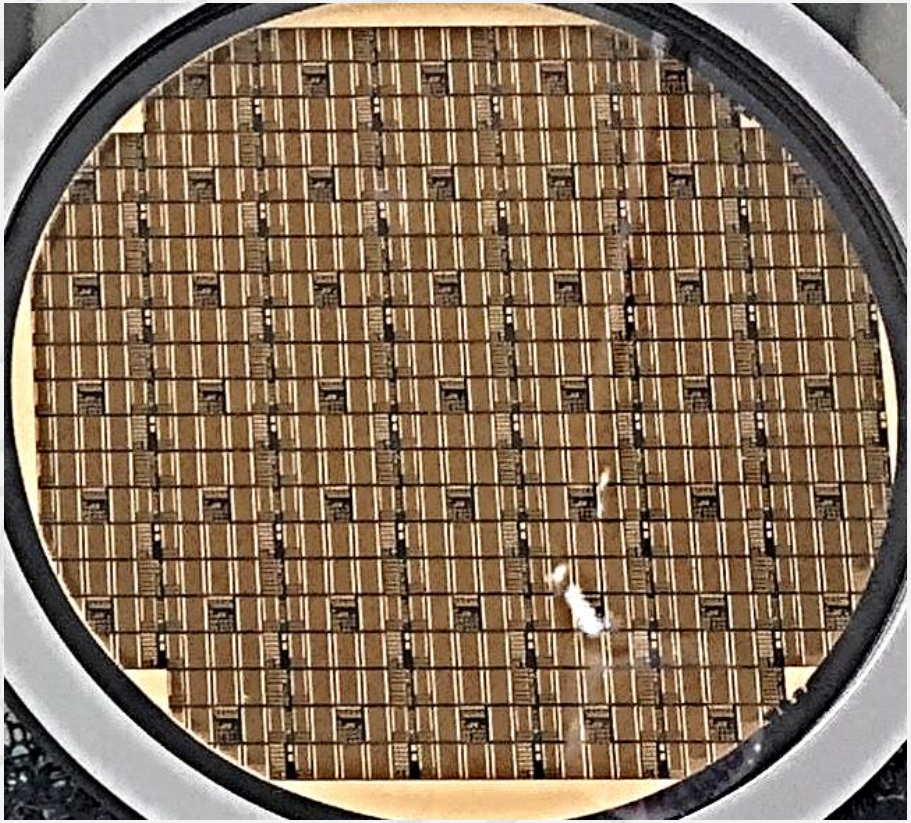
VLSI: What is it today?



Si vs. Compound Semiconductor Devices



TSMC 7nm node Chip on 12” Si



600V Normally OFF GaN power transistor on 4” Si wafer

See you Thursday