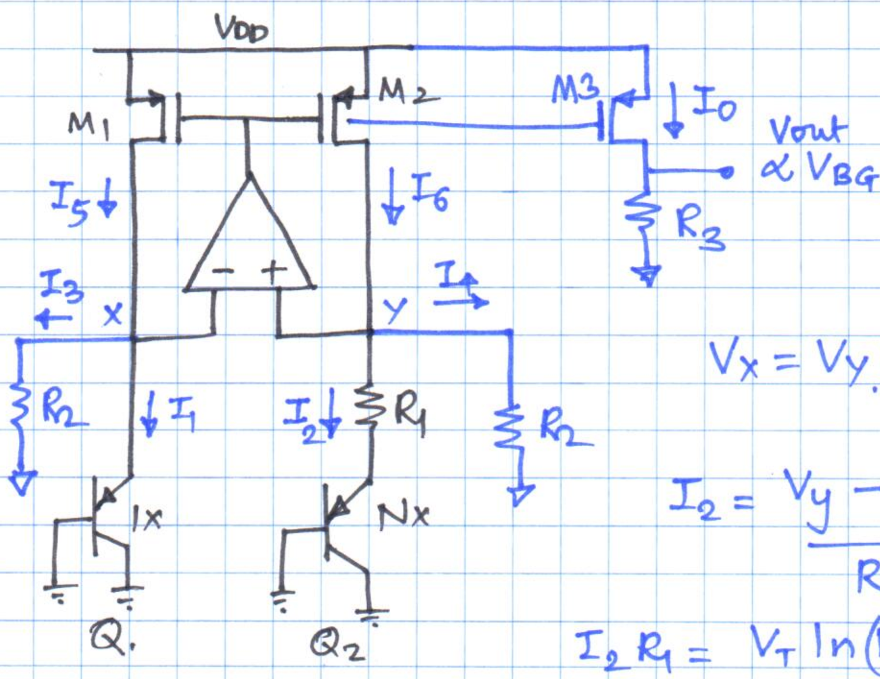
Since $V_{REF} \cong 1.25V$ $V_{DD} > 1.25V$.

What about V_{REF} for $V_{DD} < 1V$.?

Reference

H. Banba "CMOS BGAP REF with sub-1-V op"
JSSC NOV 1997.



$V_X = V_Y$ due to fbk (OPAMP)

$$I_2 = \frac{V_y - |V_{BE_2}|}{R_1} = \frac{|V_{BE_1}| - |V_{BE_2}|}{R_1}$$

$$I_2 R_1 = V_T \ln(N) \quad \text{—— (1)}$$

Also $I_3 = I_4 = \dfrac{V_{BE_1}}{R_2}$

$$I_6 = I_2 + I_4 = \frac{V_T \ln N}{R_1} + \frac{|V_{BE_1}|}{R_2} = \frac{1}{R_2}\left(|V_{BE_1}| + V_T \ln N \left(\frac{R_2}{R_1}\right)\right)$$

By choosing $\dfrac{R_2}{R_1}$. term inside brackets $= V_{BG}$

$$I_6 = \frac{V_{BG}}{R_2}$$

$$I_O = \frac{V_{BG}}{R_2} \Rightarrow \boxed{V_{out} = \frac{R_3}{R_2} V_{BG}}$$

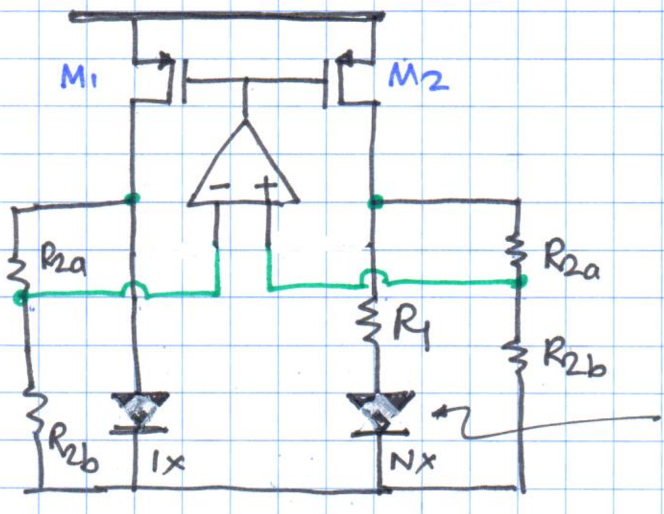
Keep $\dfrac{R_3}{R_2} < 1$ for $V_{DD} < 1V$

Issue with Banba Bgap.

Nodes X & Y DC voltage 0.7V — 0.9V ~

→ Input diff pair of opamp – Native NMOS ($V_T \simeq -0.2V$)

→ Leung / Mok solution | IEEE JSSC Apr. 2002
"A Sub-1-V 15-ppm/°C CMOS Bgap...



Lower common. mode i/p range of opamp using resistive divider.

V_{BE} junction shown as diode

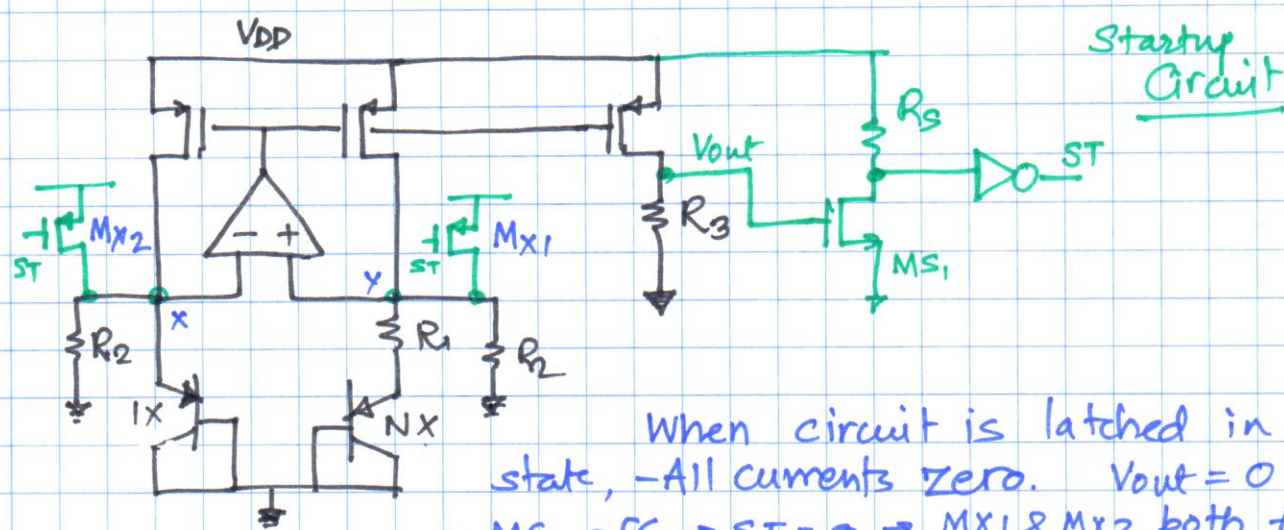
☆ Bandgap Startup Problem

→ Undesired stable solution. – All currents zero.

→ Can be observed when you ramp up power supply.

→ Startup circuit detects this condition & pumps in juice to get to desired operation point.

Startup Solution (one possible)

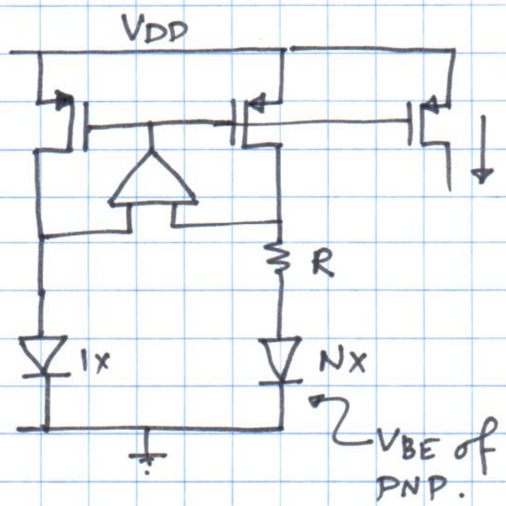


When circuit is latched in undesired state, - All currents zero. Vout = 0

→ MS_1 off → ST = 0 → MX1 & Mx2 both turn on

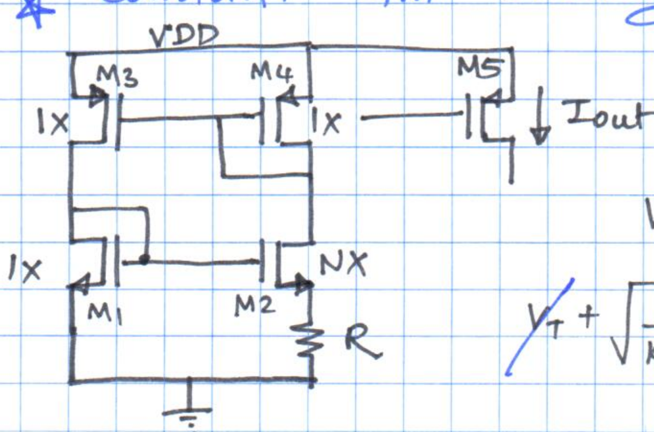
→ Lift both Nodes X & Y → opamp starts to work.

✱ PTAT Current source



$$I_{out} = \frac{V_T \ln(N)}{R}$$

✱ Constant Gm Biasing → Gm → PVT independent



$$V_{GS_1} = V_{GS_2} + IR$$

$$\cancel{V_T} + \sqrt{\frac{2I}{K_n (W/L)_1}} = \cancel{V_T} + \sqrt{\frac{2I}{K_n N \left(\frac{W}{L}\right)_1}} + IR$$

$$\Rightarrow I_{out} = I = \frac{2}{K_N\left(\frac{W}{L}\right)_1} \cdot \frac{1}{R^2} \cdot \left(1 - \frac{1}{\sqrt{N}}\right)^2$$

$$g_{m_1} = \sqrt{\underbrace{2\mu_n C_{ox}}_{K_N}\left(\frac{W}{L}\right)_1 I_1}$$

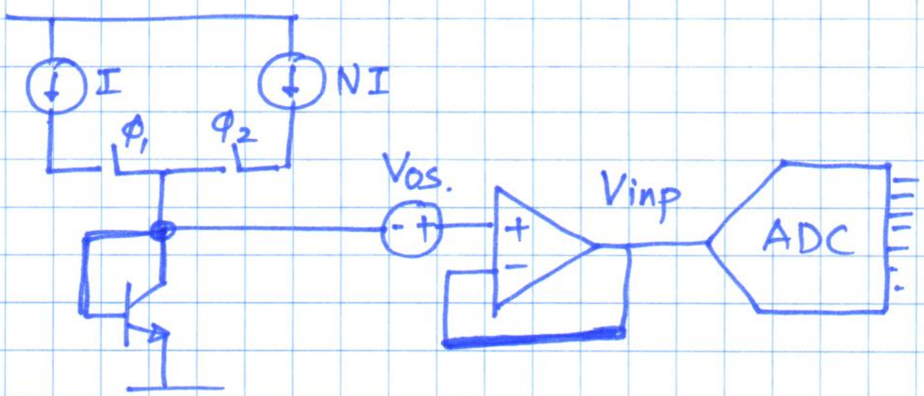
$$= \sqrt{2\,\cancel{\mu_n C_{ox}\left(\frac{W}{L}\right)_1} \times \frac{2}{\cancel{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}}\left(\frac{1}{R^2}\left(1-\frac{1}{\sqrt{N}}\right)^2\right)}$$

$$= \frac{2}{R}\left(1 - \frac{1}{\sqrt{N}}\right)$$

on-chip or off chip (R) — Scaler Ratio ($\sqrt{N}$)

→ can be tuned. digitally

* On-Chip Temperature Sensor



In ϕ_1 $V_{inp} = V_{os} + V_T \ln\left(\frac{I}{I_s}\right)$

In ϕ_2 $V_{inp} = V_{os} + V_T \ln\left(\frac{NI}{I_s}\right)$

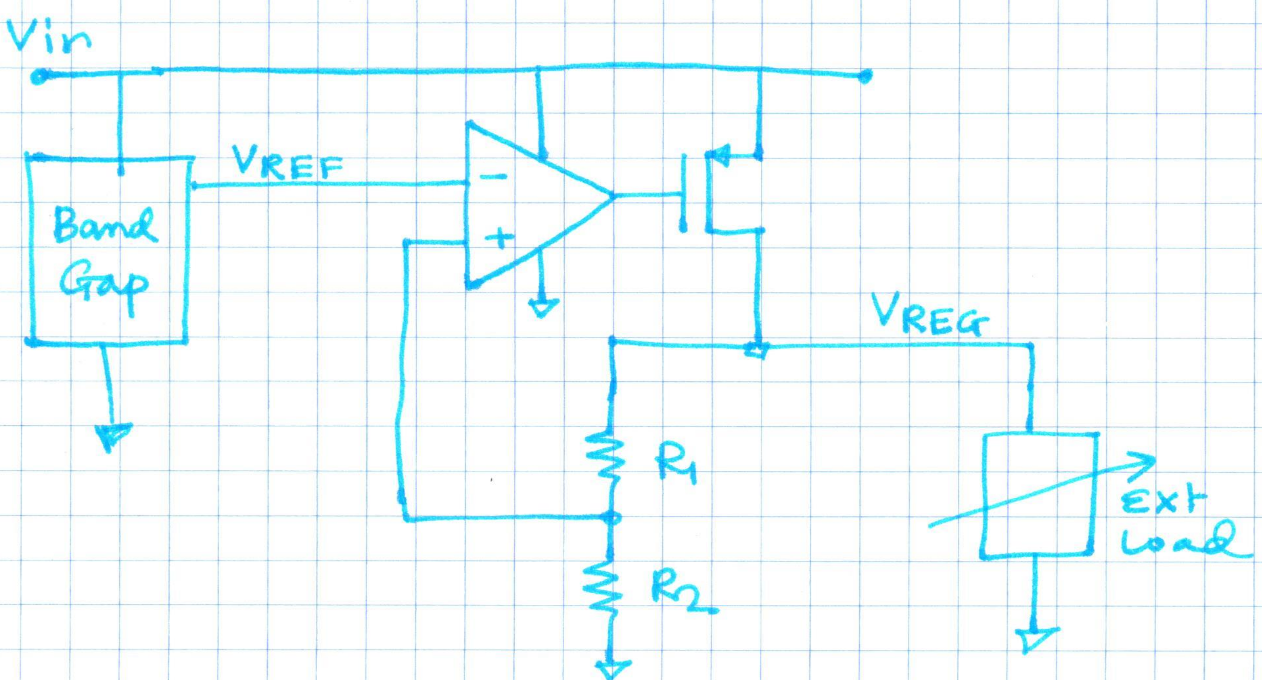
A 2D conversion & subtract digitally

Measure $V_T \ln(N)$ $\Rightarrow$ Give T in °K

Known Ratios

Voltage Regulator

→ is a constant voltage source independant of load current and input voltage.



→ V_{REF} – from Bandgap Reference. ~ 1.2V

→ Error Amplifier – OTA

→ Feedback Network

→ Pass Transistor – V_{SG} increases as I_L increas

PMOS – large. – should be able to carry desired max load current.

$$V_{REG} = \left(1 + \frac{R_1}{R_2}\right) V_{REF}$$