

EE618 (ZeLe)

CMOS Analog VLSI Design : Homework -3 (20- Marks)

Submission Deadline : 8th Sep 2019 11:55PM

- All problems are based on Cadence simulations
- The submission must contain appropriate plots labelled clearly.
- Submission must be in **Teamname_Rollnumber_Yourname_Assignment3.pdf** format.
- All MOSFET models should be used from SCL 180 nm library.
- Report all values preferably in tabular format wherever it is appropriate.
- Use unit finger width as a multiple of $0.5\mu\text{m}$ for all transistors
- Use $L = 0.18\mu\text{m}$ unless otherwise stated

Question 1

Note: First read the document uploaded to understand common mode sensing circuit implemented using R_C . Design a differential amplifier with PMOS Load as shown in Fig.2 meeting the following requirements:

Parameter	Value	
DC Power Consumption	$<1.2 \text{ mW}$	max I should be 0.66mA
V_{out+} and V_{out-} DC Voltage	$0.9\text{-}1.1\text{V}$	set vout to be 1Acm gets limited
Differential Gain	$>20\text{dB}$	gain 10
Vout Bandwidth	$>40 \text{ MHz}$	
V_{out+} and V_{out-} Voltage Headroom (pk - pk)	$>0.4 \text{ V}$	automatically sets with vout

Given $C_L = 300 \text{ fF}$, $R_C = 500\text{K}\Omega$, $R_B = 500\text{K}\Omega$, $C_B = 20\text{pF}$, L for M7 and M6 = $0.5 \mu\text{m}$, $V_{dd} = 1.8 \text{ V}$

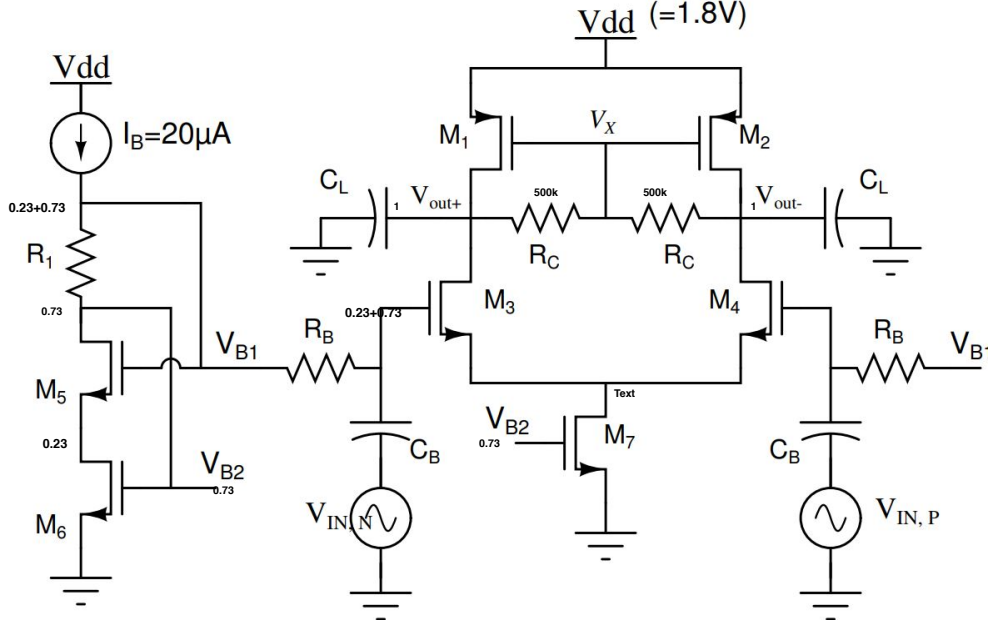


Figure 1: Diff Amplifier with PMOS Load

Hand-Calculation Questions:

(Use $k_n = 260\mu\text{A}/\text{V}^2$, $k_p = 100\mu\text{A}/\text{V}^2$, $V_{tn} = 0.5\text{V}$, $V_{tp} = 0.5\text{V}$, $\lambda_n = 0.16\text{V}^{-1}$ and $\lambda_p = 0.2\text{V}^{-1}$)

1. Draw the small signal circuit for half circuit of the differential amplifier (neglect the transistor capacitance and only consider load capacitance) [2 Marks]
2. Derive the expression for DC gain using the small signal model [1 Marks]
3. Derive the expression for Bandwidth [1 Marks]

4. Now find value of R_1 and W of M_5 , M_6 and M_7 needed for current mirroring. Tabulate the values obtained [2 Marks]
5. Finally, calculate W for M_1 , M_2 , M_3 and M_4 to meet the design specifications. Tabulate the values obtained [3 Marks]

Simulation Based Questions:

1. Show schematic with node voltages annotated [2 Marks]
2. Tabulate the V_{dsat} value, W , multipliers and no. of fingers used in the final simulations for all transistors. Also report the value of R_1 [2 Marks]
3. Show schematic with DC operating points annotated clearly (Note: They should be readable) [2 Marks]
4. Plot differential AC Gain (100 KHz to 100 GHz). Mark Gain at 1MHz and the 3 dB-Bandwidth on plot [2 Marks]
5. Plot transient differential output for a differential input of 8mV pk-pk sinusoid of 1 MHz (Plot 1 complete output cycle and mark the peak values). Also plot voltage at Node X and V_{out+} & V_{out-} in the same plot [1 Marks]
6. Fill the following table [2 Marks]

Specification	Value Obtained	Target Spec
DC Power Consumption		<1.2 mW
V_{out+} and V_{out-} DC Voltage		0.9-1.1V
Differential Gain		>20dB
Vout Bandwidth		>40 MHz