EE 735
Assignment – 1

7^{th} Aug 2019

Hints, assumptions and instructions:

1. Assume that all the capacitors are enclosed in a big box, whose boundaries are maintained at zero potential i.e. 0 V.
2. Assume that the thickness of the plates is 1 nm.
3. The entire dielectric region is charge free and $\epsilon_r = 1$
4. $V(x, y) = \frac{V(x+h,y)+V(x-h,y)+V(x,y+h)+V(x,y-h)}{4}$ in the charge free region.
5. Specify any physical quantity with the units.
6. It is mandatory to submit your code with the report (in pdf) in a single zip folder. Name the file as "RollNumber_Assignment1" for this assignment.

Questions:

Q1. Consider a system of two parallel plates as shown in Figure 1.

(a) Find out the capacitance (per unit width) of the structure by numerically solving the 2d Poisson's equation.

(b) Plot the electrostatic potential and equipotential surfaces.

(c) Plot the 2d electric field profile.

(d) Compare the simulated capacitance with the theoretical value ($C_{th} = \frac{\epsilon l}{d}$). Which one is smaller/larger and why?

Q2. For the structure mentioned in Q1,

(a) Vary l from 10 nm to 1000 nm in steps of 50 nm. Plot C as a function of l.

(b) Calculate the parasitic capacitance $C_p(l) = C(l) - C_{th}(l)$ and plot it as a function of l. Qualitatively explain the nature of the plot.

Q3. Consider an inclined plate capacitor as shown in Figure 2.

(a) Find out the capacitance (per unit width) of the structure.

(b) Plot the electrostatic potential and equipotential surfaces.

(c) Plot the 2d electric field profile.

(d) Find out the position where the magnitude of electric field is maximum.

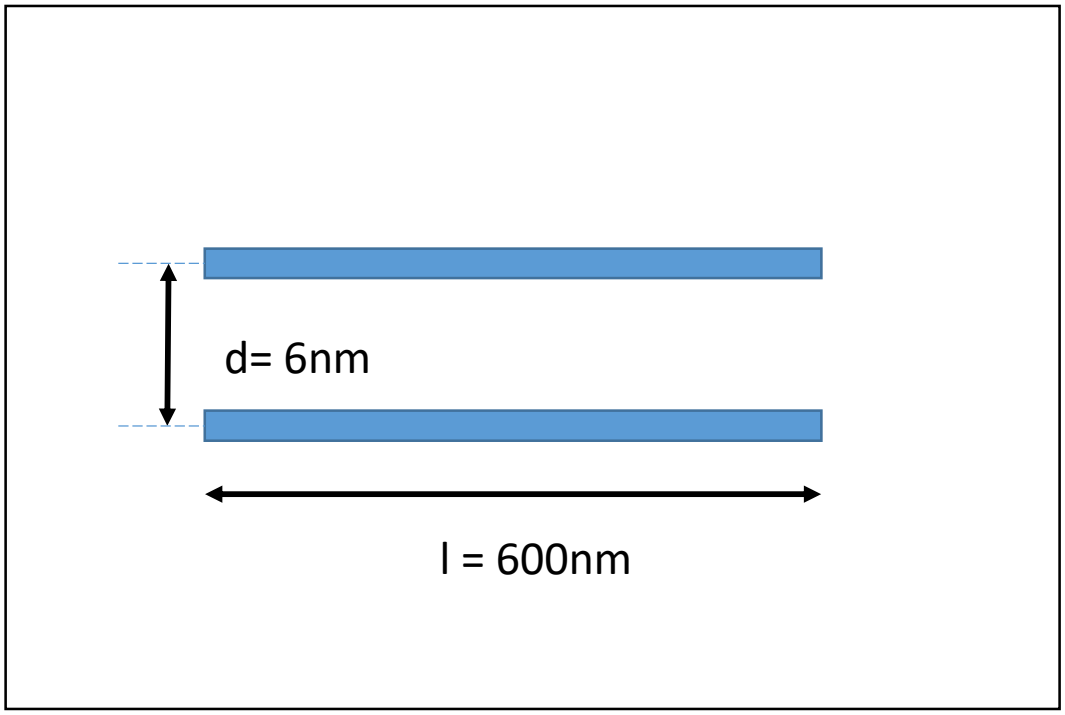

Figure 1.

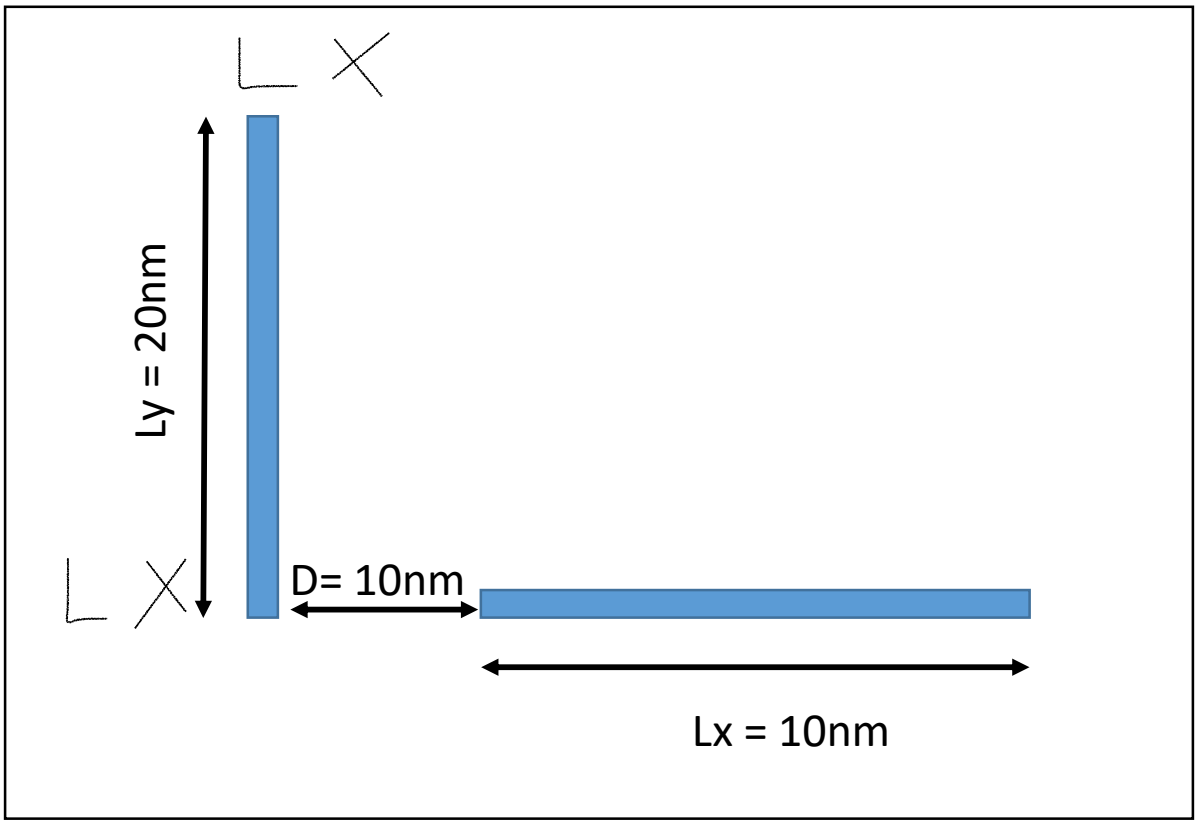

Figure 2.