Logic Design Styles

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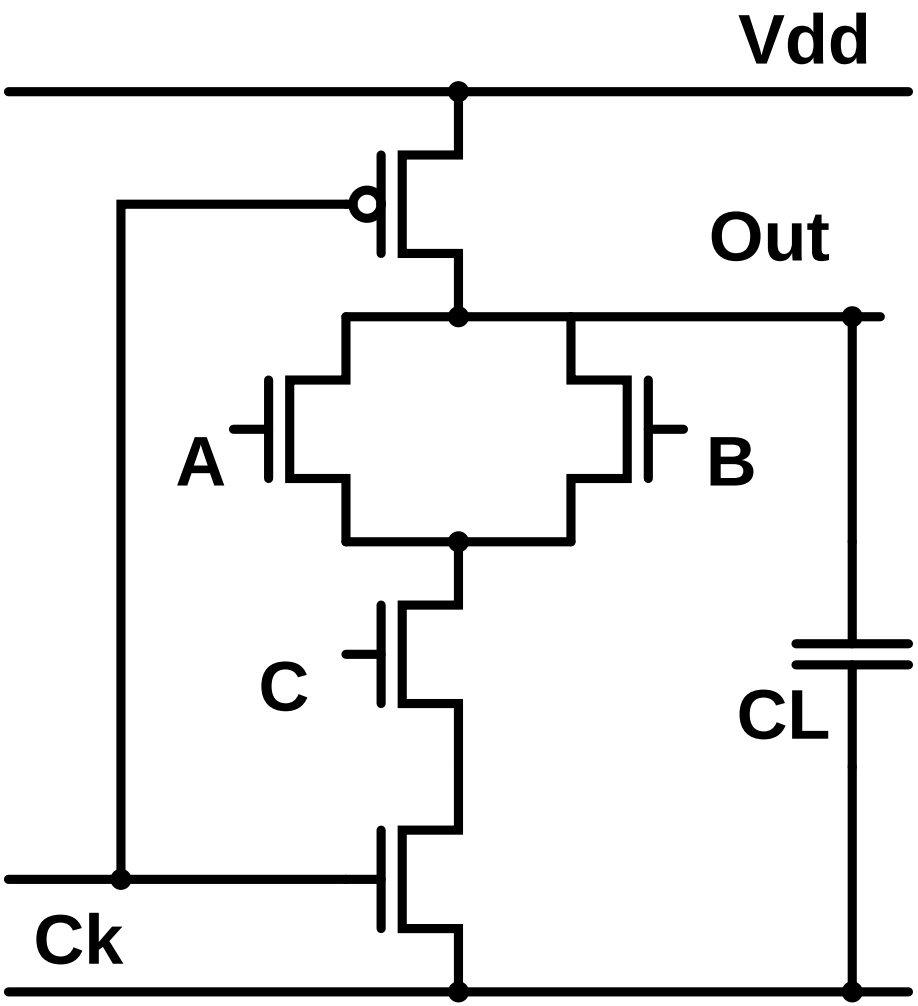
Dynamic logic

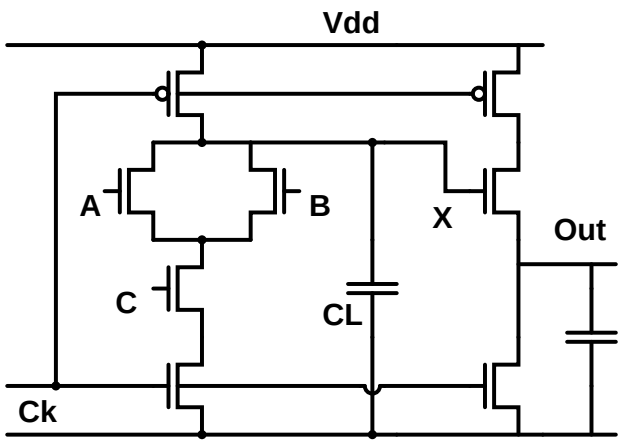
- In this style of logic, some nodes are required to hold their logic value as a charge stored on a capacitor.
- These nodes are not connected to their 'drivers' permanently.
- The 'driver' places the logic value on them, and is then disconnected from the node.
- Due to leakage etc., the logic value cannot be held indefinitely.
- Dynamic circuits therefore require a *minimum* clock frequency to operate correctly.
- Use of dynamic circuits can reduce circuit complexity and power consumption substantially.

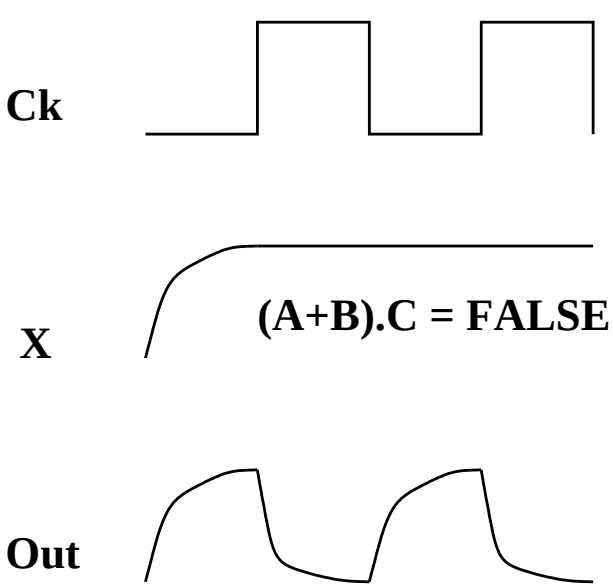
A CMOS dynamic logic circuit

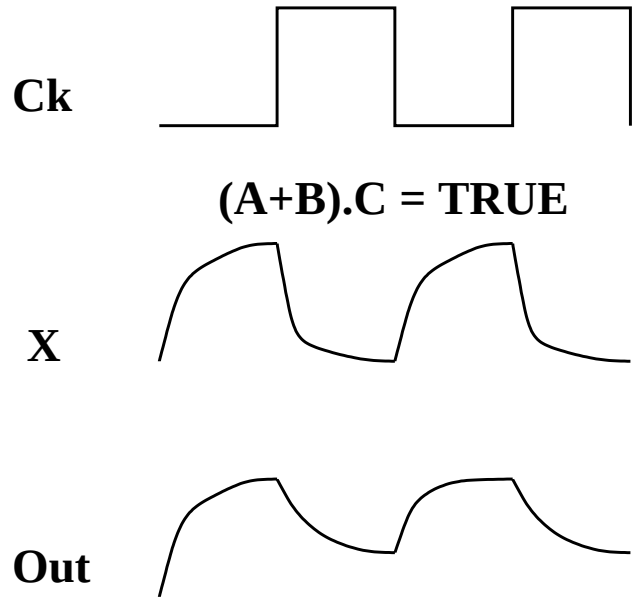


- When the clock is low, pMOS is on and the bottom nMOS is off.
- The output is 'pre-charged' to 1 unconditionally.
- When the clock goes high, the pMOS turns off and the bottom nMOS comes on.
- The circuit then conditionally discharges the output node, if (A+B).C is TRUE.
- This implements the function $\overline{(A+B).C}$.

Problem with Cascading

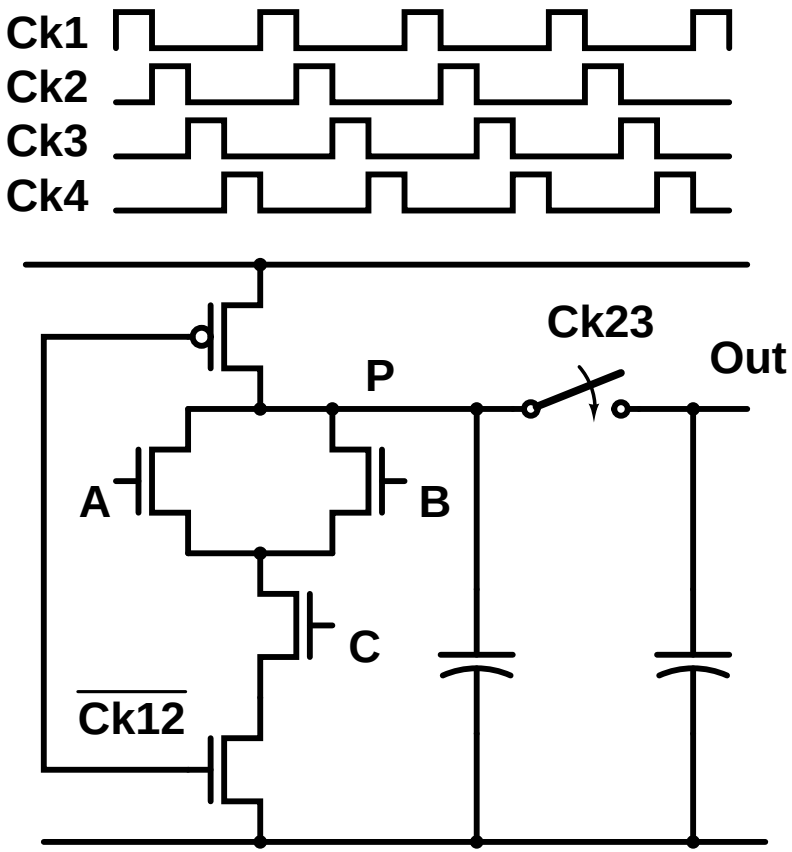






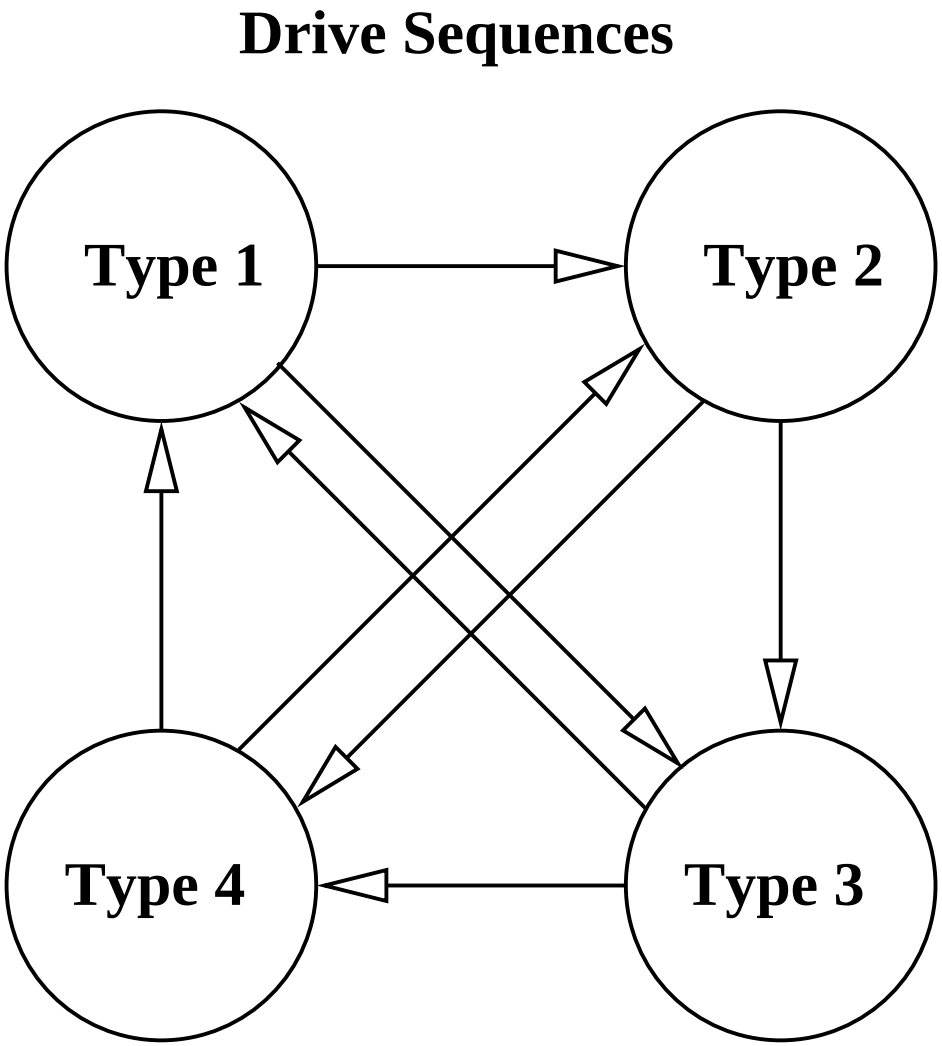
There is no problem when (A+B).C is false. X pre-charges to 1 and remains at 1.
When (A+B).C is TRUE, X takes some time to discharge.
During this time, charge placed on the output leaks away as the input to nMOS of the inverter is not 0.

4 Phase Dynamic Logic



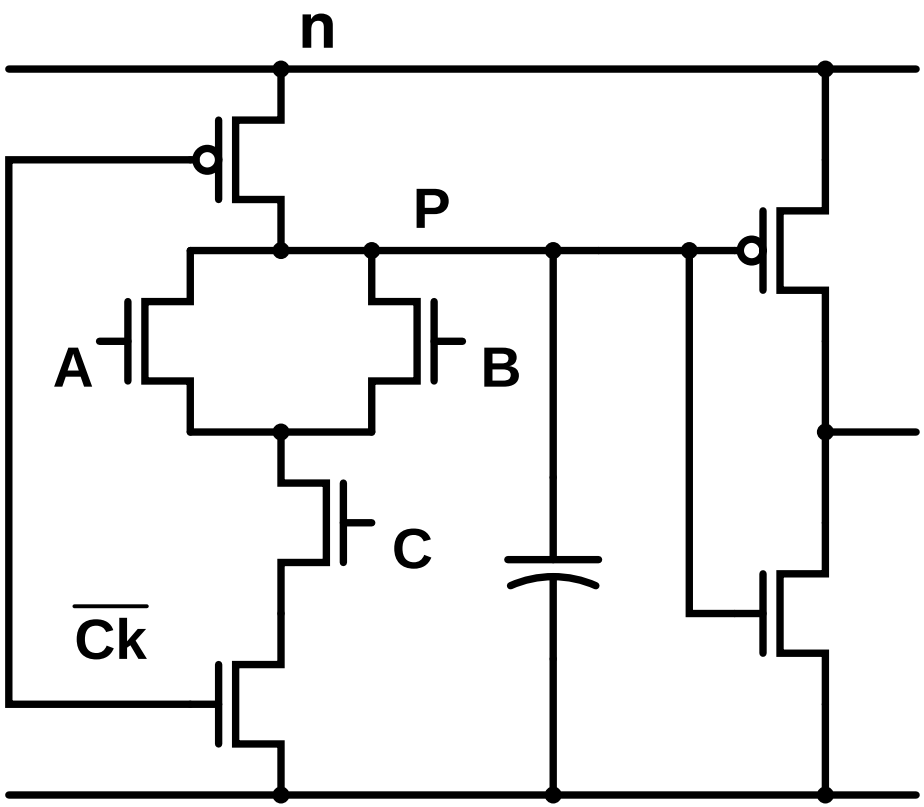
- The problem can be solved by using a 4 phase clock.
- In phase 1 node P is pre-charged.
- In phase 2 P and output are pre-charged.
- In phase 3 The gate evaluates.
- In phases 4 and 1, the output is isolated from the driver and remains valid.
- This is called a type 3 gate. It evaluates in phase 3 and is valid in phases 4 and 1.
- Similarly, we can have type 4,

Drive cycles



- A type 3 gate can drive a type 4 or a type 1 gate.
- similarly, type 4 will drive types 1 and 2; type 1 will drive types 2 and 3; and type 2 will drive types 3 and 4.
- We can use a 2 phase clock if we stick to type 1 and type 3 gates (or type 2 and type 4 gates) as these can drive each other.

Domino Logic



Another way to eliminate the problem with cascading logic stages is to use a static inverter after the CMOS dynamic gate. The output is '0' when it is not valid. Therefore, it does no affect the evaluation of the next gate.