# EE618(Zele)
# CMOS Analog IC Design

Course Project - I.
Deadline :$15^{th}$ October 2019 01:55 PM
Total Marks : 50

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**Specifications**

Design an Ultra Low Power Operational Transconductance Amplifier in SCL 180nm technology (fully differential input, single ended output) to meet the following specifications:

- DC gain $\geq$ 110 dB
- Unity gain frequency $\geq$ 70 MHz
- Output voltage swing $\geq$ 1 $V_{p-p}$
- Slew rate $\geq$ 40 V/$\mu$s
- Phase Margin $\geq 60^0$
- Input referred spot noise (at 1 MHz) $\leq$ 25 nV/$\sqrt{Hz}$
- Input referred spot noise (at 0.1 MHz) $\leq$ 35 nV/$\sqrt{Hz}$
- Input Common mode voltage = 0.9 V
- Output load capacitance = 1 pF (From analogLib)
- VDD = 1.8 V
- Power consumption $\leq$ 0.3 mW

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**Note:** A Viva voce will be held after the submission deadline. Students must explain the design flow and the results that they obtain and show the simulations on laptops.

**Simulations to be performed**

Tabulate the Opamp Specifications in typical corner as shown below: [Typical corner: TT, $27^0$C]

| Parameters | Value (Unit) |
|---|---|
| DC gain | |
| Unity Gain frequency | |
| Phase Margin | |
| Slew rate | |
| Output Swing (V$p-p$ ) | |
| Settling Time (1% accuracy) | |
| Input referred spot noise (at 1 MHz) | |
| Input referred spot noise (at 100 KHz) | |
| CMRR | |
| PSRR Pluse | |
| PSRR Minus | |
| ICR (Input Common Mode Range) | |
| Power | |

Tabulate the following specifications in the corners specified in the table below.

| **Corner** | **SS** | | **TT** | **FF** | |
|---|---|---|---|---|---|
| **Temperature ( $^0$C)** | **0** | **100** | **27** | **0** | **100** |
| DC Gain | | | | | |
| Unity Gain Frequency | | | | | |
| Phase Margin | | | | | |

**Grading**

- Initial design/Hand Calculation : 10 Marks
- Simulation Results : 20 Marks
- Quality of the report : 5 Marks
- Viva voce : 15 Marks
- Bonus points (Based on architecture)
  - MOSFET-C tracking : 5 Marks
  - [1] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers,"IEEE J. Solid-State Circuits, vol. SSC-17,no. 3, pp. 522–528, Jun. 1982. : 10 Marks

- [2] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," in IEEE Journal of Solid-State Circuits, vol. 29, no. 12, pp. 1505-1513, Dec. 1994. : 10 Marks
- [3] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," in IEEE Journal of Solid-State Circuits, vol. 25, no. 6, pp. 1379-1384, Dec. 1990 : 12.5 Marks
- [4] D. Y. Yoon, H.-S. Lee, and J. Gealow, "Power-efficient amplifier frequency compensation for continuous-time delta-sigma modulators," in IEEE International Midwest Symposium on Circuits and Systems, pp. 562-565, Aug 2013 : 12.5 Marks

**Variation in one of the specs is allowed for [1]-[4] only with prior sanction from TAs.**

**Project-2(Layout) bonus will be decided on architecture complexity.**