EE669: VLSI Technology

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Office hour: Friday 10:00 – 11.00 AM, EE Annex, Room: 104

IC fabrication

The front-end-of-line (FEOL)

Back end of line (BEOL)

Front End Processing???

Back End Processing

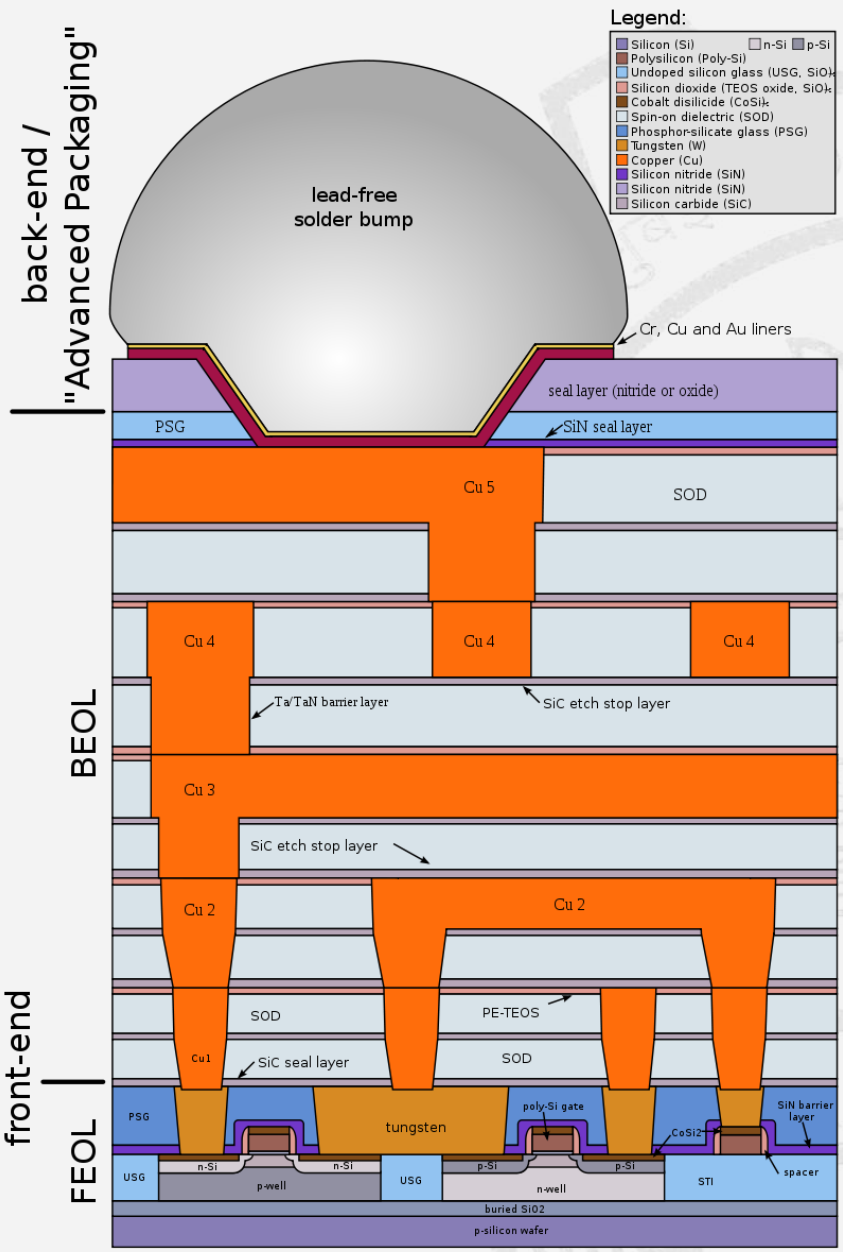
- Back-end process" (also called post-fab)
- Uusally not in the cleanroom
- often by a different company
- includes wafer test, wafer backgrinding, die separation, die tests, IC packaging and final test.

The front-end-of-line (FEOL):

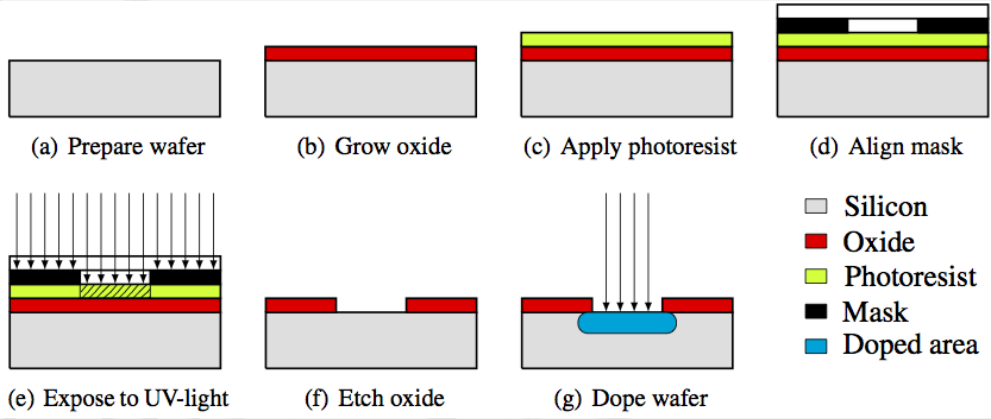
- The individual devices (transistors, capacitors, resistors, etc.) are patterned in the semiconductor.
- Generally covers everything up to (but not including) the deposition of **metal interconnect layers.**
- In **CMOS** process, ***FEOL contains all fabrication steps needed to form fully isolated CMOS elements***
- Selecting the type of wafer to be used;
- **Chemical-mechanical planarization and cleaning of the wafer. Shallow trench isolation (STI) (or LOCOS in early processes, with feature size > 0.25 µm), Well formation, Gate module formation, Source and drain module formation**

The back end of line (BEOL):

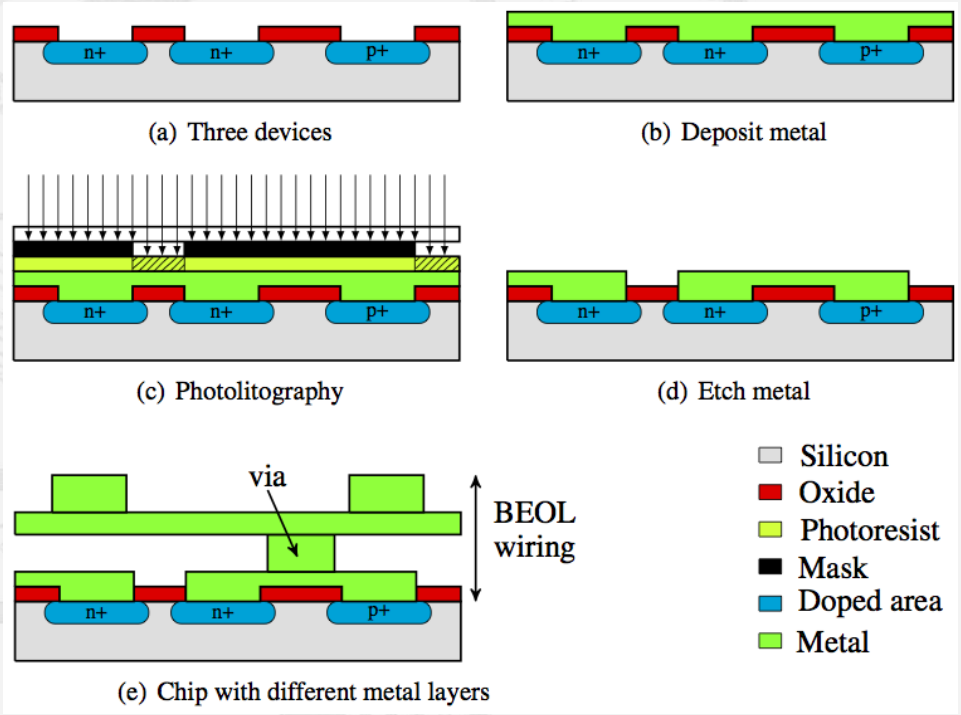
- The individual devices (transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer, the metalization layer. Common metals are **copper and aluminum**. **BEOL** generally begins with the first layer of metal deposited on the wafer.
- **BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections.**



Source: wikipedia



FEOL



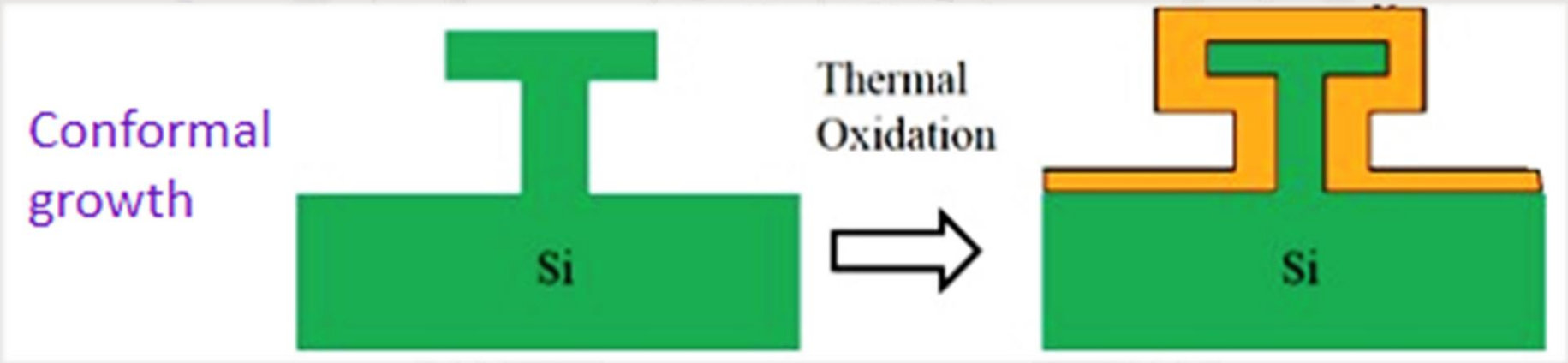
BEOL

Source: TU Vienna

Thermal Oxidation and the Si/SiO_2 interface

Properties of thermally grown SiO_2

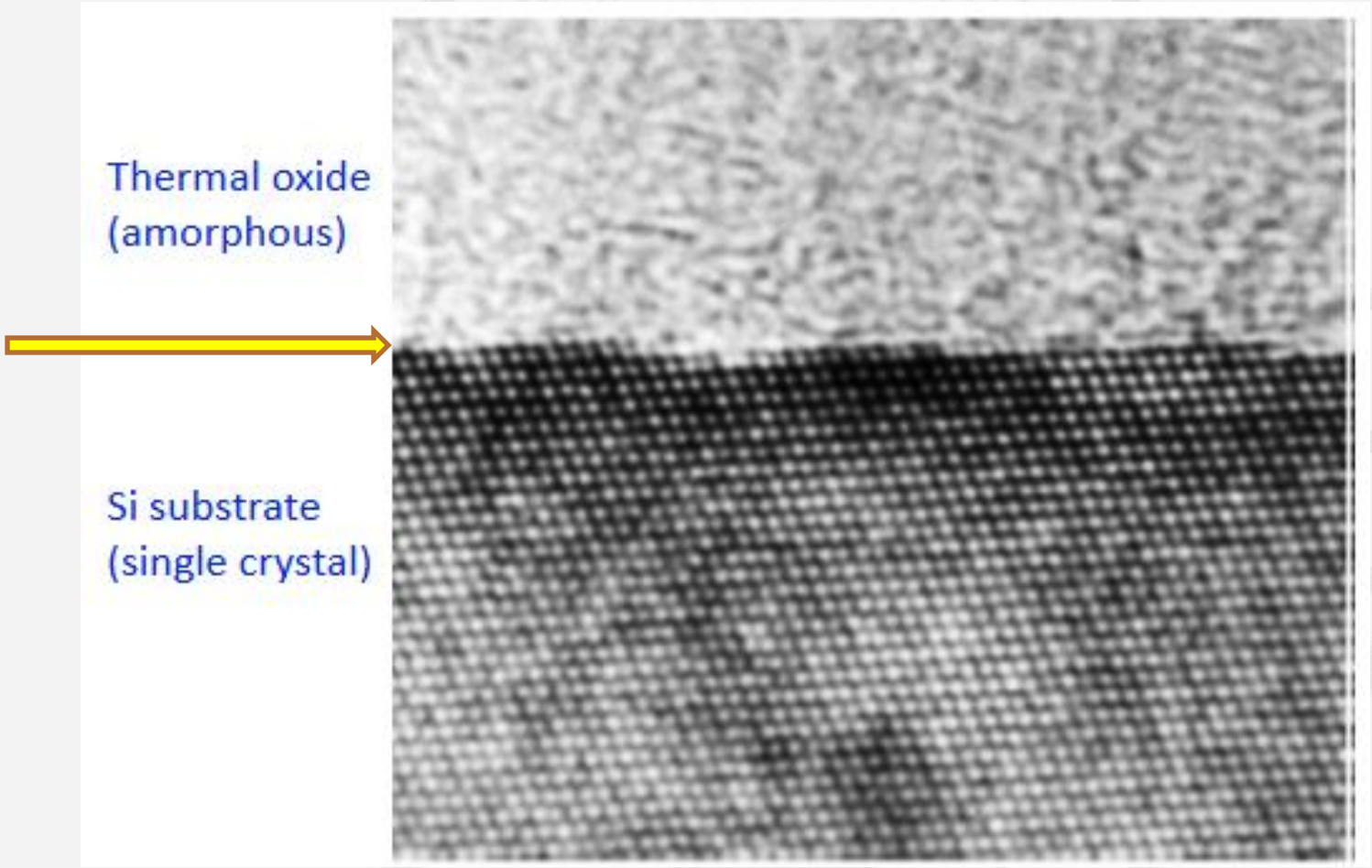
- It is amorphous.
- Stable, reproducible and conformal SiO_2 growth
- Melting point: 1700°C
- Density: 2.21 g/cm^3 (almost the same as Si that is 2.33 g/cm^3)
- Crystalline SiO_2 [Quartz] = 2.65gm/cm^3



Properties of thermally grown SiO_2

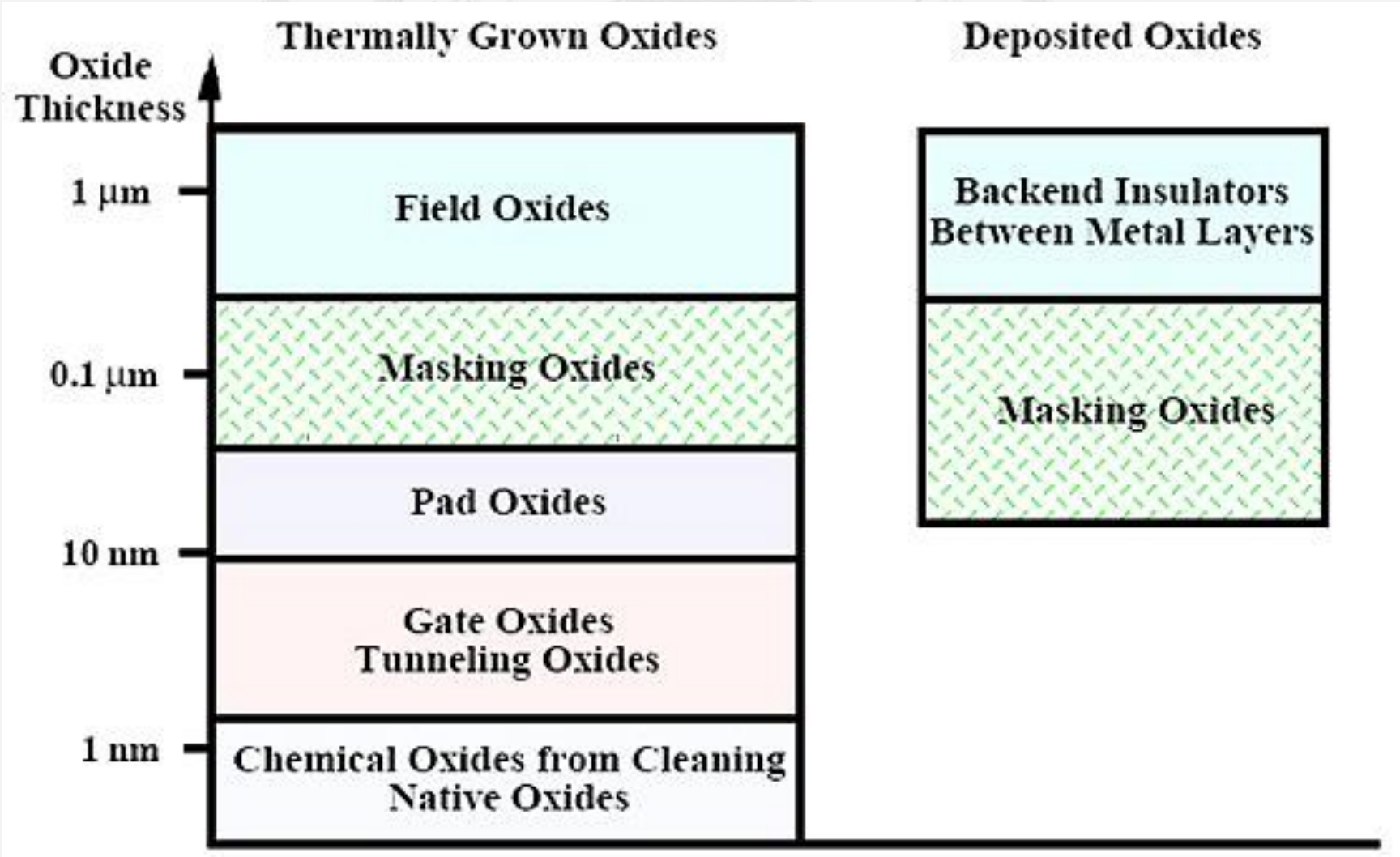
DC Resistivity (Ω cm), 25°C	10^{14} - 10^{16}	Melting Point (°C)	~1700
Density (g/cm^3)	2.27	Molecular Weight	60.08
Dielectric Constant	3.8 - 3.9	Molecules (/cm^3)	2.3×10^{22}
Dielectric Strength (V/cm)	$5 - 10 \times 10^6$	Refrctive Index	1.46
Energy Gap (eV)	~ 8	Specific Heat (J/g °C)	1.0
Etch rate in BHF (Å/min)	1000	Stress in film on Si (dyne/cm^2)	$2 - 4 \times 10^9$ (compression)
Infrared Absorption Peak	9.3		
Linear Expansion Coefficient (cm/°C)	5.0×10^{-7}	Thermal Conductivity (W/cm°C)	0.014

The Si/SiO2 Interface



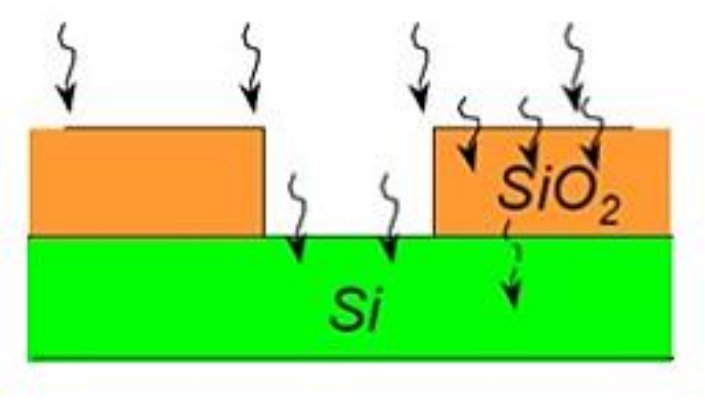
Atomically sharp interface between Si and SiO2: One major reason why Si overtook Ge in semiconductor industry

Application of SiO_2 in IC industry

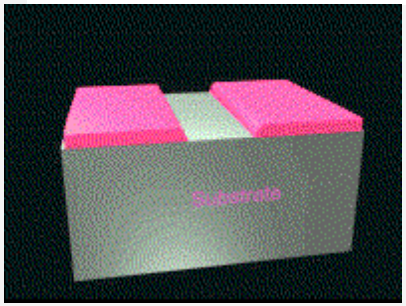


Diffusion mask for common dopant

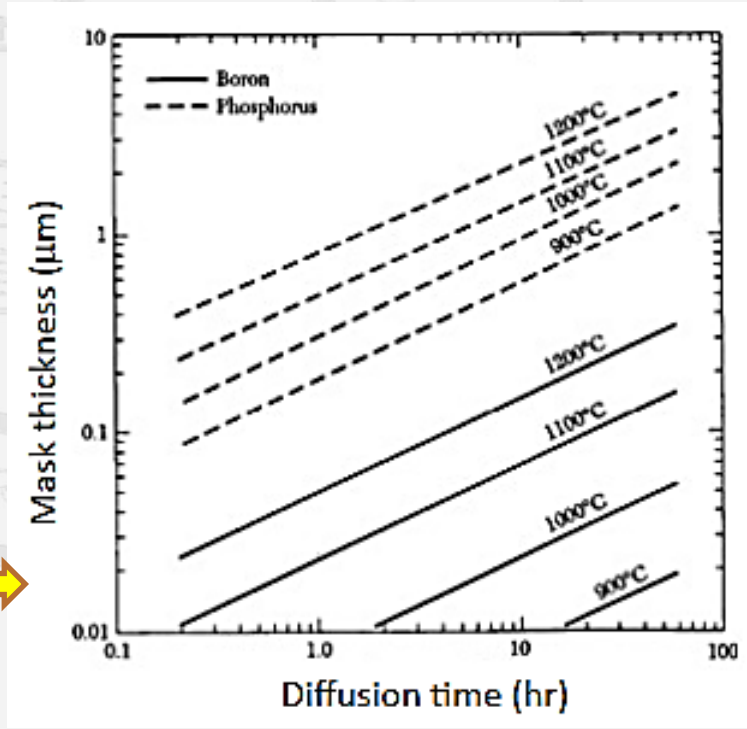
- SiO_2 provides a selective mask against
- Diffusion at high temperature ($D_{SiO2} << D_{si}$)
- Oxides used for masking: ~0.5-1μm thick



Dopants	Diffusion Constants at 1100 °C (cm^2/s)
B	$3.4 \times 10^{-17} - 2.0 \times 10^{-14}$
Ga	5.3×10^{-11} (not good for Ga)
P	$2.9 \times 10^{-16} - 2.0 \times 10^{-13}$
As	$1.2 \times 10^{-16} - 3.5 \times 10^{-15}$
Sb	9.9×10^{-17}

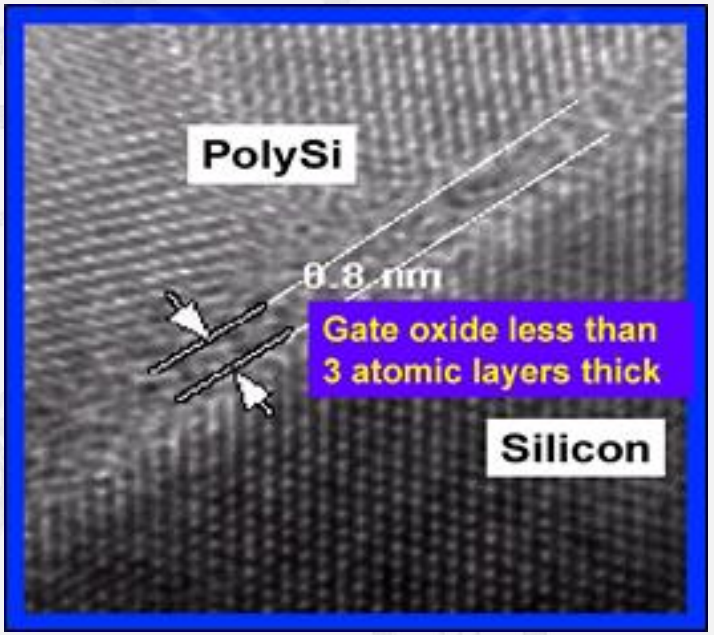


SiO_2 mask for B and P

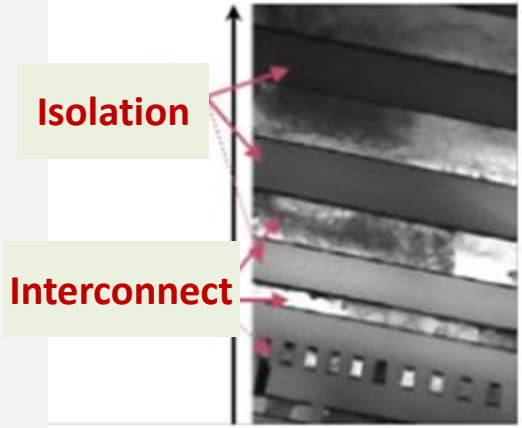


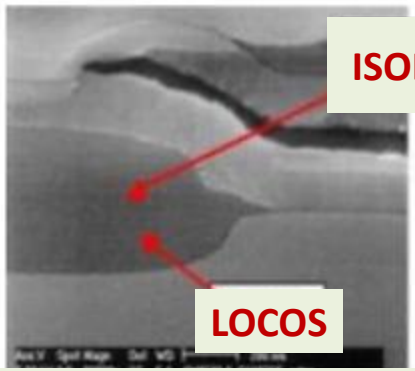
SiO_2 in MOSFET

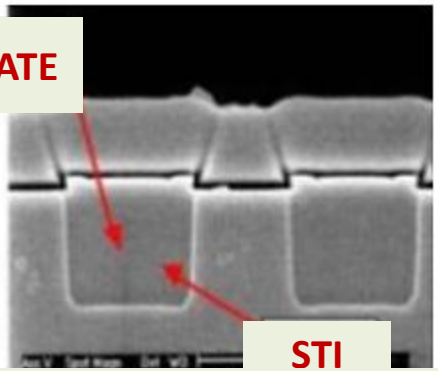
Gete oxide thickness: 0.8nm!!



An Insulation materials between Interconnect and adjacent devices

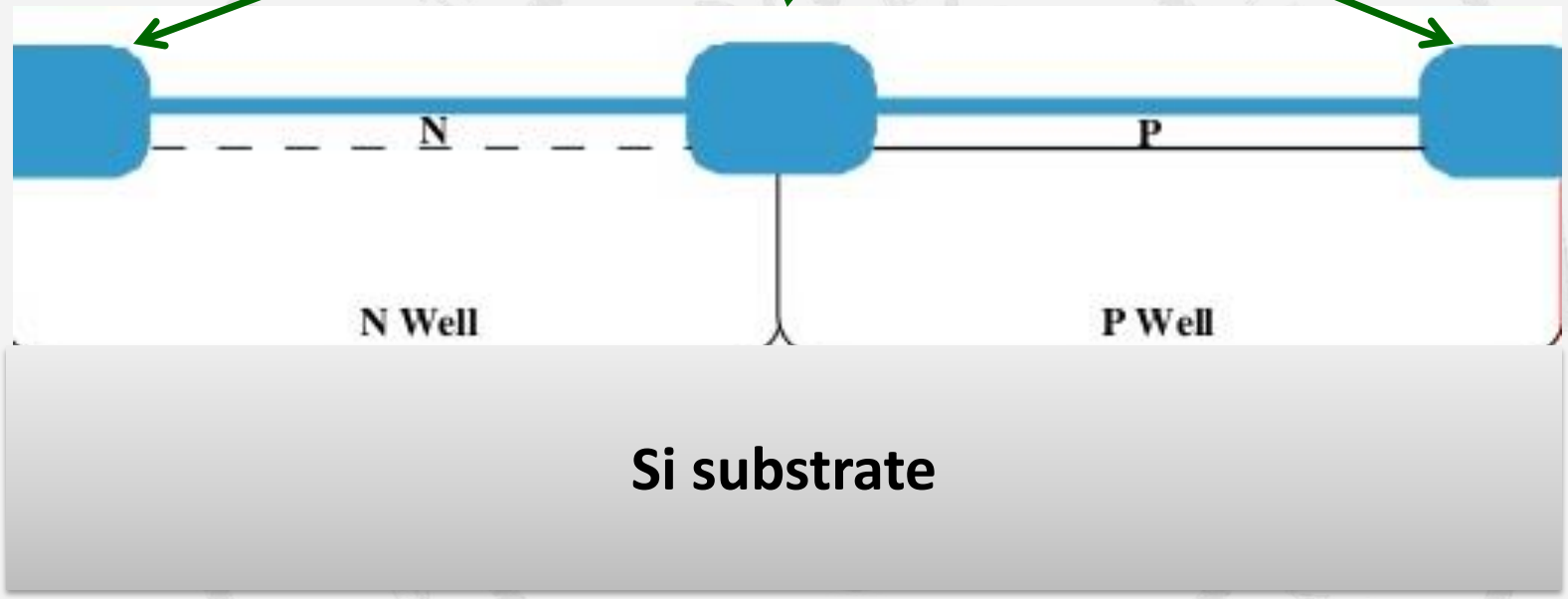






LOCOS: LOCal Oxidation Isolation, STI: Shallow Trench Isolation

LOCOS: LOCal Oxidation of Silicon



LOCOS: LOCal Oxidation of Silicon

Typical process steps are the following:

I. Preparation of silicon substrate (layer 1)

II. CVD of SiO_2, pad/buffer oxide (layer 2)

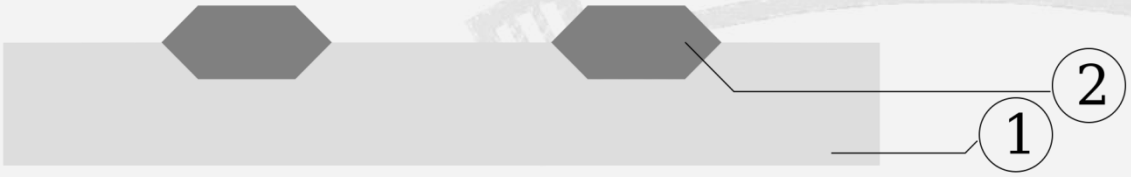
III. CVD of Si_3N_4, nitride mask (layer 3)

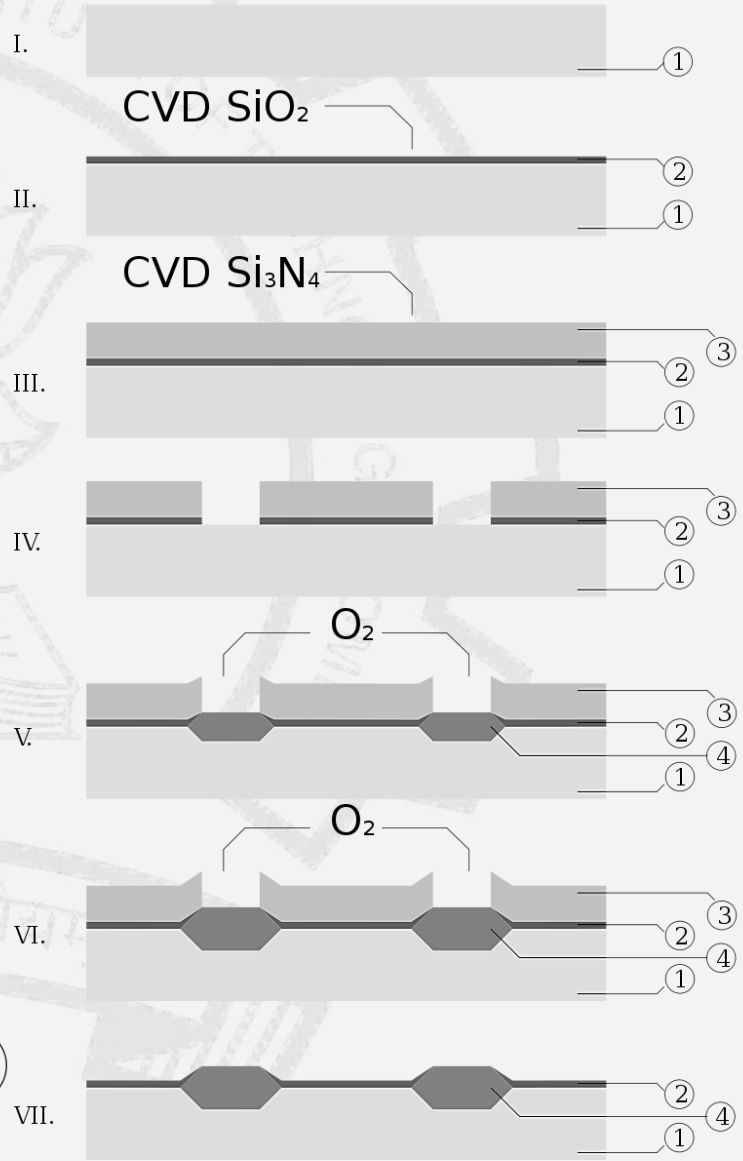
IV. Etching of nitride layer (layer 3) and silicon oxide layer (layer 2)

V. Thermal growth of silicon oxide (structure 4)

VI. Further growth of thermal silicon oxide (structure 4)

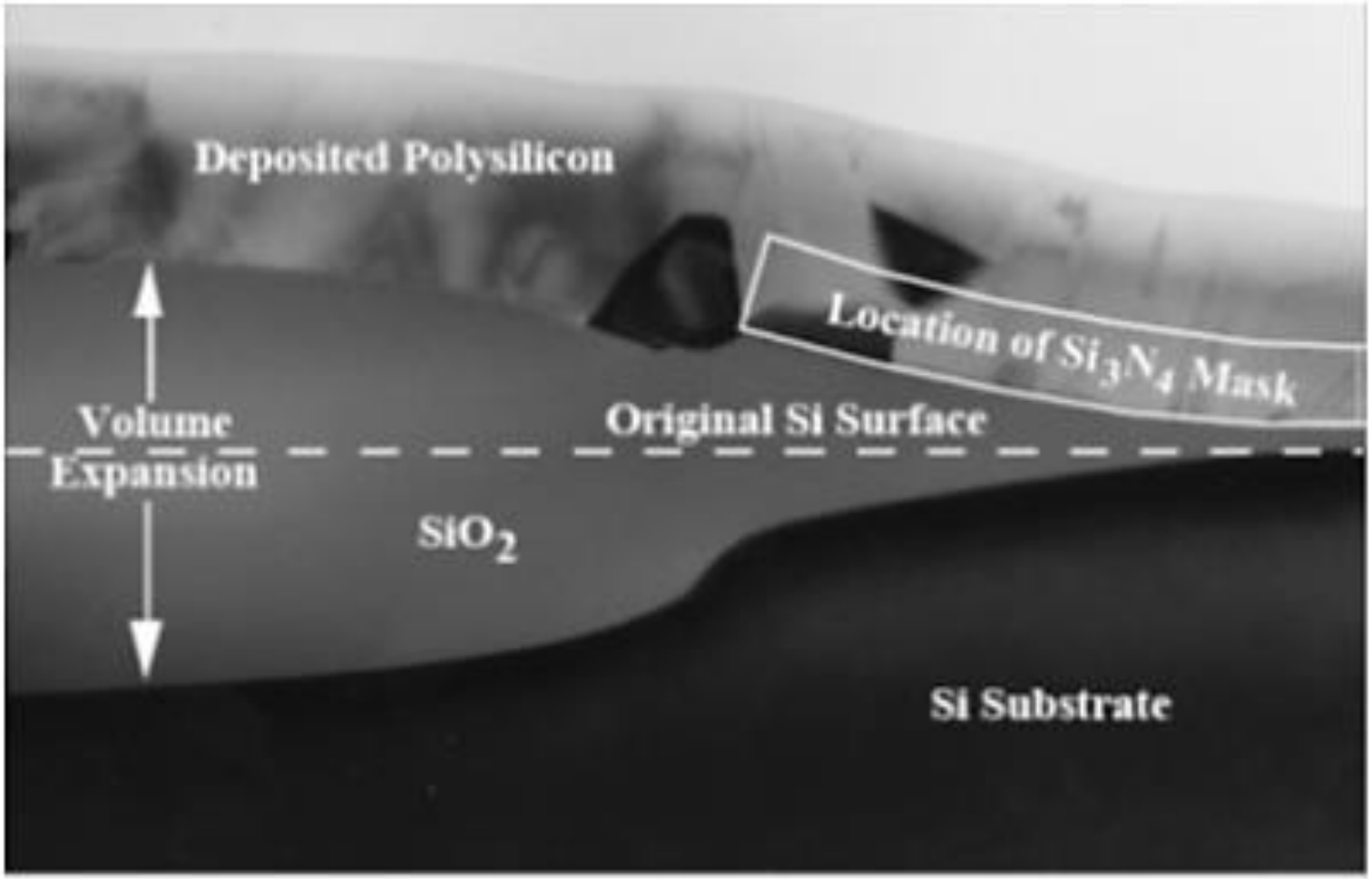
VII. Removal of nitride mask (layer 3)



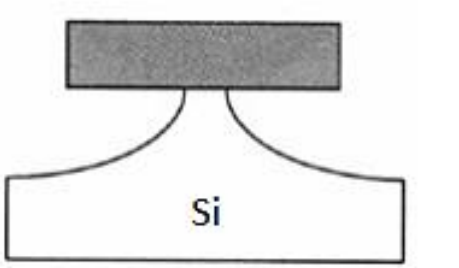


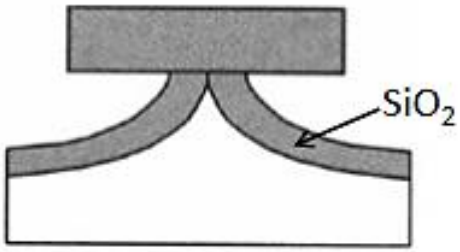
LOCOS: LOCal Oxidation of Silicon

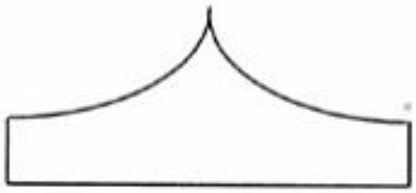
How does it look like??

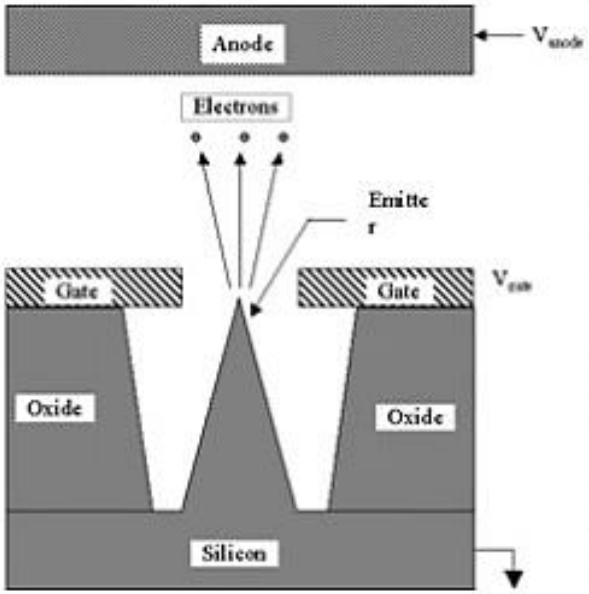


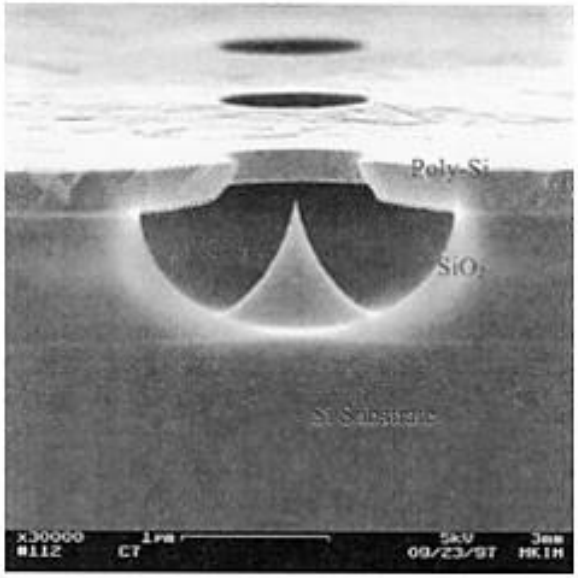
For nanofabrication: oxidation sharpening for sharp AFM tips or field emitters for display







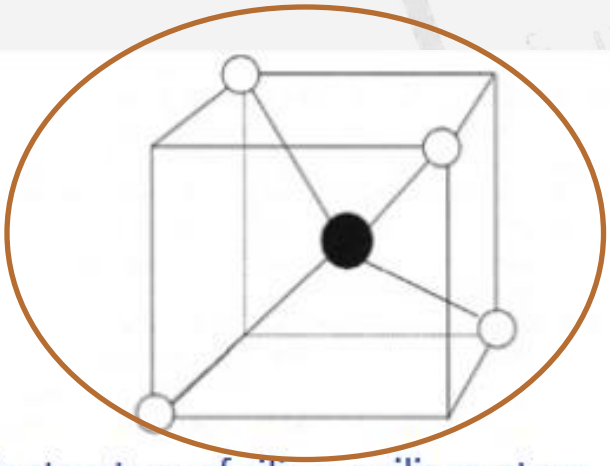




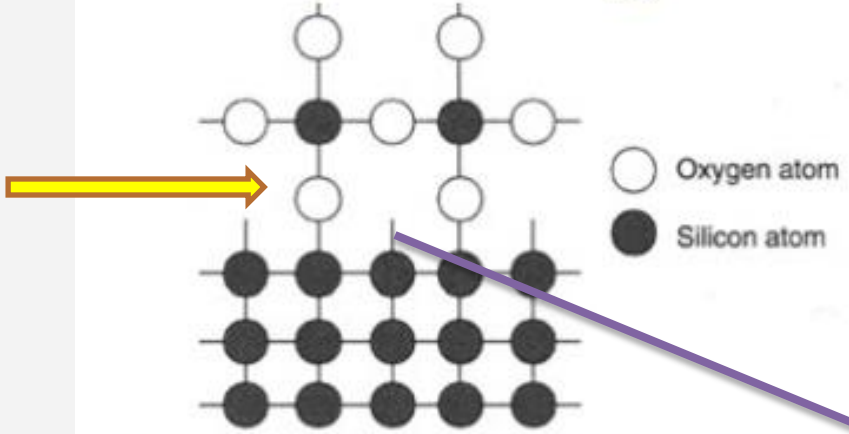
Field emission display (FED)

Silicon Field Emission Array with Atomically Sharp Tips. Turn on Voltage and The effect of Tip Radius Distribution

Oxide structure

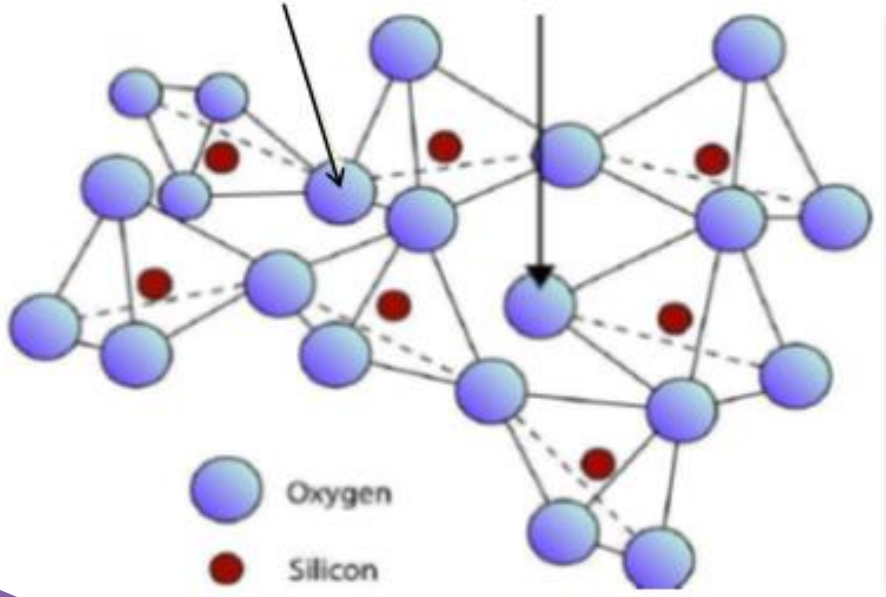


Basic structure of silica: a silicon atom tetrahedrally bonds to four oxygen atoms



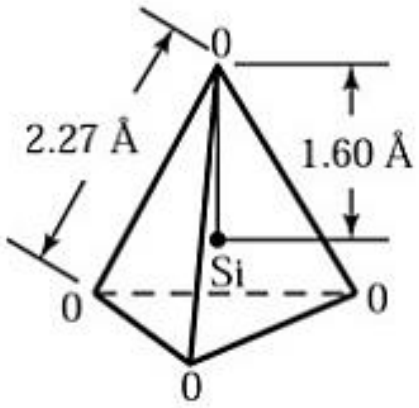
The structure of silicon-silicon dioxide interface: some silicon atoms have dangling bonds.

Amorphous tetrahedral network

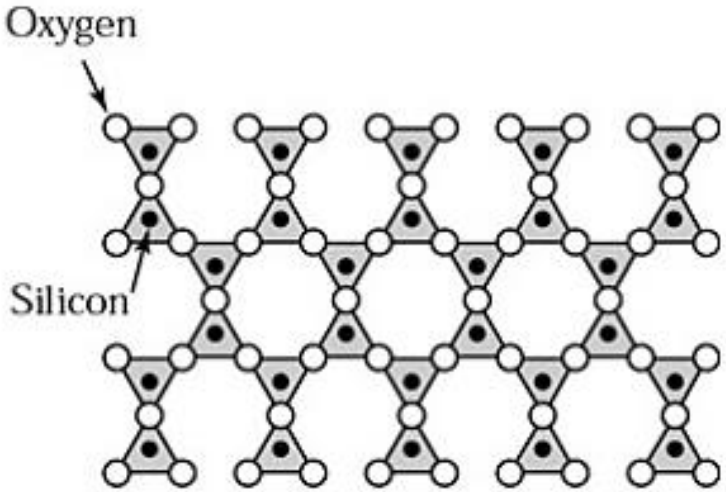


Dangling bond

Oxide Structure

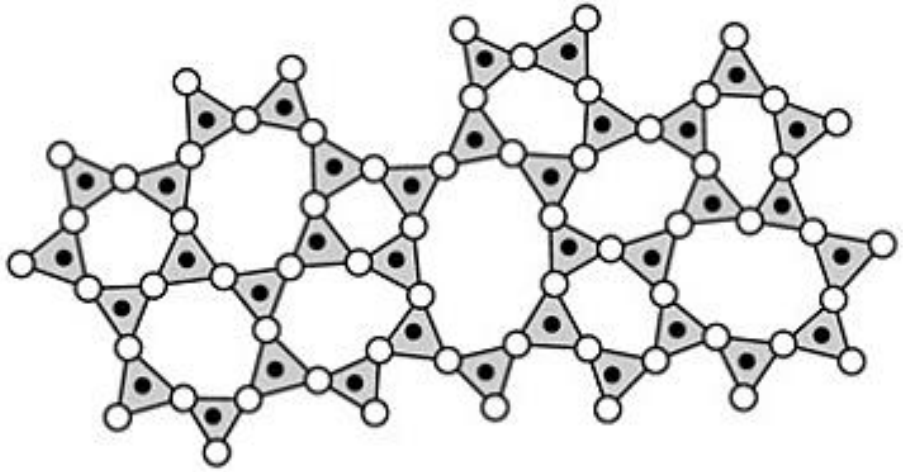


(a)



(b)

Single crystal (quartz)
2.65 g/cm^3



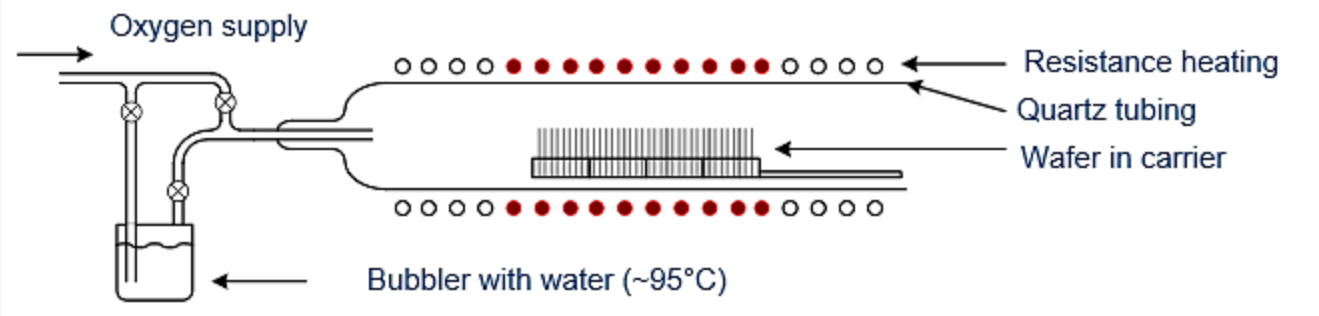
(c)

Amouphous (thermal oxide). 2.21 g/cm^3

Basics of oxidation

Dry oxidation: $Si + O_2 = SiO_2$ **Takes place under pure oxygen atmosphere.**

- **This process is done at 1000 to 1200°C actually. To create a very thin and stable oxide the process can be done at even lower temperatures of about 800 °C**



Characteristic of the dry oxidation:

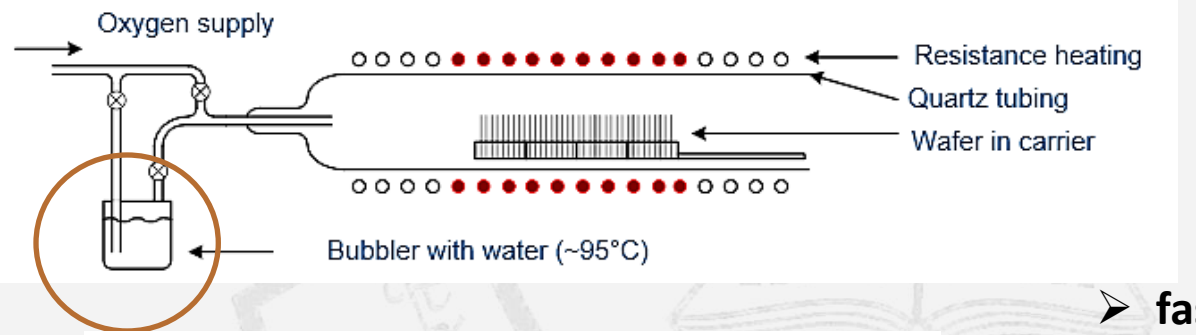
- **slow growth of oxide (0.05-0.5μm)**
- **high density, excellent quality**
- **high breakdown voltage**
- **Very thin oxide. May add nitrogen to form Oxynitride**

Basics of oxidation

Wet oxidation:

- The oxygen is led through a bubbler vessel filled with hot water (about 95°C), so that in addition to oxygen water is present in the quartz tube as steam

$$Si + 2\,H_2O \longrightarrow SiO_2 + 2\,H_2$$



This process is carried out at 900 to 1000°C.

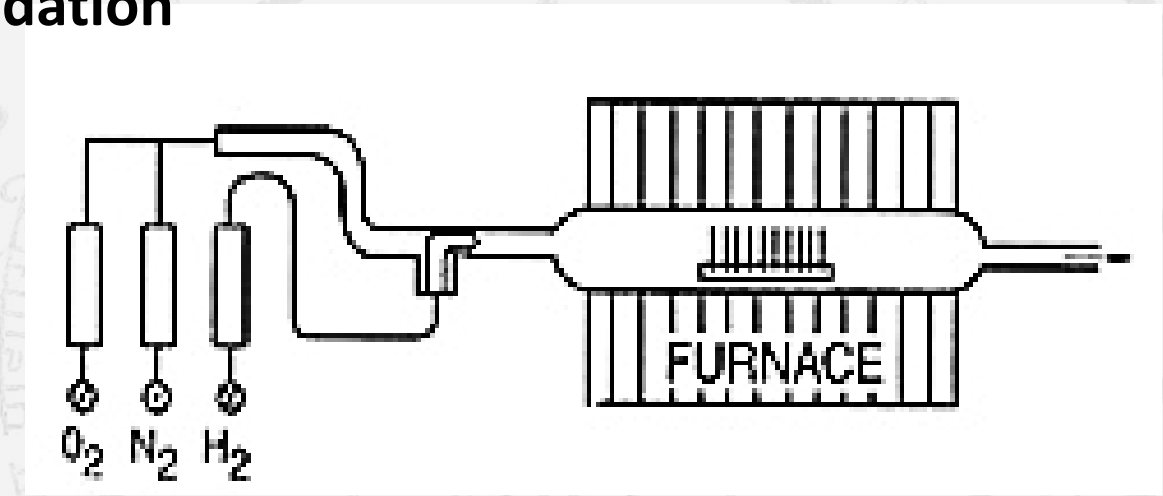
The characteristics

- fast growth even on low temperatures
- Inferior quality than dry oxides

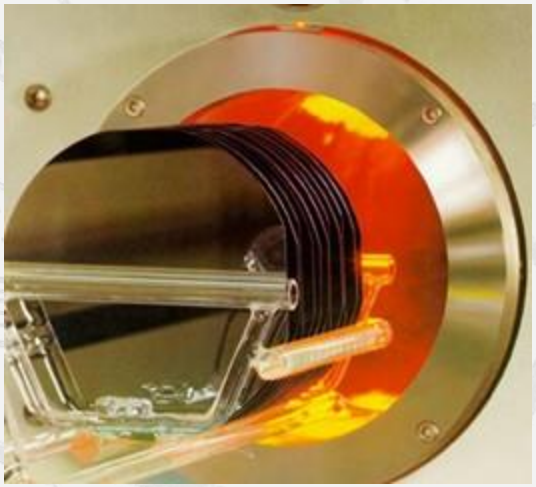
Temperature	Dry oxidation	Wet oxidation
900 °C	19 nm/h	100 nm/h
1000 °C	50 nm/h	400 nm/h
1100 °C	120 nm/h	630 nm/h

Comparison of the growth rate of wet and dry oxidation of silicon

Pyrogenic Oxidation

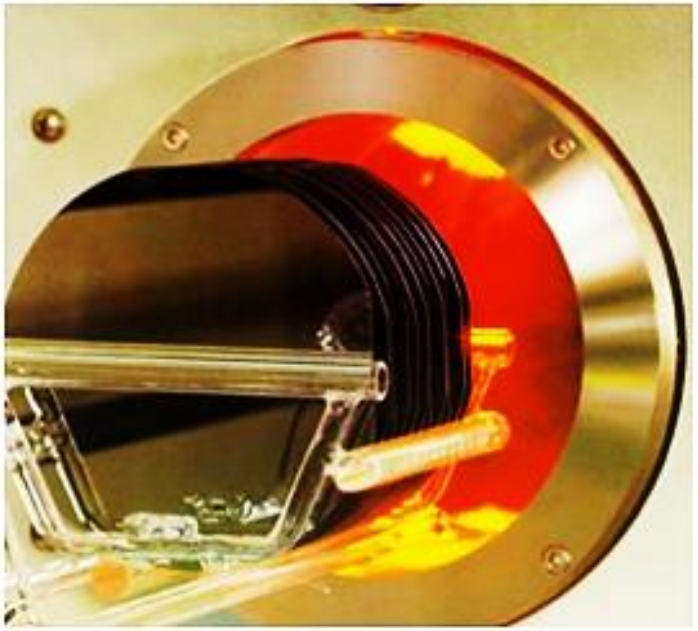


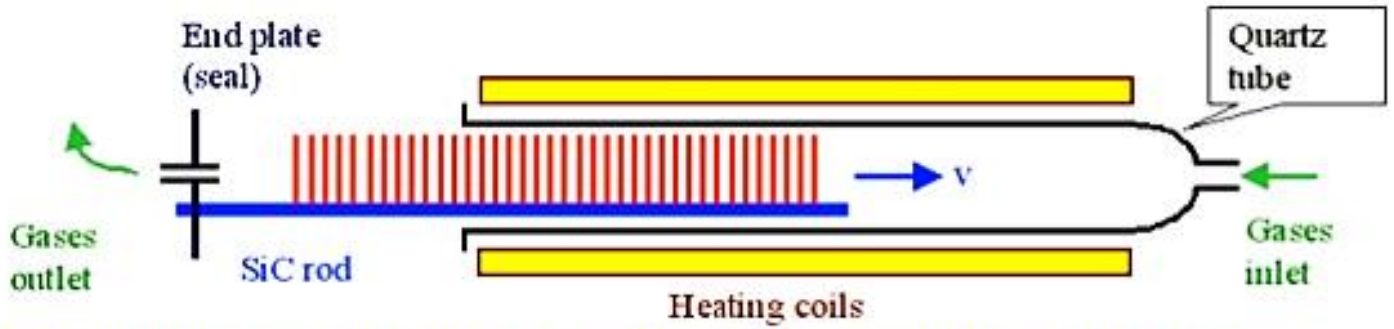
Oxidation using H_2 and O_2 is more cleaner and popular than H_2O vapor exposure



Furnaces used for diffusion and thermal oxidation

Thermal oxidation equipment

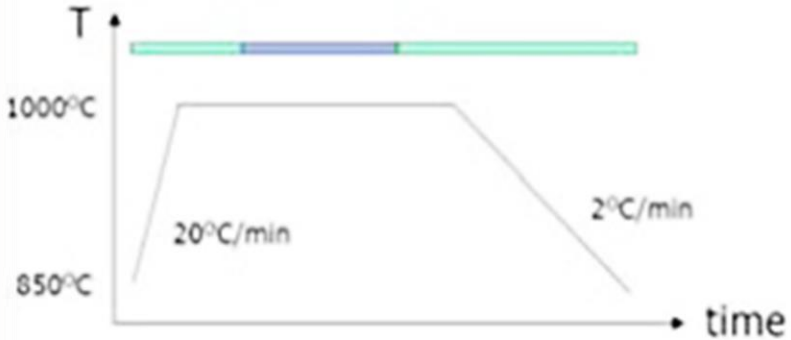




- The tubular reactor made of quartz or glass, heated by resistance.
- Oxygen or water vapor flows through the reactor and past the silicon wafers, with a typical velocity of order 1cm/s.

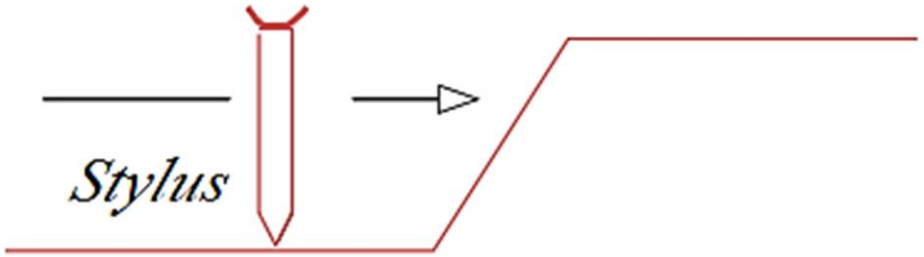
Thermal oxidation in practice

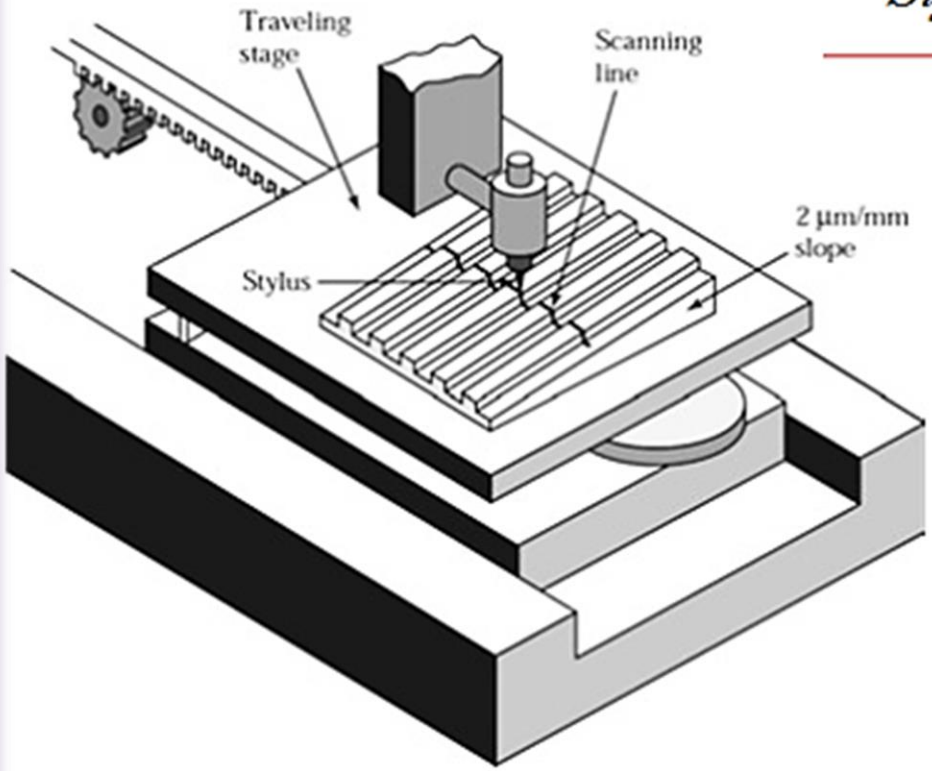
1. Clean the wafers (RCA clean, very important)
2. Put wafers in the boat
3. Load the wafers in the furnace
4. Ramp up the furnace to process temperature in N_2 (prevents oxidation from occurring)
5. Stabilize
6. Process (wet or dry oxidation)
7. Anneal in N_2. Again, nitrogen stops oxidation process.
8. Ramp down



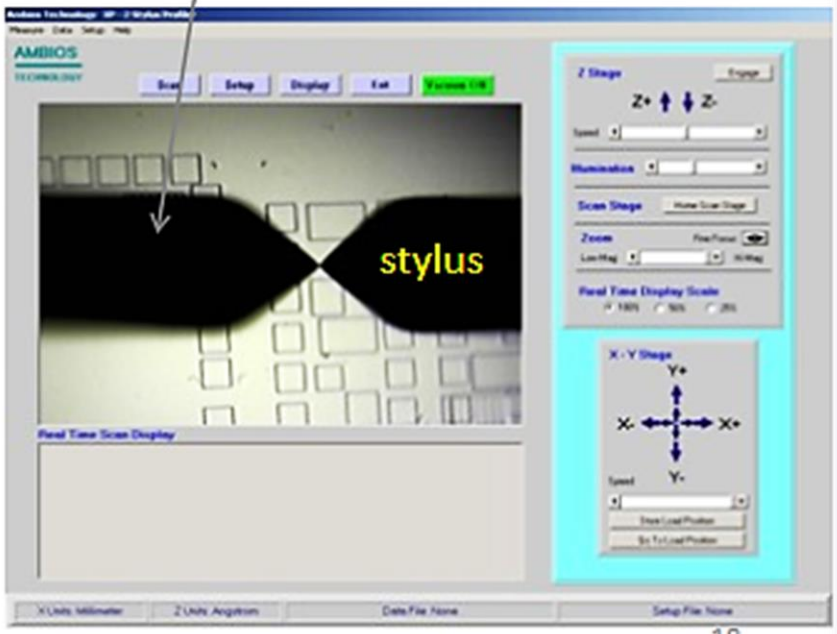
Surface profilometry (Dektak): mechanical thickness measurement

Oxide etched away by HF over part of the wafer and a mechanical stylus is dragged over the resulting step.



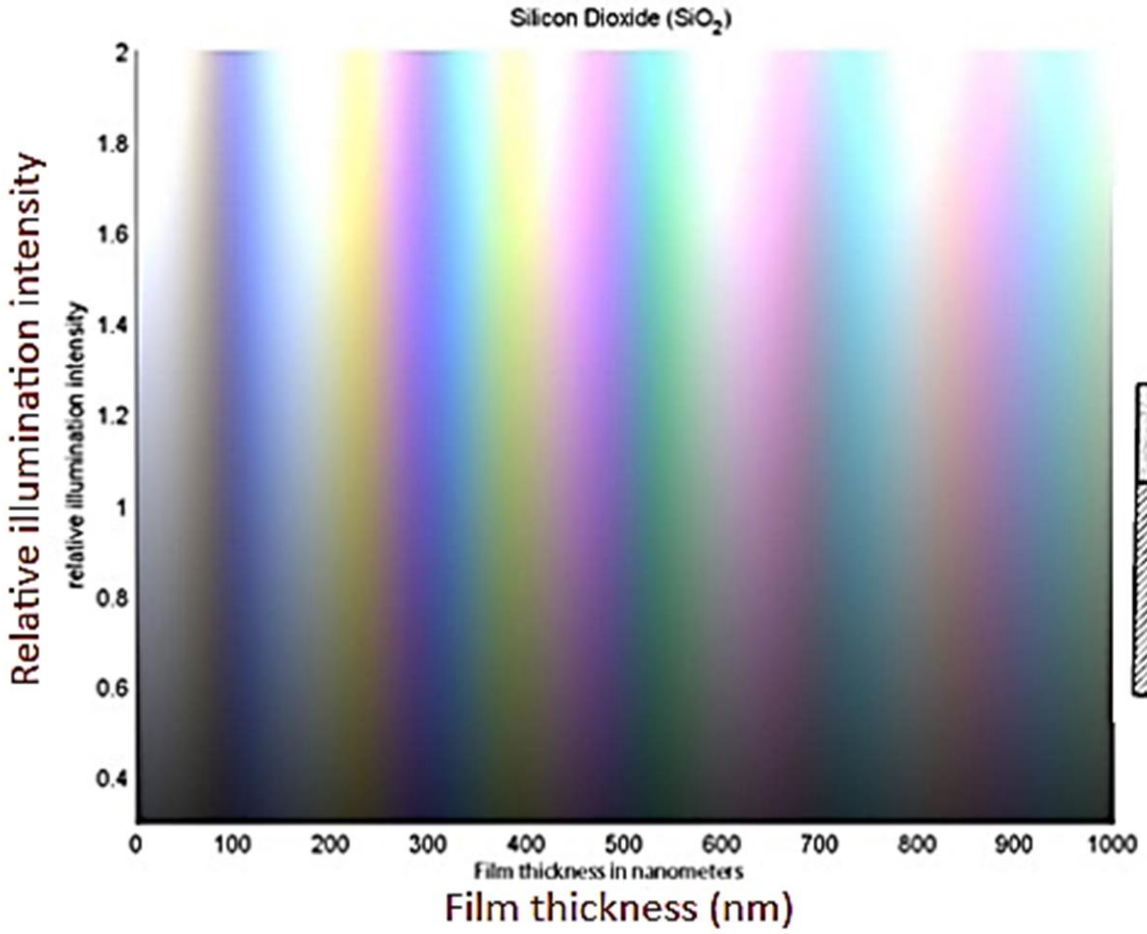


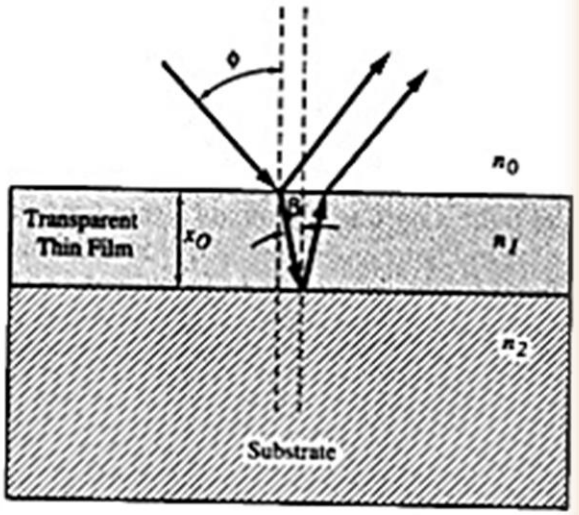
Mirror image of stylus



AFM can also be used for thickness measurement.
(AFM: atomic force microscopy)

Thickness determination by looking the color

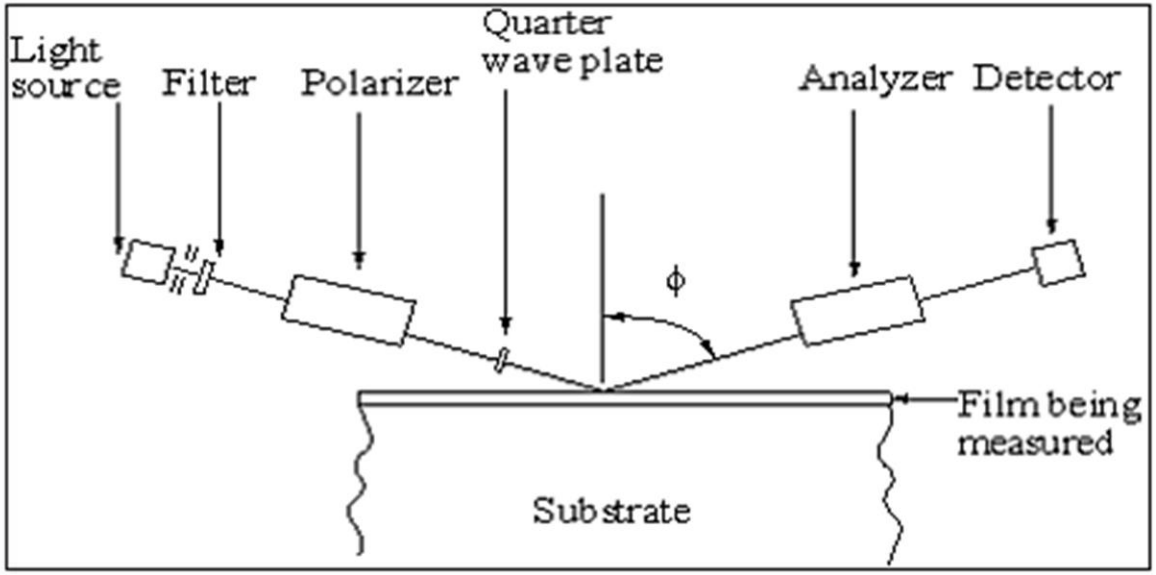




- Oxide thickness for constructive interference (viewed from above $\phi=0°$) $X_o=k\lambda/2n$, n=1.46, k=1, 2, 3…
- Our eye can tell the color difference between two films having 10nm thickness difference.

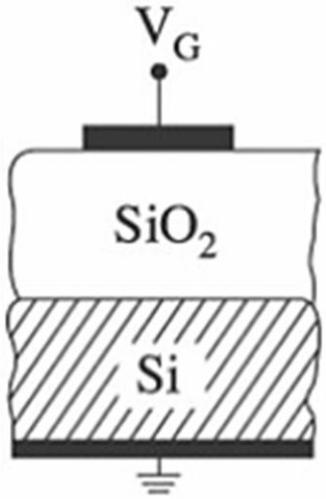
Optical thickness measurement: ellipsometry

Very accurate (1nm accuracy)

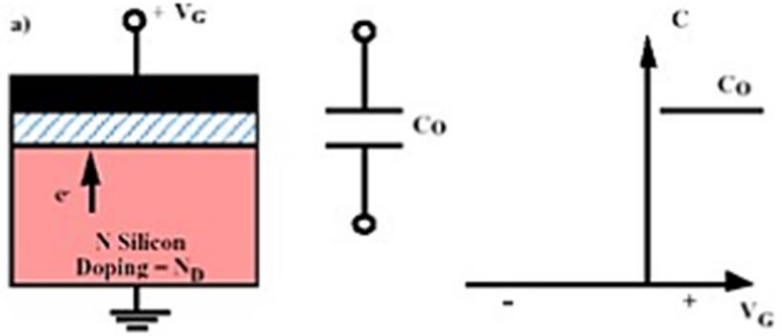


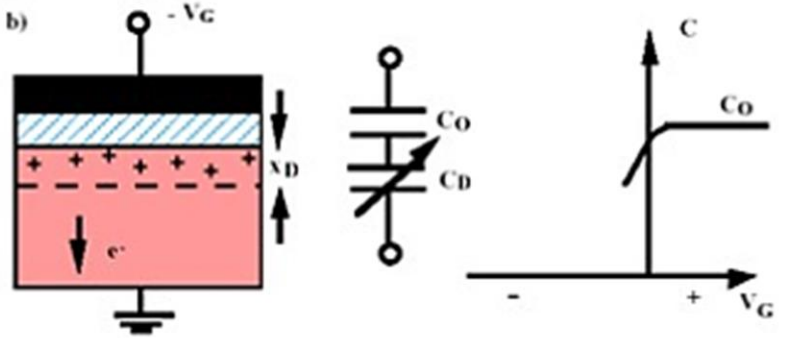
- After quarter wave plate, the linear polarized light becomes circular polarized, which is incident on the oxide covered wafer.
- The polarization of the reflected light, which depends on the thickness and refractive index (usually known) of the oxide layer, is determined and used to calculate the oxide thickness.
- Multiple wavelengths/incident angles can be used to measure thickness/refractive index of each film in a multi-film stack.

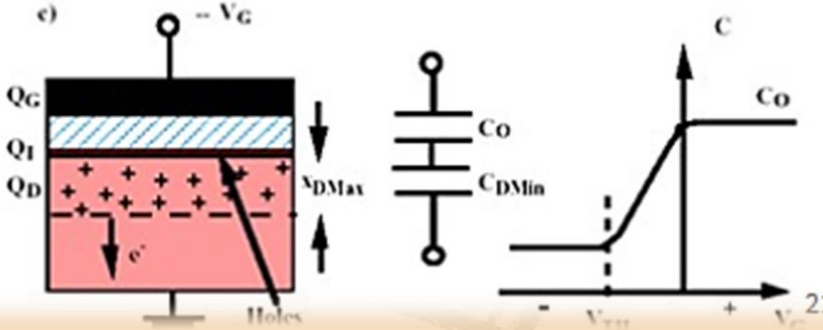
Electrical thickness measurement: C-V of MOSFET



Small *AC* voltage is applied on top of the DC voltage for capacitance measurement.







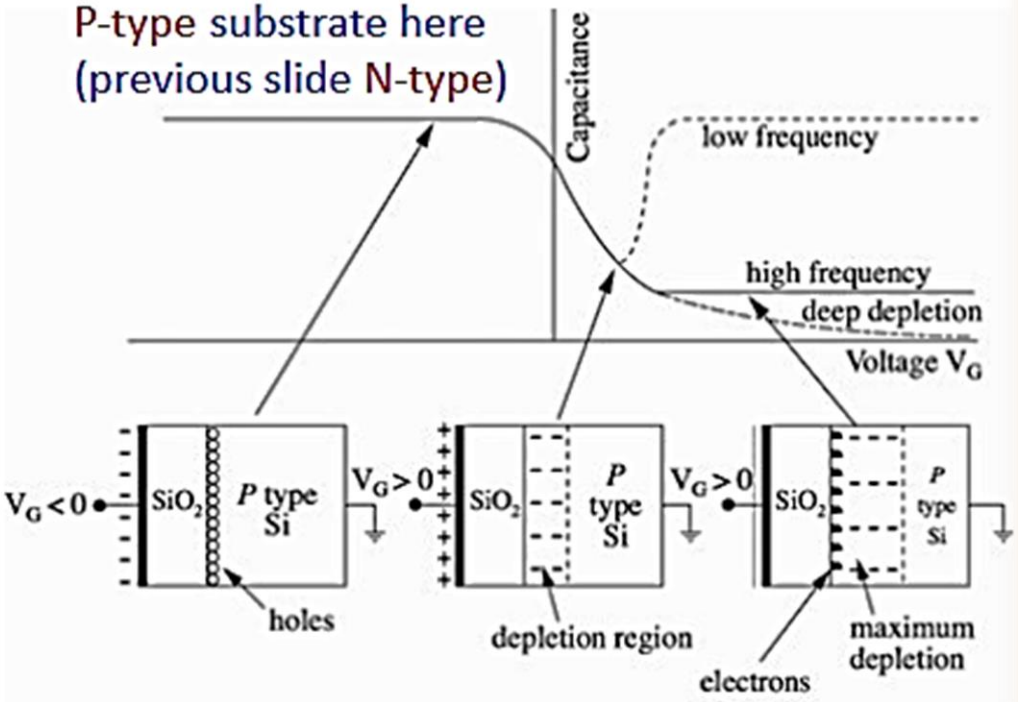
Substrate is N-type. Electron is majority carrier, hole is minority carrier.

a. Accumulation: positive gate voltage attracts electrons to the interface.

b. Depletion: negative gate bias pushes electrons away from interface. No charge at interface. Two capacitance in series.

c. Inversion: further increase (negative) gate voltage causes holes to appear at the interface.

Effect of frequency for AC capacitance measurement



$$C_{min} = \frac{C_{ox} C_{Si}}{C_{ox} + C_{Si}}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}, C_{Si} = \frac{\varepsilon_{Si}}{X_d}, X_d = \sqrt{\frac{2\varepsilon_{Si}\phi_s}{qN_a}}$$

See you on Thursday