Impact of Time-Zero and NBTI Variability on Sub-20nm FinFET Based SRAM at Low Voltages

N. Goel[1], P. Dubey[2], J. Kawa[3] and S. Mahapatra[1]**
[1]Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India
[2]Synopsys India Pvt. Ltd., NOIDA, India, [3]Synopsys, Inc., Mountain View, California, USA
(**Phone: +91-222-572-0408, Fax: +91-222-572-3707, Email: souvik@ee.iitb.ac.in)

***Abstract*— BSIM-CMG based HSPICE framework is developed for simulating time-zero and Negative Bias Temperature Instability (NBTI) variability of SRAM performance parameters. Time-zero variability of Read Static Noise Margin, Hold Static Noise Margin and Flip-Time for different process corners are simulated. Models used for SPICE simulation are foundry qualified sub-20nm FinFET for two types of 6T SRAM cells, High-Speed and High-Density cells. The Impact of stochastic BTI for DC and AC activity stress on these parameters are studied for relevant worst-case process corner. The impact of V_{DD} reduction on time-zero and post-BTI SRAM parameter variability is also studied. Critical failure situations are identified.**

Keywords- NBTI, FinFET, Variability, SRAM, SNM, Flip-Time, Reaction-Diffusion model, BSIM-CMG, HSPICE.

I. INTRODUCTION

Time-zero process variability [1], [2], [3] and stochastic Bias Temperature Instability (BTI) [4], [5], [6] are serious concerns for small-area device performance and SRAM cell reliability [7]-[13]. With technology advancement gate area reduces and new issues start appearing. For advanced nodes it is very difficult to keep initial threshold voltage (V_{T0}) of all devices same due to process variability, which is not only across different lots, wafers and dies but within a die itself. Time-zero process variability could have multiple sources such as, Line Edge Roughness (LER), Random Dopant Fluctuation (RDF), Metal Gate Grains (MGG), Gate Work-function Variability (G-WFV) etc. Yet RDF is greatly reduced for FinFET technology by low fin doping. Large variation in device parameters such as V_{T0} is reported in literature which follow Gaussian distribution [2], [3]. V_{T0} variation is very well modelled in commercial tools like TCAD [14], and SPICE [15]. However on top of time-zero variability, stochastic BTI cause additional threshold voltage shift (ΔV_T) which presumably follows gamma distribution [16], [17] whose modelling framework is not commercially available, and was recently simulated in device [13] and circuit [18] platforms using external packages to TCAD and SPICE. Note that recent reports shows either very weak or no correlation between V_{T0} and ΔV_T [19], [20].

NBTI in HKMG p-FETs was studied using mutually uncorrelated components of trap generation at Si/IL interface and IL/HK interface and hole trapping into pre-existing IL traps [21]. It is important to study impact of NBTI on circuits like SRAM cell, Ring-Oscillator (RO) and digital logic gates. Till date, impact of process and BTI variability on SRAM parameters are mostly studied in planar processes [18], [22], [23]. Due to sizing quantization, FinFET based SRAMs would offer unique process. To the best of our knowledge, impact of stochastic BTI on variability of FinFET based SRAMs for HS and HD cells for relevant worst-case process corner has not been studied. Impact on SRAM parameters before and after BTI is of interest at reduced V_{DD} (for both standby and functional modes of operation). Further, successful migration of BSIM4 based work of [18] to BSIM-CMG [24] platform is critical. In this work we choose typical 6T SRAM cell for performance evaluation as shown in Fig.1. Two types of 6T SRAM cells are used, High-Density (HD) and High-Speed (HS) cell. In HD cell, all the six FinFETs are of one fin and in HS cell p-FinFETs are of single fin while all n-FinFETs are of two fins. Time-zero variability and different process corner variations are simulated using n-FET and p-FET parameter variations by HSPICE Monte-Carlo analysis with BSIM-CMG models [24] provided by leading foundry. 6T bit-cell with and without NBTI is simulated for different AC activity factor "α" for left-latch (and "1-α" for right-latch). α= 0 implies, unstressed left p-FET and full DC stressed right p-FET. α=0.5 implies both p-FETs are AC degraded with Pulse Duty Cycle (PDC) of 50%. α=1 implies full DC stressed left pFET and unstressed right p-FET. For all the simulations internal nodes V_L and V_R are initialized to '0' and '1' respectively as shown in Fig.1. BL, BLB and WL are set to V_{DD}. Time-zero variability of SRAM performance metrics, e.g., Read Static Noise Margin (R-SNM) [25], Hold Static Noise Margin (H-SNM) [25] and Flip Time (FLT) [26] are simulated using internal Monte Carlo (MC) framework available in HSPICE.

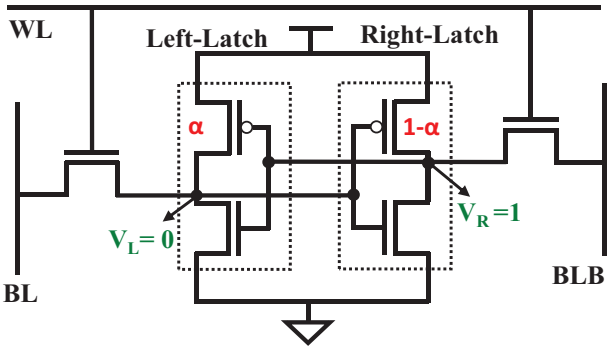

Fig.1. Schematic of 6T SRAM cell with AC activity impact **'α'** on left pFET and complementary **'1-α'** on right pFET. α=0 implies, unstressed left p-FET and full DC stress on right p-FET. **V_L** and **V_R** are internal nodal voltages of left and right latch initialized to '0' and '1' respectively.

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II. Simulation Framework

State-of-the-art foundry qualified, sub-20nm FinFET based design rules are used to design 6T HS and HD SRAM cells. Time-zero variability and process corner variations of SRAM performance matrics, e.g. Read Static Noise Margin (R-SNM), Hold Static Noise Margin (H-SNM) and Flip-Time (FLT) are simulated using internal MC framework available in HSPICE. The worst-case process corner for a particular SRAM cell performance parameter (R-SNM, H-SNM and FLT) and a particular cell type (HS and HD) is identified for time-zero variability and is chosen to study impact of NBTI variability in p-FETs; note that impact of PBTI in n-FETs is negligible [27] and therefore ignored. 6T SRAM bit-cell with NBTI is simulated for different AC activity "a" for left (and "1-a" for right) p-FET, Fig.1.

Figure 2 shows the SRAM simulation flow for NBTI variability analysis. A compact model described in [18] is used to calculate the mean ΔV_T. It is assumed that lifetime criteria of ΔV_T mean is 50mV in 10 years (~3e8s) for device under continuous DC bias condition. Due to stochastic nature of small area devices ΔV_T follows gamma distribution [17] which is centered on mean ΔV_T value. Note that gamma distribution in ΔV_T is generated using external open-source software and is added to V_{T0} distribution. V_{T0} distribution is generated by HSPICE MC simulations using foundry qualified models. After adding the two distribution (V_{T0} and ΔV_T) we get new redefined distribution of threshold voltage ($V_T = V_{T0} + \Delta V_T$). This new redefined distribution of V_T is included in HSPICE SRAM netlist for simulation of degraded SRAM cell. SRAM simulations are done on two different V_{DD}s, first at nominal V_{DD} ($V_{DD\text{-}N}$) and second at reduced V_{DD} ($2/3*V_{DD\text{-}N}$). Reduced V_{DD} simulations are done after degrading the p-FETs at $V_{DD\text{-}N}$.

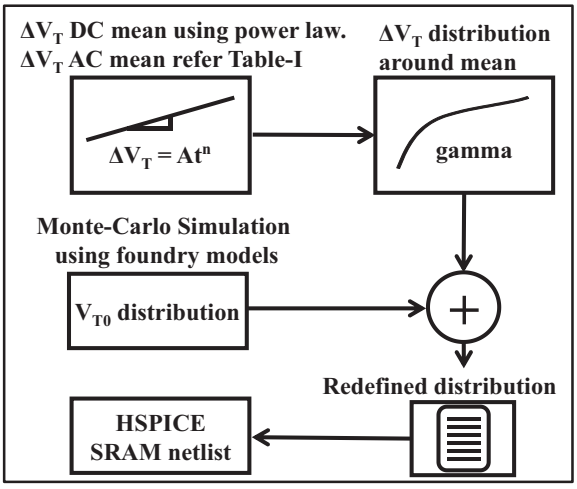

Fig.2. Simulation flow for time-zero and NBTI variability using HSPICE for SRAM cell. Gamma distribution is generated using external package.

Table-1 lists the NBTI compact model for simulating mean (μ) and distribution (σ) of ΔV_T during DC and different activity AC stress for different times. The compact model is physics based, and calculates time evolution of 'μ' (ΔV_T) by using trap generation and also considers occupancy of generated traps for AC simulation, refer to [28] for details. Hole trapping (ΔN_{HT}) into the pre-existing oxide defects is negligible for properly processed gate oxide films. So ΔN_{HT} is ignored in the present analysis and NBTI only due to ΔN_{IT} is considered. Increase in ΔN_{IT} number will cause increase in ΔV_T. Apart from number of traps, trap location (below or above Fermi level) is also important for its contribution to threshold voltage shift. During recovery or during off phase of AC stress, generated traps go below Fermi level and get neutralize after capturing electron. These traps will go structural relaxation upon electron capture and relax in energy. So, becomes inaccessible in subsequent stress phase or next on-cycle of AC stress. This we call trap disappear by electron occupancy [21].

Table-I

Compact Model equation for ΔV_T mean and distribution

$$\Delta V_{T,DC,MEAN} = A_{TECH}\, t^n\, e^{(-Ea/kT)} = \mu$$

$$\Delta V_{T,AC,MEAN} = f*(PDC)^{0.35} * \Delta V_{T,DC,MEAN}$$

f is occupancy factor [18], [21]

$$\sigma = K_{TECH}\,(\mu)^{0.5}$$

$$\Delta V_T = \text{Gamma}\,((\mu/\sigma)^2, \sigma^2/\mu)$$

To perform circuit level Monte-Carlo simulations we need suitable compact model, which incorporate occupancy and can gave us ΔV_T mean for both DC and AC stress at different time, duty factor and frequency [18]. Note that experimental results and numerical simulation shows that NBTI degradation is independent to AC frequency, but it has characteristic shape for AC stress at different duty factor [21]. For this work it is assumed that $\Delta V_{T,DC,MEAN}$ of 50mV as the failure criteria after 10 year DC stress and $\Delta V_{T,MEAN}$ of 25mV for 50% duty factor at any frequency AC stress (or AC/DC ratio of 0.5 is considered). So, A_{TECH} for 'μ' ($\Delta V_{T,DC,MEAN}$) = 5.329e-2, activation energy (Ea) = 0.1eV and temperature (T) = 350K. Power law time exponent of n = 1/6 is used as stated by RD theory [21]. For $\Delta V_{T,AC,MEAN}$ 'f' is the occupancy factor, f = 0.127 is chosen to get AC/DC ratio of 0.5 at 50% PDC.

The K_{TECH} parameter for σ (ΔV_T) is chosen to match experimental ΔV_T distribution at different stress time as shown in Fig.3 [17]. Power law time evolution is used for μ (ΔV_T) and σ (ΔV_T) with exponent n and $n/2$ respectively [16] as suggested by independent Poisson process. The model is used to first generate the ΔV_T mean values for DC stress at different times and AC stress for different activity, then distribution of 100k ΔV_T values around the mean is generated. ΔV_T distributions at long stress time for DC is shown in Fig.4 (a) and for different AC activity, Fig.4 (b). It is clear that $\Delta V_{T,MEAN}$ and ΔV_T distribution tail is increasing with increase in stress time or AC activity.

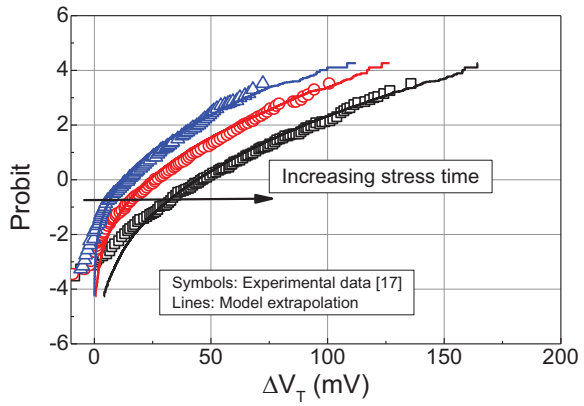

Fig.3. Measured FinFET ΔV_T distribution from [17] and its model prediction and extrapolation for 100k data points.

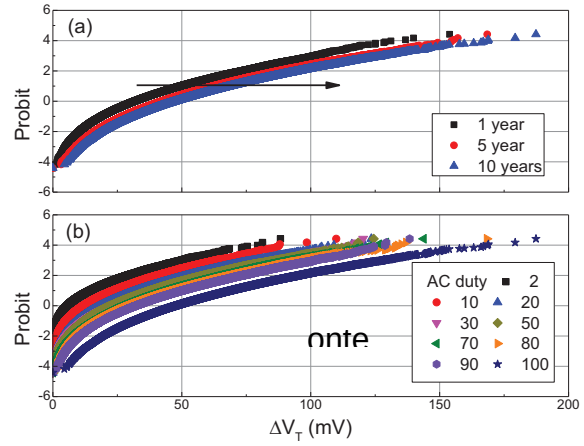

Fig.4. Mean of ΔV_T increases with stress time. ΔV_T distribution (a) after DC stress at different time (b) after AC stress at different duty.

III. Simulation Results

SRAM cell is simulated for three performance metrics (a) SNM Read (b) SNM Hold and (c) Flip time for writing into the cell. Simulations are done on both HD and HS cells at all the process corners like Typical-N-Typical-P (TT), Fast-N-Slow-P (FN-SP), Slow-N-Fast-P (SN-FP), Slow-N-Slow-P (SN-SP) and Fast-N-Fast-P (FN-FP). Worst-case process corner is identified for each performance parameter and for both types of cells. Apart from process variation, simulations are also performed at two different V_{DD} bias, nominal V_{DD} ($V_{DD\text{-}N}$) and $2/3*V_{DD}$ nominal ($2/3*V_{DD\text{-}N}$), temperature is kept constant (350K) for all the simulations. Note that, for reduced V_{DD} simulations it is assumed that NBTI degradation occurs at nominal V_{DD} ($V_{DD\text{-}N}$) and then V_{DD} is reduced for observing the bit-cell performance.

Figure 5. shows the schematic of SRAM cell for Read SNM (R-SNM) analysis [25]. Two noise sources are connected to internal nodes as shown. For calculating noise margin both voltage sources are varied from 0V to V_{DD} and R-SNM is equal to the minimum voltage at which internal nodes got flipped (crosses $V_{DD}/2$ point). R-SNM analysis is performed on both types of cells (HD and HS) for all the process corners and it is observed that FN-SP is the worst case process corner for both types of cells. It is observed that worst-case process corner does not change after NBTI. Bit-Line (BL), Bit-Line Bar (BLB) and Word-Line (WL) are set to V_{DD} (logic '1').

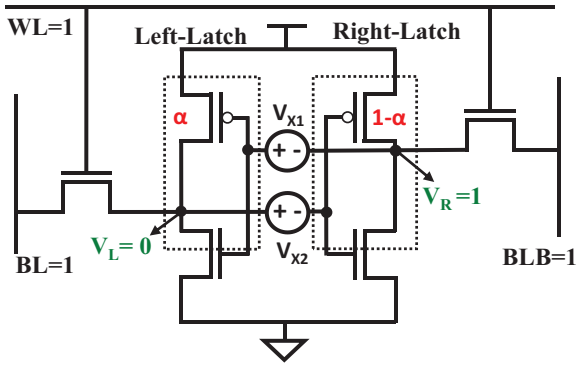

Fig. 5. Schematic of 6T SRAM cell for performing Read SNM (R-SNM) during cell read. WL, BL and BLB are kept at logic '1'.

Figure 6 (a) shows distribution of 100k MC simulation of R-SNM distribution for HD 6T SRAM cell at time-zero, DC NBTI (α=0) and 50% AC NBTI (α=0.5) for two different V_{DD} conditions ($V_{DD\text{-}N}$ and $2/3*V_{DD\text{-}N}$). It is shown that R-SNM degrades with NBTI. Note that R-SNM degradation is more for 'α' = 0 (i.e. when imbalance in degradation of two pMOS is maximum). Note that R-SNM decreases drastically at reduced V_{DD} condition (at $2/3*V_{DD\text{-}N}$). In both the bias conditions sigma increases with reduction in mean value of R-SNM. This suggests that R-SNM is best at higher V_{DD} and at balanced degradation (α=0.5) of two pMOS. Similar results are observed for HS cell, Fig.6 (b) shows reduced mean and increased sigma of R-SNM with NBTI.

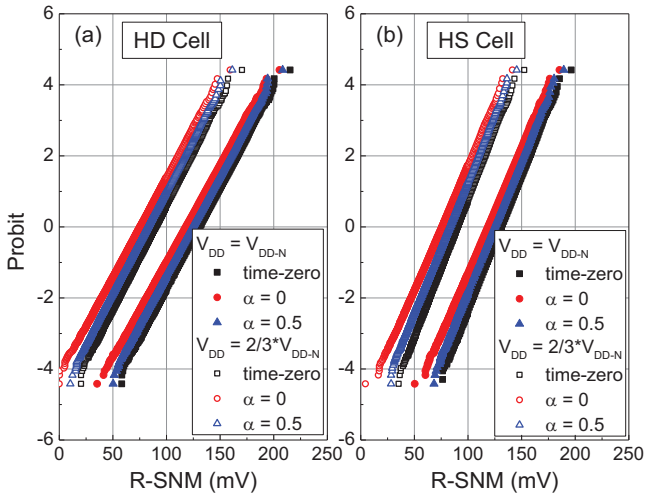

Fig.6 Distribution of 100k MC simulations for time-zero and NBTI impacted R-SNM at nominal operating Voltage ($V_{DD\text{-}N}$) and $2/3*V_{DD\text{-}N}$ for (a) High Density cell (b) High Speed cell.

Figure 7. shows mean and sigma at different activity factor 'α' for R-SNM, normalized to time-zero value of HD and HS cell at $V_{DD\text{-}N}$ and $2/3*V_{DD\text{-}N}$. NBTI results in gradual decrease

in ‘μ’ (R-SNM) and increase in ‘σ’ (RSNM) with increase is asymmetric degradation of two PMOS. Increased asymmetry in AC activity (e.g., lower “α”) results in larger reduction in ‘μ’, Fig.7a, and larger increase in ‘σ’, Fig.7b. HD and HS cell shows similar time-zero ‘μ’ (R-SNM) magnitude, while HS cells have marginally better time-zero ‘σ’ (R-SNM) but show larger fractional increase of ‘σ’ due to NBTI when compared to HD cells. Note that degradation in ‘μ’ and ‘σ’ are higher at lower V_{DD} (after NBTI stress at nominal V_{DD}). Higher failure of R-SNM is observed in HS cells for DC BTI at lower read V_{DD}. For worst case R-SNM degradation (i.e. at α = 0), ‘μ’ is reduced by 10% and ‘σ’ is increased by 7% for V_{DD-N}, while at $2/3*V_{DD-N}$ ‘μ’ is reduced by 16% and ‘σ’ is increased by 9%. This clearly states that R- SNM get worse at reduced V_{DD}.

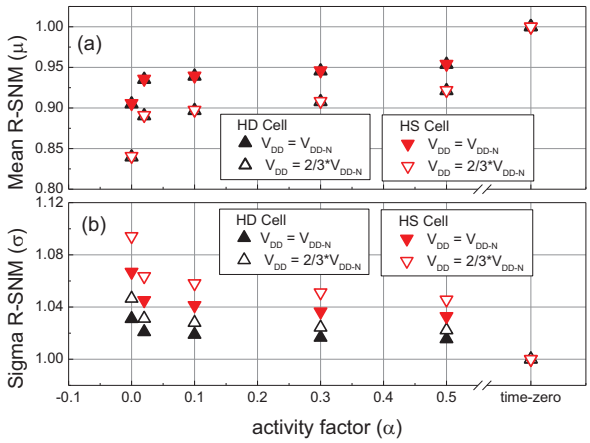

Fig.7. (a) Mean (b) Sigma of R-SNM for HD and HS cell at two different voltages normalized to their respective time-zero values.

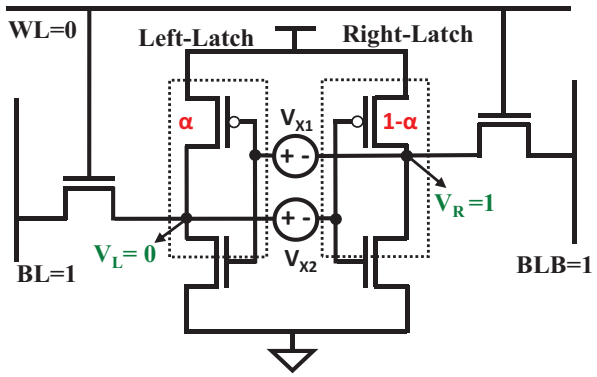

Fig. 8. Schematic of 6T SRAM cell for performing Hold SNM (H-SNM) during cell read. WL is kept at logic ‘0’ in this case rest all is same as R-SNM.

Figure 8 shows the schematic of SRAM cell for Hold SNM (H-SNM) analysis. Two noise sources are connected to internal nodes as shown [25]. For calculating noise margin both voltage sources are varied from 0V to V_{DD} and H-SNM is equal to the minimum voltage at which internal nodes got flipped (crosses $V_{DD}/2$ point). H-SNM analysis is performed on both types of cells (HD and HS) for all the process corners and it is observed that FN-SP is the worst case process corner for both types of cells. It is observed that worst-case process corner does not change after NBTI. Bit-Line (BL) and Bit-Line-Bar (BLB) are set to V_{DD} (logic ‘1’) and Word-Line (WL) is set to Ground (logic ‘0’). Study of H-SNM is important because most of the time SRAM cell remains in this state.

Fig.9 (a) shows distribution of 100k MC simulation of H-SNM distribution for HD 6T SRAM cell at time-zero, DC NBTI (α=0) and 50% AC NBTI (α=0.5) for two different V_{DD} conditions (V_{DD-N} and $2/3*V_{DD-N}$). H-SNM at lower V_{DD} is of importance as reduced V_{DD} is commonly used to save power during standby. It is shown that H-SNM not only degrades with NBTI but degrades more with increased imbalance in degradation (i.e. at lower ‘α’ or higher mismatch of degradation between two pMOS devices). Note that H-SNM decreases drastically at reduced V_{DD} condition (at $2/3*V_{DD-N}$). In both the bias conditions sigma increases with reduction in mean value of H-SNM. This suggests that H-SNM is best at higher V_{DD} and at balanced degradation (α=0.5) of two pMOS. Similar results are observed for HS cell, Fig.9 (b) shows reduced mean and increased sigma of H-SNM with NBTI.

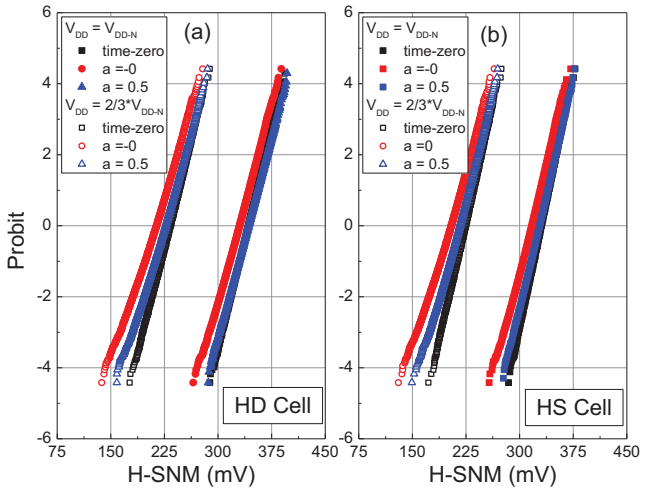

Fig.9 Distribution of 100k MC simulations for time-zero and NBTI impacted H-SNM at nominal operating Voltage (V_{DD-N}) and $2/3*V_{DD-N}$ for (a) High Density cell (b) High Speed cell.

Figure 10 shows mean and sigma at different activity factor ‘α’ for H-SNM, normalized to time-zero value of HD and HS cell at V_{DD-N} and $2/3*V_{DD-N}$. NBTI results in gradual decrease in ‘μ’ (R-SNM) and increase in ‘σ’ (RSNM). Increased asymmetry in AC activity (e.g., lower “α”) results in larger reduction in ‘μ’ Fig.10a, and larger increase in ‘σ’ Fig.10b. HD and HS cell shows similar time-zero ‘σ’ (H-SNM) magnitude, while HS cell shows marginally better time-zero ‘μ’ (H-SNM) but HS cell show larger fractional increase of ‘σ’ due to NBTI when compared to HD cells. Note that degradation in ‘μ’ and ‘σ’ are higher at lower V_{DD} (after NBTI stress at nominal V_{DD}). Higher failure of H-SNM is observed in HS cells for DC BTI at lower hold V_{DD}. For worst case H-SNM degradation (i.e. at α = 0), ‘μ’ is reduced by 4% and ‘σ’ is increased by 10 to 15% for V_{DD-N}, while at $2/3*V_{DD-N}$ ‘μ’ is reduced by 9% and ‘σ’ is increased by 25% to 30%. This clearly states that H-SNM get worse at reduced V_{DD}. HS cell shows higher ‘σ’ (H-SNM) degradation

compared to HD cell. Note that H-SNM has somewhat lower 'μ' degradation but significantly higher 'σ' degradation compared to R-SNM for both HS and HD cells. Unlike R-SNM, H-SNM at low V_{DD} is not a big concern. But for H-SNM increase in 'σ' for worst-case (α = 0) is very high in comparison to R-SNM.

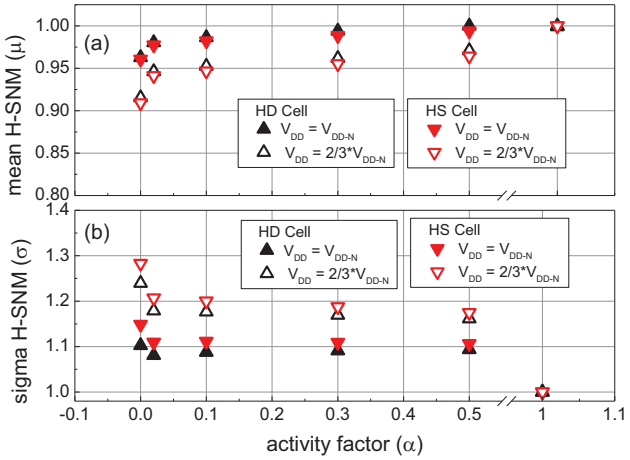

Fig.10 (a) Mean (b) Sigma of H-SNM for HD and HS cell at two different voltages normalized to respective time-zero value.

Flip-time is the measure of time taken by internal nodes to change its state when WL and BL are high and BLB is falling [26]. Fig.11 shows the schematic of SRAM cell for Flip-Time analysis. Bit-Line (BL) is set to V_{DD} (logic '1') and Bit-Line Bar (BLB) is swept from V_{DD} to Ground while Word-Line (WL) is kept at V_{DD}. Two internal nodes are initialized to logic '0' and logic '1' respectively as shown in Fig. 11. For calculating Flip-Time, the time taken by the internal nodes to reach 90% of V_{DD} (for left node) and time taken to reach 10% of Ground (for right node) is calculated and Flip-Time of bit cell is the maximum of these two times [26]. Flip-time analysis is performed on both types of cells (HD and HS) for all the process corners at two different bias conditions. Note that for all the simulations results Flip-Time is normalized to a constant arbitrary value.

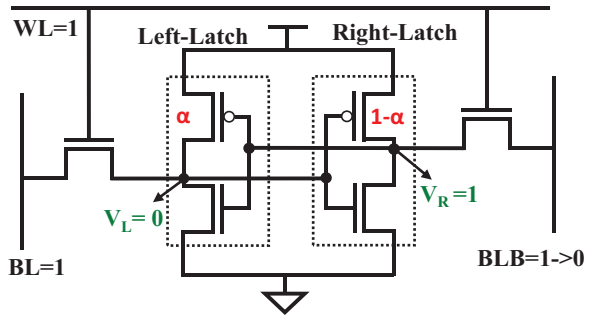

Fig.11. Schematic of 6T SRAM cell for performing Flip-time (FLT) analysis during write operation. BLB is swept from logic '1' to logic '0'.

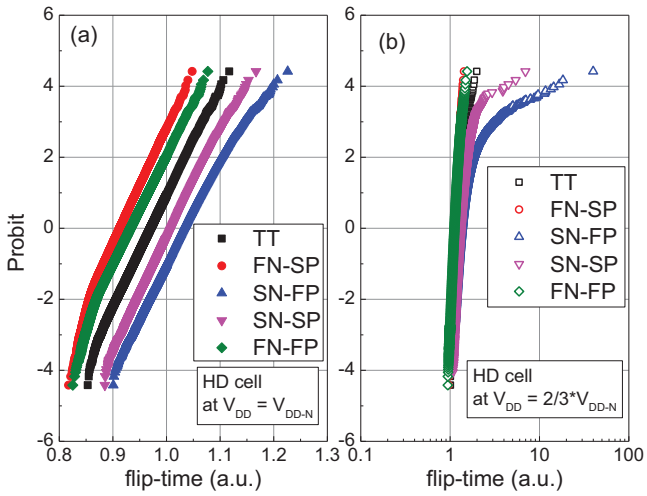

Fig.12. Time-zero flip time at different process corners of High-Density cell at (a) V_{DD-N} and (b) $2/3*V_{DD-N}$. Note log scale for right figure.

Fig.12 (a) shows time-zero distribution of 100k Monte-Carlo simulations for flip-time of HD cells at V_{DD-N} and Fig.12 (b) at $2/3*V_{DD-N}$ for all process corners. It is clear that SNFP is the worst-case process corner for HD cells. At low V_{DD} ($2/3*V_{DD-N}$) flip-time has very long distribution tail at worst-case corner, note the logarithmic scale in Fig.12 (b). This long tail distribution becomes even worse after NBTI for certain α, see Fig.13, and some cells do not flip in the required time and thus counted as failure cases, shown by circle in Fig.13 (b). Note that flip-time reduces for α=0 and α=0.5 while for α=1 flip-time increases. This is because in simulation setup we are pulling down BLB and V_R is initialized to logic '1'. So left pFET has to pull up V_L from '0' to '1'.

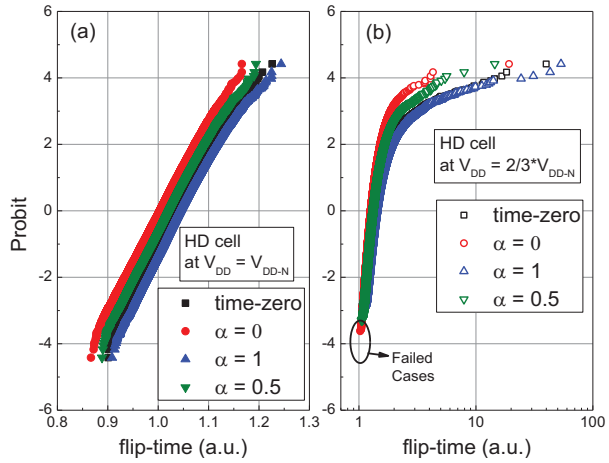

Fig.13. Time-zero and NBTI impacted flip-time for different activity at worst-case process corner (SN-FP) of High-Density cell at (a) V_{DD-N} and (b) $2/3*V_{DD-N}$. Note log scale for right figure and absence of data points due to measurement failure cases. Flip-time is measured with initialized internal nodal voltages as shown in Fig.11.

Figure 14 shows time-zero distribution of 100k MC simulations for flip-time of HS cells for different V_{DD} and

process corners; for HS cell, the worst-case corner is SN-SP. At lower V_{DD}, time-zero flip-time for SN-SP corner is slightly skewed for HS cells, unlike the long tail seen for HD cells. However, after NBTI for certain 'α', flip-time at lower V_{DD} also has long distribution tail, Fig.15). Note that for HS cell Flip-Time reduces for α=0 while for α=0.5 and α=1 flip-time increases. Distributions of Flip-Time at time-zero and after BTI shows similar shapes at V_{DD-N} for both HD and HS cells, only the worst and best-case process corners are changed. At reduced V_{DD} maximum Flip-Time for HS cell can increase by roughly two times, but it does not show any failure like HD cell. These observations shows very different impact of NBTI on HS and HD cell.

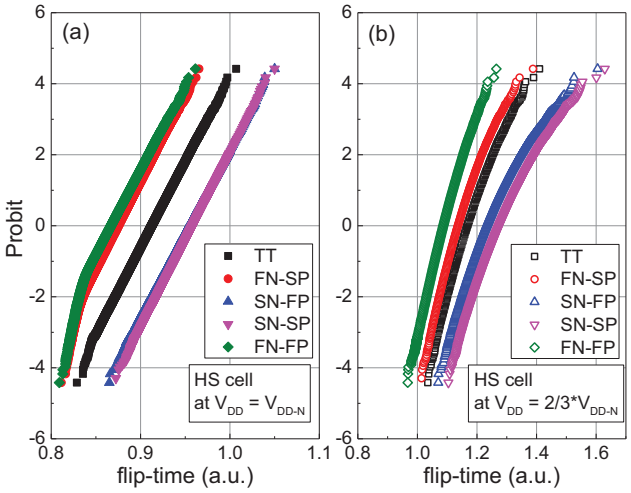

Fig.14. Time-zero flip time at different process corners of High-Speed cell at (a) V_{DD-N} and (b) $2/3*V_{DD-N}$.

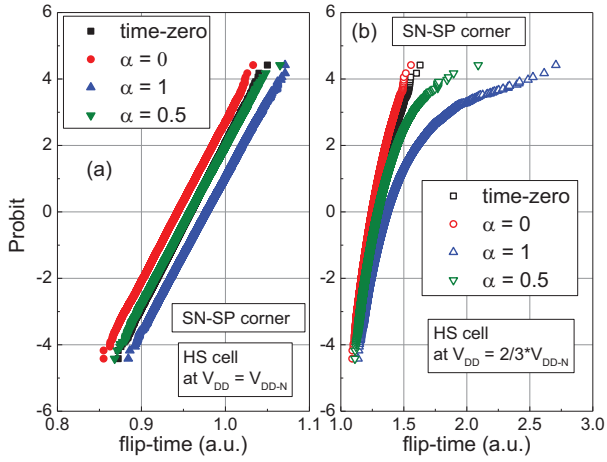

Fig.15. Time-zero and NBTI impacted flip-time for different activity at worst-case process corner (SN-SP) of High-Speed cell at (a) V_{DD-N} and (b) $2/3*V_{DD-N}$.

IV. Conclusion

Impact of process and NBTI variability on SRAM performance variability is simulated at nominal and reduced V_{DD} using sub-20nm foundry-calibrated FinFET models. Worst-case process corners for R-SNM, H-SNM and Flip-time for 6T HS and HD cells are identified. NBTI variability on worst-case process corners is simulated for DC and different activity AC stress by a novel HSPICE based BSIM-CMG framework. Vulnerability of HD cells especially for R-SNM and Flip-time at reduced V_{DD} is observed. Therefore, special design techniques would be required to achieve high yield.

Acknowledgment

Synopsys for providing internship opportunity to Nilesh Goel.

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