# EE618 (Zele)

CMOS Analog VLSI Design: Homework - 4 (30 - Marks)

Submission Deadline: 30th Sept 2019 11:55 AM

- $\bullet$  All problems are based on Cadence simulations. Use Vdd = 1.8 V
- The submission must contain appropriate plots labelled clearly.
- The submission must contain the theoretical calculations wherever it is applicable.
- Submission must be in *Teamname\_Rollnumber\_Yourname\_Assignment4.pdf* format.
- Submissions after deadline with not be accepted under any circumstances.
- All MOSFET models should be used from SCL 180 nm library.
- MOSFETS in schematics must be annotated with all required parameters. Ex: Width, Length, Fingers, Multipliers.
- Report all values preferably in tabular format wherever it is appropriate.

# Question 1

### Understanding the flicker and thermal noise of MOSFETs

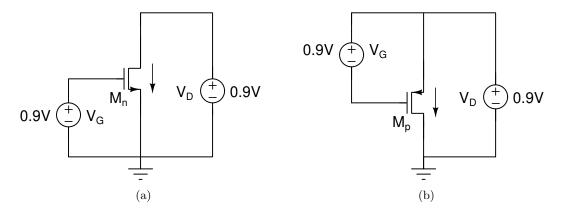


Figure 1

Consider the following cases:

- Case A for Fig. 1.a):  $(W/L) = (2.2\mu m/0.18\mu m) \times 5$  multipliers
- Case B for Fig. 1.a):  $(W/L) = (2.2 \mu m/0.36 \mu m) \times 10 \text{ multipliers}$
- Case C for Fig. 1.b):  $(W/L) = (2.2\mu m/0.18\mu m) \times 5$  multipliers
- a) For all the above cases, Overlay the plots of the noise current flowing through the transistor in the frequency range of 1Hz to 10GHz. The X-axis (frequency with 100 points/decade) and Y-axis (noise current magnitude in  $A/\sqrt{Hz}$ ) should be in logarithmic scale. [3 Marks]
- b) Report the approximate corner frequency ( $f_c$ ). (You may consider the knee region of the curve as  $f_c$ ) [3 Marks]

|        | Corner frequency $(f_c)$ |
|--------|--------------------------|
| Case A |                          |
| Case B |                          |
| Case C |                          |

Which of the above cases has the lowest thermal noise and why? Which case would you prefer to design an OTA with low flicker noise and why? [2 Marks]

## Question 2

#### Understanding the noise in amplifiers

**A.** For the CS amplifier shown in Fig. 2, perform the noise analysis in the frequency range of 1Hz to 10GHz for the following cases:

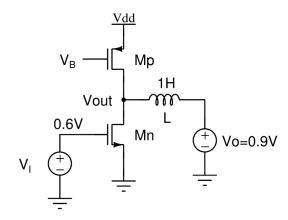


Figure 2: CS amplifier with PMOS current source load

- Case A:  $(W/L)n = (2\mu m/0.18\mu m) \times 4$ ,  $(W/L)p = (2\mu m/0.18\mu m) \times 2$ ,  $V_b = 0.9V$
- Case B:  $(W/L)n = (2\mu m/0.18\mu m) \times 2$ ,  $(W/L)p = (2\mu m/0.18\mu m) \times 9$ ,  $V_b = 1.2V$

**Note:** The inductor is added to provide a DC bias at the output node. Large inductance offers low impedance near DC.

a). Report the noise contributions at 200MHz. [3 Marks]

| Spot Noise @ 200 MHz           | Case A (in $V/\sqrt{Hz}$ ) | Case B (in $V/\sqrt{Hz}$ ) |
|--------------------------------|----------------------------|----------------------------|
| Total Noise @ output due to Mn |                            |                            |
| Total Noise @ output due to Mp |                            |                            |
| Input referred noise           |                            |                            |

- Which case has the low input referred noise voltage? Justify your answer with appropriate expressions for input referred noise of the CS amplifier shown in Fig. 2. [3 Marks]
- **B.** For the following cascode amplifier, perform the noise analysis in the frequency range of 1Hz to 10GHz and tabulate the following. [4 Marks]

Given, 
$$(W/L)_1 = (2\mu m/0.18\mu m) \times 3$$
,  $(W/L)_2 = (2\mu m/0.18\mu m) \times 3$ 

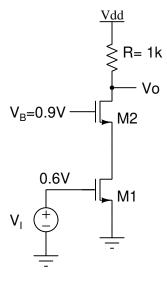


Figure 3: Cascode amplifier

| Spot Noise @ 200MHz            | Noise (in $V/\sqrt{Hz}$ ) | % of total |
|--------------------------------|---------------------------|------------|
| Total Noise @ output due to M1 |                           |            |
| Total Noise @ output due to M2 |                           |            |
| Total Noise @ output due to R  |                           |            |
| Input referred noise           |                           |            |

- What is the effect of noise of M2 on the input referred noise? Justify your answer with the appropriate expressions for the noise of a cascode amplifier. [3 Marks]
- C. Perform the noise analysis for the following differential amplifier in the frequency range of 1Hz to 10GHz.

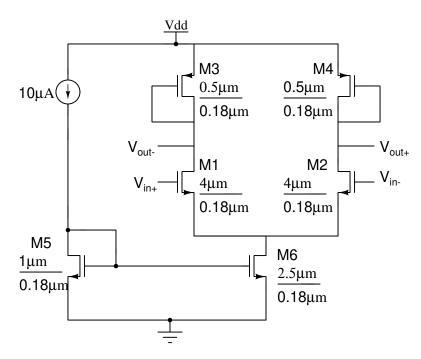


Figure 4: Differential Amplifier

**Note:** Apply an input DC Common Mode voltage of 1.1 V without any AC input. Use the following format for tabulation for C.a) and C.b).

| Transistor           | Type    | Noise (in $V^2$ ) | % of total |
|----------------------|---------|-------------------|------------|
| M1                   | Flicker |                   |            |
| M1                   | Thermal |                   |            |
| •                    |         |                   |            |
| •                    |         |                   |            |
| M6                   | Flicker |                   |            |
| M6                   | Thermal |                   |            |
| Total Noise          |         |                   |            |
| Input referred noise |         |                   |            |

- a) Tabulate the noise summary by measuring the noise values at the output in a single ended manner (i.e. at  $V_{out+}$  w.r.t ground) integrated in bandwidth of interest from 10kHz to 10MHz. Report the major contributor to output referred noise in this case? [4 Marks]
- b) Tabulate the noise summary by measuring the noise values at the output in a differential manner (i.e. at  $V_{out+}$   $V_{out-}$ ) integrated in bandwidth of interest from 10kHz to 10MHz. Report the major contributor to to output referred noise in this case? [4 Marks]
  - What is the contribution of the tail current source to the total output noise? Explain your observation. [1 Mark]

Let's make some noise ©