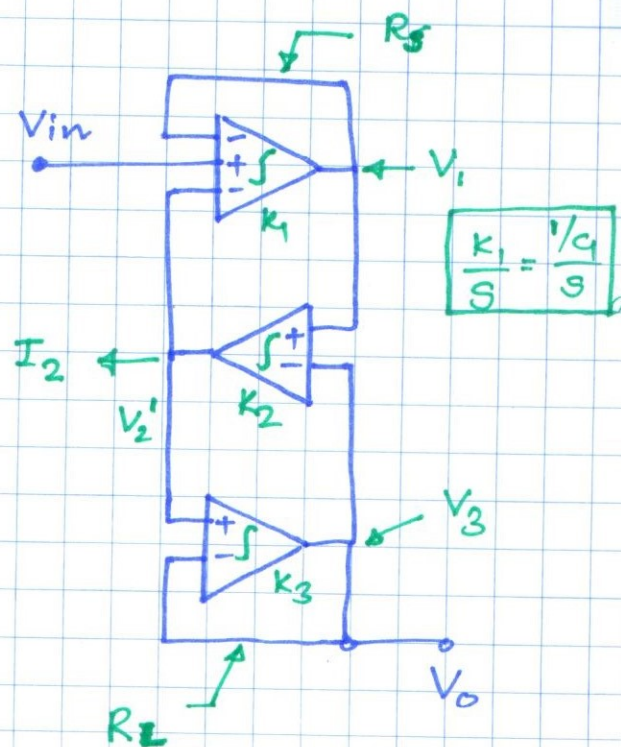
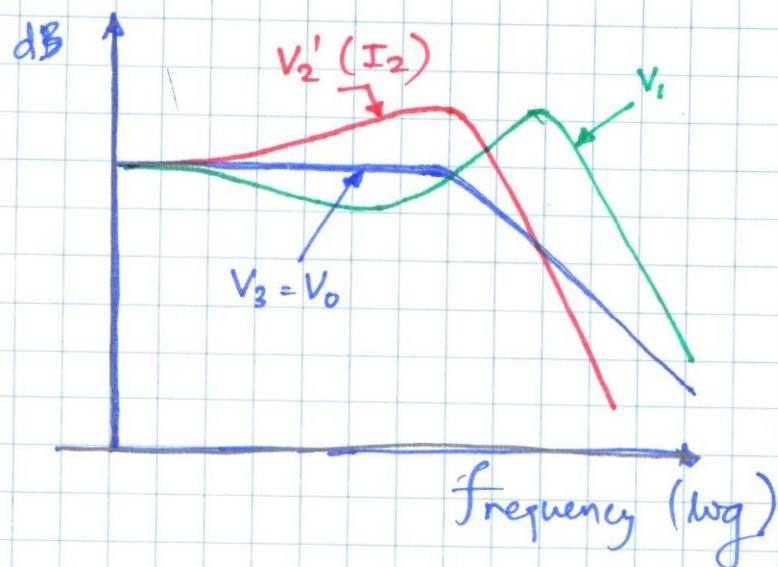
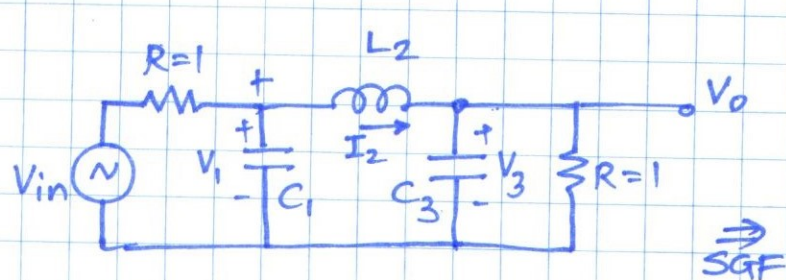


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$$\frac{K_i}{S} = \frac{1/C_i}{S}$$

Observing voltages internally, V_1 & V_2' are about 3.2 dB higher than V_o . (Based on SPICE simulations)

→ Optimal voltage swing @ each integrator output — Depends on V_{DD} .

→ Since V_1 & V_2' are 3.2 dB higher, max o/p voltage swing is reduced by 3.2 dB. [specific to our current example]

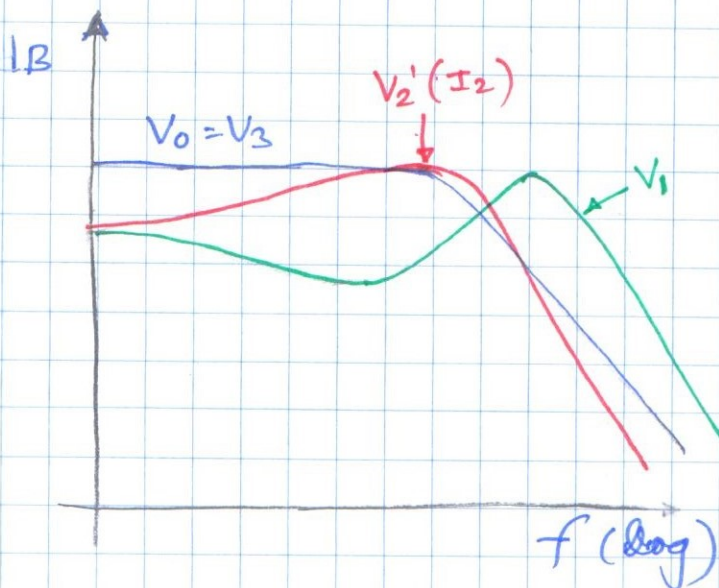
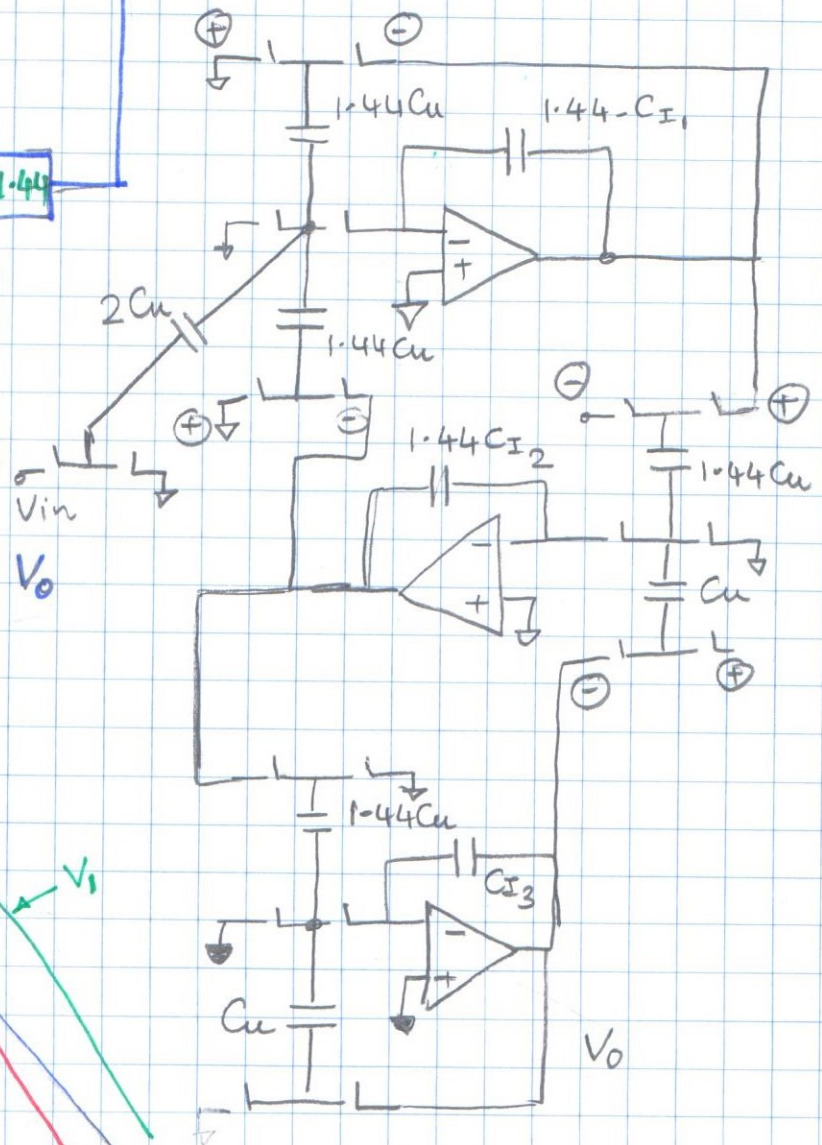
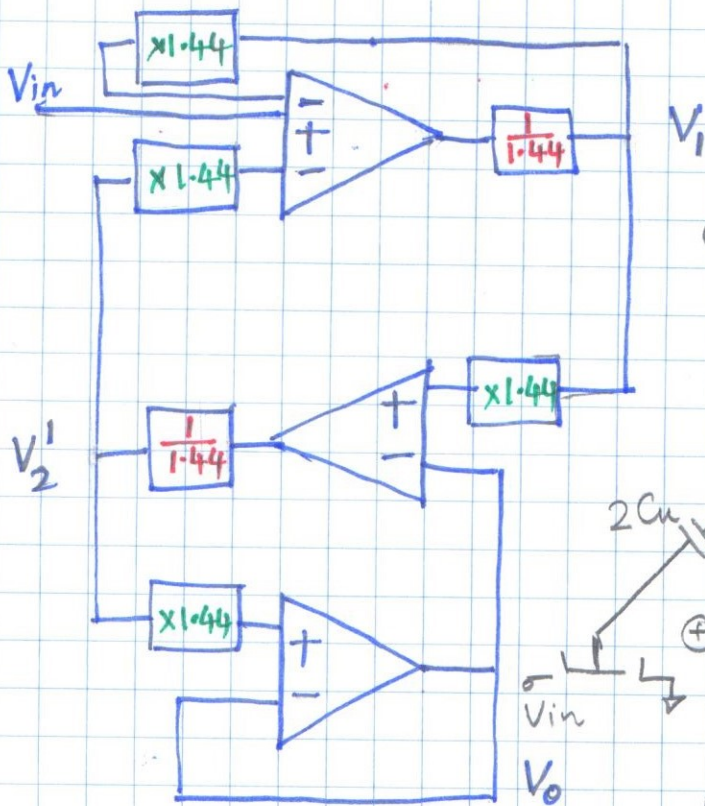
→ Else Distortion will result.

→ Need to do voltage swing equalization at each integrator o/p. { Same peak amplitude for each stage

→ Also Called Dynamic Range Scaling.

→ Applicable to continuous-time filters also.

- Need to attenuate V_1 & V_2' by 3.2 dB ($\frac{1}{1.44}$) WITHOUT changing overall xfer function.
- How?

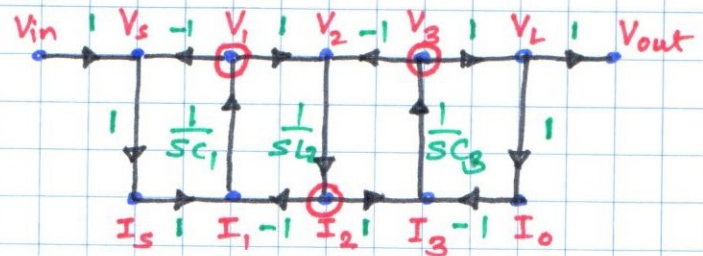
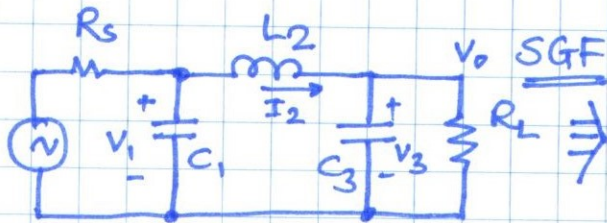


→ peak swings of all integrators equalized.

Another way to explain Voltage Swing Equalization

Start with RLC filter

Refer: L-20 page 6



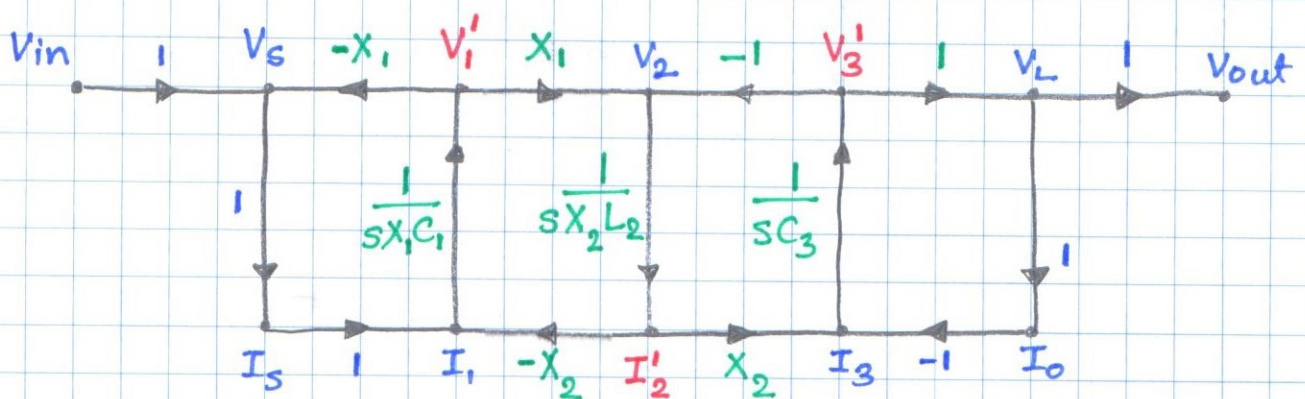
→ Simulate RLC circuit using SPICE → Determine peak gain for each variable representing INTEGRATOR OUTPUT.

For example: In this case V_1 , I_2 & V_3 (Same as V_0)

$$\frac{V_1}{V_{out}} = X_1 \quad ; \quad \frac{I_2}{V_{out}} = X_2 \quad ; \quad \frac{V_3}{V_{out}} = 1$$

X_1 & $X_2 > 1$ → Need to scale Integrator 1, 2
(Represent Peak values) So that peak gain for all integrator o/p's is same.

Modified SGF implementation

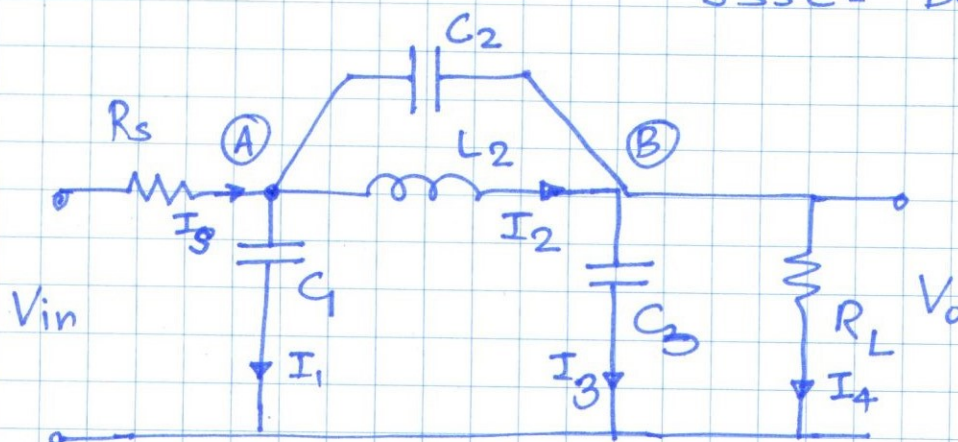


$$V_1' = \frac{V_1}{X_1} \quad ; \quad I_2' = \frac{I_2}{X_2}$$

Now all integrator o/p's will have same peak values (may be at different frequencies)
→ Optimum dynamic range

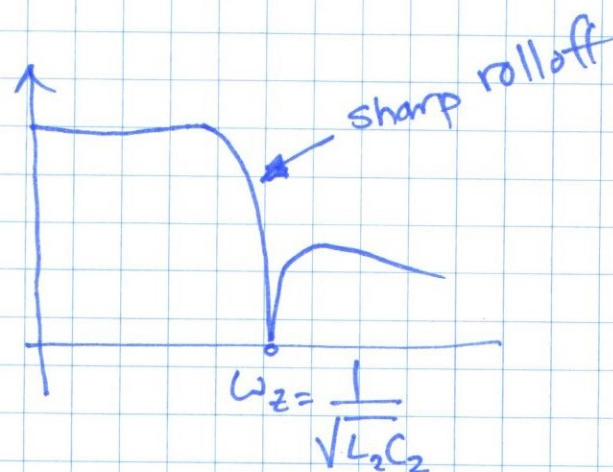
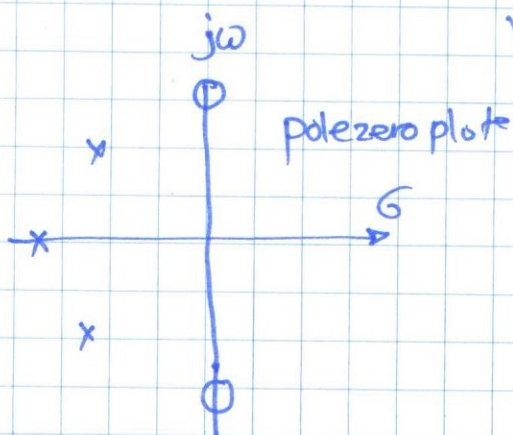
Implementing finite transmission zeros

Ref: Allstot "MOS SC Ladder Filters"
JSSC - Dec 1978.



Tx zero @ resonance of $L_2 C_2$

$$\omega_{\text{zero}} = \frac{1}{\sqrt{L_2 C_2}}$$



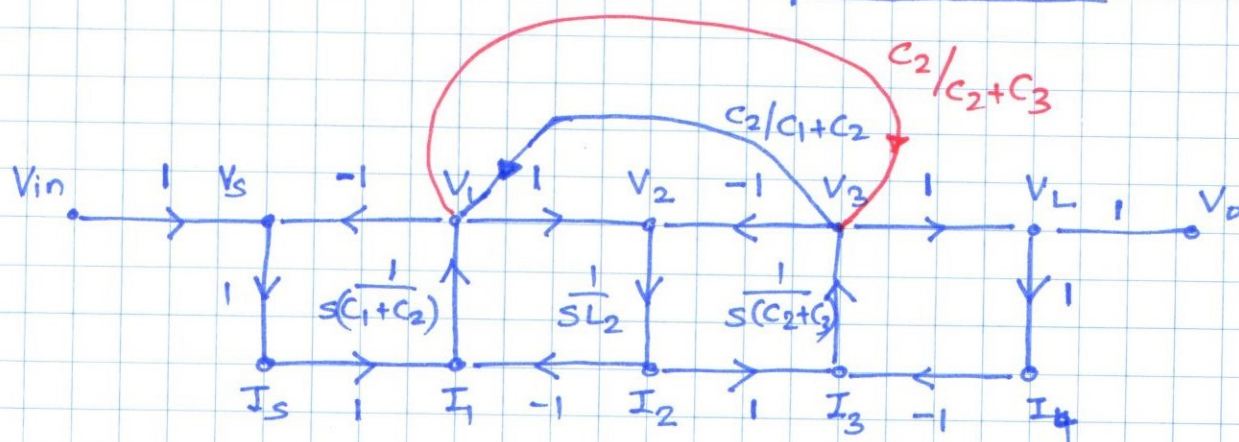
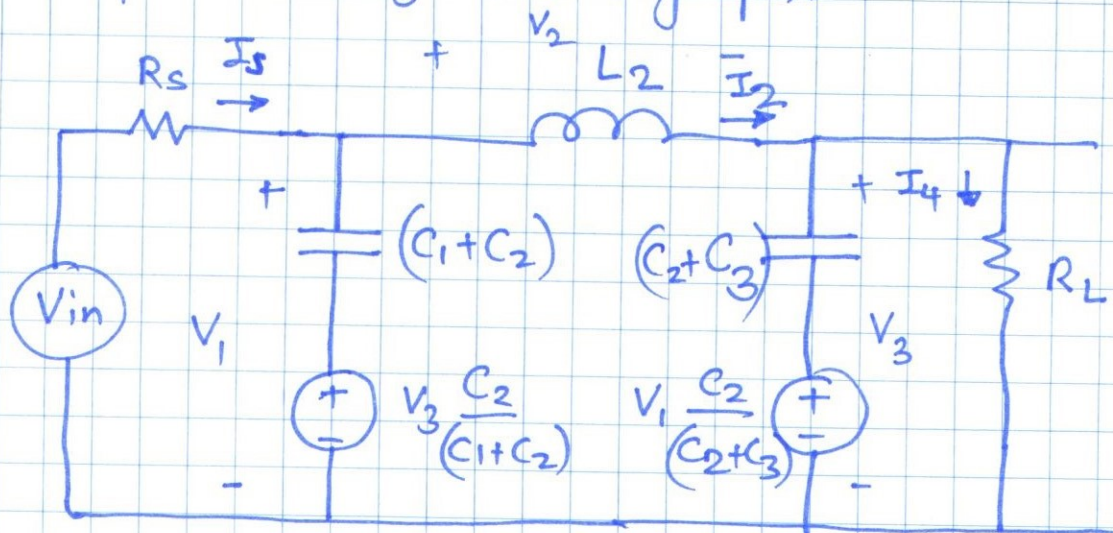
KCL @ (A) $I_9 = sC_1 V_1 + sC_2 (V_1 - V_3) + I_2$

$$V_1 = \underbrace{\frac{I_9 - I_2}{s(C_1 + C_2)}}_{\text{Integration}} + \underbrace{V_3 \frac{C_2}{(C_1 + C_2)}}_{\text{Addition}}$$

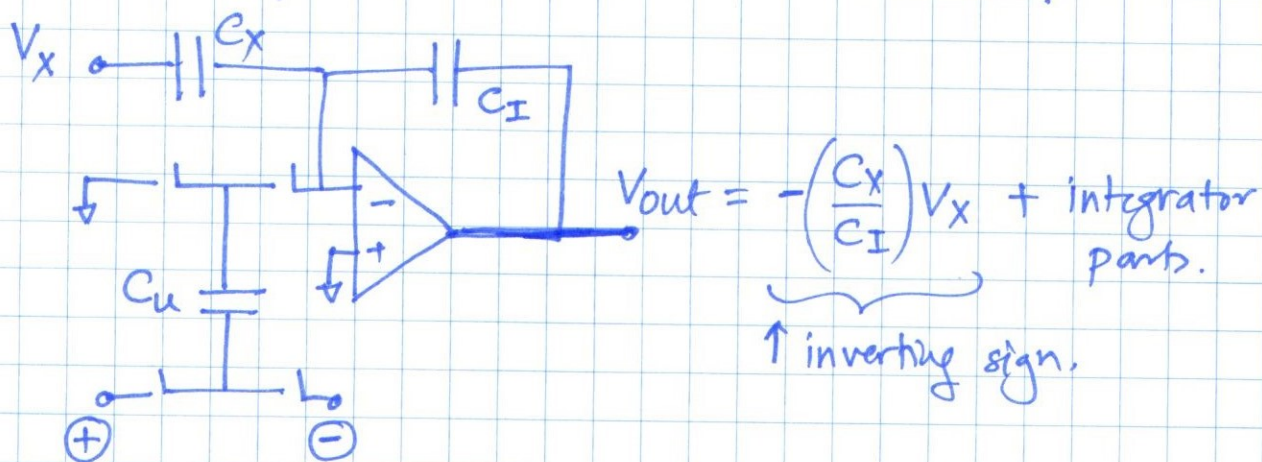
KCL @ (B) $I_2 = I_4 + sC_3 V_3 + sC_2 (V_3 - V_1)$

$$V_3 = \frac{I_2 - I_4}{s(C_2 + C_3)} + V_1 \frac{C_2}{C_2 + C_3}$$

Update Signal flow graph.

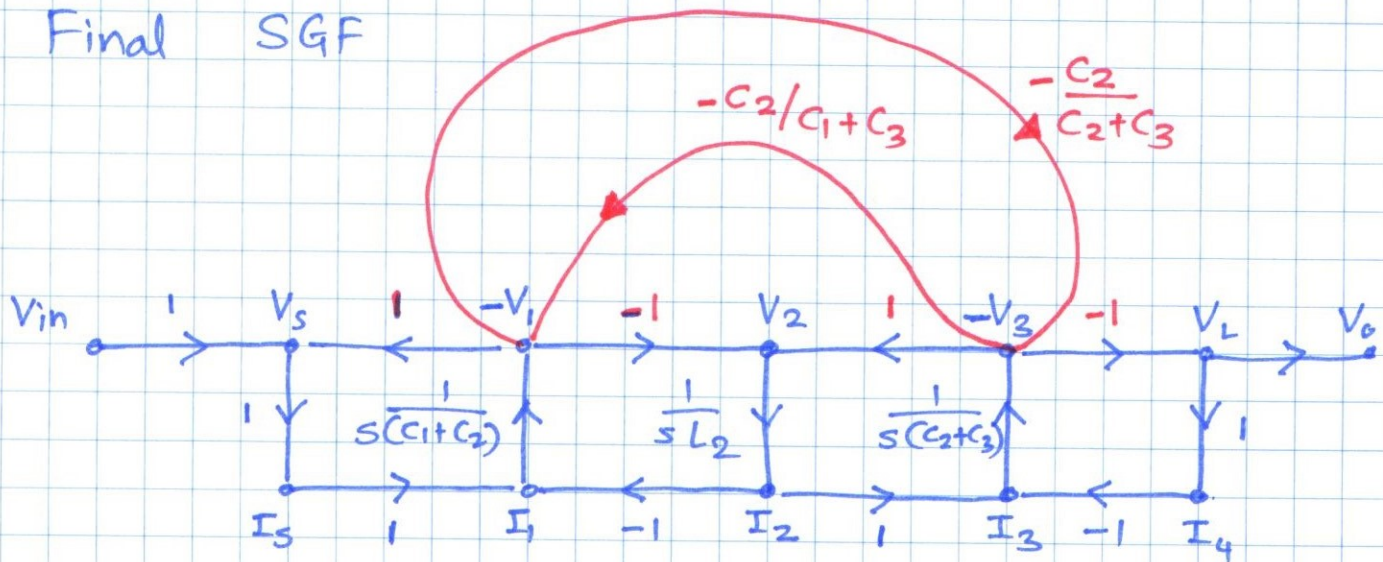


How to implement scaled addition in SC?



→ Modify SGF - Replace V_1 by $(-V_1)$
& Replace V_3 by $(-V_3)$

Final SGF

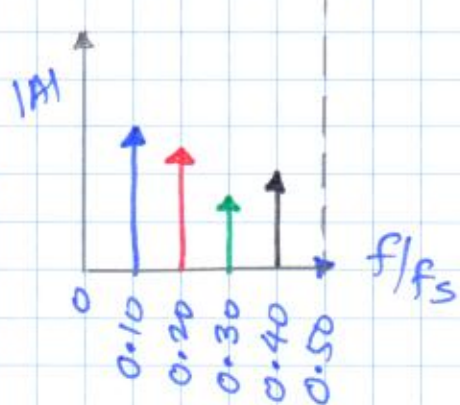
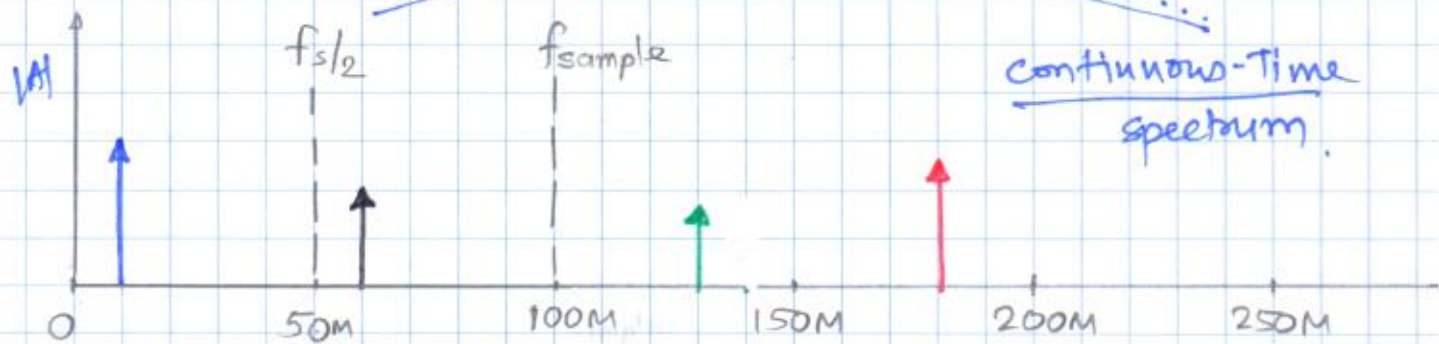


Now this can be implemented using
SC integrators & scaled addition units.

→ HOME EXERCISE -

→ Identical Technique can be
applied to Continuous-Time filters
for implementing zeros
(Eg. Elliptic filters)

ANTI_ALIASING FILTER

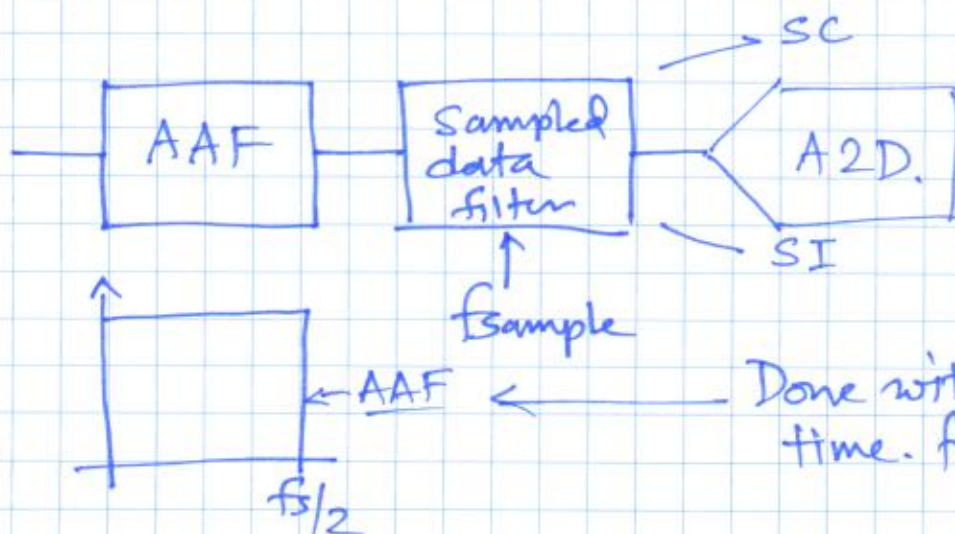


Signals higher than $\frac{f_s}{2}$
fold back into the desired band
— Aliasing.

— Corrupt desired signal forever.

— Nyquist Sampling Thm: Signal should be bandlimited to $f_s/2$.

→ Need to filter out everything above $f_s/2$
→ AAF

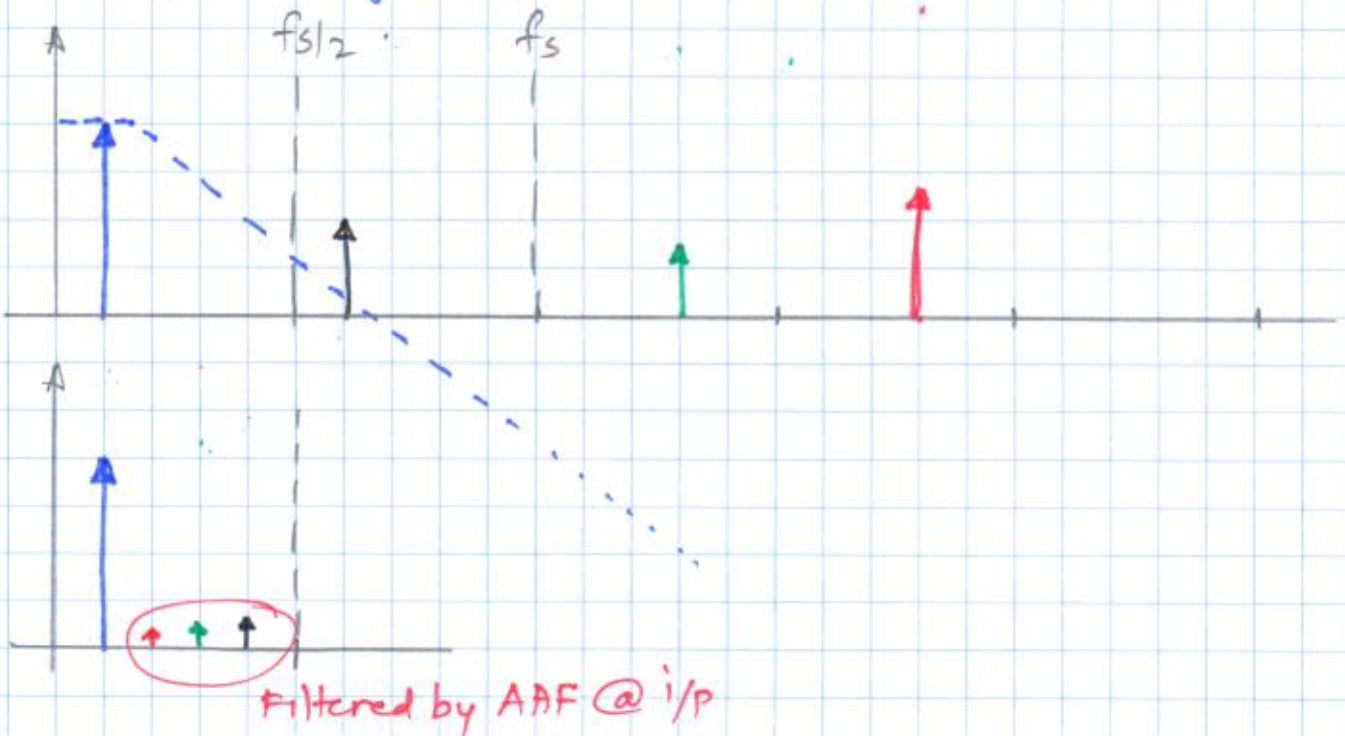


Done with continuous time filter.

Brickwall filters very difficult in cont-time.

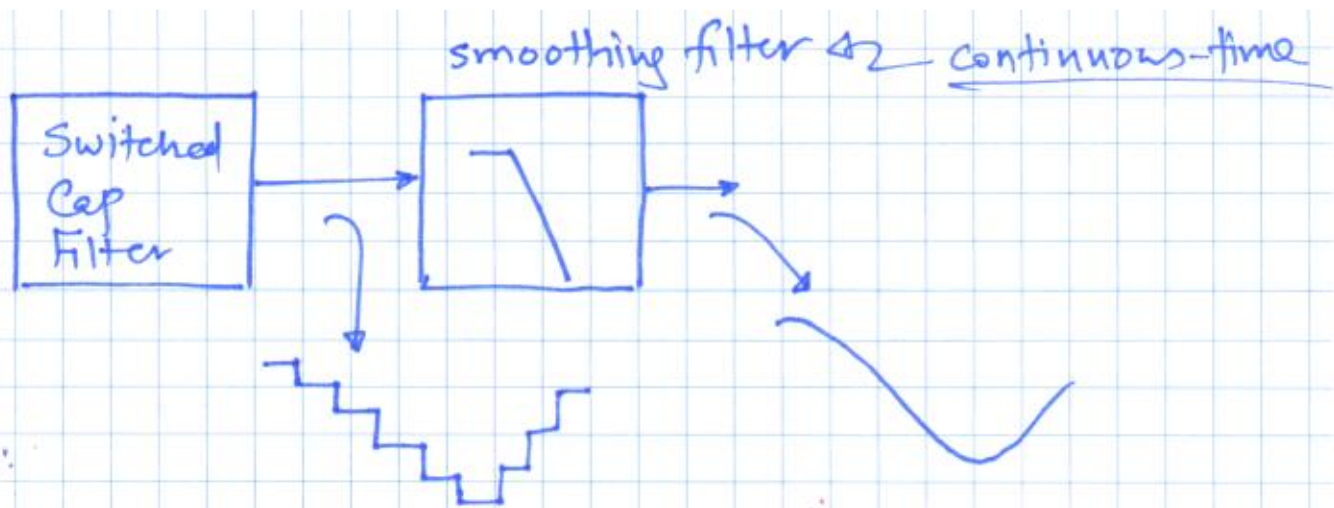
→ Increase sampling rate - oversample

→ Ease requirement on AAF.



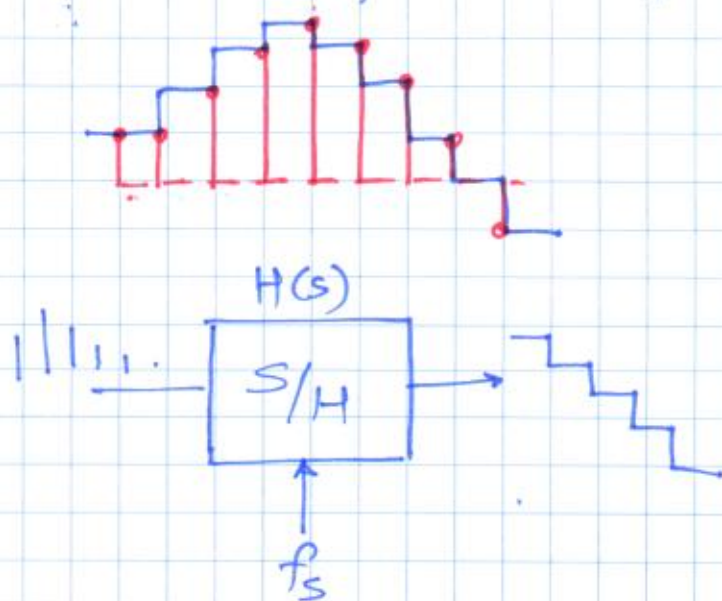
General AAF design guidelines

- low order design - of course continuous-time filter
- Make sure AAF attenuates undesired signals sufficiently with largest PVT variation
- No frequency tuning



Smoothing filter - Removes clock & high frequency artifacts.

Switched cap filter o/p. - Sampled & held o/p



$$|H(f)| = \frac{\sin(\pi f/f_s)}{(\pi f/f_s)} \quad \left. \vphantom{\frac{\sin(\pi f/f_s)}{(\pi f/f_s)}} \right\} \text{Sinc function}$$

