EE-677: Foundation of CAD for VLSI

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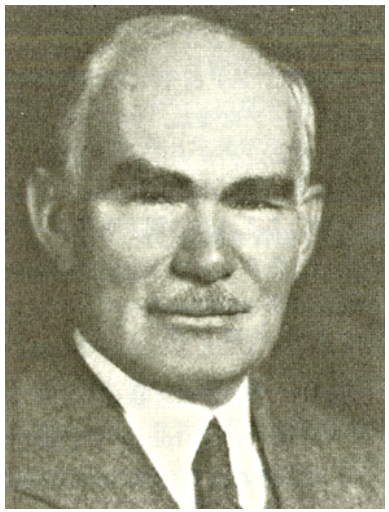
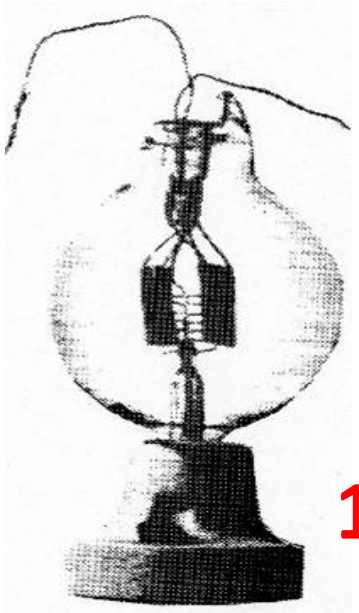
History of Electronics

- Electronics is the most important invention in the 20th cent.
- Electronic Circuits in 100 years

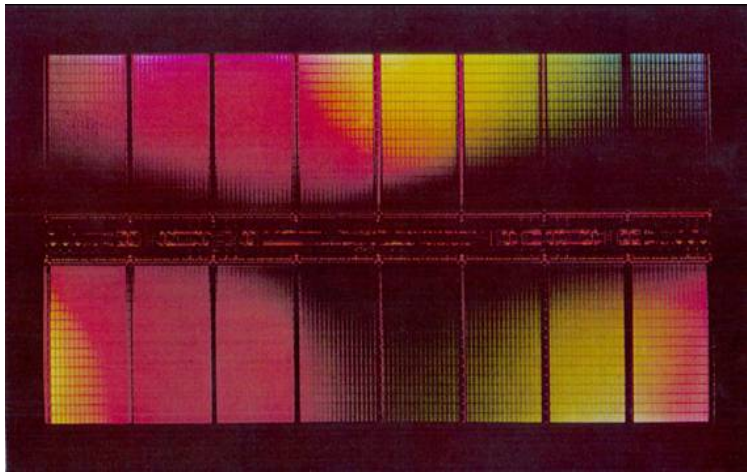
  Vacuum tube → VLSI

12 yeas ago, it was the 100 year anniversary

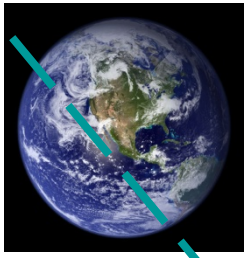




1906



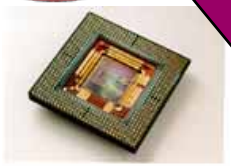
Wanted: CUSTOMERS, who breathe, eat, and live in…..



Global & Regional Political & Macro-Economic Environments

Customer Demand

Electronic End Equipment — ~$ 1050B



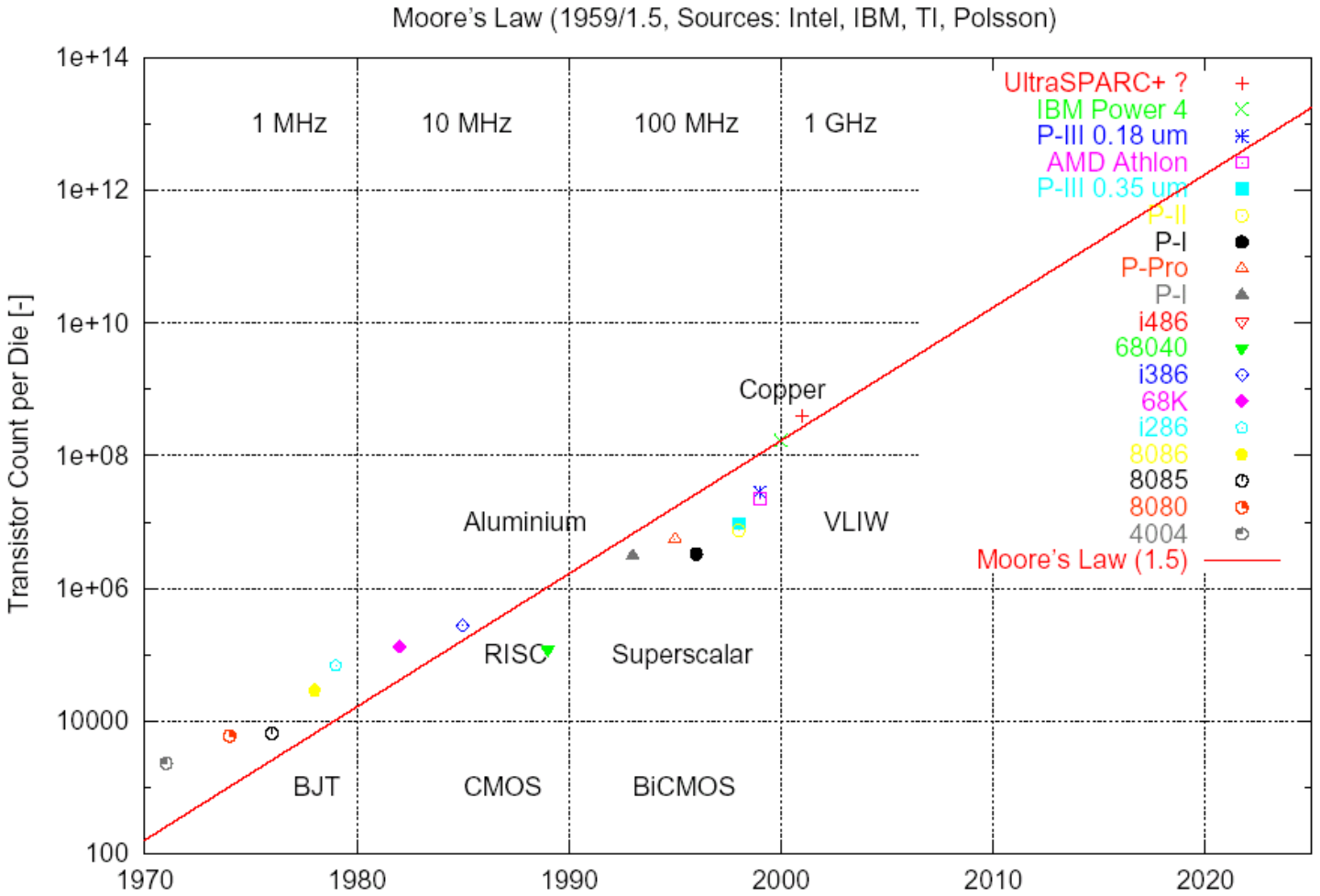
Semiconductors — ~$ 400B

Semiconductor Equipment & Materials — ~$ 100B

ITRS International Technology Roadmap for Semiconductors

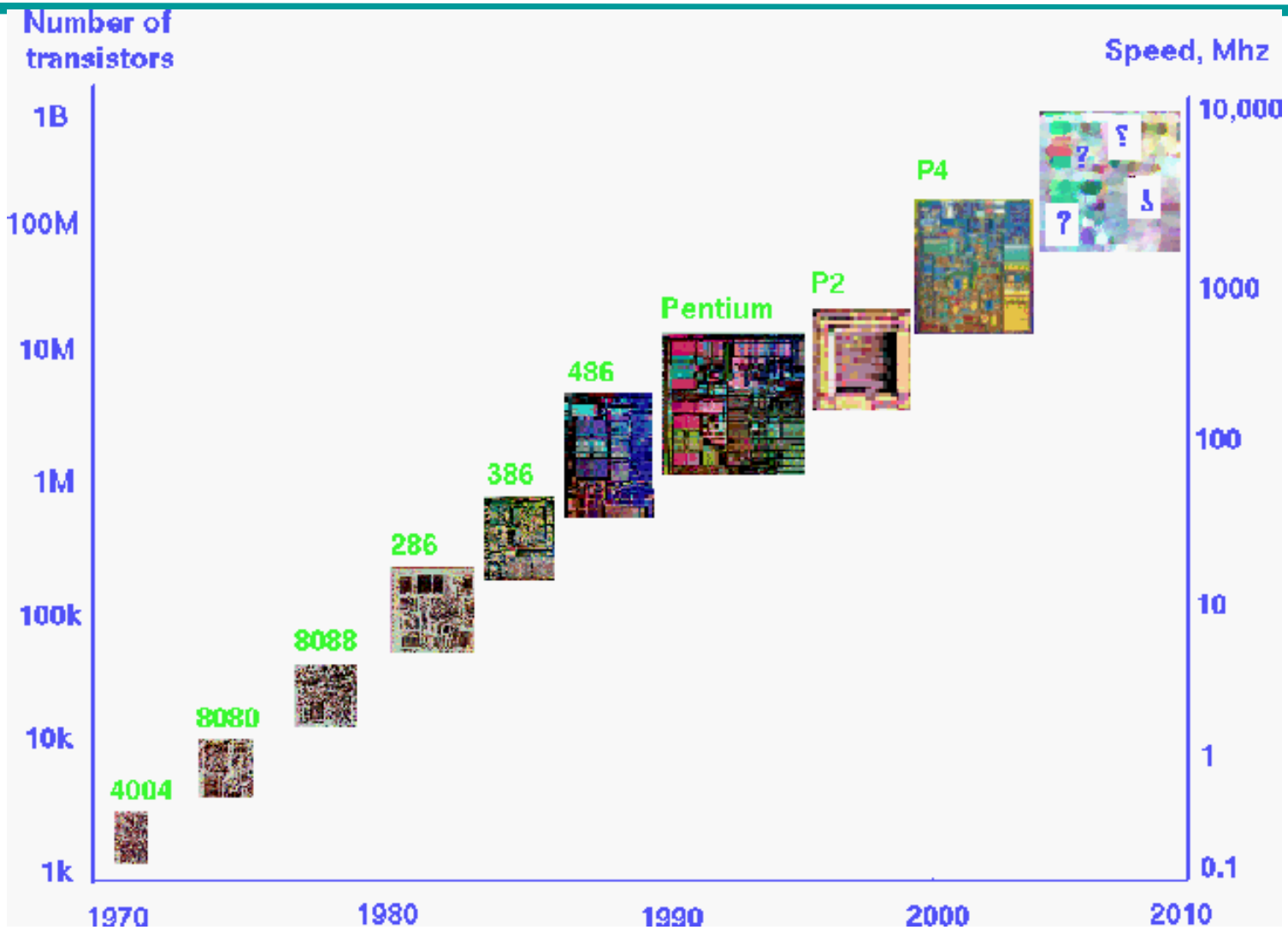
Sources: NASA Gov. ; SEMI

Motivation: Moore's Law
Complexity Growth of VLSI circuits

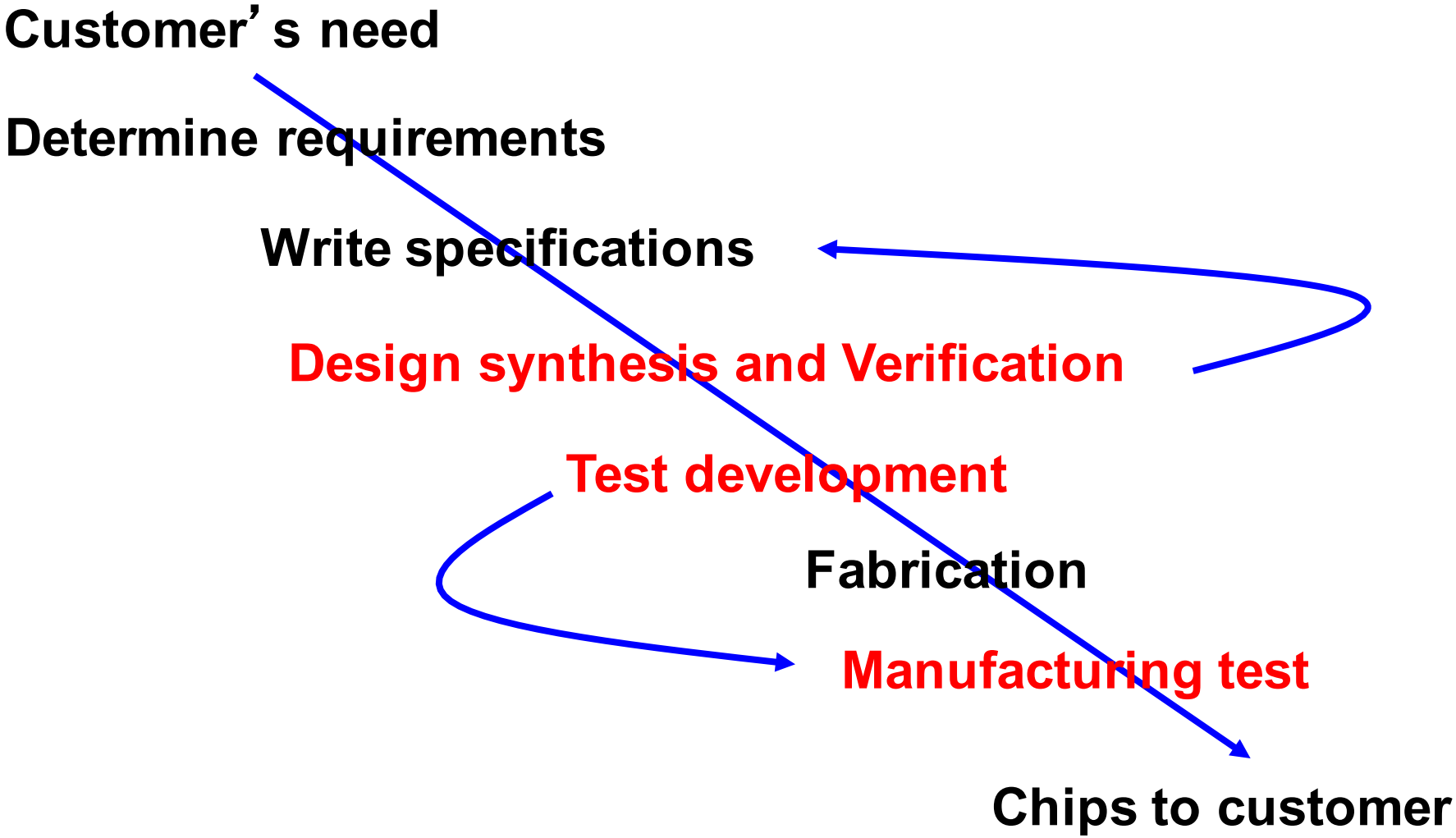


Source (Copp, *Int. AOC EW Conf., 2002*)

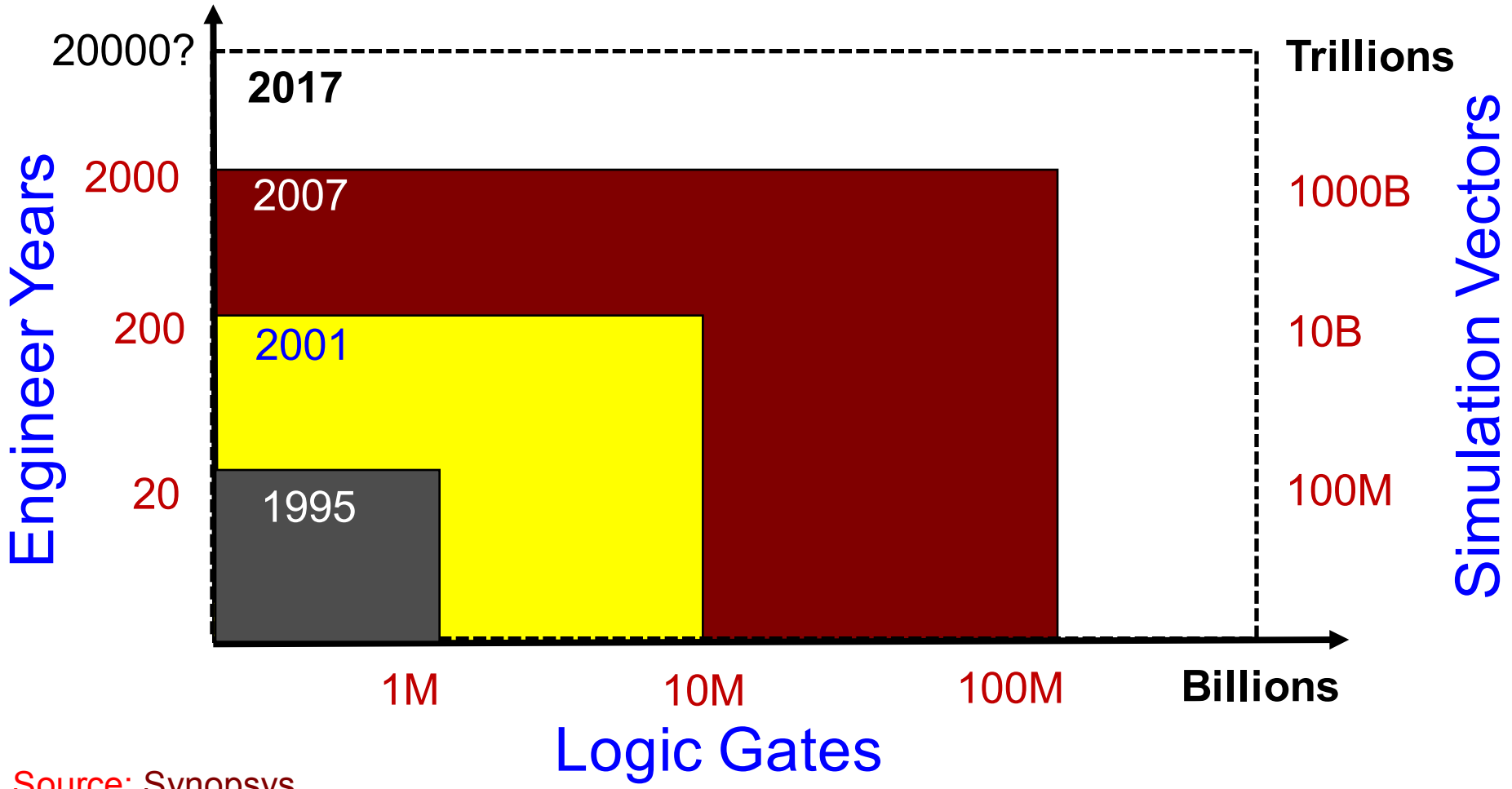
Design Complexity



VLSI Realization Process

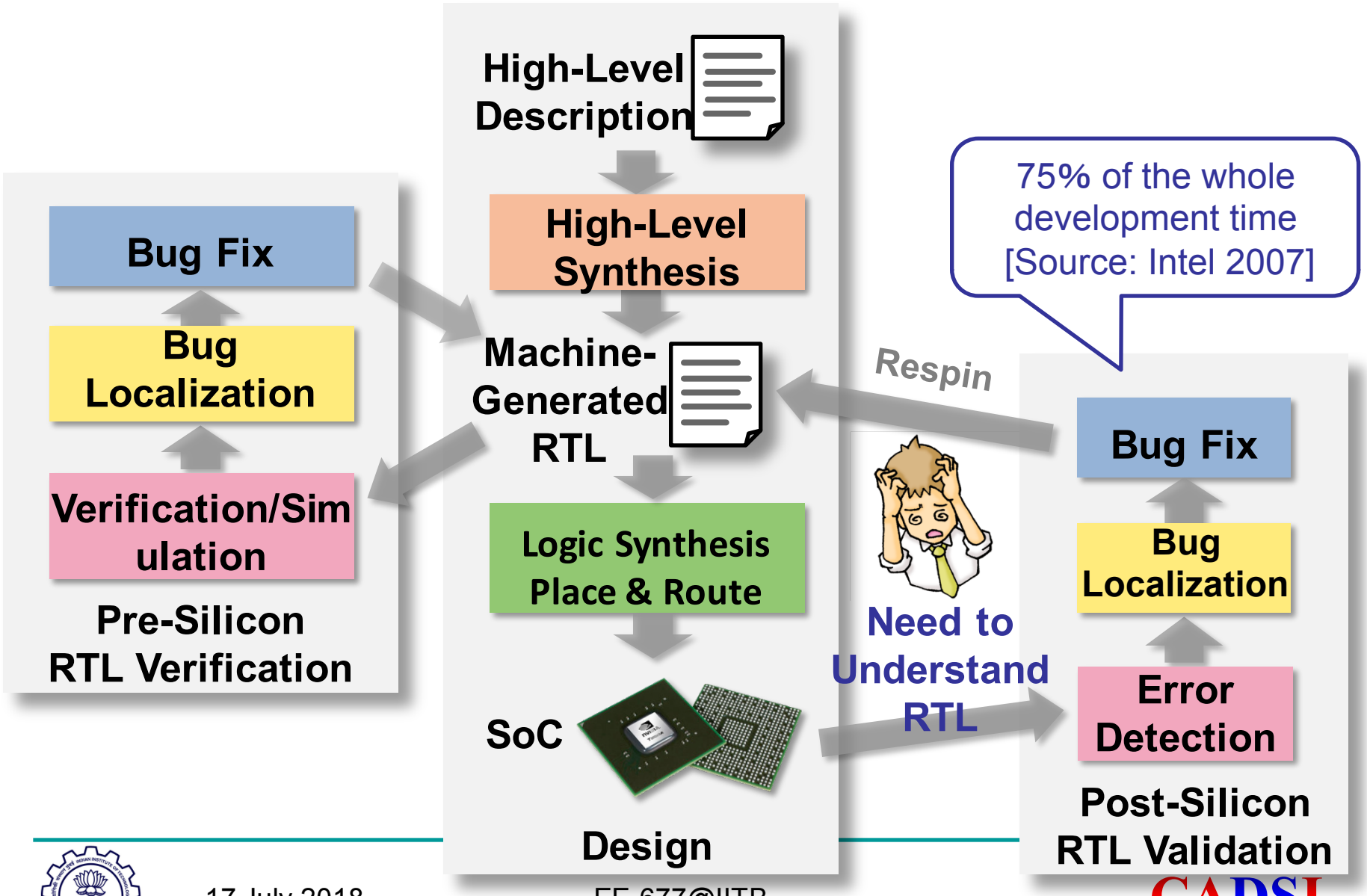


Design Validation Complexity

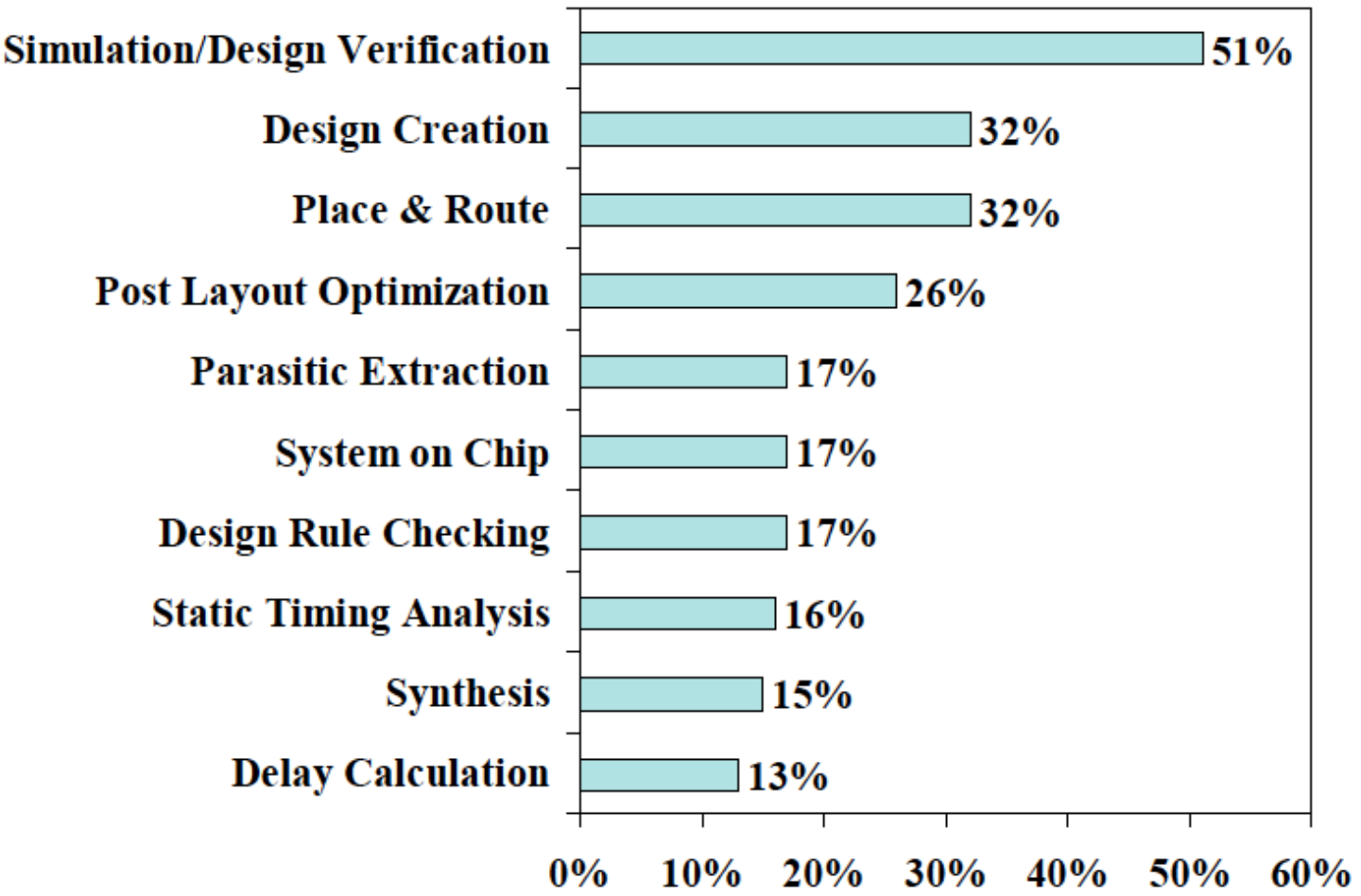


Source: Synopsys

Conventional SoC Design Flow

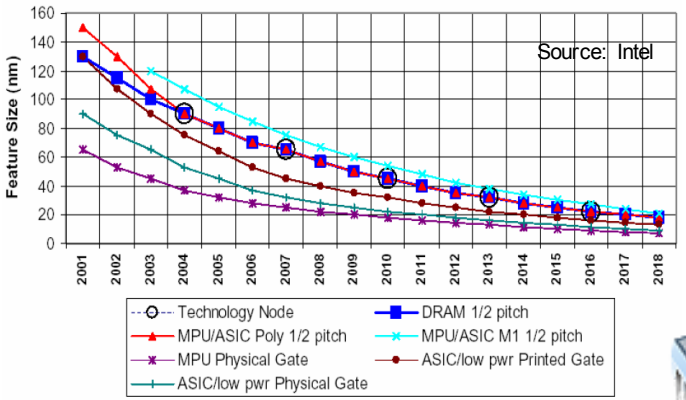


Verification challenge

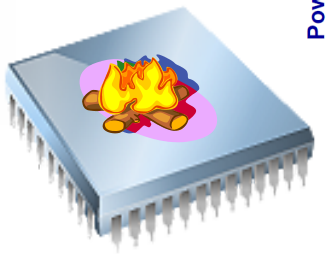


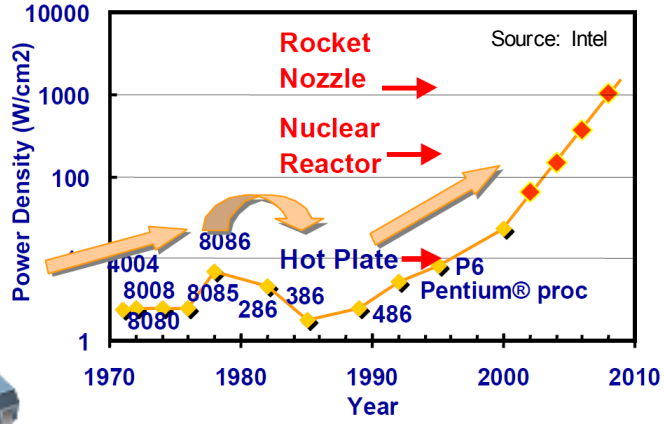
Bottlenecks in Design Cycles:
Survey of 545 engineers by EETIMES 2000

Challenges under deep submicron technologies

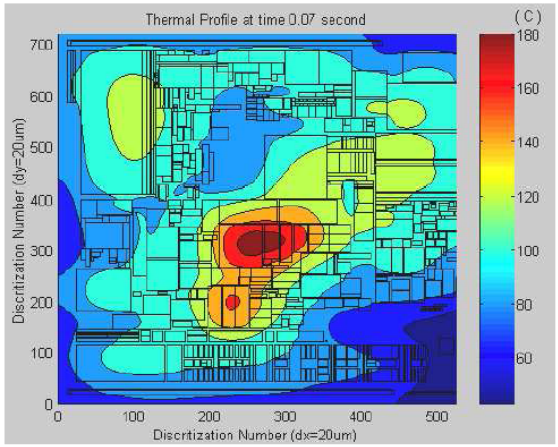


Chip size decreases



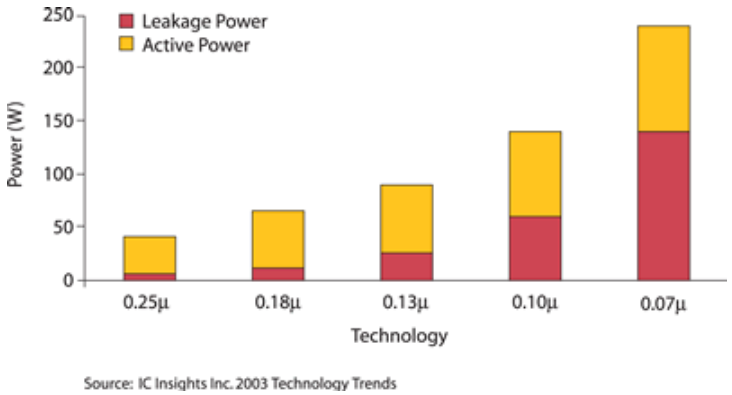


Power density increases



Source: Wang et al. ISPD2003

Chip becomes hotter



Source: IC Insights Inc. 2003 Technology Trends

Leakage power make it worse

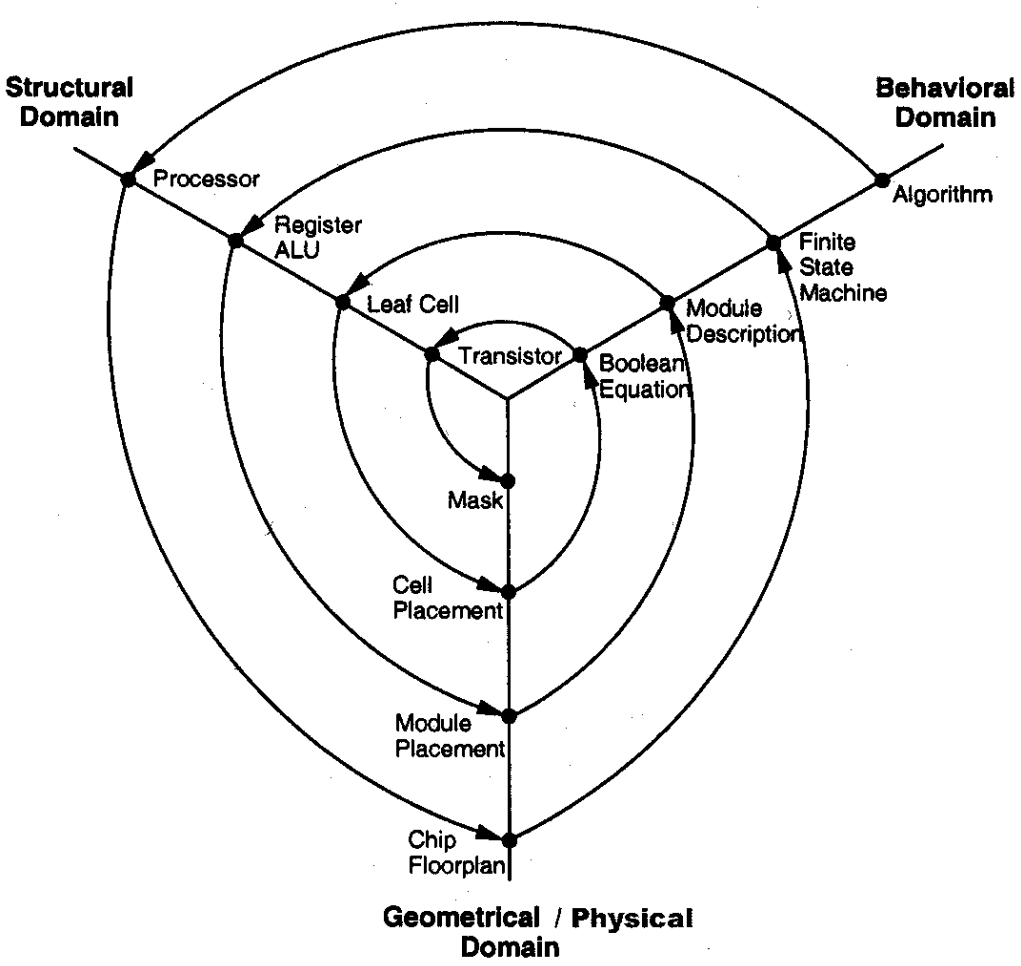
Coping with Complexity

- How to design System-on-Chip?
  - Billions of transistors
  - Tens to hundreds of engineers
- Structured Design
- Design Partitioning

Structured Design

- **Hierarchy**: Divide and Conquer
  - Recursively system into modules
- **Regularity**
  - Reuse modules wherever possible
  - Ex: Standard cell library
- **Modularity**: well-formed interfaces
  - Allows modules to be treated as black boxes
- **Locality**
  - Physical and temporal

Gajski Y-Chart



Definitions

- *Design synthesis:* Given an I/O function, develop a procedure to manufacture a device using known materials and processes.

- *Verification:* Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.

- *Test:* A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Course Outline

- VLSI Design Flow
- High Level Synthesis
- Logic Synthesis
- Physical Design
- Hardware Software Co-design [if time permits]
- Reversible Circuit Design [if time permits]

Course Schedule

Class Hours: Slot 13

- Monday (7:00 pm to 8:30 pm)
- Tuesday (7:00 pm to 8:30 pm)

Office Hours

- TBD

Course Evaluation

- Mid Term Exam (10%)
  - Open Book/Notes Exam
- Final Exam (25%)
  - Open Book/Notes Exam
- Assignments (15%)
  - Set of assignments will be given periodically
- Course Projects (20%)
  - Projects to implement CAD algorithm
- Continuous Evaluations (25%)
  - Weekly (THursday) tests (90% best will be counted)
- Presentation/Viva (5%)
- [Bonus] Research Project (15%)
- [Bonus] Course notes (5%)

Grades

Absolute Grade

- > 90: AA
- 81 – 90: AB
- 71 – 80: BB
- 61 – 70: BC
- 51 – 60: CC
- 45 – 50: CD
- 40 – 44: DD
- < 40 : FR

Books (Design Verification)

- Synthesis and Optimization of Digital Circuits
  - Giovanni De Michelli
- Logic Synthesis and Verification
  - Hatchel & Somanzi
- Algorithm for Physical Design Automation
  - Naveed Shervani
- Current Literature (IEEE TC/TCAD/TVLSI)

Acknowledgement

- Prof. Hideo Fujiwara, NAIST, Japan
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- Prof. Adit Singh, Auburn Univ.
- Prof. Samiha Mourad, Santa Clara Univ.
- Prof. Michiko Inoue, NAIST
- Prof. Erik Larsson, Linkoping Univ.
- Dr. Subir Roy, Texas Instruments, India
- Dr. Rubin Parekhji, TI, India

Thank You