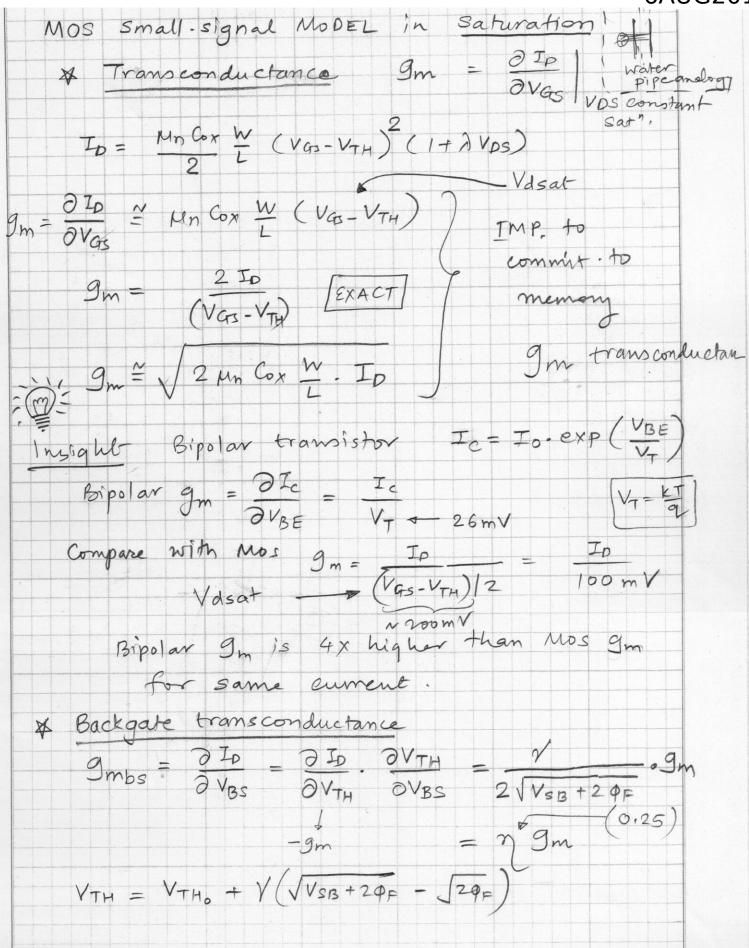
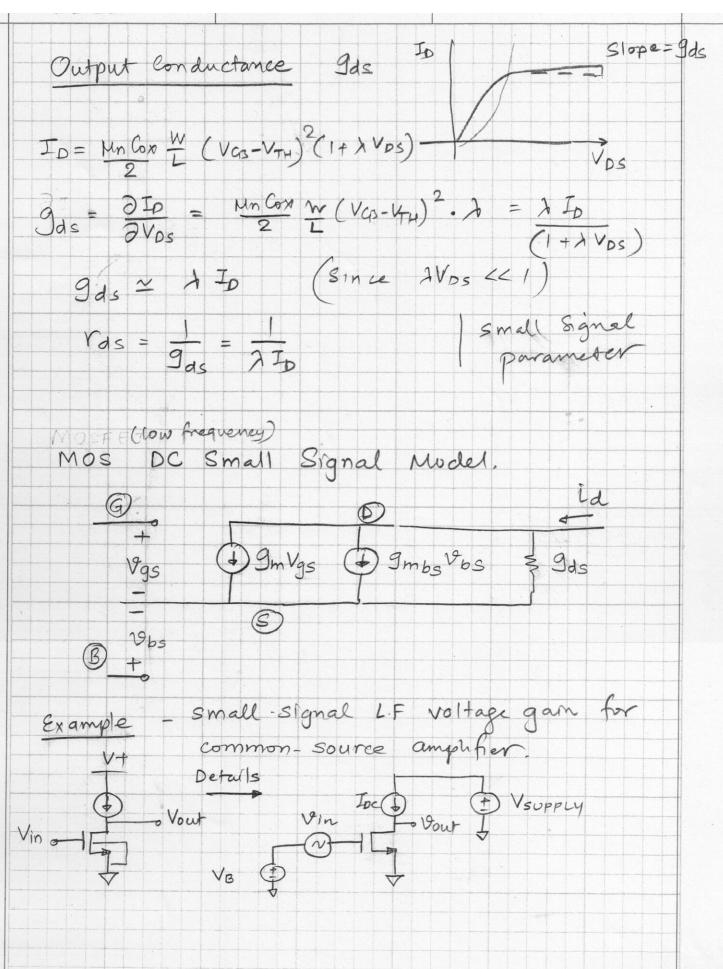
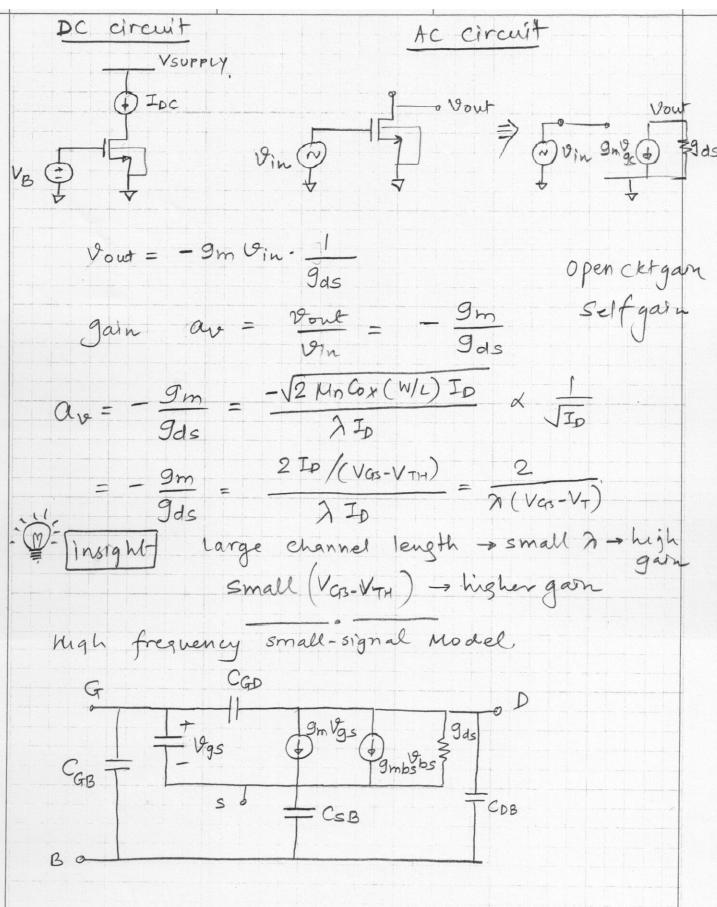
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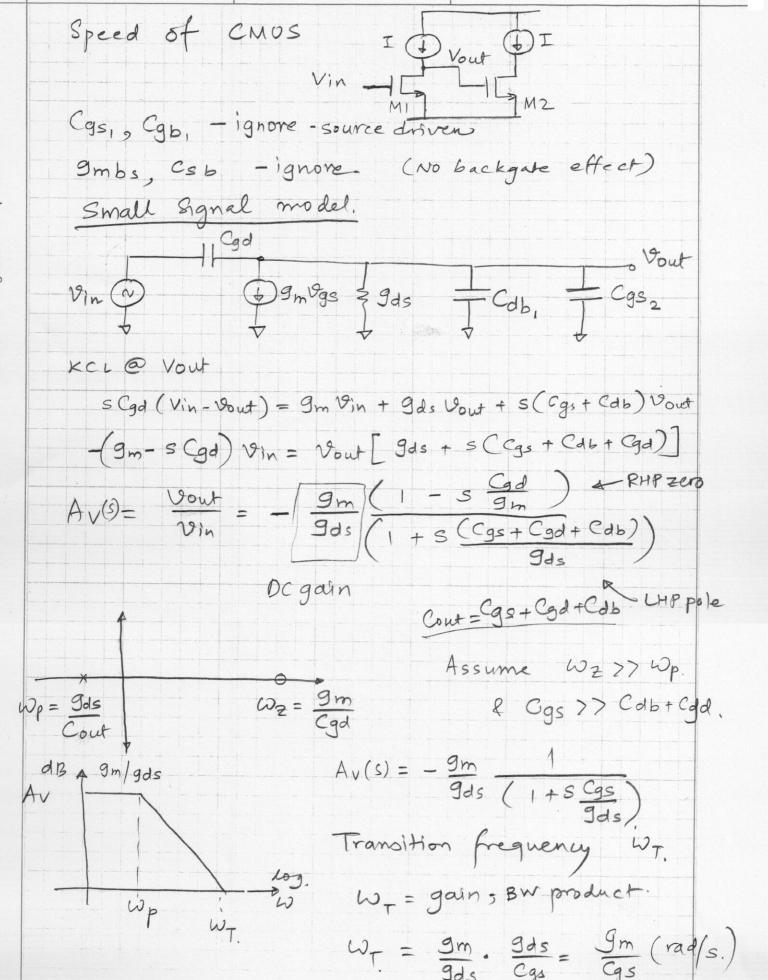








Engineer's Computation Pad



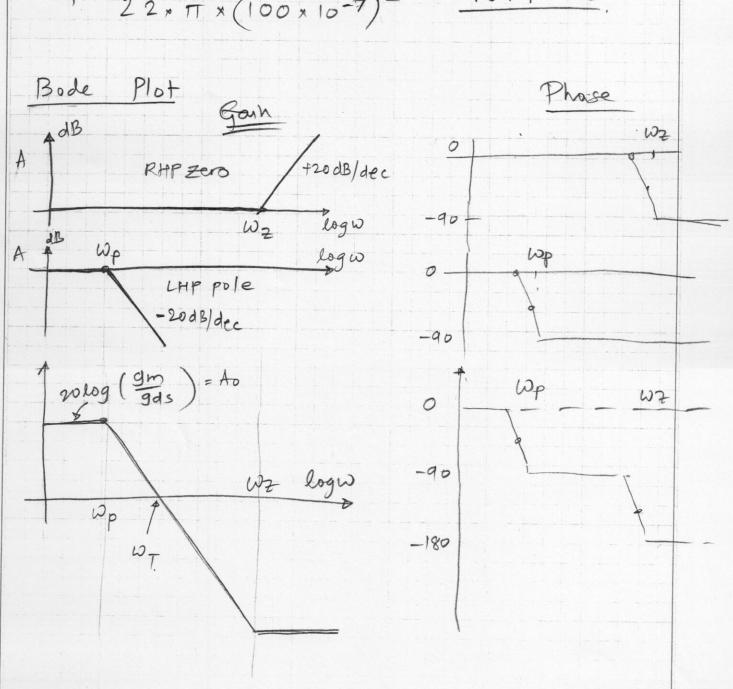
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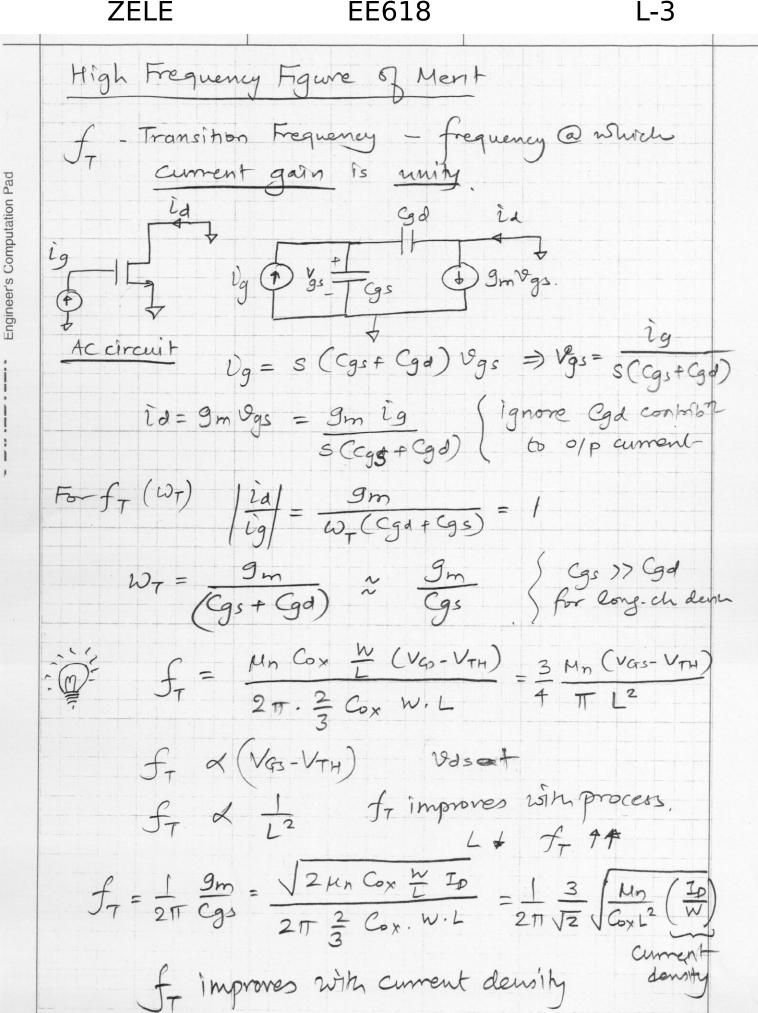
$$Lo_{7} = \frac{gm}{Cgs} = \frac{\mu_{1} Co_{x}(W/L) \cdot (V_{GS} - V_{TH})}{\frac{2}{3} Co_{x} \cdot (W \cdot L)}$$

$$= \frac{3 \mu_{1} (V_{GS} - V_{TH})}{L^{2}} = \frac{8 \times ample \cdot M_{1}}{2 \times ample \cdot M_{1}} = \frac{350 \text{ cm}^{3} V/s}{2 \times 100 \text{ m}^{3}}$$

$$= \frac{3 \cdot 350 \times 0.2}{2 \cdot 7 \times (100 \times 10^{-7})^{2}} = \frac{167.1 \text{ GHz}}{167.1 \text{ GHz}}.$$



	ZELE E	EP18		L-3	О
	Example values for	or all.	transstor	parameters	
	Example process	Lmin	= 0.5 pm		
70			NMOS	PMOS	
	VTO (V) Threshold		+0.5	-0.6	
on Pa	GAMMA (body Effect coef V	1-1/2	0.45	0.4	
nputati	Tox (A)		90	90	
's Con	UO (mobility cm2/V/s)		350	100	
Engineer's Computation Pad	LAMBDA (A-ch. length modulation Coe	f V-')	0.1	0.2	
R I	PH1 (20F) V	1	0.9	0.8-	
≈ ⊃IAEUI	$C_{0x} = \frac{c_{0x} c_{0}}{c_{0x}} = \frac{3.97}{c_{0x}}$	× 8.85 ×	10-12 (Flm)	$= 3.9 \times 10^{-3} $ F	/m²
	= 3,	9 fF/ µm²	-		
	$\lambda_n = \frac{0.1  \text{V}^{-1} \times 0.5  \text{\mu r}}{\text{Ln}}$	$\frac{n}{Ln} = \frac{0.00}{Ln}$	5 v-1 r in um		
<u> </u>	λρ = 0.2 x 0.5 =				
	Mn Cox = 350 cm²/v/s x 3.9 fF/mm²				
	= 350 × 10 <sup>-4</sup> × 3.0	7 ×10-15	1/V2 = 136.	·5 MA/V2	
	MpGx = 39 MA/V2	10-12			
	Example	9m=1	2. Mn Cox	W. Ip	
	1 100MA	= ) =	2 × 136.5 × .	0.5 × 100 6	
	1 100MA W= 10 Mm	= .	738 MA =	738 µS	
	L = 0.5 µm	gds = A	IDS = O.IX	100×106 = 10 MS	



# EE618 (Zele)

### Body Effect and Sub-threshold Conduction

## **Body Effect**

Consider the simplified NMOS shown in Fig. 1 part (A). A voltage  $V_{GS}$  is applied between gate and source whereas a voltage  $V_{SB}$  is applied between the source and bulk of the NMOS. For this explanation, we consider that the bulk is a p-well so that we can separately bias it (NMOS in a chip may lie in substrate and substrate of the whole chip will be tied to ground). We consider the following two cases -

CASE 1: 
$$V_{GS} = V_{TH}$$
 and  $V_{SB} = 0$  V

As shown in Fig. 1 part (B), Due to positive  $V_{GS}$  the holes in the channel region move out leaving negatively charged ions behind. The electrons that form the inversion layer comes from the n+(very high concentration) source region. The current in the device will be due to drift of these electrons when a  $V_{DS}$  is applied.

#### CASE 2: $V_{GS} = V_{TH}$ and $V_{SB} > 0$ V

In this case we are increasing  $V_{SB}$  (can be achieved by decreasing the bulk voltage keeping source voltage constant). Due to a net positive voltage on the source as compared to the bulk, some of the electrons present in the channel will be attracted back in the source as shown in of Fig. 1 part (C). Hence to achieve the same charge density as in CASE1 we need a more positive charge on the gate. Therefore we can say that increasing  $V_{SB}$  increases threshold voltage.

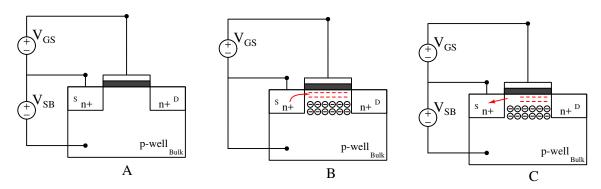


Figure 1: Body effect in MSOFETS

## Effect of $V_{DS}$ in Subthreshold Region

- The region where  $V_{GS}$  of the device is less than or close to  $V_{TH}$  is known as sub-threshold region.
- Due to diffusion of minority charge carrier electrons, some leakage current may flow in the device even when  $V_{GS}$  is less than  $V_{TH}$ .
- For a constant  $V_{DS}$ , the current equation in subthereshold region is given as

$$I_{subth} = I_O \times exp(\frac{V_{GS}}{\zeta V_T}) \times (1 - exp(\frac{-V_{DS}}{V_T}))$$

where  $\zeta$  is a non-ideality factor greater than 1 and  $V_T = KT/q$ 

- For  $V_{DS} = 0$ , the current  $I_{subth} = 0$ .
- For  $V_{DS} > 4V_{TH}$  or  $5V_{TH}$  the equation reduces to

$$I_{subth} = I_O \times exp(\frac{V_{GS}}{\zeta V_T})$$