High-Level Synthesis -V

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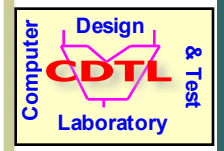


E0-285: CAD of VLSI Systems

Control Unit Synthesis

- n_{act} activation signals to be issued by the controller
- Circuit implementation
  - Microcode based
    - ROM
  - Hard-wired
    - Sequential circuit

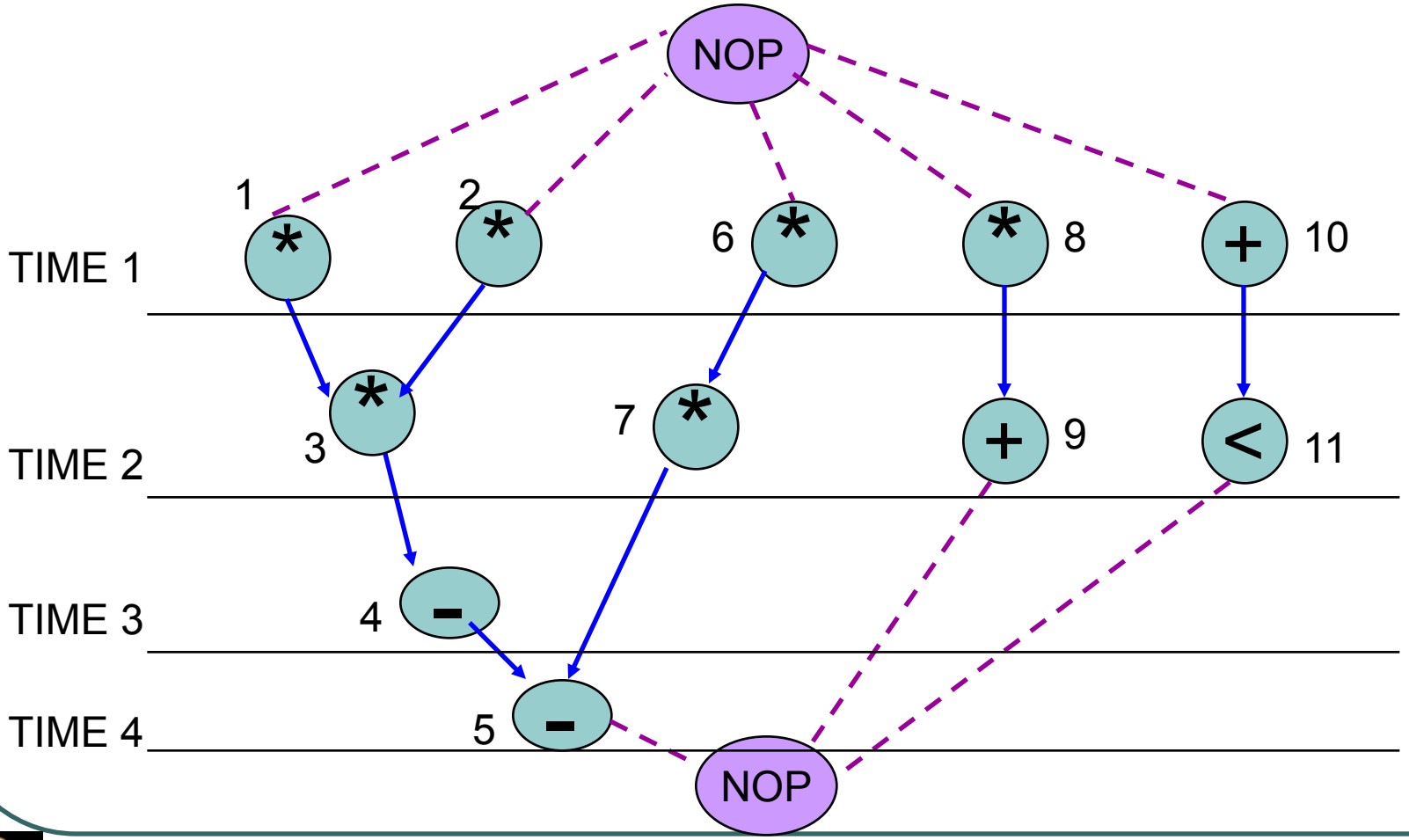
Micro-coded Control Synthesis

- Microcoded implementation can be achieved by using a memory that has as many words as latency λ
- Each word is one-to-one correspondence with a schedule step
- Address bits of ROM $n_{bit} = \log_2 \lambda$
- Synchronous counter of n_{bit} and reset signal
- Counter runs on system clock

Micro-coded Control Synthesis

- Encoding of activation signals
  - Associate the activation signal of each resource to one bit of the word
  - Horizontal Encoding
  - n_{act} is larger than λ
- Vertical Encoding
  - $\log_2 n_{act}$ bits
  - Reduces width of ROM

Scheduled Sequencing Graph



Micro-coded Control Synthesis

Vertical Encoding

- Needs decoders
  - Micro-ROM
- Operational concurrency
- Can be used by lengthening theschedule

Micro-coded Control Optimization

- Search for shortest encoding of the words such that full concurrency is preserved
  - Micro-coded compaction
  - Intractable
  - Solution
    - Word – partition into fields
    - Operation – partition into groups
  - Operation in each group are vertically encoded
  - No pair of group operation is concurrent

Micro-coded Control Optimization

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Micro-coded Control Optimization

- Heuristic
  - Optimal partition to minimize the number of groups
  - Conflict graph
    - Vertices – Operation
    - Edges – Concurrency
  - Compatibility graph

Micro-coded Control Optimization

- Partition {v1, v3, v4}, {v2}, {v6, v7, v5},
- {v8, v9}, {10, v11}

A	B	C	D	E
01	1	01	01	01
10	0	10	10	10
11	0	00	00	00
00	0	11	00	00

Hardwired Control Synthesis

- Finite State machine
  - Moore type m/c
  - No. of states = λ
  - State S = $\{s_l, l = 1, 2, \ldots, \lambda\}$
  - State transitions are unconditional
  - Conditional transition to s1 from all other states controlled by reset provides the capability of start and reset

Hardwired Control Synthesis

- Hierarchical Sequencing Graph
  - Local control unit – Control block
    - Has its own activation signal
  - Each control block reset itself after having execution of the last step
  - Controlling block of the calling model continues

High Level Synthesis

Objective

- Area
- Performance
- Power
- Reliability

Power

- Dynamic Power
- Static Power

- Transitions
- Large fraction of transitions incurred during the circuit operation are unnecessary

➢ Suppressing or eliminating unnecessary transitions

Power Reduction Techniques

Techniques

- Clock gating
- Partitioning of circuits
- Scheduling – to maximize idle time
- Maximize the sleep time of storage elements

Power Reduction Techniques

During the control steps in which functional unit is utilized to perform some operation is said to be active

During other control steps, the functional unit is said to be idle

The manner in which register sharing is performed can significantly affect the unnecessary power dissipation (spurious switching) in functional units during their idle cycle

Effect of Register Sharing

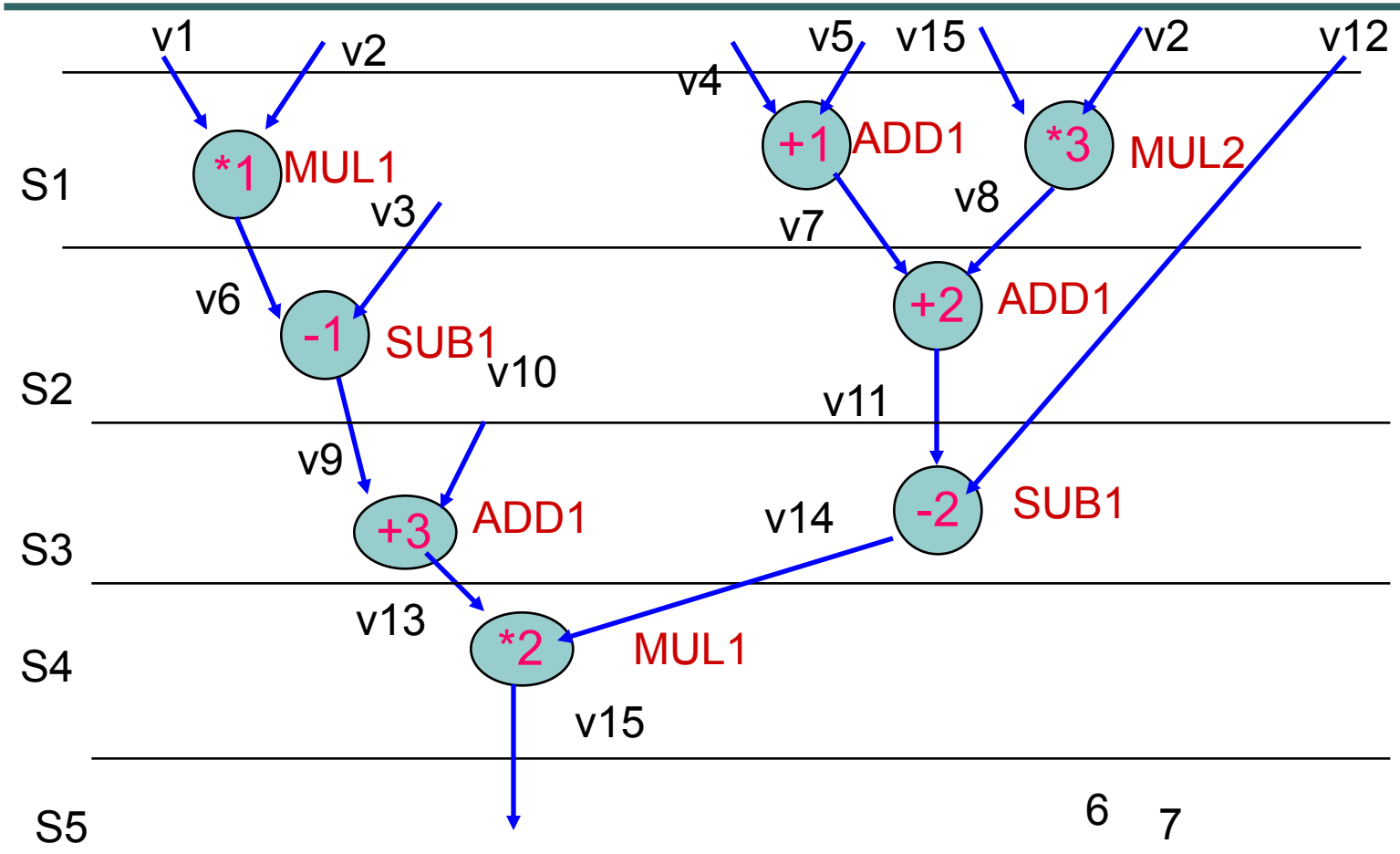
Architectural Model

Register Allocation and variable assignment

Effect on switching activity

Spurious switching activities can sometimes be eliminated without increasing the number of registers in synthesized circuit

Scheduled DFG



Variable Assignment

Register	Assignment1
R1	V1, V7, V11, V13
R2	V2, V8, V10, V14
R3	V3, V5, V9
R4	V4, V6
R5	V12
R6	V15

Switching Activity

S1	V1	*1	V2 V15	*3	V2	X	V12 V4	+1	V5
S2	V7	X	V8	X	V8 V6	-1	V3 V7	+2	V8
S3	V11	X	V10	X	V10 V11	-2	V12 V9	+3	V10
S4	V13	*2	V14	X	V14 V13	X		X	V14
S5									
		MUL 1		mu l2		Sub1		Add 1	

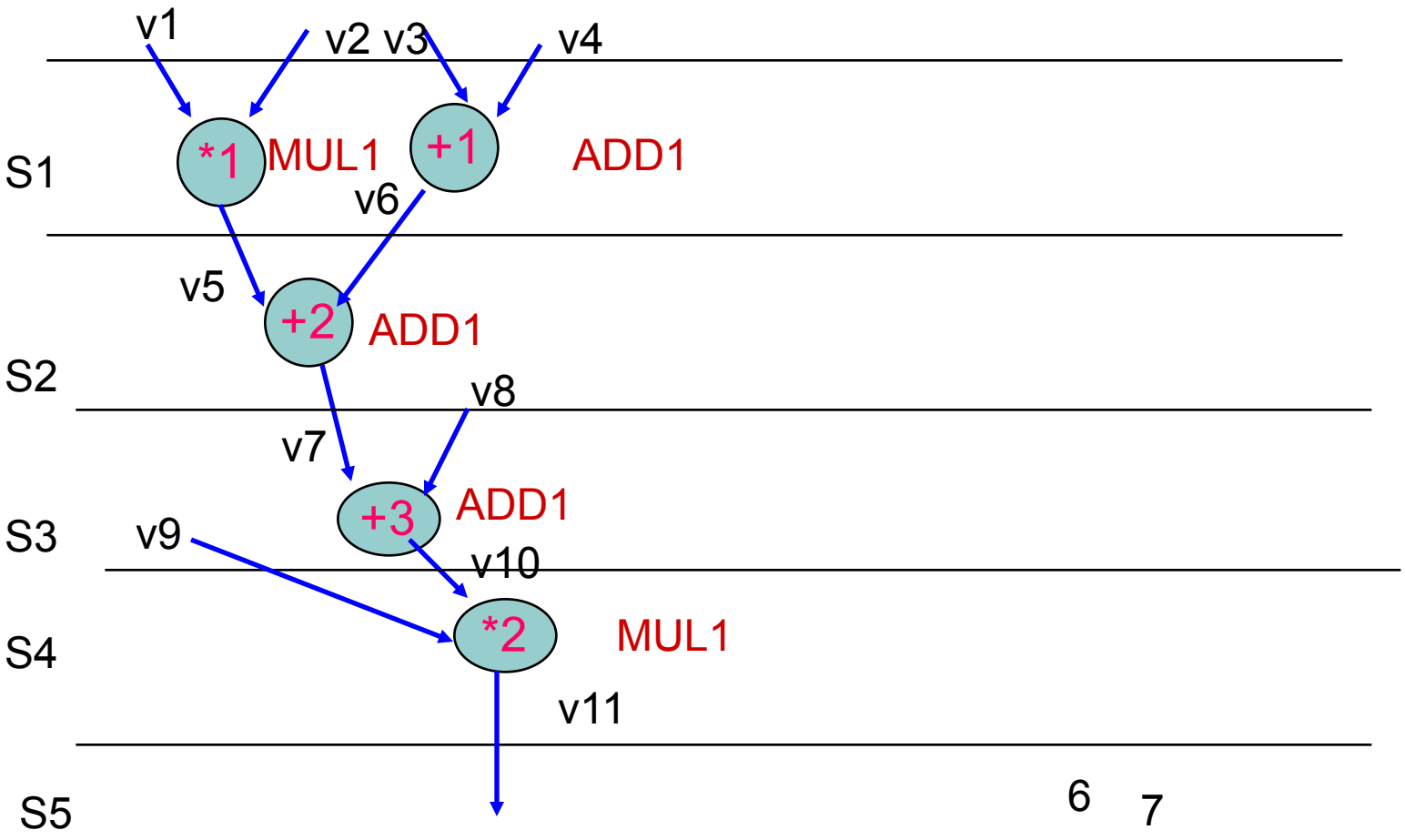
Variable Assignment

Register	Assignment2
R1	V1, V13
R2	V2
R3	V4, V8, V10
R4	V5, V7, V9
R5	V12
R6	V3
R7	V6, V11
R8	V14
R9	V15

Switching Activity

S1	V1	*1	V2 V15	*3	V2	X	V12 V4	+1	V5
S2					V6	-1	V3 V7	+2	V8
S3					V11	-2	V12 V9	+3	V10
S4	V13	*2	V14						
S5									
		MUL 1		mu l2		Add1		Add 2	

Scheduled DFG



Variable Assignment

Register	Assignment1	Assignment
R1	V1, V5, V7, V9	V1, V9
R2	V2, V6, V8, V10	V2, V10
R3	V3	V3, V5, V7
R4	V4	V4, V6, V8

THANK YOU