EE618 (Zele)

CMOS Analog VLSI Design : Homework - 2 (30 - Marks)

Submission Deadline : 25th Aug 2019 11:55PM

- All problems are based on Cadence simulations
- The submission must contain appropriate plots labelled clearly.
- The submission must contain the theoretical calculations wherever it is applicable.
- Submission must be in ***Teamname_Rollnumber_Yourname_Assignment2.pdf*** format.
- Submissions after deadline with not be accepted under any circumstances
- All MOSFET models should be used from SCL 180 nm library.
- MOSFETS in schematics must be annotated with all required parameters. Ex: Width, Length, Fingers, Multipliers.
- Report all values preferably in tabular format wherever it is appropriate.

Question 1 [10 Marks]

Design the amplifier in Figure 1 for gain $\geq$ 18 dB.
Given V_{OUT} = 0.9 V, R_B = 100 kΩ, DC Power Consumption $\leq$ 1.8 mW, $C_L = 100fF$, $C_{1,2} = 10pF$, I_B = 10 μA, L= 0.18 μm and unit finger width = 1 μm.

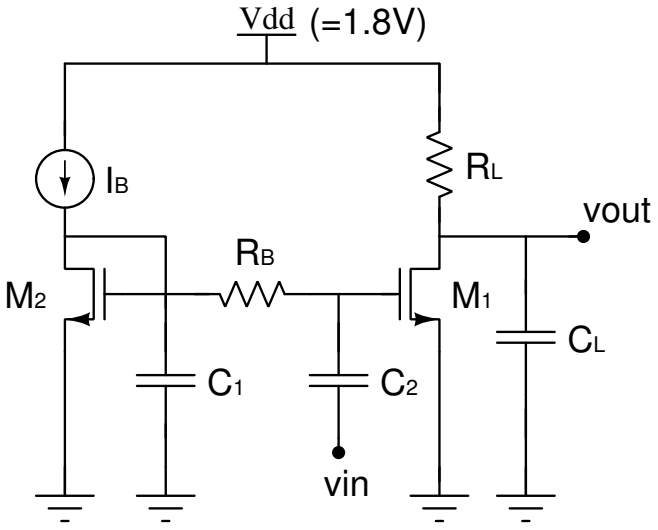

Figure 1: CS amplifier with resistive load

a) Show the step by step design procedure. [3 Marks] $\gamma_{out} = 464.02K$

b) Report the values of components: R_L, fingers, multipliers, aspect ratio of M_1 and M_2. [1 Marks]

c) Perform a DC operating point analysis and annotate the voltages at each node. [1 Marks]

d) Perform ac analysis and plot gain from 10 kHz to 10 GHz. Mark clearly (through markers/cursors) the maximum gain and the 3-db bandwidth. [1 Marks]

e) Perform a transient analysis with a 2 mV sinusoidal input at 10 MHz. Plot the input and the output wave forms and clearly mark the peak-to-peak values. [1 Marks]

f) Tabulate the simulated gain and bandwidth values. [1 Marks]

	Simulated
Gain (dB)	
Bandwidth (Hz)	

Question 2 [10 Marks]

Replace the load resistor in Figure 1 with PMOS current source load as shown in Figure 2. Maintain the DC current in M1 same as that of in Question 1.

a) Show the step by step design procedure. [4 Marks].

b) Report the values of components: fingers, multipliers, aspect ratio of all transistors. [2 Marks].

c) Perform a DC operating point analysis and annotate the voltages at each node (g_m, i_{ds}, region of op., v_{gs}). [1 Marks].

d) Perform ac analysis and plot gain from 10 kHz to 10 GHz. Mark clearly (through markers/cursors) the maximum gain and the 3-db bandwidth. [1 Marks]

e) Compare the ac response with that of Question 1 and write your observations. [2 Marks]

f) Perform a transient analysis with a 2 mV sinusoidal input at 10 MHz. Plot the input and the output wave forms and clearly mark the peak-to-peak values. [1 Marks]

g) Tabulate the simulated gain and bandwidth values. [1 Marks]

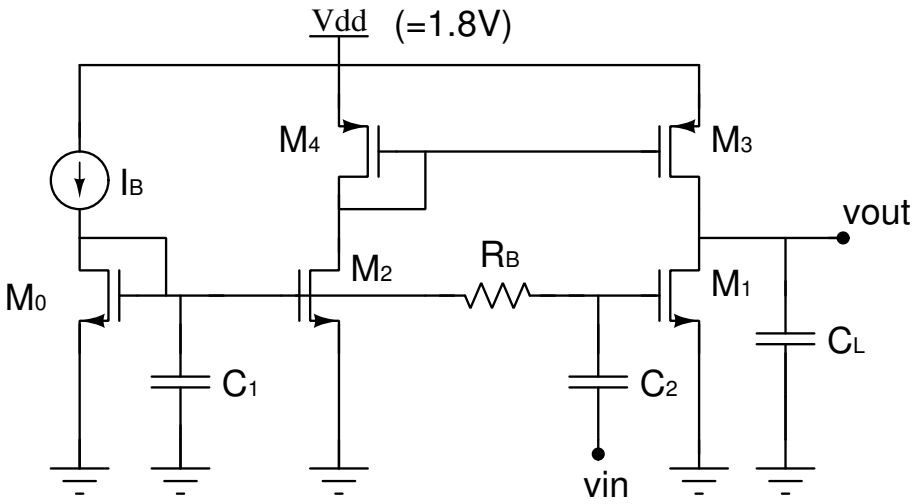

Figure 2: CS amplifier with PMOS current source load

	Simulated
Gain (dB)	
Bandwidth (Hz)	

Question 3 [10 Marks]

Design the high-swing cascode current mirror shown in Figure 3 to get I_{out} = 200 μA ($\pm$2.5 μA) with V_B = 450 mV . Given V_{dd} = 1.8 V, $C_{1,2} \leq 10pF$, I_B = 10 μA, L = 1 μm and maintain same unit finger width for each mirroring pair.

- Sweep voltage V_B from 0 V to 1.8 V and plot the following with appropriate markers and report your observations with reasons.
  a) Plot I_{out} vs V_B. [2 Marks]
  b) Plot regions of M_5 and M_7 vs V_B (overlay both). [2 Marks]
  c) Plot V_X vs V_B. [2 Marks]
  d) Tabulate the minimum required voltage (V_{Bmin}) for I_{out} = 200μA, voltages at which operating regions of M_5 and M_7 change (if any) [1 Marks]
- Tabulate the values of components: R_B, fingers, multipliers, and aspect ratio of all transistors. [2 Marks]
- Perform a DC operating point analysis and annotate the voltages and currents at V_B = 450 mV. [1 Marks]

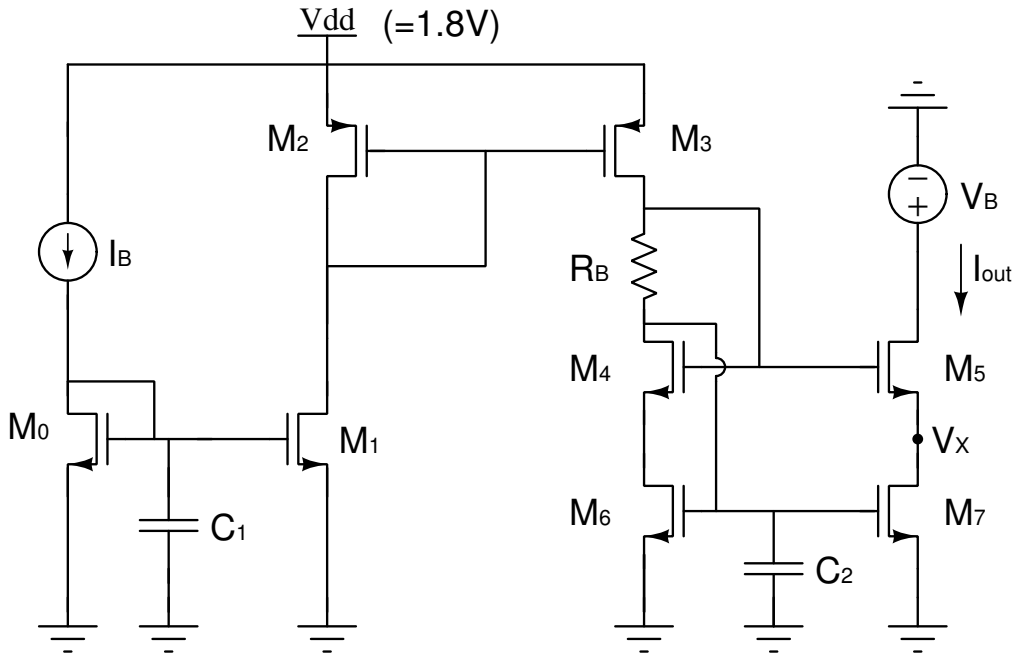

Figure 3: High-swing cascode current mirror

Let's amplify! ☺