EE669: VLSI Technology

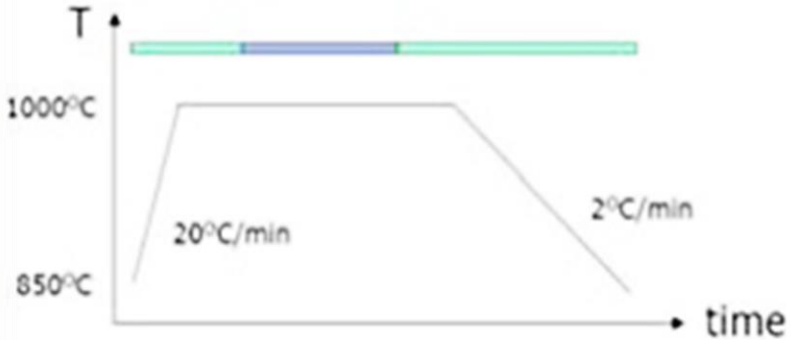
Apurba Laha
Department of Electrical Engineering
IIT Bombay 400076

Email: laha@ee.iitb.ac.in, Tel: **022 25769408**

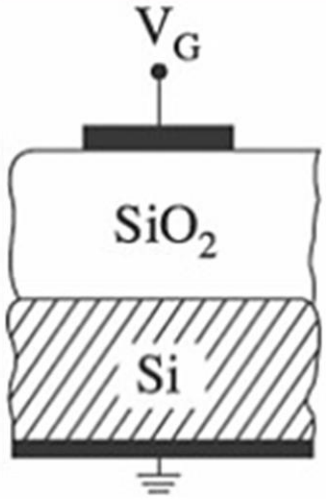
Office hour: Friday 10:00 – 11.00 AM, EE Annex, Room: 104

Thermal oxidation in practice

1. Clean the wafers (RCA clean, very important)
2. Put wafers in the boat
3. Load the wafers in the furnace
4. Ramp up the furnace to process temperature in N_2 (prevents oxidation from occurring)
5. Stabilize
6. Process (wet or dry oxidation)
7. Anneal in N_2. Again, nitrogen stops oxidation process.
8. Ramp down



Electrical thickness measurement: C-V of MOSFET



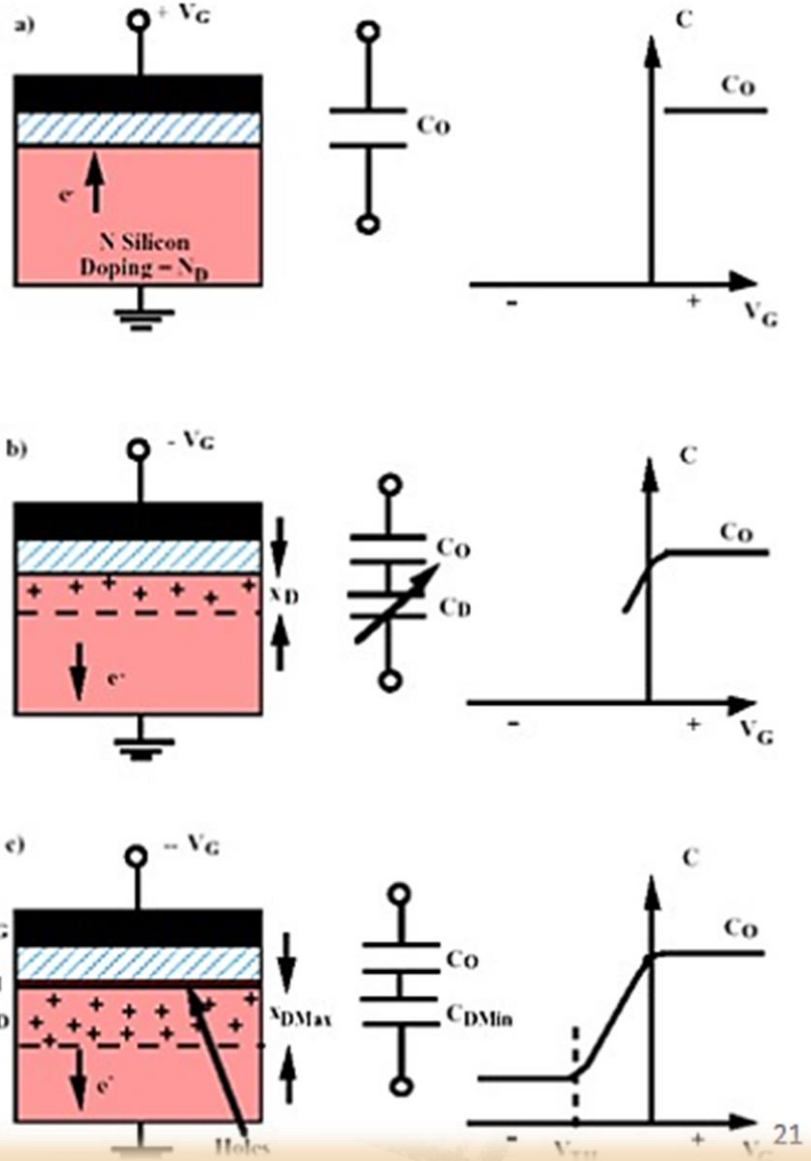
Small *AC* voltage is applied on top of the DC voltage for capacitance measurement.

Substrate is N-type. Electron is majority carrier, hole is minority carrier.

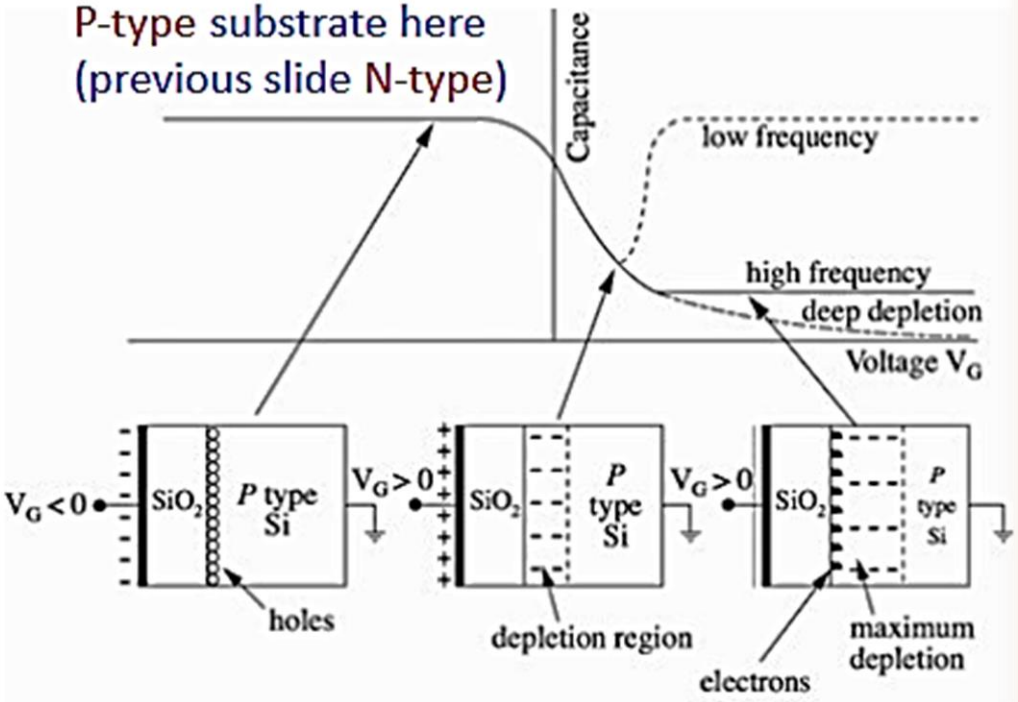
a. Accumulation: positive gate voltage attracts electrons to the interface.

b. Depletion: negative gate bias pushes electrons away from interface. No charge at interface. Two capacitance in series.

c. Inversion: further increase (negative) gate voltage causes holes to appear at the interface.



Effect of frequency for AC capacitance measurement



$$C_{min} = \frac{C_{ox} C_{Si}}{C_{ox} + C_{Si}}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}, C_{Si} = \frac{\varepsilon_{Si}}{X_d}, X_d = \sqrt{\frac{2\varepsilon_{Si}\phi_s}{qN_a}}$$

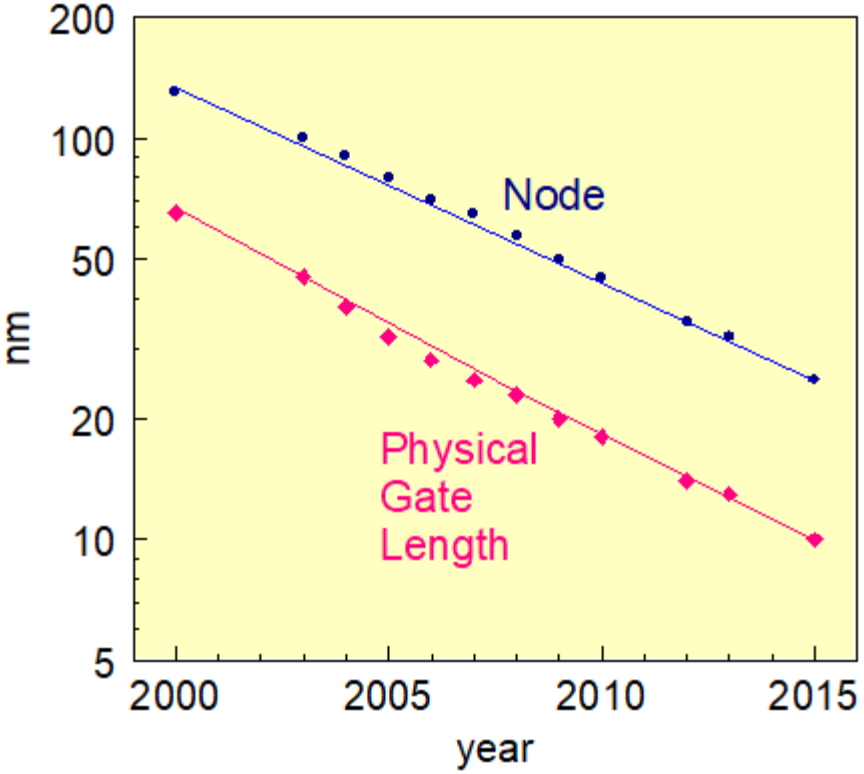
New Materials in Advanced CMOS

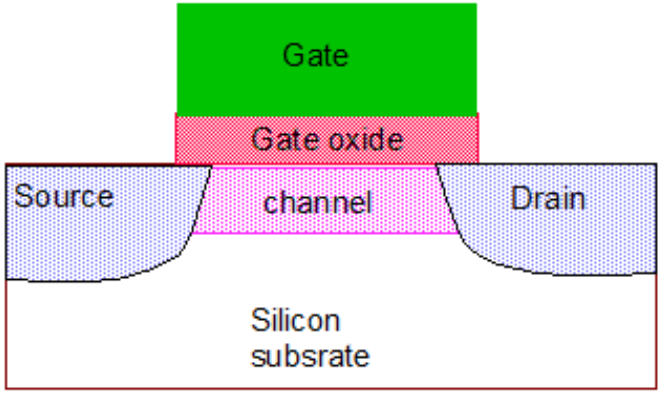
Hunt for new oxide to replace SiO_2 that served as gate dielectric over 3 decades

CMOS scaling

Moore's Law :

- **x2 more devices/wafer every 2 years**
- **Feature size decreases by x2 every 6 years**
- **ITRS roadmap shows the expected reduction in device dimensions or 'node'**

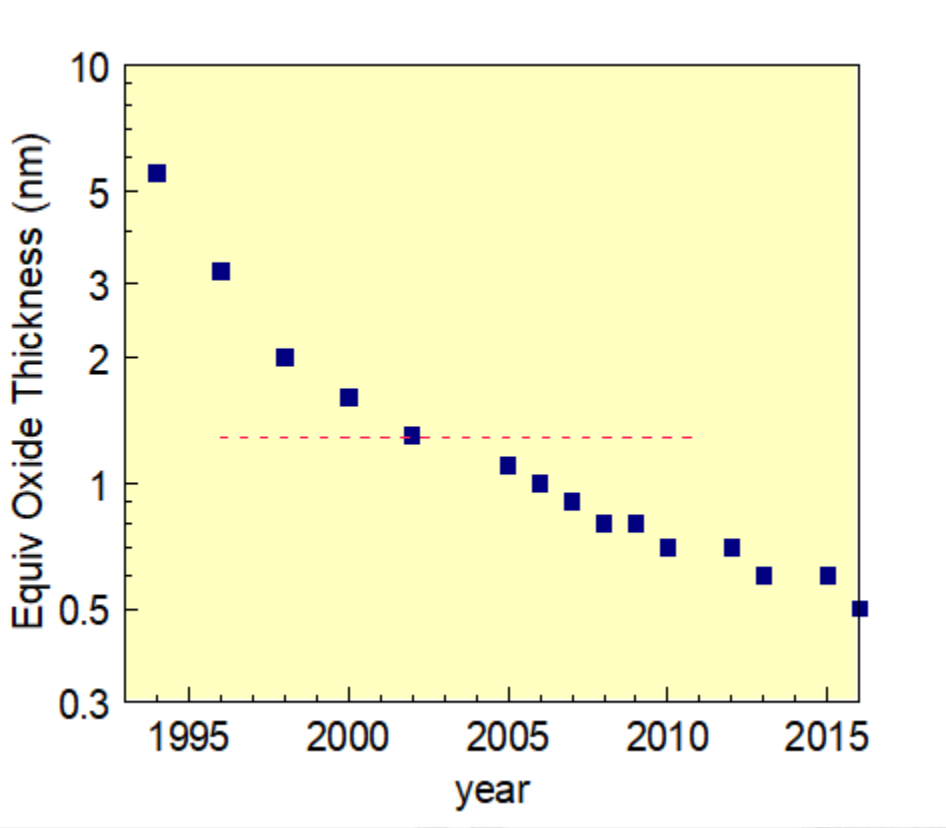


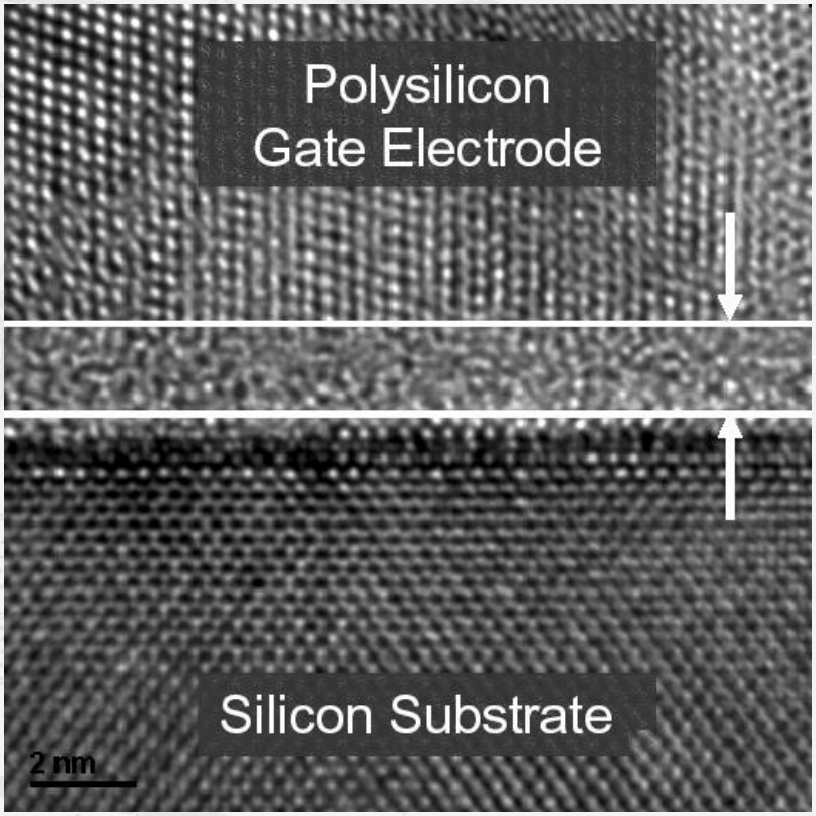


Limits to Scaling

- Lithography
- Materials
  - High dielectric constant (K) gate oxide
  - Metal gates
  - High mobility channel - Strained Si, Ge
  - Dopant activation
  - Low K inter-metal dielectrics ($SiOC_x$)
  - Electromigration – use of Cu
  - Silicon-on insulator
- Power dissipation
- Novel device structures

Gate Oxide Thickness





- SiO_2 gate oxide is only 1.2 nm thick – very ‘Nano’
- only 5 atomic layers thick

High-k, Quantum Mechanical Tunneling and Gate Leakage

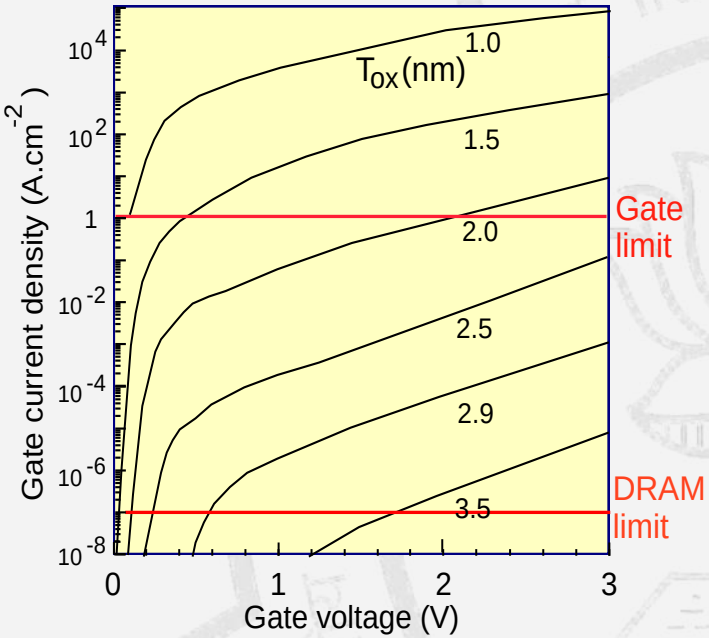
"High-k" stands for high dielectric constant, a measure of how much charge a material can hold

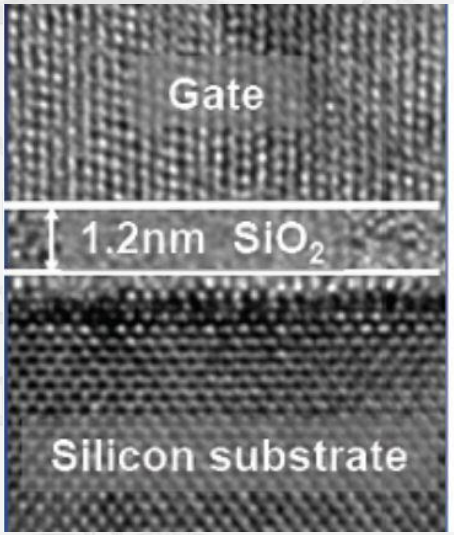
Air is the reference point for this constant and has a "k" of 1.0.

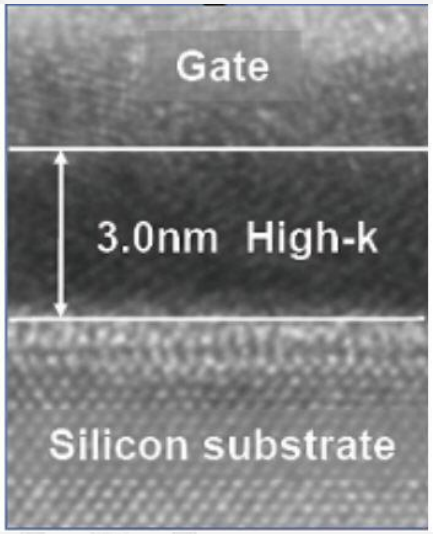
Silicon dioxide (the "old-fashioned" gate material) has a "k" of 3.9.

"High-k" materials, such as Hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2) and titanium dioxide (TiO_2) have "k" values higher than 3.9

Why High K oxides ?





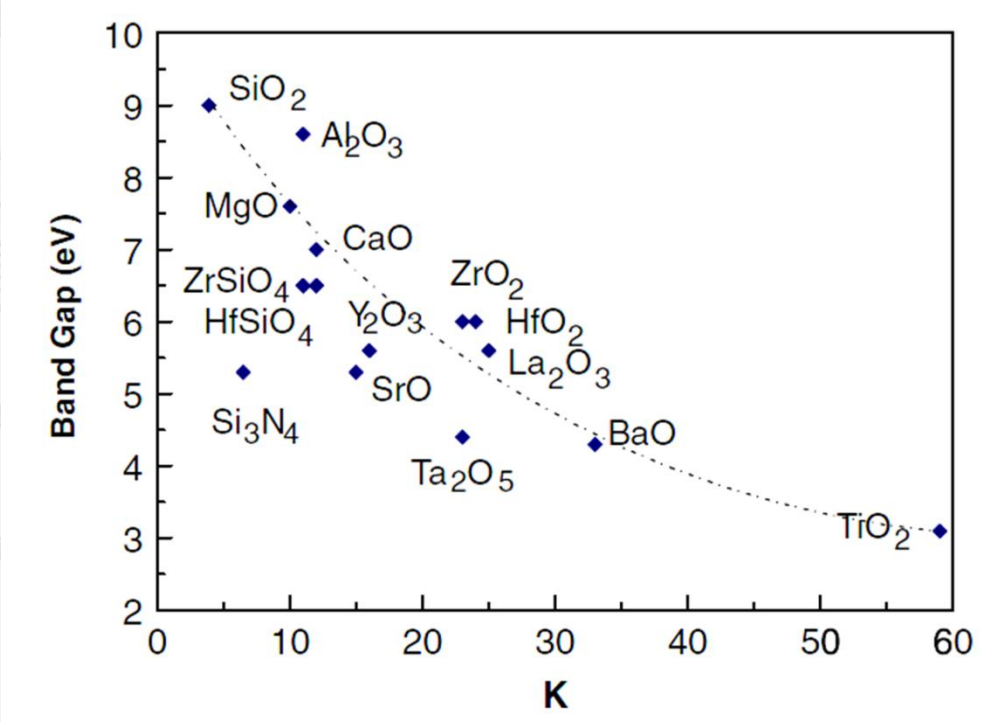


- **SiO_2 layers <1.6 nm have high leakage current due to direct tunnelling. Not insulating**
- **Maintain C/area for S-D current** $C = \frac{K\varepsilon_0}{t}$
- **Replace SiO_2 with thicker layer of new oxide with higher K**
- **Equivalent oxide thickness 'EOT'**

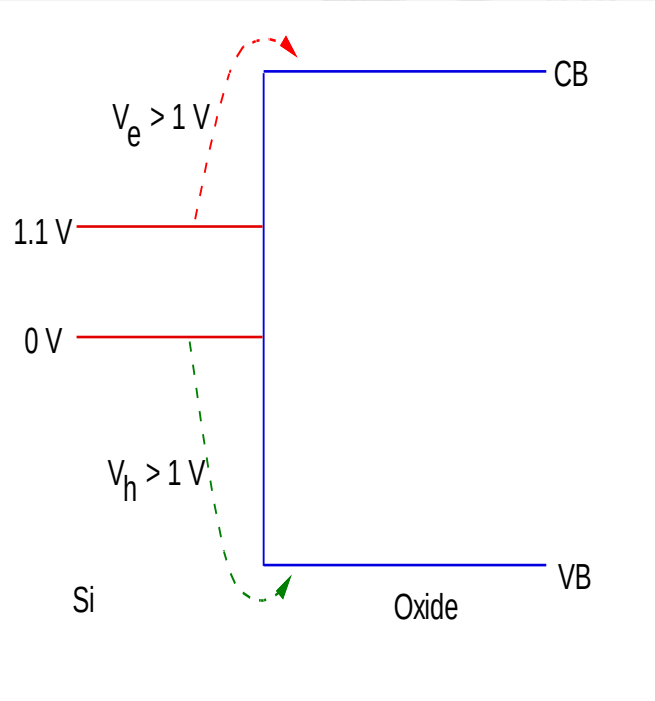
Choice of High K Oxide

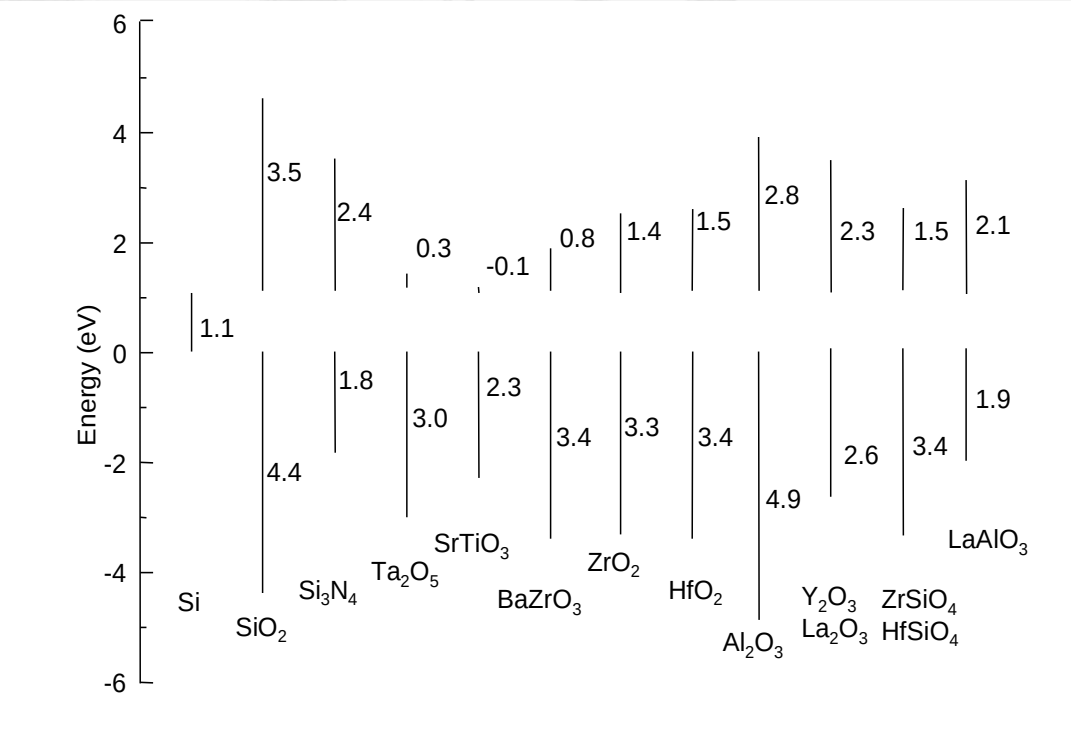
5 conditions -

- High enough dielectric constant K
- Stable - no reaction with Si
  - Oxides with high heat of formation
  - Preferred – HfO_2, Zr, Y, La, Al
- Stable up to 1050^0C
  - Low diffusion,
  - Amorphous $HfSiO_x$:N
- Band Offsets
  - Wide band gap
- Good interface
  - Few defects



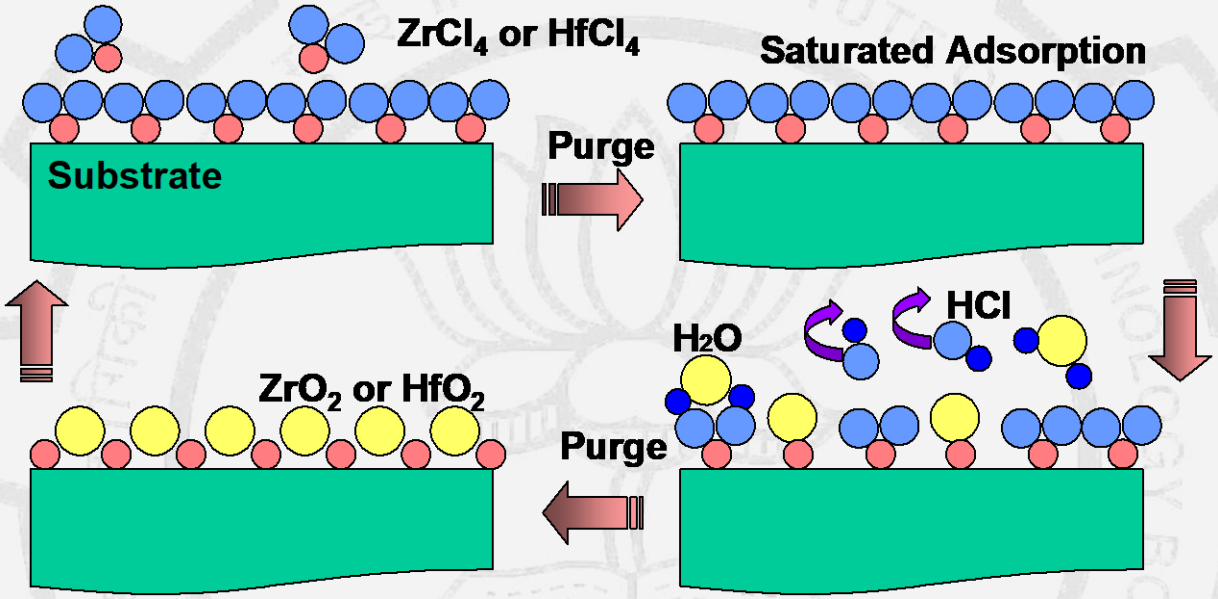
Band Offsets are a key criterion





- **Band offsets should be > 1 V**
- **Measured by photoemission; Calculated with Charge Neutrality Levels**
- **J Robertson, J Vac Sci Technol B 18 1785 (2000)**

New Oxides are deposited: e.g. Atomic Layer Deposition



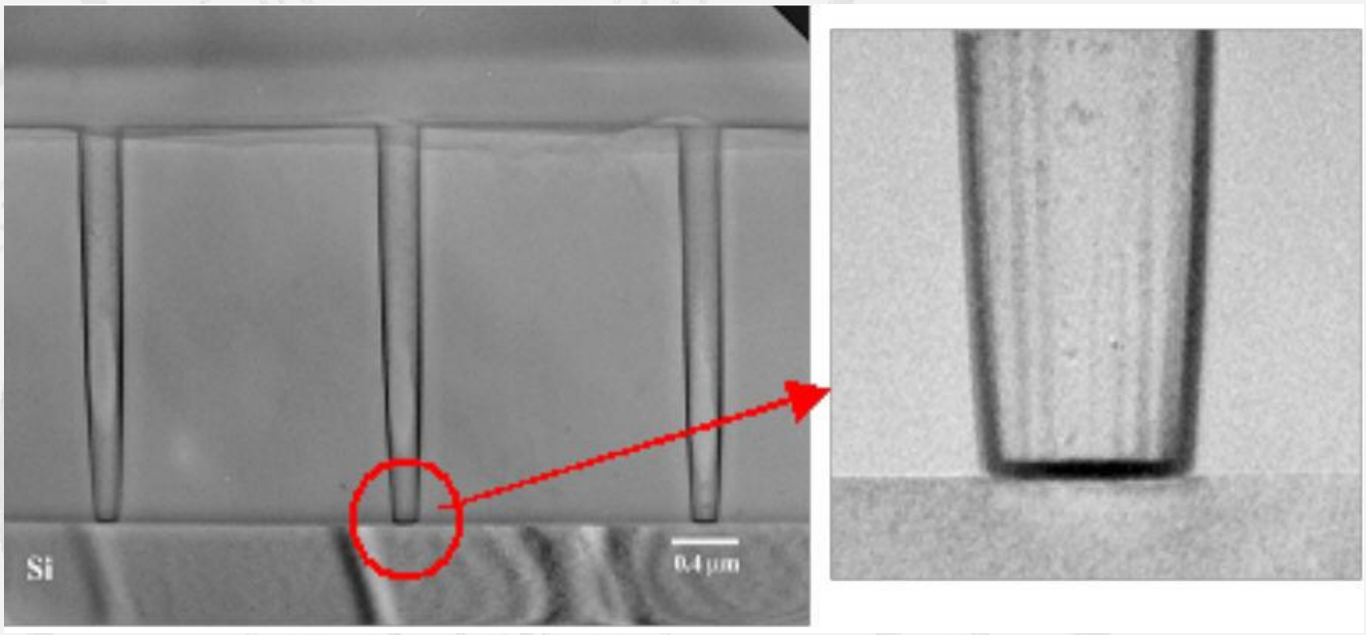
$ZrCl_4(ad.) + 2H_2O(g) \rightarrow ZrO_2(s) + 4HCl(g)$

$HfCl_4(ad.) + 2H_2O(g) \rightarrow HfO_2(s) + 4HCl(g)$

- Cyclic process of controlled by surface-saturation
- But sub-monolayer despite name

- Important industrial sector of designing precursor chemicals (Epichem..)

ALD gives highly conformal films



P McIntyre, Stanford

- Surface saturation
  - Excellent step coverage
- No pin-holes – no electrical breakdown
- Nucleates only on oxide coated Si

Scaling!!!! Moore's Law

Expected to be running into severe road block (When??)

$$t_{eq} = \left(\frac{\varepsilon_{rSiO_2}}{\varepsilon_{rlow-K}} \right) t_{low-K} + \left(\frac{\varepsilon_{rSiO_2}}{\varepsilon_{rhigh-K}} \right) t_{high-K}$$

Limit ultimate scaling

"Moore's law, the dogmatized observation that device size was shrinking exponentially with time, will soon prove not to be a law after all, but just a rule, temporarily relevance to some industries." Horst. L Stormer, Nobel Laureate in Physics 1998

Hunting begins!!!

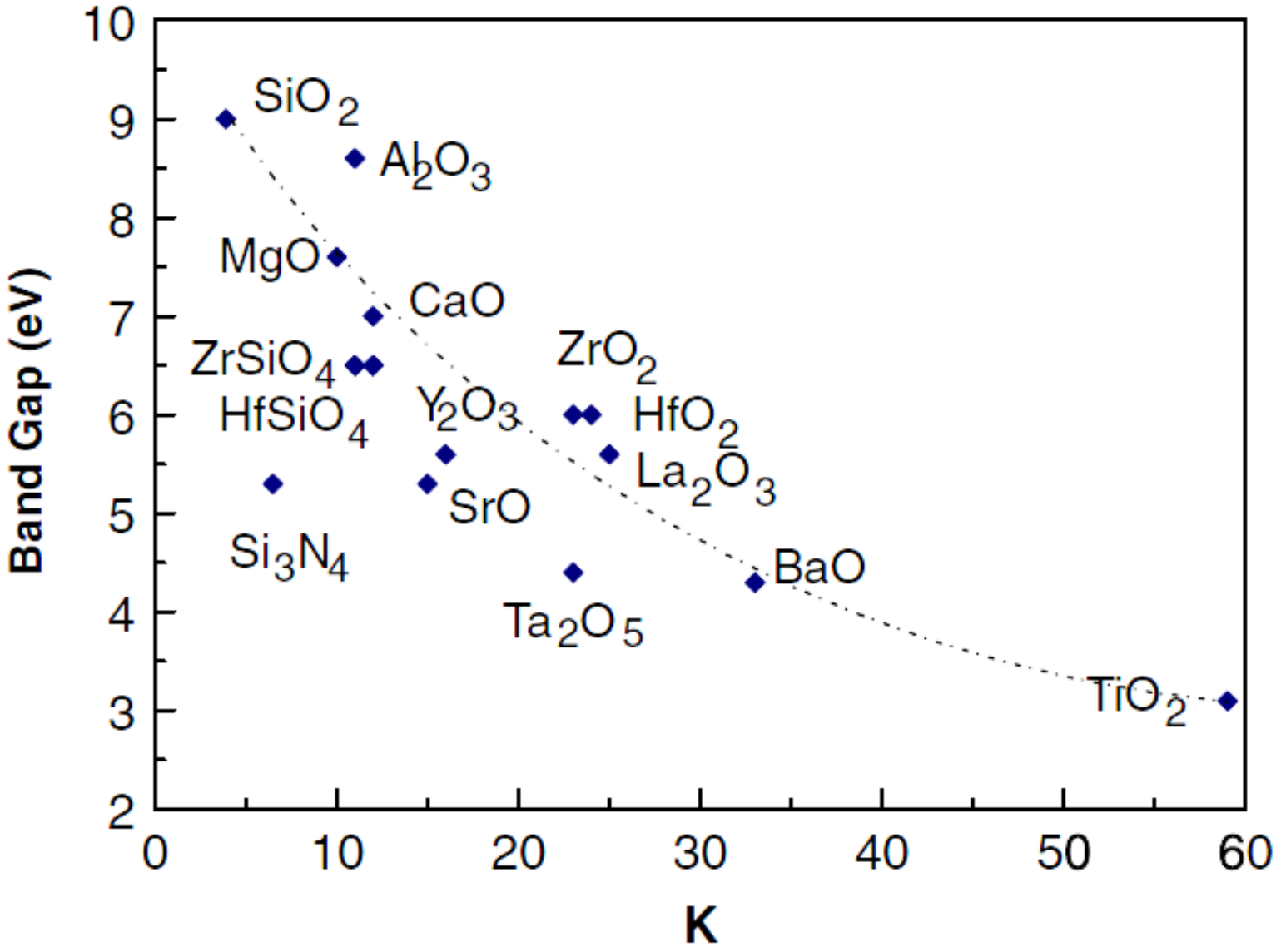
Crystalline Oxides on Silicon: The First Five Monolayers

https://link.aps.org/pdf/10.1103/PhysRevLett.81.3014

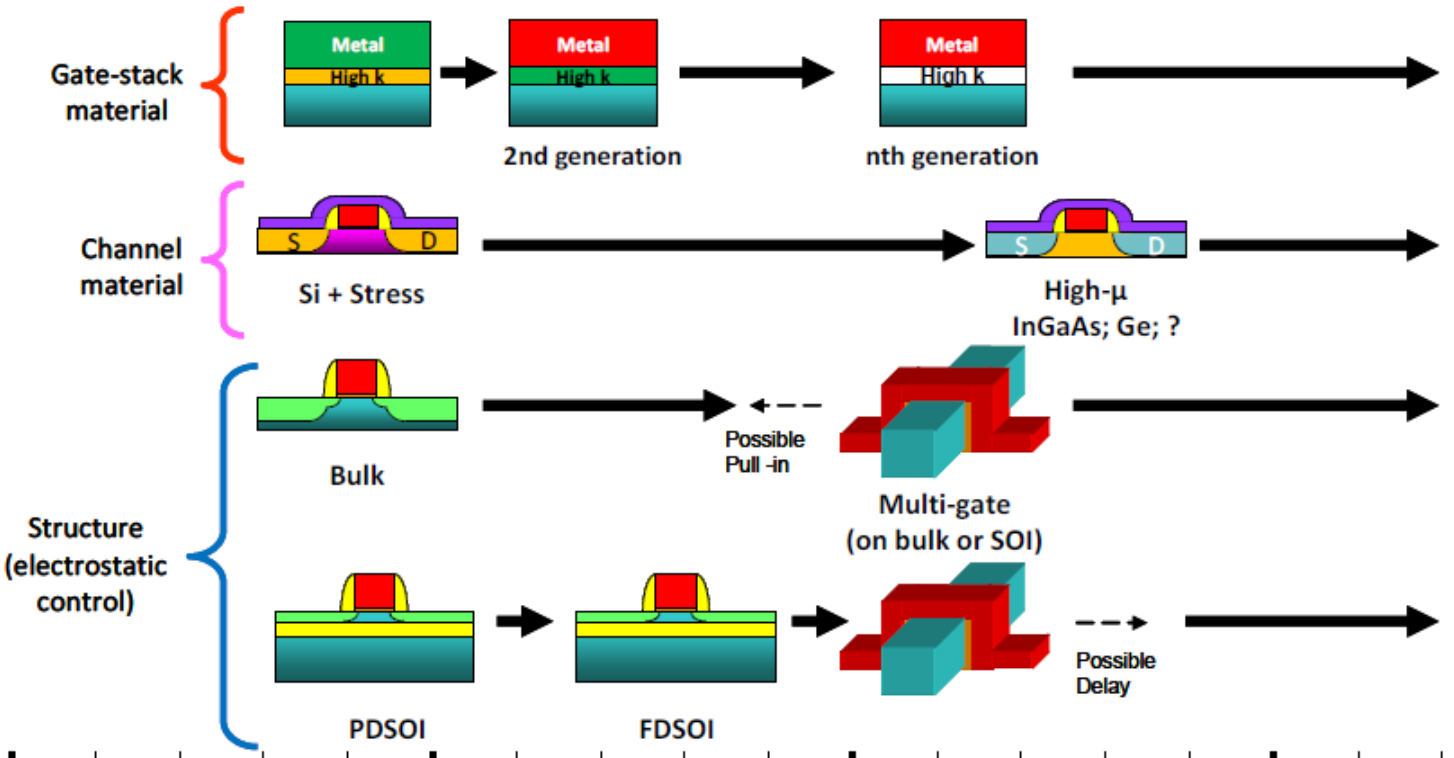
by RA McKee - 1998 - Cited by 1054 - Related articles

Oct 5, 1998 - In what follows, we will describe the **first five monolayers** of a structure transition from **silicon** to an ionic **oxide**. ... Capacitance/voltage for a SrTiO3 Si capacitor. The SrTiO3 is 150 Å thick, and with p-type **silicon** the capacitance of the **oxide** is obtained with **silicon** in accumulation at negative voltages.

Intel made a significant breakthrough in the 45nm process by using a "high-k" (Hi-k) material called hafnium to replace the transistor's silicon dioxide gate dielectric


Band Gap (eV)
K
10
9
8
7
6
5
4
3
2
0
10
20
30
40
50
60
SiO2
Al2O3
MgO
CaO
ZrSiO4
HfSiO4
Y2O3
ZrO2
HfO2
La2O3
SrO
Si3N4
BaO
Ta2O5
TiO2

TREND	*EXAMPLE*
Integration Level	Components/chip, Moore's Law
Cost	Cost per function
Speed	Microprocessor throughput
Power	Laptop or cell phone battery life
Compactness	Small and light-weight products
Functionality	Nonvolatile memory, imager



2009 ITWG Table Timing:	2007		2010		2013		2016		2019	2021
2009 IS ITRS Flash Poly :	54nm	45nm	2009	32nm	2012	22nm	2015	16nm	2018	11nm	2021
2009 IS ITRS DRAM M1 :	68nm			45nm		32nm		22nm		16nm	
MPU/hpASIC "Node":	"45nm"		"32nm"		"22nm"		"16nm"		"11nm"	"8nm"	
2009 ITRS MPU/hpASIC M1 :	76nm	65nm	54nm	45nm	38nm	32nm	27nm		19nm	13nm	
2009 ITRS hi-perf GLpr :	54nm	47nm	47nm	41nm	35nm	31nm	28nm		20nm	14nm	
2009 ITRS hi-perf GLph :	32nm	29nm	29nm	27nm	24nm	22nm	20nm		15nm	12nm	