EE669: VLSI Technology

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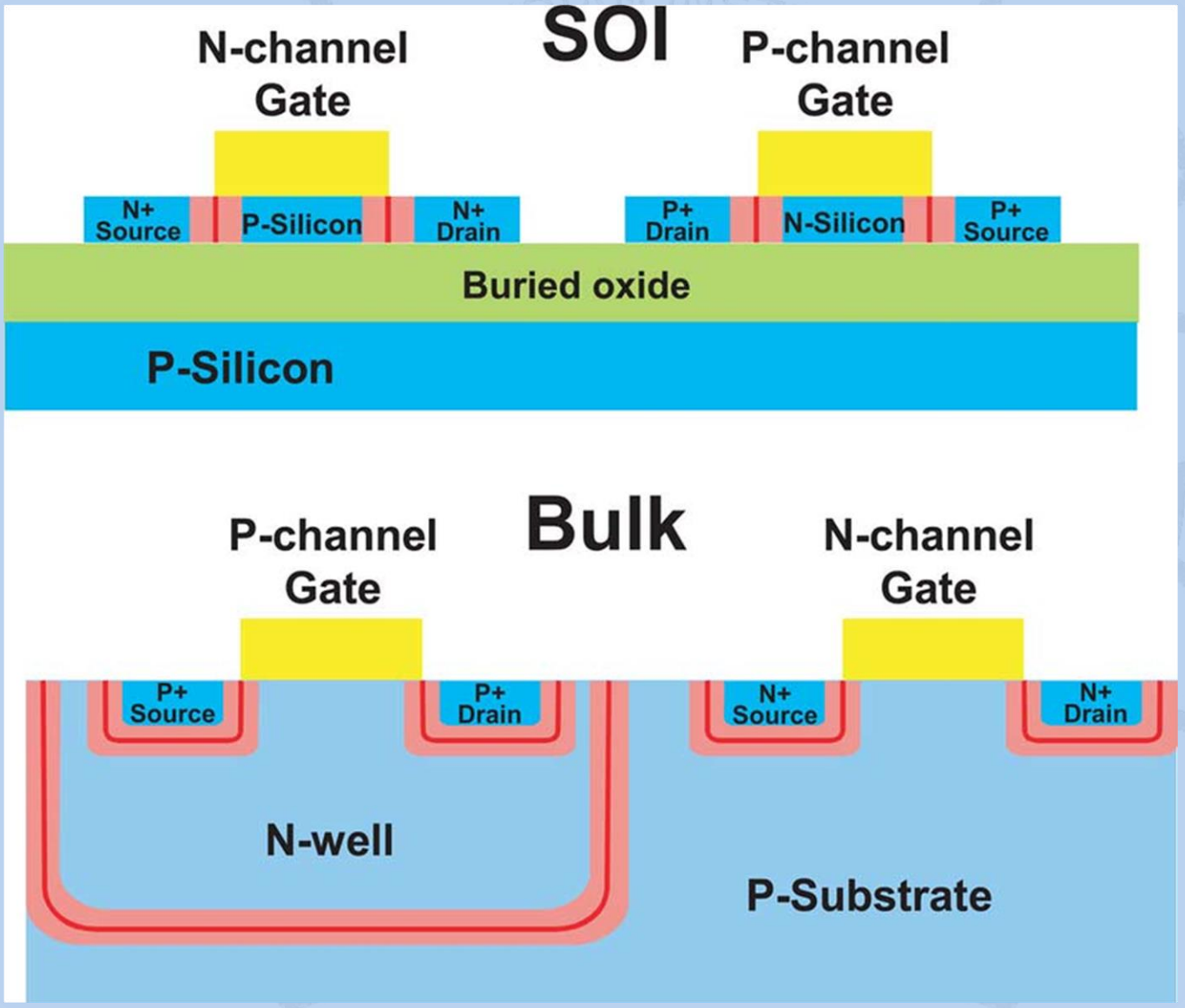
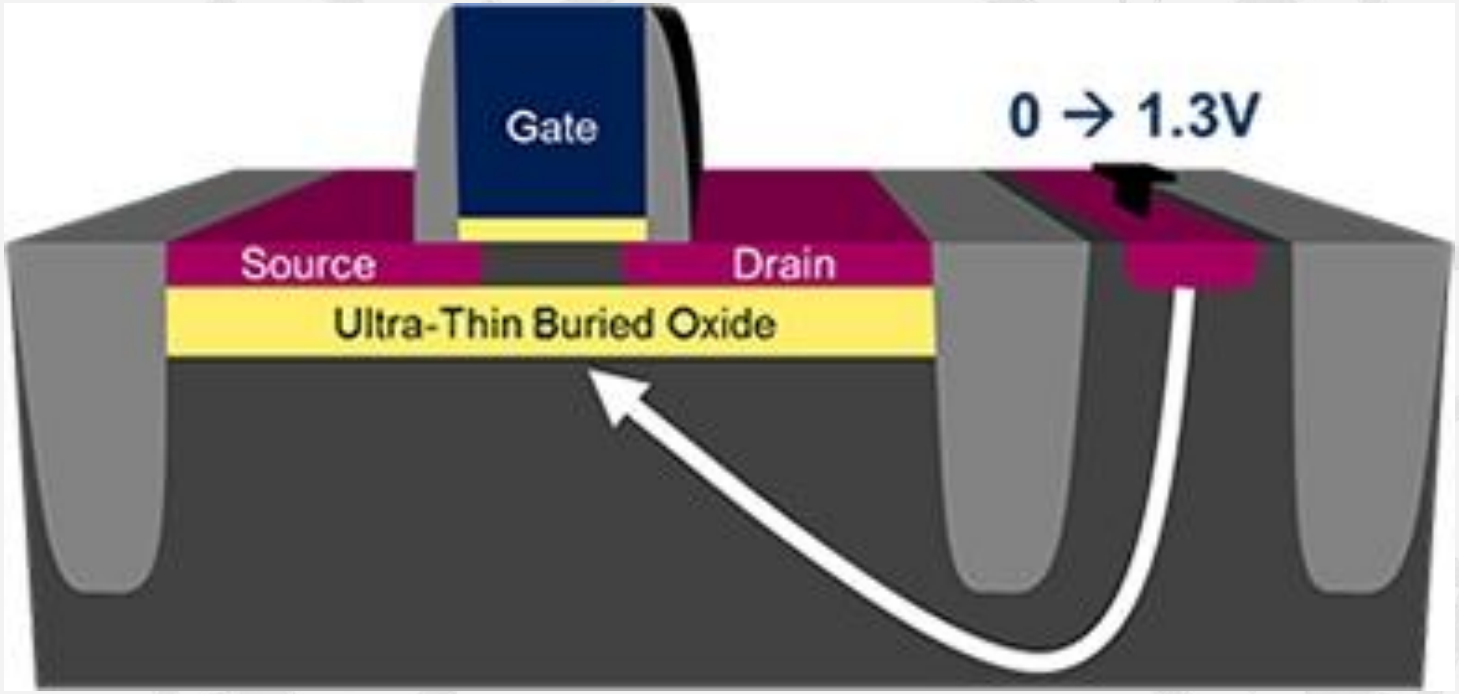
Office hour: Friday 10:00 – 11.00 AM, EE Annex, Room: 104

SOI transistors

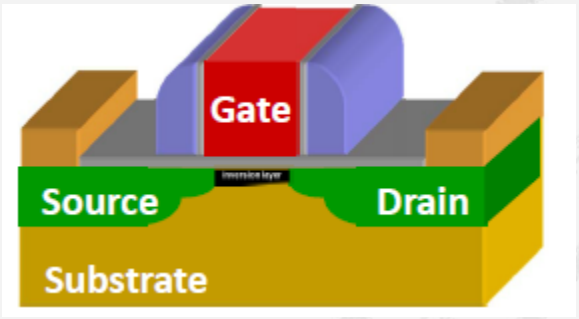


Ref: IEEE Transactions on Nuclear Science **55(4)**:1833 - 1853 · September 2008

FD-SOI allows efficient transistor control



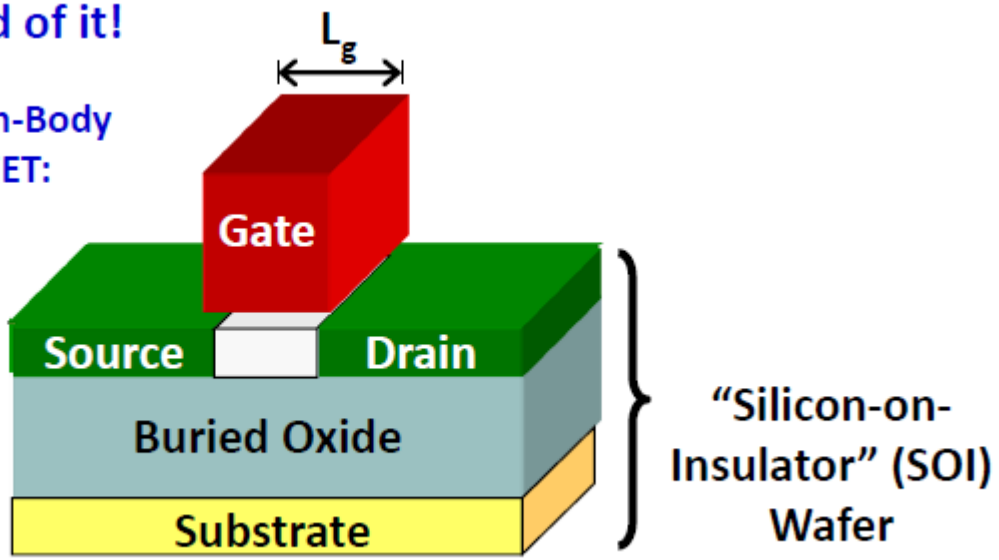
Why New Transistor Structures?



- Off-state leakage (I_{OFF}) must be suppressed as L_g is scaled down
  - allows for reductions in V_{TH} and hence V_{DD}
- Leakage occurs in the region away from the channel surface

→ Let's get rid of it!

Ultra-Thin-Body MOSFET:



Thin-Body MOSFETs

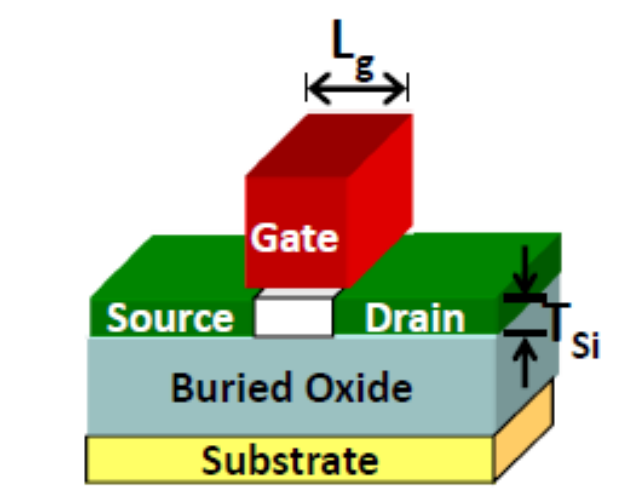
- I_{OFF} is suppressed by using an adequately thin body region.

– Body doping can be eliminated

 higher drive current due to higher carrier mobility

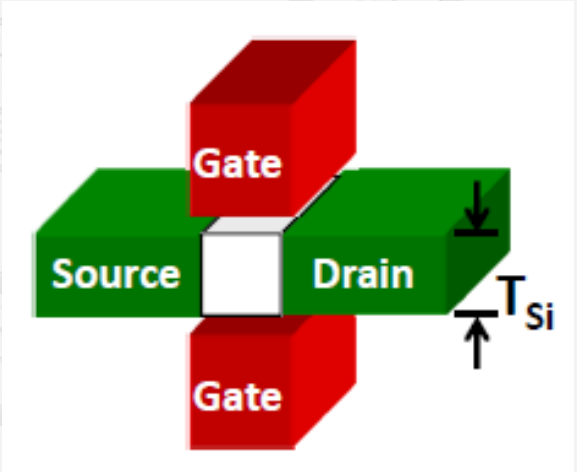
 Reduced impact of random dopant fluctuations (RDF)

Ultra-Thin Body (UTB)



B. Yu *et al.*, *ISDRS* 1997

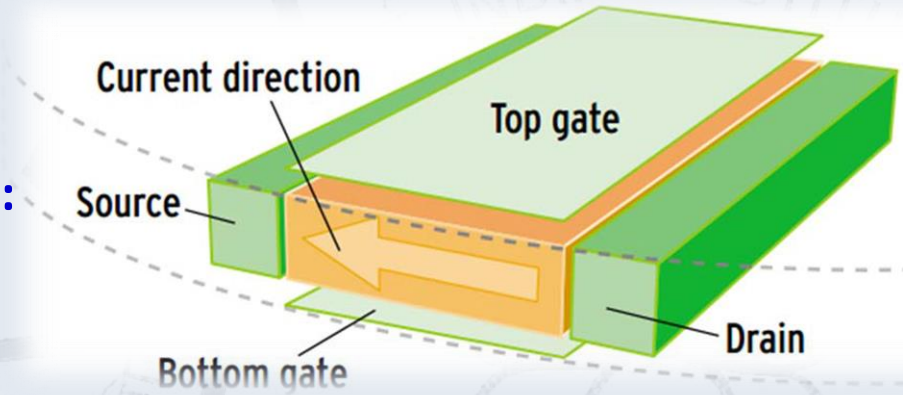
Double-Gate (DG)



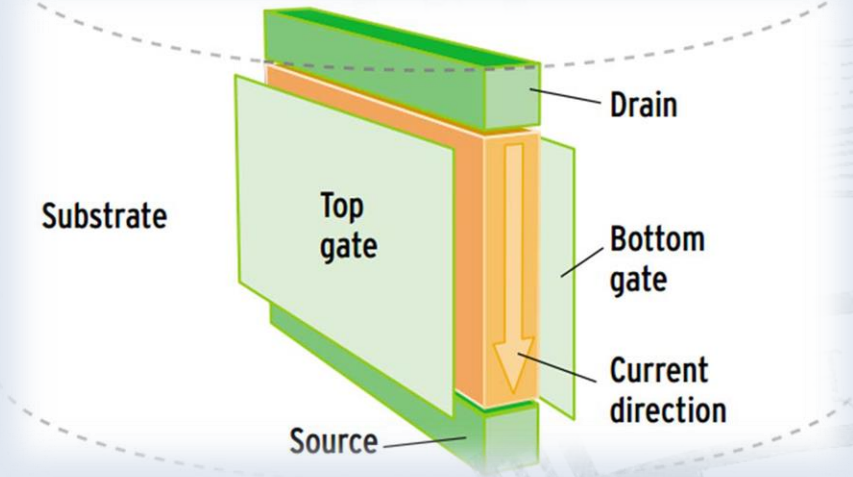
R.-H. Yan *et al.*, *IEEE TED* 1992

Double-Gate MOSFET Structures

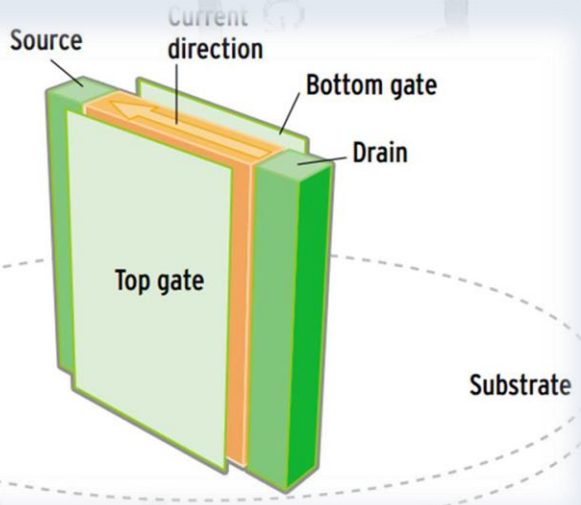
PLANAR:



VERTICAL

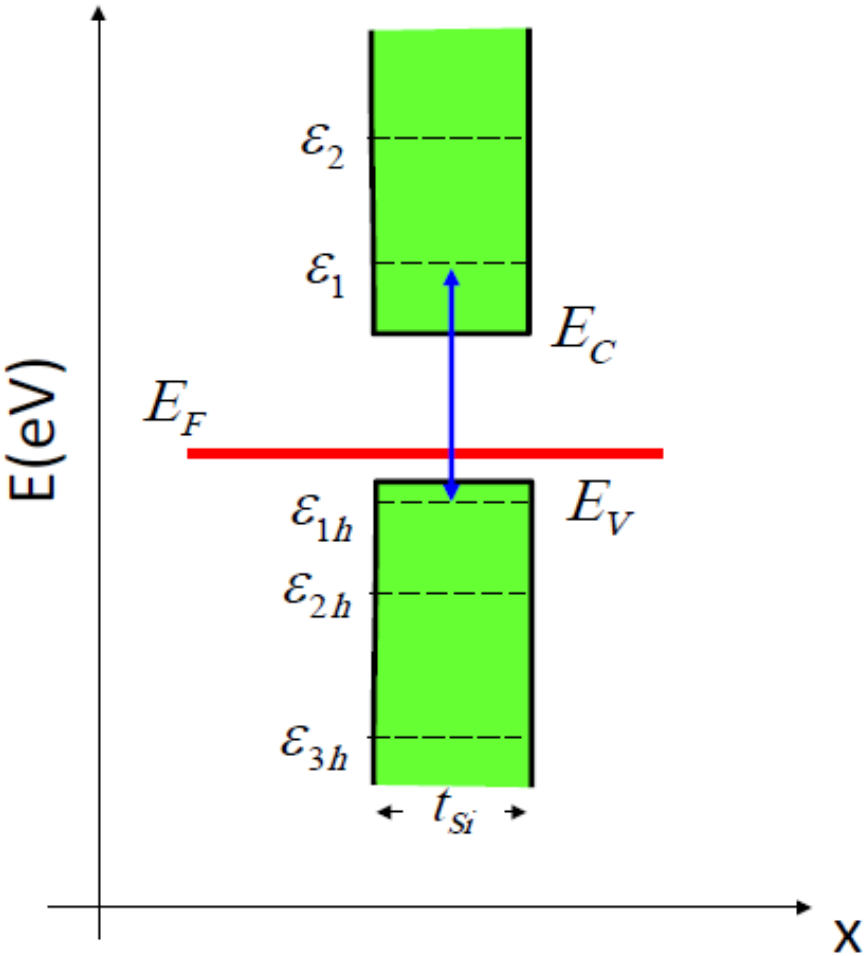


FIN:



Reference: **L. Geppert, *IEEE Spectrum*, October 2002**

Fin-FET and Quantum effect



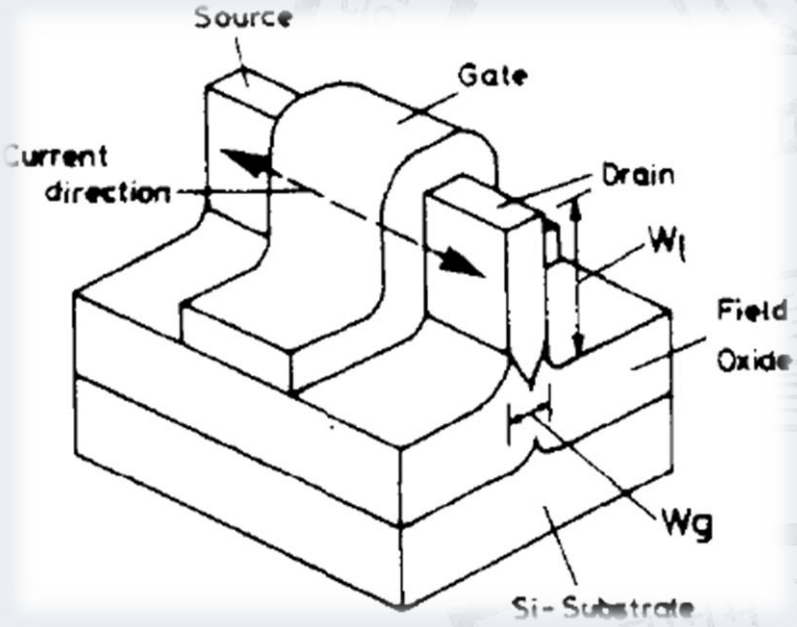
$$\varepsilon_n = \frac{h^2 n^2 \pi^2}{2 m^* t_{Si}^2}$$

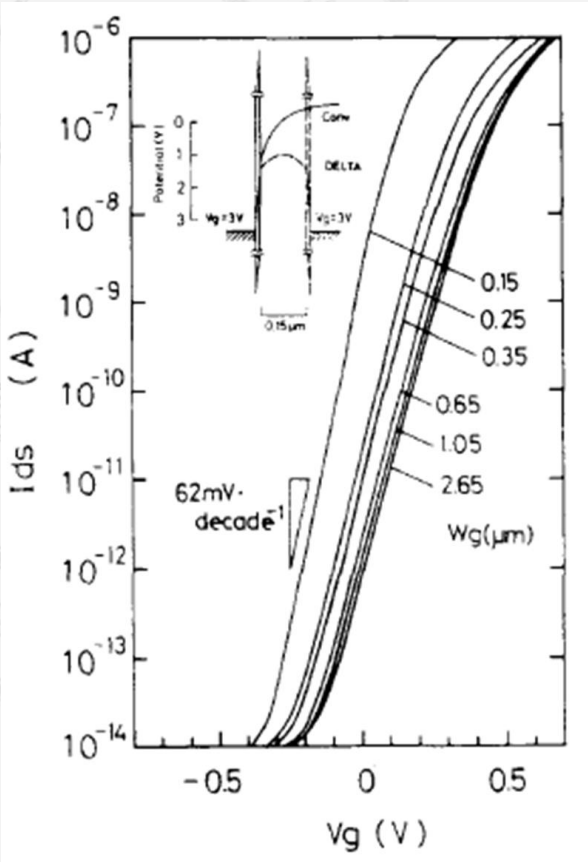
$$E_G' = E_G + \varepsilon_1 + \varepsilon_{1h}$$

Band-gap widening
Fluctuation in thickness

DELTA MOSFET

D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda (Hitachi Central Research Laboratory), "A fully depleted lean-channel transistor (DELTA) – a novel vertical ultrathin SOI MOSFET," *IEEE Electron Device Letters* Vol. 11, pp. 36-39, 1990

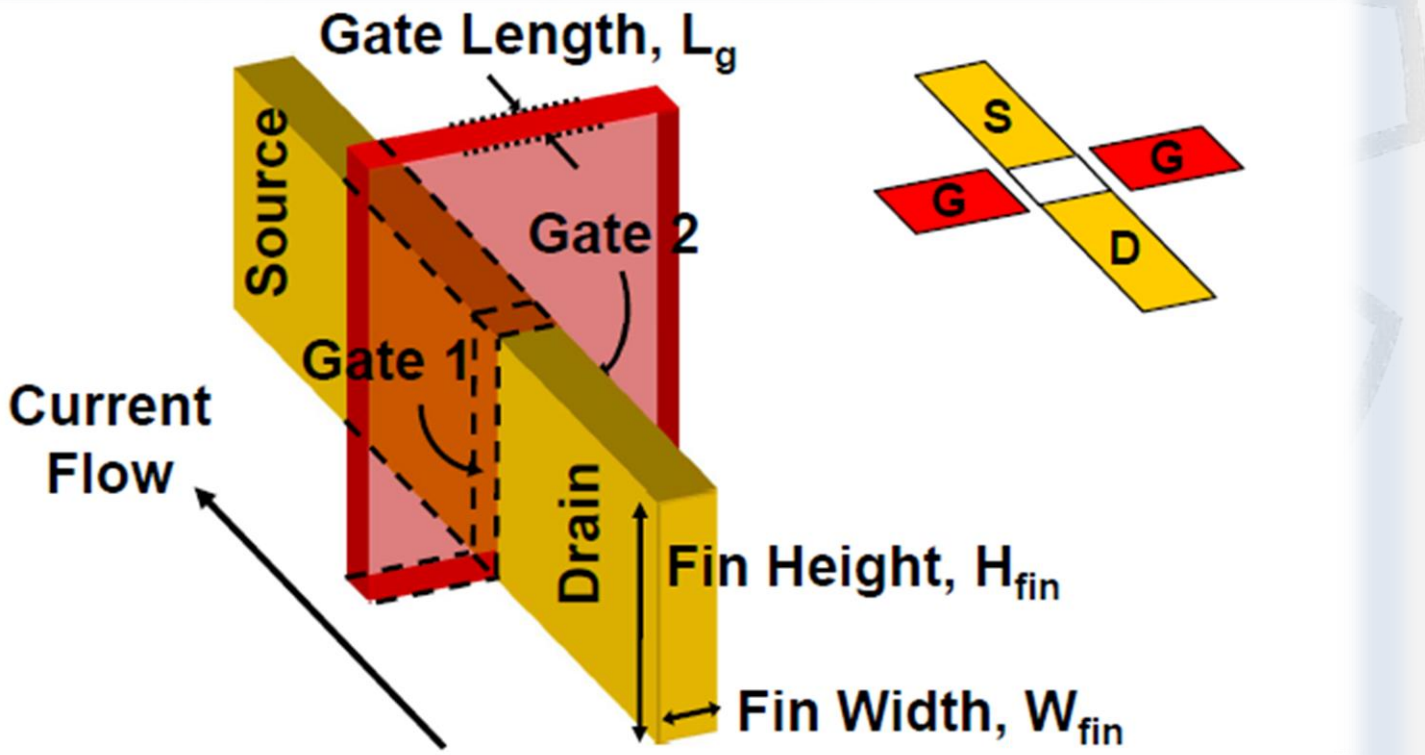




- Improved gate control observed for $W_g < 0.3\ \mu m$
  – $L_{eff} = 0.57\ \mu m$

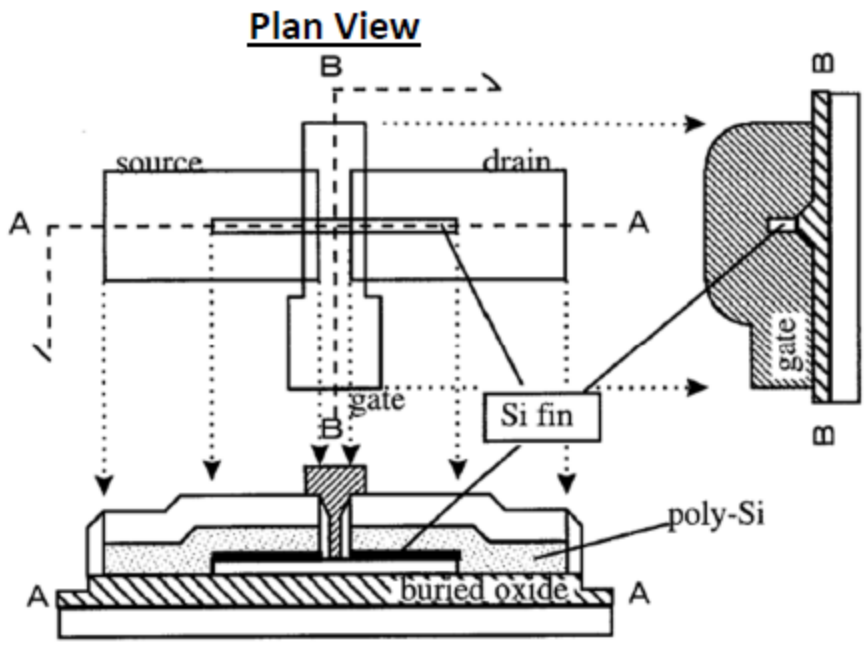
Double-Gate FinFET

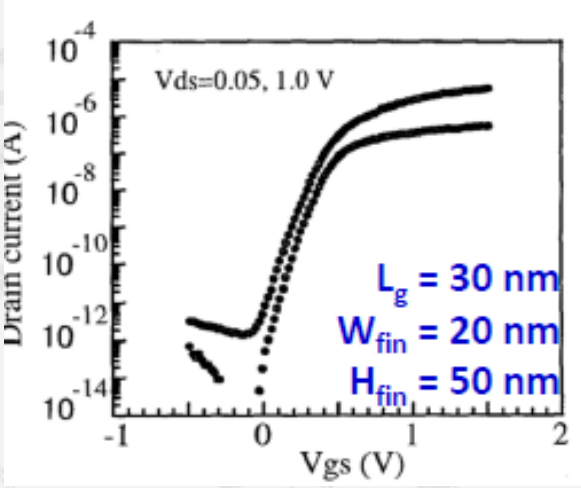
- Self-aligned gates straddle narrow silicon fin
- Current flows parallel to wafer surface

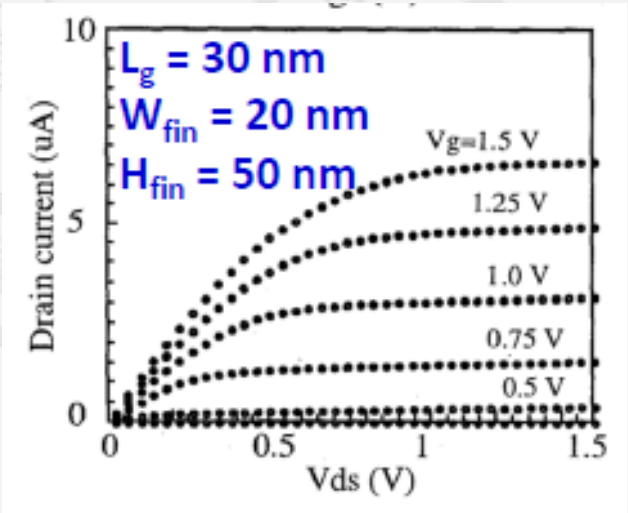


1998: First N-channel FinFETs

D. Hisamoto et al. "A folded-channel MOSFET for deep-sub-tenth micron era,"
***IEEE International Electron Devices Meeting Technical Digest*, pp. 1032-1034, 1998**







Devices with L_g down to 17 nm were successfully fabricated

1999: First P-channel FinFETs

X. Huang et al. "Sub 50-nm FinFET: PMOS," ***IEEE International Electron Devices Meeting Technical Digest*****, pp. 67-70, 1999**

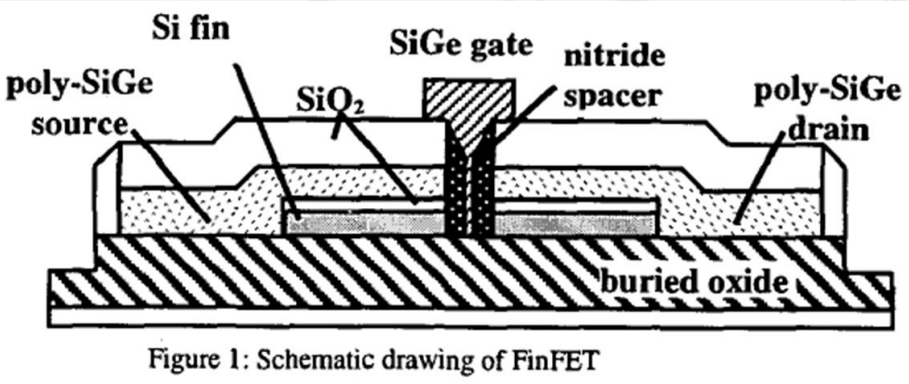
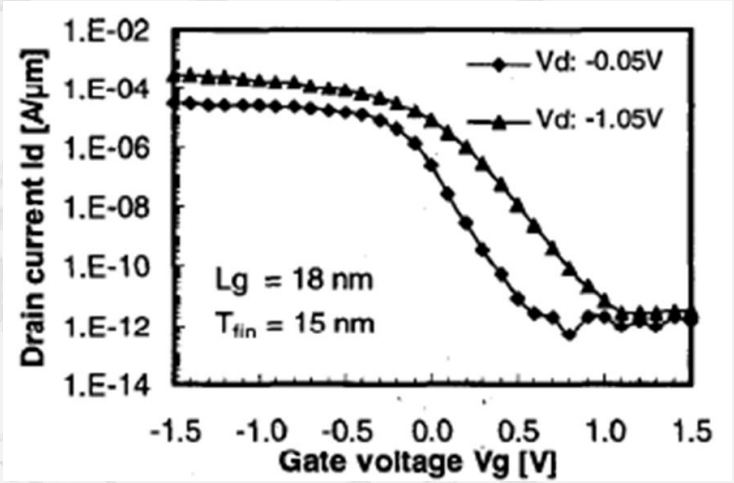
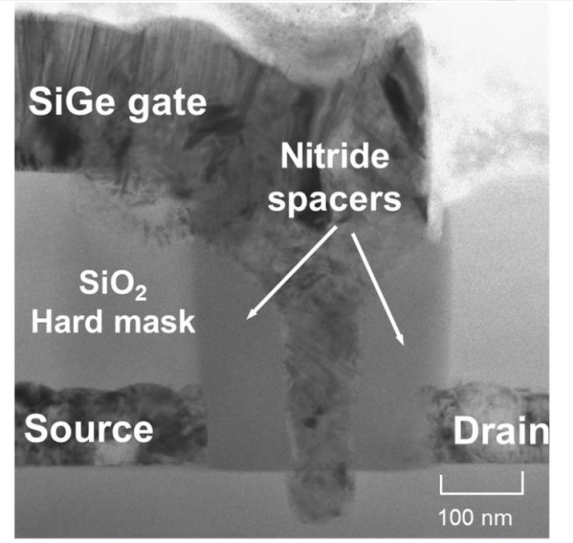
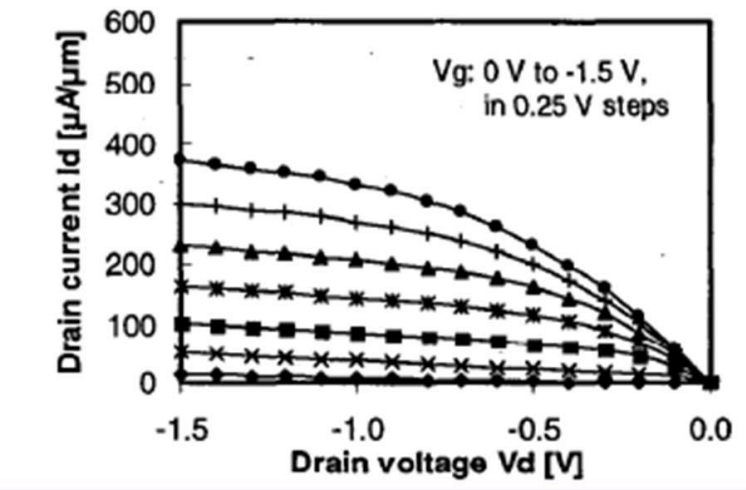


Figure 1: Schematic drawing of FinFET





Transmission Electron Micrograph



2000: Commercial Interest from Industry

- **Semiconductor Research Corporation (SRC) & AMD fund project:**
  - **Development of a FinFET process flow compatible with a conventional planar CMOS process**
  - **Demonstration of the compatibility of the FinFET structure with a production environment**

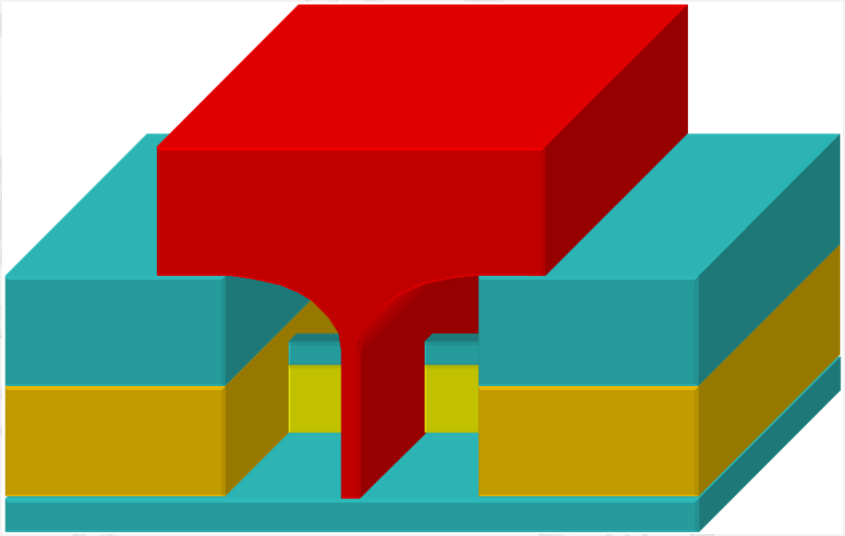
  (October 2000 through September 2003)
- **DARPA/SRC Focus Center Research Program funds projects:**
  - **Approaches for enhancing FinFET performance**

  (MSD Center, April 2001 through August 2003)
  - **FinFET-based circuit design**

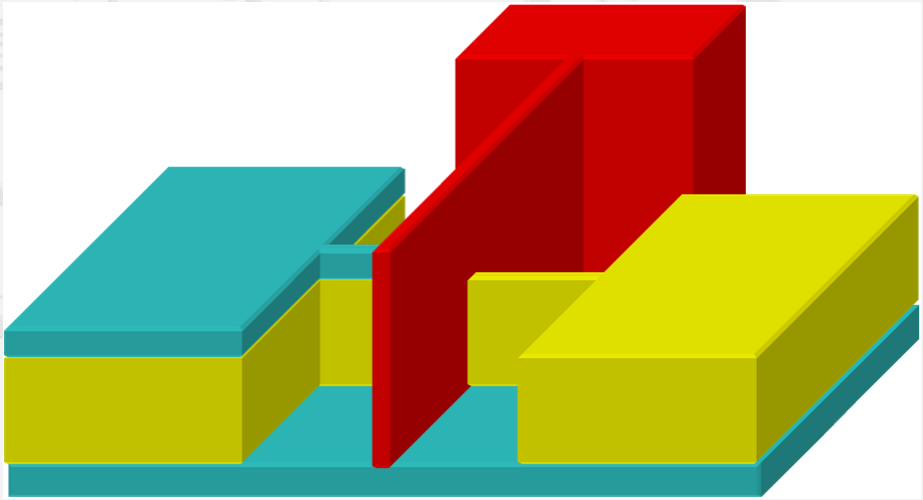
  (C2S2 Center, August 2003 through July 2006)

FinFET Structures

Original:
Gate-last process flow



Improved:
Gate-first process flow

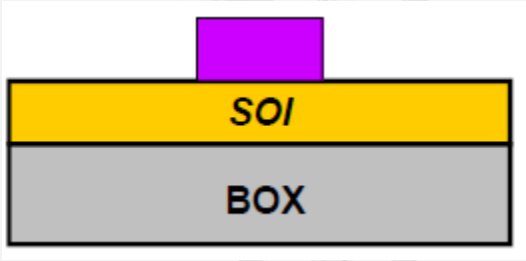


Sub-Lithographic Fin Patterning

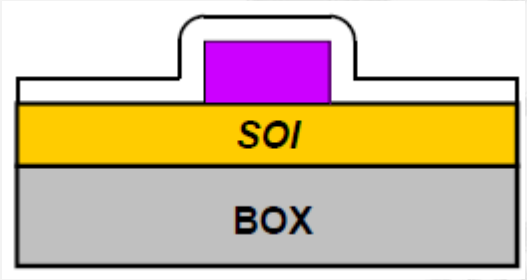
Spacer Lithography

Sidewall Image Transfer (SIT) and Self-Aligned Double Patterning (SADP)

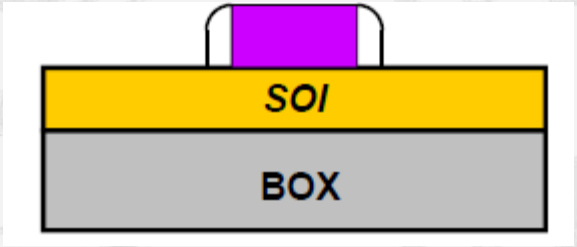
1. Deposit & pattern sacrificial layer



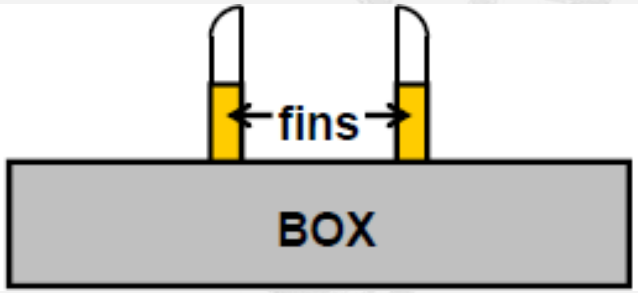
2. Deposit mask layer (SiO2 or Si3N4)



3. Etch back mask layer to form "spacers



4. Remove sacrificial layer; etch SOI layer to form fins



FinFET with High mobility and Strained Channel

US008729634B2

(12) **United States Patent**
Shen et al.

(10) **Patent No.: US 8,729,634 B2**
(45) **Date of Patent: May 20, 2014**

(54) **FINFET WITH HIGH MOBILITY AND STRAIN CHANNEL**

(75) Inventors: **Chun-Liang Shen**, New Taipei (TW); **Kuo-Ching Tsai**, Hsin-Chu (TW); **Hou-Ju Li**, Hsin-Chu (TW); **Chun-Sheng Liang**, Changhua County (TW); **Kao-Ting Lai**, Hsin-Chu (TW); **Kuo-Chiang Ting**, Hsinchu (TW); **Chi-Hsi Wu**, Hsinchu (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsin-Chu (TW)

FOREIGN PATENT DOCUMENTS

JP	2006-516821	7/2006
KR	10-2006-0130704	12/2006
WO	2004068585	8/2004
WO	2005098963	10/2005

OTHER PUBLICATIONS

Liu, C. W., et al., "Mobility-Enhancement Technologies," IEEE Circuits & Devices Magazine, May/Jun. 2005, pp. 21-36.

Oh, J., et al., "Mechanisms for Low On-State Current of Ge (SiGe) nMOSFETs: A Comparative Study on Gate Stack, Resistance, and Orientation-Dependent Effective Masses," 2009 Symposium on VLSI Technology Digest of Technical Papers, pp. 238-239

Epitaxial growth of strained and high mobility semiconductor plays important role

FinFET with high-k metal gate

High Performance 22/20nm FinFET CMOS Devices with Advanced High-K/Metal Gate Scheme

C.C. Wu, D.W. Lin, A. Keshavarzi, C.H. Huang, C.T. Chan, C.H. Tseng, C.L. Chen, C.Y. Hsieh, K.Y. Wong, M.L. Cheng, T.H. Li, Y.C. Lin, L.Y. Yang, C.P. Lin, C.S. Hou, H.C. Lin, J.L. Yang, K.F. Yu, M.J. Chen, T.H. Hsieh, Y.C. Peng, C.H. Chou, C.J. Lee, C.W. Huang, C.Y. Lu, F.K. Yang, H.K. Chen, L.W. Weng, P.C. Yen, S.H. Wang, S.W. Chang, S.W. Chuang, T.C. Gan, T.L. Wu, T.Y. Lee, W.S. Huang, Y.J. Huang, Y.W. Tseng, C.M. Wu, Eric Ou-Yang, K.Y. Hsu, L.T. Lin, S.B. Wang, T.M. Kwok, C.C. Su, C.H. Tsai, M.J. Huang, H.M. Lin, A.S. Chang, S.H. Liao, L.S. Chen, J.H. Chen, P.S. Lim, X.F. YU, S.Y. Ku, Y.B. Lee, P.C. Hsieh, P.W. Wang, Y.H. Chiu, S.S. Lin, H.J. Tao, M. Cao, Y.J. Mii

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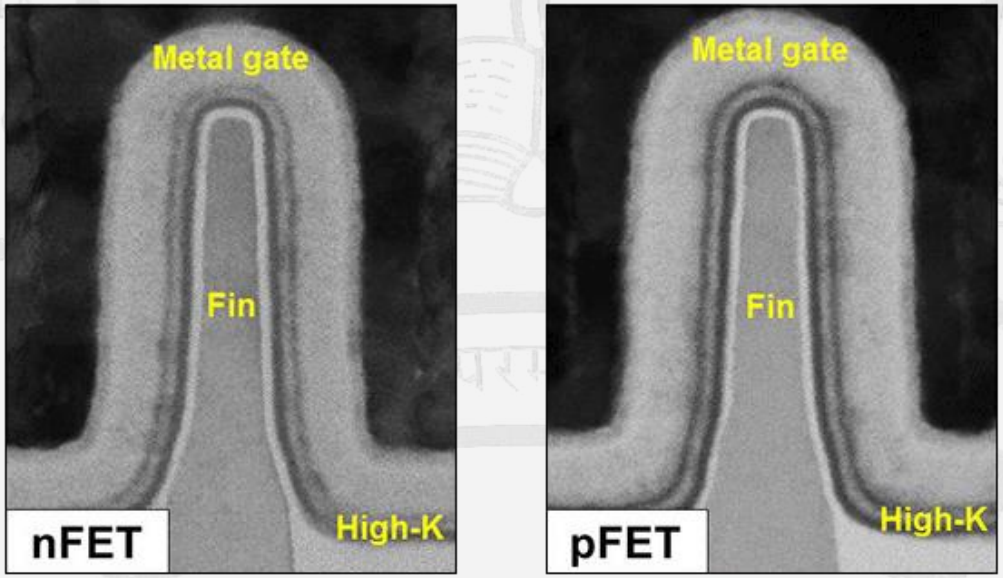
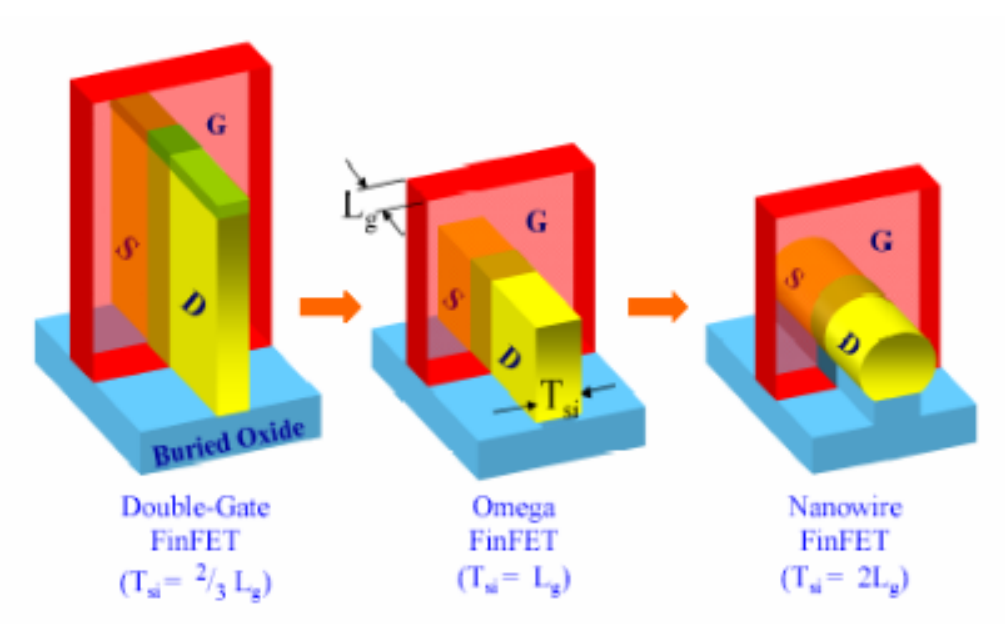


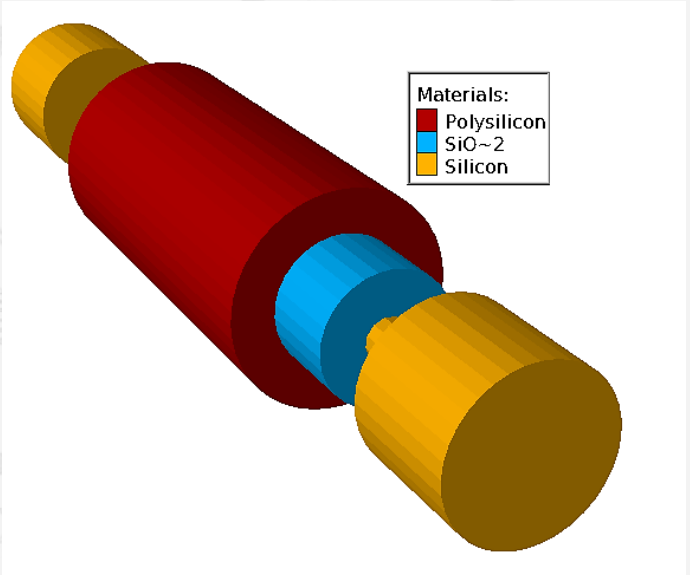
5nm-gate nanowire FinFET - IEEE Conference Publication - IEE...

https://ieeexplore.ieee.org › document

by FL Yang - 2004 - Cited by 363 - Related articles

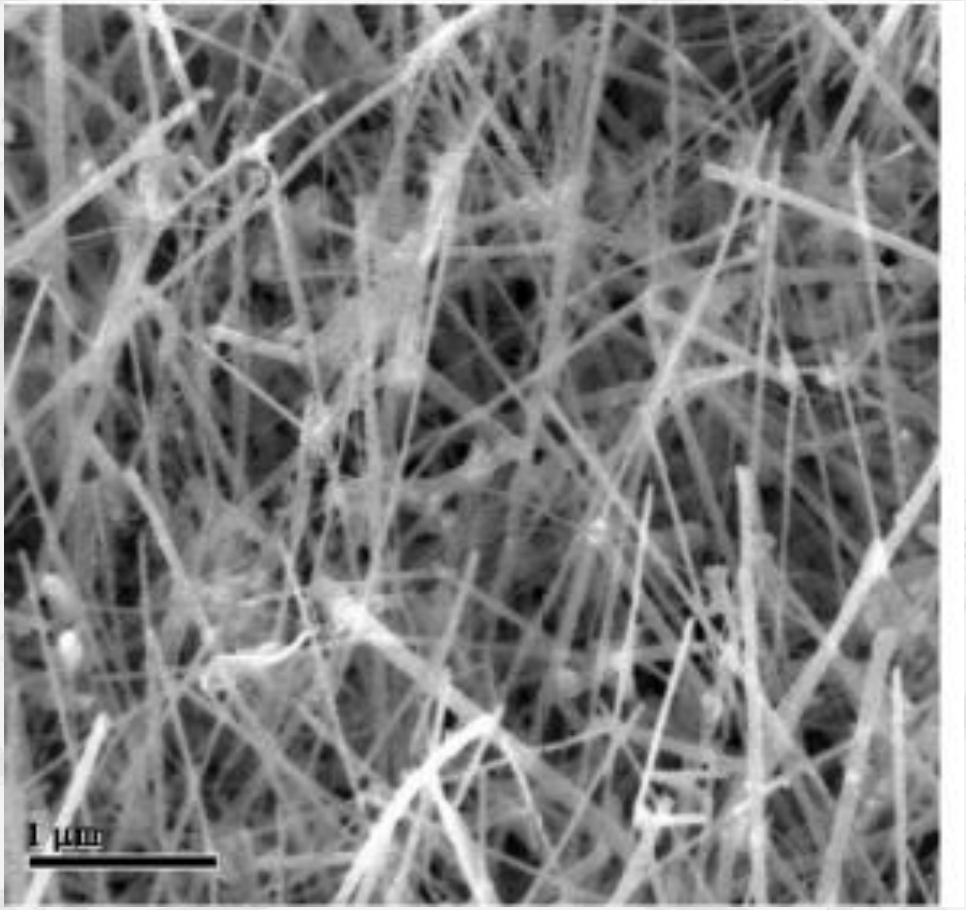
A new **nanowire FinFET** structure is developed for CMOS device scaling into the sub-10 nm regime. Accumulation mode P-FET and inversion mode N-FET with ...



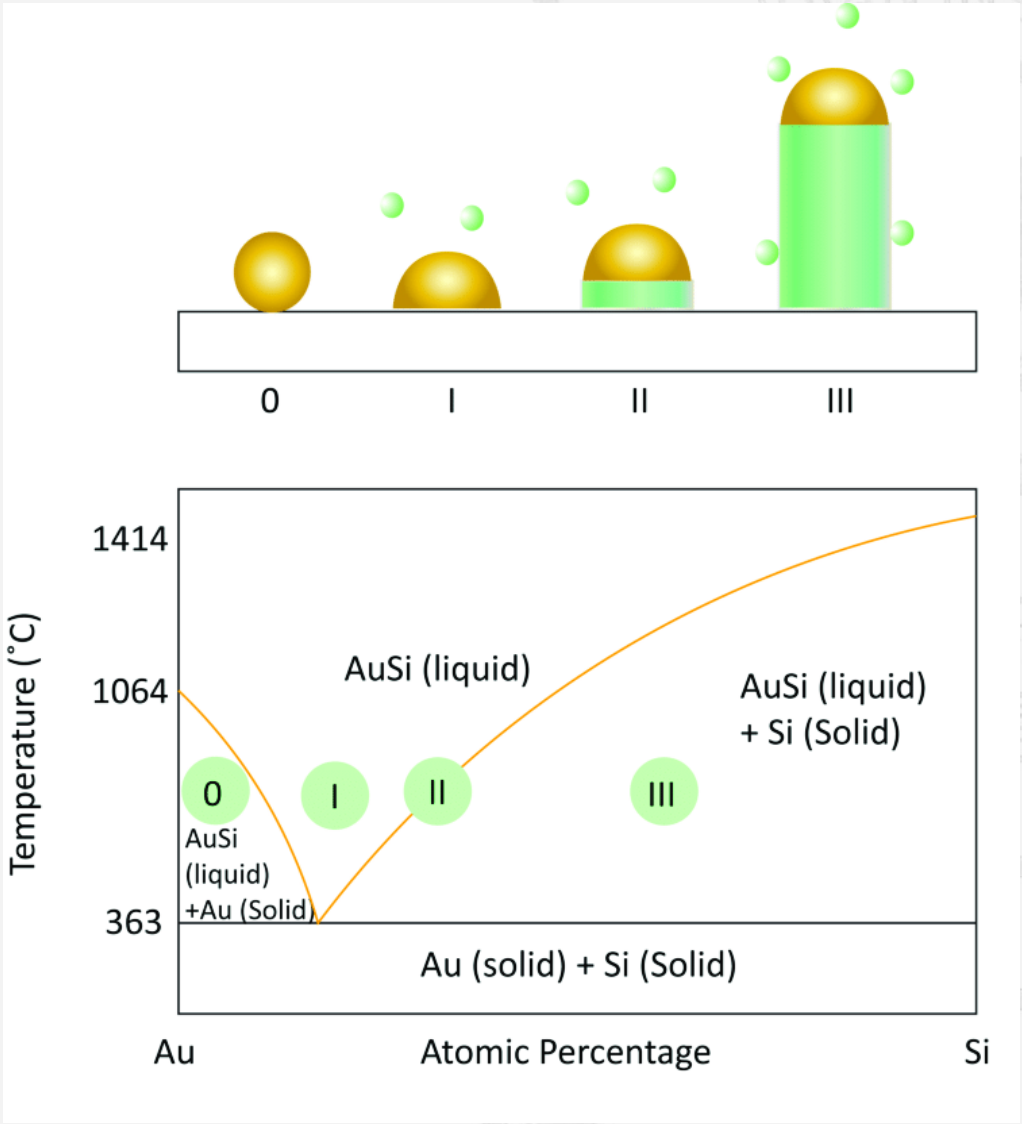


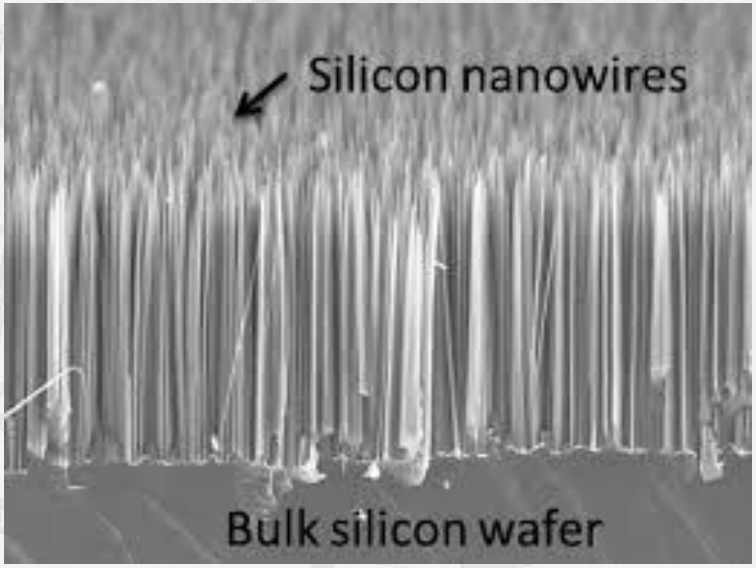
Nanowire FinFET

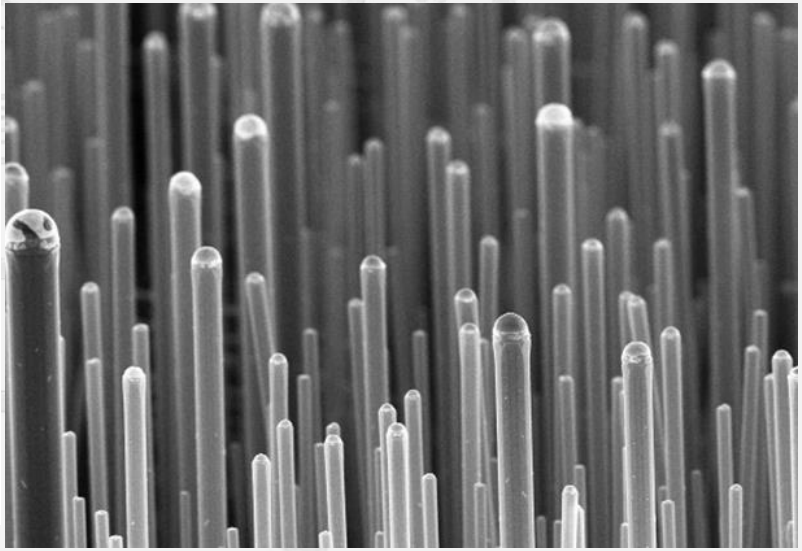
Si Nanowires: Growth



Si Nanowires: VLS Growth







How Intel could prolong Moore's Law with new materials, transistors

Intel could start using new materials and a new transistor structure in upcoming chips