INDIAN INSTITUTE OF TECHNOLOGY, BOMBAY
ELECTRICAL ENGINEERING DEPARTMENT

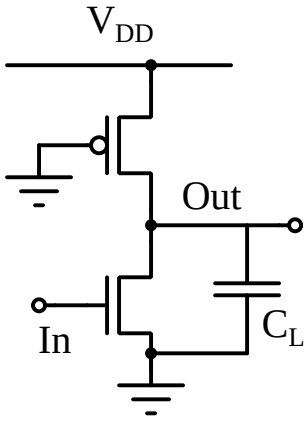
EE 671: VLSI Design

Tuesday	Class Test 1	Time: 1130-1300
22-08-16	Autumn Semester 2017	Marks: 10

All numerical answers should be accurate to 1%.

Q–1

Consider a pseudo-nMOS inverter as shown on the right. Assume that the supply voltage V_{DD} is 3.3V and the load capacitance C_L is 0.1 pF. Parameters for the n and p channel transistors are :



Parameter	N Channel	P Channel
μC_{ox}	$45\mu A/V^2$	$22\mu A/V^2$
V_T	0.6 V	-0.6 V

a) Find the W/L value for the pMOS transistor which will charge the load capacitor from 0V to 3.0V in 5 ns when the nMOS transistor is OFF. The rise time for a pseudo-nMOS inverter is given by

$$\tau_{rise} = \frac{C_L}{\mu_p C_{ox}(W_p/L_p)(V_{DD} - V_{Tp})}\left[\frac{2V_{Tp}}{V_{DD} - V_{Tp}} + \ln\frac{V_{DD} + V_{oH} - 2V_{Tp}}{V_{DD} - V_{oH}}\right]$$

V_{Tp} in the above expression represents the absolute value of the p channel threshold voltage.

Soln.: Using the given expression, we get

$$5 \times 10^{-9} = \frac{10^{-13}}{22 \times 10^{-6}(W_p/L_p)(3.3 - 0.6)}\left[\frac{1.2}{3.3 - 0.6} + \ln\frac{3.3 + 3.0 - 1.2}{3.3 - 3.0}\right]$$

$$\text{So} \quad \frac{W_p}{L_p} = \frac{20}{22 \times 2.7}\left[\frac{1.2}{2.7} + \ln\frac{5.1}{0.3}\right] = 3.3670 \times (0.4444 + 2.8332)$$

Which gives

$$\frac{W_p}{L_p} = 1.1036$$

– 2

b) Find the value of the equivalent resistor which will charge the load capacitor from 0V to 3.0V in the same amount of time (5 ns).

Soln.: The voltage across the capacitor C_L being charged by resistor R from the supply is given by:

$$V_{Out} = V_{DD}\left(1 - e^{-t/RC_L}\right)$$

This gives

$$e^{-t/RC_L} = 1 - \frac{V_{Out}}{V_{DD}} = \frac{V_{DD} - V_{Out}}{V_{DD}} \qquad \text{So} \quad e^{t/RC_L} = \frac{V_{DD}}{V_{DD} - V_{Out}}$$

$$\text{Therefore} \quad t = RC_L \ln \frac{V_{DD}}{V_{DD} - V_{Out}} \qquad \text{and so} \quad RC_L = \frac{t}{\ln \frac{V_{DD}}{V_{DD} - V_{Out}}}$$

If the resistor is so chosen that C_L charges to 3.0V in 5 ns, we get

$$R = \frac{5 \times 10^{-9}}{10^{-13} \times \ln \frac{3.3}{3.3-3.0}} = \frac{50 \times 10^3}{\ln 11} = 20.8516\text{K}\Omega$$

– **1**

c) Find the ratio of (W/L) values for the n channel and p channel transistors such that the static output voltage is = 0.3V when the input voltage is 3.0V. (No memorized expressions should be used. Find the output voltage by equating currents through the two transistors.)

Soln.: When the input voltage is 3.0V and the output is 0.3 V, the nMOS transistor is in linear mode and the pMOS is in saturation. Equating currents, we get

$$K_n \left((3.0 - 0.6) \times 0.3 - \frac{1}{2}(0.3)^2 \right) = \frac{K_p}{2}(3.3 - 0.6)^2$$

This gives

$$\frac{K_n}{K_p} = \frac{2.7^2}{2 \times 2.4 \times 0.3 - 0.09} = 5.4$$

Therefore,

$$\frac{W_n/L_n}{W_p/L_p} = 5.4 \times 22/45 = 2.64$$

– **2**

d) We represent the inverter as a voltage divider, with the p channel transistor replaced by its equivalent resistor computed in part b) above and the n channel transistor by another resistor, such that the static output is = 0.3V. What is the ratio of the equivalent resistors for n channel and p channel transistors?

Soln.: Since R_p and R_n form a voltage divider across V_{DD} to give an output of 0.3 V, we must have

$$0.3 = 3.3\frac{R_n}{R_n + R_p} \qquad \text{Or} \quad 11 = 1 + \frac{R_p}{R_n} \qquad \text{So} \quad \frac{R_p}{R_n} = 10$$

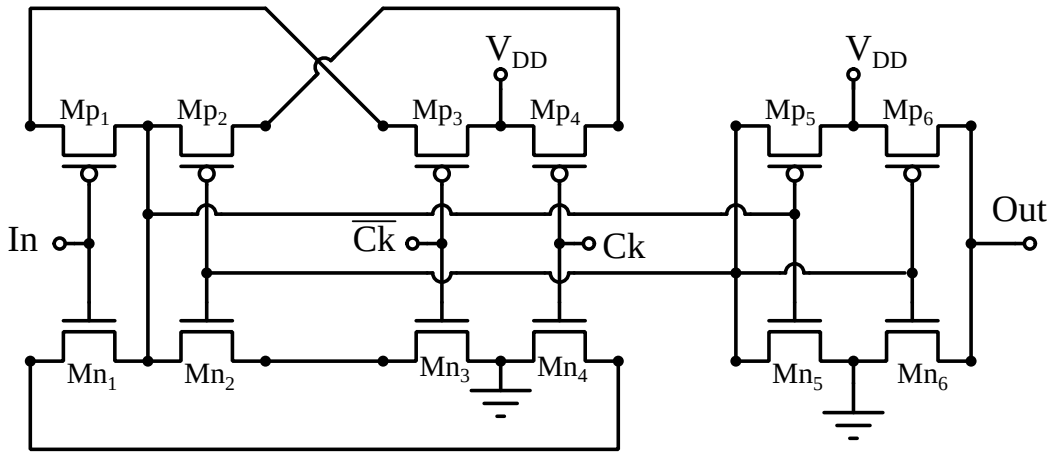
Therefore

$$\frac{R_n}{R_p} = 0.1$$

and accordingly, $R_n = 2.085\text{K}\Omega$. – **1**

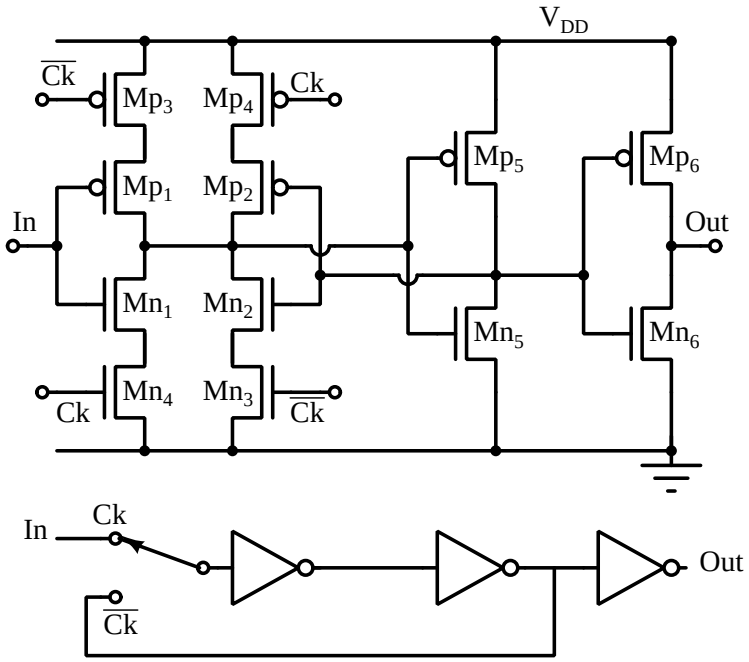
– **[Q–1: 2+1+2+1= 6 marks]**

Q–2 A circuit has been designed in "sea of gates" style, using interconnects as shown below:



a) Re-draw the schematic in conventional style, separating all gates and with V_{DD} on top and ground at the bottom. (Your schematic should clearly identify the labels for all transistors and signals corresponding to the labeling above).

Soln.: The circuit can be re-drawn as follows:



The two tri-stateable inverters are enabled by Ck and $\overline{Ck}$ respectively and have their outputs shorted. This constitutes a multiplexer with inverter. The equivalent logic diagram is also given in the figure above. **– 1**

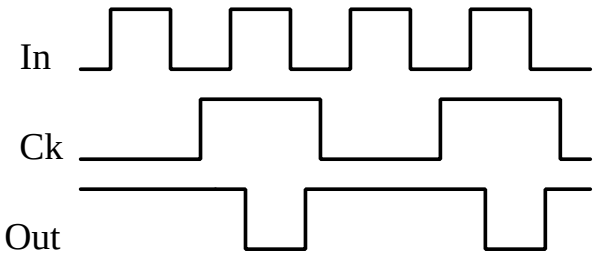
b) What function does this circuit perform? Describe how it works. When Ck is high, the multiplexer chooses In, which appears at the output after three inversions. Thus the output changes as the input changes, providing an inverted version of it.

When Ck is low, the multiplexer forms a latch with the first two inverters. Its output is inverted by the third inverter and appears as the output.

Thus the circuit is a transparent D latch, providing its $\overline{Q}$ as the output. It follows the input (with an inversion) when Ck is high, and is latched when Ck goes low. – **2**

c) For the input and clock waveforms given below, sketch the expected output showing the timing relationship with respect to the clock and the input (In).

Soln.:



The clock has just gone low at the start. Therefore the inverted value of input is latched. When the clock goes high, the latch becomes transparent and the output is the inverted value of input. Again when clock drops low, the output remains latched and ignores further changes in the input. – **1**

– **[Q–2: 1+2+1= 4 marks]**

Paper Ends

Reference

You can use the following MOS model:

$$
\begin{aligned}
I_{DS} &= 0 && \text{when } V_{GS} \le V_T \\
I_{DS} &= K\left[(V_{GS}-V_T)V_{DS} - \tfrac{1}{2}V_{DS}^2\right] && \text{when } V_{GS} > V_T, \quad V_{DS} \le V_{GS}-V_T \\
I_{DS} &= \tfrac{K}{2}\left(V_{GS}-V_T\right)^2 && \text{when } V_{GS} > V_T, \quad V_{DS} \ge V_{GS}-V_T
\end{aligned}
$$