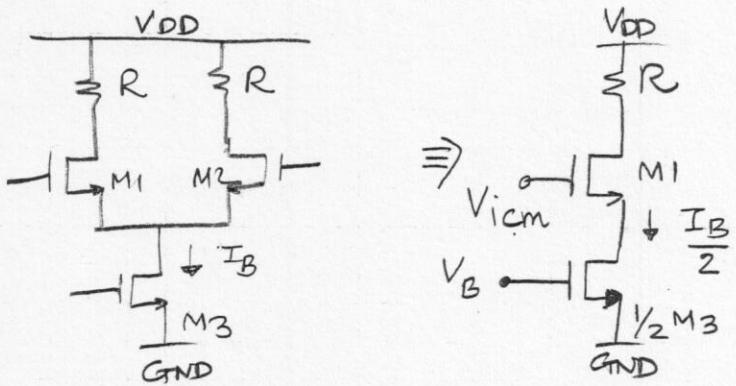
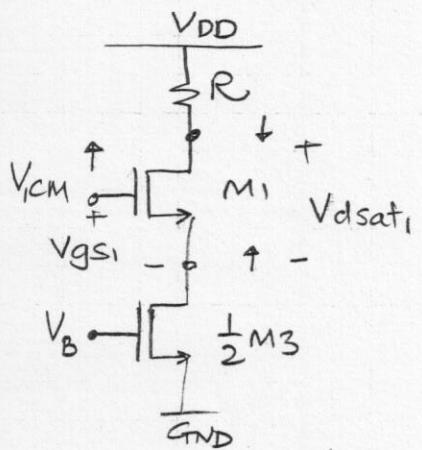


Common-mode Range CMR

- Range of common-mode input voltages for which all devices are in saturation.



Calculating $V_{CM}(max)$



$V_{CM}(max)$ when M_1 enters non-sat.

$$V_{CM}(max) - V_{GS1} = V_{DD} - \frac{I_B R}{2} - V_{DSAT1}$$

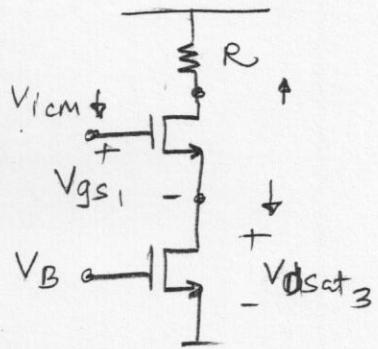
$$\begin{aligned} V_{CM}(max) &= V_{DD} - \frac{I_B R}{2} + V_{GS1} - V_{DSAT1}, \\ &= V_{DD} - \frac{I_B R}{2} + V_T, \end{aligned}$$

Typ $V_{CM}(max) = (V_{DD} - V_{DSAT})$

DC drop across R .

* Can be larger than V_{DD}

calculating $V_{CM}(min)$



$V_{CM}(min)$ - when M_3 enters non-sat.

$$V_{CM}(min) = V_{GS1} + V_{DSAT3}$$

$$= V_T + V_{DSAT1} + V_{DSAT3}$$

$$\approx V_T + 2V_{DSAT}$$

Example

$$V_{DD} = 1.8V \quad V_{TN} = 0.5V \quad V_{TP} = -0.6V$$

$$V_{dsat} \approx 150mV$$

For NMOS diff pair - amplifier

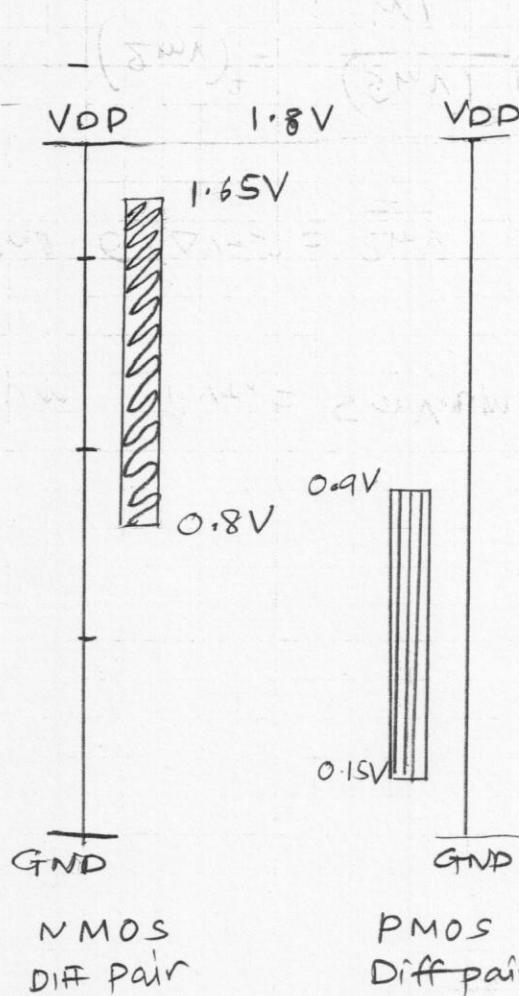
$$V_{icm(max)} = V_{DD} - V_{dsat} \approx 1.8V - 0.15V = 1.65V$$

$$V_{icm(min)} = V_T + 2V_{dsat} = 0.5V + 0.3V = 0.8V$$

For PMOS diff pair - amplifier

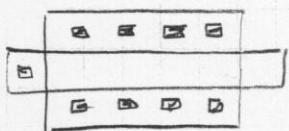
(-ve side) $V_{icm(max)} = 0 + 0.15V = 0.15V$

$$V_{icm(min)} = V_{DD} - (V_T + 2V_{dsat}) = 1.8V - (0.6V + 0.3V) = 0.9V$$

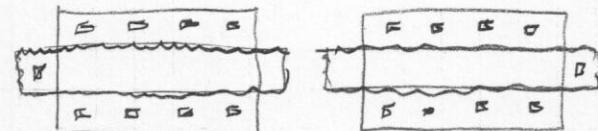
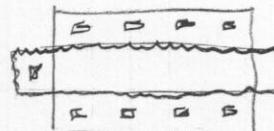
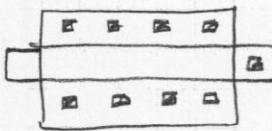


V_{icm} , smart combination of NMOS - PMOS diff pair is used.

INTRODUCTION TO MISMATCHES



Diff pair transistors
(layout tool)



After processing

jagged edges

Random variations. ΔW , ΔL

Intuitively as $W \& L \uparrow$ Relative mismatch $\frac{\Delta W}{W}, \frac{\Delta L}{L} \downarrow$

Mismatches decrease as area of transistor increases

example — Breakup transistor in small pieces
→ averaging effect

For $S \rightarrow$ Can be extended to other device parameters also.

$$\sigma(\Delta V_{TH}) = \frac{A_{V_{TH}}}{\sqrt{WL}}$$

$A_{V_{TH}}$ (mV μ m)

$$\sigma^2(\Delta V_{TH}) = \frac{A_{V_{TH}}^2}{WL}$$

≈ 5 (0.18 μ m process)
[= 30 \rightarrow 2.5 μ m]

$$\sigma\left(\frac{\Delta \beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}}$$

$A_\beta \Rightarrow (\% \mu\text{m})$
 ≈ 1 (0.18 μ m process)
[2.5 \rightarrow 2.5 μ m]

$$\sigma^2\left(\frac{\Delta \beta}{\beta}\right)^2 = \frac{A_\beta}{WL}$$

measured values.
Theory in Pelgrom - JSSC OCT 89

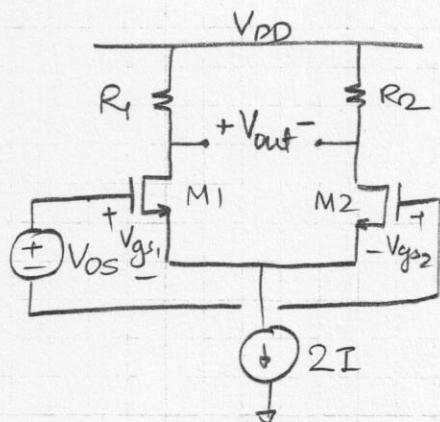
To

good
reference

Lakshmi Kumar - JSSC Dec 86

Kinget - JSSC June 2005

Effect of Mismatches



Input referred offset voltage

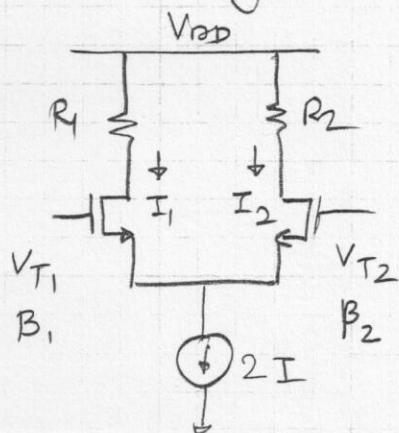
Allstat
Razani
14.2.1

$V_{os} = \text{input DC voltage required}$
 $\text{to make } V_{out} = 0$

→ Systematic offset - Bad design practices → $\left(\frac{W}{L}\right)_1 \neq \left(\frac{W}{L}\right)_2$ or $R_1 \neq R_2$

→ Random offsets - process variation

Calculating Offset voltage



$$I_1 R_1 = I_2 R_2$$

$$V_{os} = V_{gs1} - V_{gs2}$$

$$= V_{T_1} + \sqrt{\frac{I_1}{B_1}} - V_{T_2} - \sqrt{\frac{I_2}{B_2}}$$

Incremental analysis

$$\text{avg quantity } X = \frac{x_1 + x_2}{2} \quad \begin{cases} x_1 = x + \frac{\Delta x}{2} \\ x_2 = x - \frac{\Delta x}{2} \end{cases}$$

apply this to I, R, V_T, β .

$$V_{T_1} = V_T + \frac{\Delta V_T}{2}$$

$$\beta_1 = \beta + \frac{\Delta \beta}{2}$$

$$R_1 = R + \frac{\Delta R}{2}$$

$$V_{T_2} = V_T - \frac{\Delta V_T}{2}$$

$$\beta_2 = \beta - \frac{\Delta \beta}{2}$$

$$R_2 = R - \frac{\Delta R}{2}$$

$$I_1 = I + \frac{\Delta I}{2}$$

$$I_2 = I - \frac{\Delta I}{2}$$

$$\begin{aligned}
 V_{OS} &= V_{T_1} - V_{T_2} + \sqrt{\frac{I_1}{\beta_1}} - \sqrt{\frac{I_2}{\beta_2}} \\
 &= \Delta V_T + \sqrt{\frac{I}{\beta}} \sqrt{\frac{1 + \Delta I/2I}{1 + \Delta \beta/2\beta}} - \sqrt{\frac{I}{\beta}} \sqrt{\frac{1 - \Delta I/2I}{1 - \Delta \beta/2\beta}} \\
 &= \Delta V_T + \sqrt{\frac{I}{\beta}} \left[\left(1 + \frac{\Delta I}{4I} - \frac{\Delta \beta}{4\beta} \right) - \left(1 - \frac{\Delta I}{4I} + \frac{\Delta \beta}{4\beta} \right) \right] \\
 &= \Delta V_T + \sqrt{\frac{I}{\beta}} \left(\frac{\Delta I}{2I} - \frac{\Delta \beta}{2\beta} \right)
 \end{aligned}$$

Random quantities
- Rms sum all \oplus

$$\begin{aligned}
 V_{OS} &\approx \Delta V_T + \sqrt{\frac{I}{\beta}} \left(\frac{\Delta I}{2I} + \frac{\Delta \beta}{2\beta} \right) = \Delta V_T + \frac{2I}{g_m} \left(\frac{\Delta I}{2I} + \frac{\Delta \beta}{\beta} \right) \\
 &= \Delta V_T + (V_{GS} - V_T) \left(\frac{\Delta I}{2I} + \frac{\Delta \beta}{2\beta} \right)
 \end{aligned}$$

$$I_1 R_1 = I_2 R_2 \Rightarrow \left(I + \frac{\Delta I}{2} \right) \left(R + \frac{\Delta R}{2} \right) = \left(I - \frac{\Delta I}{2} \right) \left(R - \frac{\Delta R}{2} \right)$$

$$\cancel{IR} \left(1 + \frac{\Delta I}{2I} \right) \left(1 + \frac{\Delta R}{2R} \right) = \cancel{IR} \left(1 - \frac{\Delta I}{2I} \right) \left(1 - \frac{\Delta R}{2R} \right)$$

$$1 + \frac{\Delta I}{2I} + \frac{\Delta R}{2R} \approx 1 - \frac{\Delta I}{2I} - \frac{\Delta R}{2R} \Rightarrow \frac{\Delta I}{I} = \frac{\Delta R}{R}$$

$$V_{OS} \approx \Delta V_T + \frac{2I}{g_m} \left(\frac{\Delta R}{R} + \frac{\Delta \beta}{\beta} \right) \quad \sigma(V_{OS})^2 = \left(\frac{\Delta I}{I} \right)^2 + \left(\frac{\Delta R}{R} \right)^2 + \left(\frac{\Delta \beta}{\beta} \right)^2$$

$$\text{Taking to the next level} \quad \frac{\Delta \beta}{\beta} = \frac{\Delta K'}{K'} + \frac{\Delta W}{W} + \frac{\Delta L}{L}$$

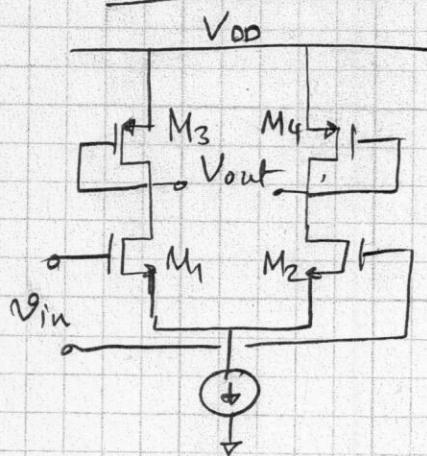
$$\frac{\Delta R}{R} = \frac{\Delta \rho_{\square}}{\rho_{\square}} + \frac{\Delta L}{L} + \frac{\Delta W}{W} \quad w \& L \text{ of Resistor}$$

Sheet R \rightarrow Many terms contribute to offsets.

Back to Diff Pair

MOS Load instead of R load

Diode PMOS load



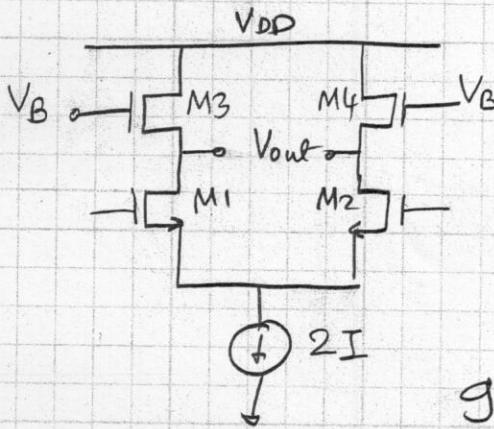
Voltage gain

$$A_V = - \frac{g_{mN}}{g_{mp} + g_{dsN} + g_{dsp}}$$

$$A_V \approx - \frac{g_{mN}}{g_{mp}}$$

$$A_V = - \sqrt{\frac{M_N}{M_P} \frac{(W/L)_N}{(W/L)_P}} \quad (\text{Low value})$$

Current Source PMOS LOAD.



Voltage Gain

$$A_V = - \frac{g_{mN}}{(g_{dsN} + g_{dsp})} \quad \text{High}$$

$$g_{mN} = \frac{2I}{(V_{GS} - V_T)_N} \quad g_{dsN} = \lambda_N I \quad g_{dsp} = \lambda_P I$$

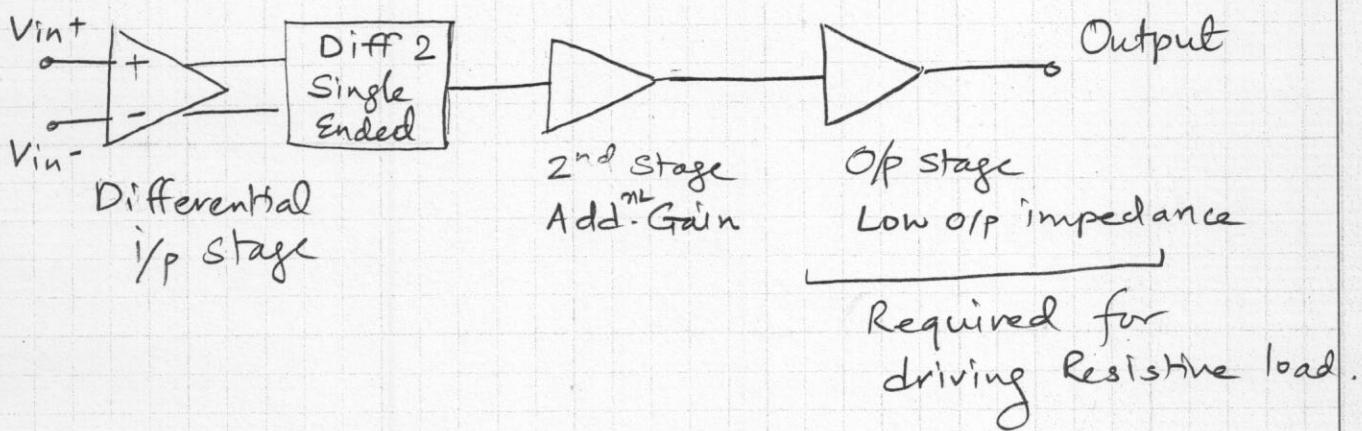
$$A_V = \frac{2}{(V_{GS} - V_T)_N} \cdot \frac{1}{(\lambda_N + \lambda_P)} \leftarrow \begin{array}{l} \text{decided by channel} \\ \text{length} \\ \text{for NMOS} \\ \text{PMOS} \end{array}$$

0.15V

OPERATIONAL AMPLIFIERS

- Basic building block
- High gain differential Amplifier
- A very high V_{out} gain (need not be accurate)
- High input impedance
- Low output impedance

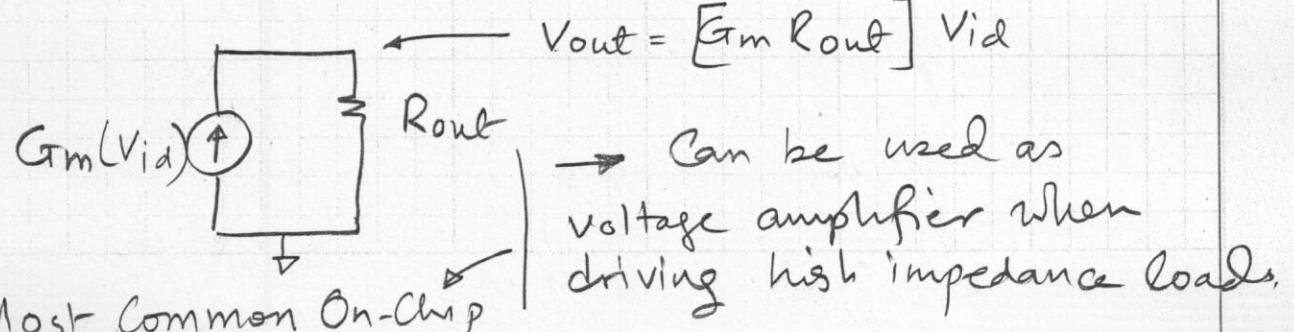
Generic Topology



OPAMP — Low O/P impedance includes final buffer stage

OTA - Operational Transconductance Amplifier

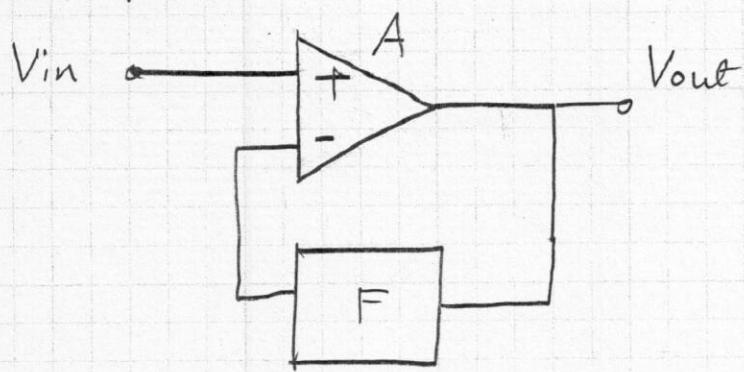
- high O/P impedance
- Current O/P



OPAMP / OTA performance Parameters

- * Voltage Gain — Determines precision of feedback System.

Example:



$$\frac{V_{out}}{V_{in}} = \frac{A}{1 + AF} = \frac{1}{\frac{1}{A} + F} \approx \frac{1}{F}$$

A needs to be larger than spec.

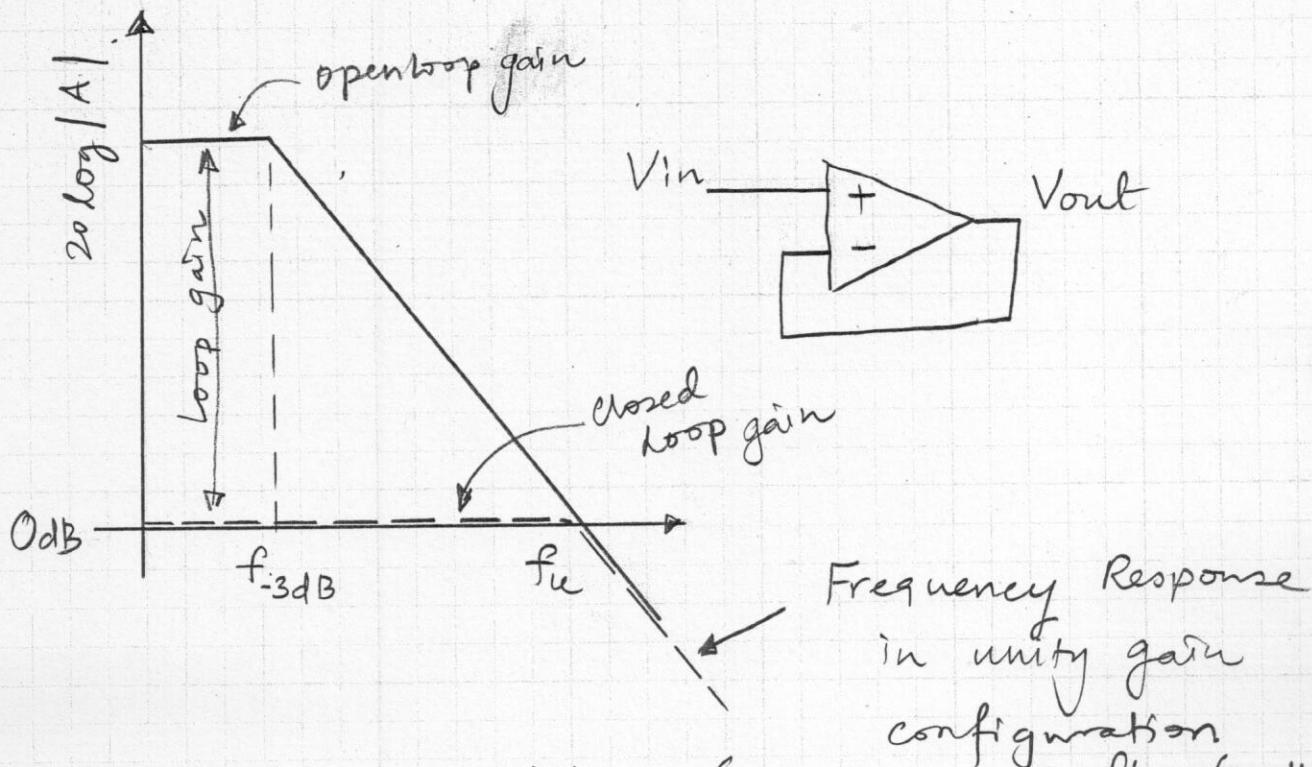
\downarrow
Does not need to be accurate

$\overline{\overline{F}}$
driven by
desired accuracy

F can be decided by ratio of R or
es., — accurate vs. process. Temp. voltage
variations.

* Small Signal BW

Open loop frequency response



- Decides Closed loop freq. response after feedback
- Gain Margin / Phase Margin
(we will be discussing this extensively later)
- Stability important.

- * Output swing - Large - keeping all transistors in saturation (maintaining high ac gain)

* Input Common-Mode range

- i/p CMR for which all transistors are in saturation.
- NMOS - $(V_{DD} - V_{DSAT}) \leftrightarrow V_T + 2V_{DSAT}$
- PMOS - $[V_{DD} - (V_T + 2V_{DSAT})] \leftrightarrow V_{DSAT}$
- To handle Rail2Rail i/p
 - combo of NMOS & PMOS Diff i/p pair

* Input Referred Offset

- Dominated by i/p Diff pair & load
- First Stage high gain
- Avoid systematic mismatches
- Large Device sizes to reduce random mismatches.

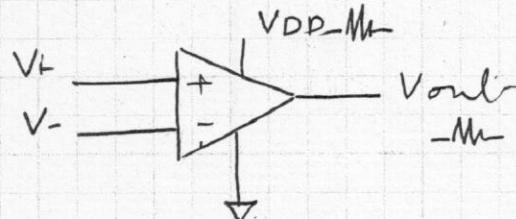
* Noise - Determines minimum signal that can be accurately processed

- Similar treatment like offsets
- We will be studying this extensively.

CMRR - Common-mode rejection ratio
(already discussed)

PSRR - Power Supply Rejection Ratio

- How much of supply noise shows up @ op.



Large Signal Behavior - Slew rate

Slewing - Fastest change in the node voltage. Generally decided by

$$I/C = \frac{dV}{dt}$$

Example

