INDIAN INSTITUTE OF TECHNOLOGY, BOMBAY
ELECTRICAL ENGINEERING DEPARTMENT

Mid Semester Examination

Wednesday	EE 671: VLSI Design	Time: 0830-1030
09-09-15	Autumn Semester 2015	Marks: 25

Q–1 Consider a pseudo NMOS inverter where the ratio of K_n and K_p is β. ($K \equiv \mu C_{ox} W/L$).

a) Assuming perfect saturation for drain currents of transistors, find the input 'High' and output 'Low' logic levels in terms of the supply voltage V_{DD}, turn on voltages V_{Tn} and V_{Tp} and β.
(V_{iH} and V_{oL} are defined by the point on the transfer curve where the gain is -1, with PMOS in saturation and NMOS in linear regime.)

Soln.: Drain currents of PMOS and NMOS must be equal. So

$$\frac{K_p}{2}(V_{DD} - V_{Tp})^2 = K_n\left((V_i - V_{Tn})V_{out} - V_{out}^2/2\right)$$

$$\text{Let } V_1 \equiv V_i - V_{Tn} \quad \text{and } V_2 \equiv V_{DD} - V_{Tp}$$

$$V_2^2 = 2\beta\left(V_1 V_{out} - V_{out}^2/2\right) = 2\beta V_1 V_{out} - \beta V_{out}^2$$

$$\text{So} \quad \beta V_{out}^2 - 2\beta V_1 V_{out} + V_2^2 = 0$$

This leads to

$$V_{out} = \frac{2\beta V_1 \pm \sqrt{4\beta^2 V_1^2 - 4\beta V_2^2}}{2\beta} = V_1 \pm \sqrt{V_1^2 - V_2^2/\beta}$$

$$\text{So} \qquad V_{out} = Vi - V_{Tn} \pm \sqrt{(Vi - V_{Tn})^2 - (V_{DD} - V_{Tp})^2/\beta}$$

We must choose the minus sign, otherwise the NMOS will not be in linear regime and our starting equations will not apply. Thus,

$$V_{out} = Vi - V_{Tn} - \sqrt{(Vi - V_{Tn})^2 - (V_{DD} - V_{Tp})^2/\beta}$$

Taking the derivative with respect V_i and setting it equal to -1 gives

$$-1 = 1 - \frac{2(V_{iH} - V_{Tn})}{2\sqrt{(V_{iH} - V_{Tn})^2 - (V_{DD} - V_{Tp})^2/\beta}}$$

$$2 = \frac{(V_{iH} - V_{Tn})}{\sqrt{(V_{iH} - V_{Tn})^2 - (V_{DD} - V_{Tp})^2/\beta}}$$

Squaring and cross multiplying gives

$$4(V_{iH} - V_{Tn})^2 - \frac{4}{\beta}(V_{DD} - V_{Tp})^2 = (V_{iH} - V_{Tn})^2$$

This gives

$$3(V_{iH} - V_{Tn})^2 = \frac{4}{\beta}(V_{DD} - V_{Tp})^2 \qquad \text{So} \quad V_{iH} - V_{Tn} = \frac{2}{\sqrt{3\beta}}(V_{DD} - V_{Tp})$$

Therefore,

$$V_{iH} = V_{Tn} + \frac{2}{\sqrt{3\beta}}(V_{DD} - V_{Tp})$$

The corresponding output voltage is given by

$$V_{oL} = V_{iH} - V_{Tn} - \sqrt{(V_{iH} - V_{Tn})^2 - (V_{DD} - V_{Tp})^2/\beta}$$

$$= \frac{2}{\sqrt{3\beta}}(V_{DD} - V_{Tp}) - \sqrt{\frac{4}{3\beta}(V_{DD} - V_{Tp})^2 - (V_{DD} - V_{Tp})^2/\beta}$$

So

$$V_{oL} = \frac{2}{\sqrt{3\beta}}(V_{DD} - V_{Tp}) - \frac{1}{\sqrt{3\beta}}(V_{DD} - V_{Tp}) = \frac{V_{DD} - V_{Tp}}{\sqrt{3\beta}}$$

Thus

$$V_{iH} = V_{Tn} + \frac{2}{\sqrt{3\beta}}(V_{DD} - V_{Tp}) \quad \text{and} \quad V_{oL} = \frac{V_{DD} - V_{Tp}}{\sqrt{3\beta}}$$

– **[6]**

b) If $\mu_n = 2.2 \times \mu_p$, find the ratio of W/L values for N and P channel transistors, such that $V_{oL} \leq V_{Tn}$.

Soln.:

$$V_{oL} = \frac{V_{DD} - V_{Tp}}{\sqrt{3\beta}} \leq V_{Tn}$$

So

$$\beta \geq \frac{1}{3}\left(\frac{V_{DD} - V_{Tp}}{V_{Tn}}\right)^2$$

$$\frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} \geq \frac{1}{3}\left(\frac{V_{DD} - V_{Tp}}{V_{Tn}}\right)^2$$

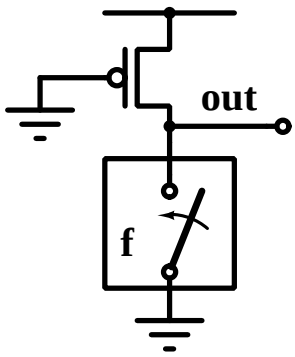
$$\frac{(W/L)_n}{(W/L)_p} \geq \frac{1}{6.6}\left(\frac{V_{DD} - V_{Tp}}{V_{Tn}}\right)^2$$

– **[2]**

– **[Q1: 6 + 2 = 8 marks]**

Q–2 **a)** How is the pseudo NMOS configuration modified to form the dual rail Cascade Voltage Switch Logic, such that static power dissipation is avoided?

Soln.: Consider the pseudo NMOS gate shown below. The switch f represents the entire series-parallel network of NMOS transistors used to generate the logic.



The output of this gate is $\overline{f}$ since the compound switch formed by NMOS transistors is on when f is 'TRUE'. Since the PMOS transistor is always ON, static power is dissipated when f is 'TRUE'. This could be avoided if instead of grounding the PMOS gate, we could drive it with f. Then the PMOS would be OFF whenever f is TRUE. If inputs as well as their complements are available, we can use an additional logic stage and generate f by using the complement of this network and feeding it with complemented inputs. (The complement network replaces series connections by parallel and parallel connections by series).

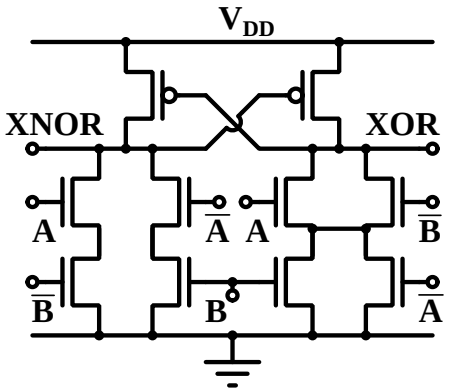
However, what about the static power consumed by this additional stage?

The additional stage will consume static power when its output is LOW, that is when f is 'FALSE'. But we already have $\overline{f}$ available as the output of the original logic stage – so we can use it to turn off the PMOS of the additional logic stage. Now neither stage will consume static power.

This kind of logic is called Cascade Voltage Switch Logic. It needs both true and complemented form of all signals, and generates the output in both true and complemented form. This is called dual rail logic. – **[3]**

b) Draw the transistor level schematic of an XOR/XNOR gate using Cascade Voltage Switch Logic (CVSL).

Soln.: The figure below shows the XOR/XNOR gate in CVSL.

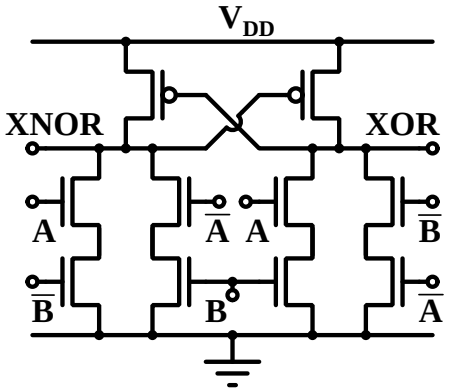


In the circuit on the left, The NMOS transistors have A in series with $\overline{B}$ and this series combination is in parallel with the series combination of $\overline{A}$ and B. The output of the left half is therefore LOW when $A \cdot \overline{B} + \overline{A} \cdot B$ is 'TRUE', thus producing XNOR.

The half circuit on the right changes series to parallel, parallel to series and complements the inputs.

Thus, it has $\overline{A}$ in parallel with B and this parallel combination is in series with the parallel combination of A and $\overline{B}$. This produces the XOR output.

The network on the right can be simplified. Consider the lower shorting line used for paralleling NMOS transistors. No current will ever flow through this wire because it provides a path between an NMOS driven by A to another driven by $\overline{A}$. Similarly, it provides a path between an NMOS driven by $\overline{B}$ to another driven by B. Since no current will flow through this, we may as well remove it. This results in the alternative circuit shown below.



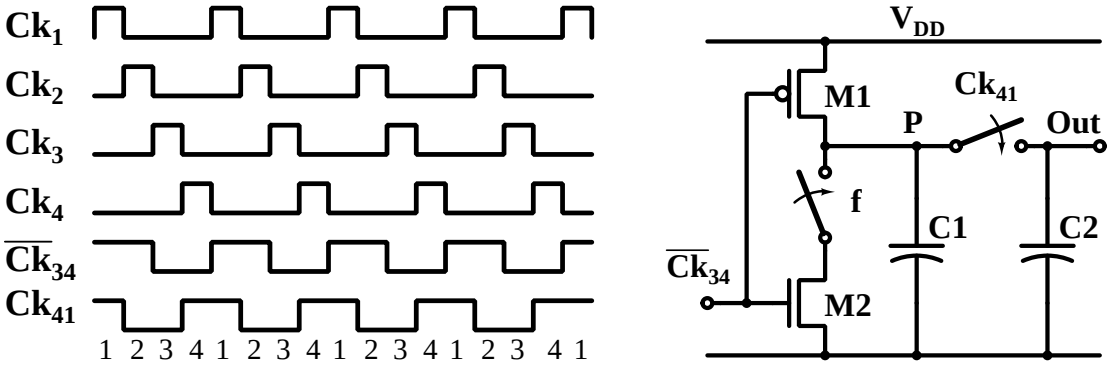
This alternative circuit is not surprising. The right half circuit is seen to implement the series parallel combination corresponding to $A \cdot B + \overline{A} \cdot \overline{B}$, which is just the expression for XNOR. Thus the output of this half circuit is LOW when XNOR is true – that is, the output is XOR, which is just what we wanted.

– **[2]**

– **[Q2: 3 + 2 = 5 marks]**

Q–3 **a)** Show the timing diagram for clocks, internal nodes and output of a 4 phase CMOS dynamic logic gate of type 1. The logic function performed by series/parallel connection of NMOS transistors need not be shown and can be represented by a black box. You should clearly mark the clock phases during which the output is valid.

Soln.: The figure below shows a dynamic 4phase logic gate of type 1.



The signal $\overline{Ck_{34}}$ is LOW during phases 3 and 4 of the clock, while Ck_{41} is HIGH during phases 4 and 1 of the clock..

- During phase 3, the PMOS transistor M1 is ON, the NMOS transistor M2 is OFF and the switch controlled by CK_{41} is OFF. In this phase, capacitor C1 is pre-charged to V_{DD}, while C2 holds its previous value.
- During phase 4, the PMOS transistor M1 remains ON, the NMOS transistor M2 remains OFF and the switch controlled by CK_{41} turns ON. In this phase, capacitors C1 and C2 are pre-charged to V_{DD}.
- During phase 1, the PMOS transistor M1 turns OFF, the NMOS transistor M2 turns ON, while the switch controlled by CK_{41} remains ON. During this phase, capacitors C1 and C2 are conditionally discharged depending on the status of the switch f. Thus the output evaluates $\overline{f}$ during this phase.
- During phase 2, the PMOS transistor M1 remains OFF, the NMOS transistor M2 remains ON, and the switch controlled by CK_{41} turns OFF. The output is valid during this phase, as well as in the next phase.

– **[2]**

b) A circuit module receives external signals ATN (attention) and four address lines A3-A0. It is supposed to respond to incoming data on a data bus D7-D0 if ATN is '1', irrespective of address line values. If ATN is '0', it should respond to the data bits only if the bit pattern on A3-A0 is 0110 (which is its address).

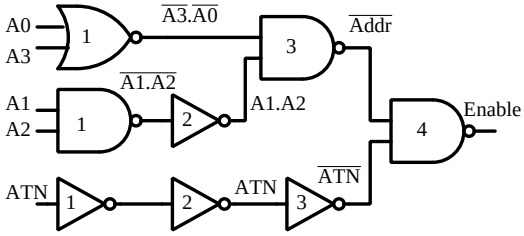
We want to generate an 'Enable' signal which will be 1 only when the circuit module needs to respond to incoming data, using 4 phase CMOS Dynamic logic. Signals ATN and A3-A0 are valid only in phase 1 of the clock. Due to a restriction on series connected transistors, only NAND and NOR gates with a maximum of 3 inputs and inverters can be used.

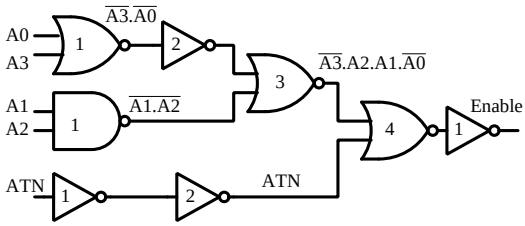
Show a gate level implementation, clearly marking the type of all gates. Specify the clock phases during which the 'Enable' signal is valid. The design should minimize complexity and delay.

Soln.:

$$\text{Enable} = \text{ATN} + \overline{\text{ATN}} \cdot \overline{\text{A3}} \cdot \text{A2} \cdot \text{A1} \cdot \overline{\text{A0}} = \text{ATN} + \overline{\text{A3}} \cdot \text{A2} \cdot \text{A1} \cdot \overline{\text{A0}}$$

This can be generated by either of the circuit shown below:





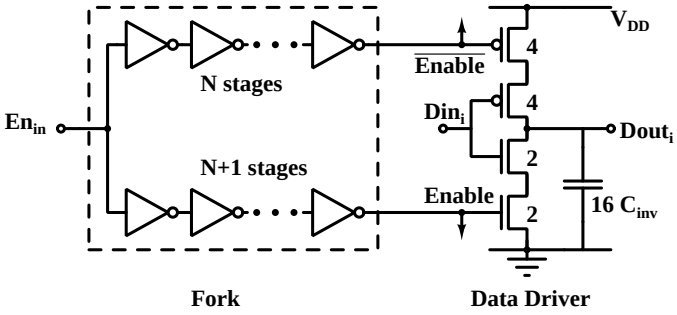
Both circuits use 8 gates. The output of the circuit on the left is available earlier and is valid in phases 1 and 2 of the next clock.

The output of the circuit on the right is valid in phases 2 and 3 of the next clock. If complemented output is acceptable, its output will also be available in phases 1 and 2 of the next clock and it will need one less inverter. – [3]

– **[Q3: 2 + 3 = 5 marks]**

Q–4 The figure below shows a tri-stateable driver which needs Enable and $\overline{\text{Enable}}$ signals generated by a fork. (A fork is a parallel path of N and N+1 inverters with nearly matched total delays).

Each driver sees a load of 16 minimum sized inverters. 8 such drivers are to be driven by a single fork. The input En_{in} can drive a load of 2 minimum sized inverters. Sizes shown for transistors in the data driver are for a minimum sized driver; all of these can be scaled by any factor depending on requirements.



Assume that the mobility correction factor for PMOS transistor widths is 2 and the parasitic delay of inverters (p_{inv}) is 1.

a) Find the optimum stage effort for the whole chain by solving the equation

$$p_{inv} + \rho(1 - \ln \rho) = 0 \qquad \text{iteratively.}$$

Find the number of stages in the logic chain corresponding to this value of ρ. (This number should be adjusted to be an integer just less than the calculated value).

Soln.:

$$p_{inv} + \rho(1 - \ln \rho) = 0 \qquad \text{so} \;\; \ln \rho = 1 + \frac{p_{inv}}{\rho}$$

$$\text{Therefore} \qquad \rho = \exp\left(1 + \frac{p_{inv}}{\rho}\right) = \exp\left(1 + \frac{1}{\rho}\right)$$

Starting with a trial value of $\rho = 3$, we get successive values of ρ as $3.7937, 3.5381, 3.6061, 3.5869, 3.5923, 3.5908, 3.5912, 3.5911, 3.5911, \cdots$

The logical effort of the data driver is $4/3 = 1.33$
Therefore $G = 1 \times 1 \times \cdots \times 1.33 = 1.33$
$B = 2 \times 1 \times \cdots \times 8 \times 1 = 16$ and $H = 16/2 = 8$.
Therefore $F = GBH = 4/3 \times 16 \times 8 = 170.67$.
Optimum number of stages is therefore $\ln(170.67)/\ln(3.5911) = 4.02$
Therefore the branch with N inverters can have 4 stages, while the branch with N+1 inverters will have 5 stages. Since one of the stages is the data driver itself, the fork will have 3 and 4 stages in the two branches. – [4]

b) Distribute the total effort equally over the logic chain taking the N inverter branch in the fork. Find the transistor widths for all transistors. (The branch with N+1 inverters is not to be designed in this question).

Soln.: Equally distributed effort $= 170.67^{1/4} = 3.6144$.
The scale factor of a stage is given by C_{in}.

$$\text{Since} \quad f = gh = g\frac{C_{out}}{C_{in}}, \qquad C_{in} = g\frac{C_{out}}{f}$$

In our case the value of f is 3.6144 for every stage. The data driver stage should have $C_{in} = 4/3 \times 16/3.6144 = 5.9022$.
Since there are 8 such drivers loading the Enable signal, C_{out} seen by the last inverter is $8 \times 5.9023 = 47.22$
Its C_{in} is therefore $1 \times 47.22/3.6144 = 13.064$. C_{in} of the middle inverter is $1 \times 13.064/3.6144 = 3.6144$,
and C_{in} of the first inverter is $1 \times 3.6144/3.6144 = 1$ as expected.
So the scaling of the 3 inverters is 1, 3.61 and 13.06 respectively. The delay of the 3 inverters is 4.61τ each, leading to a total delay of 12.83τ in the inverter chain. Geometries of transistors are given as:

Stage	Scale Factor	Width Of	
		NMOS	PMOS
Inverter 1	1	1	2
Inverter 2	3.61	3.61	7.22
Inverter 3	13.06	13.06	26.13
Data Driver	5.90	8.85	17.7

In the case of the data driver, only the PMOS is driven. Therefore, just the PMOS presents a capacitive load equivalent to 5.9022 inverters. Therefore, its width should be $3 \times 5.9 = 17.7$ times the minimum transistor size. The NMOS transistors will be half this size and will be driven by the N+1 stage inverter chain. The data driver has two NMOS transistors with $W/L = 8.85$ in series, with corresponding mobility corrected W/L for PMOS transistors. It therefore has the drive strength of $8.85/2 = 4.425$ minimum sized inverters. Since each inverter optimally drives other inverters which are 3.6144 times its own size, this stage can drive $4.425 \times 3.6144 = 16$ inverters, as required. – [3]

– **[Q4: 4 + 3 = 7 marks]**

Paper Ends