EE 618 (ZELE)

CMOS ANALOG IC DESIGN

End Semester Exam

20th NOV 2018 9:00 AM – 12:00 PM

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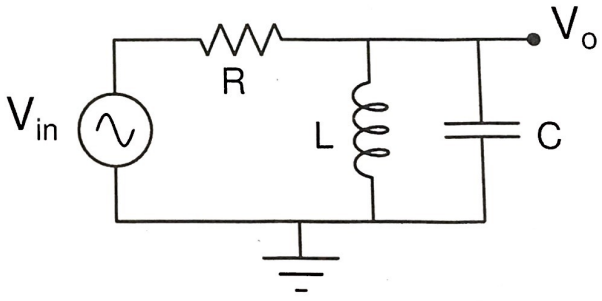
State your assumptions clearly if any.

1. (a) Draw the schematic diagram for Operational Trans-conductance Amplifier that you designed in the project. Clearly label transistors, inputs, outputs and bias voltages. Schematic for biasing circuits is not necessary. (4)
   (b) Derive an expression for gain of your OTA. State your assumptions. (2)

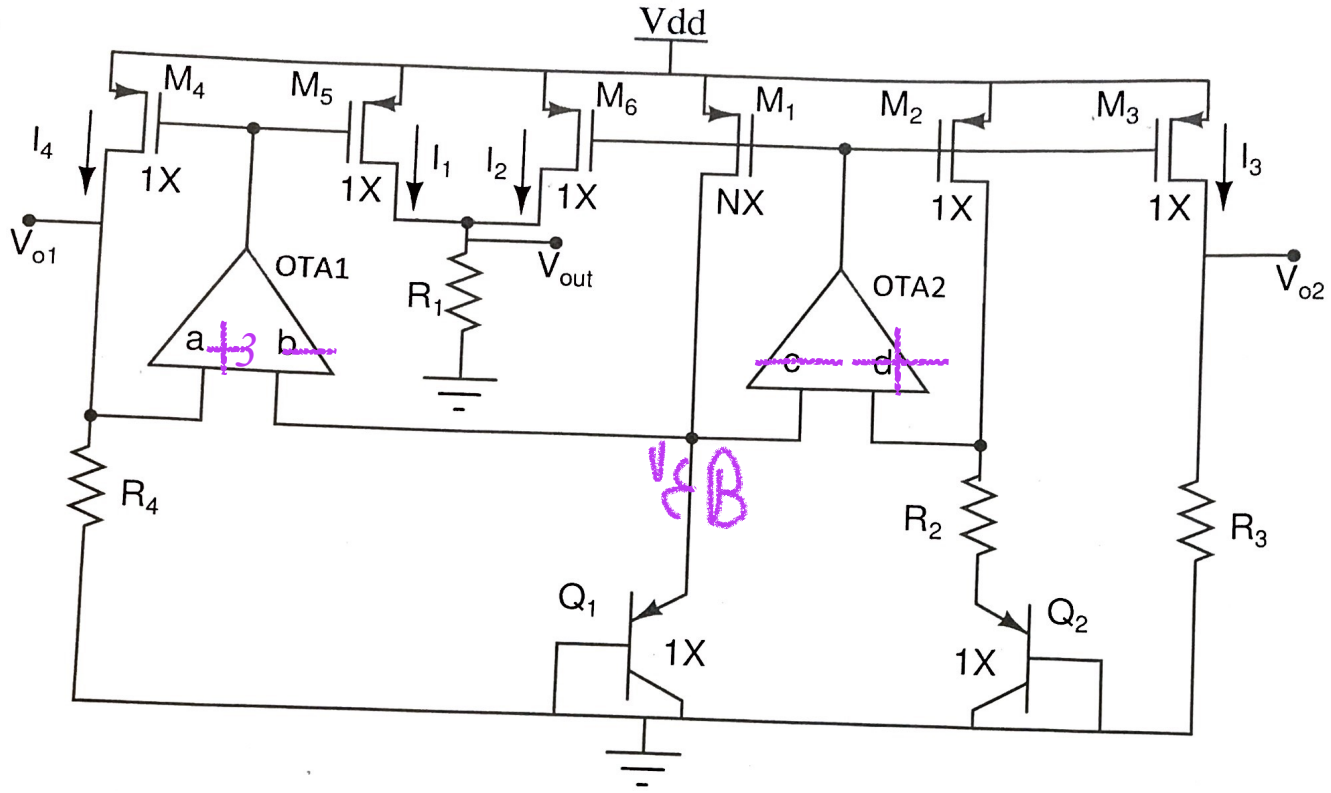
2. Consider the RLC filter as shown in Figure.
   L = 159 nH; C = 159 nF, R = 1 Ω



   (a) Write the transfer function Vo/Vin. Identify the type of the filter. (Frequency Response). (1)

   (b) Comparing with standard transfer function polynomial ($s^2+\omega_0.s/Q+\omega_0^2$), calculate ω_0 and Q values. (1)
   (c) Draw signal flow-graph for the RLC circuit from Figure 1. (3)
   (d) Using parasitic insensitive Switched-Capacitor (SC) integrator construct SC filter schematic using signal flow graph from (c). (4)
   (e) Annotate your clocking scheme for filter in (d). (1)
   (f) Choose clock frequency. Justify why? (1)
   (g) For all SC integrators C_u = 0.2pF (input capacitor). Figure out values of C_i (feedback capacitors) of all integrators. (2)

3. For the circuit shown in figure, note the Bipolar transistors and MOSFET scaling ratios carefully.



Assume $dV_{EB}/dT = -\alpha$ V/K.

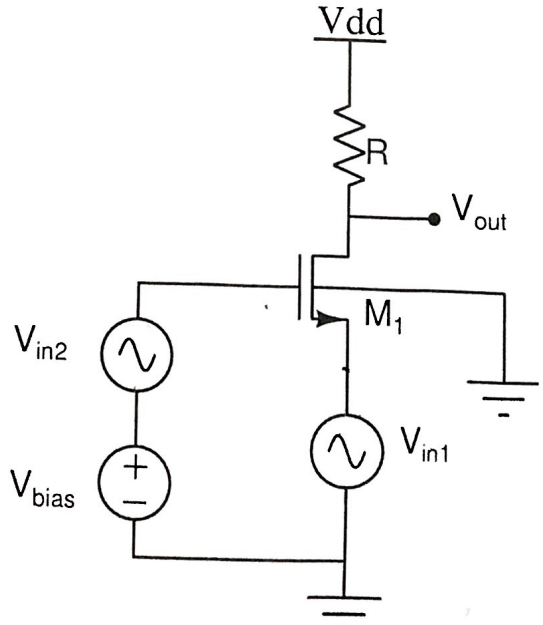
(a) Indicate the opamp input polarity for OTA1 and OTA2 using annotations a,b,c,d. Explain your reasoning. (3)

(b) Write expressions for V_{o1} and V_{o2}. (3)

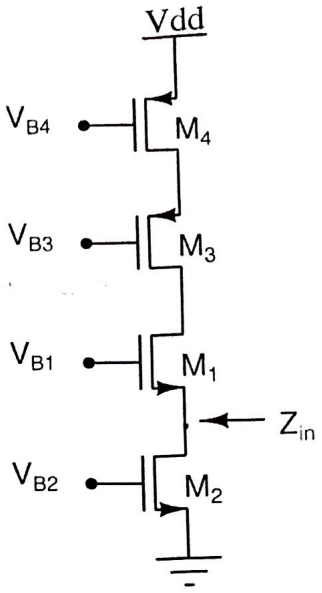
(c) Write an expression for V_{out}. Derive the condition under which V_{out} will be independent of process, temperature and supply voltage. (3)

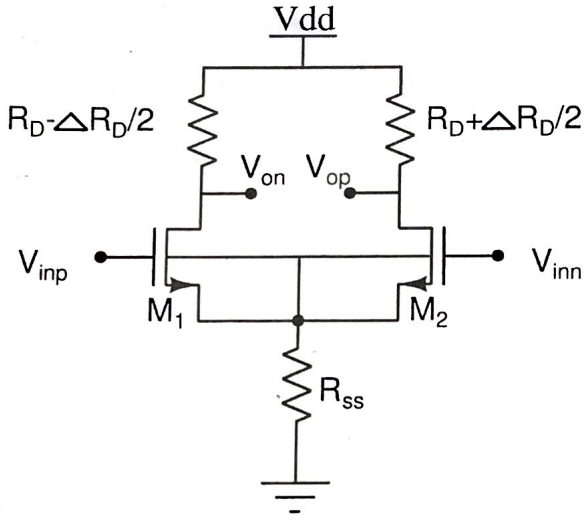
(d) During power-up, this circuit has stable operating point with all the currents equal to zero. Draw a startup circuit which will make sure that the circuit wakes up in the proper operating mode. Only redraw the relevant part of the circuit. No need to draw entire schematic. (2)

4. For the circuit shown in figure, derive an expression for small signal gain V_{out}/V_{in}. for each ac input. (3)



5. For the circuit shown in figure, derive an expression for input impedance Z_{in}. Assume all transistors have same g_m and r_{out}. Each transistor is biased with bias voltage at the gate terminal keeping all of them in saturation region. Ignore Body effect. (3)





6. Derive an expression for A_{CM-DM} (Common-Mode to Differential-Mode Gain). Ignore channel length modulation. (4)

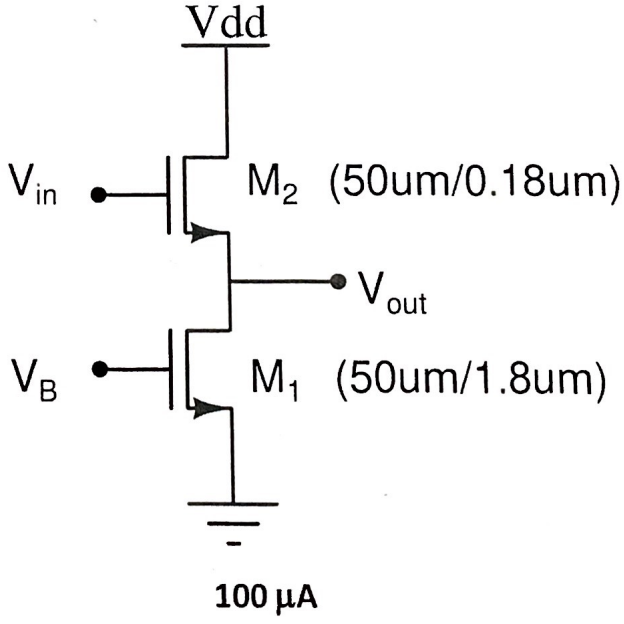
7. Calculate the value of input-referred noise voltage in nV/√Hz. I_{bias} = 100 μA. Ignore Body Effect. (5)

$KT = 4.14 \times 10^{-21}$ J

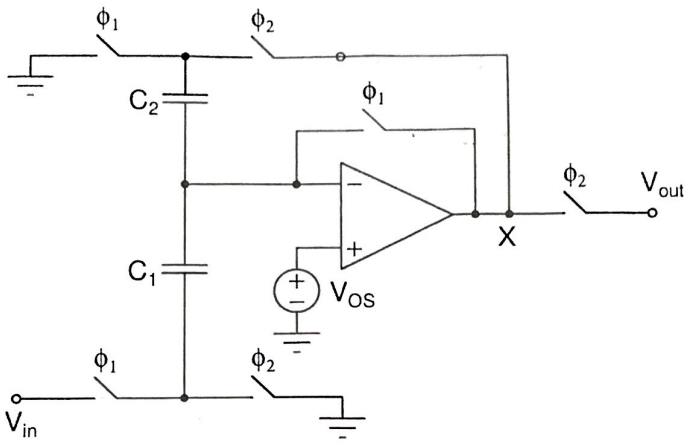
$K_n = \mu_n C_{ox} = 263\ \mu A/V^2$;

$\lambda_n = 0.5\ V^{-1}$ (for L =0.18 μm);

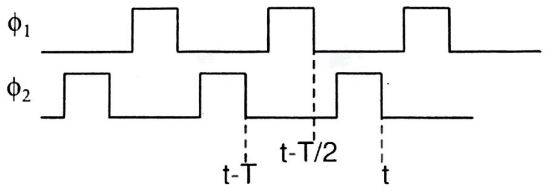
$V_{Tn} = 0.5$ V; $\gamma_n = 1$.



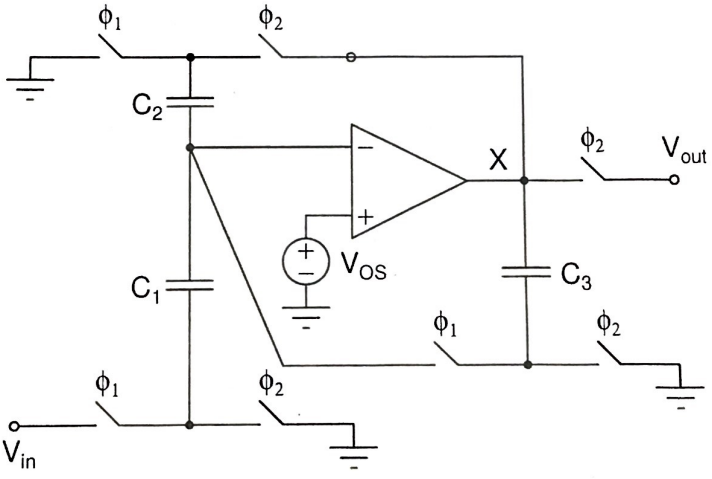
8. (a) For the switched-capacitor circuit on right (top), use charge conservation principle to figure out V_{out}/V_{in} transfer function in Z- domain. V_{os} is the input-referred offset voltage (constant) of the OPAMP. (2)



(b) Assuming low frequency sine wave input, draw time-domain waveform at **node X**. (2)



(c) For the switched-capacitor circuit on right, use charge conservation principle to figure out V_{out}/V_{in} transfer function in Z- domain. V_{os} is the input-referred offset voltage (constant) of the OPAMP. (4)



(d) Assuming low frequency sine wave input, draw time-domain waveform at **node X** qualitatively. You can assume C3 >> C1 or C2 so that from ϕ_2 to ϕ_1, charge across C3 doesn't change. (2)

(e) Compare the opamp output waveforms in (b) and (d). Comment on the performance requirement for the opamp design for the two implementations. (2)

9. As a layout designer, you are required to match the input differential pair NMOS transistors sized 50μm/0.2μm each. Assuming maximum finger width < 5 μm, how would you floorplan your layout of the differential pair for common-centroid matching? Draw the picture with size of each transistor (W,L,No. of fingers). No routing necessary. (3)