EE669: VLSI Technology

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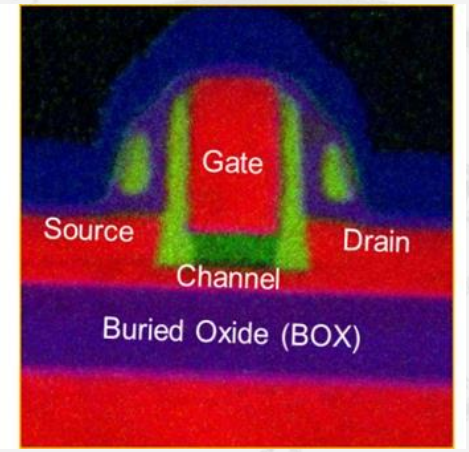
Office hour: Friday 10:00 – 11.00 AM, EE Annex, Room: 104

Silicon on insulator (SOI) technology



SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic devices

Extending Moore's Law" (or "More on Moore", "MM")

Fully Depleted Silicon On Insulator, or FD-SOI: A planar process technology that relies on two primary innovations.

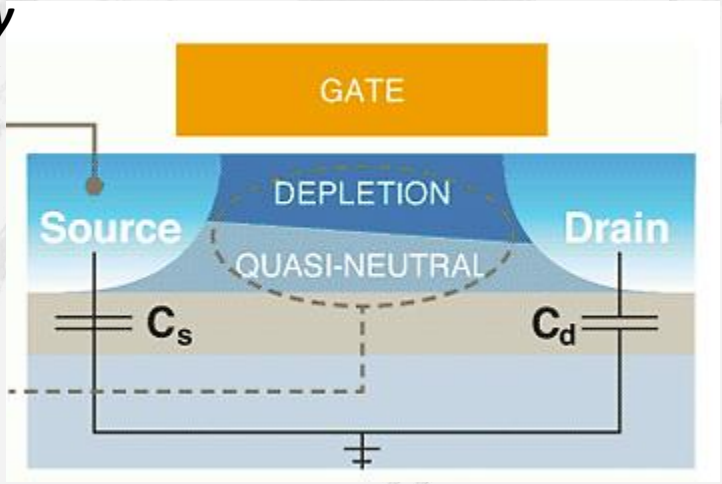
(1) An ultra-thin layer of insulator, called the buried oxide

(2) A very thin silicon film implements the transistor channel.

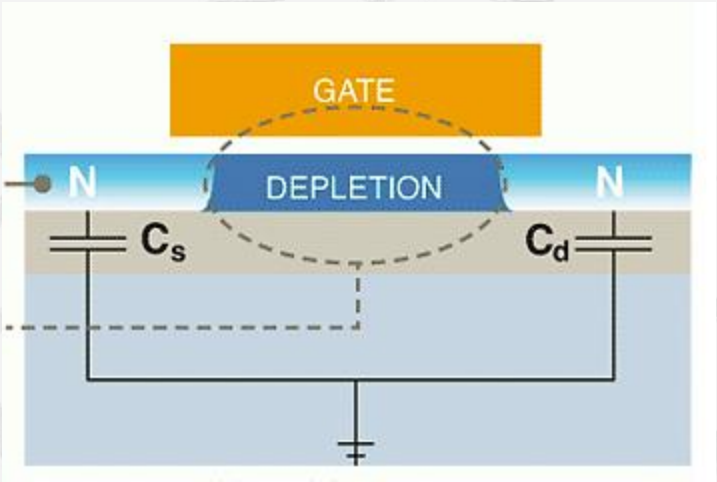
Source: ST Microelectronics

Fully Depleted(FD) vs. Partially Depleted (PD) SOI

- *Top Si layer is typically between 50-100nm thick depending on design*
- *Si under the channel is partially depleted. Avalanche ionization at the drain can lead to charge accumulating in the quasi-neutral region (floating body effect*



- *Top Si layer is typically between 5-20nm thick- typically 1/4th of gate length*
- *Si under the gate is fully depleted. There is no floating body effect*



- **Channel thickness decides the SOI type**

PD:
Thicker top layer, "floating body".

FD:
Thinner top layer, Channel is fully depleted of charges.

Benefits of SOI technology relative to conventional silicon

- *Lower parasitic capacitance* due to isolation from the bulk silicon, which improves power consumption
- *Resistance to latchup* due to complete isolation of the n- and p-well structures
- Reduced temperature dependency due to no doping
- Better yield due to high density, better wafer utilization
- Reduced antenna issues
- No body or well taps are needed
- Lower leakage currents due to isolation thus higher power efficiency
- Inherently radiation hardened (resistant to soft errors), reducing the need for redundancy

Radiation hardening is process of making electronic components and circuits resistant to damage or malfunction caused by high levels of ionizing radiation (particle radiation and high-energy electromagnetic radiation),

- From a manufacturing perspective, SOI substrates are compatible with most conventional fabrication processes.
- An SOI-based process may be implemented without special equipment or significant retooling of an existing factory
- Novel metrology requirements to account for the buried oxide layer
- Concerns about differential stress in the topmost silicon layer.
- The primary barrier to SOI implementation is the drastic increase in substrate cost, which contributes an estimated 10–15% increase to total manufacturing costs.

Different Manufacturing Methods of SOI

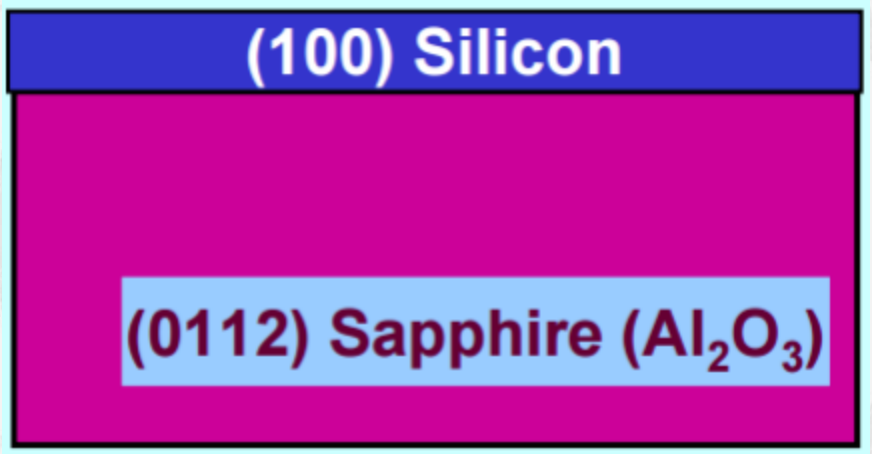
- **Seed Method** – the topmost Si layer is grown directly on the insulator.

- **SIMOX - Separation by IMplantation of Oxygen** – uses an oxygen ion beam implantation process followed by high temperature annealing to create a buried SiO_2 layer.

- **Wafer bonding** - the insulating layer is formed by directly bonding oxidized silicon with a second substrate.

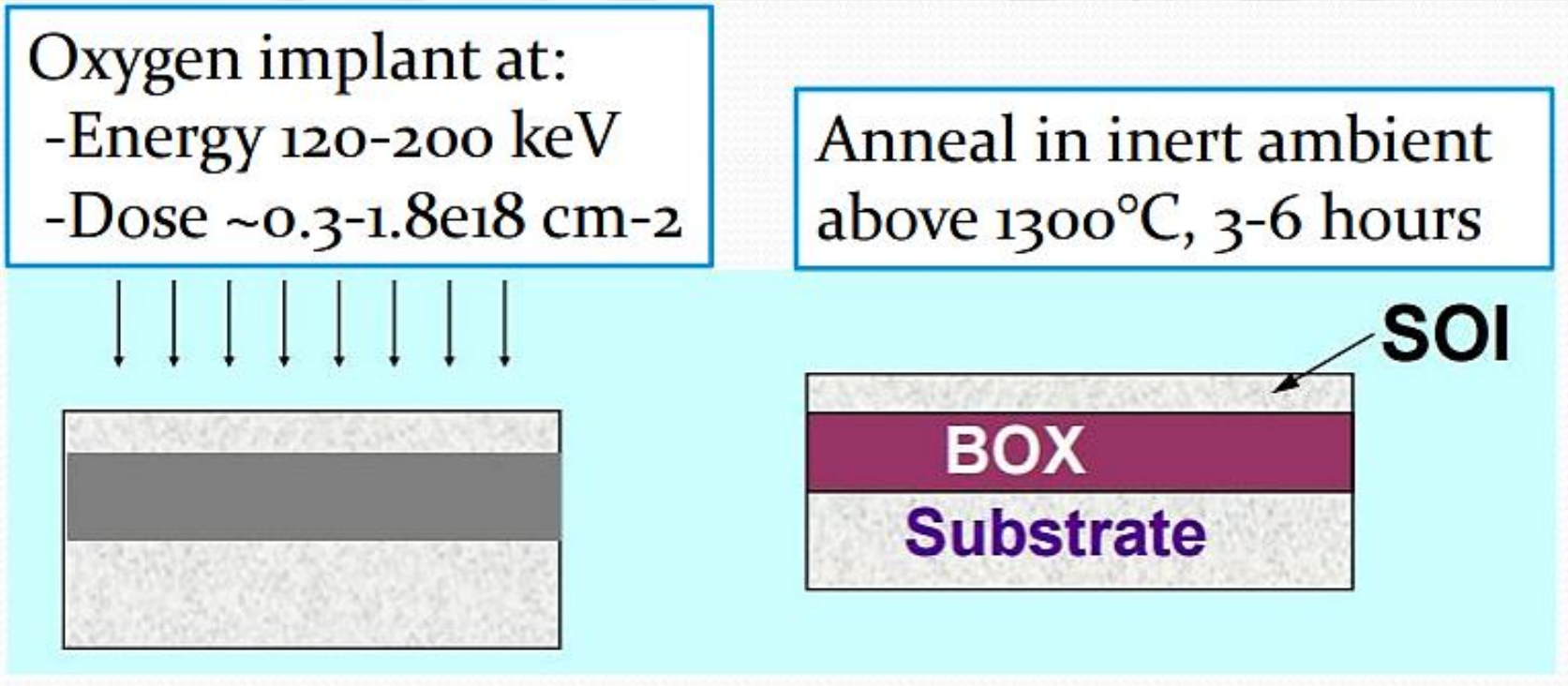
- ***Smart Cut Method***
- ***ELTRAN***
- ***Nano Cleave***

Seed Method - Silicon-On-Sapphire (SOS)



Solid Phase Epitaxy (SPE)

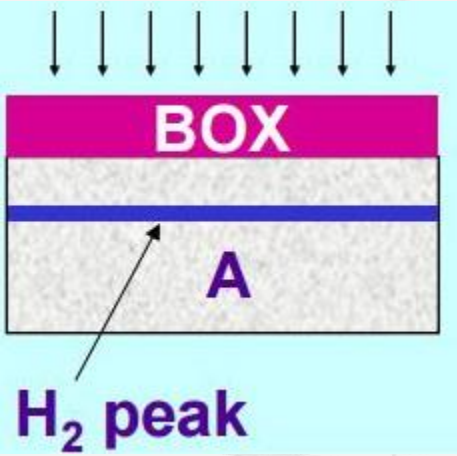
Separation by Implanted Oxygen (SIMOX)



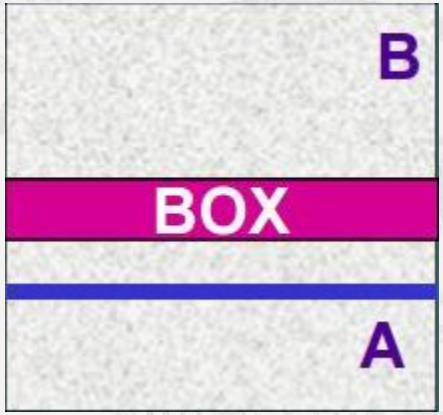
Typical BOX thickness: 100, 200, 400 nm

SOI film thickness varies from ~50 - 240 nm

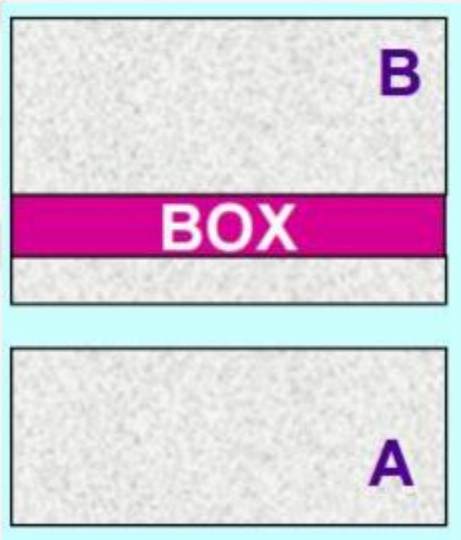
Wafer Bonding – Smart Cut Method



Step 1:
Hydrogen implantation through thermal oxide dose ~1-5e^{16} cm-2



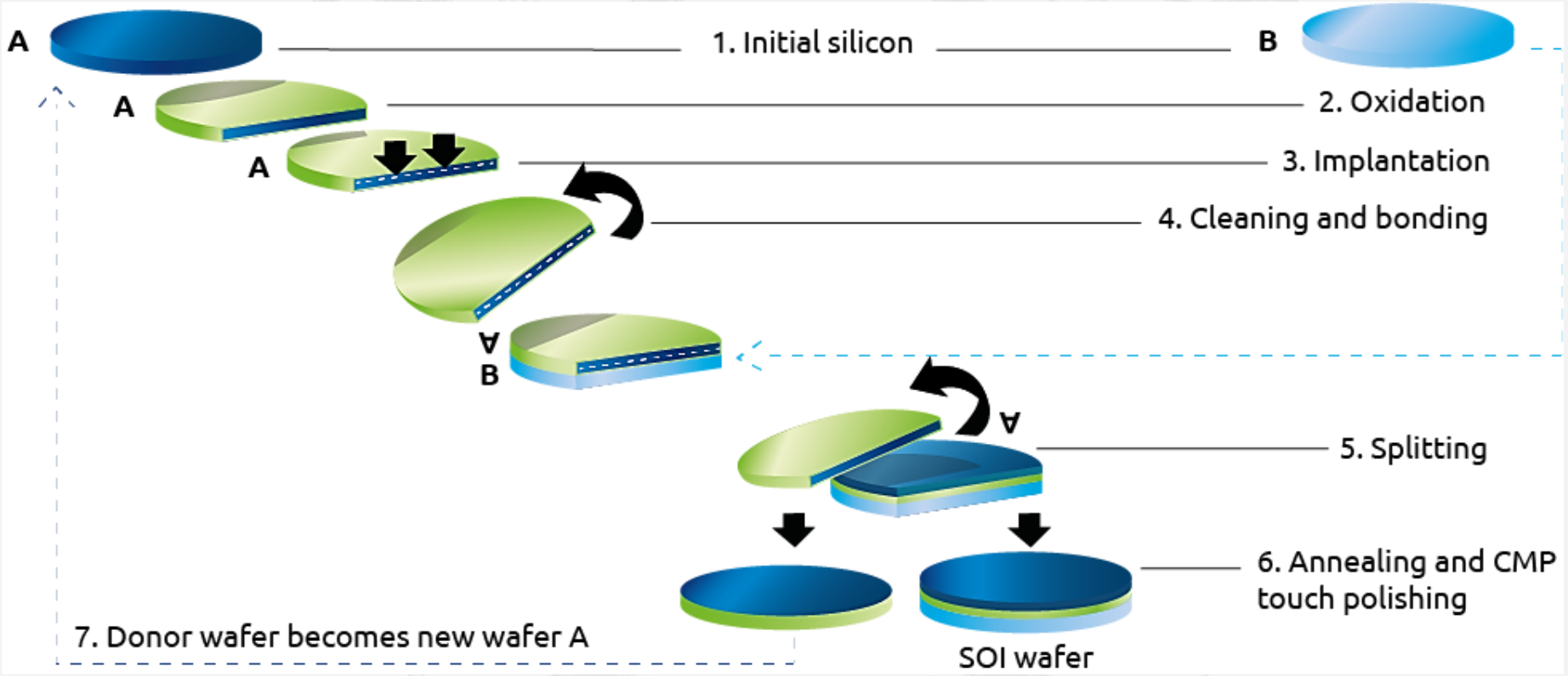
Step 2:
Handle wafer B is bonded



Step 3:
At ~400-600°C wafer A separates from B at H_2 peak

Step 4:
After splitting, SOI wafer (B) is annealed at 1100°C to strengthen the bond, whereas wafer A is reused.
Remark: SOI film thickness set by H_2 implant energy and BOX thickness.

Wafer Bonding – Smart Cut Method

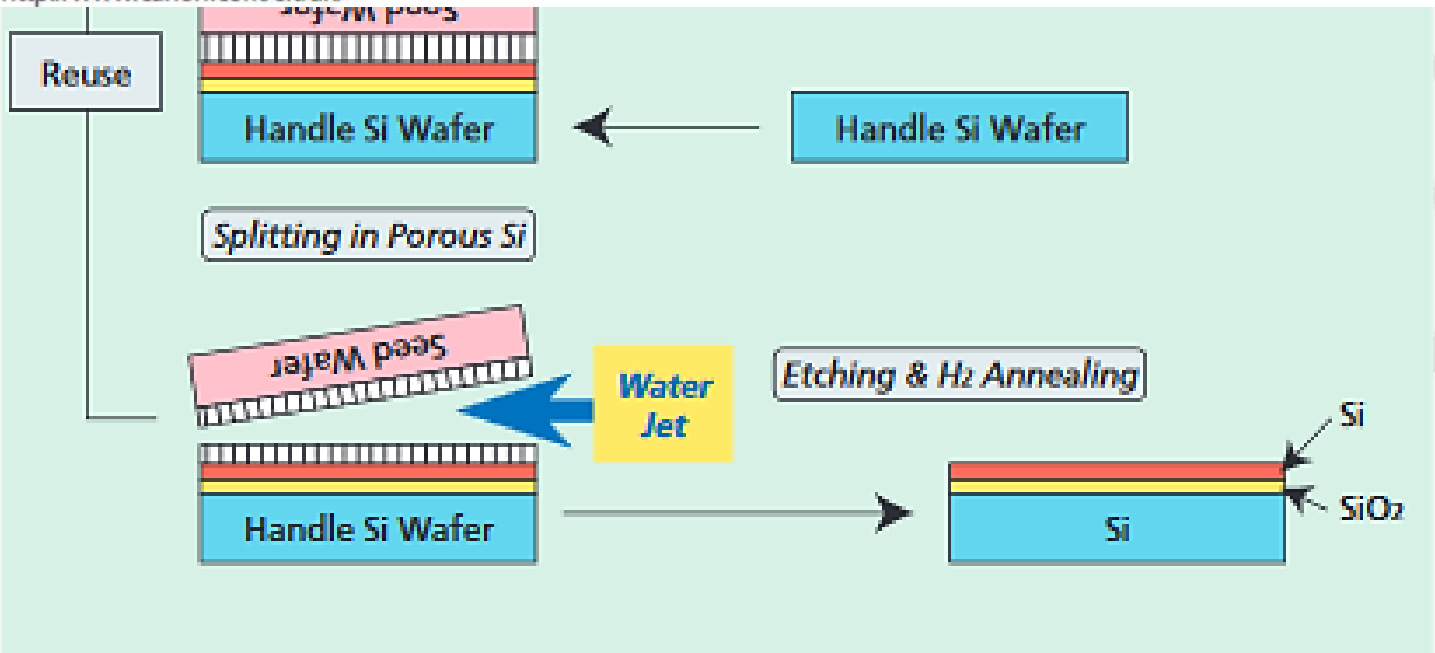


ELTRAN®: Novel SOI Wafer Technology

Cutting Edge 2

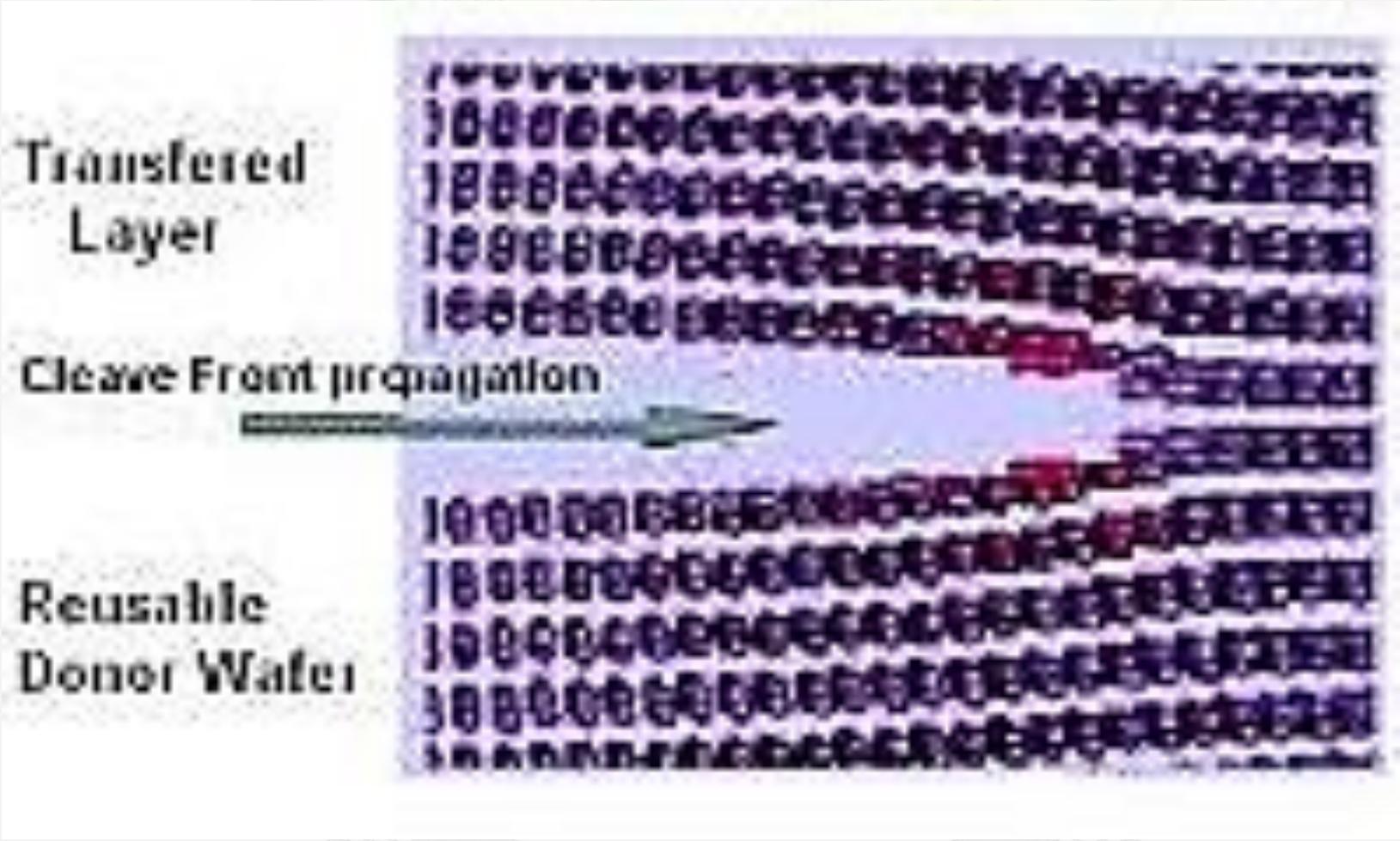
ELTRAN® ; Novel SOI Wafer Technology

Takao Yonehara and Kiyofumi Sakaguchi
ELTRAN Business Center, Canon Inc.,
6770 Tamura, Hiratsuka, Kanagawa, 254-0013, Japan
http://www.canon.com/eltran/

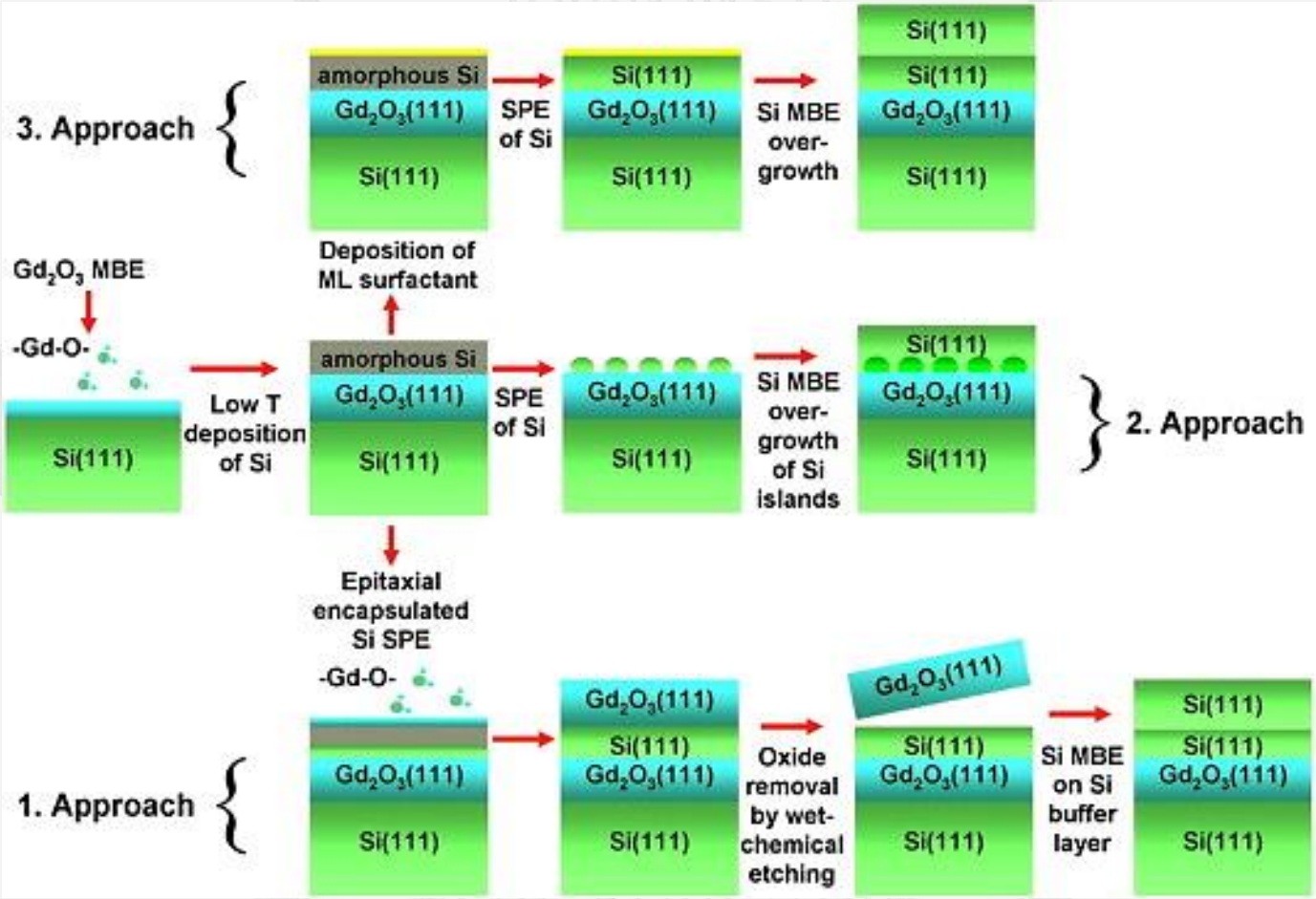


ELTRAN®(Epitaxial Layer TRANsfer) wafers

Nano Cleave


Transfered
Layer
Cleave Front propagation
Reusable
Donor Wafer

Modified solid-phase epitaxy



Epitaxial growth and thermal stability of silicon layers on crystalline gadolinium oxide
R Dargis, A Fissel, D Schwendt, E Bugiel, J Krügener, T Wietler, A Laha,
Vacuum **85** (4), 523-526

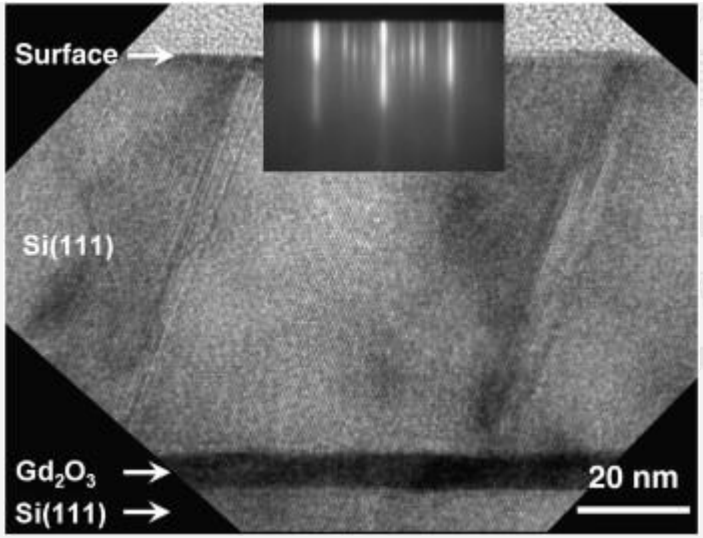
ELSEVIER

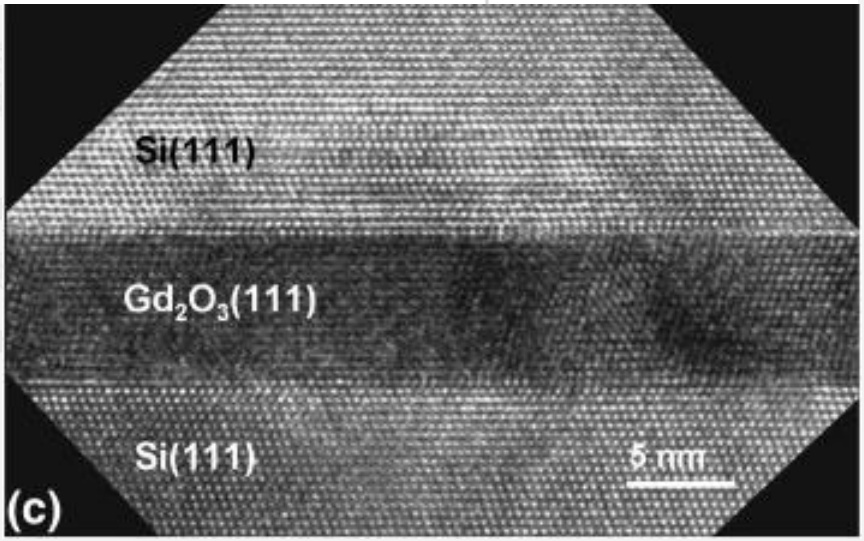
Thin Solid Films

Volume 518, Issue 9, 26 February 2010, Pages 2546-2550

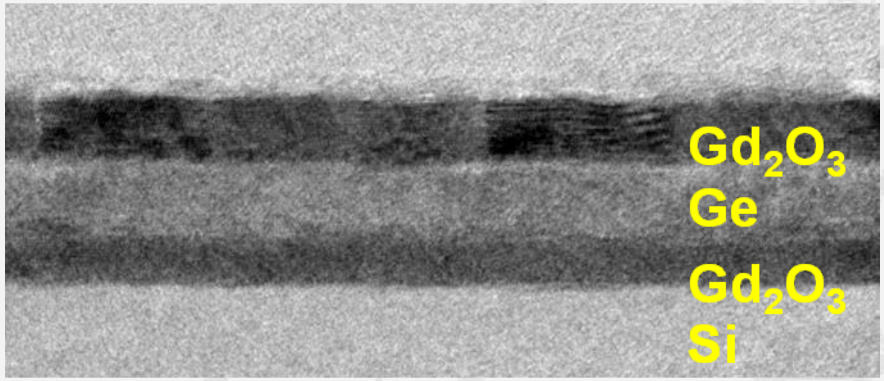
Single-crystalline Si grown on single-crystalline Gd_2O_3 by modified solid-phase epitaxy

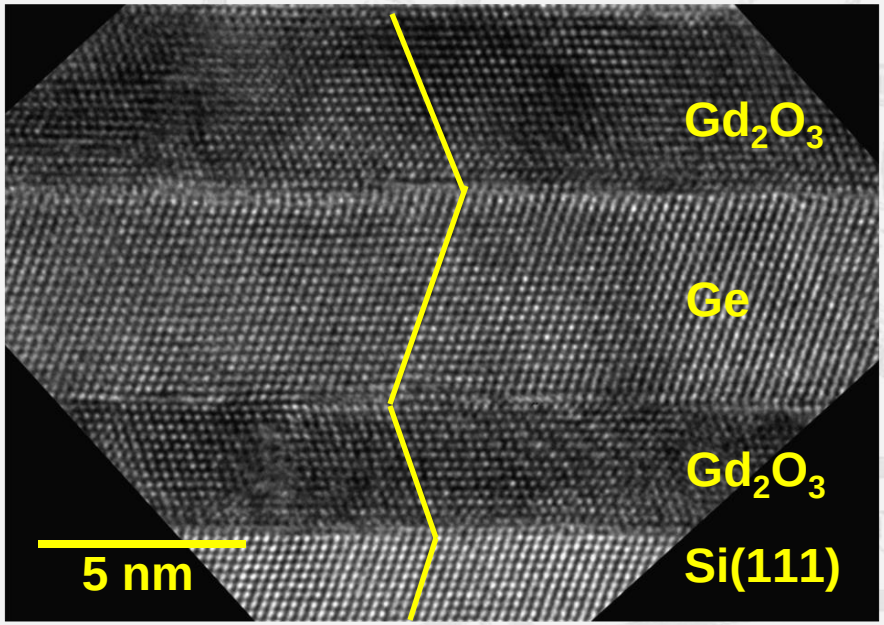
A. Fissel [a] ✉, R. Dargis [a], E. Bugiel [b], D. Schwendt [b], T. Wietler [b], J. Krügener [a], A. Laha [b], H.J. Osten [b]

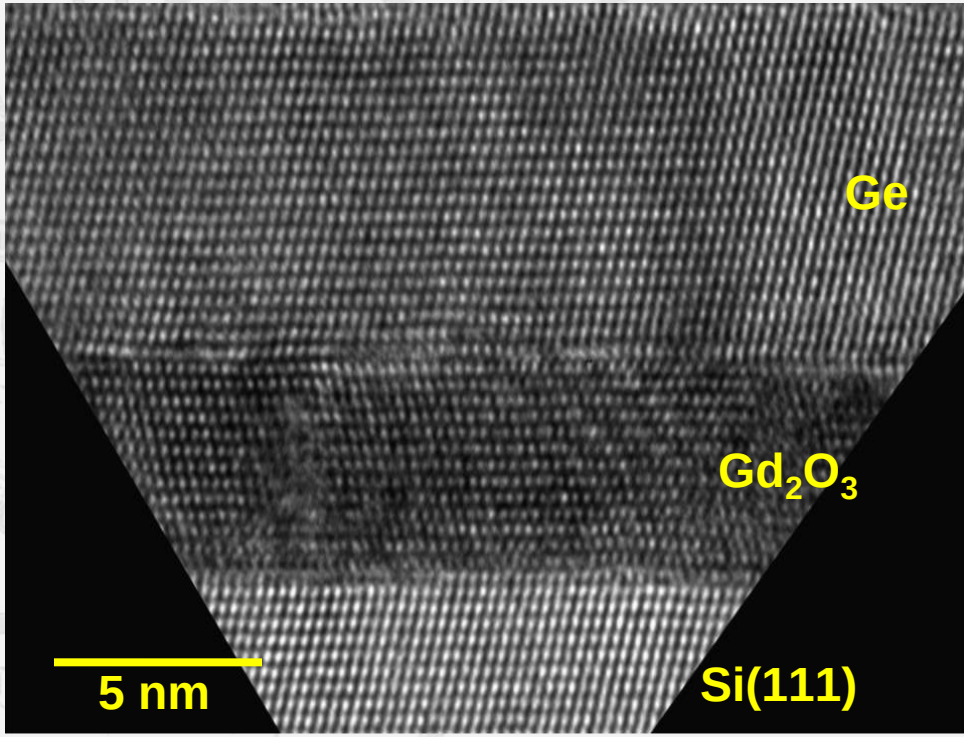




Encapsulated Solid-Phase Epitaxy of Ge







A. Laha et al, Nanotechnology 20, (2009) 475604