$$f'(\rho) = 1 - \frac{\rho}{\rho} - \ln\rho = -\ln\rho$$

$$\Rightarrow g_{next} = g - \frac{(g - g\ln g + p_{inv})}{-\ln g}$$

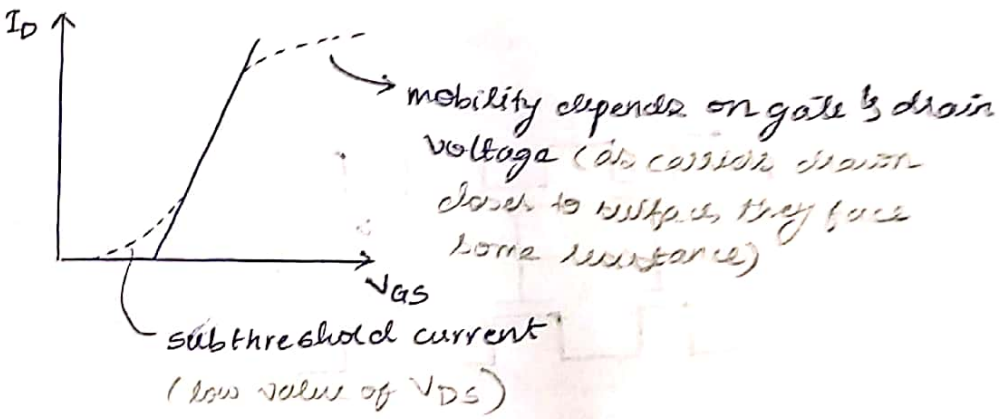
$$= \frac{g + p_{inv}}{\ln g}$$

Now, $N = \frac{\ln F}{\ln \rho}$

once we find the ceil of N we have to recalculate F.

- optimization is better for larger no. of stages rather than smaller values.

12/09



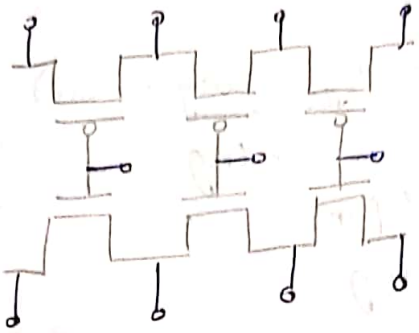
$$I_D = K_n\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

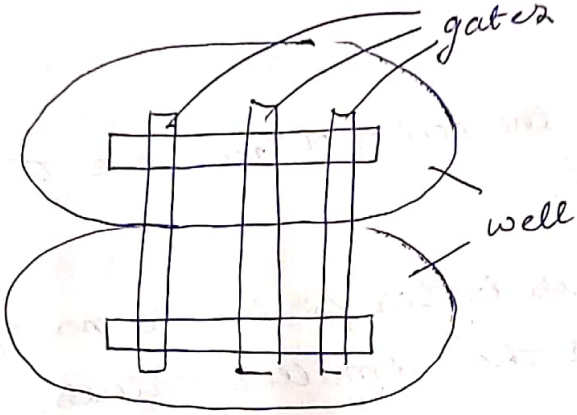
$$= K_n V_{DS}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]$$

Sea of Gates

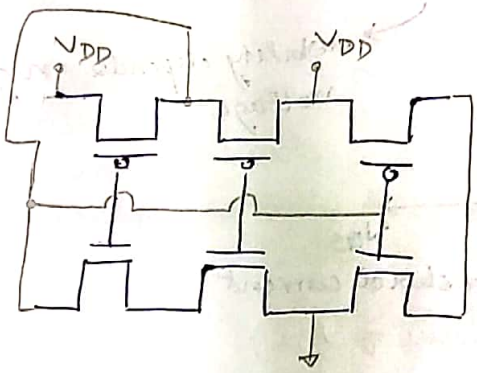
- Performance doesn't need to be optimized, then we use this
- common choice is to use 3 pairs & 2 pairs

- only the contacts brought out





(a much more compact structure)

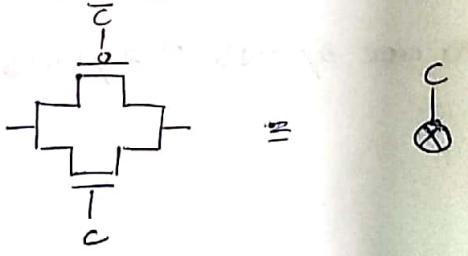


NAND NOT ⇒ AND

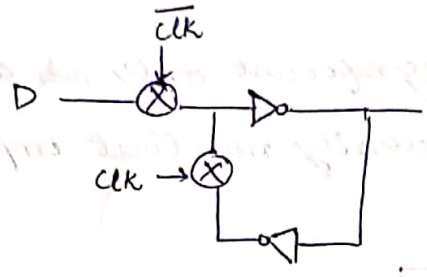
Logic diagram for NAND, NOT, NOR directly available

}

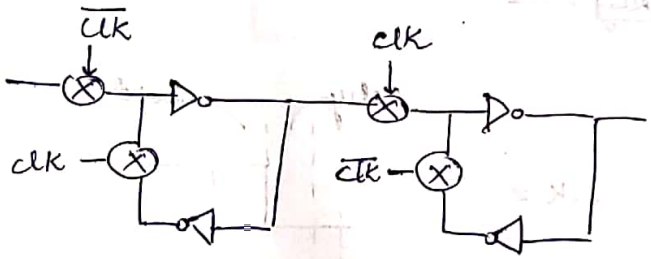
{ D-flipflop



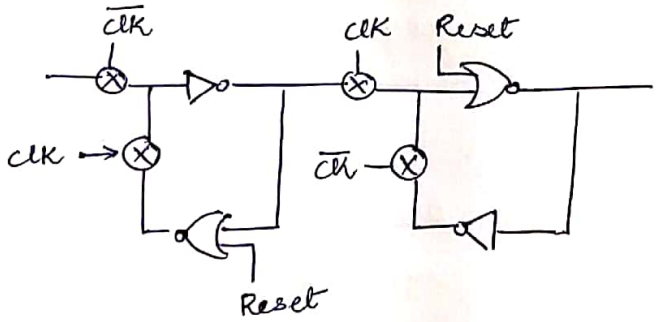
- when you observe D you make a replica of it (when clock high). when clock high we send out the replica (
- however this is level sensitive



- so we add a slave to make it edge sensitive



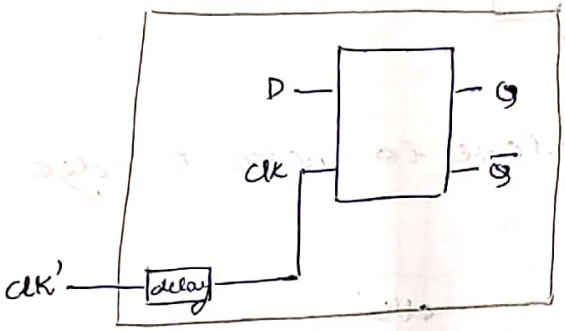
- adding a reset

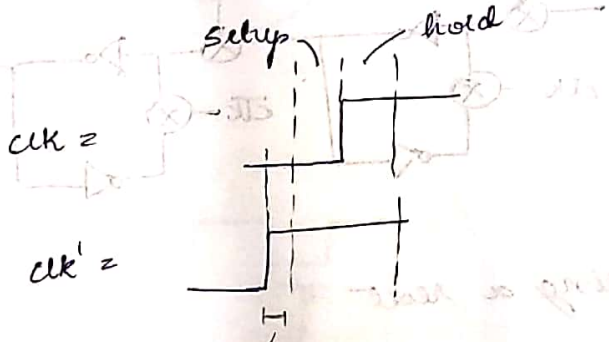


- SETUP - HOLD TIME

  - setup time : need to keep the input stable for long enough to create a replica of the input

  - setup and hold are significant only as a combination, individually not that important





setup time is negative

hold time increased

But as a combination, the setup and hold time remains const

- C_L = C_{out} + $C_{of\ next\ stage\ MOS}$

  C_p = self parasitic capacitance