EE 618 (ZELE)

CMOS ANALOG IC DESIGN End-Sem Exam

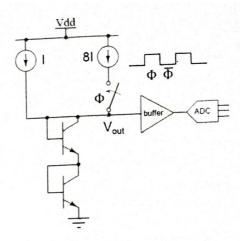
11th NOV 2017 5:30 - 8:30 PM

ACADEMIC HONESTY POLICY – IIT BOMBAY (http://www.iitb.ac.in/newacadhome/rules.jsp)
Copying in Examinations has serious consequences.

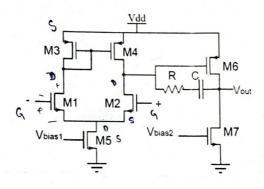
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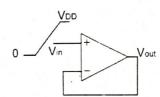
3.1 Communicate with other students during exams 3.2 Carry unauthorized material during exams 3.4 Make changes in valued answer books 3.5 Communicate with others during toilet breaks during exams State your assumptions clearly if any. 1. Draw the schematic diagram for Operational Amplifier you designed in your project. Make sure (4)that you have biasing circuits included. Label nodes with correct polarity. 2. Design a Butterworth low-pass filter to meet the following specifications using the tables/charts provided. -3 dB Bandwidth = 14.14 MHz; Stopband frequency = 141.4 MHz; Stopband Attenuation = 38 dB ✓. Using Table/Graph provided identify the order of filter. Draw RLC prototype of the filter with correctly scaled LC values annotated to meet the specifications above. £. Use signal flow graph technique to draw integrator (block diagram) based schematic. (3) Use Opamp-RC continuous time integrator to design the filter schematic. You can use inverting amplifier block where signal inversion is needed. (4) $\underline{\mathscr{E}}$. Assuming $C_{integrator} = 1pF$, find out values of all resistors. (2)1/2 Draw schematic diagram for parasitic insensitive switched-capacitor integrator. Make sure polarities and phases are properly annotated. g. Use the integrator from (f) in (c) to construct switched-capacitor filter schematic. (4) h. Choose clock frequency. Justify why? (1) Annotate your clocking scheme for filter. For all SC integrators Cu = 0.25pF (input capacitor). Figure out values of CI (feedback capacitors) of all integrators. Discuss one advantage and disadvantage each of both - continuous time and switchedcapacitor filter. (2)

For the circuit on right, derive an expression for V_{out} (Ø) -V_{out} (Ø). Two bipolar transistors are identical. (4)

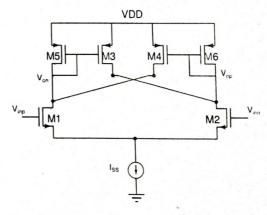


For the two-stage opamp shown below, calculate V_{inmax} and V_{inmin} for which all transistors are in saturation when configured in Unity gain as shown on right. Assume all transistors have same V_T = 0.4 and V_{dsat}= 0.2. Vdd = 1.8. Also calculate peak to peak output swing in Unity gain mode. (4)





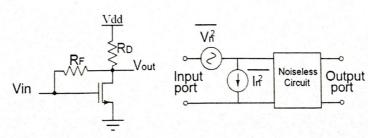
 For the amplifier circuit on right, calculate the differential voltage gain. You can first calculate output impedance using test voltage source. Ignore r_o for PMOS transistors. Ignore body-effect. (3)



- 6. For the amplifier circuit below, Calculate
 - Input referred noise voltage. (Short circuit the input to calculate)
- (3)

(3)

b. Input referred noise current. (Open circuit input to calculate)

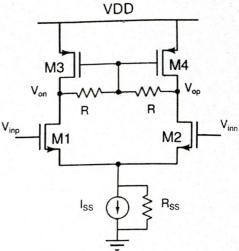


Ignore ro.

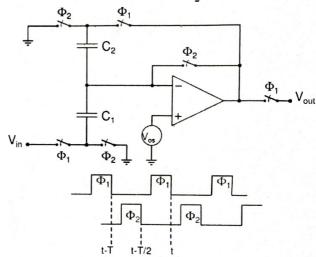
- 7. For fully differential opamp, calculate:
 - a. Common-mode voltage at output
 - b. Differential Gain

- (2) (2)
- c. Common-mode Gain
- (2)

Ignore Body effect. M1, M2 are identical (g_{mn} , r_{on}), M3, M4 are identical (g_{mp} , r_{op}).



For the switched-capacitor circuit on right, use charge conservation principle to figure out V_{out}/V_{in} transfer function. V_{os} is the input-referred offset voltage (constant) of the OPAMP. (4)

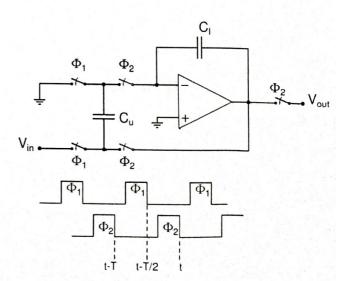


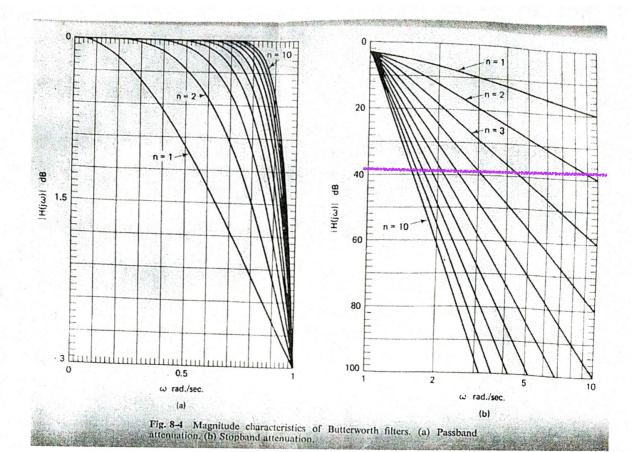
 For the switched-capacitor circuit below, use charge conservation principle to figure out V_{out}/V_{in} transfer function. Use z-domain analysis.

(4)

Identify the filter type.

(1)





BUTTERWORTH FILTER

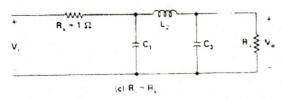


Fig. 8-9 Circuit structures of low pass Butterworth filters.

FILTER ORDER

	NAME OF TAXABLE PARTY.		and and		-		C.	t topic of the control of the control	r
N	C_1	Lı	C1	4.4	C ₃	L	C ?	A B	С,
1	2.0000		200						
2	1.4142	1.4142							
3	1.0000	2.0000	1.0000						
4	0.7654	1.8478	1.8478	0.7654					
5	0.6180	1.6180	2.0000	1.6180	0.6180				
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176			
7	0.4450	1 2470	1.8019	2.0000	1.8019	1.2470	0.4450		
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902	
0	0.3473	1.0000	1.5321	1.8794	2.0000	1 8794	1.5321	1.0000	0.347