High-Level Synthesis -III

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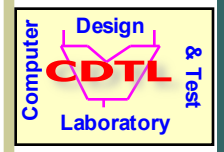


E0-285: CAD of VLSI Systems

Resource Sharing

Resource sharing: Assignment of resource to more than one operation

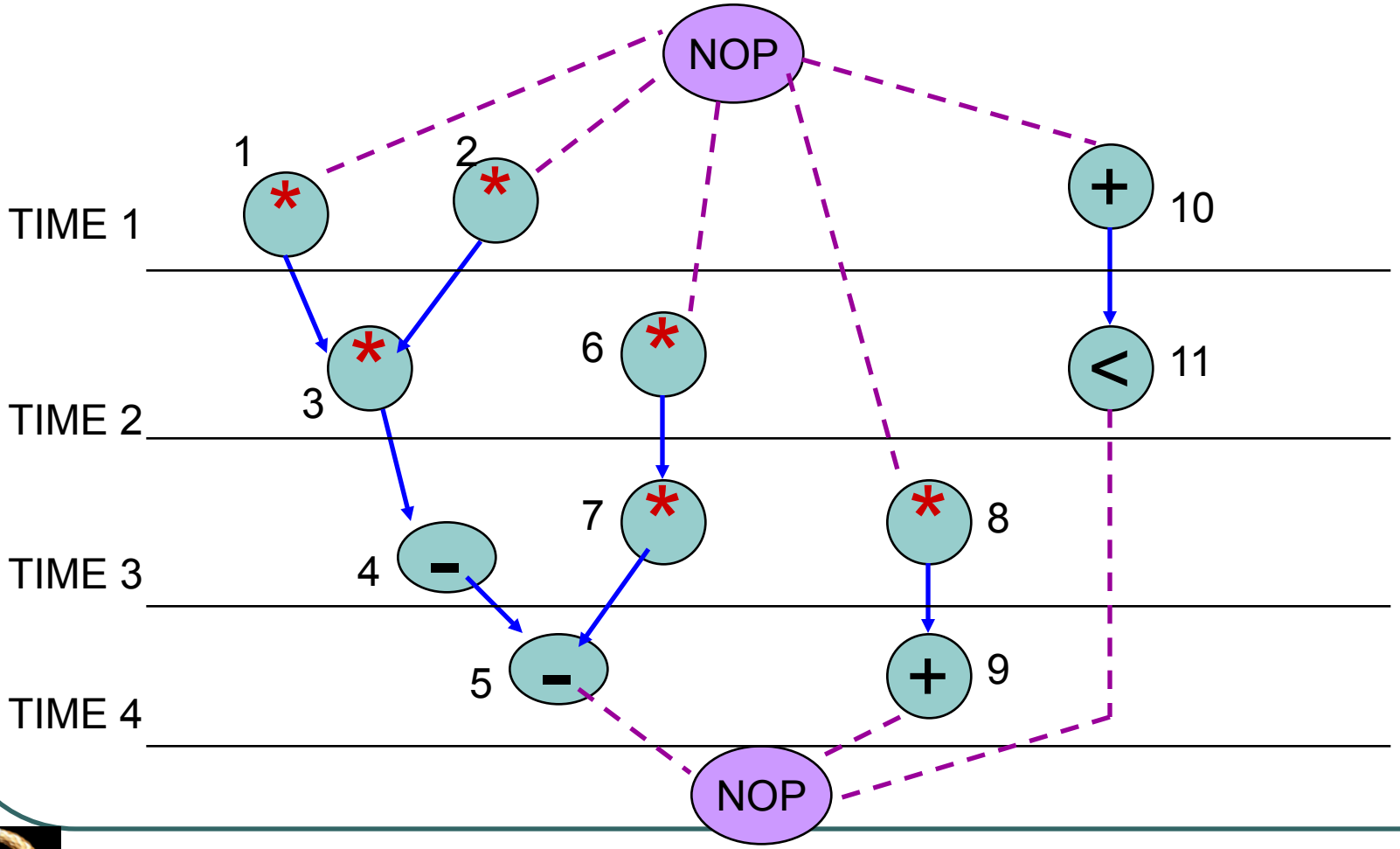
Goal: Reduce area

Resource binding: explicit definition of mapping between resources and operation

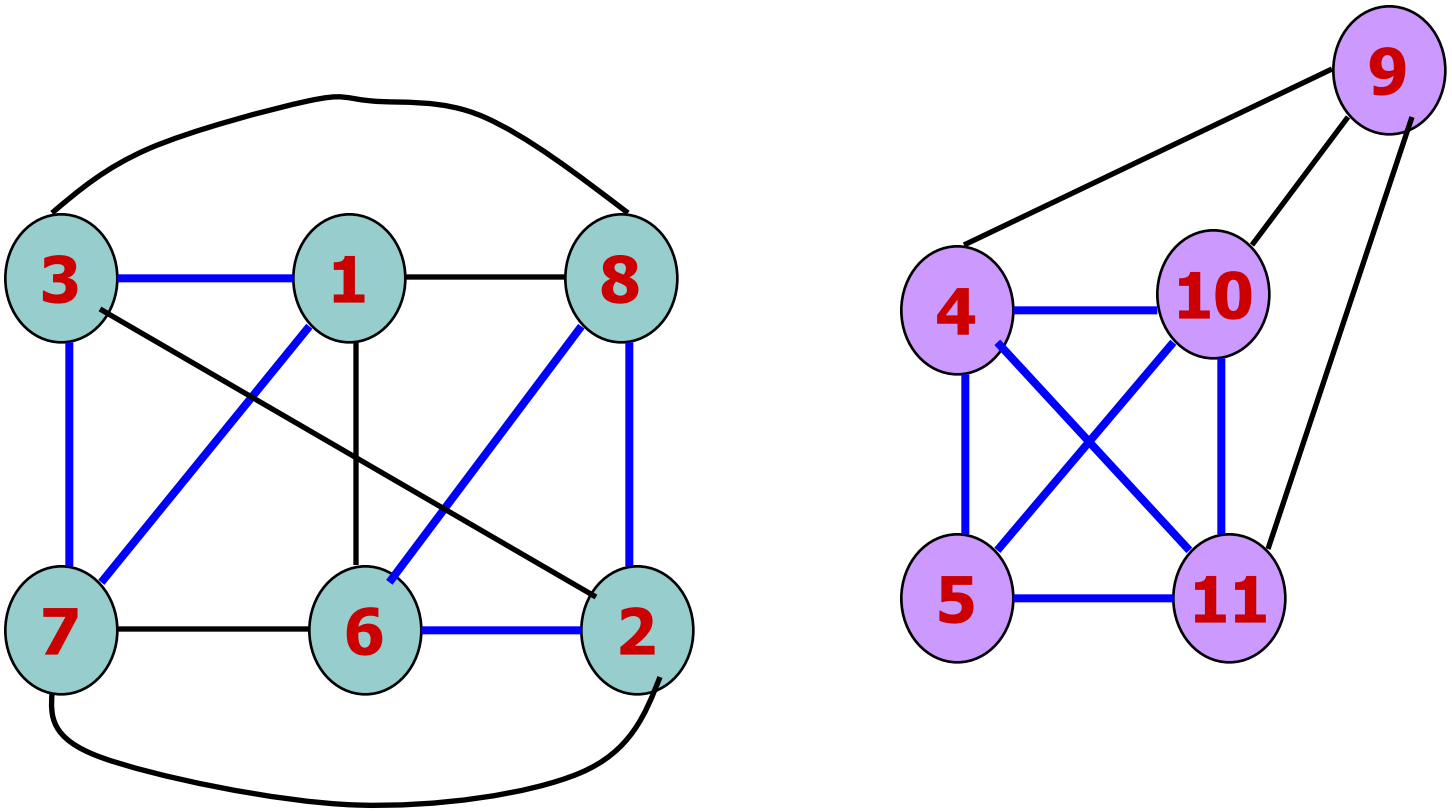
Two or more operation may be bound to the same resource if they are not concurrent and they can be implemented by the resources of the same type

- Compatible operations

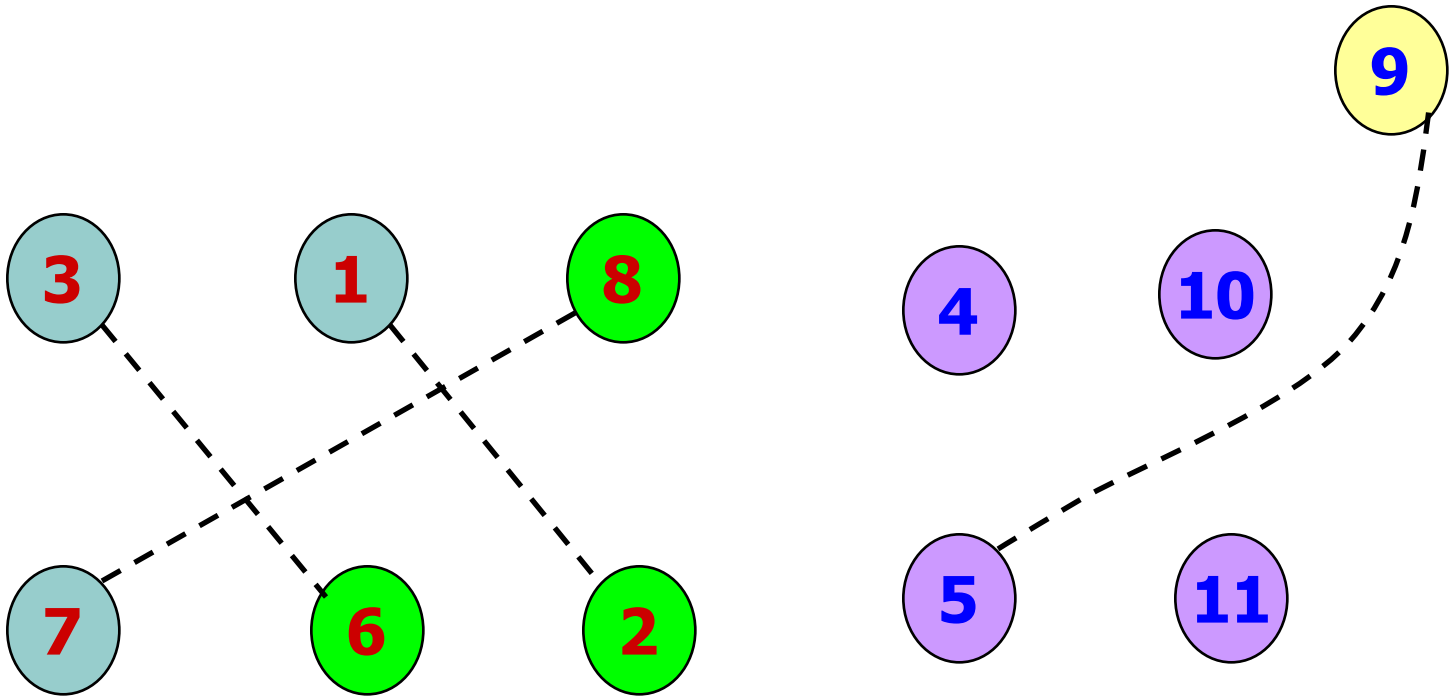
Scheduled Sequencing Graph



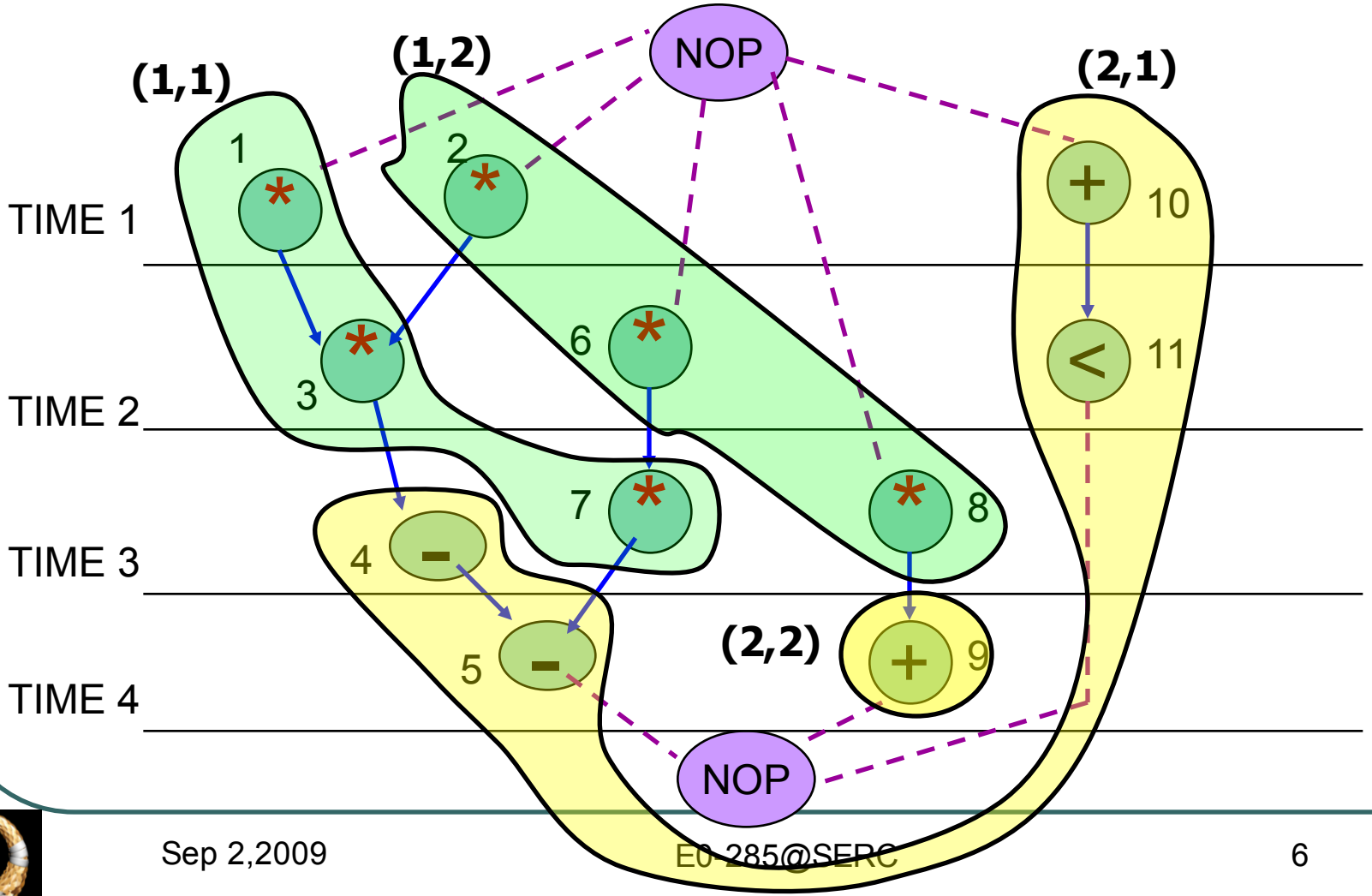
Compatibility Graph



Conflict Graph



Scheduled and Bound Sequencing Graph



Resource Sharing in Non-Hierarchical Seq. Graph

ILP Formulation

- All operations and resources have the same type
- Use binary decision variable with two indices
  - $B = \{b_{ir}; i = 1,2,\ldots, n_{op}; r = 1,2, .. a\}$
- A set of binary decision constants with two indices
  - $X = \{x_{il}, i = 1,2, .., n_{op}; l = 1,2, .., \lambda+1\}$
- b_{ir} is 1 only when v_i is bound to resource r
- x_{il} is 1 only when v_i starts in step l

Resource Sharing in Non-Hierarchical Seq. Graph

ILP Formulation

Each operation should be assigned to one and only one resource

$$\Sigma_{r=1}^{a} b_{ir} = 1, \quad i = 1,2, \ldots, n_{op}$$

At most one operation can be executing, among those assigned to resource ***r***, at any time step

$$\Sigma_{i=1}^{nop} b_{ir} \Sigma_{m=l-di+1}^{l} x_{im} \leq 1$$

$b_{ir} \in \{0, 1\}$

Resource Sharing in Non-Hierarchical Seq. Graph

Two operations (Multiplier type, ALU type)

Unit Delay

Resource 1

$\Sigma_{r=1}^{a1} b_{ir} = 1, \quad T(v_i) = 1$

$\Sigma_i b_{ir} x_{il} \leq 1$

Resource 2

$\Sigma_{r=1}^{a2} b_{ir} = 1, \quad T(v_i) = 2$

$\Sigma_i b_{ir} x_{il} \leq 1$

Resource Sharing in Non-Hierarchical Seq. Graph

$a1 = 1$

Find solution of

$$b_{i1} = 1, \quad \text{for all } i \in \{1,2,3,6,7,8\}$$

$$\Sigma_{i \in \{1,2,3,6,7,8\}} b_{i1}\, x_{il} \leq 1, \quad l = 1,2, \ldots, 5$$

Solution does not exists

$b_{1,1} + b_{2,1} \leq 1$

Contradict with the first

Resource Sharing in Non-Hierarchical Seq. Graph

a1 = 2

Find solution of

$b_{i1} + b_{i2} = 1$, for all i ∈ {1,2,3,6,7,8}

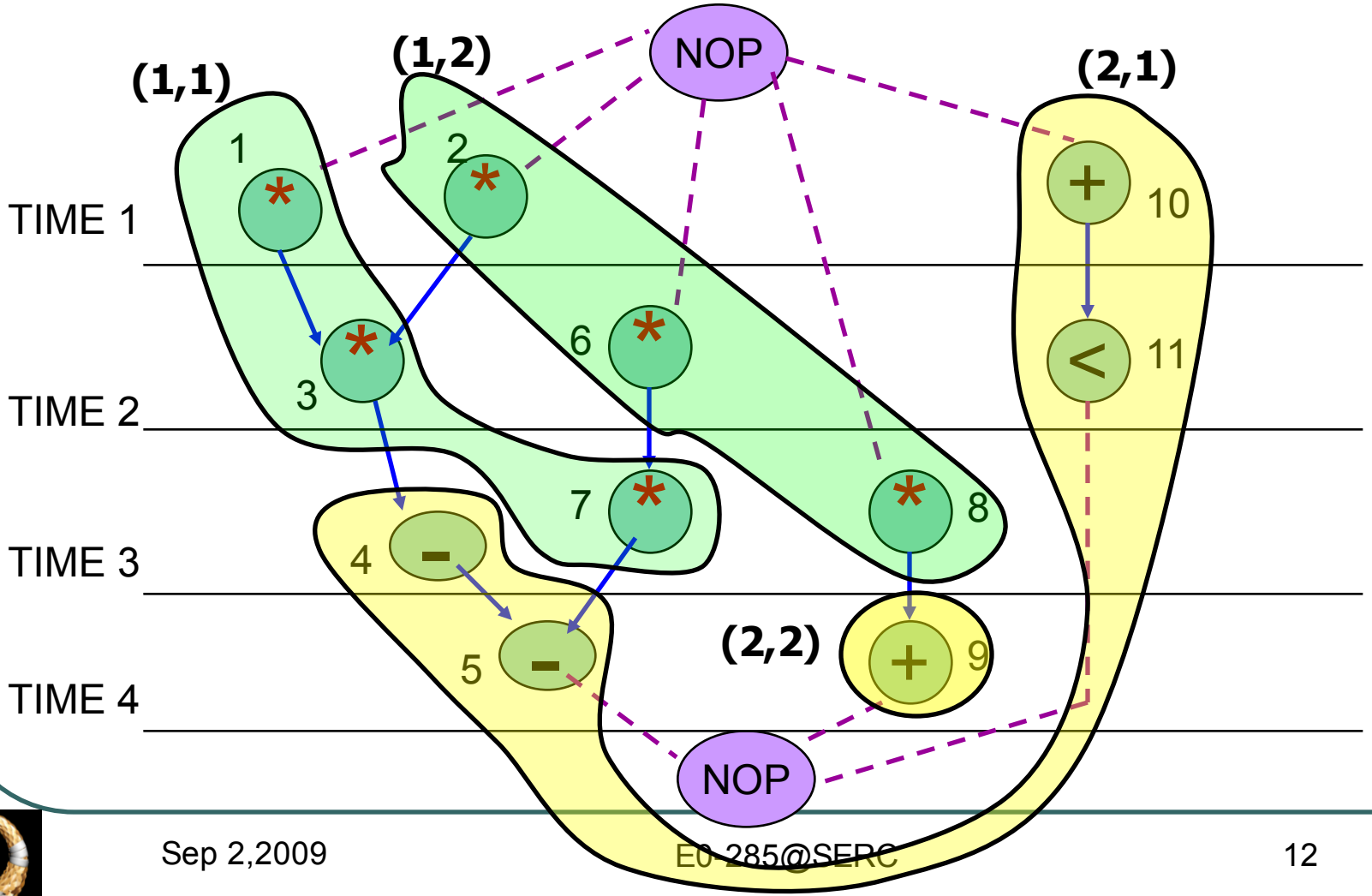
$\Sigma_{i \in \{1,2,3,6,7,8\}} b_{i1} x_{il} \leq 1, \quad l = 1,2, \ldots, 5$

$\Sigma_{i \in \{1,2,3,6,7,8\}} b_{i2} x_{il} \leq 1, \quad l = 1,2, \ldots, 5$

Solution

$b_{1,1} = 1, b_{2,2} = 1, b_{3,1} = 1, b_{6,2} = 1, b_{7,1} = 1, b_{8,2} = 1$

Scheduled and Bound Sequencing Graph

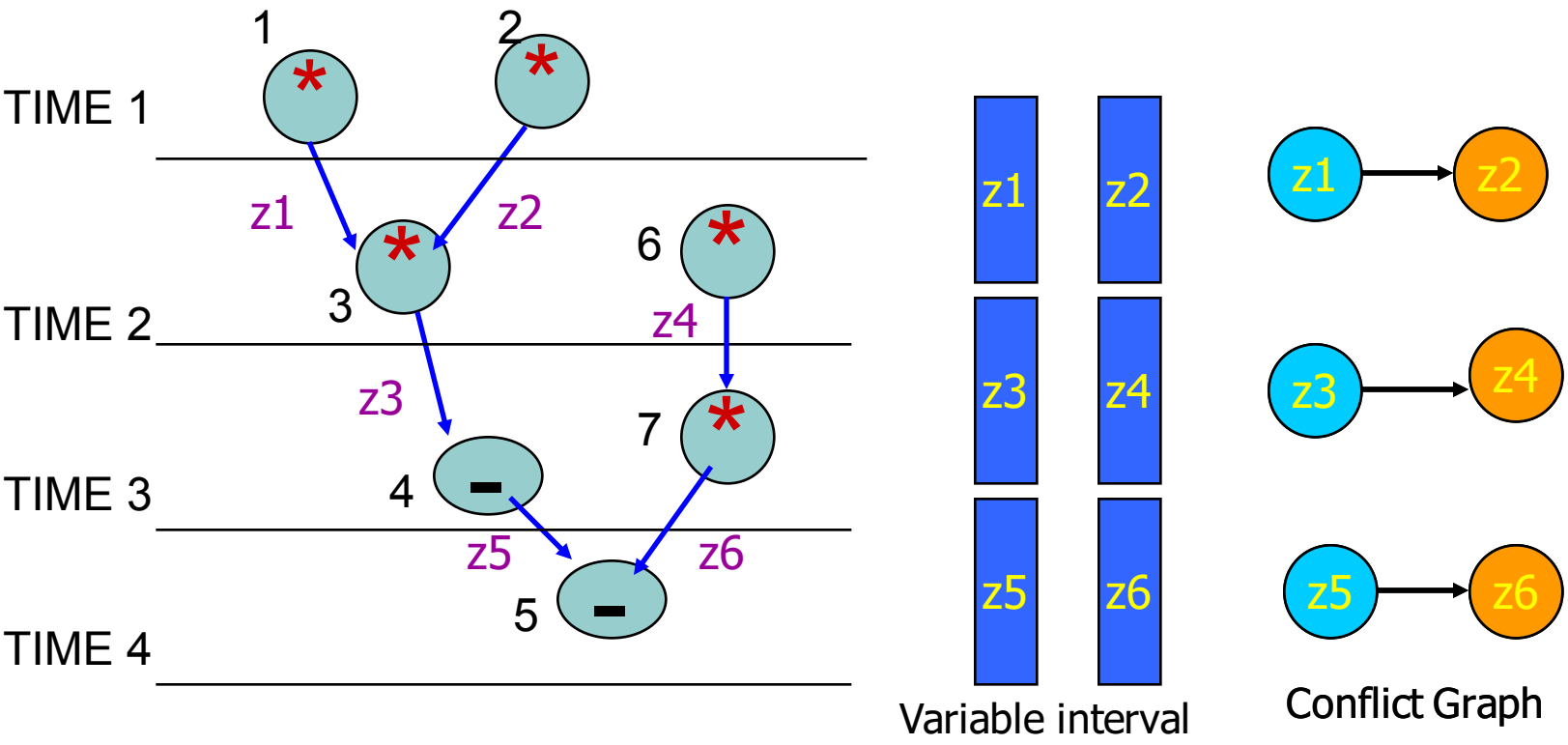


Register Binding

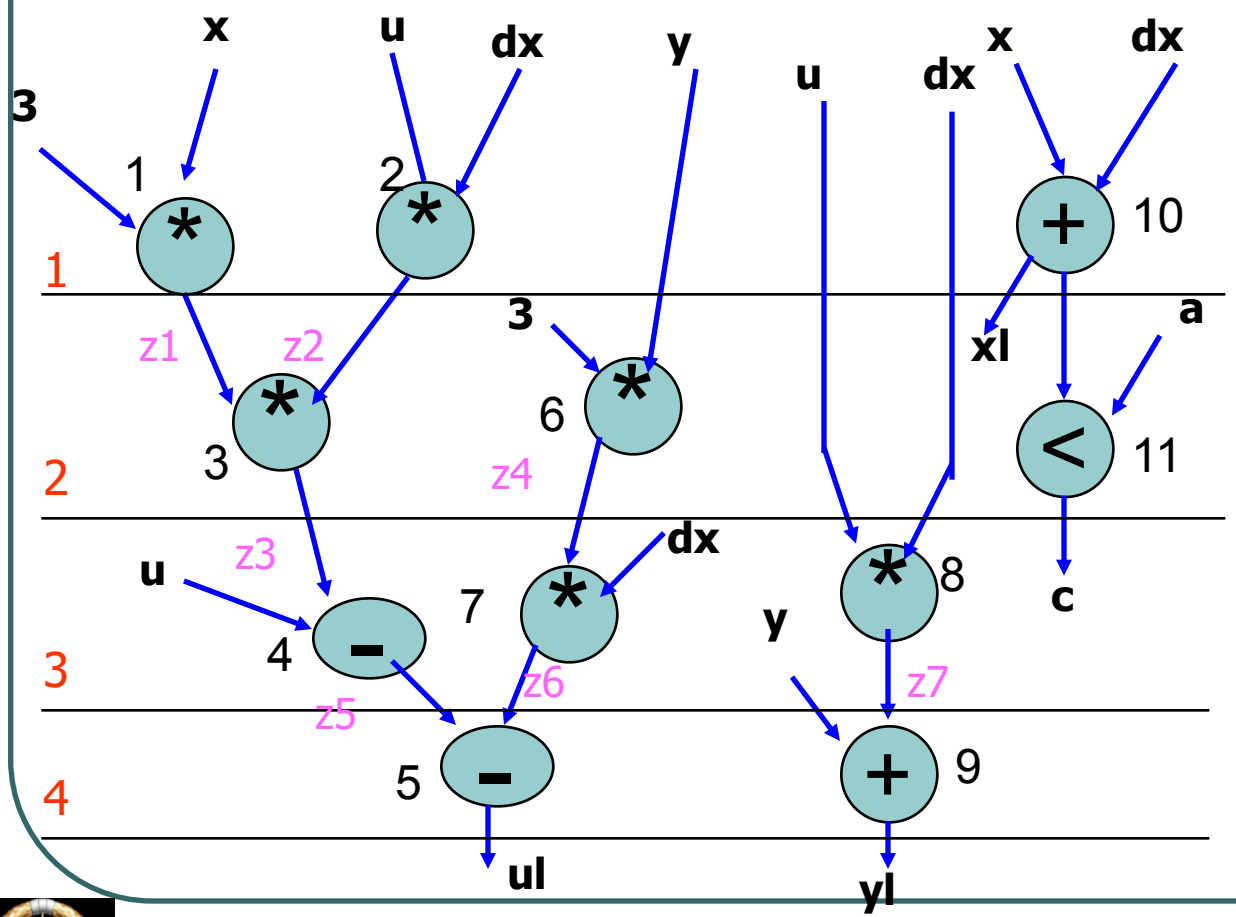
- Registers hold values of variables
  - ❖ Lifetime
  - ➢ Lifetime can be data dependent – branching
  - ➢ Implementation that associates a register with each variable is suffice
    - ❖ Inefficient
  - ➢ Variables that are alive in different interval can share the same register
    - ➢ Compatible

Register Sharing

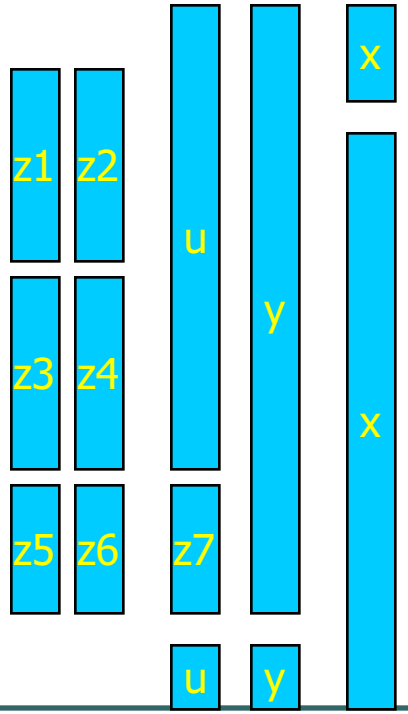
Construct compatibility or conflict graph



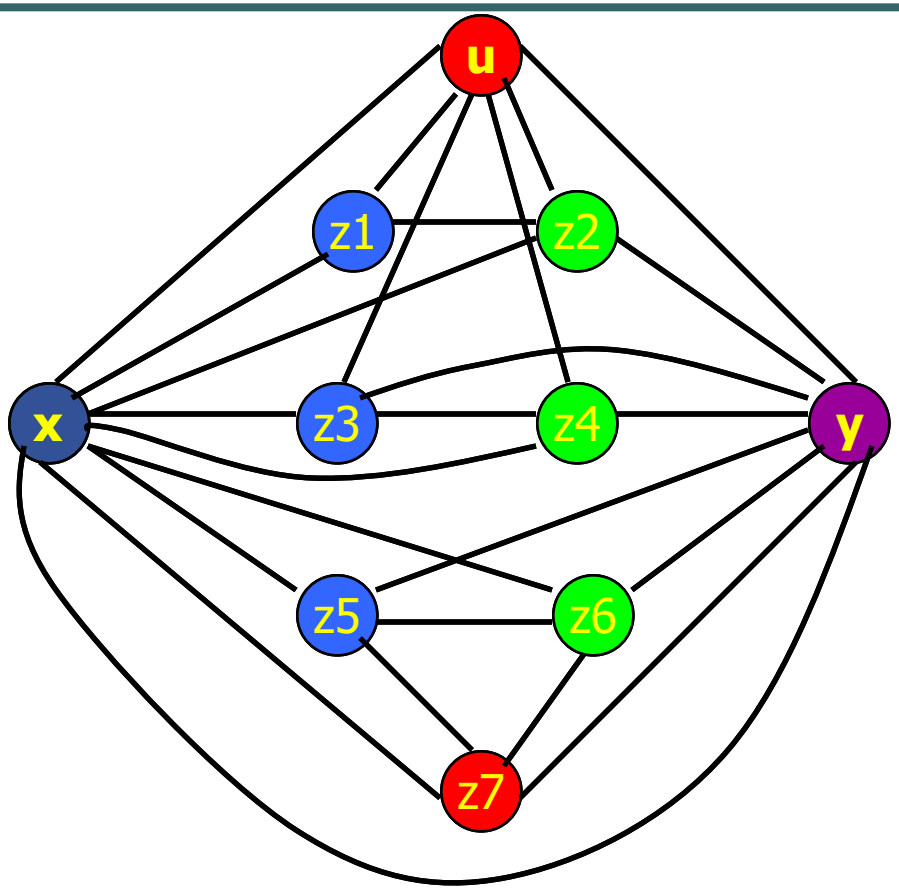
Register Sharing



xl = x + dx
ul = u – (3*x*u*dx) – (3*y*dx)
c = xl < a



Register Sharing



Conflict Graph

Multi-port Memory Binding

- Multi-port memory arrays to store the values of variable
- Assume memory with a ports (either read or write) - GPRF
- Large memory - to hold all data
  - Computing minimum number of memory ports a required to access as many variables as needed
    - If each variable access the memory through the same port
    - Functional resource binding
    - Ports can be seen as interface resources

Multi-port Memory Binding

- If variables can be accessed through different port
- Minimum port – maximum number of concurrent access
- Max $\sum_{i=1}^{nvar} x_{il}$
- Dual Problem
  - Assume fix number of ports and maximize the number of variables to be stored, subject to port limitation
  - Max $1^T b$ s.t.
  - $\sum_i b_i x_{il} \leq a$

Multi-port Memory Binding

- Scheduled sequence of operations
  - Step 1: $z_3 = z_1 + z_2$; $z_{12} = z_1$
  - Step 2: $z_5 = z_3 + z_4$; $z_7 = z_3 * z_6$; $z_{13} = z_3$
  - Step 3: $z_8 = z_3 + z_5$; $z_9 = z_1 + z_7$; $z_{11} = z_{10}/z_5$
  - Step 4: $z_4 = z_{11} \wedge z_8$; $z_{15} = z_{12} \wedge z_9$; z_{11}
  - Step 5: $z_1 = z_{14}$; $z_2 = z_{15}$

➢ $b_1 + b_2 + b_3 + b_{12} \leq a$

Multi-port Memory Binding

- $b_1+b_2 + b_3 + b_{12} \leq a$
- $b_3+b_4 + b_5 + b_6 + b_7 + b_{13} \leq a$
- $b_1+ b_3+b_5 + b_7 + b_8 + b_9 + b_{10} + b_{11} \leq a$
- $b_8+ b_9+b_{11} + b_{12} + b_{14} + b_{15} \leq a$
  - $b_1+ b_2+b_{14} + b_{15} \leq a$

Multi-port Memory Binding

- for a =1
  - $\{b_2 , b_4 , b_8\}$ are non-zero
- For a = 2
  - $\{b_2 , b_4 , b_5 , b_{10} , b_{12} , b_{14} \}$ are non zero
- For a = 3
  - $\{b_1, b_2 , b_4 , b_6 , b_8 , b_{10} , b_{12}, b_{13}, b_{14} \}$ are non zero

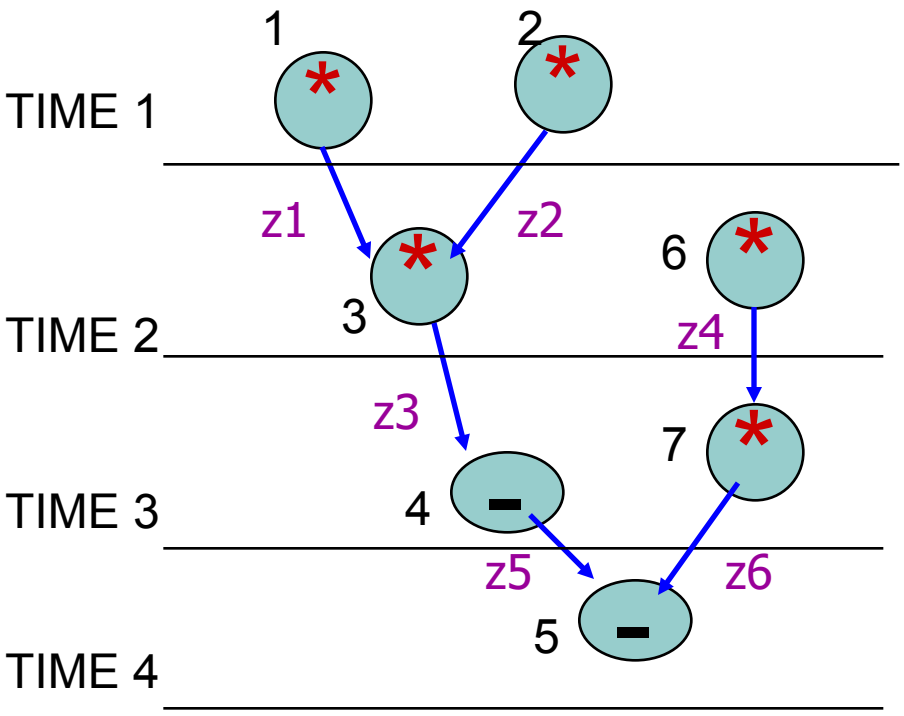
Bus Sharing

- Act as transfer resources the t feed data to functional resources
- Operation of writing specific bus
  - Vertex in SG
- Conflict and compatibility graph can be generated
- Alternate
  - Bus may not be described in SG
  - Usage can be derived from exploiting timing of data transfer

Bus Sharing

- Problems
  - Minimum number of buses
  - Maximum number of data transfer that can done through given number of buses

Bus Sharing and Binding



- $b_1 + b_2 \leq a$
- $b_3 + b_4 \leq a$
- $b_5 + b_6 \leq a$

Concurrent Scheduling and Binding

Concurrent Scheduling and Binding

- **Define upper bound on resource usage and latency**

Problems

- **Intractable problem**

Concurrent Scheduling and Binding

ILP Formulation

1. Start time of each operation is unique

   $\Sigma_l x_{il} = 1$

2. Sequencing relations represented by $G_s(V,E)$ must be satisfied

   $\Sigma_l \, l. x_{il} \geq \Sigma_l \, l. x_{jl} + d_j$

3. Resource bound must be met at every schedule step

   $\Sigma_k \Sigma_m x_{im} \leq a_k$

Concurrent Scheduling and Binding

4. Operation has to bound one and only one resource

$$\Sigma_r \, b_{ir} = 1$$

5. Operation bound to same resource must not be concurrent

$$\Sigma_i \, b_{ir} \sum_{m = l-d_i+1}^{l} x_{im} \leq 1$$

Latency: $\lambda = \Sigma_l \, l. \, x_{nl} - \Sigma_l \, l. \, x_{0l}$

Minimize area and latency simultaneously

ILP Formulation

All operation must start only once

$x_{0,1} = 1$

$x_{1,1} = 1$

$x_{2,1} = 1$

$x_{3,2} = 1$

$x_{4,3} = 1$

$x_{5,4} = 1$

$x_{6,1} + x_{6,2} = 1$

$x_{7,2} + x_{7,3} = 1$

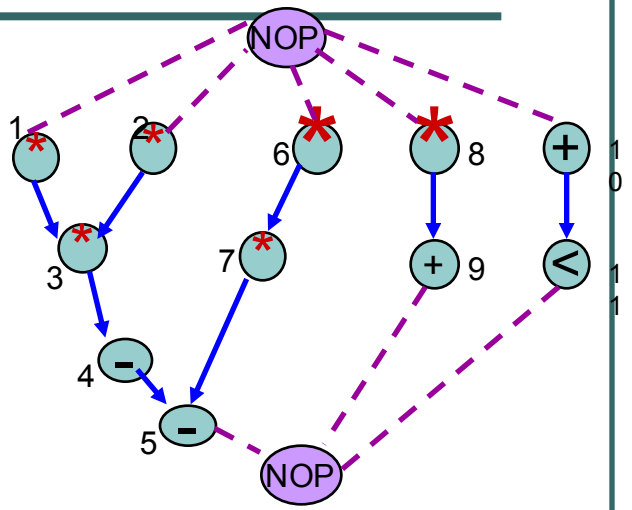
$x_{8,1} + x_{8,2} + x_{8,3} = 1$

$x_{9,2} + x_{9,3} + x_{9,4} = 1$

$x_{10,1} + x_{10,2} + x_{10,3} = 1$

$x_{11,2} + x_{11,3} + x_{11,4} = 1$

$x_{n,5} = 1$



ILP Formulation

Constraints – based on sequencing

(more than one starting time for at least one operation)

$$2\,x_{7,2} + 3\,x_{7,3} - x_{6,1} - 2\,x_{6,2} - 1 \geq 0$$

$$2\,x_{9,2} + 3\,x_{9,3} + 4\,x_{9,4} - x_{8,1} - 2\,x_{8,2} - 3\,x_{8,3} - 1 \geq 0$$

$$2\,x_{11,2} + 3\,x_{11,3} + 4\,x_{11,4} - x_{10,1} - 2\,x_{10,2} - 3\,x_{10,3} - 1 \geq 0$$

$$4\,x_{5,4} - 2\,x_{7,2} - 3\,x_{7,3} - 1 \geq 0$$

$$5\,x_{n,5} - 2\,x_{9,2} - 3\,x_{9,3} - 4\,x_{9,4} - 1 \geq 0$$

$$5\,x_{n,5} - 2\,x_{11,2} - 3\,x_{11,3} - 4\,x_{11,4} - 1 \geq 0$$

ILP Formulation

Resource Constraints

$x_{1,1} + x_{2,2} + x_{6,1} + x_{8,1} \leq a1$

$x_{3,2} + x_{6,2} + x_{7,2} + x_{8,2} \leq a1$

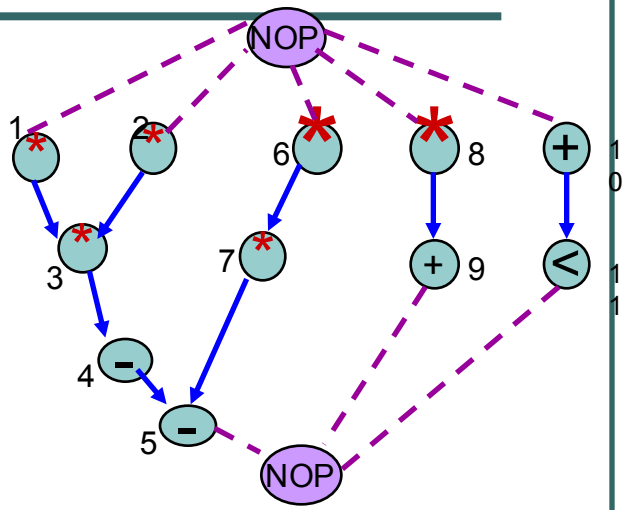
$x_{7,3} + x_{8,3} \leq a1$

$x_{10,1} \leq a2$

$x_{9,2} + x_{10,2} + x_{11,2} \leq a2$

$x_{4,3} + x_{9,3} + x_{10,3} + x_{11,3} \leq a2$

$x_{5,4} + x_{9,4} + x_{11,4} \leq \mathbf{a2}$



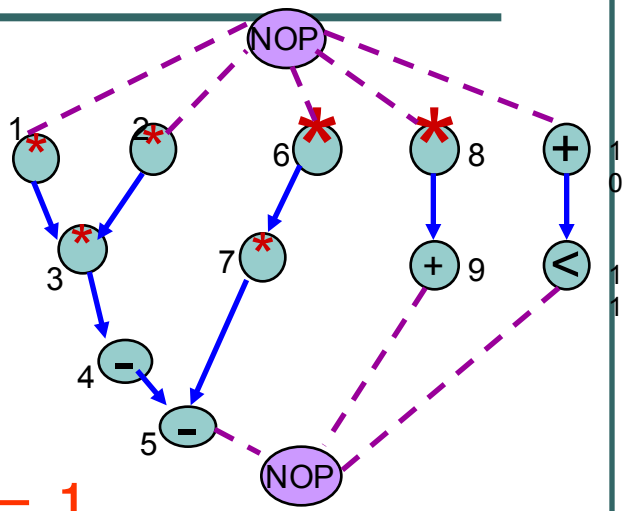
ILP Formulation

Resource Bind

$$b_{1,1} + b_{2,1} + b_{3,1} + b_{6,1} + b_{7,1} + b_{8,1} = 1$$

$$b_{1,2} + b_{2,2} + b_{3,2} + b_{6,2} + b_{7,2} + b_{8,2} = 1$$

$$b_{1,a1} + b_{2,a1} + b_{3,a1} + b_{6,a1} + b_{7,a1} + b_{8,a1} = 1$$



THANK YOU