EE 618

CMOS ANALOG IC DESIGN Quiz 1

12th Aug 2018 4:00 – 5:00 PM

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3.1 Communicate with other students during exams
3.2 Carry unauthorized material during exams
3.4 Make changes in valued answer books
3.5 Communicate with others during toilet breaks during exams

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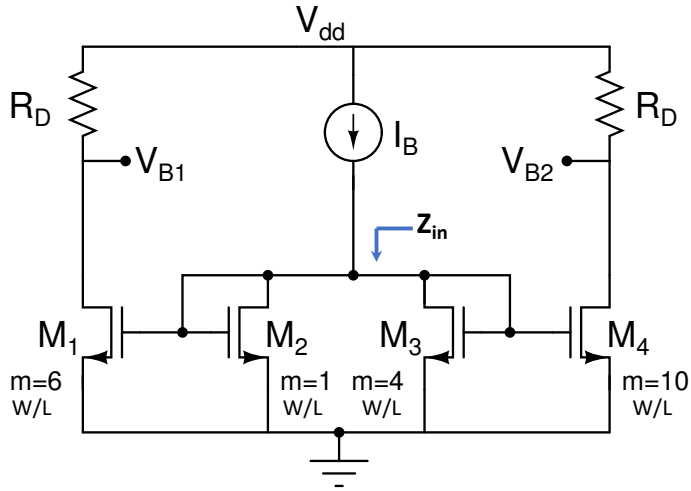
State your assumptions clearly if any.

1.

A. Calculate Z_{in} in terms of I_B, W/L & $\mu_n C_{ox}$. (2)

B. Calculate V_{B1} and V_{B2} in terms of V_{DD}, R_D, I_B, W/L & $\mu_n C_{ox}$. (4)



Ignore Body effect, Channel length modulation.
m= multiplier.

2. Using one NMOS transistor and one Resistor, draw the following three amplifiers (3).
   a. Common-source Amplifier
   b. Common-gate Amplifier
   c. Common-drain Amplifier

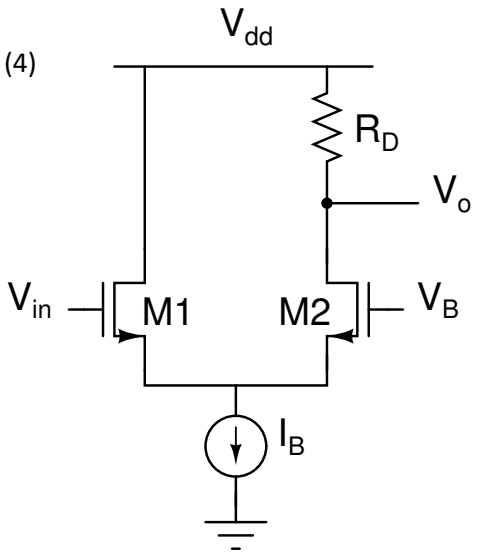
   Clearly label input and output. Write gain expression for each case (9).

   Do not ignore Body effect, Channel length modulation. Body must be connected to ground.

3. Draw small signal model for the circuit below. (2)

   Calculate small-signal gain for the amplifier below. (4)

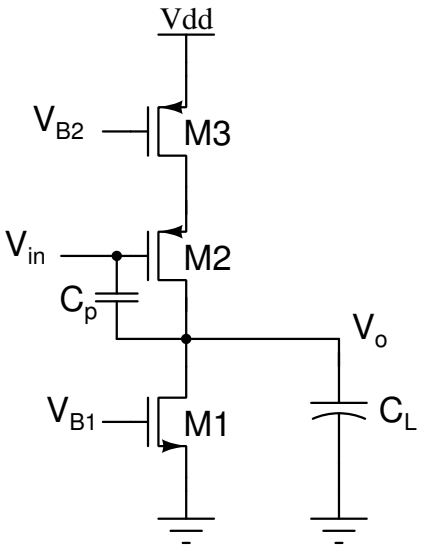
   Do not ignore Body effect, Channel length modulation. Both transistors have identical g_m and g_{ds}.



4.

   A. Draw the small signal model for the circuit below. (2)
   B. Derive expression for DC gain. (2)
   C. Derive an expression for transfer function (frequency response). (6)
   D. Show pole, zero plot. (2)
   E. Show Bode plot (Gain & Phase) (2)

   All transistors have same g_m and g_o. $g_m >> 2\ g_{ds}$. Ignore body effect and transistor capacitances.



5. Write an expression for intrinsic gain of a MOS transistor sized W/L. What happens to the gain when both W & L are scaled up while keeping current constant? (2)