EE 618 (ZELE)

CMOS ANALOG IC DESIGN MidTerm

19th Sep 2018 9:00PM – 11:00 PM

ACADEMIC HONESTY POLICY – IIT BOMBAY (http://www.iitb.ac.in/newacadhome/rules.jsp)

Copying in Examinations has serious consequences.

DO NOT

3.1 Communicate with other students during exams
3.2 Carry unauthorized material during exams
3.4 Make changes in valued answer books
3.5 Communicate with others during toilet breaks during exams

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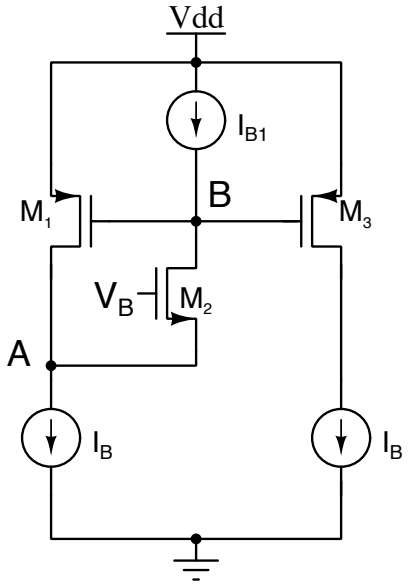
State your assumptions clearly if any.

1. Draw the transistor level schematic diagram for folded-cascode Operational Trans-conductance Amplifier (OTA) with PMOS input differential pair. Annotate inputs with correct polarities. Annotate bias voltages. Label the transistors. (3)

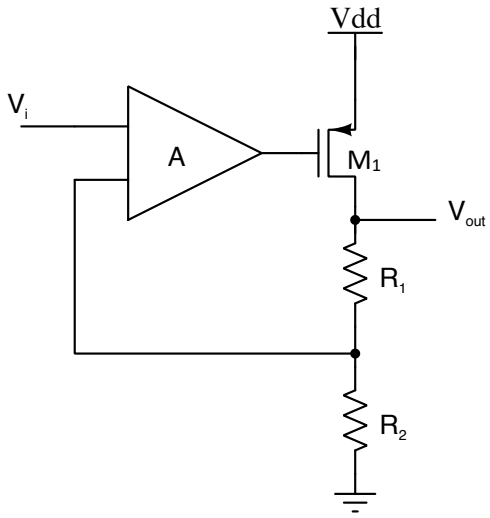
   Using single ideal current source, generate all the required bias voltages. (2)

2. Calculate the small-signal input impedance for the high performance current mirror at Node A (3 pts) and Node B (1 pt). (4)

   All NMOS have g_{mn}, r_{on}.
   All PMOS have g_{mp}, r_{op}.
   Ignore body effect.



3. For the circuit in figure below, assume opamp has finite gain A. Assume M_1 is in saturation with trans-conductance g_m and output resistance r_o.



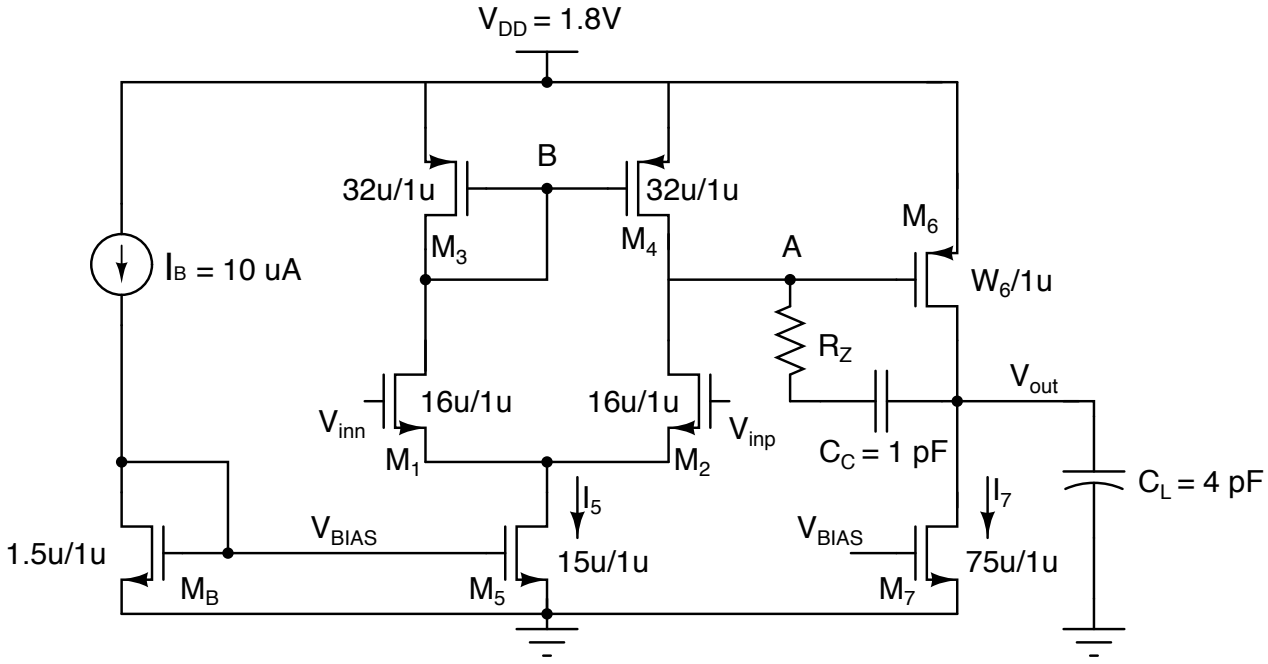
   a. Mark the Opamp polarity for Negative feedback operation (1)

   b. Find transfer function V_{out}/V_i. (2)

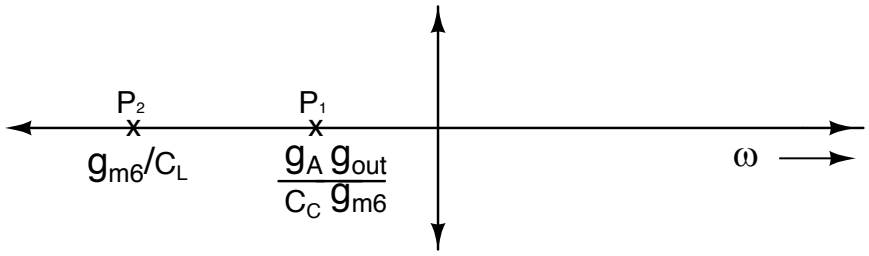
   c. Find the transfer function V_{out}/Vdd (Assume $V_i \rightarrow$ small signal ground). (2)

   d. What happens to transfer functions in (b) & (c), when A and $r_o \rightarrow$ infinity. (2)

4. For the OTA schematic shown on the next page, use the process parameters provided for 0.18 um CMOS technology.
   Calculate the following.
   a. I_5 (1)
   b. I_7 (1)
   c. Total power dissipation (1)
   d. Node voltage V_B (1)
   e. W_6 - Width of transistor M_6 to achieve zero systematic offset. (2)
   f. DC gain of the OTA (4)
   g. Input common mode range $V_{i,cmr}$ (high) (2)
   h. Input common mode range $V_{i,cmr}$ (low) (2)
   i. Derive the expression for zero location. (2)
   j. Given the pole locations (Dominant pole approximation) in the figure, calculate value of R_z to achieve the best phase margin. (2)
   k. The Unity Gain Frequency of the OTA. (2)
   l. Slew rate of the OTA (Assume slew rate is limited by input differential pair) (2)
   m. OTA input referred noise voltage V/$\sqrt{\text{Hz}}$. (Consider thermal noise only). (4)



Two Stage Operational Transconductance Amplifier



Pole Locations of the OTA

Process Parameters for 0.18 μm CMOS process.

t_{ox} = 4 nm; μ_n = 300 $cm^2/V.s$; μ_p = 70 $cm^2/V.s$; C_{ox} = 8.78 $fF/\mu m^2$;

$|V_{Tp}|$ = 0.4 V; V_{Tn} = 0.48 V; λ_p = 0.328 V^{-1}; λ_n = 0.48 V^{-1} [for L_{min} = 0.18 μm]