INDIAN INSTITUTE OF TECHNOLOGY, BOMBAY
ELECTRICAL ENGINEERING DEPARTMENT

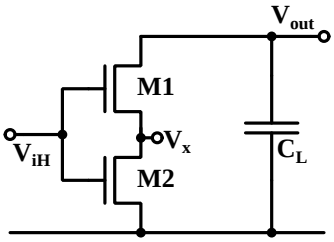
Mid Semester Examination

Saturday	EE 671: VLSI Design	Time: 1330-1530
15-09-18	Autumn Semester 2018	Marks: 25

For iterative solutions, all intermediate values must be reported.
Quantitative answers must be accurate at least to 0.1%.

Q–1 Consider a 2 input CMOS NAND gate acting as an inverter with both its inputs tied to a logic 'High' value. Since the inputs are 'High', the pMOS transistors are OFF and may be ignored for this problem. The two n channel transistors M1 and M2 have identical geometries and electrical parameters. We wish to analyse this circuit without approximating the behaviour of the transistors as equivalent resistors.

Assume that the load capacitor C_L is initially charged to $V_{DD} =$ 3.3V. Both inputs are tied to $V_{iH} = 3.0$V. Assume $V_{Tn} = 0.6$V. Dependence of V_{Tn} on the source voltage (bulk effect) is to be ignored. As the output discharges, V_{out} goes from V_{DD} towards 0 V. Use the simple MOS model with perfect saturation for MOS transistor currents.



a) In what modes (saturated or linear) are the two transistors for different values of V_{out} as it drops from V_{DD} to 0?

Soln. Q1a: Condition for saturation is $V_{ds} \geq V_{gs} - V_{Tn}$. For M1, this translates to $V_{out} - V_x \geq V_{iH} - V_x - V_{Tn}$. Canceling V_x from both sides, the condition becomes $V_{out} \geq V_{iH} - V_{Tn}$. Thus M1 is in saturation for $V_{out} \geq V_{iH} - V_{Tn}$ and is in linear mode for $V_{out} \leq V_{iH} - V_{Tn}$. The single transistor replacing M1 and M2 will also be in saturation for $V_{out} \geq V_{iH} - V_{Tn}$ and in linear mode for $V_{out} \leq V_{iH} - V_{Tn}$.

Since the input is 'High', both transistors are conducting.
Therefore V_{gs} for M1 is $> V_{Tn}$. This implies that the drain of M2 has lower voltage compared to its gate by $> V_{Tn}$. Therefore M2 is always in linear mode. – **[1]**

b) Derive expressions for the voltage at the source of M1 (V_x) in terms of V_{iH}, V_{Tn} and V_{out} for different combinations of modes of M1 and M2 which will occur during the discharge. Taking $V_{iH} = 3.0$V and $V_{Tn} = 0.6$V, tabulate values of V_x for:
$V_{out} =$ i) 3.3 V, ii) 3.0 V, iii) 2.4 V, iv) 1.8 V and v) 1.2 V.

Soln. Q1b: For $V_{out} \geq V_{iH} - V_{Tn}$, M1 is in saturation, while M2 is in linear mode. Since the two are in series, their currents must be equal. Therefore,

$$\frac{K_n}{2}(V_{iH} - V_x - V_{Tn})^2 = K_n\left((V_{iH} - V_{Tn})V_x - \frac{1}{2}V_x^2\right)$$

$$\text{This gives} \quad (V_{iH} - V_x - V_{Tn})^2 = 2\left((V_{iH} - V_{Tn})V_x - \frac{1}{2}V_x^2\right)$$

$$\text{Defining } V_1 \equiv V_{iH} - V_{Tn}, \text{ we get} \quad (V_1 - V_x)^2 = 2V_1V_x - V_x^2$$

$$\text{Therefore} \quad V_1^2 + V_x^2 - 2V_1V_x = 2V_1V_x - V_x^2 \quad \text{So,} \quad 2V_x^2 - 4V_1V_x + V_1^2 = 0$$

$$\text{This can be solved to give} \quad V_x = \frac{4V_1 \pm \sqrt{16V_1^2 - 8V_1^2}}{4} = V_1 \pm \sqrt{\frac{V_1^2}{2}}$$

Since V_x must be $< V_{iH} - V_{Tn}$, the negative sign should be chosen.

$$\text{So} \quad V_x = V_1\left(1 - \frac{1}{\sqrt{2}}\right) = \left(1 - \frac{1}{\sqrt{2}}\right)(V_{iH} - V_{Tn})$$

Thus the voltage V_x remains constant at $(1-1/\sqrt{2})(V_{iH} - V_{Tn})$ till V_{out} drops below $V_{iH} - V_{Tn}$.

For $V_{out} \leq V_{iH} - V_{Tn}$, both M1 and M2 are in linear mode. Since these are in series, their currents must be equal. This gives

$$K_n\left((V_{iH} - V_x - V_{Tn})(V_{out} - V_x) - \frac{1}{2}(V_{out} - V_x)^2\right) = K_n\left((V_{iH} - V_{Tn})V_x - \frac{1}{2}V_x^2\right)$$

$$\text{So} \quad (V_1 - V_x)(V_{out} - V_x) - \frac{1}{2}(V_{out} - V_x)^2 = V_1V_x - \frac{1}{2}V_x^2$$

$$\text{Or} \quad V_1V_{out} - V_xV_{out} - V_1V_x + V_x^2 - \frac{1}{2}(V_{out}^2 + V_x^2 - 2V_{out}V_x) = V_1V_x - \frac{1}{2}V_x^2$$

$$\text{This leads to} \quad V_x^2 - 2V_1V_x + V_1V_{out} - \frac{1}{2}V_{out}^2 = 0$$

We can solve this quadratic equation to give

$$V_x = \frac{2V_1 \pm \sqrt{4V_1^2 - 4(V_1V_{out} - \frac{1}{2}V_{out}^2)}}{2} = V_1 \pm \sqrt{V_1^2 - V_1V_{out} + \frac{1}{2}V_{out}^2)}$$

Again, since $V_x < V_{iH} - V_{Tn}$, the negative sign must be chosen.

$$\text{Then} \quad V_x = V_1 - \sqrt{V_1^2 - V_1V_{out} + \frac{1}{2}V_{out}^2}$$

$$\text{Or} \quad V_x = V_1 - \sqrt{V_1(V_1 - V_{out}) + \frac{1}{2}V_{out}^2}$$

It is interesting to evaluate this at $V_{out} = V_1 = V_{iH} - V_{Tn}$ when M1 is at the edge of saturation. We get

$$V_x = V_1\left(1 - \frac{1}{\sqrt{2}}\right)$$

This matches with the value we obtained in the saturation case, as indeed it should. In our case, $V_{iH} = 3.0$V, $V_{Tn} = 0.6$V, so $V_1 = 2.4$V. We can now compute and tabulate the values of V_x for all the given values of V_{out}, noticing that for $V_{out} \geq 2.4$V, M1 is saturated and V_x is constant at $(1 - 1/\sqrt{2})V_1 = 0.703$V.

V_{out}	3.3	3.0	2.4	1.8	1.2
V_x	0.703	0.703	0.703	0.651	0.503

– **[4]**

c) How much is the discharge current through the series connected transistors M1 and M2, when expressed as a fraction of the discharge current through a single nMOS transistor with identical dimensions replacing the series connected transistors M1 and M2, with the same input voltage V_{iH} applied to its gate? Evaluate this ratio for all combinations of operating modes of M1 and M2 which occur during discharge.

Soln. Q1c:

$$\text{When M1 is saturated,} \quad V_x = V_1\left(1 - \frac{1}{\sqrt{2}}\right)$$

The discharge current is the same as the current through M1, so

$$I_{ds} = \frac{K_n}{2}(V_1 - V_x)^2 = \frac{K_n}{2}\frac{V_1^2}{2}$$

The current through a single transistor would have been $\frac{K_n}{2}V_1^2$. So the current through M1 and M2 is half as much as that through a single transistor with identical geometry.

$$\text{When M1 is linear,} \quad V_x = V_1 - \sqrt{V_1(V_1 - V_{out}) + \frac{1}{2}V_{out}^2}$$

The discharge current through M1 and M2 is the same as the current through M2, given by $K_n(V_1V_x - 1/2V_x^2)$. The current through a single transistor would have been $K_n(V_1V_{out} - 1/2\,V_{out}^2)$. The quadratic equation for V_x was

$$V_x^2 - 2V_1V_x + V_1V_{out} - \frac{1}{2}V_{out}^2 = 0$$

$$\text{Therefore} \quad V_1V_x - \frac{1}{2}V_x^2 = \frac{1}{2}\left(V_1V_{out} - \frac{1}{2}V_{out}^2\right)$$

So, current through M1 and M2 is

$$I = K_n(V_1V_x - \frac{1}{2}V_x^2) = \frac{K_n}{2}\left(V_1V_{out} - \frac{1}{2}V_{out}^2\right)$$

Thus the current through the series connected transistors M1 and M2 is half of what a single transistor with identical geometry replacing them would have been.

This can be shown in another way: Let I be the current through the series connected transistors. Since the currents through the two transistors must be equal, the sum of these currents must equal $2I$.

$$2I = K_n\left((V_1 - V_x)(V_{out} - V_x) - \frac{1}{2}(V_{out} - V_x)^2\right) + K_n\left((V_1V_x - \frac{1}{2}V_x^2\right)$$

$$\text{Therefore} \quad \frac{2I}{K_n} = (V_1 - V_x)(V_{out} - V_x) - \frac{1}{2}(V_{out} - V_x)^2 + V_1V_x - \frac{1}{2}V_x^2$$

$$\text{So} \quad \frac{2I}{K_n} = V_1V_{out} - V_xV_{out} - V_xV_1 + V_x^2 - \frac{1}{2}(V_{out}^2 + V_x^2 - 2V_{out}V_x) + V_1V_x - \frac{1}{2}V_x^2$$

All terms involving V_x cancel and we are left with

$$\frac{2I}{K_n} = V_1V_{out} - \frac{1}{2}V_{out}^2$$

$$\text{Hence} \quad 2I = K_n\left(V_1V_{out} - \frac{1}{2}V_{out}^2\right)$$

The expression on the right is just the current through a single transistor with identical K_n and V_{Tn} and with V_{iH} applied to its gate.

Thus *for all output voltages*, the discharge current provided by M1 in series with M2 is half the current which would have been provided by a single transistor of identical geometry replacing them. – **[3]**

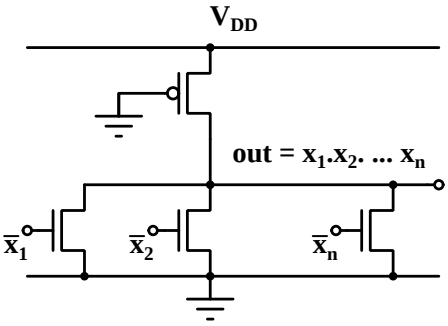
– **[Q1: 1+4+3=8 marks]**

Q–2 In a programmable logic array using pseudo NMOS style logic, we generate programmable products in one array and then add programmably selected products in the other.

a) NAND functions need to size the nMOS transistors depending on the number of inputs. This presents problems with programmability of the product array. How is this problem solved in PLAs?

Soln. Q2a: The number of inputs to be included in a product is variable in programmable logic. If we implement the product by using NAND gates, we shall have the problem that the nMOS transistor will have to be sized depending on the number of terms in the product – which is variable.

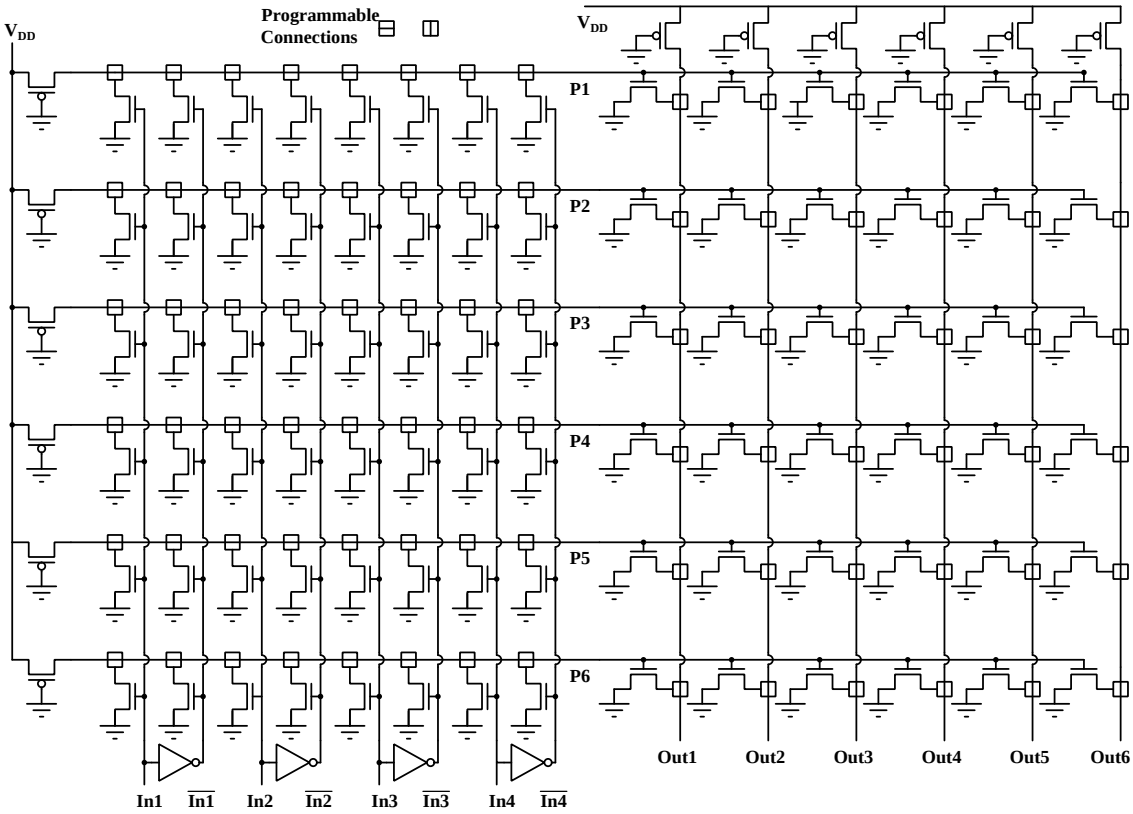
This problem is solved by implementing the product as the NOR of complemented inputs. The transistor size is independent of the number of inputs in a NOR gate, so we can include a variable number of (complemented) inputs without having to re-size the transistors.



– [**1**]

b) Show a transistor level circuit for a PLA implemented with pseudo NMOS logic with four primary inputs, six possible products and six outputs.

Soln. Q2b: The Product array will have 8 columns (for four inputs and their complements) and six rows for the six programmable products.
The Sum array will have six rows (from the six product inputs) and six columns for the six outputs. A circuit diagram is shown below:

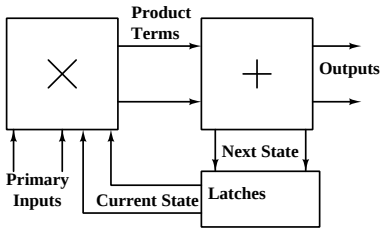


– [**1**]

c) Show how this configuration can be enhanced with latches to implement generic finite state machines.

Soln. Q2c: A finite state machine has a storage block (which encodes the current state) and two blocks of random logic – one to compute the next state from the current state and inputs, and the other to generate the outputs from the current state and inputs. Inputs to these two blocks is the same: current state information from the storage block and primary inputs to the fsm.

Since the PLA can generate arbitrary sums of products, the two random logic blocks can be easily implemented. Thus we only have to add latches for storage of current state and feed their outputs as additional inputs to the programmable logic array to implement any finite state machine. The PLA will generate the next state as well as outputs from latch outputs and primary inputs.

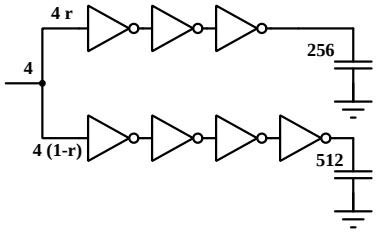


– **[1]**

– **[Q2: 1+1+1=3 marks]**

Q–3 We want to design a 3-4 fork with the total input capacitance (to be driven by the upstream driver) equal to 4 times the minimum inverter input capacitance.
Assume $\mathbf{p_{inv}} = \mathbf{2.0}, \gamma = \mathbf{2.2}$.

The input capacitance is divided in the ratio r:(1-r) for the 3 and 4 inverter branches of the fork respectively. The final load on the branch with 3 inverters is equivalent to 256 minimum inverters, while that on the 4 inverter branch is equivalent to 512 minimum inverters.



a) Evaluate the value of r such that the optimum delay in the two branches is equal, using Newton Raphson technique (starting with a guess value of r=0.5).

Soln. Q3a: For the upper branch, the input capacitance is $4r$, while the output capacitance is 256. Thus $H_1 = 256/4r = 64/r$. All g and b values are 1.

$$\text{Therefore,} \quad F_1 = 64/r, \text{ and correspondingly,} \quad \hat{f}_1 = \left(\frac{64}{r}\right)^{1/3} = 4r^{-1/3}$$

The delay through the upper arm of the fork is

$$D_1 = 3\hat{f}_1 + 3p_{inv} = 12r^{-1/3} + 3p_{inv}$$

For the lower branch, the input capacitance is $4(1-r)$, while the output capacitance is 512. Thus $H_2 = 512/4(1-r) = 128/(1-r)$. Since all g and b values are 1,

$$F_2 = \frac{128}{1-r}, \text{ and correspondingly,} \quad \hat{f}_2 = \left(\frac{128}{1-r}\right)^{1/4} = 3.3636(1-r)^{-1/4}$$

The delay through the lower arm of the fork is

$$D_2 = 4\hat{f}_2 + 4p_{inv} = 13.4543(1-r)^{-1/4} + 4p_{inv}$$

Condition for the two delays to be equal is: $13.4543(1-r)^{-1/4} + p_{inv} - 12r^{-1/3} = 0$

$$\text{Defining} \quad f(r) \equiv 13.4543(1-r)^{-1/4} + p_{inv} - 12r^{-1/3}$$

We seek the value of r which will make $f(r) = 0$. The derivative of $f(r)$ may be written as

$$f'(r) = -\frac{13.4543}{4}(1-r)^{-5/4}(-1) + \frac{12}{3}r^{-4/3} = 3.3636(1-r)^{-5/4} + 4r^{-4/3}$$

Taking the initial guess for r as 0.5, successive values for r can be tabulated as:

r	f(r)	f'(r)	next r
0.5	2.88095	18.0794	0.34065
0.34065	-0.251373	22.4743	0.351835
0.351835	-0.00333406	21.8878	0.351987
0.351987	-5.78369e-07	21.8803	0.351987
0.351987	-1.42109e-14	21.8803	0.351987

Thus, r = 0.352 will equalize delays. – **[3]**

b) Calculate the sizes of all transistors in the fork. Transistor widths are to be specified in units of the width of nMOS in the unit inverter.

Soln. Q3b:

$$\text{For the upper branch,} \quad \hat{f}_1 = \frac{4}{r^{1/3}} = \frac{4}{0.351987^{1/3}} = \frac{4}{0.70606} = 5.665232$$

All stages are inverters with $g = 1, b = 1$. Since $\hat{f} = gbh = 5.665232$, $h = 5.665232$ for all stages.

The first inverter should have an input capacitance of $4r = 1.408$
The next inverter should have an input capacitance of $1.408 \times h = 1.408 \times 5.665232 = 7.976$.
Input capacitance for the final inverter will be $7.976 \times h = 7.976 \times 5.665232 = 45.188$.
The final inverter can drive a load of $45.188 \times 5.665232 = 256$ as required.

Alternatively, we could have started with the output. As before:
$\hat{f} = gbh = 5.665232, g = 1, b = 1$, so $h = 5.665232$ for all stages. Final $C_{out} = 256$.
For the last inverter, $C_{in} = 256/5.665232 = 45.188$. This becomes the output capacitance of the second inverter. Since $h = 5.665232$ for all stages, $C_{in} = 45.188/5.665232 = 7.976$. for the second inverter. Finally, since the output capacitance of the first inverter is 7.976, its input capacitance is $7.976/5.665232 = 1.408$. This agrees with the value $4r$ as required.

Either way, we get the input capacitances of $1.408, 7.976$ and 45.188 respectively, for the three inverters.

Transistor geometries for the upper branch
The unit of width is the n channel transistor width in the minimal inverter. Thus, input capacitance of 1 corresponds to n channel width of 1 and p channel width of γ. Therefore an inverter stage with input capacitance of C_{in} will have n channel transistor width of C_{in} and p channel transistor width of $\gamma \times C_{in}$. Thus we can tabulate the transistor geometries as

First Inverter		Second Inverter		Third Inverter	
$C_{in} = 1.408$		$C_{in} = 7.976$		$C_{in} = 45.188$	
n width	p width	n width	p width	n width	p width
1.408	3.10	7.976	17.548	45.188	99.413

For the lower branch, $\hat{f}_2 = 3.3636/(1-r)^{1/4} = 3.749$.
Again all stages are inverters with $g = 1, b = 1$. Therefore, for all stages, $h = 3.749$.
Input capacitance of the first inverter is $4 \times (1-r) = 2.592$
Input capacitance of the following three inverters should be $2.592 \times 3.749 = 9.717$, $9.717 \times 3.749 = 36.43$ and $36.43 \times 3.749 = 136.57$.
The final inverter can drive a capacitance of $136.57 \times 3.749 = 512$ as expected.

We could have started with the output capacitance of 512 and successively divided by $h = 3.749$ to get input capacitances of the four inverters.

Given these input capacitance values, the n channel widths are equal to the capacitance, while the p channel widths are 2.2 times this value. Thus we can tabulate the transistor geometries for the lower branch as

First Inverter		Second Inverter		Third Inverter		Fourth Inverter	
$C_{in} = 2.592$		$C_{in} = 9.717$		$C_{in} = 36.43$		$C_{in} = 136.57$	
n width	p width	n width	p width	n width	p width	n width	p width
2.592	5.703	9.717	21.378	36.43	80.146	136.57	300.46

– **[4]**

c) Compute delays for both the branches of the fork.

Soln. Q3c: Delay for the upper branch is $3\hat{f}_1 + 3p_{inv} = 3 \times 5.665 + 6 = 22.995$.
Delay for the lower branch is $4\hat{f}_2 + 4p_{inv} = 4 \times 3.749 + 8 = 22.995$. – **[1]**

d) Without changing inverter sizes, assume that the actual load capacitors in both the branches are higher by 10%. Now what are the delays and how much is the difference in delays of the two branches?

Soln. Q3d: Since inverter sizes remain the same, all inverters except the final one see the same load. Therefore change in the final load capacitor will change the delay of the last stage only. The remaining delays will remain the same. therefore delays in the two branches are:

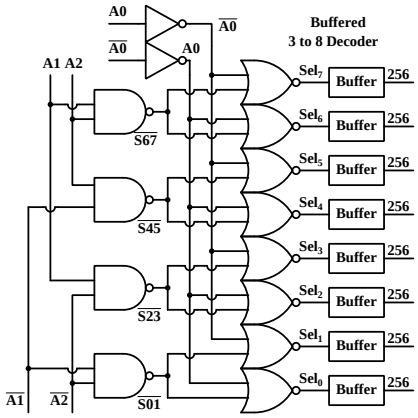
$$\begin{aligned} D_1 &= 2\hat{f}_1 + 1.1 \times \hat{f}_1 + 3p_{inv} = 3.1 \times 5.665 + 6 = 17.562 + 6 = 23.562 \\ D_2 &= 3\hat{f}_2 + 1.1 \times \hat{f}_2 + 4p_{inv} = 4.1 \times 3.749 + 8 = 17.562 + 6 = 23.371 \end{aligned}$$

The difference in delays is therefore $23.562 - 23.371 = 0.192$. (The upper branch is slower by this amount). – **[1]**

– **[Q3: 3+4+1+1=9 marks]**

Q–4 We want to design a 3 bit decoder where the decoder outputs have to be buffered to drive a load equivalent to 256 minimal inverters. Assume $\mathbf{p_{inv}} = \mathbf{2.0}, \gamma = \mathbf{2.2}$.

Assume that the 3 bits to be decoded and their complemented values are available as inputs and can drive loads equivalent to 4 minimal inverters. Decoding is done using a 2 step NAND-NOR circuit as shown. The decoded outputs Sel_i are buffered using inverters to drive the load. The number of inverters in the buffer is to be chosen to minimise the delay of the path involving NAND-NOR-Buffer. The number of inverters in the buffer can be even or odd, since true or complemented values of select outputs are equally acceptable.



a) Find the optimum value of ρ using Newton Raphson technique, starting with a guess value of $\rho = 4$.

Soln. Q4a: We define $f(\rho) \equiv \rho(1 - \ln \rho) + p_{inv}$.
Then the optimum value of ρ is the one which makes $f(\rho) = 0$.
We can solve this non-linear equation using Newton Raphson iterations. Derivative of $f(\rho)$ is given by

$$f'(\rho) = 1 - \ln \rho - \rho \frac{1}{\rho} = -ln(\rho)$$

Therefore given a guess value g for ρ, is the next refined value of g is given by

$$g_{next} = g - \frac{f(g)}{f'(g)} = g + \frac{g - g \ln g + p_{inv}}{\ln g} = \frac{g + p_{inv}}{\ln g}$$

Starting with $g = 4$, we get successive values for ρ as
4.0, 4.3281, 4.3191, 4.3191.
Thus the optimum stage ratio is 4.3191. – **[1]**

b) Find the optimum number of stages in the path through NAND-NOR and Buffer. How many inverters should be used in the buffer?

Soln. Q4b: Since each input drives two NAND gates, each NAND gate should have an input capacitance of 2. Thus H = 256/2 = 128.
The output of each NAND drives two NOR gates. Therefore $b = 2$ for the NAND stage, while all other stages have $b = 1$. Therefore B = 2.
g for the NAND gates is $(2 + \gamma)/(1 + \gamma) = 4.2/3.2 = 1.3125$.
g for NOR gates is $(1 + 2\gamma)/((1 + \gamma) = 5.4/3.2 = 1.6875$.
Therefore G for the path is $1.3125 \times 1.6875 \times 1 \times 1 = 2.214844$.
Thus the path effort $F = GBH = 2.21488 \times 2 \times 128 = 567$.
The optimum number of stages for this path effort is

$$N = \frac{\ln F}{\ln \rho} = \frac{6.34036}{1.46305} = 4.333667$$

This suggests a total of 4 or 5 stages. For 4 stages, $\hat{f} = 567^{1/4} = 4.87973$ and the delay is $4 \times 4.87973 + p_{NAND} + p_{NOR} + 2p_{inv}$.
With $p_{inv} = 2$, this is $23.5189 + p_{NAND} + p_{NOR}$.

For 5 stages, $\hat{f} = 567^{1/5} = 3.55399$. This gives a delay of $5 \times 3.55399 + 3p_{inv} + p_{NAND} + p_{NOR}$. With $p_{inv} = 2$, this is $23.76997 + p_{NAND} + p_{NOR}$.

Thus there is slightly higher delay for a 5 stage implementation. Not only is the 4 stage decoder somewhat faster, it is smaller and is likely to consume less power.

Hence we choose a 4 stage design. Two of these are the NAND and NOR gates, so we should buffer Sel_i outputs with 2 inverters. – **[1]**

c) Find the transistor sizes for NAND, NOR and all the inverters in the buffer such that the path delay is minimum.

Soln. Q4c: The path to be optimized has four stages: NAND, NOR, Inverter1 and Inverter2. $F = 567$ and correspondingly $\hat{f} = 567^{1/4} = 4.87973$.

Parameter	NAND	NOR	Inv.1	Inv.2
$\hat{f}$	4.87973			
g	$4.2/3.2 = 1.3125$	$5.2/3.2 = 1.6875$	1	1
b	2	1	1	1
$h = \hat{f}/gb$	1.858945	2.8917	4.87973	4.87973
C_{in}	2	3.718	10.751	52.462
$C_{out} = hC_{in}$	3.718	10.751	52.462	256
W_n	3.048	2.203	10.751	52.462
W_p	3.352	9.694	23.652	115.42
$W_n + W_p$	6.4	11.897	34.403	167.882
$(W_n + W_p)/C_{in}$	3.2	3.2	3.2	3.2

1. **NAND stage:** $g = 4.2/3.2 = 1.3125, b = 2, \hat{f} = gbh = 4.87973$.
   So $h = 4.87973/(2 \times 1.3125) = 1.858945$.
   C_{in} for NAND is 2, Hence $C_{out} = C_{in} \times h = 2 \times 1.858945 = 3.718$.
   A NAND gate with n width of 2 and p width of $\gamma(= 2.2)$ will have
   $C_{in} = 4.2/3.2 = 1.3125$ in units of minimal inverter capacitance.
   Thus, $C_{in} = 1.3125$ corresponds to nMOS width of 2 and pMOS width of 2.2.
   Since actual C_{in} for NAND is 2, the nMOS width should be $2 \times 2/1.3125 = 3.048$, and pMOS width should be $2 \times 2.2/1.3125 = 3.352$.
2. **NOR stage:** $g = 1.6875, b = 1, \hat{f} = gbh = 4.87973$.
   So $h = 4.87973/(1 \times 1.6875) = 2.8917$
   C_{in} for NOR C_{out} for NAND $= 3.718$.
   Hence $C_{out} = C_{in} \times h = 3.718 \times 2.8917 = 10.751$.
   A NOR gate with n width of 1 and p width of $2\gamma = 4.4$ has $C_{in} = 5.4/3.2$ in units of inverter capacitance. Thus, $C_{in} = 1.6875$ corresponds to nMOS width of 1 and pMOS width of $2\gamma = 4.4$. Since actual $C_{in} = 3.718$ for the NOR gate, nMOS width should be $3.718/1.6875 = 2.203$. and pMOS width should be $4.4 \times 3.718/1.6875 = 9.694$.
3. **First inverter** $g = 1, b = 1, \hat{f} = gbh = 4.87973$. So $h = 4.87973$
   $C_{in} = 10.751$. $C_{out} = C_{in} \times h = 10.751 \times 4.87973 = 52.462$.
   nMOS width for the first inverter should be 10.751,
   while the pMOS width should be $2.2 \times 10.751 = 23.652$.
4. **Second inverter** $g = 1, b = 1, \hat{f} = gbh = 4.87973$. So $h = 4.87973$
   $C_{in} = 52.462$, $C_{out} = C_{in} \times h = 52.462 \times 4.87973 = 256$. This is as desired.
   For $C_{in} = 52.462$, nMOS width should be 52.462 and pMOS width should be $2.2 \times 52.462 = 115.42$

– **[3]**

– **[Q4: 1+1+3=5 marks]**