Effect of PROCESS variation, Temp & Voltage varⁿ. on filter response.

Absolute Value of R ± 20%.

of C ± 15%

Gm ± 40%.

Filter Corner freq ± 50%. easily over PVT

However, ~~&~~ using layout matching techniques.

R mismatch 0.1% ; Cap mismatch 0.1%

Gm mismatches < 0.5%. Can be achieved.

→ Filter Shape is preserved. – Corner freq $\propto \frac{1}{RC}$ changes over PVT.

Filter Tuning over PVT → make sure $\frac{1}{RC}$ or $\frac{g_m}{C}$ is trimmed to get desired f_{corner}.

1. Digital programing
2. Automatic Tuning on-chip.

Master Slave .

Haideh Khorramabadi paper — 1. Use phase difference @ o/p of filter ~~to~~ & compare to crystal clock. reference

K.S. Tan paper — 2 Create VCO using integrators. & then compare oscillation freq. to Reference.

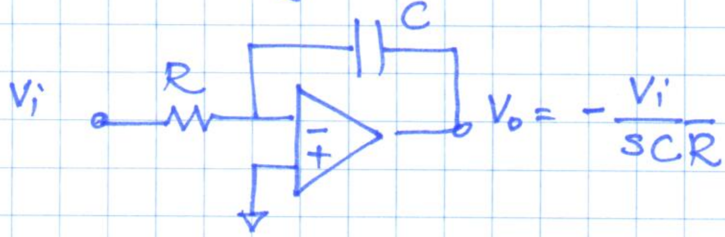
3 DSP based filter calibration

└ used in most radios we use today.

Switched-Capacitor Circuits – Introduction

Motivation:

RC integrator used in CT. filters



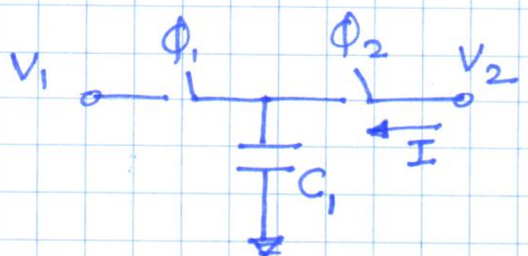
$R \rightarrow \pm 20\%$

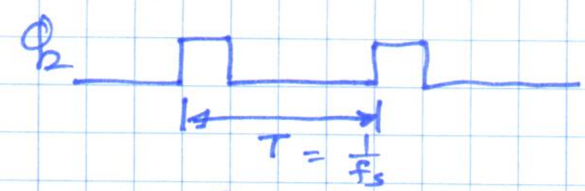
$C \rightarrow \pm 10\text{-}15\%$

$RC \rightarrow \pm 35\%$ variations

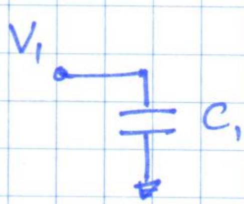
CT Filter designed using various methods discussed in Lecture 22 will result in f_{3dB} (corner frequency) variation upto $\pm 50\%$. $\rightarrow$ Require Tuning etc.

Consider switched-capacitor circuit below:



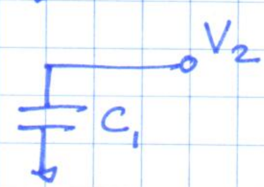


During ϕ_1



$Q_1 = C_1 V_1$

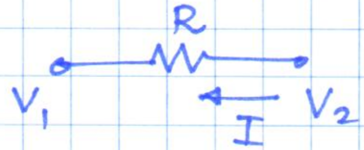
During ϕ_2



$Q_2 = C_1 V_2$

Current flowing from V_2 to V_1 $= \frac{\Delta Q}{\Delta t}$

$$I = \frac{\Delta Q}{T} = \frac{C_1(V_2 - V_1)}{T} = f_s C_1 (V_2 - V_1)$$

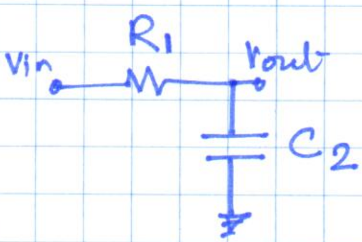
Compare 

$$I = \frac{1}{R}(V_2 - V_1)$$

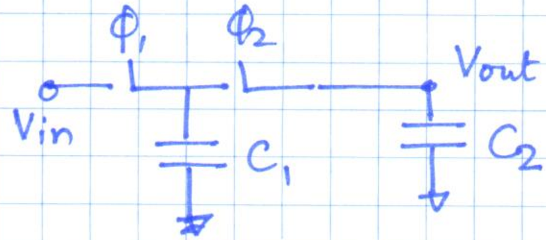
Equivalent resistor $R = \frac{T}{C_1} = \frac{1}{f_s C_1}$

2 → Switched-Capacitor Resistor Implementation.

FIRST ORDER Low Pass filter



Switched Cap →



$$\omega_p = \frac{1}{R_1 C_2} = \frac{f_s C_1}{C_2} = f_s\left(\frac{C_1}{C_2}\right)$$

Sampling Clock generally derived from Crystal Reference ~5 ppm accuracy

Capacitor ratios Proper layout Techniq. 0.1% matching possible.

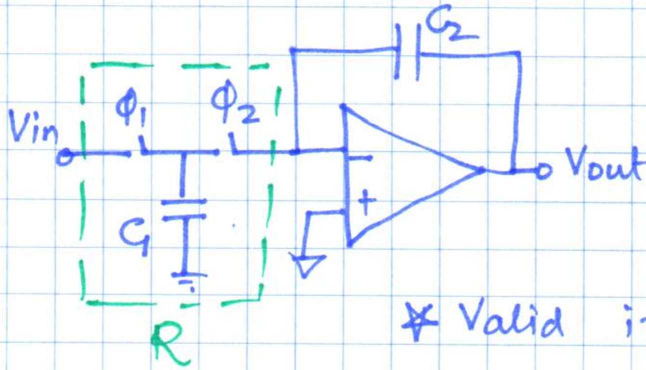
Very accurate frequency Response over PVT.

Ref:

Analog Sample-Data Filters – David. Fried,

JSSC – Aug 1972.

Switched. Cap. Integrator



$$\frac{V_{out}}{V_i} \simeq -\frac{1}{sRC_2} = \frac{-f_s\left(\frac{C_1}{C_2}\right)}{s}$$

* Valid if $f_s \gg$ frequency of interest
example UGF of Integ.

<u>Rule of Thumb</u> at least factor of <u>10</u>

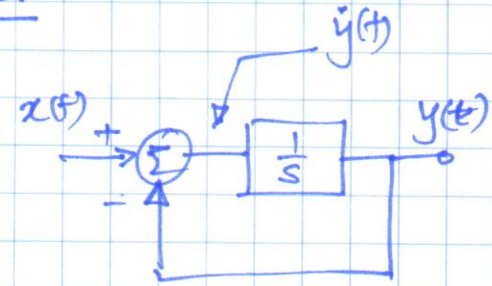
<u>Lets get into details</u> ∴ <u>Exact Analysis</u>

<u>Z-domain Refresher</u>

<u>Continuous-Time</u>

Start from differential equation

eg: $\dot{y}(t) = x(t) - y(t)$



Laplace Transform

$$sY(s) = X(s) - Y(s)$$

$$H(s) = \frac{Y(s)}{X(s)} = \frac{1}{s+1}$$

$\boxed{s = j\omega}$ $\quad H(j\omega) = \frac{1}{j\omega+1}$ plot → $|H(j\omega)|$
→ phase $H(j\omega)$

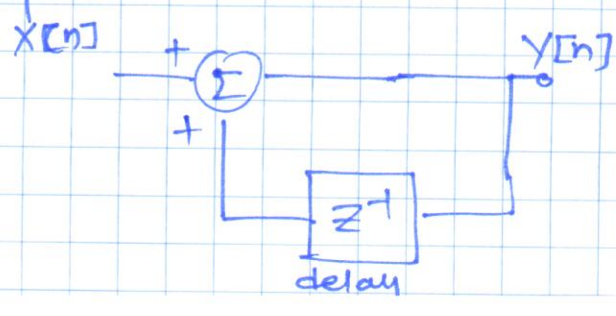
<u>Discrete-Time Analysis</u> → assumption Nyquist sampling criteria

Processing signal at discrete-timepoints

Start from difference equations

eg:

$Y[n] = X[n] + Y[n-1]$



Delay operator z^{-1}

$Y[z] = X[z] + z^{-1} Y[z]$

$H(z) = \frac{Y[z]}{X[z]} = \frac{1}{1 - z^{-1}}$

$\frac{1}{T}$ sampling frequency

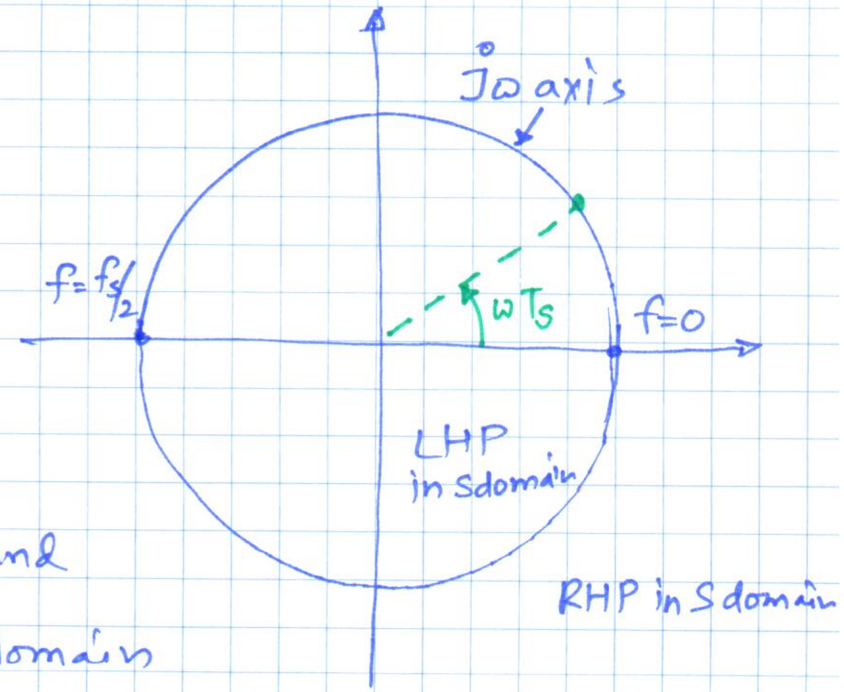
$Z = e^{sT} = e^{j\omega T}$
$= \cos(\omega T_s) + j\sin(\omega T_s)$

→ plot $H(z)$ is mag & phase response.

Z-transform operator.

$nT_s \rightarrow 1$
$(n-1)T_s \rightarrow z^{-1}$
$(n-\frac{1}{2})T_s \rightarrow z^{-1/2}$
$(n+1)T_s \rightarrow z^{+1}$.

$Z = e^{sT_s}$



S=jω axis is warped/wrapped around unit circle in Z domain

$f=0 \quad z=1$
$f = f_s/2 \quad z=-1$

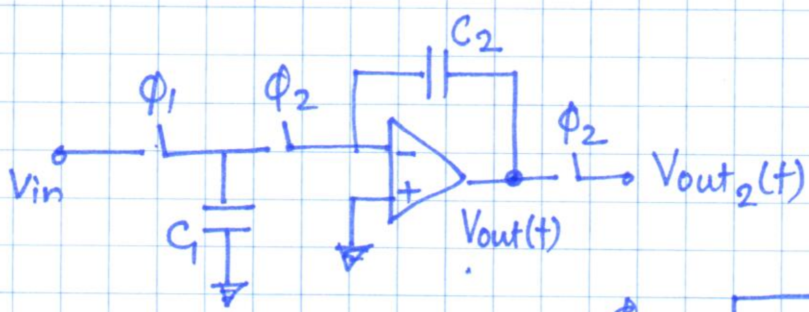
After $f = f_s/2$, frequency response repeats.

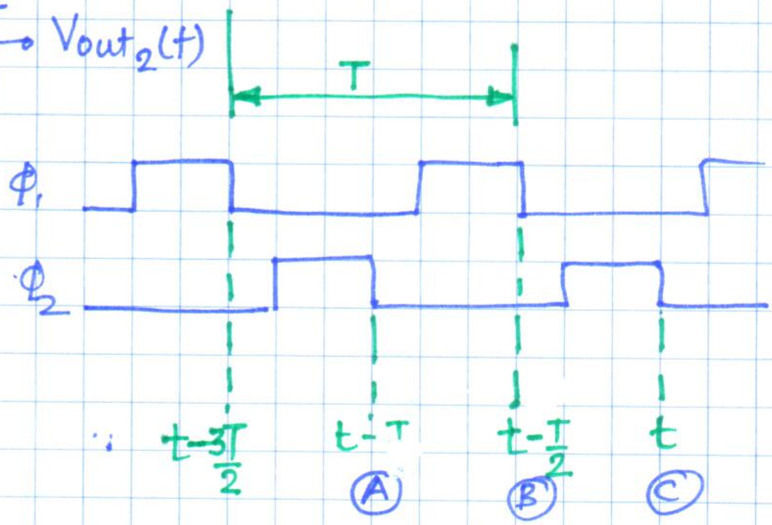
→ Note s-domain integrator → pole @ DC

Z-domain → pole @ $z=1$

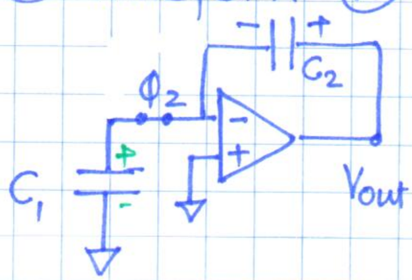
BACK TO SWITCHED-CAP CIRCUITS

Key concept : Charge Conservation





@ Timepoint A



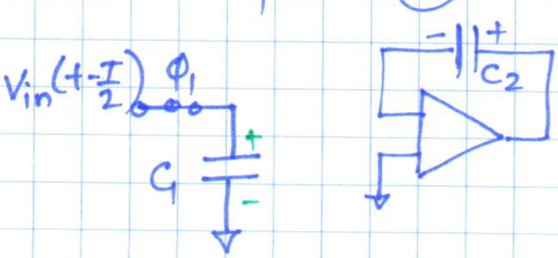
No charge on C_1 (both sides @ ac virtual ground)

$Q_{C_{1+}} = 0$

Charge on -ve plate of C_2

$Q_{C_{2-}} = -C_2 V_{out}(t-T)$

@ Timepoint B



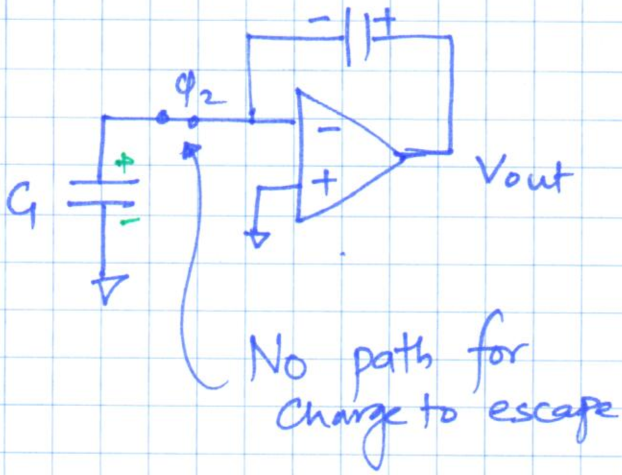
Charge on +ve plate of C_1

$Q_{C_{1+}} = C_1 V_{in}(t-\frac{T}{2})$

Charge on -ve plate of C_2

$Q_{C_{2-}} = -C_2 V_{out}(t-T)$

@ Timepoint (C) — charge redistribution happens.



$Q_{C_1+} = 0$

$Q_{C_2-} = -C_2 V_{out}(t)$

→ opamp - zero i/p current
-ve feedback makes sure
-ve i/p is driven to virtual gnd.

Charge Conserved from (B) to (C)

$$\underbrace{Q_{C_1+} + Q_{C_2-}}_{B} = \underbrace{Q_{C_1+} + Q_{C_2-}}_{C}$$

$$C_1 V_{in}\left(t-\frac{T}{2}\right) - C_2 V_{out}(t-T) = 0 - C_2 V_{out}(t)$$

$$V_{out}(t) = V_{out}(t-T) - \frac{C_1}{C_2} V_{in}\left(t-\frac{T}{2}\right)$$

If we sample o/p during ϕ_2, then

$$V_{out_2}(t) = V_{out_2}(t-T) - \frac{C_1}{C_2} V_{in}\left(t-\frac{T}{2}\right)$$

Z-transform

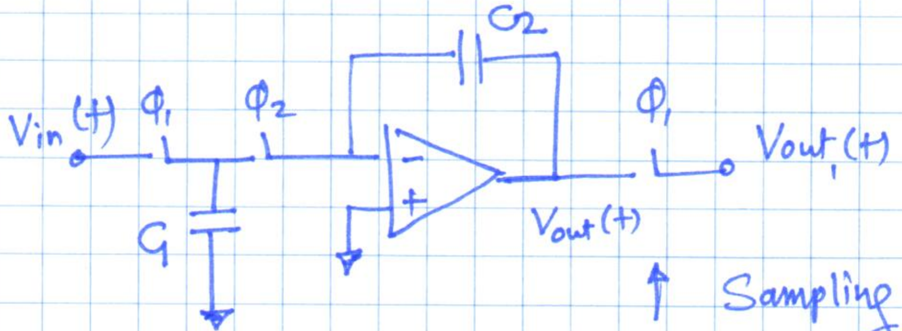
$$V_{out_2}(z) = z^{-1} V_{out_2}(z) - \frac{C_1}{C_2} V_{in}(z) \cdot z^{-1/2}$$

$$V_{out_2}(z) = \frac{-\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1 - z^{-1}} V_{in}(z)$$

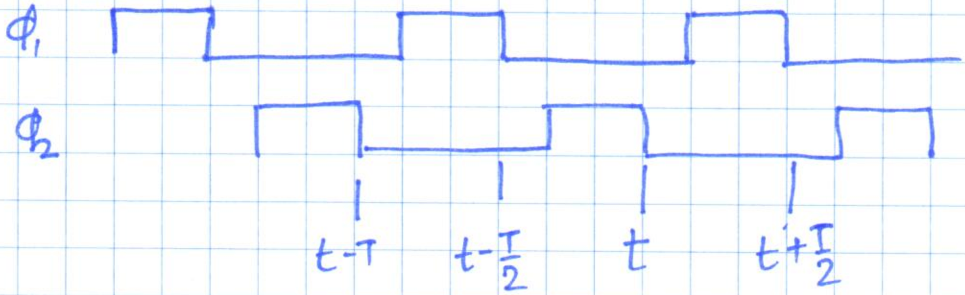
half delay from V_{in} to V_{out}

inverting config

pole @ $z=1$ ⇒ S domain pole @ DC integrator $\frac{1}{s}$



↑ Sampling o/p in phase 1. ϕ_1



During ϕ_2 Vout(t) changes. — Then we observe (Sample) o/p in ϕ_1 ($\frac{T}{2}$ later). → $z^{-1/2}$ delay later

$$V_{out_1}\left(t + \frac{T}{2}\right) = V_{out_2}(t)$$

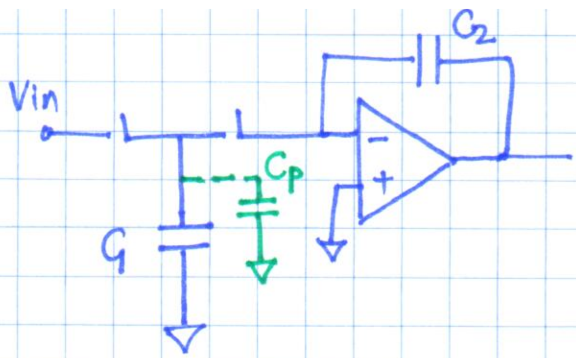
$$z^{+1/2} V_{out_1}(z) = V_{out_2}(z)$$

$$V_{out_1}(z) = z^{-1/2} V_{out_2}(z)$$

Full delay

$$V_{out_1}(z) = \frac{-\left(\frac{C_1}{C_2}\right) z^{-1}}{1 - z^{-1}} V_{in}(z)$$

Transfer Function depends on when you Sample the o/p. — Time Variant Discrete Time circuits



Cp – parasitic @ top plate node of C_1
→ due to routing
→ switches
→ parasitics of C_1

→ can't be avoided.

All other parasitics - don't affect integration operation.

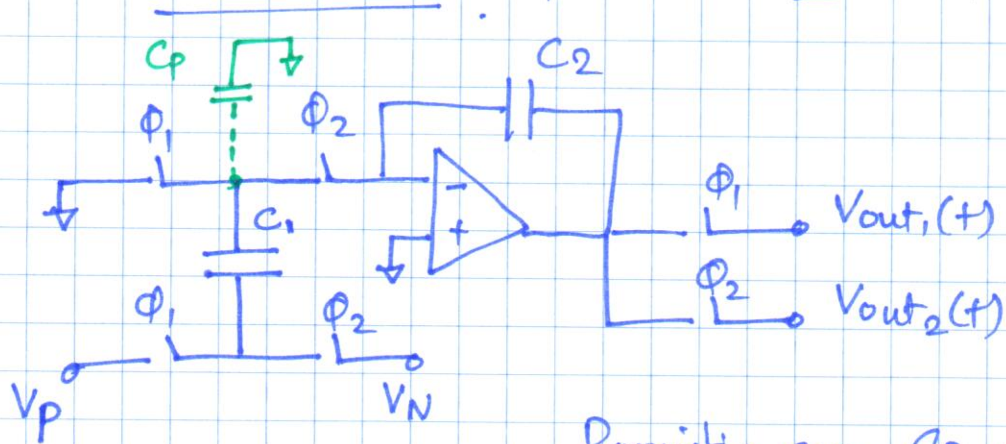
Impact of parasitics

$$V_{out,1}(z) = -\frac{\left(\frac{C_1 + C_p}{C_2}\right) z^{-1}}{1 - z^{-1}} V_{in}(z)$$

Advantage of $\left(\frac{C_1}{C_2}\right) \Rightarrow 0.1\%$ matching accuracy is lost.

C_p can be as high as 10% of C_1. Also, will not match.

→ Innovation. Parasitic Insensitive SC integrator



Parasitic cap Cp, always @ virtual gnd node.

→ Doesn't contribute to charge conservation process.