Multicore Architectures:

Interconnect Network

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EE-739: Processor Design

Lecture 16 (13 March 2015) CADSL

Switching/Flow Control Overview

- Topology: determines connectivity of network
- Routing: determines paths through network
- Flow Control: determine allocation of resources to messages as they traverse network

Routing Summary

- Latency paramount concern
  - Minimal routing most common for NoC
  - Non-minimal can avoid congestion and deliver low latency
- To date: NoC research favors DOR for simplicity and deadlock freedom
  - On-chip networks often lightly loaded
- Only covered unicast routing
  - Recent work on extending on-chip routing to support multicast

Switching/Flow Control Overview

- Topology: determines connectivity of network
- Routing: determines paths through network
- Flow Control: determine allocation of resources to messages as they traverse network
  - Buffers and links
  - Significant impact on throughput and latency of network

Switching

- Different flow control techniques based on granularity
- Circuit-switching: operates at the granularity of messages
- Packet-based: allocation made to whole packets
- Flit-based: allocation made on a flit-by-flit basis

Deadlock

- Using flow control to guarantee deadlock freedom give more flexible routing
- Escape Virtual Channels
  - If routing algorithm is not deadlock free
  - VCs can break resource cycle
  - Place restriction on VC allocation or require one VC to be DOR

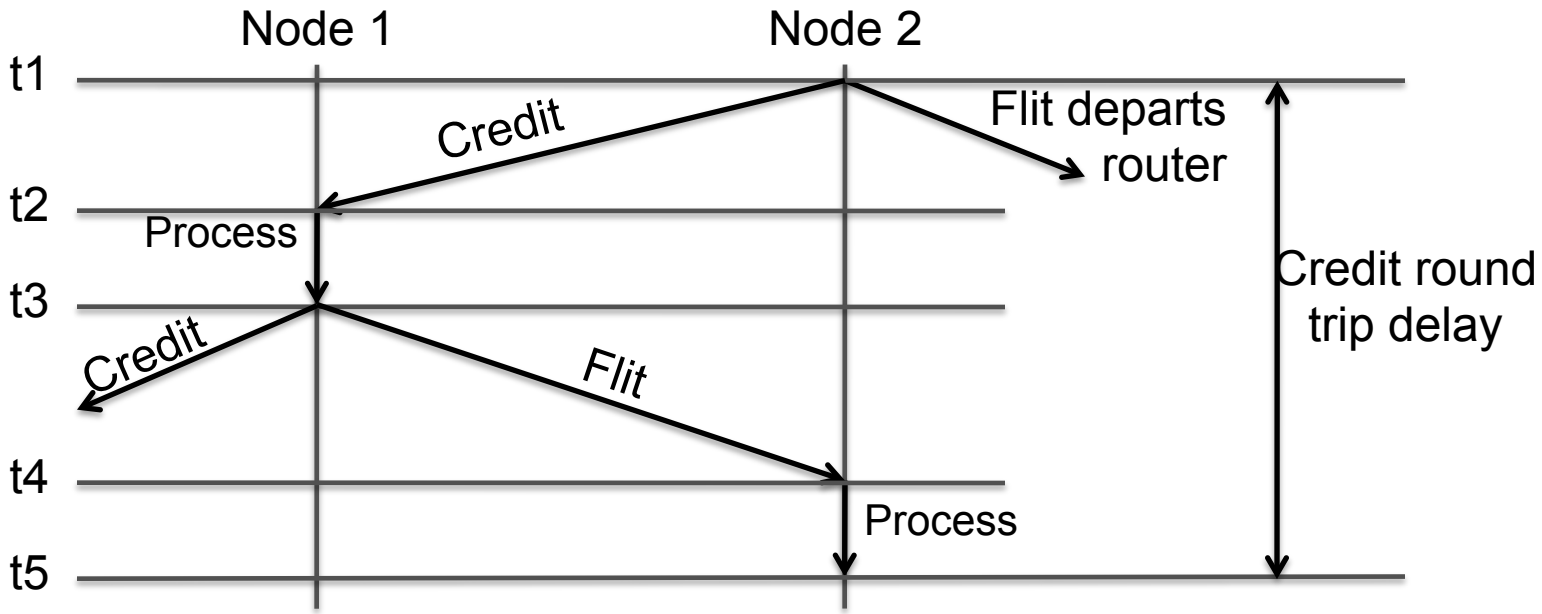
Buffer Backpressure

- Need mechanism to prevent buffer overflow
  - Avoid dropping packets
  - Upstream nodes need to know buffer availability at downstream routers
- Significant impact on throughput achieved by flow control
- Credits
- On-off

Credit-Based Flow Control

- Upstream router stores credit counts for each downstream VC
- Upstream router
  - When flit forwarded
    - Decrement credit count
  - Count == 0, buffer full, stop sending
- Downstream router
  - When flit forwarded and buffer freed
    - Send credit to upstream router
    - Upstream increments credit count

Credit Timeline

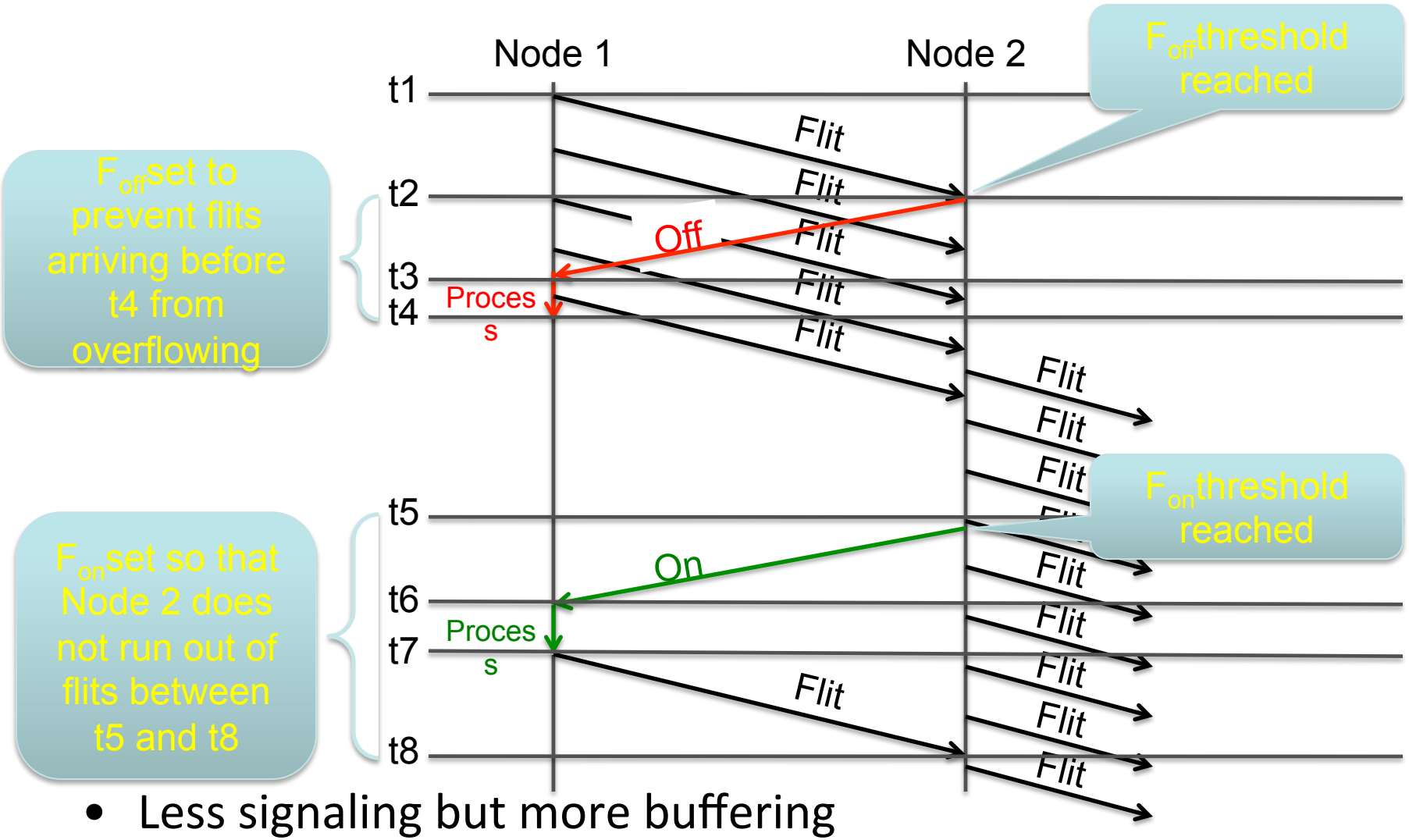


- Round-trip credit delay:
  - Time between when buffer empties and when next flit can be processed from that buffer entry
  - If only single entry buffer, would result in significant throughput degradation
  - Important to size buffers to tolerate credit turn-around

On-Off Flow Control

- Credit: requires upstream signaling for every flit
- On-off: decreases upstream signaling
- Off signal
  - Sent when number of free buffers falls below threshold F_{off}
- On signal
  - Send when number of free buffers rises above threshold F_{on}

On-Off Timeline



- Less signaling but more buffering
  - On-chip buffers more expensive than wires

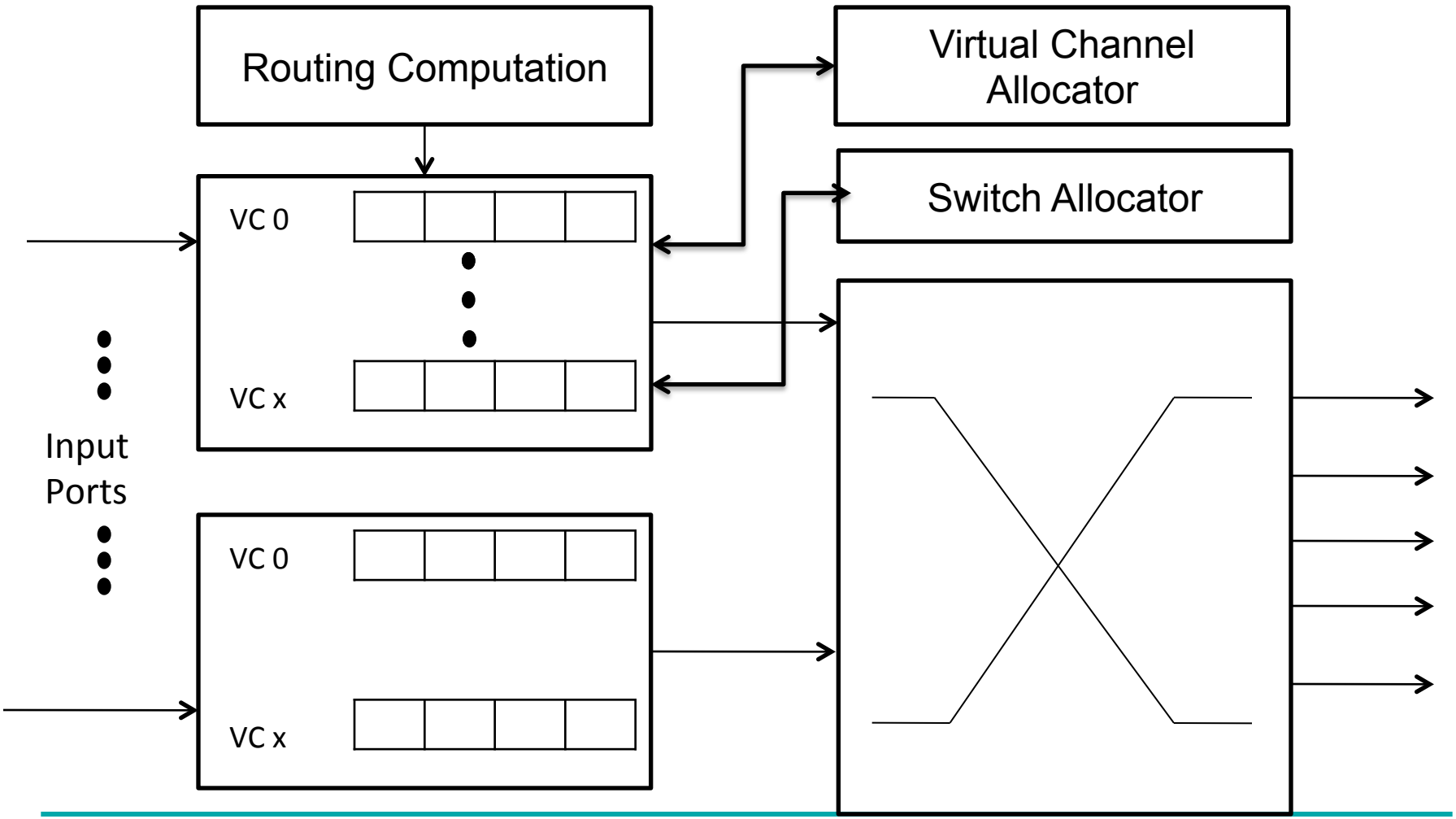
Flow Control Summary

- On-chip networks require techniques with lower buffering requirements
  - Wormhole or Virtual Channel flow control
- Dropping packets unacceptable in on-chip environment
  - Requires buffer backpressure mechanism
- Complexity of flow control impacts router microarchitecture (next)

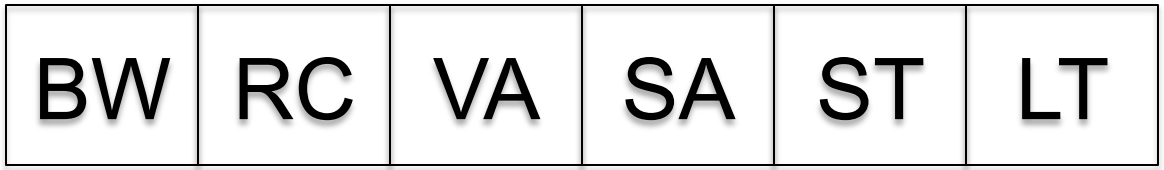
Router Microarchitecture Overview

- Consist of buffers, switches, functional units, and control logic to implement routing algorithm and flow control
- Focus on microarchitecture of Virtual Channel router
- Router is pipelined to reduce cycle time

Virtual Channel Router

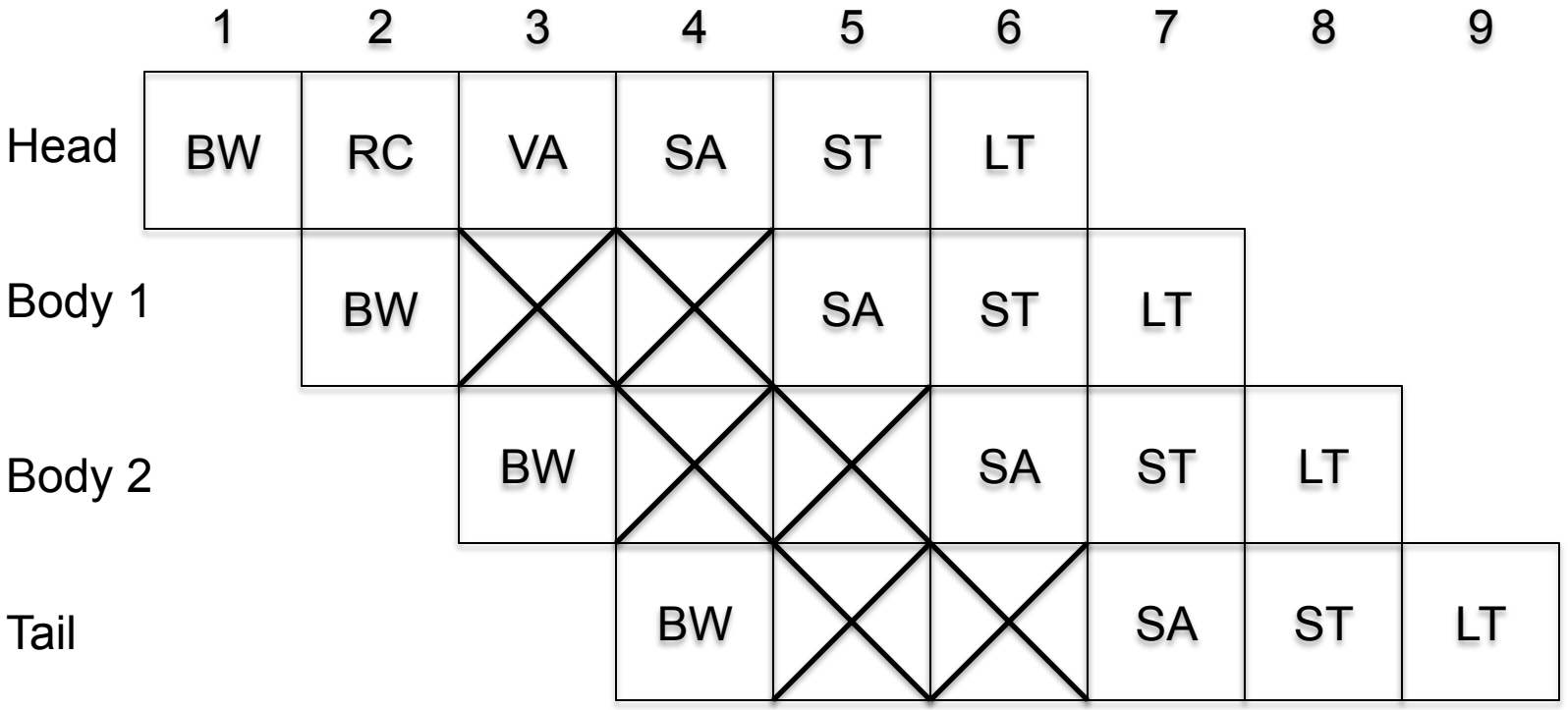


Baseline Router Pipeline



- Canonical 5-stage (+link) pipeline
  - BW: Buffer Write
  - RC: Routing computation
  - VA: Virtual Channel Allocation
  - SA: Switch Allocation
  - ST: Switch Traversal
  - LT: Link Traversal

Baseline Router Pipeline



- Routing computation performed once per packet
- Virtual channel allocated once per packet
- body and tail flits inherit this info from head flit

Router Pipeline Optimizations

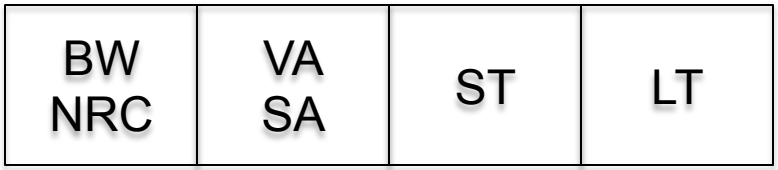
- Baseline (no load) delay

$$= (5 cycles + link delay) \times hops + t_{serialization}$$

- Ideally, only pay link delay
- Techniques to reduce pipeline stages
  - Lookahead routing: At current router perform routing computation for next router
    - Overlap with BW

Router Pipeline Optimizations

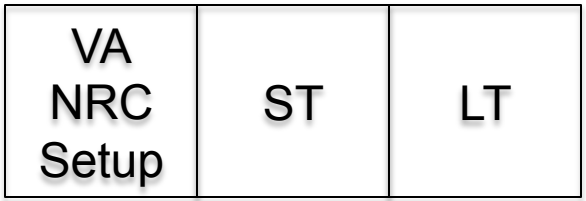
- Speculation
  - Assume that Virtual Channel Allocation stage will be successful
    - Valid under low to moderate loads
  - Entire VA and SA in parallel



  - If VA unsuccessful (no virtual channel returned)
    - Must repeat VA/SA in next cycle
  - Prioritize non-speculative requests

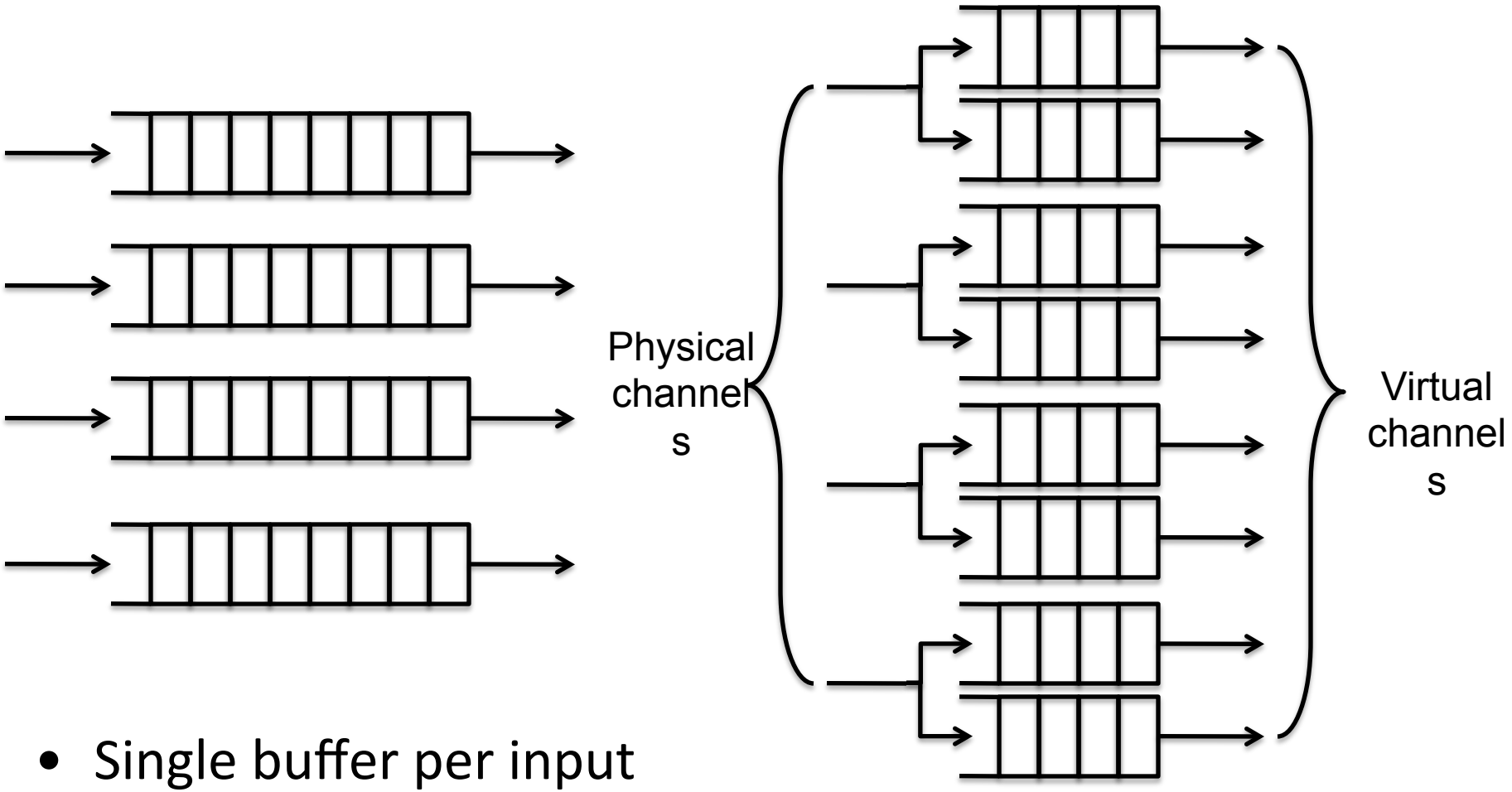
Router Pipeline Optimizations

- Bypassing: when no flits in input buffer
  - Speculatively enter ST
  - On port conflict, speculation aborted



  - In the first stage, a free VC is allocated, next routing is performed and the crossbar is setup

Buffer Organization



- Single buffer per input
- Multiple fixed length queues per physical channel

Arbiters and Allocators

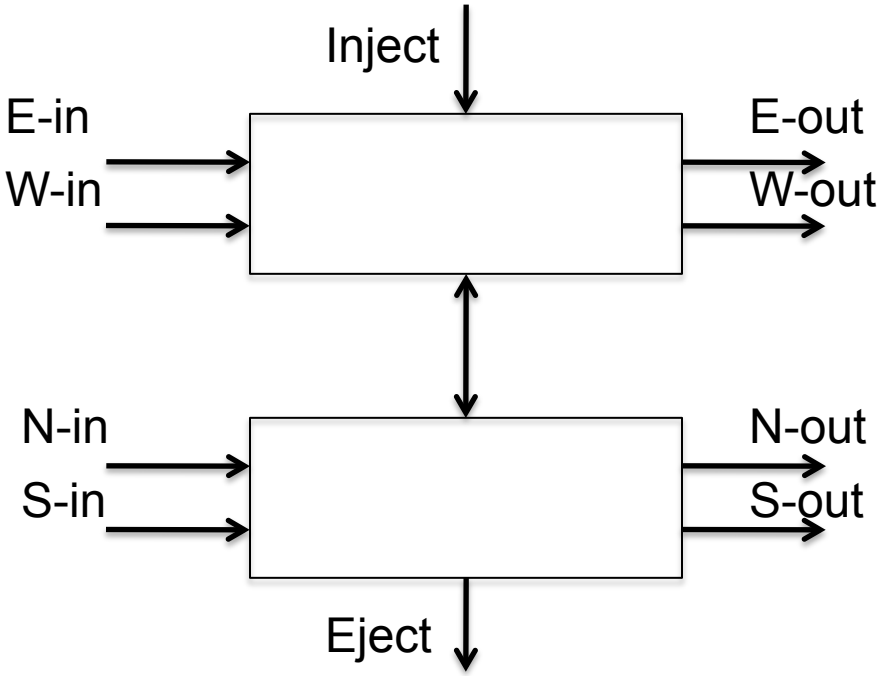
- *Allocator* matches N requests to M resources
- *Arbiter* matches N requests to 1 resource
- Resources are VCs (for virtual channel routers) and crossbar switch ports.
- Virtual-channel allocator (VA)
  - Resolves contention for output virtual channels
  - Grants them to input virtual channels
- Switch allocator (SA) that grants crossbar switch ports to input virtual channels
- Allocator/arbiter that delivers high matching probability translates to higher network throughput.
  - Must also be fast and able to be pipelined

Round Robin Arbiter

- Last request serviced given lowest priority
- Generate the next priority vector from current grant vector
- Exhibits fairness

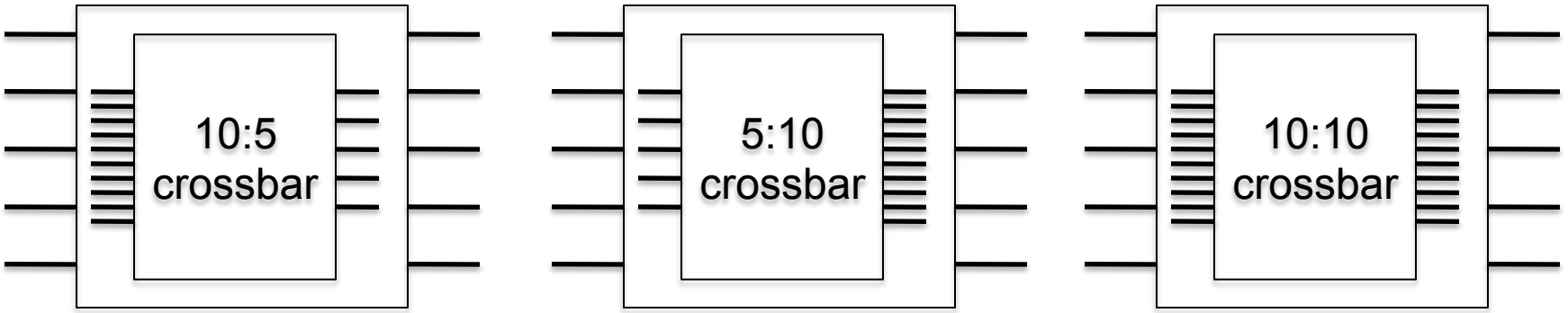
Crossbar Dimension Slicing

- Crossbar area and power grow with $O((pw)^2)$



- Replace 1 5x5 crossbar with 2 3x3 crossbars

Crossbar speedup



- Increase internal switch bandwidth
- Simplifies allocation or gives better performance with a simple allocator
- Output speedup requires output buffers
  - Multiplex onto physical link

Evaluating Interconnection Networks

- Network latency
  - Zero-load latency: average distance * latency per unit distance
- Accepted traffic
  - Measure the max amount of traffic accepted by the network before it reaches saturation
- Cost
  - Power, area, packaging

Interconnection Network Evaluation

- Trace based
  - Synthetic trace-based
    - Injection process
      - Periodic, Bernoulli, Bursty
  - Workload traces
- Full system simulation

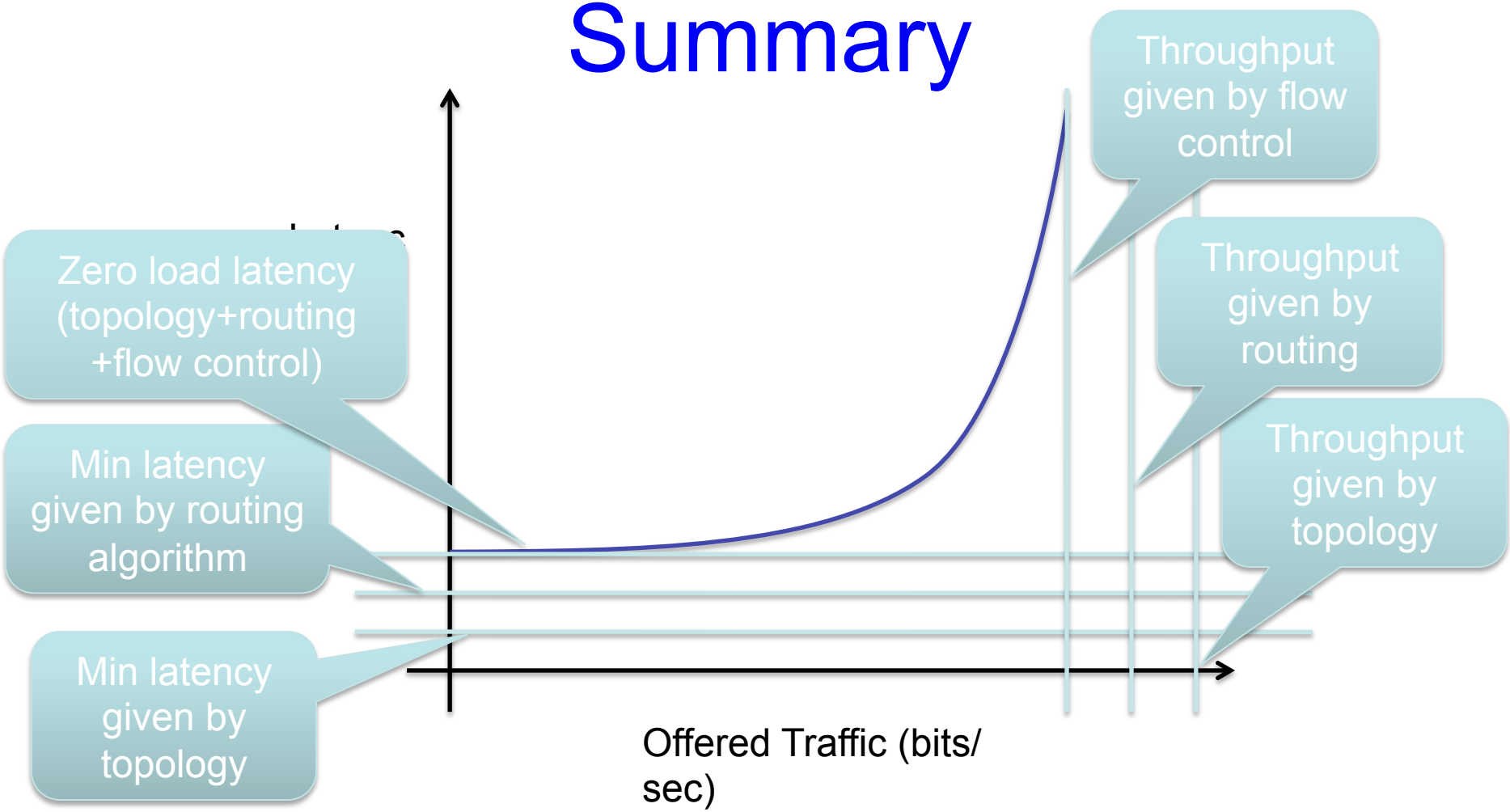
Traffic Patterns

- Uniform Random
  - Each source equally likely to send to each destination
  - Does not do a good job of identifying load imbalances in design
- Permutation (several variations)
  - Each source sends to one destination
- Hot-spot traffic
  - All send to 1 (or small number) of destinations

Microarchitecture Summary

- Ties together topological, routing and flow control design decisions
- Pipelined for fast cycle times
- Area and power constraints important in NoC design space

Interconnection Network Summary



- Latency vs. Offered Traffic

Thank You