EE 709 Testing and Verification of VLSI Circuits

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1. ASSIGNMENT 1

Q1. From the Handout the bridge detection probability with two test vectors (for G/0 and G/1) is 75 assuming equal probability of 1's and 0's on line H. (see slides 25-27). Recompute the bridge detection probability assuming the signal probability of 1's is 20 and of 0's is 80. Generalize this result for signal probability of 1's being p and number of times the node G tested is n.

$$\text{Let } P_{h(1)} = p$$
$$\text{then } P_{h(0)} = 1 - p$$

ANS Size of one test vector. = 2 and no of such test conducted = n
The test will fail if both the test vector fails which will happen if G/0 has H 1 or G/1 has H 0. Both of these should happen.
So probability that one test will fail $= p * (1 - p)$
probability that n test will fail $= (p * (1 - p))^n$
probability that n test will pass $= 1 - (p * (1 - p))^n$
If p = 0.2 and n = 1. $P_{pass} =$ **0.84**.

Q2 Compute a Fault Dictionary like slide-14, for a 3-input CMOS NOR gate. The inputs are a, b, c, and the output is d. The faulty outputs should be from 0, 1, N, Z. The fault list consists of input faults a/0, a/1, b/0, b/1, c/0, c/1 and transistor open and closed faults. Label the p-transistors ap, bp, and cp; the n-transistors an, bn, and cn

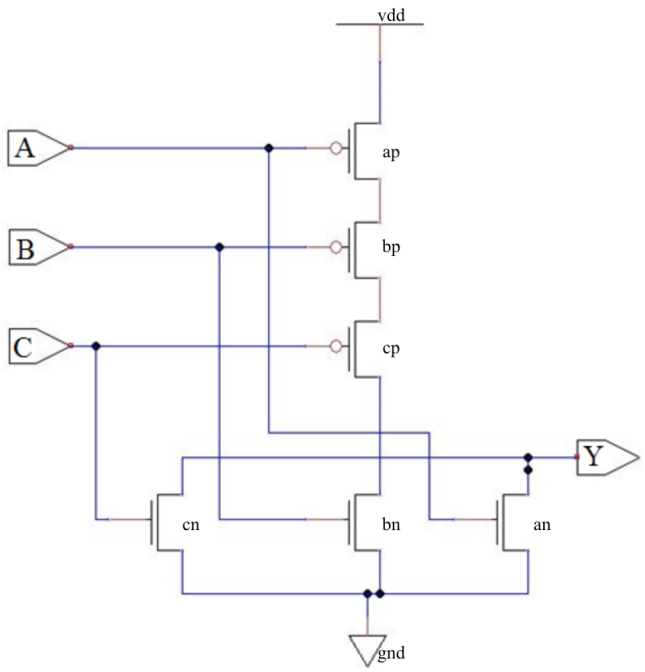

Figure 1. Nor gate

A	B	C	an(open)	an(short)	bn(open)	bn(short)	cn(open)	cn(short)
0	0	0	1	n	1	n	1	n
0	0	1	0	0	0	0	z	0
0	1	0	0	0	z	0	0	0
0	1	1	0	0	0	0	0	0
1	0	0	z	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

A	B	C	ap(open)	ap(short)	bp(open)	bp(short)	cp(open)	cp(short)
0	0	0	z	1	z	1	z	1
0	0	1	0	0	0	0	0	n
0	1	0	0	0	0	n	0	0
0	1	1	0	0	0	0	0	0
1	0	0	0	n	0	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

Q3 From the Handout slide-19, use the multiplexer with the node names shown to perform the following. Derive a minimal test set for "pin-faults" by inspection or trial and error. Apply this test to find the internal faults that are not covered.

ANS

A	B	C	Y	Fault testable
0	0	0	0	A/1. Y/1
0	0	1	0	B/1 Y/1
0	1	0	0	A/1 C/1 Y/1
0	1	1	1	B/0 C/0 Y/0
1	0	0	1	A/0 C/1 Y/0
1	0	1	0	B/1 C/0 Y/1
1	1	0	1	A/0 Y/0
1	1	1	1	B/0 Y/0

Now we can see that if we take the following testvector then all the faults will be detected.
We see that every internal fault is testable with this testvector.

A	B	C	Y	Pin Fault testable	Internal fault testable
0	1	0	0	A/1 C/1 Y/1	E/1 G/1 H/1
0	1	1	1	B/0 C/0 Y/0	E/0 H/0
1	0	0	1	A/0 C/1 Y/0	D/1 F/0 G/0
1	0	1	0	B/1 C/0 Y/1	D/0 F/1 G/1 H/1

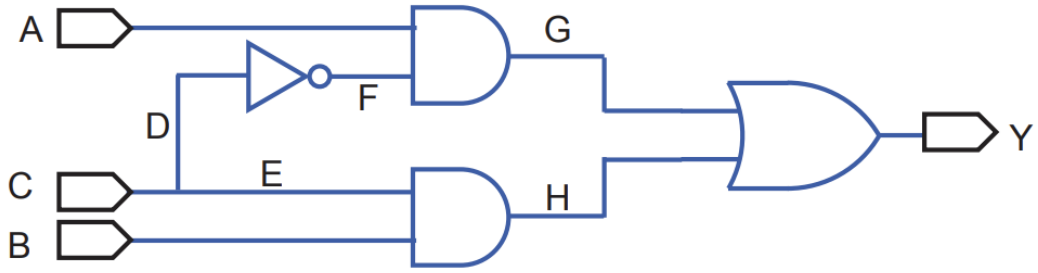

Figure 2. 2-to-1 MUX