Week 2: Assignment Solutions

1. Which of the following statements is true for Verilog modules?
    a. A module can contain definitions of other modules.
    b. When a module X is called multiple numbers of times from some other module, only one copy of module X is included in the hardware after synthesis.
    c. More than one module can be instantiated within another module.
    d. If a module X is instantiated 4 times within another module, 4 copies of X are created.

    Correct answers are (c) and (d).

    Module definitions must be disjoint. Also there is no concept of calling a module from other modules. We can only make copies or "instantiate" a module any number of times within another module.

2. What does the statement "assign f = (a & b) | (a ^ b)" signify?
    a. A gate level netlist consisting of one AND gate, one OR gate, and one XOR gate.
    b. A behavioral description of the function *f*.
    c. A structural description of the function *f*.
    d. A continuous assignment of the function realized by the right hand side to the net type variable on the left hand side.

    Correct answers are (b) and (d).

    The "assign" statement only specifies the function; it does not specify the gates or the netlist to be used for implementation. Hence (a) and (c) are false.

    It only specifies the behavior of the function. Only "net" type variables can be assigned in an "assign" statement. Hence (b) and (d) are true.

3. Which of the following is not true for register type variables?
    a. It will always map to a hardware register after synthesis.
    b. It can be used in an expression on the RHS of an "assign" statement.
    c. Once a value is assigned, it will hold the value.
    d. None of the above.

    Correct answer is (a).

    A register type variable may either map to a storage cell during synthesis, or it may also realize a pure combinational circuit.

    In an "assign" statement, both "net" and "register" type variables may be used in the expression on the right hand side. In terms of the behavior, a register type variable holds a value once it is assigned to it.

4. For the following Verilog code segment, what will be the number of bits in C as deduced during synthesis?

```
wire [9:0] A, B;
integer C;
C = A + B + 1;
```

a. 11
b. 10
c. 20
d. None of the above

Correct answer is (a).

Both A and B are 10-bit variables. When you compute A + B + 1, the result can never be more than 11 bits. For example in 4 bits, the maximum unsigned value can be 1111 = 15. Now, 15 + 15 + 1 = 31, which can be represented in 5 bits.

5. For the following Verilog code segment, if the initial value of IR is ABCD3456 (in hexadecimal), the value of "data" in decimal will be …….. (Note that "data" is a 4-bit variable)

```
wire [31:0] IR;
wire [3:0] data;
wire [15:0] d1;
wire [31:16] d2;
assign d1 = IR[31:16];
assign d2 = IR[15:0];
assign data = d1[11:8] + d2[19:16] + d2[31:28];
```

Correct answer is 4.

In binary, assignments occur as follows:

d1 = 1010 1011 1100 1101 (i.e. ABCD in hex)

d2 = 0011 0100 0101 0110 (i.e. 3456 in hex)

data = 1011 + 0110 + 0011 = 0100 (with a carry out of 1) = 4

6. Consider the following Verilog module.

```
module guess (data, cond, result);
  input [7:0] data;
  input [1:0] cond;
  output reg [7:0] result;
  always @(data)
    begin
      if (cond == 2'b01) result = data;
      else if (cond == 2'b10) result = data + 1;
      else if (cond == 2'b11) result = data - 1;
    end
endmodule
```

Which of the following is true when the module is synthesized?

a. A combinational circuit will be generated.

b. A sequential circuit with storage elements will be generated.
c. If the synthesizer supports adder and subtractor blocks, a combinational circuit will be generated.
d. None of the above.

Correct answer is (b).

Here, we do not assign values to "result" for all possible combinations of "cond". The case for cond = 00 is not specified, and hence storage elements will be generated for "result".

7. For the following Verilog code segment:

```
wire [7:0] A;
wire B;
assign B = ^A;
```

if the value of A is 16'b10110011, what will be the value of {A[4:3], 3{B}}?

a. 5'b10111 *
b. 5'b10000
c. 5'b01000
d. None of the above

Correct answer is (a).

The value of A[4:3] will be "10", and B = "1" (bitwise exor of all bits of A).

Thus the value will be 10 1 1 1.

8. When does the $monitor statement in a Verilog test bench print the specified values?

a. At the beginning of the simulation.
b. When the $monitor statement is first encountered.
c. Whenever the value of any of the specified variables change.
d. None of the above.

Correct answer is (c).

The $display statement prints the value whenever it is executed. In contrast, the $monitor statement prints the values whenever at least one of the variables in the list is modified.