Week 1: Assignment Solutions

1. What does Moore's law specify?
    a. The number of transistors in a VLSI chip will increase linearly with time.
    b. The number of transistors in a VLSI chip will increase exponentially with time.
    c. The power consumption in a VLSI chip will increase linearly with time.
    d. None of the above.

    Correct answer is (b).

    According to Moore's law, the number of transistors that can be fabricated in a chip will double every 18 months, i.e. an exponential growth is predicted. It does not talk anything about power consumption.

2. Which of the following does not represent a behavioral representation for the function f=A.B+C?
    a. The truth table of the function with output column (01010111)
    b. A Verilog specification: assign f = (A & B) | C;
    c. A netlist consisting of one 2-input AND and one 2-input OR gate
    d. None of the above

    Correct answer is (c).

    Truth table represents behavioral description, and so are logic expressions specified using "assign" statements. Any netlist representing an interconnection of blocks represents structural description.

3. Given a gate-level netlist represented by a graph, which of the following is not true for 4-input LUT mapping in a typical FPGA?
    a. The 4-input LUT is typically realized using a 16x1 SRAM unit.
    b. Any circuit subgraph with up to 4 input edges and 1 output edge can be mapped to a LUT irrespective of the number of vertices included therein.
    c. In SRAM-based LUTs, the function of the LUT can be changed by downloading appropriate bit patterns in the associated RAM locations.
    d. None of the above

    Correct answer is (d).

    The LUTs are typically realized using small SRAM units, and can realize any arbitrary function of up to 4 variables. The output column of the truth table of the function to be realized is downloaded to the SRAM.

4. For which design style, the following statement is true?

"*The fabrication cost of a chip is C = C1 + C2, where C1 represents a cost that is shared among several customers, while C2 represents a cost that is to be separately borne by every customer*."

a. Gate array
b. FPGA
c. Standard cell
d. Full custom

Correct answer is (a).

For gate arrays, fabrication proceeds in two phases. In the first phase, uncommitted transistors are fabricated that are independent of the functions being implemented. In the second phase, the interconnections of the transistors are carried out to realize arbitrary functionality. The first component of the cost (C1) is shared among all customers who are fabricating gate array chips, while the second component (C2) is specific to every customer).

5. Which of the following is not true for standard cell based design?
   (i) The heights of the cells are fixed but the widths can be different.
   (ii) Any number of cells can be placed in a row.
   (iii) The number of cells that can be placed in a row is fixed.
   (iv) It requires more design effort as compared to full custom design.
   a. (ii) and (iii)
   b. (ii) only
   c. (iii) and (iv)
   d. (iii) only

   Correct answer is (c).

   (iii) is false since the number of cells that can be placed in a row depends on their widths. (iv) is false since the cells are already pre-designed and just have to be places along rows in the layout.

6. Which of the following represents the correct ordering with respect to speed of circuits (fastest to slowest)?
   a. Full custom, Gate array, Standard cell, FPGA
   b. Full custom, Standard cell, FPGA, Gate array
   c. Full custom, Gate array, FPGA, Standard cell
   d. None of the above

   Correct answer is (d).

   The correct ordering should be Full Custom, Standard Cell, Gate Array, FPGA

7. Which of the following is true for structural design representation?
    a. The design is represented as a netlist of gates.
    b. The design is represented as a netlist of functional level modules.
    c. The input-output functional behavior will be specified.
    d. The "assign" statement in Verilog can be used to specify the design.

    Correct answers are (a) and (b).

    In structural design, we express the module as a netlist of blocks, where the blocks may be defined at any level (viz. gates, functional blocks, etc.). (c) and (d) corresponds to behavioral design.

8. Which of the following statements are not true?
    a. A test bench is required when we want to simulate a design.
    b. When we map the design to an application specific integrated circuit, we do not need a test bench.
    c. When we map the design to a field programmable gate array, we need a test bench.
    d. Simulation means generation of a gate level netlist from a behavioral specification.

    Correct answers are (c) and (d).

    (a) and (b) are clearly true. When we map a design to hardware like FPGA or ASIC, we do not need any test bench. Test bench is required for simulation, which involves using simulator software to analyze the input-output behavior of a given design.

9. What function do the following Verilog module implement?

```
module guess (f, a, b, c);
  input a,b,c;  output f,
  wire t1, t2;
  nand #1 G1 (t1,a,b);
  or   #1 G2 (t2,b,c);
  and  #1 G3 (f,t1,t2);
endmodule
```

    a. f = a'.b + a'.c + b'.c
    b. f = a'.b + b'.c + c'.a
    c. f = a.b + b.c + c.a
    d. None of the above

    Correct answer is (a).

    From the gate descriptions, we can write:

    t1 = (a.b)' = a' + b'

    t2 = b + c

    f = t1.t2 = (a' + b').(b+c) = a'.b + a'.c + b'.b + b'.c

    = a'.b + a'.c + b'.c

10. What function do the following Verilog module implement?

```
module guess (f, a, b, c);
  input a,b,c;  output f,
  wire t;
  assign t = (a & b) | c;
  assign f = a ^ t;
endmodule
```

a. f = a'.b + a'.b'.c

b. f = a'.c + a.b'.c'

c. f = a'.c + a'.b.c'

d. None of the above

Correct answer is (b).

From the logic expressions, we can write

t = a.b + c

f = a^t = a'.t + a.t' = a'.(a.b + c) + a.(a.b + c)' = a'.c + a.b'.c'