EE 709 Assignment: Due on 14 February

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February 5, 2020

You are asked to design an 8-bit adder with inputs $a7, a6, \ldots, a0$ and $b7, b6, \ldots, b0$ and outputs $s7, s6, \ldots s0$ which satisfy the following specification:

$$
\begin{aligned}
s0 &= a0 \oplus b0 \\
c0 &= a0.b0 \\
s1 &= a1 \oplus b1 \oplus c0 \\
c1 &= a1.b1 + a1.c0 + b1.c0 \\
s2 &= a2 \oplus b2 \oplus c1 \\
c1 &= a2.b2 + a2.c1 + b2.c1 \\
&\ldots \\
s7 &= a7 \oplus b7 \oplus c6
\end{aligned}
$$

- Design a carry lookahead adder implementation of this adder in which the carries are directly generated from the primary inputs.
- Verify, using the BDD package, that the implementation is equivalent to the specification.