Week 3: Assignment Solutions

1. Which of the following statements are false?
    a. The “assign” statement implements continuous assignment.
    b. The procedural assignment statements can be used to mode structural designs.
    c. For an “assign” statement, the left hand side can be either a “net” type or a “register” type variable.
    d. All of the above.

    Correct answers are (b) and (c).
    Procedural assignment statements can only model behavior; they cannot model netlist that is a requirement for structural modeling.
    For an “assign” statement, the left hand side can only be a “net” type variable.
2. Which of the following are true for the following code segment?

```
input [31:0] a;
input [0:4] b;
input sel;
output f;
assign f = sel ? a[b] : 1'b0;
```

    a. One 32-to-1 and one 2-to-1 multiplexers will be generated.
    b. One 2-to-1 multiplexer will be generated.
    c. A single large multiplexer will be generated.
    d. None of the above.

    Correct answer is (a).
    The conditional statement “? :” will be generating a 2-to-1 multiplexer, with “sel” as the select input. The first input of the multiplexer will be connected to 0, while the second input will be connected to the output of a 32-to-1 multiplexer. This multiplexer will have the bits of “a” as input, and “b” as the select lines.
3. Which of the following constructs will be generating a decoder / demultiplexer, where “a”, “b” and “c” are variables?
    a. assign a = b[c];
    b. assign b[c] = a;
    c. assign a = (b) ? c : ~c;
    d. assign a = b & c

    Correct answer is (b).
    A decoder will be generated if the LHS of an assignment is an array reference with a variable as index.
4. What does the following code segment implement?

```
assign d = ~(c & b);
assign c = ~(a & d);
```

    a. A 2-bit shift-register.
    b. Two NOR functions connected in cascade.
    c. A one-bit latch.
    d. A 2-bit comparator.

    Correct answer is (c).
    The first NOR will have “b” and “c” as inputs and give “d” as output. The second NOR will have “a” and “d” as inputs and give “c” as output. This

corresponds to a pair of cross-coupled NOR gate, which is used to build s one-bit latch.

5. Which of the following is true for the "initial" procedural block?
    a. It can be used to specify a module for synthesis.
    b. A module can contain any number of "initial" blocks.
    c. An "initial" block is executed only once.
    d. The "initial" block can contain a number of sequential statements inside "begin … end".

    Correct answers are (b), (c) and (d).
    (a) is false because the "initial" block is used only in test benches, and cannot be used to write a module that can be synthesized. (b), (c) and (d) are true that follows from the definition of "initial" block.
6. What does the following code segment indicate?

```
initial  clk = 1'b1;
always #10 clk = ~clk;
```

    a. Falling edges of the clock will appear at times 10, 30, 50, 70, …
    b. Falling edges of the clock will appear at times 20, 40, 60, 80, …
    c. Falling edges of the clock will appear at times 10, 20, 30, 40, …
    d. None of the above

    Correct answer is (a).
    The "initial" block sets the "clk" signal to 1 at time 0. The "always" block toggles "clk" with a delay of 10. Clearly, the period of the clock is 20. The first falling edge will appear at time 10, and repeat at intervals of 20 henceforth.
7. If "clk" and "clear" are two inputs of a module that defines a register, which of the following event expressions must be used if we want to implement asynchronous clear (assuming "clear" is active low)?
    a. always @(posedge clk)
    b. always @(negedge clear)
    c. always @(posedge clk or negedge clear)
    d. None of the above

    Correct answer is (c).
    For asynchronous clear, the "always" block must be activated whenever "clear" goes low irrespective of the "clk" edge. Thus option (c) has to be used.
8. Which of the following is true for the following module?

```
module mydesign (a, b);
input [1:0] b;
output reg a;
always @(b)
begin
if (b == 2'b00) a = 1'b0;
else if (b == 2'b11) a = 1'b1;
end
endmodule
```

    a. A combinational circuit implementing a XOR function will be generated.
    b. A combinational circuit implementing an AND function will be generated.

c. A latch will be generated for the output “a”.
d. The synthesis tool will give an error.

Correct answer is (c).
Assignment to variable “a” is not specified for all values of the input “b”. Hence a latch will be generated for “a”.

9. Which of the following is true for the “repeat” loop?
    a. It can be used to iterate a block a fixed number of times.
    b. It can be used to iterate a block until a specified condition is true.
    c. It can be used to iterate a block indefinitely.
    d. It can be used to repeat execution of the block two times.

    Correct answer is (a).
    The syntax of the “repeat” statement is “repeat (n) begin … end”, where “n” is some constant. The statements in “begin … end” are executed “n” times.
10. What does the construct “#10” indicate in simulation?
    a. Unit of delay is 10.
    b. Give a delay of 10 before executing the next statement.
    c. Execute the next statement at time 10.
    d. Pause execution of the statements that follow after time 10.

    Correct answer is (b).
    Whenever the construct #10 is encountered, simulation is delayed for 10 time units before going to the next statement.