S1

R7 → mem, alu_a, tp

db → ir

+1 → alu_b

alu → R7

S2

I_{11-9} → A1-RF

I_{8-6} → A2-RF

D1 → T1

D2 → T2

R7 → alu_a

I_{5-0} → SE_6 → alu_b

alu → T3

I_{8-0} → P.E

S3

T1 → alu_a

T2 → alu_b

alu → T3

P.E → A2-RF

D2 → T2

S4

I_{5-3} → A3-RF

T3 → D3-RF

S5

I_{5-0} → SE_6 → alu_a

+1 → alu_b

alu → T3

tp → mem_add

db → tp

S6

I_{8-6} → A3-RF

T3 → D3

S7

I_{5-0} → SE_6 → alu_a

T2 → alu_b

alu → T3

S8

I_{11-9} → A3-RF

tp → D3-RF

S9

T3 → mem - add
T1 → mem - data

S10

T1 → alu_a
T2 → alu_b
if (z) T3 → R7

S11

T3 → D3_RF
I_{11-9} → A3-RF
T2 → R7

S12

tp → alu
I_{8-0} → SE_9 → alu
alu → T3
T1 → mem_add
db → T2

S13

R7 → D3_RF
I_{11-9} → A3_RF
T3 → R7

S14

I_{8-0} → L.Sh-7 → D3
I_{11-9} → A3

S15

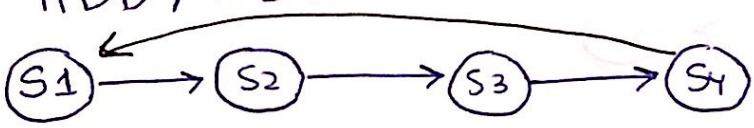
P.E → A3_RF
T2 → D3_RF
T1 → alu_a
+1 → alu_b
alu → T1

S16

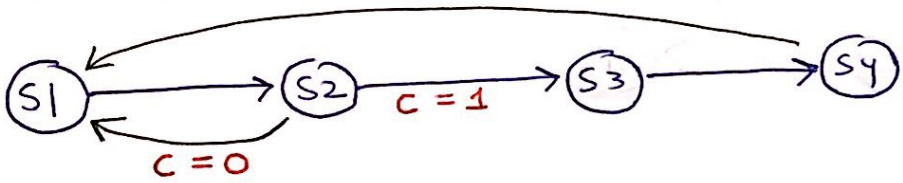
T1 → mem_add
T2 → mem_data
T1 → alu
+1 → alu
alu → T1

STATE TRANSITION DIAGRAMS

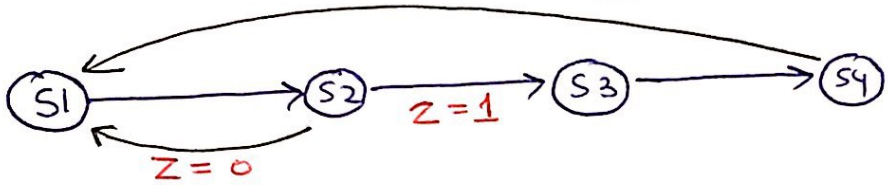
(1) ADD / NDU



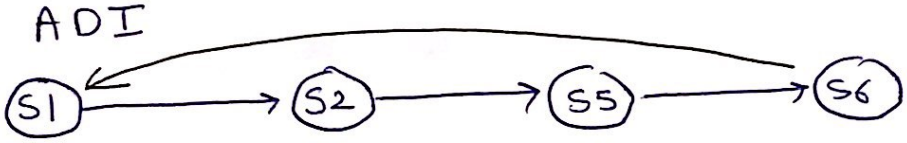
(2) ADC / NDC



(3) ADZ / NDZ

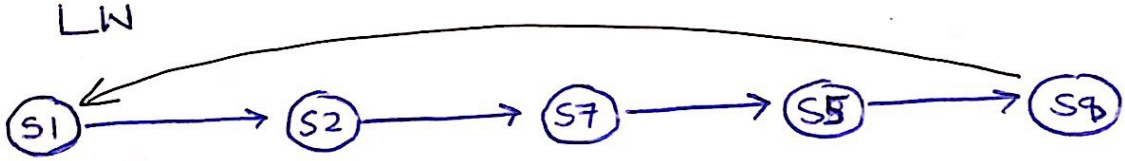


(4) ADI

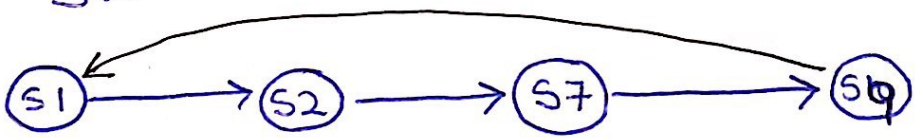


(5) LHI

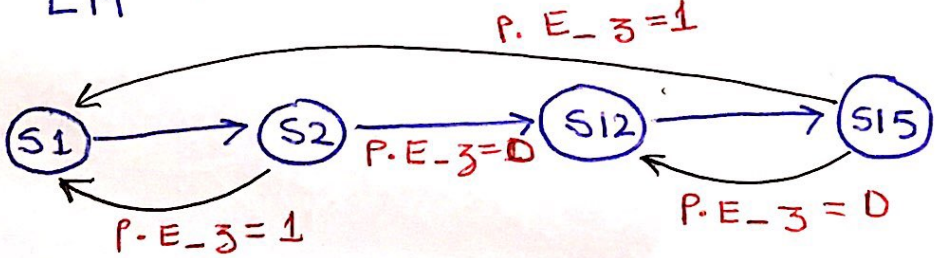
(6) LW



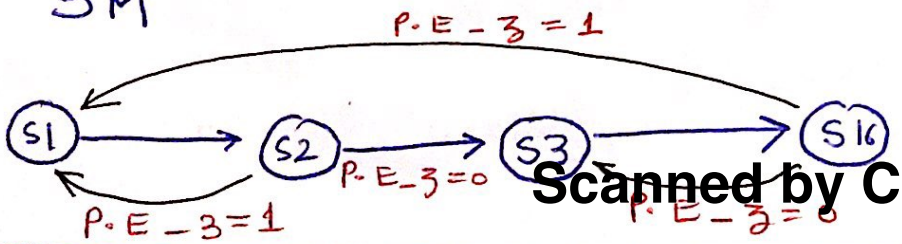
(7) SW



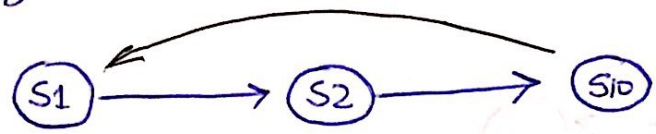
(8) LM



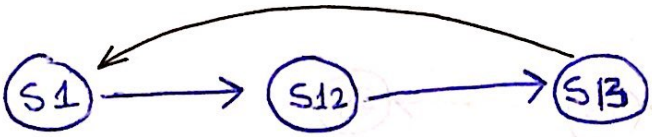
(9) SM



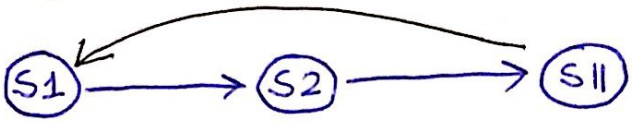
(10) BEQ



(11) JAL



(12) JLR



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