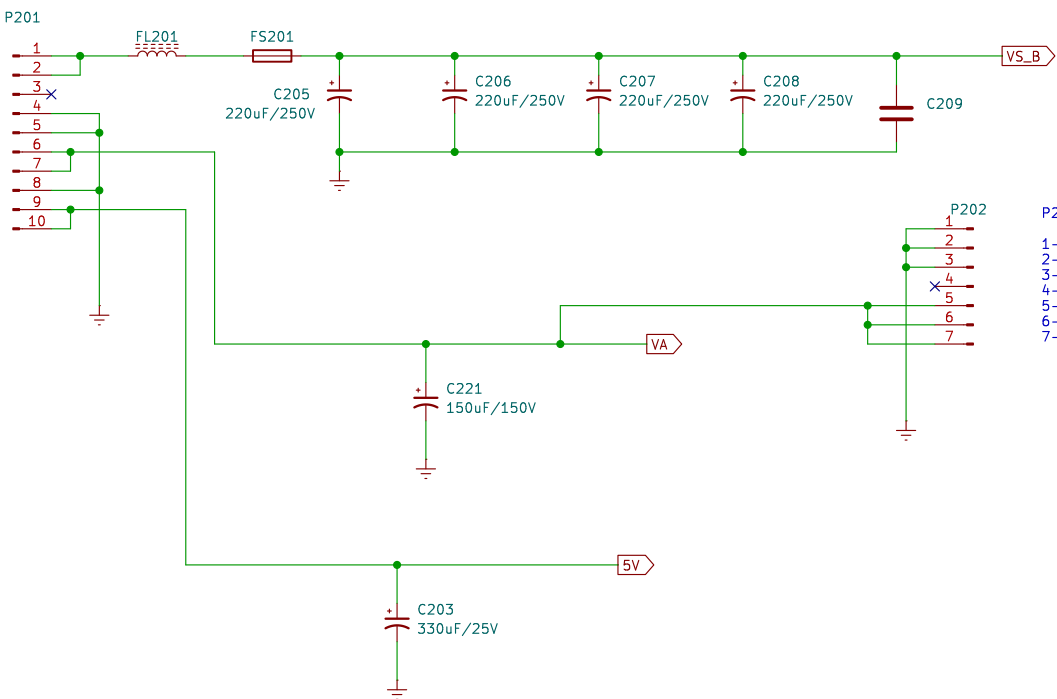


VOLTAGES SUPPLY

P201 (Input Power Supply)

- 1- +VS
- 2- +VS
- 3- NC
- 4- GND
- 5- GND
- 6- +VA
- 7- +VA
- 8- GND
- 9- +5V
- 10- +5V



P202 (Output VA Supply)

- 1- GND
- 2- GND
- 3- GND
- 4- NC
- 5- +VA
- 6- +VA
- 7- +VA

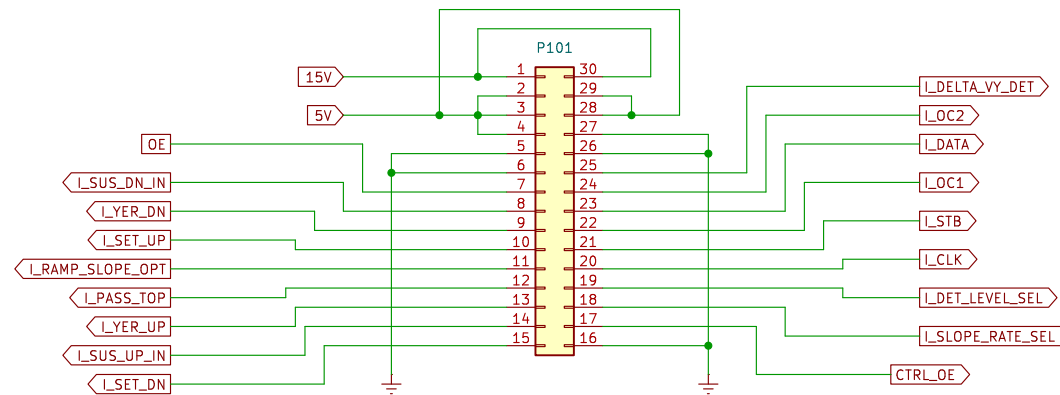
VS Voltage supply
Author: Fábio Pereira da Silva

Sheet: /
File: y_board.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4	Date: 2025-03-24	Rev: 1.0
KiCad E.D.A. 8.0.9		Id: 1/15

Input Control (Part 1 of 3)



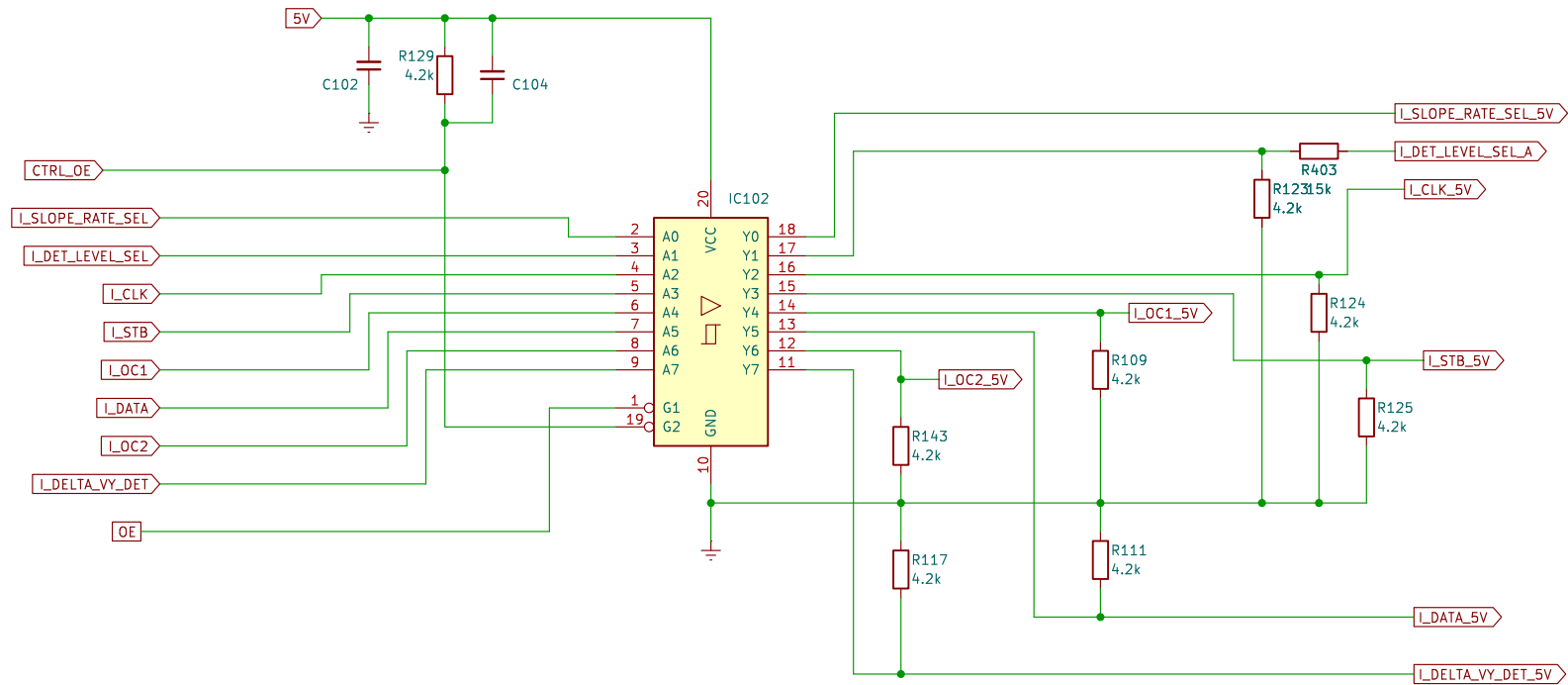
Input Control (Part 1 of 3)
Author: Fábio Pereira da Silva

Sheet: /Input control (Part 1 of 3)/
File: input_control.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4	Date: 2025-03-24	Rev: 1.0
KiCad E.D.A. 8.0.9		Id: 2/15

Input Control (Part 2 of 3)



Input Control (Part 2 of 3)
Author: Fábio Pereira da Silva

Sheet: /Input control (Part 2 of 3)/
File: input_control2.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4	Date: 2025-03-24	Rev: 1.0
KiCad E.D.A. 8.0.9		Id: 3/15

The schematic diagram illustrates the internal connections of the IC103, a 20-pin integrated circuit. The IC is represented by a yellow rectangle with pins numbered 1 to 20. The pins are connected as follows:

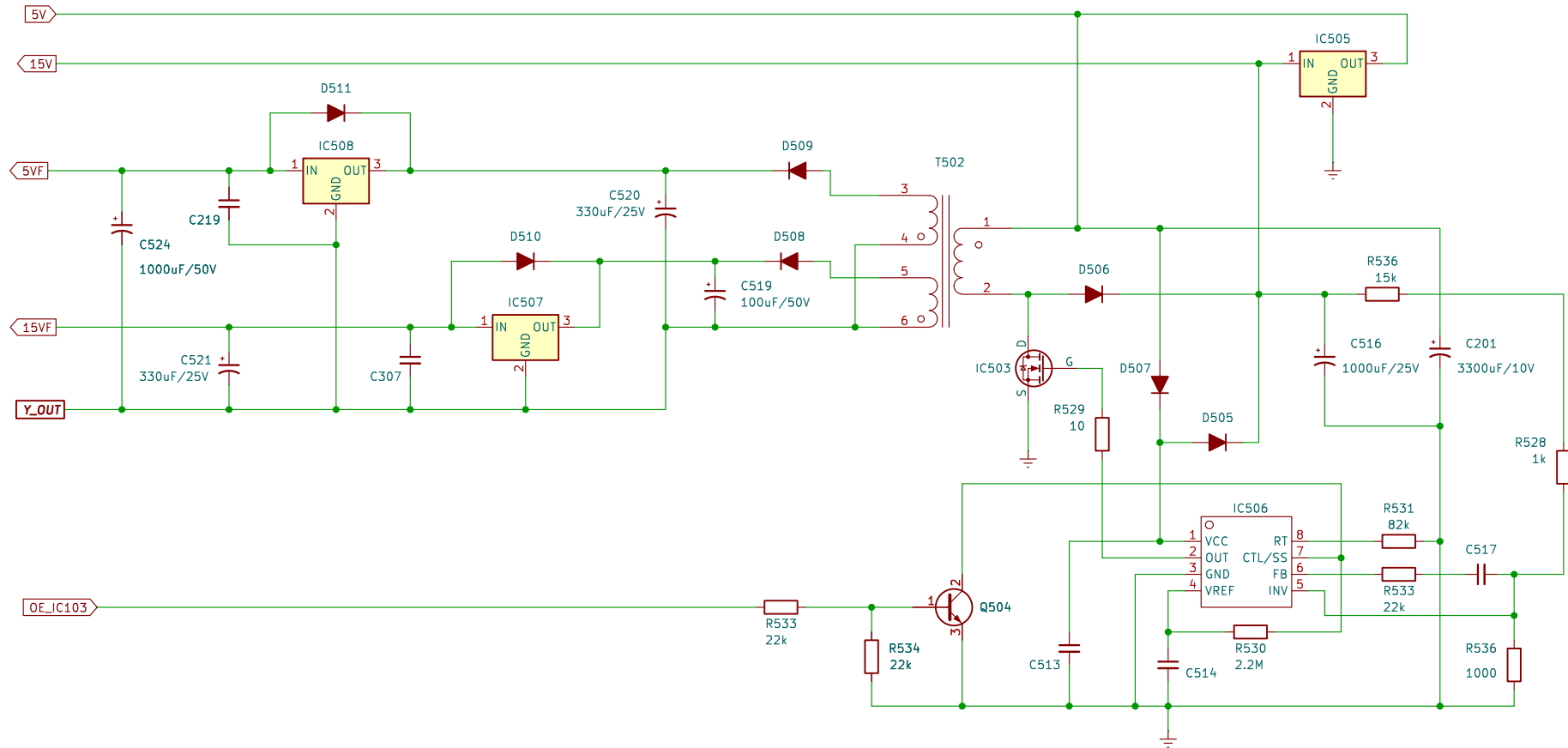
- Power Supply:**
 - VCC (Pin 20) is connected to a 5V supply.
 - GND (Pin 10) is connected to ground.
- Inputs:**
 - A0 (Pin 2) is connected to CTRL_OE.
 - A1 (Pin 3) is connected to I_SUS_DN_IN.
 - A2 (Pin 4) is connected to I_YER_DN.
 - A3 (Pin 5) is connected to I_SET_UP.
 - A4 (Pin 6) is connected to I_RAMP_SLOPE_OPT.
 - A5 (Pin 7) is connected to I_PASS_TOP.
 - A6 (Pin 8) is connected to I_YER_UP.
 - A7 (Pin 9) is connected to I_SUS_UP_IN.
 - G1 (Pin 1) is connected to I_SET_DN.
 - G2 (Pin 19) is connected to OE.
- Outputs:**
 - Y0 (Pin 18) is connected to Y_SUS_DOWN_5V.
 - Y1 (Pin 17) is connected to Y_ER_DOWN_5V.
 - Y2 (Pin 16) is connected to SET_UP_5V.
 - Y3 (Pin 15) is connected to RAMP_SLOPE_OPT_5V.
 - Y4 (Pin 14) is connected to BLOCKING_5V.
 - Y5 (Pin 13) is connected to Y_ER_UP_5V.
 - Y6 (Pin 12) is connected to Y_SUS_UP_5V.
 - Y7 (Pin 11) is connected to SET_DOWN_5V.
- Other Components:**
 - A capacitor C103 is connected to the 5V supply.
 - Resistors R105 and R108 (both 4.2k) are connected to the OE pin (G2) and ground.

Metadata:

- Input Control (Part 3 of 3)
- Author: Fábio Pereira da Silva
- Sheet: /Input control (Part 3 of 3)/
- File: input_control3.kicad_sch
- Title: Y BOARD LG PLASMA TV PANEL**
- Size: A4
- Date: 2025-03-24
- Rev: 1.0
- KiCad E.D.A. 8.0.9
- Id: 4/15

Id: 4/15

5VF, 15VF and 15V Supply



5VF, 15VF and 15V Supply
 Author: Fábio Pereira da Silva

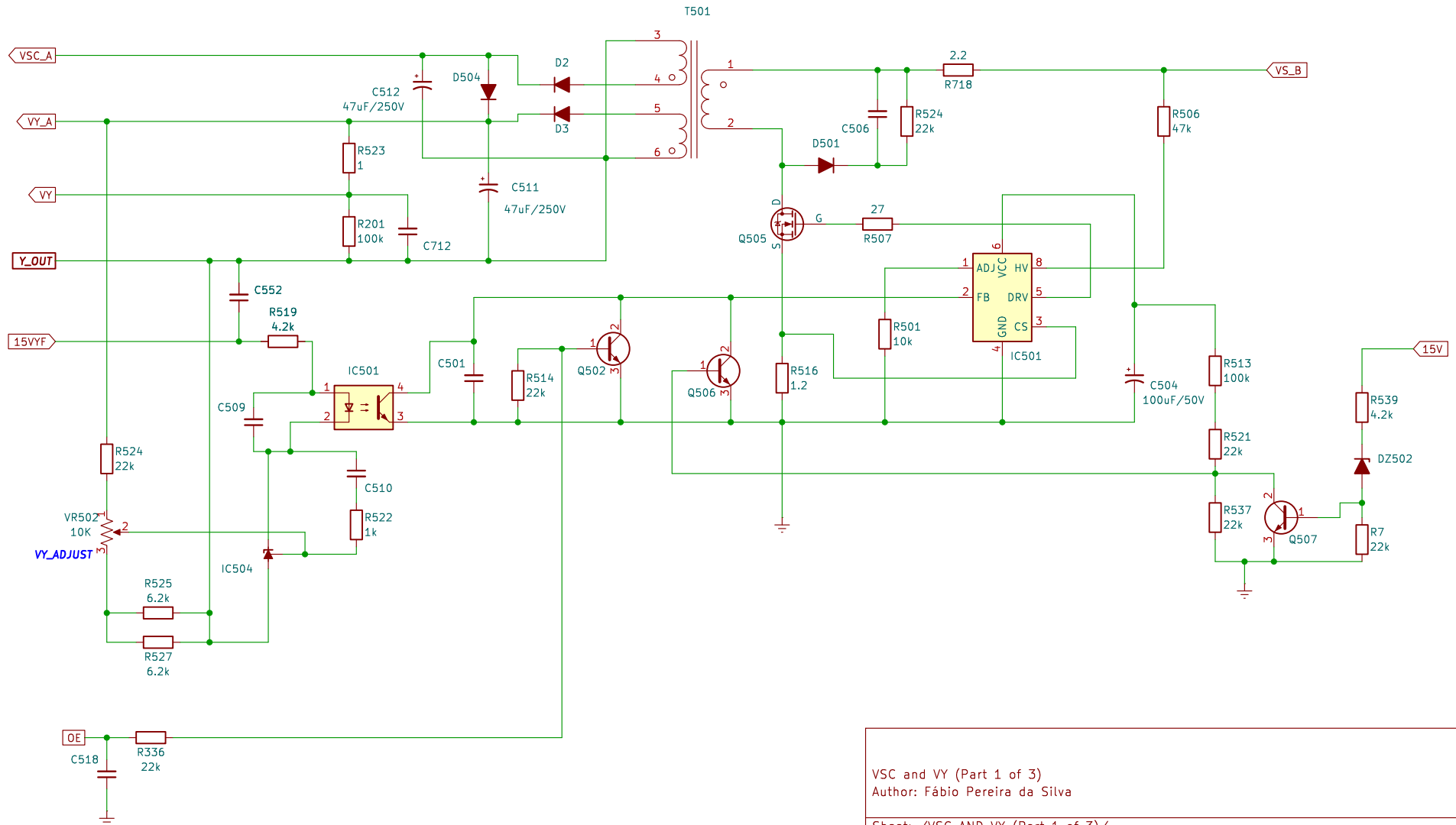
Sheet: /5VF, 15VF 15v/
 File: 5VF_15VF_15V.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4 Date: 2025-03-24
 KiCad E.D.A. 8.0.9

Rev: 1.0
 Id: 5/15

VSC and VY (Part 1 of 3)



VSC and VY (Part 1 of 3)
Author: Fábio Pereira da Silva

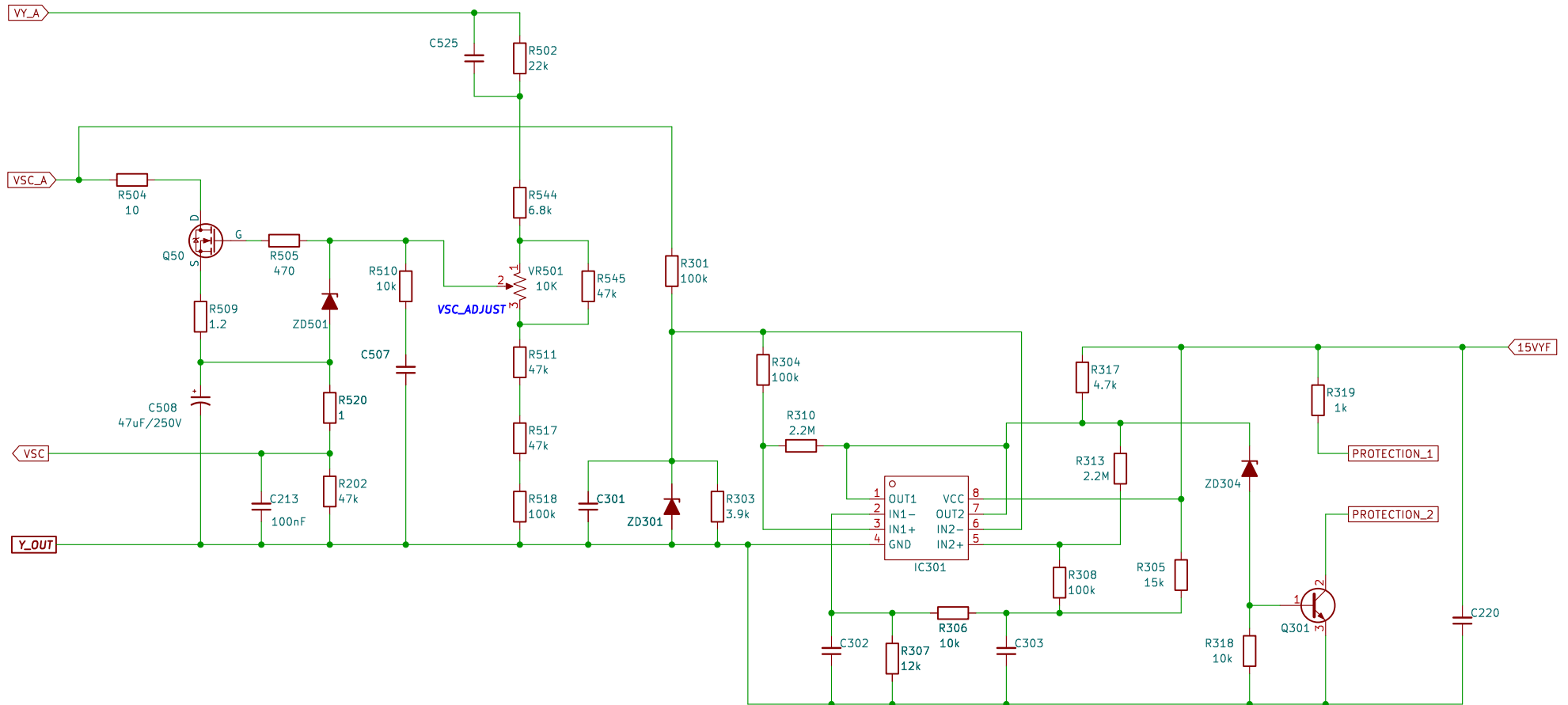
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File: vsc_and_vy.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4 Date: 2025-03-24
KiCad E.D.A. 8.0.9

Rev: 1.0
Id: 6/15

VSC and VY (Part 2 of 3)



VSC and VY (Part 2 of 3)
Author: Fábio Pereira da Silva

Sheet: /VSC and VY (Part 2 of 3)/
File: vcs_and_vy_part2_of_3.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

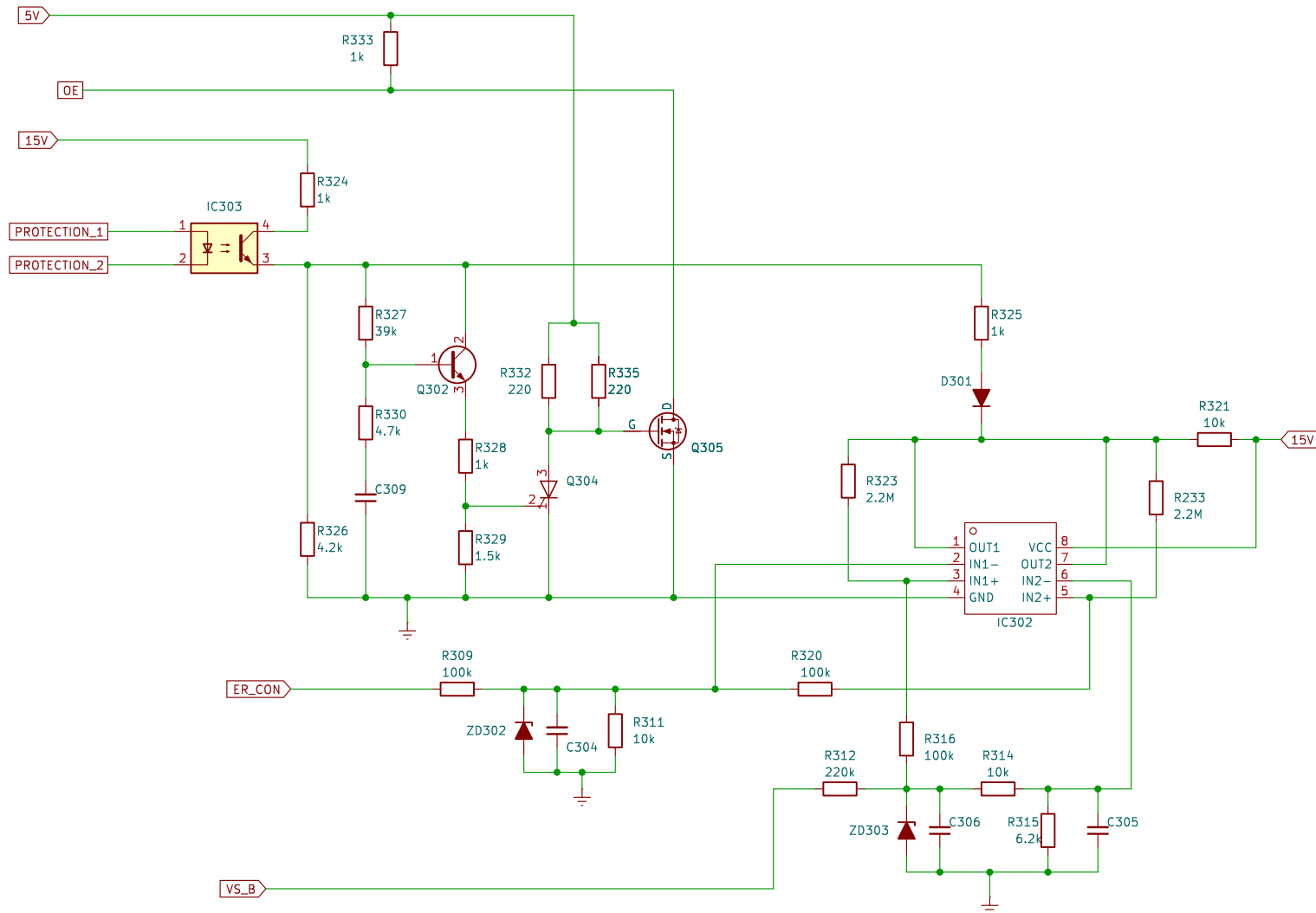
Size: A4
KiCad E.D.A. 8.0.9

Date: 2025-03-24

Rev: 1.0

Id: 7/15

VSC and VY (Part 3 of 3)



Author: Fábio Pereira da Silva

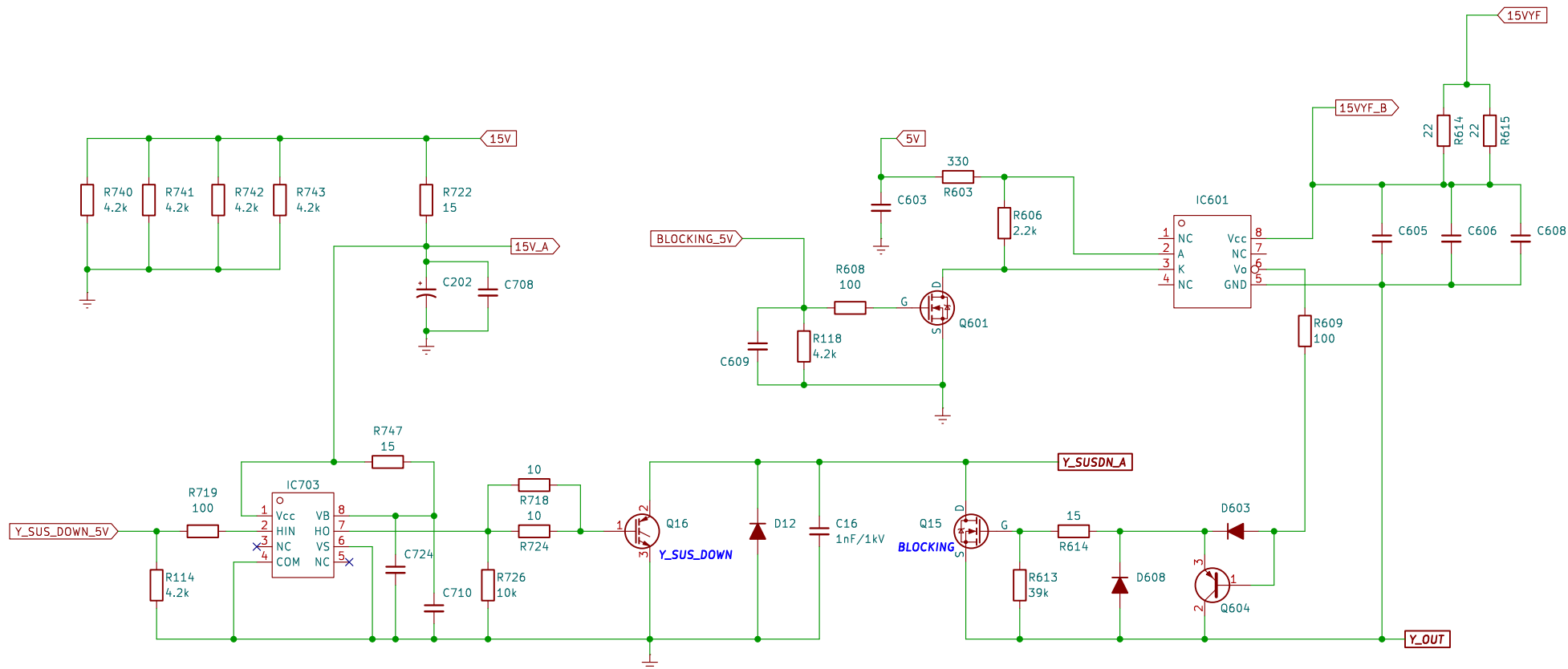
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File: vsc_and_vy_part3_of_3.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4 Date: 2025-03-24
KiCad E.D.A. 8.0.9

Rev: 1.0
Id: 8/15

Y BLOCKING AND Y SUS DOWN



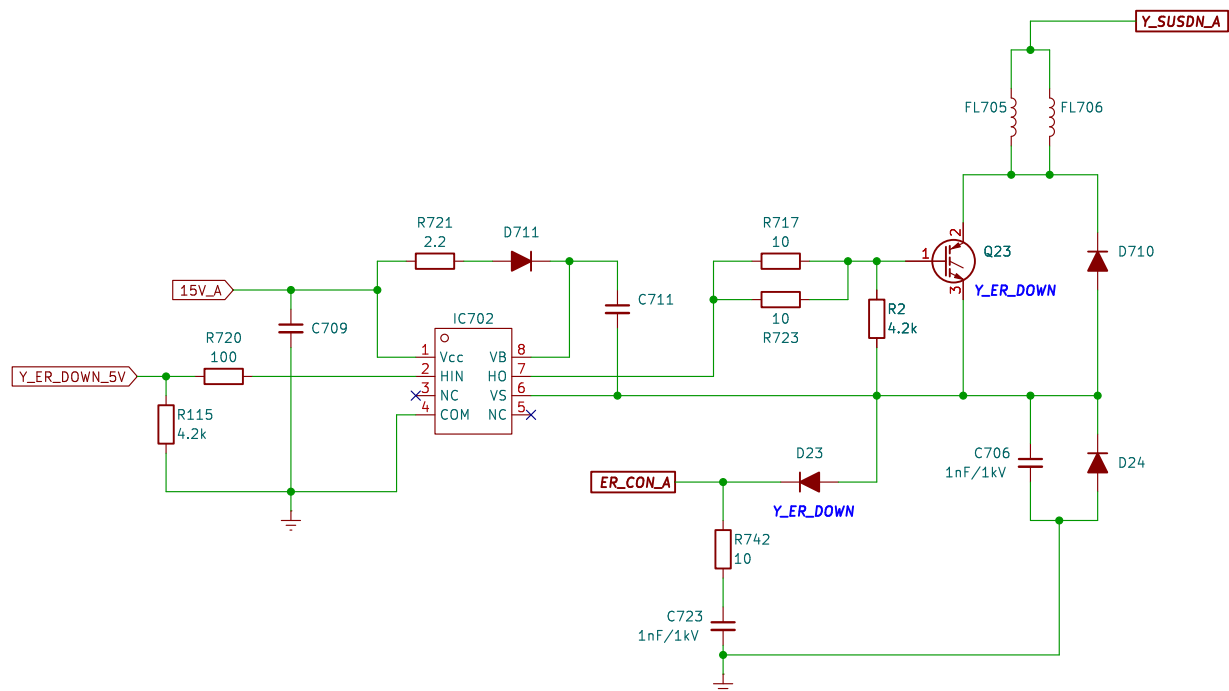
Y_BLOCKING | Y_SUS_DOWN
 Author: Fábio Pereira da Silva

Sheet: /Y_SUS_DOWN_AND_Y_BLOCKING/
 File: y_sus_dn_and_blocking.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4	Date: 2025-03-24	Rev: 1.0
KiCad E.D.A. 8.0.9		Id: 9/15

Y ENERGY RECOVERY DOWN



Y ER DOWN
Author: Fábio Pereira da Silva

Sheet: /y_er_down/
File: y_er_down.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4 Date: 2025-03-24
KiCad E.D.A. 8.0.9

Rev: 1.0
Id: 10/15

Y ENERGY RECOVERY UP AND Y SUS UP

Y ENERGY RECOVERY COIL

ER_CON_A

L703

ER_CON

C717

C720

FL702

FL701

D22

VS_B

C707

D21

Y_SUS_UP

Q13

Q12

Q11

R713

R708

R709

R711

R710

R714

D11

Y_OUT

15VVF_B

R730

R728

C704

C702

IC704

C1

B1

E1_E2

B2

R705

10k

R4

R5

R6

10k

Y_ER_UP

D701

5V

C701

R702

100

R120

4.2k

C713

IC701

1

2

3

4

5

6

7

8

16

15

14

13

12

11

10

9

Via

Vib

VDD1

GND1

DISABLE

NC

NC

NC

VDDB

Vob

NC

VDD1

VDDA

Voa

GNDA

NC

NC

NC

VDDB

Vob

GNDB

R704

10

C705

R703

10

Q701

Q702

15VVF_C

R12

10k

Y_ER_UP_5V

Y_SUS_UP_5V

C714

R721

4.2k

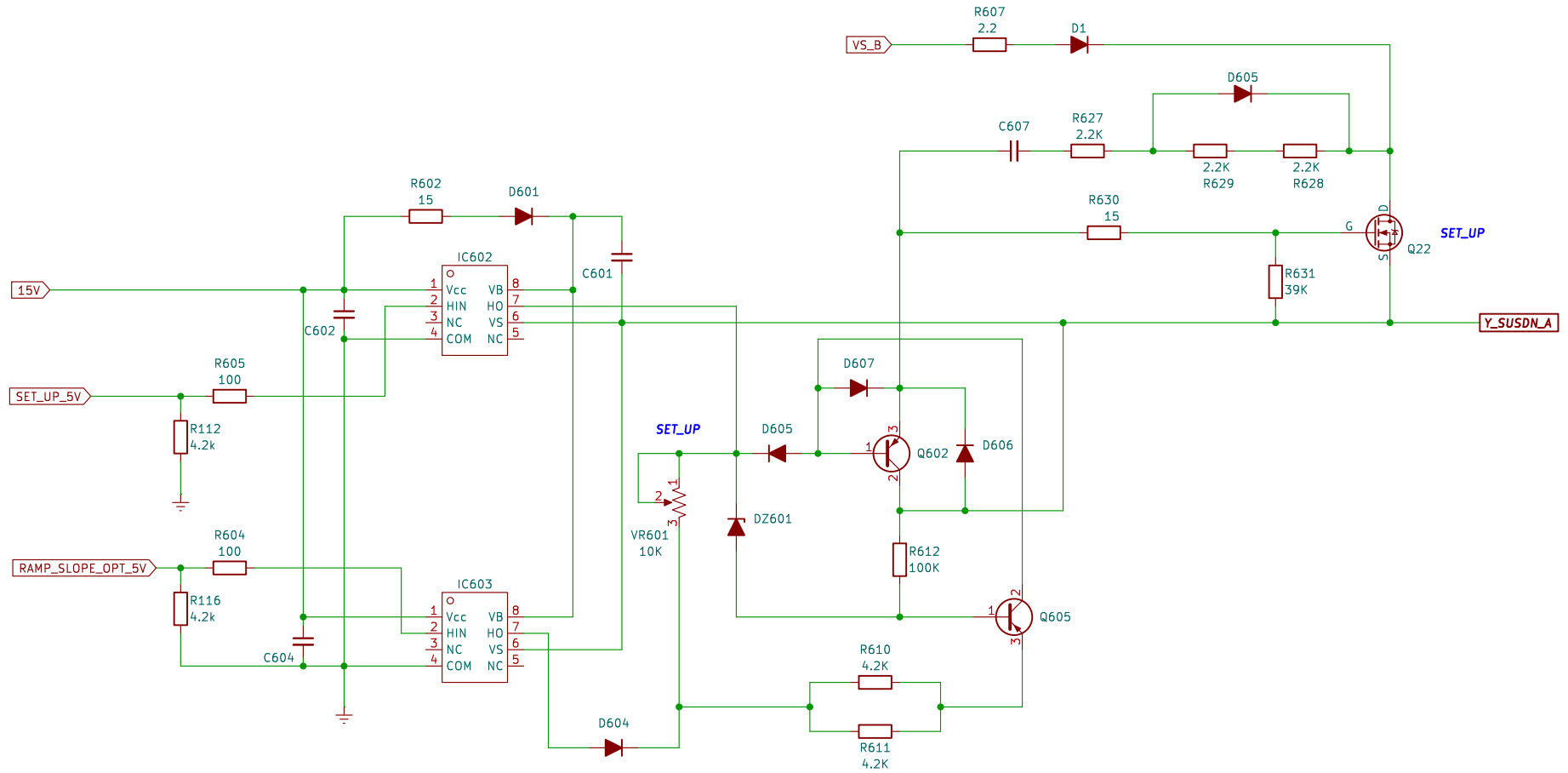
R701

100

Sheet: /y_er_up_and_sus_up/
File: y_er_up_and_sus_up.kicad_sch
Title: Y BOARD LG PLASMA TV PANEL
Size: A4 Date: 2025-03-24 Rev: 1.0
KiCad E.D.A. 8.0.9 Id: 11/15

Rev: 1.0
Id: 11/15

SET UP



Set Up
Author: Fábio Pereira da Silva

Sheet: /SetUp/
File: set_up.kicad_sch

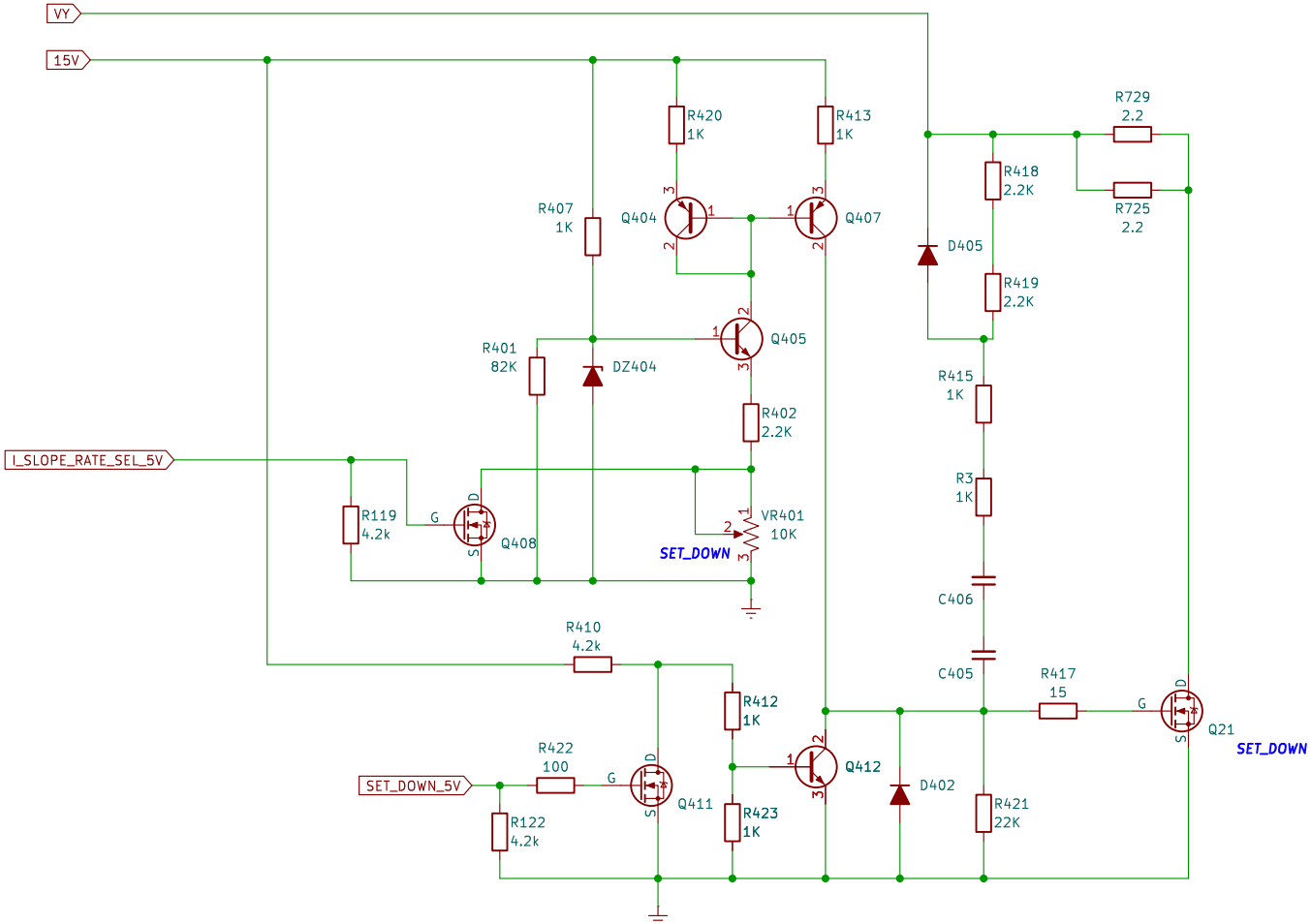
Title: Y BOARD LG PLASMA TV PANEL

Size: A4
Date: 2025-03-24

KiCad E.D.A. 8.0.9

Rev: 1.0
Id: 12/15

SET DOWN



Author: Fábio Pereira da Silva

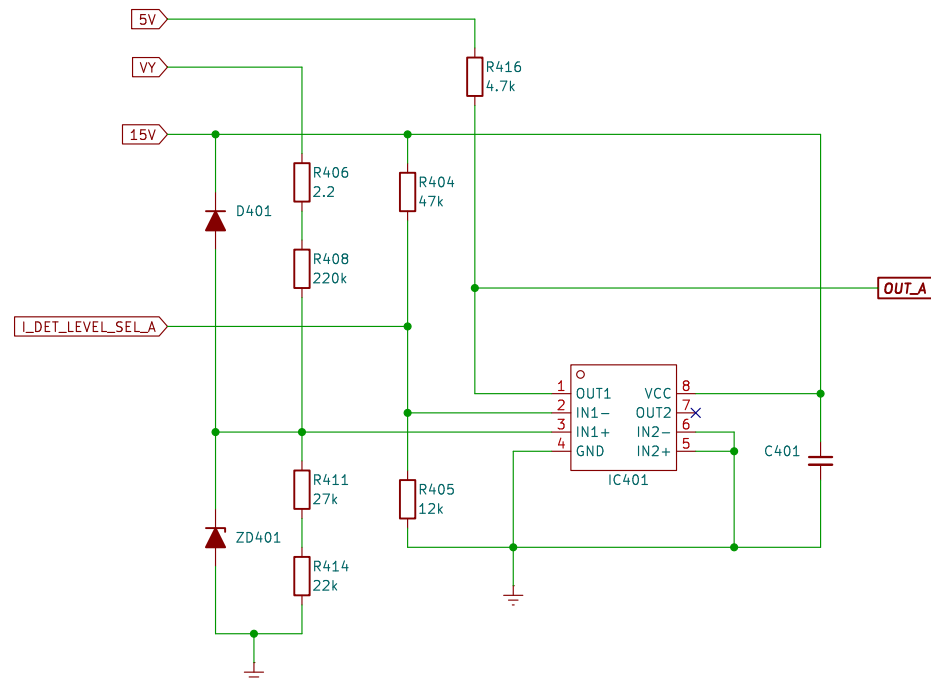
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File: set_down.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4	Date: 2025-03-24
KiCad E.D.A. 8.0.9	

Rev: 1.0
Id: 13/15

OUTPUT CONTROL (Part 1 of 3)



Output Control (Part 1 of 3)
Author: Fábio Pereira da Silva

Sheet: /Output Control (Part 1 of 3)/
File: output_control.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4

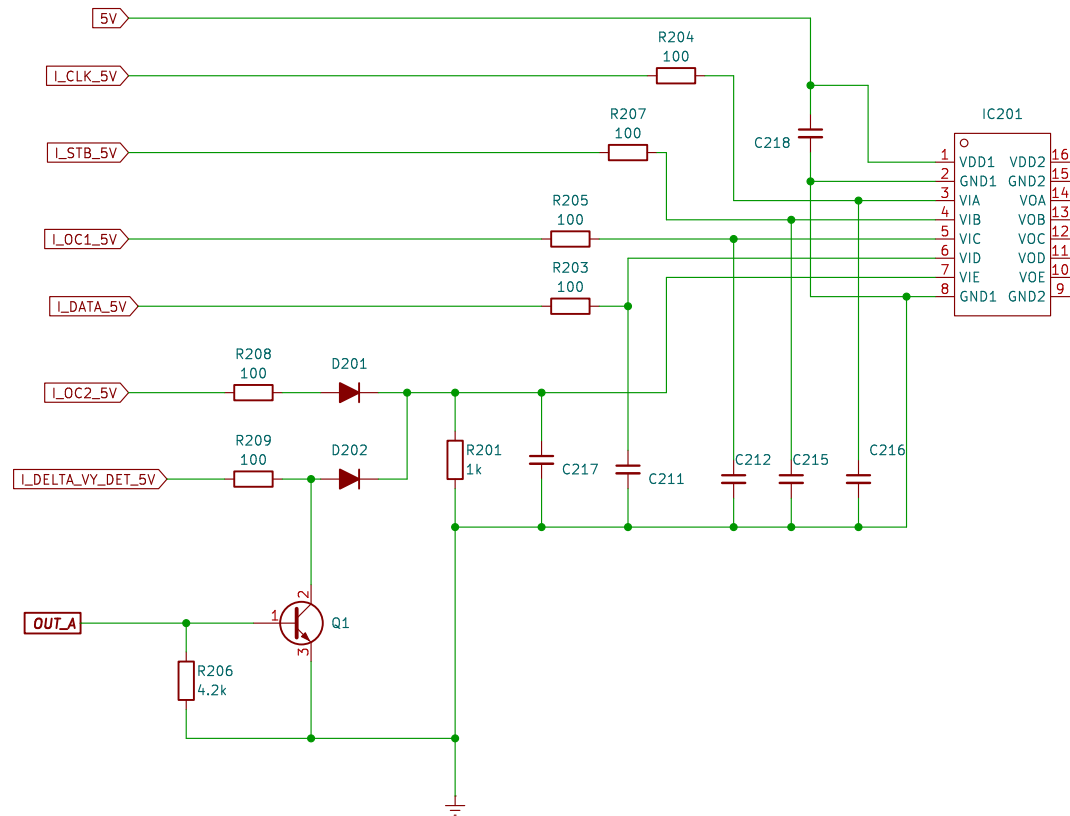
Date: 2025-03-24

Rev: 1.0

KiCad E.D.A. 8.0.9

Id: 14/15

OUTPUT CONTROL (Part 2 of 3)



Output control (Part 2 of 3)
Author: Fábio Pereira da Silva

Sheet: /Output Control (Part 2 of 3)/
File: output_control2.kicad_sch

Title: Y BOARD LG PLASMA TV PANEL

Size: A4

Date: 2025-03-24

Rev: 1.0

KiCad E.D.A. 8.0.9

Id: 15/15