1 Device Summary

1.1 Features

- Highlights
  - Leading Edge Technology
    - 28nm high k metal gate (HKMG) technology
  - 504GH/s @ 1.05GHz clock rate
  - Small Footprint
    - 37.5mm x 37.5mm package
    - 1296 pins
  - Up to 4 independent Processing Units generating 168GH/s each
    - Isolated Power Plane
    - Core Voltage Sense Lines
    - Motorola compatible SPI port
    - 128 deep Input Work FIFO
    - 128 deep Output Status FIFO
    - 120 parallel dual SHA-256 fully pipelined hash engines
    - Programmable PLL with 50 MHz external oscillator
    - Thermal Diode
- Isolated Power Plane
  - 0.65V to 0.85V Input Supply
  - Each Processing Unit has a separate power plane
  - Improves overall device power distribution
  - Simplifies external DC to DC converter design
- Core Voltage Sense Lines
  - Each Processing Unit has a pair of core power sense lines
  - Sense lines are utilized by the PCB DC to DC converter power supplies to maintain proper voltage across the Processing Unit logic
- Motorola Compatible SPI Port
  - 16-bit Slave Interface
  - Chip Select per Processing Unit
  - High Throughput
    - Operates up to 40MHz
  - Mode 3 operation
  - Simple, Full duplex Interface
    - Output Status is returned as Input Commands are sent
- 128 Deep Input FIFO
  - Compact 400-bit hash command Structure (25 16-bit SPI transfers)
  - 128 entries for efficient handshake with control CPU
  - 24Kb/s required per die to keep engines fully loaded
- 128 Deep Output FIFO
  - Compact 80-bit hash status result
  - 128 entries for efficient handshake with control CPU
- 120 Parallel Hash Engines
  - Implement a highly optimized version of the SHA-256 hash algorithm defined in the FIPS-180 Secure Hash Standard
  - Completely Pipelined
    - Generates a dual hash result every clock cycle
  - Low Power/Highly Optimized Design
    - < $1mm^2$ die area/Hash Engine
    - < 600mW/ Hash Engine @ 1.1GHz clock rate
- Programmable PLL
  - Separate PLL Control Bus
    - Clock/data Interface allows a flexible software bit bang communication interface
  - Programmable Operating Frequency
    - 0.5GHz to 1.75GHz[1][2]

[1] The maximum specified Operating Frequency is 1.1GHz. The device may be overclocked as long as the maximum junction temperature is not exceeded.

  - Processing Unit is automatically reset when PLL parameters change and held in reset until PLL is stable
- Thermal Diode
  - Utilized for Remote Temperature Sensing
  - Compatible with discrete components 2N3906, 2N3904
  - Interfaces with Industry standard Temperature Sensor devices

1.2 Applications

- Bitcoin Mining
- Cryptocurrency
- Hash Offload Engine

[2] Some operational errors may occur if internal timing requirements are violated during over clocking.

1.3 Description

The Goldstrike1™ high performance Hash Engine executes the hashing algorithms of the Bitcoin transaction protocol. The protocol requires pair of SHA-256 hashes and a comparison of that result to a given target. The successful target result is then verified by the transaction protocol.

This hashing can be accomplished in software, but current CPU architectures are incapable of attaining the hash rates required. Goldstrike1™ performs the hashes to offload the CPU to execute the Bitcoin protocol and other necessary functions of a complete mining solution.

Since the Goldstrike1™ does not directly decode the Bitcoin protocol, a local processing entity is required to create work for the hash engines. Goldstrike1™ has been designed to interface with available software mining packages. Communication occurs through custom device drivers written for these software packages.

1.4 Functional Block Diagram

The Goldstrike1™ functional block diagram is shown in Figure 1-1. Each Goldstrike1™ contains up to 4 independent Processing Units (PU). Each PU contains a SPI Interface, Input FIFO, Output FIFO and 120 Hash Engines.

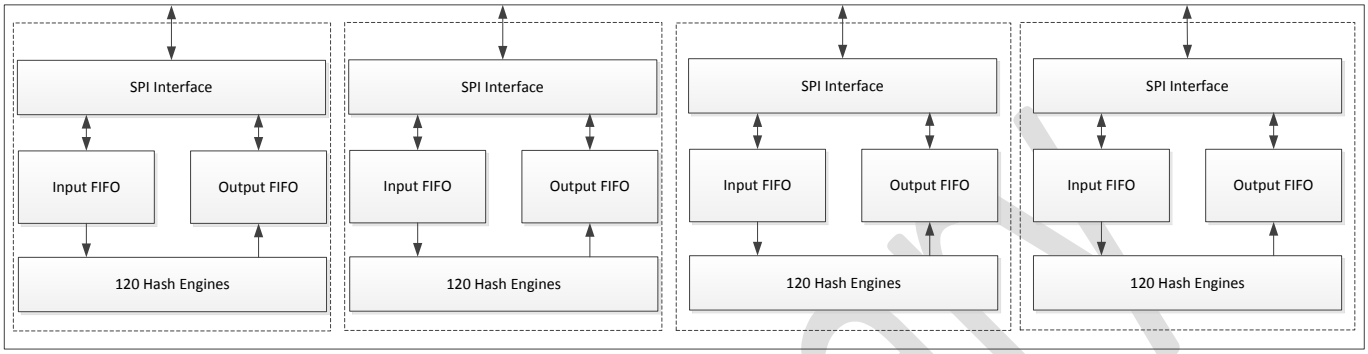

Figure 1-1. Goldstrike1™ Functional Block Diagram

1.5 Work Flow

The Goldstrike1™ accepts Bitcoin Block-headers from the CPU via the SPI Interfaces. Headers are stored in the Input FIFO until Hash Engines are ready to work on them. Once work is complete, Hash result packets are placed into the Output FIFOs. The CPU collects the results through the SPI Interface.

1.5.1 Work Order

From a Hash Engines perspective, *i.e.,* just following the Input FIFO, work arrives as packets, each corresponding exactly to a single Block-header problem to work on. Although work necessarily arrives in a given order, the time to solve a given Block-header problem may not be the same[3] when a given Block header has a solution and another does not or simply has a solution that took longer to encounter. When this occurs, it is possible for work packets received later to generate result packets that are generated earlier. In other words, input and output are **not** guaranteed to be ordered.

Internally, work is assigned by the Input FIFO to the lowest-numbered Hash Engine that is ready. Note that Engines may be disabled and as a consequence, in a lightly loaded scenario, the same few Engines would repeatedly receive work—there is no round-robin concept. During fully loaded operation, which is the intended scenario, all Engines will necessarily be busy because the rate of input work packets transferred to the Input FIFO will equal to or exceed the total number of available Engines.

Despite the likelihood of out-of-order results, the correlation of output packet to input packet is guaranteed by a 32-bit tag that is maintained throughout the processing.

[3] The time for a hash engine to compute a Block-header problem will most often be 2^{32} internal clock cycles plus a small time for filling the pipeline. This time is a result of most block header problems not containing a nonce solution.

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Revision History

	Changes for Revision B (November 2013)	Page
▪	Updated for 4-die pinout	all
	Changes for Revision C (May 2014)	
▪	Added additional PLL frequencies to Table 4-3	37

2 Terminal Description

2.1 Pin Assignments

2.1.1 1296 pin FCBGA

- 37.5mm x 37.5mm

2.2 Pin Maps

In the following pin maps, signals attached to a particular die are defined as follows:

<signal_name>_# - where # is 1 through 4 indicating the die #.

For example SPI_RXD_4 is the SPI_RXD signal on die #4.

Note: *not all dies are populated. Check the Part Number to see how many dies are populated. If one die is populated, it will utilize the _1 pins, 2 dies will utilize the _1 and _2 pins, and so on.*

Table 2-1 FCBGA Pin Map by Pin Location

Pin	Name	Direction	Description
A1	VSS	Supply	Ground
A2	VSS	Supply	Ground
A3	TEST_GPIO[46]_4		Test Pin (leave floating)
A4	TEST_GPIO[49]_4		Test Pin (leave floating)
A5	DBG_HEART_BEAT_4	Output	Heart Beat. Toggles once per second @ 1GHz
A6	SPI_RXD_4	Input	SPI Receive Data
A7	VDDIO_4	Supply	IO VDD (3.3V)
A8	PLL_CFG_CLK_4	Input	PLL Config Bus Clock
A9	PLL_BYPASS_IN_4	Input	PLL Clock Bypass
A10	VSS	Supply	Ground
A11	VDD_TOP_4	Supply	Core VDD (0.85V)
A12	VSS	Supply	Ground
A13	TEST_GPIO[56]_4		Test Pin (leave floating)
A14	TEST_GPIO[57]_4		Test Pin (leave floating)
A15	TEST_GPIO[62]_4		Test Pin (leave floating)
A16	TEST_GPIO[61]_4		Test Pin (leave floating)
A17	VDDIO_4	Supply	IO VDD (3.3V)
A18	TEST_GPIO[68]_4		Test Pin (leave floating)
A19	VSS	Supply	Ground
A20	TEST_GPIO[3]_3		Test Pin (leave floating)
A21	TEST_GPIO[5]_3		Test Pin (leave floating)
A22	TEST_GPIO[9]_3		Test Pin (leave floating)
A23	TEST_GPIO[14]_3		Test Pin (leave floating)
A24	VDDIO_3	Supply	IO VDD (3.3V)
A25	JTG_TMS_3	Input	JTAG Test Mode Select
A26	JTG_TDI_3	Input	JTAG Test Data Input
A27	TEST_GPIO[17]_3		Test Pin (leave floating)
A28	TEST_GPIO[21]_3		Test Pin (leave floating)
A29	VSS	Supply	Ground
A30	TEST_GPIO[28]_3		Test Pin (leave floating)
A31	TEST_GPIO[30]_3		Test Pin (leave floating)
A32	TEST_GPIO[31]_3		Test Pin (leave floating)
A33	TEST_GPIO[35]_3		Test Pin (leave floating)
A34	VDDIO_3	Supply	IO VDD (3.3V)
A35	VSS	Supply	Ground

A36	VSS	Supply	Ground
B1	VSS	Supply	Ground
B2	TEST_GPIO[42]_4		Test Pin (leave floating)
B3	TEST_GPIO[45]_4		Test Pin (leave floating)
B4	VDDIO_4	Supply	IO VDD (3.3V)
B5	TEST_GPIO[48]_4		Test Pin (leave floating)
B6	TEST_GPIO[51]_4		Test Pin (leave floating)
B7	SPI_SCLK_IN_4	Input	SPI Clock
B8	RESET_COLD_L_4	Input	Hard Reset, Active Low
B9	VSS	Supply	Ground
B10	DBG_PLL_RFSLIP_4	Output	PLL Reference Cycle Slip
B11	ANAVSS_DIO_4	Analog	Thermal Diode Cathode
B12	DBG_SPARE[1]_4		Spare (leave floating)
B13	TEST_GPIO[53]_4		Test Pin (leave floating)
B14	VDDIO_4	Supply	IO VDD (3.3V)
B15	TEST_GPIO[60]_4		Test Pin (leave floating)
B16	TEST_GPIO[63]_4		Test Pin (leave floating)
B17	TEST_GPIO[66]_4		Test Pin (leave floating)
B18	TEST_GPIO[70]_4		Test Pin (leave floating)
B19	TEST_GPIO[0]_3		Test Pin (leave floating)
B20	TEST_GPIO[1]_3		Test Pin (leave floating)
B21	VDDIO_3	Supply	IO VDD (3.3V)
B22	TEST_GPIO[10]_3		Test Pin (leave floating)
B23	TEST_GPIO[12]_3		Test Pin (leave floating)
B24	TEST_GPIO[13]_3		Test Pin (leave floating)
B25	JTG_TRST_L_3	Input	JTAG Test Reset
B26	VSS	Supply	Ground
B27	TEST_GPIO[18]_3		Test Pin (leave floating)
B28	TEST_GPIO[22]_3		Test Pin (leave floating)
B29	TEST_GPIO[23]_3		Test Pin (leave floating)
B30	TEST_GPIO[27]_3		Test Pin (leave floating)
B31	VDDIO_3	Supply	IO VDD (3.3V)
B32	VSS	Supply	Ground
B33	TEST_GPIO[36]_3		Test Pin (leave floating)
B34	TEST_GPIO[38]_3		Test Pin (leave floating)
B35	TEST_GPIO[42]_3		Test Pin (leave floating)
B36	VSS	Supply	Ground
C1	VDDIO_4	Supply	IO VDD (3.3V)
C2	TEST_GPIO[38]_4		Test Pin (leave floating)
C3	TEST_GPIO[40]_4		Test Pin (leave floating)
C4	TEST_GPIO[41]_4		Test Pin (leave floating)
C5	TEST_GPIO[44]_4		Test Pin (leave floating)
C6	VSS	Supply	Ground
C7	TEST_GPIO[50]_4		Test Pin (leave floating)
C8	SPI_SS_IN_L_4	Input	SPI Chip Select
C9	DBG_PLL_FBSLIP_4	Output	PLL Feedback Cycle Slip
C10	PLL_CFG_DAT_4	Input	PLL Config Bus Data
C11	VDDIO_4	Supply	IO VDD (3.3V)
C12	DBG_SPARE[0]_4		Spare (leave floating)
C13	TEST_GPIO[52]_4		Test Pin (leave floating)
C14	TEST_GPIO[54]_4		Test Pin (leave floating)
C15	TEST_GPIO[58]_4		Test Pin (leave floating)
C16	VSS	Supply	Ground
C17	TEST_GPIO[65]_4		Test Pin (leave floating)
C18	TEST_GPIO[69]_4		Test Pin (leave floating)
C19	VSS	Supply	Ground

C20	TEST_GPIO[2]_3		Test Pin (leave floating)
C21	TEST_GPIO[6]_3		Test Pin (leave floating)
C22	TEST_GPIO[8]_3		Test Pin (leave floating)
C23	VSS	Supply	Ground
C24	TEST_GPIO[15]_3		Test Pin (leave floating)
C25	JTG_TDO_3	Output-TS	JTAG Test Data Output
C26	TEST_GPIO[16]_3		Test Pin (leave floating)
C27	TEST_GPIO[20]_3		Test Pin (leave floating)
C28	VDDIO_3	Supply	IO VDD (3.3V)
C29	TEST_GPIO[25]_3		Test Pin (leave floating)
C30	TEST_GPIO[29]_3		Test Pin (leave floating)
C31	TEST_GPIO[32]_3		Test Pin (leave floating)
C32	VDDIO_3	Supply	IO VDD (3.3V)
C33	VSS	Supply	Ground
C34	TEST_GPIO[40]_3		Test Pin (leave floating)
C35	TEST_GPIO[45]_3		Test Pin (leave floating)
C36	TEST_GPIO[46]_3		Test Pin (leave floating)
D1	TEST_GPIO[35]_4		Test Pin (leave floating)
D2	TEST_GPIO[36]_4		Test Pin (leave floating)
D3	VSS	Supply	Ground
D4	TEST_GPIO[37]_4		Test Pin (leave floating)
D5	TEST_GPIO[39]_4		Test Pin (leave floating)
D6	TEST_GPIO[43]_4		Test Pin (leave floating)
D7	TEST_GPIO[47]_4		Test Pin (leave floating)
D8	VDDIO_4	Supply	IO VDD (3.3V)
D9	SPI_TXD_4	Output-TS	SPI Transmit Data
D10	DBG_PLL_LOST_LOCK_4	Output	PLL Lost Lock
D11	PLL_REF_CLK_4	Input	PLL Reference Clock
D12	ANAVDD_DIO_4	Analog	Thermal Diode Anode
D13	VSS	Supply	Ground
D14	TEST_GPIO[55]_4		Test Pin (leave floating)
D15	TEST_GPIO[59]_4		Test Pin (leave floating)
D16	TEST_GPIO[64]_4		Test Pin (leave floating)
D17	TEST_GPIO[67]_4		Test Pin (leave floating)
D18	VDDIO_4	Supply	IO VDD (3.3V)
D19	VDD_TOP_3	Supply	Core VDD (0.85V)
D20	VSS	Supply	Ground
D21	TEST_GPIO[4]_3		Test Pin (leave floating)
D22	TEST_GPIO[7]_3		Test Pin (leave floating)
D23	TEST_GPIO[11]_3		Test Pin (leave floating)
D24	TEST_MODE_3	Input	Test Mode
D25	VDDIO_3	Supply	IO VDD (3.3V)
D26	JTG_TCK_3	Input	JTAG Test Clock
D27	TEST_GPIO[19]_3		Test Pin (leave floating)
D28	TEST_GPIO[24]_3		Test Pin (leave floating)
D29	TEST_GPIO[26]_3		Test Pin (leave floating)
D30	VSS	Supply	Ground
D31	TEST_GPIO[33]_3		Test Pin (leave floating)
D32	TEST_GPIO[34]_3		Test Pin (leave floating)
D33	TEST_GPIO[37]_3		Test Pin (leave floating)
D34	TEST_GPIO[41]_3		Test Pin (leave floating)
D35	VDDIO_3	Supply	IO VDD (3.3V)
D36	TEST_GPIO[49]_3		Test Pin (leave floating)
E1	TEST_GPIO[31]_4		Test Pin (leave floating)
E2	VSS	Supply	Ground
E3	VDDIO_4	Supply	IO VDD (3.3V)

E4	TEST_GPIO[34]_4		Test Pin (leave floating)
E5	VDDIO_4	Supply	IO VDD (3.3V)
E6	VSS	Supply	Ground
E7	VDD_TOP_4	Supply	Core VDD (0.85V)
E8	VSS	Supply	Ground
E9	VDD_TOP_4	Supply	Core VDD (0.85V)
E10	VSS	Supply	Ground
E11	ANAVDD_PLL_4	Supply	PLL Analog VDD (0.85V)
E12	VSS	Supply	Ground
E13	VDD_TOP_4	Supply	Core VDD (0.85V)
E14	VSS	Supply	Ground
E15	VDDIO_4	Supply	IO VDD (3.3V)
E16	VSS	Supply	Ground
E17	VSS	Supply	Ground
E18	TEST_GPIO[71]_4		Test Pin (leave floating)
E19	VSS	Supply	Ground
E20	VDD_TOP_3	Supply	Core VDD (0.85V)
E21	VSS	Supply	Ground
E22	VDD_TOP_3	Supply	Core VDD (0.85V)
E23	VSS	Supply	Ground
E24	VDD_TOP_3	Supply	Core VDD (0.85V)
E25	VSS	Supply	Ground
E26	VDD_TOP_3	Supply	Core VDD (0.85V)
E27	VSS	Supply	Ground
E28	VDD_TOP_3	Supply	Core VDD (0.85V)
E29	VSS	Supply	Ground
E30	VDD_SENSE_3	Analog	Core VDD Sense
E31	VSS_SENSE_3	Analog	Core VSS Sense
E32	VDDIO_3	Supply	IO VDD (3.3V)
E33	TEST_GPIO[39]_3		Test Pin (leave floating)
E34	TEST_GPIO[44]_3		Test Pin (leave floating)
E35	TEST_GPIO[48]_3		Test Pin (leave floating)
E36	DBG_HEART_BEAT_3	Output	Heart Beat. Toggles once per second @ 1GHz
F1	TEST_GPIO[30]_4		Test Pin (leave floating)
F2	VDDIO_4	Supply	IO VDD (3.3V)
F3	TEST_GPIO[32]_4		Test Pin (leave floating)
F4	TEST_GPIO[33]_4		Test Pin (leave floating)
F5	VSS_SENSE_4	Analog	Core VSS Sense
F6	VDD_TOP_4	Supply	Core VDD (0.85V)
F7	VSS	Supply	Ground
F8	VDD_TOP_4	Supply	Core VDD (0.85V)
F9	VSS	Supply	Ground
F10	VDD_TOP_4	Supply	Core VDD (0.85V)
F11	ANAVSS_PLL_4	Supply	PLL Analog Ground
F12	VDD_TOP_4	Supply	Core VDD (0.85V)
F13	VSS	Supply	Ground
F14	VDD_TOP_4	Supply	Core VDD (0.85V)
F15	VSS	Supply	Ground
F16	VDD_TOP_4	Supply	Core VDD (0.85V)
F17	VSS	Supply	Ground
F18	VDD_TOP_4	Supply	Core VDD (0.85V)
F19	VDD_TOP_3	Supply	Core VDD (0.85V)
F20	VSS	Supply	Ground
F21	VDD_TOP_3	Supply	Core VDD (0.85V)
F22	VSS	Supply	Ground
F23	VDD_TOP_3	Supply	Core VDD (0.85V)

F24	VSS	Supply	Ground
F25	VDD_TOP_3	Supply	Core VDD (0.85V)
F26	VSS	Supply	Ground
F27	VDD_TOP_3	Supply	Core VDD (0.85V)
F28	VSS	Supply	Ground
F29	VDD_TOP_3	Supply	Core VDD (0.85V)
F30	VSS	Supply	Ground
F31	VDD_TOP_3	Supply	Core VDD (0.85V)
F32	VSS	Supply	Ground
F33	TEST_GPIO[43]_3		Test Pin (leave floating)
F34	VSS	Supply	Ground
F35	TEST_GPIO[51]_3		Test Pin (leave floating)
F36	SPI_RXD_3	Input	SPI Receive Data
G1	TEST_GPIO[28]_4		Test Pin (leave floating)
G2	TEST_GPIO[27]_4		Test Pin (leave floating)
G3	TEST_GPIO[29]_4		Test Pin (leave floating)
G4	VSS	Supply	Ground
G5	VDD_SENSE_4	Analog	Core VDD Sense
G6	VSS	Supply	Ground
G7	VDD_TOP_4	Supply	Core VDD (0.85V)
G8	VSS	Supply	Ground
G9	VDD_TOP_4	Supply	Core VDD (0.85V)
G10	VSS	Supply	Ground
G11	VDD_TOP_4	Supply	Core VDD (0.85V)
G12	VSS	Supply	Ground
G13	VDD_TOP_4	Supply	Core VDD (0.85V)
G14	VSS	Supply	Ground
G15	VDD_TOP_4	Supply	Core VDD (0.85V)
G16	VSS	Supply	Ground
G17	VDD_TOP_4	Supply	Core VDD (0.85V)
G18	VSS	Supply	Ground
G19	VSS	Supply	Ground
G20	VDD_TOP_3	Supply	Core VDD (0.85V)
G21	VSS	Supply	Ground
G22	VDD_TOP_3	Supply	Core VDD (0.85V)
G23	VSS	Supply	Ground
G24	VDD_TOP_3	Supply	Core VDD (0.85V)
G25	VSS	Supply	Ground
G26	VDD_TOP_3	Supply	Core VDD (0.85V)
G27	VSS	Supply	Ground
G28	VDD_TOP_3	Supply	Core VDD (0.85V)
G29	VSS	Supply	Ground
G30	VDD_TOP_3	Supply	Core VDD (0.85V)
G31	VSS	Supply	Ground
G32	VDD_TOP_3	Supply	Core VDD (0.85V)
G33	TEST_GPIO[47]_3		Test Pin (leave floating)
G34	TEST_GPIO[50]_3		Test Pin (leave floating)
G35	SPI_SCLK_IN_3	Input	SPI Clock
G36	VDDIO_3	Supply	IO VDD (3.3V)
H1	VSS	Supply	Ground
H2	TEST_GPIO[23]_4		Test Pin (leave floating)
H3	TEST_GPIO[25]_4		Test Pin (leave floating)
H4	TEST_GPIO[26]_4		Test Pin (leave floating)
H5	VSS	Supply	Ground
H6	VDD_TOP_4	Supply	Core VDD (0.85V)
H7	VSS	Supply	Ground

H8	VDD_TOP_4	Supply	Core VDD (0.85V)
H9	VSS	Supply	Ground
H10	VDD_TOP_4	Supply	Core VDD (0.85V)
H11	VSS	Supply	Ground
H12	VDD_TOP_4	Supply	Core VDD (0.85V)
H13	VSS	Supply	Ground
H14	VDD_TOP_4	Supply	Core VDD (0.85V)
H15	VSS	Supply	Ground
H16	VDD_TOP_4	Supply	Core VDD (0.85V)
H17	VSS	Supply	Ground
H18	VDD_TOP_4	Supply	Core VDD (0.85V)
H19	VDD_TOP_3	Supply	Core VDD (0.85V)
H20	VSS	Supply	Ground
H21	VDD_TOP_3	Supply	Core VDD (0.85V)
H22	VSS	Supply	Ground
H23	VDD_TOP_3	Supply	Core VDD (0.85V)
H24	VSS	Supply	Ground
H25	VDD_TOP_3	Supply	Core VDD (0.85V)
H26	VSS	Supply	Ground
H27	VDD_TOP_3	Supply	Core VDD (0.85V)
H28	VSS	Supply	Ground
H29	VDD_TOP_3	Supply	Core VDD (0.85V)
H30	VSS	Supply	Ground
H31	VDD_TOP_3	Supply	Core VDD (0.85V)
H32	VSS	Supply	Ground
H33	VDDIO_3	Supply	IO VDD (3.3V)
H34	SPI_SS_IN_L_3	Input	SPI Chip Select
H35	RESET_COLD_L_3	Input-Schmidt	Hard Reset, Active Low
H36	PLL_CFG_CLK_3	Input	PLL Config Bus Clock
J1	TEST_GPIO[21]_4		Test Pin (leave floating)
J2	TEST_GPIO[22]_4		Test Pin (leave floating)
J3	VDDIO_4	Supply	IO VDD (3.3V)
J4	TEST_GPIO[24]_4		Test Pin (leave floating)
J5	VDD_TOP_4	Supply	Core VDD (0.85V)
J6	VSS	Supply	Ground
J7	VDD_TOP_4	Supply	Core VDD (0.85V)
J8	VSS	Supply	Ground
J9	VDD_TOP_4	Supply	Core VDD (0.85V)
J10	VSS	Supply	Ground
J11	VDD_TOP_4	Supply	Core VDD (0.85V)
J12	VSS	Supply	Ground
J13	VDD_TOP_4	Supply	Core VDD (0.85V)
J14	VSS	Supply	Ground
J15	VDD_TOP_4	Supply	Core VDD (0.85V)
J16	VSS	Supply	Ground
J17	VDD_TOP_4	Supply	Core VDD (0.85V)
J18	VSS	Supply	Ground
J19	VSS	Supply	Ground
J20	VDD_TOP_3	Supply	Core VDD (0.85V)
J21	VSS	Supply	Ground
J22	VDD_TOP_3	Supply	Core VDD (0.85V)
J23	VSS	Supply	Ground
J24	VDD_TOP_3	Supply	Core VDD (0.85V)
J25	VSS	Supply	Ground
J26	VDD_TOP_3	Supply	Core VDD (0.85V)
J27	VSS	Supply	Ground

J28	VDD_TOP_3	Supply	Core VDD (0.85V)
J29	VSS	Supply	Ground
J30	VDD_TOP_3	Supply	Core VDD (0.85V)
J31	VSS	Supply	Ground
J32	VDD_TOP_3	Supply	Core VDD (0.85V)
J33	SPI_TXD_3	Output-TS	SPI Transmit Data
J34	DBG_PLL_FBSLIP_3	Output	PLL Feedback Cycle Slip
J35	VSS	Supply	Ground
J36	PLL_BYPASS_IN_3	Input	PLL Clock Bypass
K1	TEST_GPIO[17]_4		Test Pin (leave floating)
K2	TEST_GPIO[18]_4		Test Pin (leave floating)
K3	TEST_GPIO[20]_4		Test Pin (leave floating)
K4	TEST_GPIO[19]_4		Test Pin (leave floating)
K5	VSS	Supply	Ground
K6	VDD_TOP_4	Supply	Core VDD (0.85V)
K7	VSS	Supply	Ground
K8	VDD_TOP_4	Supply	Core VDD (0.85V)
K9	VSS	Supply	Ground
K10	VDD_TOP_4	Supply	Core VDD (0.85V)
K11	VSS	Supply	Ground
K12	VDD_TOP_4	Supply	Core VDD (0.85V)
K13	VSS	Supply	Ground
K14	VDD_TOP_4	Supply	Core VDD (0.85V)
K15	VSS	Supply	Ground
K16	VDD_TOP_4	Supply	Core VDD (0.85V)
K17	VSS	Supply	Ground
K18	VDD_TOP_4	Supply	Core VDD (0.85V)
K19	VDD_TOP_3	Supply	Core VDD (0.85V)
K20	VSS	Supply	Ground
K21	VDD_TOP_3	Supply	Core VDD (0.85V)
K22	VSS	Supply	Ground
K23	VDD_TOP_3	Supply	Core VDD (0.85V)
K24	VSS	Supply	Ground
K25	VDD_TOP_3	Supply	Core VDD (0.85V)
K26	VSS	Supply	Ground
K27	VDD_TOP_3	Supply	Core VDD (0.85V)
K28	VSS	Supply	Ground
K29	VDD_TOP_3	Supply	Core VDD (0.85V)
K30	VSS	Supply	Ground
K31	VDD_TOP_3	Supply	Core VDD (0.85V)
K32	VSS	Supply	Ground
K33	DBG_PLL_LOST_LOCK_3	Output	PLL Lost Lock
K34	PLL_CFG_DAT_3	Input	PLL Config Bus Data
K35	DBG_PLL_RFSLIP_3	Output	PLL Reference Cycle Slip
K36	VSS	Supply	Ground
L1	JTG_TDI_4	Input	JTAG Test Data Input
L2	VSS	Supply	Ground
L3	TEST_GPIO[16]_4		Test Pin (leave floating)
L4	JTG_TCK_4	Input	JTAG Test Clock
L5	VDD_TOP_4	Supply	Core VDD (0.85V)
L6	VSS	Supply	Ground
L7	VDD_TOP_4	Supply	Core VDD (0.85V)
L8	VSS	Supply	Ground
L9	VDD_TOP_4	Supply	Core VDD (0.85V)
L10	VSS	Supply	Ground
L11	VDD_TOP_4	Supply	Core VDD (0.85V)

L12	VSS	Supply	Ground
L13	VDD_TOP_4	Supply	Core VDD (0.85V)
L14	VSS	Supply	Ground
L15	VDD_TOP_4	Supply	Core VDD (0.85V)
L16	VSS	Supply	Ground
L17	VDD_TOP_4	Supply	Core VDD (0.85V)
L18	VSS	Supply	Ground
L19	VSS	Supply	Ground
L20	VDD_TOP_3	Supply	Core VDD (0.85V)
L21	VSS	Supply	Ground
L22	VDD_TOP_3	Supply	Core VDD (0.85V)
L23	VSS	Supply	Ground
L24	VDD_TOP_3	Supply	Core VDD (0.85V)
L25	VSS	Supply	Ground
L26	VDD_TOP_3	Supply	Core VDD (0.85V)
L27	VSS	Supply	Ground
L28	VDD_TOP_3	Supply	Core VDD (0.85V)
L29	VSS	Supply	Ground
L30	VDD_TOP_3	Supply	Core VDD (0.85V)
L31	ANAVSS_PLL_3	Supply	PLL Analog Ground
L32	ANAVDD_PLL_3	Supply	PLL Analog VDD (0.85V)
L33	PLL_REF_CLK_3	Input	PLL Reference Clock
L34	VDDIO_3	Supply	IO VDD (3.3V)
L35	ANAVSS_DIO_3	Analog	Thermal Diode Cathode
L36	VDD_TOP_3	Supply	Core VDD (0.85V)
M1	JTG_TMS_4	Input	JTAG Test Mode Select
M2	JTG_TRST_L_4	Input	JTAG Test Reset
M3	JTG_TDO_4	Output	JTAG Test Data Output
M4	VDDIO_4	Supply	IO VDD (3.3V)
M5	VSS	Supply	Ground
M6	VDD_TOP_4	Supply	Core VDD (0.85V)
M7	VSS	Supply	Ground
M8	VDD_TOP_4	Supply	Core VDD (0.85V)
M9	VSS	Supply	Ground
M10	VDD_TOP_4	Supply	Core VDD (0.85V)
M11	VSS	Supply	Ground
M12	VDD_TOP_4	Supply	Core VDD (0.85V)
M13	VSS	Supply	Ground
M14	VDD_TOP_4	Supply	Core VDD (0.85V)
M15	VSS	Supply	Ground
M16	VDD_TOP_4	Supply	Core VDD (0.85V)
M17	VSS	Supply	Ground
M18	VDD_TOP_4	Supply	Core VDD (0.85V)
M19	VDD_TOP_3	Supply	Core VDD (0.85V)
M20	VSS	Supply	Ground
M21	VDD_TOP_3	Supply	Core VDD (0.85V)
M22	VSS	Supply	Ground
M23	VDD_TOP_3	Supply	Core VDD (0.85V)
M24	VSS	Supply	Ground
M25	VDD_TOP_3	Supply	Core VDD (0.85V)
M26	VSS	Supply	Ground
M27	VDD_TOP_3	Supply	Core VDD (0.85V)
M28	VSS	Supply	Ground
M29	VDD_TOP_3	Supply	Core VDD (0.85V)
M30	VSS	Supply	Ground
M31	VDD_TOP_3	Supply	Core VDD (0.85V)

M32	VSS	Supply	Ground
M33	ANAVDD_DIO_3	Analog	Thermal Diode Anode
M34	DBG_SPARE[0]_3		Spare (leave floating)
M35	DBG_SPARE[1]_3		Spare (leave floating)
M36	VSS	Supply	Ground
N1	VDDIO_4	Supply	IO VDD (3.3V)
N2	TEST_GPIO[13]_4		Test Pin (leave floating)
N3	TEST_GPIO[15]_4		Test Pin (leave floating)
N4	TEST_MODE_4	Input	Test Mode
N5	VDD_TOP_4	Supply	Core VDD (0.85V)
N6	VSS	Supply	Ground
N7	VDD_TOP_4	Supply	Core VDD (0.85V)
N8	VSS	Supply	Ground
N9	VDD_TOP_4	Supply	Core VDD (0.85V)
N10	VSS	Supply	Ground
N11	VDD_TOP_4	Supply	Core VDD (0.85V)
N12	VSS	Supply	Ground
N13	VDD_TOP_4	Supply	Core VDD (0.85V)
N14	VSS	Supply	Ground
N15	VDD_TOP_4	Supply	Core VDD (0.85V)
N16	VSS	Supply	Ground
N17	VDD_TOP_4	Supply	Core VDD (0.85V)
N18	VSS	Supply	Ground
N19	VSS	Supply	Ground
N20	VDD_TOP_3	Supply	Core VDD (0.85V)
N21	VSS	Supply	Ground
N22	VDD_TOP_3	Supply	Core VDD (0.85V)
N23	VSS	Supply	Ground
N24	VDD_TOP_3	Supply	Core VDD (0.85V)
N25	VSS	Supply	Ground
N26	VDD_TOP_3	Supply	Core VDD (0.85V)
N27	VSS	Supply	Ground
N28	VDD_TOP_3	Supply	Core VDD (0.85V)
N29	VSS	Supply	Ground
N30	VDD_TOP_3	Supply	Core VDD (0.85V)
N31	VSS	Supply	Ground
N32	VDD_TOP_3	Supply	Core VDD (0.85V)
N33	VSS	Supply	Ground
N34	TEST_GPIO[52]_3		Test Pin (leave floating)
N35	TEST_GPIO[53]_3		Test Pin (leave floating)
N36	TEST_GPIO[56]_3		Test Pin (leave floating)
P1	TEST_GPIO[14]_4		Test Pin (leave floating)
P2	TEST_GPIO[12]_4		Test Pin (leave floating)
P3	VSS	Supply	Ground
P4	TEST_GPIO[11]_4		Test Pin (leave floating)
P5	VSS	Supply	Ground
P6	VDD_TOP_4	Supply	Core VDD (0.85V)
P7	VSS	Supply	Ground
P8	VDD_TOP_4	Supply	Core VDD (0.85V)
P9	VSS	Supply	Ground
P10	VDD_TOP_4	Supply	Core VDD (0.85V)
P11	VSS	Supply	Ground
P12	VDD_TOP_4	Supply	Core VDD (0.85V)
P13	VSS	Supply	Ground
P14	VDD_TOP_4	Supply	Core VDD (0.85V)
P15	VSS	Supply	Ground

P16	VDD_TOP_4	Supply	Core VDD (0.85V)
P17	VSS	Supply	Ground
P18	VDD_TOP_4	Supply	Core VDD (0.85V)
P19	VDD_TOP_3	Supply	Core VDD (0.85V)
P20	VSS	Supply	Ground
P21	VDD_TOP_3	Supply	Core VDD (0.85V)
P22	VSS	Supply	Ground
P23	VDD_TOP_3	Supply	Core VDD (0.85V)
P24	VSS	Supply	Ground
P25	VDD_TOP_3	Supply	Core VDD (0.85V)
P26	VSS	Supply	Ground
P27	VDD_TOP_3	Supply	Core VDD (0.85V)
P28	VSS	Supply	Ground
P29	VDD_TOP_3	Supply	Core VDD (0.85V)
P30	VSS	Supply	Ground
P31	VDD_TOP_3	Supply	Core VDD (0.85V)
P32	VSS	Supply	Ground
P33	TEST_GPIO[55]_3		Test Pin (leave floating)
P34	TEST_GPIO[54]_3		Test Pin (leave floating)
P35	VDDIO_3	Supply	IO VDD (3.3V)
P36	TEST_GPIO[57]_3		Test Pin (leave floating)
R1	TEST_GPIO[9]_4		Test Pin (leave floating)
R2	TEST_GPIO[10]_4		Test Pin (leave floating)
R3	TEST_GPIO[8]_4		Test Pin (leave floating)
R4	TEST_GPIO[7]_4		Test Pin (leave floating)
R5	VDD_TOP_4	Supply	Core VDD (0.85V)
R6	VSS	Supply	Ground
R7	VDD_TOP_4	Supply	Core VDD (0.85V)
R8	VSS	Supply	Ground
R9	VDD_TOP_4	Supply	Core VDD (0.85V)
R10	VSS	Supply	Ground
R11	VDD_TOP_4	Supply	Core VDD (0.85V)
R12	VSS	Supply	Ground
R13	VDD_TOP_4	Supply	Core VDD (0.85V)
R14	VSS	Supply	Ground
R15	VDD_TOP_4	Supply	Core VDD (0.85V)
R16	VSS	Supply	Ground
R17	VDD_TOP_4	Supply	Core VDD (0.85V)
R18	VSS	Supply	Ground
R19	VSS	Supply	Ground
R20	VDD_TOP_3	Supply	Core VDD (0.85V)
R21	VSS	Supply	Ground
R22	VDD_TOP_3	Supply	Core VDD (0.85V)
R23	VSS	Supply	Ground
R24	VDD_TOP_3	Supply	Core VDD (0.85V)
R25	VSS	Supply	Ground
R26	VDD_TOP_3	Supply	Core VDD (0.85V)
R27	VSS	Supply	Ground
R28	VDD_TOP_3	Supply	Core VDD (0.85V)
R29	VSS	Supply	Ground
R30	VDD_TOP_3	Supply	Core VDD (0.85V)
R31	VSS	Supply	Ground
R32	VDDIO_3	Supply	IO VDD (3.3V)
R33	TEST_GPIO[59]_3		Test Pin (leave floating)
R34	TEST_GPIO[58]_3		Test Pin (leave floating)
R35	TEST_GPIO[60]_3		Test Pin (leave floating)

R36	TEST_GPIO[62]_3		Test Pin (leave floating)
T1	TEST_GPIO[5]_4		Test Pin (leave floating)
T2	VDDIO_4	Supply	IO VDD (3.3V)
T3	TEST_GPIO[6]_4		Test Pin (leave floating)
T4	TEST_GPIO[4]_4		Test Pin (leave floating)
T5	VSS	Supply	Ground
T6	VDD_TOP_4	Supply	Core VDD (0.85V)
T7	VSS	Supply	Ground
T8	VDD_TOP_4	Supply	Core VDD (0.85V)
T9	VSS	Supply	Ground
T10	VDD_TOP_4	Supply	Core VDD (0.85V)
T11	VSS	Supply	Ground
T12	VDD_TOP_4	Supply	Core VDD (0.85V)
T13	VSS	Supply	Ground
T14	VDD_TOP_4	Supply	Core VDD (0.85V)
T15	VSS	Supply	Ground
T16	VDD_TOP_4	Supply	Core VDD (0.85V)
T17	VSS	Supply	Ground
T18	VDD_TOP_4	Supply	Core VDD (0.85V)
T19	VDD_TOP_3	Supply	Core VDD (0.85V)
T20	VSS	Supply	Ground
T21	VDD_TOP_3	Supply	Core VDD (0.85V)
T22	VSS	Supply	Ground
T23	VDD_TOP_3	Supply	Core VDD (0.85V)
T24	VSS	Supply	Ground
T25	VDD_TOP_3	Supply	Core VDD (0.85V)
T26	VSS	Supply	Ground
T27	VDD_TOP_3	Supply	Core VDD (0.85V)
T28	VSS	Supply	Ground
T29	VDD_TOP_3	Supply	Core VDD (0.85V)
T30	VSS	Supply	Ground
T31	VDD_TOP_3	Supply	Core VDD (0.85V)
T32	VSS	Supply	Ground
T33	TEST_GPIO[64]_3		Test Pin (leave floating)
T34	VSS	Supply	Ground
T35	TEST_GPIO[63]_3		Test Pin (leave floating)
T36	TEST_GPIO[61]_3		Test Pin (leave floating)
U1	TEST_GPIO[3]_4		Test Pin (leave floating)
U2	TEST_GPIO[1]_4		Test Pin (leave floating)
U3	TEST_GPIO[2]_4		Test Pin (leave floating)
U4	VSS	Supply	Ground
U5	VDD_TOP_4	Supply	Core VDD (0.85V)
U6	VSS	Supply	Ground
U7	VDD_TOP_4	Supply	Core VDD (0.85V)
U8	VSS	Supply	Ground
U9	VDD_TOP_4	Supply	Core VDD (0.85V)
U10	VSS	Supply	Ground
U11	VDD_TOP_4	Supply	Core VDD (0.85V)
U12	VSS	Supply	Ground
U13	VDD_TOP_4	Supply	Core VDD (0.85V)
U14	VSS	Supply	Ground
U15	VDD_TOP_4	Supply	Core VDD (0.85V)
U16	VSS	Supply	Ground
U17	VDD_TOP_4	Supply	Core VDD (0.85V)
U18	VSS	Supply	Ground
U19	VSS	Supply	Ground

U20	VDD_TOP_3	Supply	Core VDD (0.85V)
U21	VSS	Supply	Ground
U22	VDD_TOP_3	Supply	Core VDD (0.85V)
U23	VSS	Supply	Ground
U24	VDD_TOP_3	Supply	Core VDD (0.85V)
U25	VSS	Supply	Ground
U26	VDD_TOP_3	Supply	Core VDD (0.85V)
U27	VSS	Supply	Ground
U28	VDD_TOP_3	Supply	Core VDD (0.85V)
U29	VSS	Supply	Ground
U30	VDD_TOP_3	Supply	Core VDD (0.85V)
U31	VSS	Supply	Ground
U32	VSS	Supply	Ground
U33	TEST_GPIO[67]_3		Test Pin (leave floating)
U34	TEST_GPIO[65]_3		Test Pin (leave floating)
U35	TEST_GPIO[66]_3		Test Pin (leave floating)
U36	VDDIO_3	Supply	IO VDD (3.3V)
V1	VSS	Supply	Ground
V2	TEST_GPIO[0]_4		Test Pin (leave floating)
V3	VSS	Supply	Ground
V4	VDD_TOP_4	Supply	Core VDD (0.85V)
V5	VSS	Supply	Ground
V6	VDD_TOP_4	Supply	Core VDD (0.85V)
V7	VSS	Supply	Ground
V8	VDD_TOP_4	Supply	Core VDD (0.85V)
V9	VSS	Supply	Ground
V10	VDD_TOP_4	Supply	Core VDD (0.85V)
V11	VSS	Supply	Ground
V12	VDD_TOP_4	Supply	Core VDD (0.85V)
V13	VSS	Supply	Ground
V14	VDD_TOP_4	Supply	Core VDD (0.85V)
V15	VSS	Supply	Ground
V16	VDD_TOP_4	Supply	Core VDD (0.85V)
V17	VSS	Supply	Ground
V18	VDD_TOP_4	Supply	Core VDD (0.85V)
V19	VDD_TOP_3	Supply	Core VDD (0.85V)
V20	VSS	Supply	Ground
V21	VDD_TOP_3	Supply	Core VDD (0.85V)
V22	VSS	Supply	Ground
V23	VDD_TOP_3	Supply	Core VDD (0.85V)
V24	VSS	Supply	Ground
V25	VDD_TOP_3	Supply	Core VDD (0.85V)
V26	VSS	Supply	Ground
V27	VDD_TOP_3	Supply	Core VDD (0.85V)
V28	VSS	Supply	Ground
V29	VDD_TOP_3	Supply	Core VDD (0.85V)
V30	VSS	Supply	Ground
V31	VDD_TOP_3	Supply	Core VDD (0.85V)
V32	TEST_GPIO[71]_3		Test Pin (leave floating)
V33	VDDIO_3	Supply	IO VDD (3.3V)
V34	TEST_GPIO[69]_3		Test Pin (leave floating)
V35	TEST_GPIO[70]_3		Test Pin (leave floating)
V36	TEST_GPIO[68]_3		Test Pin (leave floating)
W1	TEST_GPIO[68]_1		Test Pin (leave floating)
W2	TEST_GPIO[70]_1		Test Pin (leave floating)
W3	TEST_GPIO[69]_1		Test Pin (leave floating)

W4	VDDIO_1	Supply	IO VDD (3.3V)
W5	TEST_GPIO[71]_1		Test Pin (leave floating)
W6	VDD_TOP_1	Supply	Core VDD (0.85V)
W7	VSS	Supply	Ground
W8	VDD_TOP_1	Supply	Core VDD (0.85V)
W9	VSS	Supply	Ground
W10	VDD_TOP_1	Supply	Core VDD (0.85V)
W11	VSS	Supply	Ground
W12	VDD_TOP_1	Supply	Core VDD (0.85V)
W13	VSS	Supply	Ground
W14	VDD_TOP_1	Supply	Core VDD (0.85V)
W15	VSS	Supply	Ground
W16	VDD_TOP_1	Supply	Core VDD (0.85V)
W17	VSS	Supply	Ground
W18	VDD_TOP_1	Supply	Core VDD (0.85V)
W19	VDD_TOP_2	Supply	Core VDD (0.85V)
W20	VSS	Supply	Ground
W21	VDD_TOP_2	Supply	Core VDD (0.85V)
W22	VSS	Supply	Ground
W23	VDD_TOP_2	Supply	Core VDD (0.85V)
W24	VSS	Supply	Ground
W25	VDD_TOP_2	Supply	Core VDD (0.85V)
W26	VSS	Supply	Ground
W27	VDD_TOP_2	Supply	Core VDD (0.85V)
W28	VSS	Supply	Ground
W29	VDD_TOP_2	Supply	Core VDD (0.85V)
W30	VSS	Supply	Ground
W31	VDD_TOP_2	Supply	Core VDD (0.85V)
W32	VSS	Supply	Ground
W33	VDD_TOP_2	Supply	Core VDD (0.85V)
W34	VSS	Supply	Ground
W35	TEST_GPIO[0]_2		Test Pin (leave floating)
W36	VSS	Supply	Ground
Y1	VDDIO_1	Supply	IO VDD (3.3V)
Y2	TEST_GPIO[66]_1		Test Pin (leave floating)
Y3	TEST_GPIO[65]_1		Test Pin (leave floating)
Y4	TEST_GPIO[67]_1		Test Pin (leave floating)
Y5	VSS	Supply	Ground
Y6	VSS	Supply	Ground
Y7	VDD_TOP_1	Supply	Core VDD (0.85V)
Y8	VSS	Supply	Ground
Y9	VDD_TOP_1	Supply	Core VDD (0.85V)
Y10	VSS	Supply	Ground
Y11	VDD_TOP_1	Supply	Core VDD (0.85V)
Y12	VSS	Supply	Ground
Y13	VDD_TOP_1	Supply	Core VDD (0.85V)
Y14	VSS	Supply	Ground
Y15	VDD_TOP_1	Supply	Core VDD (0.85V)
Y16	VSS	Supply	Ground
Y17	VDD_TOP_1	Supply	Core VDD (0.85V)
Y18	VSS	Supply	Ground
Y19	VSS	Supply	Ground
Y20	VDD_TOP_2	Supply	Core VDD (0.85V)
Y21	VSS	Supply	Ground
Y22	VDD_TOP_2	Supply	Core VDD (0.85V)
Y23	VSS	Supply	Ground

Y24	VDD_TOP_2	Supply	Core VDD (0.85V)
Y25	VSS	Supply	Ground
Y26	VDD_TOP_2	Supply	Core VDD (0.85V)
Y27	VSS	Supply	Ground
Y28	VDD_TOP_2	Supply	Core VDD (0.85V)
Y29	VSS	Supply	Ground
Y30	VDD_TOP_2	Supply	Core VDD (0.85V)
Y31	VSS	Supply	Ground
Y32	VDD_TOP_2	Supply	Core VDD (0.85V)
Y33	VSS	Supply	Ground
Y34	TEST_GPIO[2]_2		Test Pin (leave floating)
Y35	TEST_GPIO[1]_2		Test Pin (leave floating)
Y36	TEST_GPIO[3]_2		Test Pin (leave floating)
AA1	TEST_GPIO[61]_1		Test Pin (leave floating)
AA2	TEST_GPIO[63]_1		Test Pin (leave floating)
AA3	VSS	Supply	Ground
AA4	TEST_GPIO[64]_1		Test Pin (leave floating)
AA5	VSS	Supply	Ground
AA6	VDD_TOP_1	Supply	Core VDD (0.85V)
AA7	VSS	Supply	Ground
AA8	VDD_TOP_1	Supply	Core VDD (0.85V)
AA9	VSS	Supply	Ground
AA10	VDD_TOP_1	Supply	Core VDD (0.85V)
AA11	VSS	Supply	Ground
AA12	VDD_TOP_1	Supply	Core VDD (0.85V)
AA13	VSS	Supply	Ground
AA14	VDD_TOP_1	Supply	Core VDD (0.85V)
AA15	VSS	Supply	Ground
AA16	VDD_TOP_1	Supply	Core VDD (0.85V)
AA17	VSS	Supply	Ground
AA18	VDD_TOP_1	Supply	Core VDD (0.85V)
AA19	VDD_TOP_2	Supply	Core VDD (0.85V)
AA20	VSS	Supply	Ground
AA21	VDD_TOP_2	Supply	Core VDD (0.85V)
AA22	VSS	Supply	Ground
AA23	VDD_TOP_2	Supply	Core VDD (0.85V)
AA24	VSS	Supply	Ground
AA25	VDD_TOP_2	Supply	Core VDD (0.85V)
AA26	VSS	Supply	Ground
AA27	VDD_TOP_2	Supply	Core VDD (0.85V)
AA28	VSS	Supply	Ground
AA29	VDD_TOP_2	Supply	Core VDD (0.85V)
AA30	VSS	Supply	Ground
AA31	VDD_TOP_2	Supply	Core VDD (0.85V)
AA32	VSS	Supply	Ground
AA33	TEST_GPIO[4]_2		Test Pin (leave floating)
AA34	TEST_GPIO[6]_2		Test Pin (leave floating)
AA35	VDDIO_2	Supply	IO VDD (3.3V)
AA36	TEST_GPIO[5]_2		Test Pin (leave floating)
AB1	TEST_GPIO[62]_1		Test Pin (leave floating)
AB2	TEST_GPIO[60]_1		Test Pin (leave floating)
AB3	TEST_GPIO[58]_1		Test Pin (leave floating)
AB4	TEST_GPIO[59]_1		Test Pin (leave floating)
AB5	VDDIO_1	Supply	IO VDD (3.3V)
AB6	VSS	Supply	Ground
AB7	VDD_TOP_1	Supply	Core VDD (0.85V)

AB8	VSS	Supply	Ground
AB9	VDD_TOP_1	Supply	Core VDD (0.85V)
AB10	VSS	Supply	Ground
AB11	VDD_TOP_1	Supply	Core VDD (0.85V)
AB12	VSS	Supply	Ground
AB13	VDD_TOP_1	Supply	Core VDD (0.85V)
AB14	VSS	Supply	Ground
AB15	VDD_TOP_1	Supply	Core VDD (0.85V)
AB16	VSS	Supply	Ground
AB17	VDD_TOP_1	Supply	Core VDD (0.85V)
AB18	VSS	Supply	Ground
AB19	VSS	Supply	Ground
AB20	VDD_TOP_2	Supply	Core VDD (0.85V)
AB21	VSS	Supply	Ground
AB22	VDD_TOP_2	Supply	Core VDD (0.85V)
AB23	VSS	Supply	Ground
AB24	VDD_TOP_2	Supply	Core VDD (0.85V)
AB25	VSS	Supply	Ground
AB26	VDD_TOP_2	Supply	Core VDD (0.85V)
AB27	VSS	Supply	Ground
AB28	VDD_TOP_2	Supply	Core VDD (0.85V)
AB29	VSS	Supply	Ground
AB30	VDD_TOP_2	Supply	Core VDD (0.85V)
AB31	VSS	Supply	Ground
AB32	VDD_TOP_2	Supply	Core VDD (0.85V)
AB33	TEST_GPIO[7]_2		Test Pin (leave floating)
AB34	TEST_GPIO[8]_2		Test Pin (leave floating)
AB35	TEST_GPIO[10]_2		Test Pin (leave floating)
AB36	TEST_GPIO[9]_2		Test Pin (leave floating)
AC1	TEST_GPIO[57]_1		Test Pin (leave floating)
AC2	VDDIO_1	Supply	IO VDD (3.3V)
AC3	TEST_GPIO[54]_1		Test Pin (leave floating)
AC4	TEST_GPIO[55]_1		Test Pin (leave floating)
AC5	VSS	Supply	Ground
AC6	VDD_TOP_1	Supply	Core VDD (0.85V)
AC7	VSS	Supply	Ground
AC8	VDD_TOP_1	Supply	Core VDD (0.85V)
AC9	VSS	Supply	Ground
AC10	VDD_TOP_1	Supply	Core VDD (0.85V)
AC11	VSS	Supply	Ground
AC12	VDD_TOP_1	Supply	Core VDD (0.85V)
AC13	VSS	Supply	Ground
AC14	VDD_TOP_1	Supply	Core VDD (0.85V)
AC15	VSS	Supply	Ground
AC16	VDD_TOP_1	Supply	Core VDD (0.85V)
AC17	VSS	Supply	Ground
AC18	VDD_TOP_1	Supply	Core VDD (0.85V)
AC19	VDD_TOP_2	Supply	Core VDD (0.85V)
AC20	VSS	Supply	Ground
AC21	VDD_TOP_2	Supply	Core VDD (0.85V)
AC22	VSS	Supply	Ground
AC23	VDD_TOP_2	Supply	Core VDD (0.85V)
AC24	VSS	Supply	Ground
AC25	VDD_TOP_2	Supply	Core VDD (0.85V)
AC26	VSS	Supply	Ground
AC27	VDD_TOP_2	Supply	Core VDD (0.85V)

AC28	VSS	Supply	Ground
AC29	VDD_TOP_2	Supply	Core VDD (0.85V)
AC30	VSS	Supply	Ground
AC31	VDD_TOP_2	Supply	Core VDD (0.85V)
AC32	VSS	Supply	Ground
AC33	TEST_GPIO[11]_2		Test Pin (leave floating)
AC34	VSS	Supply	Ground
AC35	TEST_GPIO[12]_2		Test Pin (leave floating)
AC36	TEST_GPIO[14]_2		Test Pin (leave floating)
AD1	TEST_GPIO[56]_1		Test Pin (leave floating)
AD2	TEST_GPIO[53]_1		Test Pin (leave floating)
AD3	TEST_GPIO[52]_1		Test Pin (leave floating)
AD4	VSS	Supply	Ground
AD5	VDD_TOP_1	Supply	Core VDD (0.85V)
AD6	VSS	Supply	Ground
AD7	VDD_TOP_1	Supply	Core VDD (0.85V)
AD8	VSS	Supply	Ground
AD9	VDD_TOP_1	Supply	Core VDD (0.85V)
AD10	VSS	Supply	Ground
AD11	VDD_TOP_1	Supply	Core VDD (0.85V)
AD12	VSS	Supply	Ground
AD13	VDD_TOP_1	Supply	Core VDD (0.85V)
AD14	VSS	Supply	Ground
AD15	VDD_TOP_1	Supply	Core VDD (0.85V)
AD16	VSS	Supply	Ground
AD17	VDD_TOP_1	Supply	Core VDD (0.85V)
AD18	VSS	Supply	Ground
AD19	VSS	Supply	Ground
AD20	VDD_TOP_2	Supply	Core VDD (0.85V)
AD21	VSS	Supply	Ground
AD22	VDD_TOP_2	Supply	Core VDD (0.85V)
AD23	VSS	Supply	Ground
AD24	VDD_TOP_2	Supply	Core VDD (0.85V)
AD25	VSS	Supply	Ground
AD26	VDD_TOP_2	Supply	Core VDD (0.85V)
AD27	VSS	Supply	Ground
AD28	VDD_TOP_2	Supply	Core VDD (0.85V)
AD29	VSS	Supply	Ground
AD30	VDD_TOP_2	Supply	Core VDD (0.85V)
AD31	VSS	Supply	Ground
AD32	VDD_TOP_2	Supply	Core VDD (0.85V)
AD33	TEST_MODE_2	Input	Test Mode
AD34	TEST_GPIO[15]_2		Test Pin (leave floating)
AD35	TEST_GPIO[13]_2		Test Pin (leave floating)
AD36	VDDIO_2	Supply	IO VDD (3.3V)
AE1	VSS	Supply	Ground
AE2	DBG_SPARE[1]_1		Spare (leave floating)
AE3	DBG_SPARE[0]_1		Spare (leave floating)
AE4	ANAVDD_DIO_1	Analog	Thermal Diode Anode
AE5	VSS	Supply	Ground
AE6	VDD_TOP_1	Supply	Core VDD (0.85V)
AE7	VSS	Supply	Ground
AE8	VDD_TOP_1	Supply	Core VDD (0.85V)
AE9	VSS	Supply	Ground
AE10	VDD_TOP_1	Supply	Core VDD (0.85V)
AE11	VSS	Supply	Ground

AE12	VDD_TOP_1	Supply	Core VDD (0.85V)
AE13	VSS	Supply	Ground
AE14	VDD_TOP_1	Supply	Core VDD (0.85V)
AE15	VSS	Supply	Ground
AE16	VDD_TOP_1	Supply	Core VDD (0.85V)
AE17	VSS	Supply	Ground
AE18	VDD_TOP_1	Supply	Core VDD (0.85V)
AE19	VDD_TOP_2	Supply	Core VDD (0.85V)
AE20	VSS	Supply	Ground
AE21	VDD_TOP_2	Supply	Core VDD (0.85V)
AE22	VSS	Supply	Ground
AE23	VDD_TOP_2	Supply	Core VDD (0.85V)
AE24	VSS	Supply	Ground
AE25	VDD_TOP_2	Supply	Core VDD (0.85V)
AE26	VSS	Supply	Ground
AE27	VDD_TOP_2	Supply	Core VDD (0.85V)
AE28	VSS	Supply	Ground
AE29	VDD_TOP_2	Supply	Core VDD (0.85V)
AE30	VSS	Supply	Ground
AE31	VDD_TOP_2	Supply	Core VDD (0.85V)
AE32	VSS	Supply	Ground
AE33	VDDIO_2	Supply	IO VDD (3.3V)
AE34	JTG_TDO_2	Output	JTAG Test Data Output
AE35	JTG_TRST_L_2	Input	JTAG Test Reset
AE36	JTG_TMS_2	Input	JTAG Test Mode Select
AF1	VDD_TOP_1	Supply	Core VDD (0.85V)
AF2	ANAVSS_DIO_1	Analog	Thermal Diode Cathode
AF3	VDDIO_1	Supply	IO VDD (3.3V)
AF4	PLL_REF_CLK_1	Input	PLL Reference Clock
AF5	ANAVDD_PLL_1	Supply	PLL Analog VDD (0.85V)
AF6	ANAVSS_PLL_1	Supply	PLL Analog Ground
AF7	VDD_TOP_1	Supply	Core VDD (0.85V)
AF8	VSS	Supply	Ground
AF9	VDD_TOP_1	Supply	Core VDD (0.85V)
AF10	VSS	Supply	Ground
AF11	VDD_TOP_1	Supply	Core VDD (0.85V)
AF12	VSS	Supply	Ground
AF13	VDD_TOP_1	Supply	Core VDD (0.85V)
AF14	VSS	Supply	Ground
AF15	VDD_TOP_1	Supply	Core VDD (0.85V)
AF16	VSS	Supply	Ground
AF17	VDD_TOP_1	Supply	Core VDD (0.85V)
AF18	VSS	Supply	Ground
AF19	VSS	Supply	Ground
AF20	VDD_TOP_2	Supply	Core VDD (0.85V)
AF21	VSS	Supply	Ground
AF22	VDD_TOP_2	Supply	Core VDD (0.85V)
AF23	VSS	Supply	Ground
AF24	VDD_TOP_2	Supply	Core VDD (0.85V)
AF25	VSS	Supply	Ground
AF26	VDD_TOP_2	Supply	Core VDD (0.85V)
AF27	VSS	Supply	Ground
AF28	VDD_TOP_2	Supply	Core VDD (0.85V)
AF29	VSS	Supply	Ground
AF30	VDD_TOP_2	Supply	Core VDD (0.85V)
AF31	VSS	Supply	Ground

AF32	VDD_TOP_2	Supply	Core VDD (0.85V)
AF33	JTG_TCK_2	Input	JTAG Test Clock
AF34	TEST_GPIO[16]_2		Test Pin (leave floating)
AF35	VSS	Supply	Ground
AF36	JTG_TDI_2	Input	JTAG Test Data Input
AG1	VSS	Supply	Ground
AG2	DBG_PLL_RFSLIP_1	Output	PLL Reference Cycle Slip
AG3	PLL_CFG_DAT_1	Input	PLL Config Bus Data
AG4	DBG_PLL_LOST_LOCK_1	Output	PLL Lost Lock
AG5	VSS	Supply	Ground
AG6	VDD_TOP_1	Supply	Core VDD (0.85V)
AG7	VSS	Supply	Ground
AG8	VDD_TOP_1	Supply	Core VDD (0.85V)
AG9	VSS	Supply	Ground
AG10	VDD_TOP_1	Supply	Core VDD (0.85V)
AG11	VSS	Supply	Ground
AG12	VDD_TOP_1	Supply	Core VDD (0.85V)
AG13	VSS	Supply	Ground
AG14	VDD_TOP_1	Supply	Core VDD (0.85V)
AG15	VSS	Supply	Ground
AG16	VDD_TOP_1	Supply	Core VDD (0.85V)
AG17	VSS	Supply	Ground
AG18	VDD_TOP_1	Supply	Core VDD (0.85V)
AG19	VDD_TOP_2	Supply	Core VDD (0.85V)
AG20	VSS	Supply	Ground
AG21	VDD_TOP_2	Supply	Core VDD (0.85V)
AG22	VSS	Supply	Ground
AG23	VDD_TOP_2	Supply	Core VDD (0.85V)
AG24	VSS	Supply	Ground
AG25	VDD_TOP_2	Supply	Core VDD (0.85V)
AG26	VSS	Supply	Ground
AG27	VDD_TOP_2	Supply	Core VDD (0.85V)
AG28	VSS	Supply	Ground
AG29	VDD_TOP_2	Supply	Core VDD (0.85V)
AG30	VSS	Supply	Ground
AG31	VDD_TOP_2	Supply	Core VDD (0.85V)
AG32	VSS	Supply	Ground
AG33	TEST_GPIO[19]_2		Test Pin (leave floating)
AG34	TEST_GPIO[20]_2		Test Pin (leave floating)
AG35	TEST_GPIO[18]_2		Test Pin (leave floating)
AG36	TEST_GPIO[17]_2		Test Pin (leave floating)
AH1	PLL_BYPASS_IN_1	Input	PLL Clock Bypass
AH2	VSS	Supply	Ground
AH3	DBG_PLL_FBSLIP_1	Output	PLL Feedback Cycle Slip
AH4	SPI_TXD_1	Output-TS	SPI Transmit Data
AH5	VDD_TOP_1	Supply	Core VDD (0.85V)
AH6	VSS	Supply	Ground
AH7	VDD_TOP_1	Supply	Core VDD (0.85V)
AH8	VSS	Supply	Ground
AH9	VDD_TOP_1	Supply	Core VDD (0.85V)
AH10	VSS	Supply	Ground
AH11	VDD_TOP_1	Supply	Core VDD (0.85V)
AH12	VSS	Supply	Ground
AH13	VDD_TOP_1	Supply	Core VDD (0.85V)
AH14	VSS	Supply	Ground
AH15	VDD_TOP_1	Supply	Core VDD (0.85V)

AH16	VSS	Supply	Ground
AH17	VDD_TOP_1	Supply	Core VDD (0.85V)
AH18	VSS	Supply	Ground
AH19	VSS	Supply	Ground
AH20	VDD_TOP_2	Supply	Core VDD (0.85V)
AH21	VSS	Supply	Ground
AH22	VDD_TOP_2	Supply	Core VDD (0.85V)
AH23	VSS	Supply	Ground
AH24	VDD_TOP_2	Supply	Core VDD (0.85V)
AH25	VSS	Supply	Ground
AH26	VDD_TOP_2	Supply	Core VDD (0.85V)
AH27	VSS	Supply	Ground
AH28	VDD_TOP_2	Supply	Core VDD (0.85V)
AH29	VSS	Supply	Ground
AH30	VDD_TOP_2	Supply	Core VDD (0.85V)
AH31	VSS	Supply	Ground
AH32	VDD_TOP_2	Supply	Core VDD (0.85V)
AH33	TEST_GPIO[24]_2		Test Pin (leave floating)
AH34	VDDIO_2	Supply	IO VDD (3.3V)
AH35	TEST_GPIO[22]_2		Test Pin (leave floating)
AH36	TEST_GPIO[21]_2		Test Pin (leave floating)
AJ1	PLL_CFG_CLK_1	Input	PLL Config Bus Clock
AJ2	RESET_COLD_L_1	Input-Schmidt	Hard Reset, Active Low
AJ3	SPI_SS_IN_L_1	Input	SPI Chip Select
AJ4	VDDIO_1	Supply	IO VDD (3.3V)
AJ5	VSS	Supply	Ground
AJ6	VDD_TOP_1	Supply	Core VDD (0.85V)
AJ7	VSS	Supply	Ground
AJ8	VDD_TOP_1	Supply	Core VDD (0.85V)
AJ9	VSS	Supply	Ground
AJ10	VDD_TOP_1	Supply	Core VDD (0.85V)
AJ11	VSS	Supply	Ground
AJ12	VDD_TOP_1	Supply	Core VDD (0.85V)
AJ13	VSS	Supply	Ground
AJ14	VDD_TOP_1	Supply	Core VDD (0.85V)
AJ15	VSS	Supply	Ground
AJ16	VDD_TOP_1	Supply	Core VDD (0.85V)
AJ17	VSS	Supply	Ground
AJ18	VDD_TOP_1	Supply	Core VDD (0.85V)
AJ19	VDD_TOP_2	Supply	Core VDD (0.85V)
AJ20	VSS	Supply	Ground
AJ21	VDD_TOP_2	Supply	Core VDD (0.85V)
AJ22	VSS	Supply	Ground
AJ23	VDD_TOP_2	Supply	Core VDD (0.85V)
AJ24	VSS	Supply	Ground
AJ25	VDD_TOP_2	Supply	Core VDD (0.85V)
AJ26	VSS	Supply	Ground
AJ27	VDD_TOP_2	Supply	Core VDD (0.85V)
AJ28	VSS	Supply	Ground
AJ29	VDD_TOP_2	Supply	Core VDD (0.85V)
AJ30	VSS	Supply	Ground
AJ31	VDD_TOP_2	Supply	Core VDD (0.85V)
AJ32	VSS	Supply	Ground
AJ33	TEST_GPIO[26]_2		Test Pin (leave floating)
AJ34	TEST_GPIO[25]_2		Test Pin (leave floating)
AJ35	TEST_GPIO[23]_2		Test Pin (leave floating)

AJ36	VSS	Supply	Ground
AK1	VDDIO_1	Supply	IO VDD (3.3V)
AK2	SPI_SCLK_IN_1	Input	SPI Clock
AK3	TEST_GPIO[50]_1		Test Pin (leave floating)
AK4	TEST_GPIO[47]_1		Test Pin (leave floating)
AK5	VDD_TOP_1	Supply	Core VDD (0.85V)
AK6	VSS	Supply	Ground
AK7	VDD_TOP_1	Supply	Core VDD (0.85V)
AK8	VSS	Supply	Ground
AK9	VDD_TOP_1	Supply	Core VDD (0.85V)
AK10	VSS	Supply	Ground
AK11	VDD_TOP_1	Supply	Core VDD (0.85V)
AK12	VSS	Supply	Ground
AK13	VDD_TOP_1	Supply	Core VDD (0.85V)
AK14	VSS	Supply	Ground
AK15	VDD_TOP_1	Supply	Core VDD (0.85V)
AK16	VSS	Supply	Ground
AK17	VDD_TOP_1	Supply	Core VDD (0.85V)
AK18	VSS	Supply	Ground
AK19	VSS	Supply	Ground
AK20	VDD_TOP_2	Supply	Core VDD (0.85V)
AK21	VSS	Supply	Ground
AK22	VDD_TOP_2	Supply	Core VDD (0.85V)
AK23	VSS	Supply	Ground
AK24	VDD_TOP_2	Supply	Core VDD (0.85V)
AK25	VSS	Supply	Ground
AK26	VDD_TOP_2	Supply	Core VDD (0.85V)
AK27	VSS	Supply	Ground
AK28	VDD_TOP_2	Supply	Core VDD (0.85V)
AK29	VSS	Supply	Ground
AK30	VDD_TOP_2	Supply	Core VDD (0.85V)
AK31	VSS	Supply	Ground
AK32	VDD_SENSE_2	Analog	Core VDD Sense
AK33	VSS	Supply	Ground
AK34	TEST_GPIO[29]_2		Test Pin (leave floating)
AK35	TEST_GPIO[27]_2		Test Pin (leave floating)
AK36	TEST_GPIO[28]_2		Test Pin (leave floating)
AL1	SPI_RXD_1	Input	SPI Receive Data
AL2	TEST_GPIO[51]_1		Test Pin (leave floating)
AL3	VSS	Supply	Ground
AL4	TEST_GPIO[43]_1		Test Pin (leave floating)
AL5	VSS	Supply	Ground
AL6	VDD_TOP_1	Supply	Core VDD (0.85V)
AL7	VSS	Supply	Ground
AL8	VDD_TOP_1	Supply	Core VDD (0.85V)
AL9	VSS	Supply	Ground
AL10	VDD_TOP_1	Supply	Core VDD (0.85V)
AL11	VSS	Supply	Ground
AL12	VDD_TOP_1	Supply	Core VDD (0.85V)
AL13	VSS	Supply	Ground
AL14	VDD_TOP_1	Supply	Core VDD (0.85V)
AL15	VSS	Supply	Ground
AL16	VDD_TOP_1	Supply	Core VDD (0.85V)
AL17	VSS	Supply	Ground
AL18	VDD_TOP_1	Supply	Core VDD (0.85V)
AL19	VDD_TOP_2	Supply	Core VDD (0.85V)

AL20	VSS	Supply	Ground
AL21	VDD_TOP_2	Supply	Core VDD (0.85V)
AL22	VSS	Supply	Ground
AL23	VDD_TOP_2	Supply	Core VDD (0.85V)
AL24	VSS	Supply	Ground
AL25	VDD_TOP_2	Supply	Core VDD (0.85V)
AL26	ANAVSS_PLL_2	Supply	PLL Analog Ground
AL27	VDD_TOP_2	Supply	Core VDD (0.85V)
AL28	VSS	Supply	Ground
AL29	VDD_TOP_2	Supply	Core VDD (0.85V)
AL30	VSS	Supply	Ground
AL31	VDD_TOP_2	Supply	Core VDD (0.85V)
AL32	VSS_SENSE_2	Analog	Core VSS Sense
AL33	TEST_GPIO[33]_2		Test Pin (leave floating)
AL34	TEST_GPIO[32]_2		Test Pin (leave floating)
AL35	VDDIO_2	Supply	IO VDD (3.3V)
AL36	TEST_GPIO[30]_2		Test Pin (leave floating)
AM1	DBG_HEART_BEAT_1	Output	Heart Beat. Toggles once per second @ 1GHz
AM2	TEST_GPIO[48]_1		Test Pin (leave floating)
AM3	TEST_GPIO[44]_1		Test Pin (leave floating)
AM4	TEST_GPIO[39]_1		Test Pin (leave floating)
AM5	VDDIO_1	Supply	IO VDD (3.3V)
AM6	VSS_SENSE_1	Analog	Core VSS Sense
AM7	VDD_SENSE_1	Analog	Core VDD Sense
AM8	VSS	Supply	Ground
AM9	VDD_TOP_1	Supply	Core VDD (0.85V)
AM10	VSS	Supply	Ground
AM11	VDD_TOP_1	Supply	Core VDD (0.85V)
AM12	VSS	Supply	Ground
AM13	VDD_TOP_1	Supply	Core VDD (0.85V)
AM14	VSS	Supply	Ground
AM15	VDD_TOP_1	Supply	Core VDD (0.85V)
AM16	VSS	Supply	Ground
AM17	VDD_TOP_1	Supply	Core VDD (0.85V)
AM18	VSS	Supply	Ground
AM19	TEST_GPIO[71]_2		Test Pin (leave floating)
AM20	VSS	Supply	Ground
AM21	VSS	Supply	Ground
AM22	VDDIO_2	Supply	IO VDD (3.3V)
AM23	VSS	Supply	Ground
AM24	VDD_TOP_2	Supply	Core VDD (0.85V)
AM25	VSS	Supply	Ground
AM26	ANAVDD_PLL_2	Supply	PLL Analog VDD (0.85V)
AM27	VSS	Supply	Ground
AM28	VDD_TOP_2	Supply	Core VDD (0.85V)
AM29	VSS	Supply	Ground
AM30	VDD_TOP_2	Supply	Core VDD (0.85V)
AM31	VSS	Supply	Ground
AM32	VDDIO_2	Supply	IO VDD (3.3V)
AM33	TEST_GPIO[34]_2		Test Pin (leave floating)
AM34	VDDIO_2	Supply	IO VDD (3.3V)
AM35	VSS	Supply	Ground
AM36	TEST_GPIO[31]_2		Test Pin (leave floating)
AN1	TEST_GPIO[49]_1		Test Pin (leave floating)
AN2	VDDIO_1	Supply	IO VDD (3.3V)
AN3	TEST_GPIO[41]_1		Test Pin (leave floating)

AN4	TEST_GPIO[37]_1		Test Pin (leave floating)
AN5	TEST_GPIO[34]_1		Test Pin (leave floating)
AN6	TEST_GPIO[33]_1		Test Pin (leave floating)
AN7	VSS	Supply	Ground
AN8	TEST_GPIO[26]_1		Test Pin (leave floating)
AN9	TEST_GPIO[24]_1		Test Pin (leave floating)
AN10	TEST_GPIO[19]_1		Test Pin (leave floating)
AN11	JTG_TCK_1	Input	JTAG Test Clock
AN12	VDDIO_1	Supply	IO VDD (3.3V)
AN13	TEST_MODE_1	Input	Test Mode
AN14	TEST_GPIO[11]_1		Test Pin (leave floating)
AN15	TEST_GPIO[7]_1		Test Pin (leave floating)
AN16	TEST_GPIO[4]_1		Test Pin (leave floating)
AN17	VSS	Supply	Ground
AN18	VDD_TOP_1	Supply	Core VDD (0.85V)
AN19	VDDIO_2	Supply	IO VDD (3.3V)
AN20	TEST_GPIO[67]_2		Test Pin (leave floating)
AN21	TEST_GPIO[64]_2		Test Pin (leave floating)
AN22	TEST_GPIO[59]_2		Test Pin (leave floating)
AN23	TEST_GPIO[55]_2		Test Pin (leave floating)
AN24	VSS	Supply	Ground
AN25	ANAVDD_DIO_2	Analog	Thermal Diode Anode
AN26	PLL_REF_CLK_2	Input	PLL Reference Clock
AN27	DBG_PLL_LOST_LOCK_2	Output	PLL Lost Lock
AN28	SPI_TXD_2	Output-TS	SPI Transmit Data
AN29	VDDIO_2	Supply	IO VDD (3.3V)
AN30	TEST_GPIO[47]_2		Test Pin (leave floating)
AN31	TEST_GPIO[43]_2		Test Pin (leave floating)
AN32	TEST_GPIO[39]_2		Test Pin (leave floating)
AN33	TEST_GPIO[37]_2		Test Pin (leave floating)
AN34	VSS	Supply	Ground
AN35	TEST_GPIO[36]_2		Test Pin (leave floating)
AN36	TEST_GPIO[35]_2		Test Pin (leave floating)
AP1	TEST_GPIO[46]_1		Test Pin (leave floating)
AP2	TEST_GPIO[45]_1		Test Pin (leave floating)
AP3	TEST_GPIO[40]_1		Test Pin (leave floating)
AP4	VSS	Supply	Ground
AP5	VDDIO_1	Supply	IO VDD (3.3V)
AP6	TEST_GPIO[32]_1		Test Pin (leave floating)
AP7	TEST_GPIO[29]_1		Test Pin (leave floating)
AP8	TEST_GPIO[25]_1		Test Pin (leave floating)
AP9	VDDIO_1	Supply	IO VDD (3.3V)
AP10	TEST_GPIO[20]_1		Test Pin (leave floating)
AP11	TEST_GPIO[16]_1		Test Pin (leave floating)
AP12	JTG_TDO_1	Output-TS	JTAG Test Data Output
AP13	TEST_GPIO[15]_1		Test Pin (leave floating)
AP14	VSS	Supply	Ground
AP15	TEST_GPIO[8]_1		Test Pin (leave floating)
AP16	TEST_GPIO[6]_1		Test Pin (leave floating)
AP17	TEST_GPIO[2]_1		Test Pin (leave floating)v
AP18	VSS	Supply	Ground
AP19	TEST_GPIO[69]_2		Test Pin (leave floating)
AP20	TEST_GPIO[65]_2		Test Pin (leave floating)
AP21	VSS	Supply	Ground
AP22	TEST_GPIO[58]_2		Test Pin (leave floating)
AP23	TEST_GPIO[54]_2		Test Pin (leave floating)

AP24	TEST_GPIO[52]_2		Test Pin (leave floating)
AP25	DBG_SPARE[0]_2		Spare (leave floating)
AP26	VDDIO_2	Supply	IO VDD (3.3V)
AP27	PLL_CFG_DAT_2	Input	PLL Config Bus Data
AP28	DBG_PLL_FBSLIP_2	Output	PLL Feedback Cycle Slip
AP29	SPI_SS_IN_L_2	Input	SPI Chip Select
AP30	TEST_GPIO[50]_2		Test Pin (leave floating)
AP31	VSS	Supply	Ground
AP32	TEST_GPIO[44]_2		Test Pin (leave floating)
AP33	TEST_GPIO[41]_2		Test Pin (leave floating)
AP34	TEST_GPIO[40]_2		Test Pin (leave floating)
AP35	TEST_GPIO[38]_2		Test Pin (leave floating)
AP36	VDDIO_2	Supply	IO VDD (3.3V)
AR1	VSS	Supply	Ground
AR2	TEST_GPIO[42]_1		Test Pin (leave floating)
AR3	TEST_GPIO[38]_1		Test Pin (leave floating)
AR4	TEST_GPIO[36]_1		Test Pin (leave floating)
AR5	VSS	Supply	Ground
AR6	VDDIO_1	Supply	IO VDD (3.3V)
AR7	TEST_GPIO[27]_1		Test Pin (leave floating)
AR8	TEST_GPIO[23]_1		Test Pin (leave floating)
AR9	TEST_GPIO[22]_1		Test Pin (leave floating)
AR10	TEST_GPIO[18]_1		Test Pin (leave floating)
AR11	VSS	Supply	Ground
AR12	JTG_TRST_L_1	Input	JTAG Test Reset
AR13	TEST_GPIO[13]_1		Test Pin (leave floating)
AR14	TEST_GPIO[12]_1		Test Pin (leave floating)
AR15	TEST_GPIO[10]_1		Test Pin (leave floating)
AR16	VDDIO_1	Supply	IO VDD (3.3V)
AR17	TEST_GPIO[1]_1		Test Pin (leave floating)
AR18	TEST_GPIO[0]_1		Test Pin (leave floating)
AR19	TEST_GPIO[70]_2		Test Pin (leave floating)
AR20	TEST_GPIO[66]_2		Test Pin (leave floating)
AR21	TEST_GPIO[63]_2		Test Pin (leave floating)
AR22	TEST_GPIO[60]_2		Test Pin (leave floating)
AR23	VDDIO_2	Supply	IO VDD (3.3V)
AR24	TEST_GPIO[53]_2		Test Pin (leave floating)
AR25	DBG_SPARE[1]_2		Spare (leave floating)
AR26	ANAVSS_DIO_2	Analog	Thermal Diode Cathode
AR27	DBG_PLL_RFSLIP_2	Output	PLL Reference Cycle Slip
AR28	VSS	Supply	Ground
AR29	RESET_COLD_L_2	Input-Schmidt	Hard Reset, Active Low
AR30	SPI_SCLK_IN_2	Input	SPI Clock
AR31	TEST_GPIO[51]_2		Test Pin (leave floating)
AR32	TEST_GPIO[48]_2		Test Pin (leave floating)
AR33	VDDIO_2	Supply	IO VDD (3.3V)
AR34	TEST_GPIO[45]_2		Test Pin (leave floating)
AR35	TEST_GPIO[42]_2		Test Pin (leave floating)
AR36	VSS	Supply	Ground
AT1	VSS	Supply	Ground
AT2	VSS	Supply	Ground
AT3	VDDIO_1	Supply	IO VDD (3.3V)
AT4	TEST_GPIO[35]_1		Test Pin (leave floating)
AT5	TEST_GPIO[31]_1		Test Pin (leave floating)
AT6	TEST_GPIO[30]_1		Test Pin (leave floating)
AT7	TEST_GPIO[28]_1		Test Pin (leave floating)

AT8	VSS	Supply	Ground
AT9	TEST_GPIO[21]_1		Test Pin (leave floating)
AT10	TEST_GPIO[17]_1		Test Pin (leave floating)
AT11	JTG_TDI_1	Input	JTAG Test Data Input
AT12	JTG_TMS_1	Input	JTAG Test Mode Select
AT13	VDDIO_1	Supply	IO VDD (3.3V)
AT14	TEST_GPIO[14]_1		Test Pin (leave floating)
AT15	TEST_GPIO[9]_1		Test Pin (leave floating)
AT16	TEST_GPIO[5]_1		Test Pin (leave floating)
AT17	TEST_GPIO[3]_1		Test Pin (leave floating)
AT18	VSS	Supply	Ground
AT19	TEST_GPIO[68]_2		Test Pin (leave floating)
AT20	VDDIO_2	Supply	IO VDD (3.3V)
AT21	TEST_GPIO[61]_2		Test Pin (leave floating)
AT22	TEST_GPIO[62]_2		Test Pin (leave floating)
AT23	TEST_GPIO[57]_2		Test Pin (leave floating)
AT24	TEST_GPIO[56]_2		Test Pin (leave floating)
AT25	VSS	Supply	Ground
AT26	VDD_TOP_2	Supply	V Core VDD (0.85V)
AT27	VSS	Supply	Ground
AT28	PLL_BYPASS_IN_2	Input	PLL Clock Bypass
AT29	PLL_CFG_CLK_2	Input	PLL Config Bus Clock
AT30	VDDIO_2	Supply	IO VDD (3.3V)
AT31	SPI_RXD_2	Input	SPI Receive Data
AT32	DBG_HEART_BEAT_2	Output	Heart Beat. Toggles once per second @ 1GHz
AT33	TEST_GPIO[49]_2		Test Pin (leave floating)
AT34	TEST_GPIO[46]_2		Test Pin (leave floating)
AT35	VSS	Supply	Ground
AT36	VSS	Supply	Ground

Table 2-2 FCBGA Pin Map

2.3 Signal Descriptions

Table 2-3. SPI Interface Descriptions

Signal Name	Description	Type		Ball Number
SPI_TXD	SPI Transmit Data	Output	3.3V LVCMOS	
SPI_RXD	SPI Receive Data	Input	3.3V LVCMOS	
SPI_SCLK_IN	SPI Clock	Input	3.3V LVCMOS	
SPI_SS_IN_L	SPI Slave Select	Input	3.3V LVCMOS	

Table 2-4. PLL Interface Descriptions

Signal Name	Description	Type		Ball Number
ANAVDD_PLL	Analog VDD	Supply	Power(0.85V)	
ANAVSS_PLL	Analog VSS	Supply	Power	
PLL_CFG_CLK	PLL Configuration Clock	Input	3.3V LVCMOS	
PLL_CFG_DAT	PLL Configuration Data	Input	3.3V LVCMOS	

Table 2-5. JTAG Interface Descriptions

Signal Name	Description	Type		Ball Number
JTG_TDO	JTAG Test Data Output	Output	3.3V LVCMOS	

JTG_TDI	JTAG Test Data Input	Input	3.3V LVCMOS	
JTG_TRST_L[4]	JTAG Test Reset	Input	3.3V LVCMOS	
JTG_TCK	JTAG Test Clock	Input	3.3V LVCMOS	
JTG_TMS	JTAG Test Mode Select	Input Schmidt	3.3V LVCMOS	

Table 2-6. Clock Reset Interface Descriptions

Signal Name	Description	Type		Ball Number
PLL_REF_CLK	PLL Reference Clock	Input	3.3V LVCMOS	
RESET_COLD_L	Reset Input	Input	3.3V LVCMOS	

Table 2-7. Debug Interface Descriptions

Signal Name	Description	Type		Ball Number
DBG_HEART_BEAT	Heartbeat Monitor	Output	3.3V LVCMOS	
DBG_PLL_LOST_LOCK	PLL Lost Lock	Output	3.3V LVCMOS	
DBG_PLL_RFSLIP	PLL Reference Cycle Slip	Output	3.3V LVCMOS	
DBG_PLL_FBSLIP	PLL Feedback Cycle Slip	Output	3.3V LVCMOS	
PLL_BYPASS_IN[5]	PLL Clock Bypass	Input	3.3V LVCMOS	
DBG_SPARE[1:0][6]	Spare Debug	BiDi	3.3V LVCMOS	

Table 2-8. Thermal Diode Signal Descriptions

Signal Name	Description	Type		Ball Number
ANAVDD_DIO	Thermal diode Anode	Analog	ESD Protected	
ANAVSS_DIO	Thermal diode Cathode	Analog	ESD Protected	

Table 2-9. Core Voltage Sense Signal Descriptions

Signal Name	Description	Type		Ball Number
VDD_SENSE	VDD Sense	Analog	ESD Protected	
VSS_SENSE	VSS Sense	Analog	ESD Protected	

Table 2-10. Test Signal Descriptions

Signal Name	Description	Type		Ball Number
TEST_MODE[7]	Test Mode Select	Input	3.3V LVCMOS	
TEST_GPIO[71:0][8]	Test Pins	BiDi	3.3V LVCMOS	

Table 2-11. Power Signal Descriptions

Signal Name	Description	Type		Ball Number
VSS	Ground	Supply		
VDD_TOP	Core Supply Voltage	Supply	0.85V	
VDDIO	IO Supply Voltage	Supply	3.3V	

[4] If the JTAG port is not utilized, JTAG_TRST_L should be tied low.
[5] PLL_BYPASS_IN must be pulled low external to the Goldstrike1™.
[6] The Debug Spare pins are currently disabled and should be left floating.
[7] The TEST_MODE pin should be tied low for normal operation.
[8] Test pins are for manufacturing use only. All TEST_GPIO[*] pins should not be tied on the PCB and left floating.

3 Device Operating Conditions

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings Over Junction Temperature [9][10]

PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Core Supply Voltage	0.765	0.850	0.935	V
f_{MAX}	PLL Operating Frequency		1.05	1.75	GHz
T_J	Junction temperature		105	125	°C
V_{DIO}	Voltage between Diode Terminals			1.21	V
ESD	ESD protection			2K (HBM) 200 (MM) 500 (CDM)	V
V_{DVDD}	IO Supply Voltage	-0.5		3.63	V
V_{PAD}	Voltage Range at IO	-0.5		V_{DVDD} + 0.5	V
I_{OSH}	Short Circuit Current – Output High			65	mA
I_{OSL}	Short Circuit Current – Output Low			68	mA

3.2 Recommended Operating Conditions

Table 3-2. Operating Performance Points

PARAMETER		MIN	MAX	UNIT	NOTES
V_{DD}	Core Supply Voltage	0.765	0.850	V	[11]
f_{MAX}	PLL Operating Frequency		1.1	GHz	[12]
T_J	Junction temperature		105	°C	[13]
$I_{VDDP/N}$	Diode Injection Current	5		200	µA
V_{DVDD}	IO Supply Voltage	2.97	3.3	3.63	V
V_{PAD}	Voltage Range at IO	-0.3		V_{DVDD} + 0.3	V
I_{JIT}	PLL Reference input jitter (long-term, P-P)		2%	divided reference cycle	

Table 3-3. Maximum Current Ratings at Power Terminals

PARAMETER		MAX	UNIT
I_{DD}	Core Supply Current @ V_{DD} = 0.765V	190	A
I_{DD}	Core Supply Current @ V_{DD} = 0.650V	150	A
I_{DVDD}	IO Supply Current @ V_{DVDD} = 3.3V	TBD	mA

[9] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[10] All voltage values are with respect to their associated VSS.
[11] This voltage range allows the Goldstrike1™ to operate at temperatures below the max junction temperature rating of 125°C.
[12] The Goldstrike1™ logic may be clocked as high as 1.75GHz. However care must be taken to ensure other parameters are not violated e.g. the max junction temperature.
[13] The max junction temperature is a function of a number of variables: fabrication variances, operating voltage, operating frequency, package thermal resistance (θ_{JC}), cooling system (θ_{JA}).

3.3 DC Electrical Characteristics

Table 3-4. DC Electrical Characteristics over Recommended Ranges of Supply Voltage and Operating Temperature

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Low-level input voltage	V_{DVSS} – 0.3		0.3 * V_{DVDD}	V
V_{OH}	High-level output voltage	V_{DVSS} – 0.4			V
V_{OL}	Low-level output voltage		0.4		V
V_{HYS}	Input Hysteresis Voltage	0.4			V
I_{IL}	Input leakage current			10	µA
I_{ILZ}	High-Z State Pad Leakage			1	µA
I_{OH}	Output Drive Current (V_{OH} = V_{DVDD} – 0.4)	7.07	11.17	16.68	mA
I_{OL}	Output Drive Current (V_{OL} = 0.4)	7.53	12.74	18.02	mA
I_{PU}	Pull-Up Current	32.5	56.8	97.8	µA
I_{PD}	Pull-Down Current	30.2	54.9	96.4	µA

3.4 AC Electrical Characteristics

Table 3-5. DC Electrical Characteristics over Recommended Ranges of Supply Voltage and Operating Temperature

PARAMETER		MIN	TYP	MAX	UNIT
T_{SCLK}	High-level input voltage	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Low-level input voltage	V_{DVSS} – 0.3		0.3 * V_{DVDD}	V
V_{OH}	High-level output voltage	V_{DVSS} – 0.4			V
V_{OL}	Low-level output voltage		0.4		V
V_{HYS}	Input Hysteresis Voltage	0.4			V
I_{IL}	Input leakage current			10	µA
I_{ILZ}	High-Z State Pad Leakage			1	µA
I_{OH}	Output Drive Current (V_{OH} = V_{DVDD} – 0.4)	7.07	11.17	16.68	mA
I_{OL}	Output Drive Current (V_{OL} = 0.4)	7.53	12.74	18.02	mA
I_{PU}	Pull-Up Current	32.5	56.8	97.8	µA
I_{PD}	Pull-Down Current	30.2	54.9	96.4	µA

3.5 External Capacitors

To improve module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

3.5.1 Voltage Decoupling Capacitors

Table 3-6 summarizes the power supply decoupling capacitor recommendations.

Table 3-6. Power Supply Decoupling Capacitor Characteristics

PARAMETER	TYP	UNIT
C_{VDD}	TBD	µF

3.5.2 IO Decoupling Capacitors

Table 3-7 summarizes the power supply decoupling capacitor recommendations.

Table 3-7. Power Supply Decoupling Capacitor Characteristics

PARAMETER	TYP	UNIT
C_{IO}	TBD	µF

4 Power and Clocking

4.1 Power Supplies

4.1.1 Power-Up Sequencing

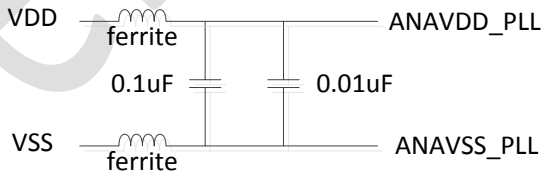
There is no specific power up sequence required by the Goldstrike1™ device.

4.1.2 VDD/VSS Sense Connections

The Goldstrike1™ has two analog pins, VDD_SENSE and VSS_SENSE, for connection to the external power supply sense lines. The Goldstrike1™ device consumes a large amount of current and some drop is expected between the supply and the power delivered to the silicon logic. The sense lines will ensure the Goldstrike1™ dies are being delivered the correct voltages.

4.1.3 PLL Power Supply Requirements

The PLL's two analog supplies should be filtered with two series ferrite beads and two shunt 0.1uF and 0.01uF capacitors. The ferrite on VSS is preferred but optional. Adding the ferrite on VSS converts supply noise to substrate noise as seen by the PLL. The PLLs are designed to be relatively insensitive to supply and substrate noise, so the presence of this ferrite is a second order issue.



The ferrite beads should be similar one of the following from Murata:

Table 4-1. Ferrite Bead Characteristics

PART NUMBER	R@DC	Z@10MHz	Z@100MHz	Z@1GHz	SIZE
BLM18EG601SN1*	0.35	200	600		0603
BLM18PG471SN1	0.20	130	470		0603
BLM18KG601SN1	0.15	160	600		0603
BLM18AG601SN1	0.38	180	600		0603
BLM18AG102SN1	0.50	280	1000		0603

BLM18TG601TN1	0.45	190	600		0603
BLM15AG601SN1	0.60	200	600		0402
BLM15AX601SN1*	0.34	190	600		0402
BLM15AX102SN1	0.49	250	1000		0402
BLM03AX601SN1	0.85	120	600		0201

* Denotes preferred choice

Similar ferrite beads are also available from Panasonic. The key characteristics to select are:

- DC resistance less than 0.40 ohms
- Impedance at 10MHz equal to or greater 180 ohms
- Impedance at 100MHz equal to or greater than 600 ohms

The capacitors should be mounted as close to the package balls as possible.

4.2 Clock Specifications

4.2.1 Input Clock Specifications

Each Hash Engine in the Goldstrike1™ has a single clock input, PLL_REF_CLK, and is supplied by and external oscillator. The oscillator provides the reference clock for the Goldstrike1™ internal PLL. The output frequency of the PLL is determined by the following equation:

$$F_{out} = F_{ref} * NF / NR / OD$$

F_{REF} is the reference frequency (PLL_CLK_REF) which must be 50 MHz. NF, NR and OD are set by the Goldstrike1's PLL Control Register.

4.2.2 PLL Control Register

A 22 bit PLL Control Register is used to tune the PLL frequency during normal operation and can be used to modify PLL settings. The register fields are shown here.

Table 4-2. PLL Control Register

BITS	NAME	DESCRIPTION
[21:16]	NB-1	This field selects the values of 1-64 for the PLL's bandwidth divider (NB). This field should always be set to equal the value for NF-1. **Reset Value: 6'd19**
[15]	TEST	The PLL has a divider test mode (TEST=1) to allow for rapid production testing of the dividers in the PLLs without using the internal analog circuitry. This mode (TEST=1) overrides the bypass mode (BYPASS=1). This bit should be set to zero (TEST=0) for normal operation. **Reset Value: 1'b0**
[14]	BYPASS	When set (BYPASS=1) the reference input (PLL_REF_CLK) is bypassed directly to the outputs (Core Clock). This bit should be set to zero (BYPASS=0) for normal operation. **Reset Value: 1'b0**
[13:8]	NF-1	This field selects the values of 1-64 for the PLL's multiplication factor (NF). This field should be set to the desired NF value minus one (NF-1). For example, the reset value of 6'd19 sets the multiplication factor NF = 6'd20. This field should be modified during normal operation as needed to adjust the Goldstrike1™ internal clock frequency. **Reset Value: 6'd19**

[7:4]	NR-1	This field selects the values of 1-16 for the PLL's reference divider (NR). This field should be set to the desired NR value minus one (NR-1). For example, the reset value of 0 sets the reference divider NR = 1.[14] **Reset Value: 4'd0**
[3:0]	OD-1	This field selects the values of 1-16 for the PLL's post VCO divider (OD). This field should be set to the desired OD value minus one (OD-1). For example, the reset value of 0 sets the post VDO divider OD = 1.[6] **Reset Value: 4'd0**

The default settings of the PLL Control Register are designed to provide a 1 GHz frequency for the Goldstrike1™ Core Clock. The following table shows recommended settings for the expected operating range. The default setting is highlighted in orange. Note NB-1 should always be set the same as NF-1.

Table 4-3. Typical PLL Control Register Settings[15]

PLL Control Register Settings (TEST=0, BYPASS=0)				Output Freq (MHz)	Heartbeat Period (sec)[16]
NB-1 [21:16]	NF-1 [13:8]	NR-1 [7:4]	OD-1 [3:0]		
6'h15	6'h15	4'b0	4'b0	1100.0	0.976
6'h2A	6'h2A	4'b1	4'b0	1075.0	0.999
6'h14	6'h14	4'b0	4'b0	1050.0	1.023
6'h3D	6'h3D	4'b2	4'b0	1033.3	1.039
6'h28	6'h28	4'b1	4'b0	1025.0	1.048
6'h3C	6'h3C	4'b2	4'b0	1016.6	1.056
6'h13	6'h13	4'b0	4'b0	1000.0	1.074
6'h3A	6'h3A	4'b2	4'b0	983.3	1.092
6'h26	6'h26	4'b1	4'b0	975.0	1.101
6'h39	6'h39	4'b2	4'b0	966.6	1.111
6'h12	6'h12	4'b0	4'b0	950.0	1.130
6'h37	6'h37	4'b2	4'b0	933.3	1.150
6'h24	6'h24	4'b1	4'b0	925.0	1.161
6'h36	6'h36	4'b2	4'b0	916.6	1.171
6'h11	6'h11	4'b0	4'b0	900.0	1.193
6'h34	6'h34	4'b2	4'b0	883.3	1.216
6'h22	6'h22	4'b0	4'b1	875.0	1.227
6'h33	6'h33	4'b2	4'b0	866.6	1.239
6'h21	6'h21	4'b0	4'b1	850.0	1.263

4.2.3 Writing the PLL Control Register

The PLL Control Register is written through a slow bit bang interface which could be driven from GPIOs external to the Goldstrike1. There are only 2 pins for this interface, PLL_CFG_CLK and PLL_CFG_DAT. A timing diagram for this interface is shown in Figure 4-1.

[14] It is recommended that this field be left at the reset value during normal operation in order to reach the range of expected operating frequencies for the Goldstrike1.
[15] Other frequencies can be obtained. Please contact Cointerra Customer Support for assistance in setting the Goldstrike1™ PLL parameters for your specific requirements.
[16] The heartbeat logic is described in section 5.4.1.

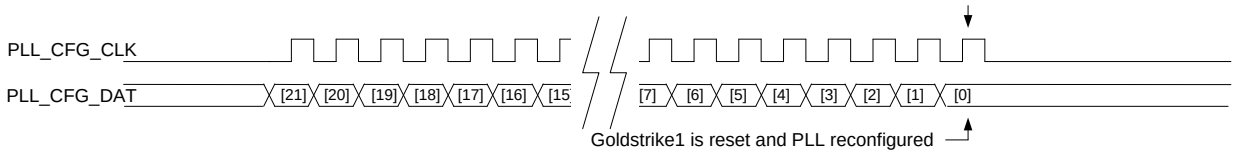


Figure 4-1. PLL_CFG Interface Timing Diagram

The serial data from PLL_CFG_DAT is clocked into a shift register on the rising edge of PLL_CFG_CLK. Data should be transmitted MSB first, starting with the MSB of the NB-1 field in PLL Control Register [21]. To reconfigure the PLL the PLL_CFG_CLK should toggle from low to high to low exactly 22 times. After the rising edge of the 22th clock the Goldstrike1™ will go through a reset sequence during which the PLL will be configured with the new data in the PLL Control Register. The PLL_CFG_CLK should be held low during normal operation and only toggled to modify the PLL settings. An external pull-down should be used on the PLL_CFG_CLK pin.

After the last (22nd) falling edge of PLL_CFG_CLK, the system should wait at least 5µs + 500 divided reference clocks (F_{REF}/NR) before sending new data to the chip to allow time for the PLL to complete the reset sequence and lock.

4.2.4 Reading the PLL Control Register

This register cannot be read directly. Instead, the current PLL settings as well as a PLL lost lock indication will be returned over the SPI interface in the status field of results packets (see section 5.1.3). The PLL settings returned will always be the current (static) setting of the PLL. It is not possible to read changes in progress to the PLL Control Register as new bits are shifting into place.

In normal operation the PLL Lost Lock indication will be 1'b0 indicating that the PLL is locked. If the PLL loses lock at any point after reset the PLL Lost Lock indication will be set to 1'b1 and remain set. The system must reset the Goldstrike1™to clear the Lost Lock indication.

4.2.5 Minimizing Jitter

The amount of period jitter observed will depend on the actual noise level on the PLL supplies and chip substrate and noise frequency content. It will increase roughly linearly with the output period and will be roughly independent of multiplication factor or bandwidth setting.

To minimize the overall output jitter, the PLL should be operated as close as possible to the maximum frequency before any output division. Thus if some division is necessary for the PLL, it should be performed by the OD divider rather than in a reference divider to maximize the VCO frequency. Since the PLL power dissipation increases with increased VCO frequency, there will be a trade-off between jitter performance and power dissipation. The overall tracking jitter can be minimized by increasing the divided reference frequency. The overall period jitter can be minimized by using an NF value that is as small as possible.

The PLL will work beyond the specified maximum frequencies, but the jitter performance will be degraded.

5 Peripheral Timing

5.1 SPI Interface

The Goldstrike1™ includes a Serial Peripheral Interface Bus slave interface for communication with a control processor (CPU). This is a synchronous serial data link that operates in full duplex mode. Devices communicate in master/slave mode where the CPU's master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

The SPI_SS_IN_L pin is the slave select input. Before a data transmission occurs, the SPI_SS_IN_L pin of the slave SPI must be low. SPI_SS_IN_L must remain low until the transmission is complete. If SPI_SS_IN_L goes high, the SPI is forced into idle state.

The SPI_SS_IN_L input also controls the serial data output pin, if SPI_SS_IN_L is high (not selected), the serial data output pin is high impedance, and, if SPI_SS_IN_L is low the first bit in the SPI Data Register is driven out of the serial data output pin. Also, if the slave is not selected (SPI_SS_IN_L is high), then the SPI_SCLK_IN input is ignored and no internal shifting of the SPI shift register takes place.

The Goldstrike1™ begins transmitting data on the first serial clock edge of SPI_SCLK_IN after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock.

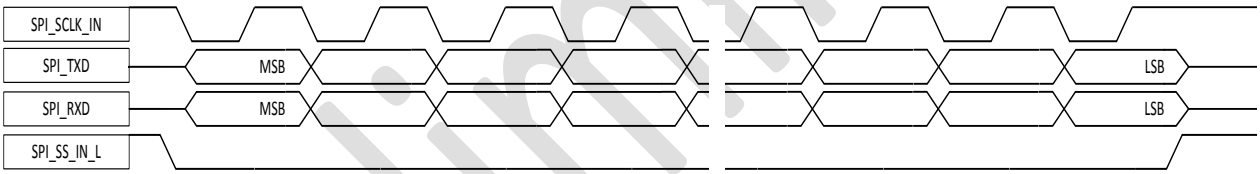


Figure 5-1. SPI Serial Format

5.1.1 SPI Transfers

The SPI Interface controls transfers of data to/from the Goldstrike1. The SPI protocol dictates that frames are limited to 16 bits or fewer. This dictates that transfers between the CPU Master SPI and the Goldstrike1™ are each 16 bits.

Communication to/from the Goldstrike1™ transfers 400-bits of information per packet. Each packet contains two parts: a 16-bit address field and a 384-bit data field. Arriving packets are acted upon based on their associated address field as determined by the Goldstrike1™ memory map shown below.

Table 5-1. Goldstrike1™ Memory Map

ADDRESS	RECEIVE DESTINATION	TRANSMIT RESPONSE
16'h0000	Pipe Control Register (PCR)	FIFO Status + 1-4 Output Results
16'h0001	Block-header for Input FIF0	FIFO Status + 1-4 Output Results
16'h0002		FIFO Status + 1-4 Output Results
16'h0003		PCR + PLL Config

In response to a SPI receive request, data is sent to either the Input FIFO or to the PCR or the Goldstrike1™ does nothing (NOP). After power up, the chip is immediately ready for operation.

However, before sending the first block-header packet, the PCR (Pipe Control Register) needs to be written if the power up value is to be changed.

5.1.2 Pipe Control Register

The PCR is shown in the figure below.

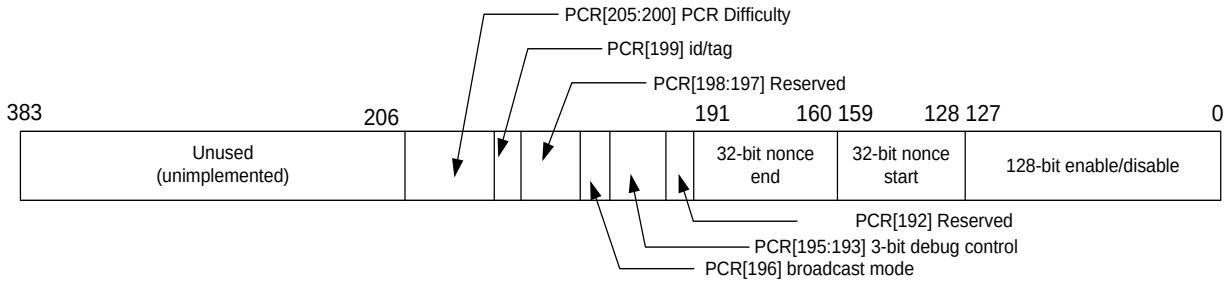


Figure 5-2. Fields of the Pipe Control Register (PCR)

BITS	NAME	DESCRIPTION
[383:206]	RSRV3	Reserved
[205:200]	TARGET	6-bit PCR target value. **Reset Value: 6'h20**
[199]	ENGINE_ID	Overwrite 7 bits of tag with hash engine id number. See §5.2.3. **Reset Value: 1'b0, Merge pipeline id into MSBs of tag disabled**
[198:197]	RSRV2	Reserved
[196]	BCAST	When set, the same input packet is broadcast to all enabled and ready pipes. This is used to allow for [quickly] running the same test in all hash pipes. In this unique situation, more output packets may be generated than input packets were received. **Reset Value: 1'b0, Broadcast mode off**
[195:193]	DBG	3-bit Enumeration for controlling the hash pipes' debug mode. 3'b000—3'b011: Normal operation 3'b1XX: Return 64 bits of hash[255:192] value in lieu of tag and nonce **Reset Value: 3'b000**
[192]	RSRV1	Reserved
[191:160]	END_NONCE	This 32-bit field is the end nonce for the nonce range to be swept. Note, the end value must be larger than or equal to the start value specified in START_NONCE]. **Reset Value: 32'hffff_ffff**
[159:128]	START_NONCE	Starting nonce value for nonce range to be swept. In normal operation this field will be set to 32'h0000_0000. This field and the ending nonce value are provided to allow for sweeping a reduced range typically used during bring-up and debug. **Reset Value: 32'h0000_0000**
[127:0]	HASH_CTRL	Hash Engine enable/disable. This 128-bit vector provides an enable control for each of the Hash Engines. Normal operation is ideally with all 120 engines enabled and thus a value of 120'hffff_ffff_ffff_ffff_ffff_ffff_ffff_ffff[17]. The 120-bit pipe enable/disable vector can be set to any value, however a value of 128'h0 implies that all engines are disabled, and accordingly all work will queue up in the Input FIFO until such time as at least one pipe is enabled. **Reset Value: 128'hffff_ffff_ffff_ffff_ffff_ffff_ffff_ffff**

[17] While the Enable/disable vector is 128 bits, the Goldstrike1™ only contains 120 physical hash engines. Every 16th engine is missing. Enabling or disabling these engines has no affect.

5.1.3 Block-header Packet

The Goldstrike1™ receives 384-bit Bitcoin Block-header packets from the SPI interface. These packets are stored in the Input FIFO and transferred to the Hash Engines as they request work. The format of the packet is as follows

Table 5-2. Block-header Format

BITS	NAME	DESCRIPTION
[383:352]	TAG_ID	Arbitrary 32-bit value passed along verbatim by hash pipeline
[351:96]	SHA	midstate = 256-bit SHA state after processing first 64-byte chunk of 80 byte header
[95:64]	MERKLE_ROOT	Final 32-bits of merkle root (because first portion of merkle root is already incorporated in first 64-byte chunk.)
[63:32]	TIME_STAMP	Timestamp from the block header
[31:0]	TARGET	Difficulty Target from the block header

The CPU sends block-headers to the Goldstrike1™ through the Input FIFO. This FIFO is capable of holding up to 128 headers. As Hash Engines become free, they will request a new block header from the FIFO. The CPU must ensure the Input FIFO does not go empty or the Goldstike1™ will not be fully utilized. The depth of the Input FIFO can be monitored through the status bits available every time data is sent to the device. Status is sent along with the Hash Engine Results packets.

5.1.4 Hash Engine Results Packet Format

The CPU master SPI controller will transfer 400 bits (or 25 words) of data as shown in Table 5-1. This packet size allows the Goldstrike1™ to transfer up to 4, 80-bit Hash Engine results for every block-header, PCR or NOP packet received. The remaining 80-bits are utilized to transfer status information. The Hash Engine Results packet is described in Figure 5-3.

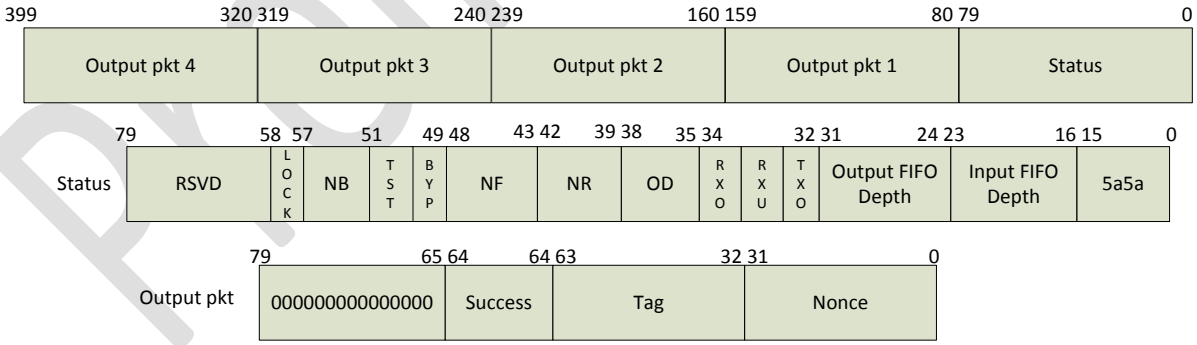


Figure 5-3 Hash Engine Response Transfers (as seen by the SPI receiver)

The status field provides critical operational parameters for the CPU software drivers. The fields are described below.

Table 5-3. Goldstrike1™ Status Fields

BITS	NAME	DESCRIPTION
[79:58]	RSVD	Reserved (all 0's when read)
[57]	PLL_LOST_LOCK	PLL Lost Lock value from the PLL control logic. Refer to 4.2.4
[56:51]	PLL_NB	NB-1 value from the PLL control logic. Refer to 4.2.2
[50]	PLL_TEST	Test value from the PLL control logic. Refer to 4.2.2
[49]	PLL_BYPASS	Bypass value from the PLL control logic. Refer to 4.2.2
[48:43]	PLL_NF	NF-1 value from the PLL control logic. Refer to 4.2.2
[42:39]	PLL_NR	NR-1 value from the PLL control logic. Refer to 4.2.2
[38:35]	PLL_OD	OD-1 value from the PLL control logic. Refer to 4.2.2
[34]	RXOVR	Receive Overrun interrupt – indicates the Goldstrike1™ logic attempted to write to a full receive FIFO on the Goldstrike1™ SPI Interface
[33]	RXUDR	Receive Underrun interrupt – indicates no data was available from the receive FIFO on the Goldstrike1™ SPI Interface during a SPI transfer
[32]	TXOVR	Transmit Overrun interrupt – indicates data was written into a full transmit buffer FIFO in the Goldstrike1™ SPI Interface during a SPI transfer
[31:24]	OFIFO_DEPTH	current depth (or number of entries in the Output FIFO)
[23:16]	IFIFO_DEPTH	current depth (or number of entries in the Input FIFO)
[15:0]	SYNC	Hex value 5A5A.

Output Packets are generated each time a Hash Engine completes its assigned work. Hash Engines generate output packets regardless of whether a problem solution met the required success criteria. The output packet fields are described below.

Table 5-4. Goldstrike1™ Output Packet Fields

BITS	NAME	DESCRIPTION
[79:65]	RSVD	Reserved (all 0's when read)
[64]	SUCCESS	Success flag: 0: no nonce was found that met the Bitcoin target 1: a nonce was found that met the Bitcoin target
[63:32]	TAG_ID	Tag ID given in the Block-header
[31:0]	NONCE	Nonce value: if SUCCESS=1, value of nonce which met the Bitcoin target; if SUCCESS=0, the last value of nonce attempted

5.2 Debug Modes

The debugging scheme is provided via bits of the PCR.

5.2.1 Hash Value Debug

By combining use of the nonce start/end range fields and the enable/disable vector with the debug mode, it is possible to coerce the Goldstrike1™ to have a given hash pipe return the *actual hash* results of the double hash problem for a given nonce rather than the nonce resulting from the search. Operation is straightforward. The PCR is set as:

- The enable/disable vector (PCR[127:0]) is set to enable only the pipe of interest,

- The start nonce field (PCR[159:128])is set to the nonce value to be used.
- The end nonce field (PCR[191:160]) is set to some arbitrarily large value >= start nonce.
- The debug field (PCR[195:193]=1XX) is set to request the computed hash value. Since the hash result is 256 bits and the output packet is 65 bits, only the upper 64 bits of the hash is forwarded to the Output FIFO.

Note in debug mode, the MSB is still set as the found/not-found result of the nonce search (see Figure 5-4).

5.2.2 Hash Engine Debugging

When PCR[199] is set, the Goldstrike1™ will insert the hash engine id (0-127) in lieu of bits 56-62 of the normal tag field.

Note: *Hash Value Debug takes precedence over Hash Engine Debug.*

5.2.3 Debug Output FIFO Formats

The Output FIFO packet formats are shown in Figure 5-4. Figure 5-4A shows the format in normal operation in which the tag is copied verbatim from the input packet and the nonce field is either the nonce value found (if Success flag is set) or is the final nonce value tried. In Figure 5-4B and Figure 5-4C the variants of the output packet for debug mode are shown.

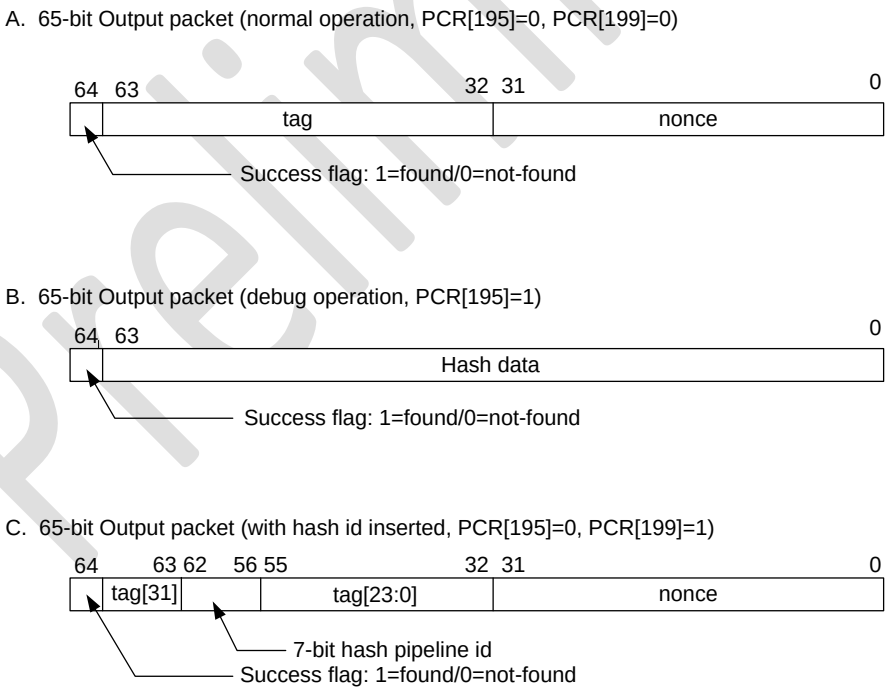


Figure 5-4 Output Packet Format Normal and Debug Modes

In Figure 5-4B, PCR bit 195 is set indicating the hash computation should be returned instead of the normal nonce/tag values.

In Figure 5-4C PCR bit 195 is not set, and PCR bit 199 is, indicating the hash engine ID is to replace bits 24-30 of the tag.

5.2.4 Broadcast Mode

Overclocking the Goldstrike1™ can result in hash errors due to increased frequency, thermal and voltage stresses on the dies. Which engines will be affected is unknown and needs to be determined. Broadcast mode is utilized to override the Input FIFO's selection of the lowest-numbered ready hash engine and instead have the Input FIFO send data to all ready hash engines. This has the effect of generating multiple output packets for the same input packet; assuming all engines are idle at the time the packet reaches the bottom of the Input FIFO. The intent of the broadcast mode is to test all hash engines simultaneously with the same block header problem to determine if data integrity has been compromised in any of the engines. Given that identical packets are being sent to each of the hash pipelines, it's required to also enable PCR[199] to have the hash pipe id merged into the tag. In the case of a data mismatch, this allows for determining which hash engine(s) produced the faulty data. Note, broadcast mode can also be used with the hash engine debug mode described in Section 5.2.2 In general, broadcast mode is only useful when a single input packet is going to be provided to the Goldstrike1™, the reason being that following the broadcast of the first packet, the participating hash pipelines will necessarily receive and compute their results at the same time, but will be serialized upon writing to the Output FIFO, thus causing them to no longer be exactly in sync.

Note: the software must execute the following process when utilizing the broadcast mode:

1. Set the BCAST and ENGINE_ID bits in the PCR – writing the PCR will result in a soft reset of the Goldstrike1™. Wait for the system to stabilize, i.e. the PLL to lock (see Section 4.2.3).
2. Send a known good packet.
3. Collect all results from the hash engines – all engines must finish and go idle.
4. Repeat steps 2 & 3 if required.
5. Reset the BCAST and ENGINE_ID bits in the PCR and disable engines which returned incorrect calculations – this will result in a soft reset of the Goldstrike1™. Wait for the system to stabilize, i.e. the PLL to lock (see Section 4.2.3).
6. Continue with normal work traffic.

5.3 Thermal Diode

The Goldstrike1™ thermal diode intended for measuring the die temperature of an operating chip. The temperature sensing diode generates a voltage drop that is proportional to temperature, and is compatible with standard discrete components 2N3906 PNP or 2N3904 NPN which are specified to be used with temperature monitor IC's.

The thermal diode design utilizes an on chip PNP transistor whose base-emitter junction with its collector shorted to ground. A thermal sensor IC on the system board may monitor the temperature of the product it is integrated with for thermal management and fan speed control.

Table 5-5 Thermal Diode Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT	Notes
I_{fwd}	Forward Bias Current	5		200	µA	[18]
I_e	Emitter current (fwd)	5		200	µA	
n_Q	Transistor Ideality	1.01745	1.02	1.02255		[19]
R_s	Series Resistance	0.5		3	Ohm	[20]

5.4 Goldstrike1™ Monitoring Signals

5.4.1 Heartbeat

The DBG_HEART_BEAT signal is driver by a 31-bit counter as shown below:

Figure 5-5 Debug Heart Beat Logic

This circuit divides the PLL clock by 2^{30} = 1,073,741,824. The heartbeat rates are shown in Table 4-3.

5.4.2 PLL Debug Pins

The Goldstrike1™ has 3 output pins and 1 input pin intended for PLL debug use. These pins should not be used during normal operation. Debug pins on the chip can be used to monitor the PLL lost lock indication (DBG_PLL_LOST_LOCK) as well as the two PLL slip indications directly from the PLL (DBG_PLL_RFSLIP, DBG_PLL_FBSLIP).

- DBG_PLL_RFSLIP goes active for one or more divided feedback VCO cycles when the phase detector misses a divided reference cycle, i.e. when the VCO is running too fast.
- DBG_PLL_FBSLIP goes active for one or more divided reference cycles when the phase detector misses a divided feedback VCO cycle, i.e. when the VCO is running too slow.

  Neither signal is synchronized to the PLL output clock.

- The PLL_BYPASS_IN debug pin should be pulled low external to the chip for normal operation. Driving this pin high will force the PLL into bypass mode so that the system runs off the 50 MHz PLL_REF_CLK.
- DBG_PLL_LOST_LOCK is a sticky signal and one triggered remains set until the system reset signal, RESET_COLD_L, is asserted.

[18] Cointerra does not support or recommend operation of the thermal diode under reverse bias

[19] The ideality factor, nQ represents the deviation from the ideal transistor model behavior as exemplified by the equation for the collector current: Ic=Is((exp(qVbe/(nkT)-1) Where: Is,Ic = saturation current, collector current, respectively; q=electronic charge; Vbe= Voltage across the transistor emitter-base junction; K= Boltzmann Constant; T = absolute temperature in degrees Kelvin.

[20] R_S is provided for series resistance corrections as needed: T_{err} =[R_S(N-1)(I_{fwd} min)]/[(nK/q)ln(N)] Where: T_{err} = sensor temperature error correction; N = sensor current ratio.

6 Mechanical Packaging

6.1 1 die

TBD

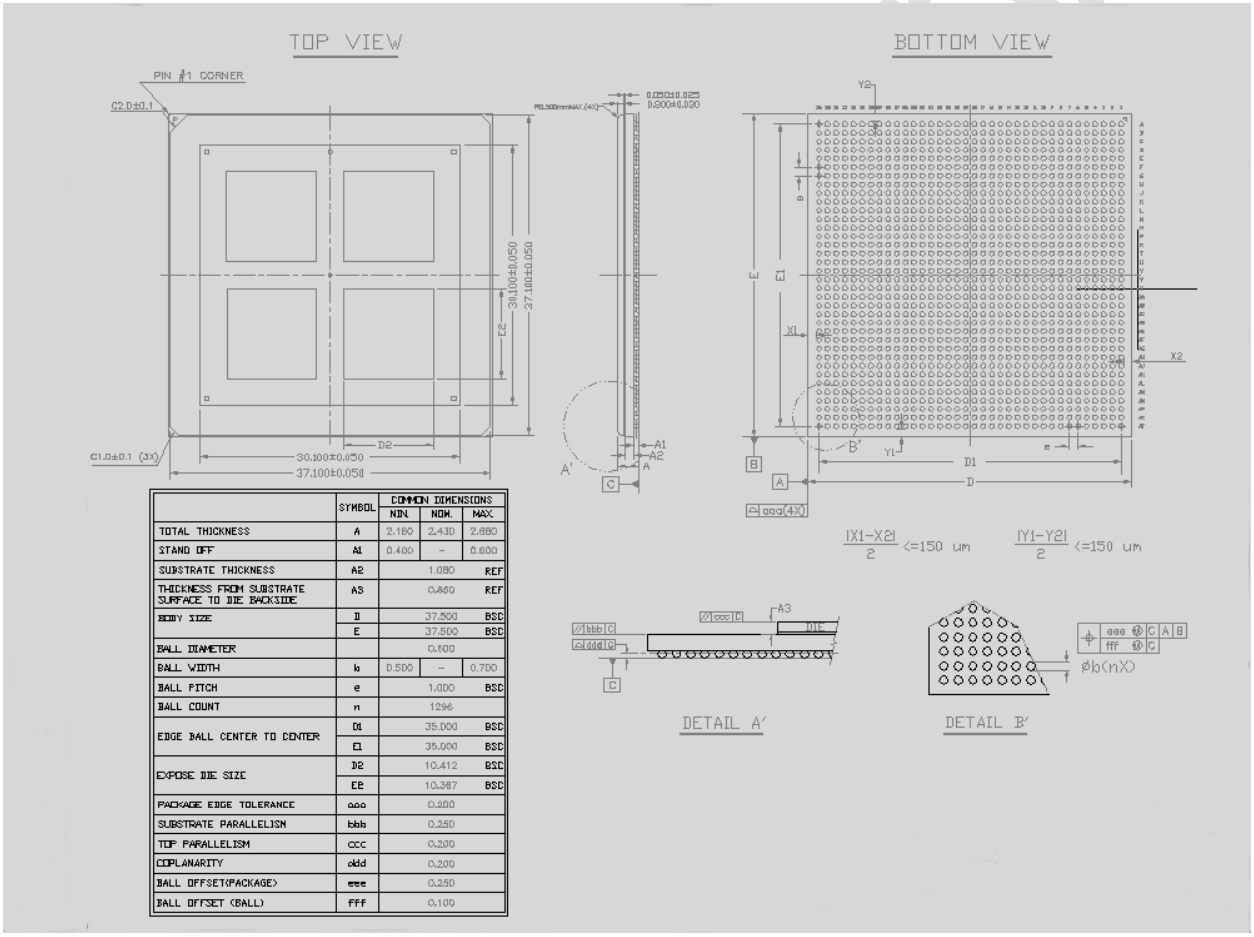
6.2 2 die

TBD

6.3 3 die

TBD

6.4 4 die



	SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.
TOTAL THICKNESS	A	2.180	2.430	2.680
STAND OFF	A1	0.400	–	0.600
SUBSTRATE THICKNESS	A2		1.080	REF
THICKNESS FROM SUBSTRATE SURFACE TO DIE BACKSIDE	A3		0.850	REF
BODY SIZE	D		37.500	BSC
	E		37.500	BSC
BALL DIAMETER			0.600	
BALL WIDTH	b	0.500	–	0.700
BALL PITCH	e		1.000	BSC
BALL COUNT	n		1296	
EDGE BALL CENTER TO CENTER	D1		35.000	BSC
	E1		35.000	BSC
EXPOSE DIE SIZE	D2		10.412	BSC
	E2		10.387	BSC
PACKAGE EDGE TOLERANCE	aaa		0.200	
SUBSTRATE PARALLELISM	bbb		0.250	
TOP PARALLELISM	ccc		0.200	
COPLANARITY	ddd		0.200	
BALL OFFSET(PACKAGE)	eee		0.250	
BALL OFFSET (BALL)	fff		0.100	

7 Applications

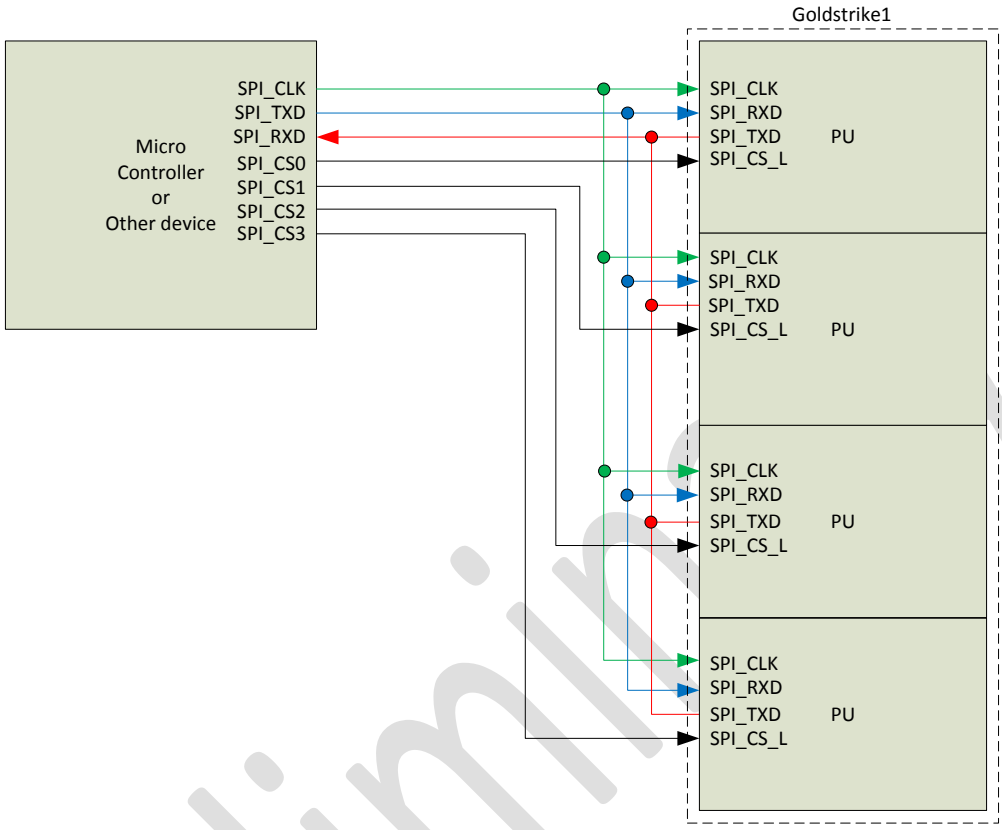


Figure 7-1 SPI Connections to 4-die Goldstrike1™

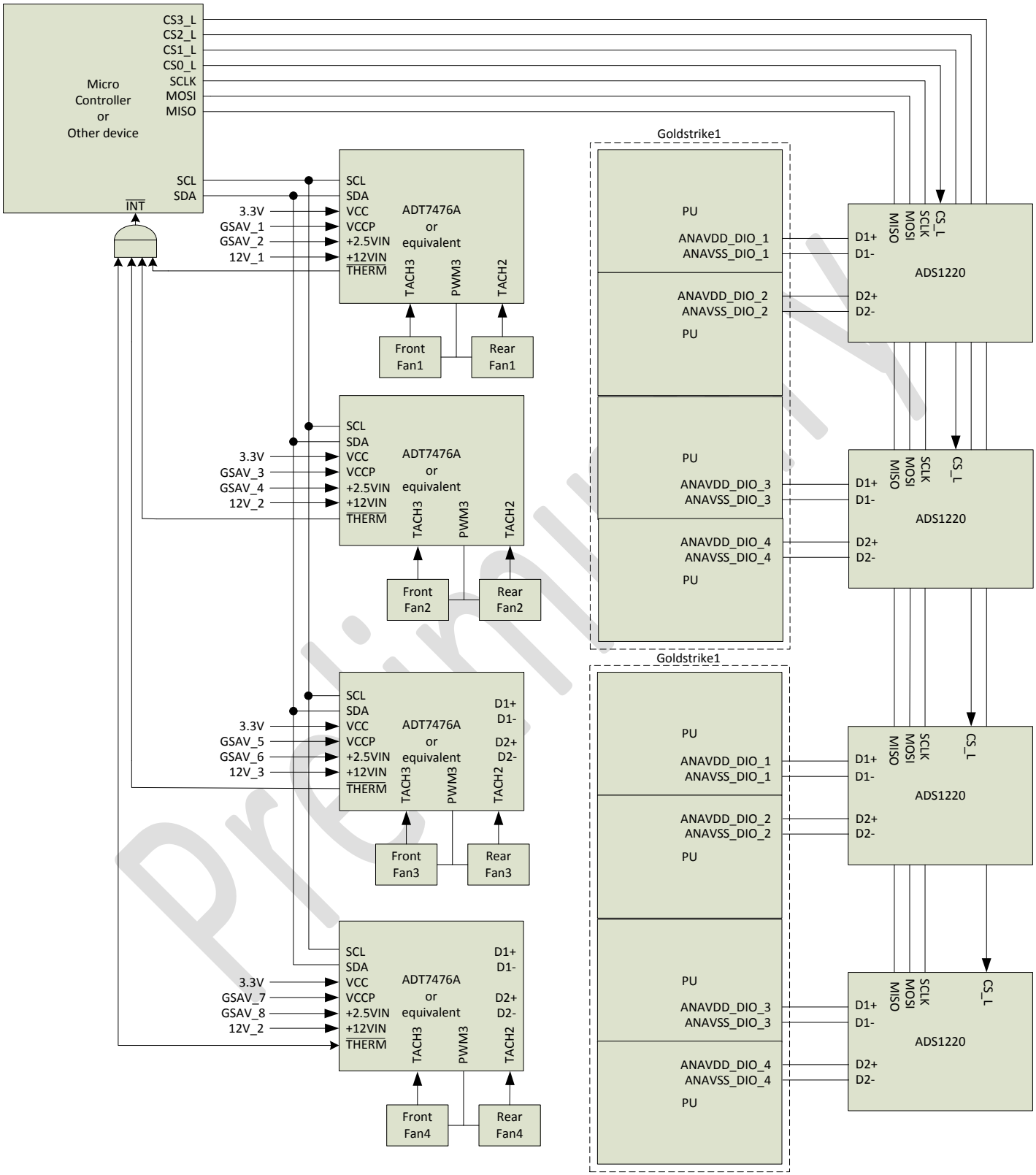


Figure 7-2 Thermal Monitoring/Fan Control for 4-die Goldstrike1™

8 Part Numbering

Part Number	Hash Rate GH/s @1.05GHz	Hash Engines	Thermal Diodes	SPI	Overclocking[21]	Voltage Sense Lines	Package
GS1C120FA	126	120	1	1	Y	1	TBD
GS1C240FA	252	240	2	2	Y	2	TBD
GS1C360FA	378	360	3	3	Y	3	TBD
GS1C480FA	504	480	4	4	Y	4	1296FCBGA

[21] The Goldstrike1™ can be overclocked to 1.1GHz as a maximum reliable frequency. Overclocking Goldstrike1™devices above 1.1GHz may not be reliable and cannot be guaranteed to function properly. The System Designer is responsible for operating the Goldstrike1™ at safe thermal levels per Table 3-1.