Lab 3 Report

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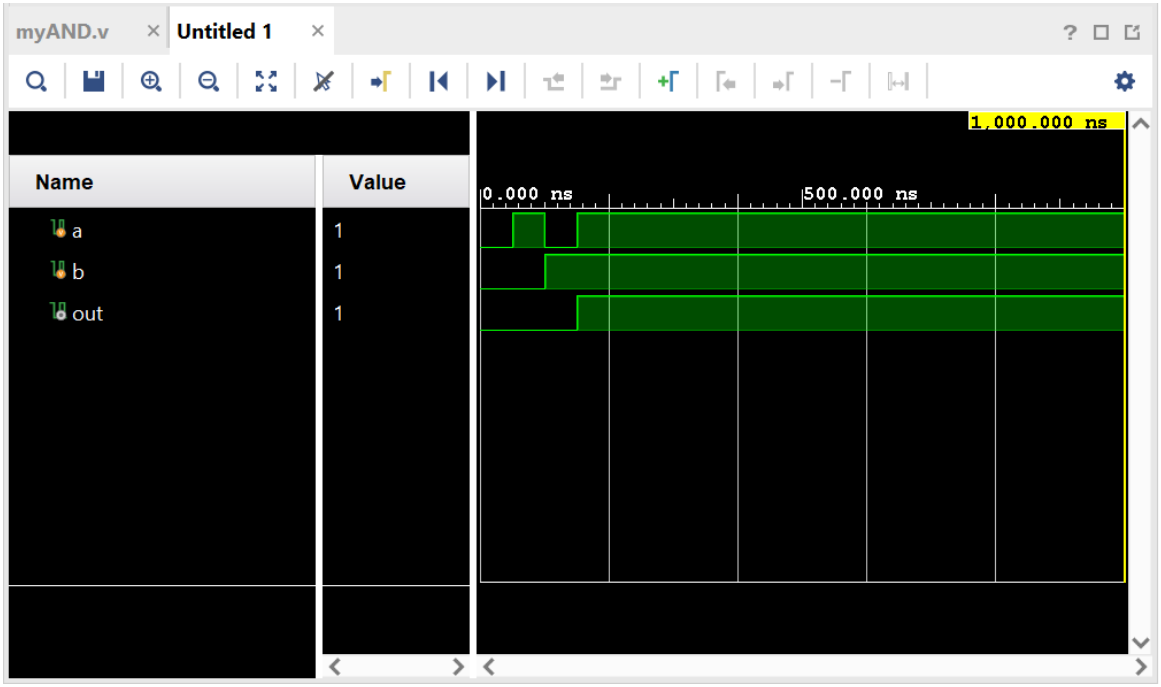
Part 1 –

i. Waveform of the Structural AND Gate:



ii. Constraints File:

```
## Switches
## Connects pin V17 (SW0 on the board) to input a in our gate module
set_property PACKAGE_PIN V17 [get_ports {a}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]

## Connects pin V16 (SW1 on the board) to input b in our gate module
```

```
set_property PACKAGE_PIN V16 [get_ports {b}]
## Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]

## LEDs
## Connects the output c in our gate module to pin U16 (LED0 on-board)
set_property PACKAGE_PIN U16 [get_ports {out}]
## Sets the LED to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {out}]
```

Part 2 –

iii. Constraints File Code:

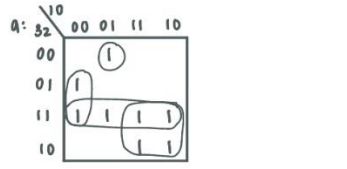
```
## Switches
# Connects pin V17 (SW0 on the board) to input a in our gate module
set_property PACKAGE_PIN V17 [get_ports {right}]
# Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {right}]

# Connects pin V16 (SW1 on the board) to input b in our gate module
set_property PACKAGE_PIN V16 [get_ports {left}]
# Sets the switch to use 3.3V logic
        set_property IOSTANDARD LVCMOS33 [get_ports {left}]

set_property PACKAGE_PIN W16 [get_ports {up}]
        set_property IOSTANDARD LVCMOS33 [get_ports {up}]

set_property PACKAGE_PIN W13 [get_ports {center}]
        set_property IOSTANDARD LVCMOS33 [get_ports {center}]
```

Part 3 –

iv. Truth Table:

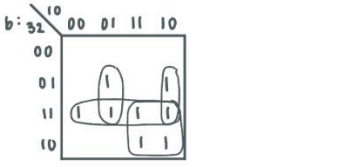
in3	in2	in1	in0	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0
1	0	1	0	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1

v, vi. Minimized Output Equations and K-Maps



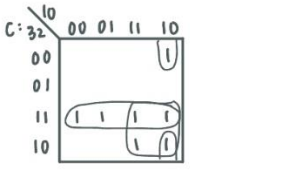
3 4 1 2

a = i3'i2'i1'i0 + i2i1'i0' + i3i2 + i3i1



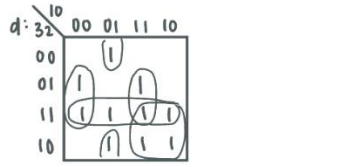
1 2 5 6

b = i3i2 + i3i1 + i2i1'i0 + i2i1i0'



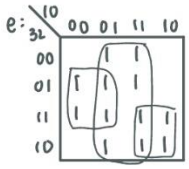
1 2 7

c = i3i2 + i3i1 + i2'i1i0'



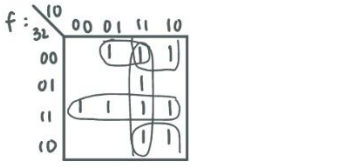
1 2 8 9 10

d = i3i2 + i3i1 + i2'i1'i0 + i2i1'i0' + i2i1i0



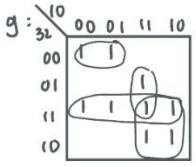
11 1

e = i0 + i2i1' + i3i1



2 12 13 14

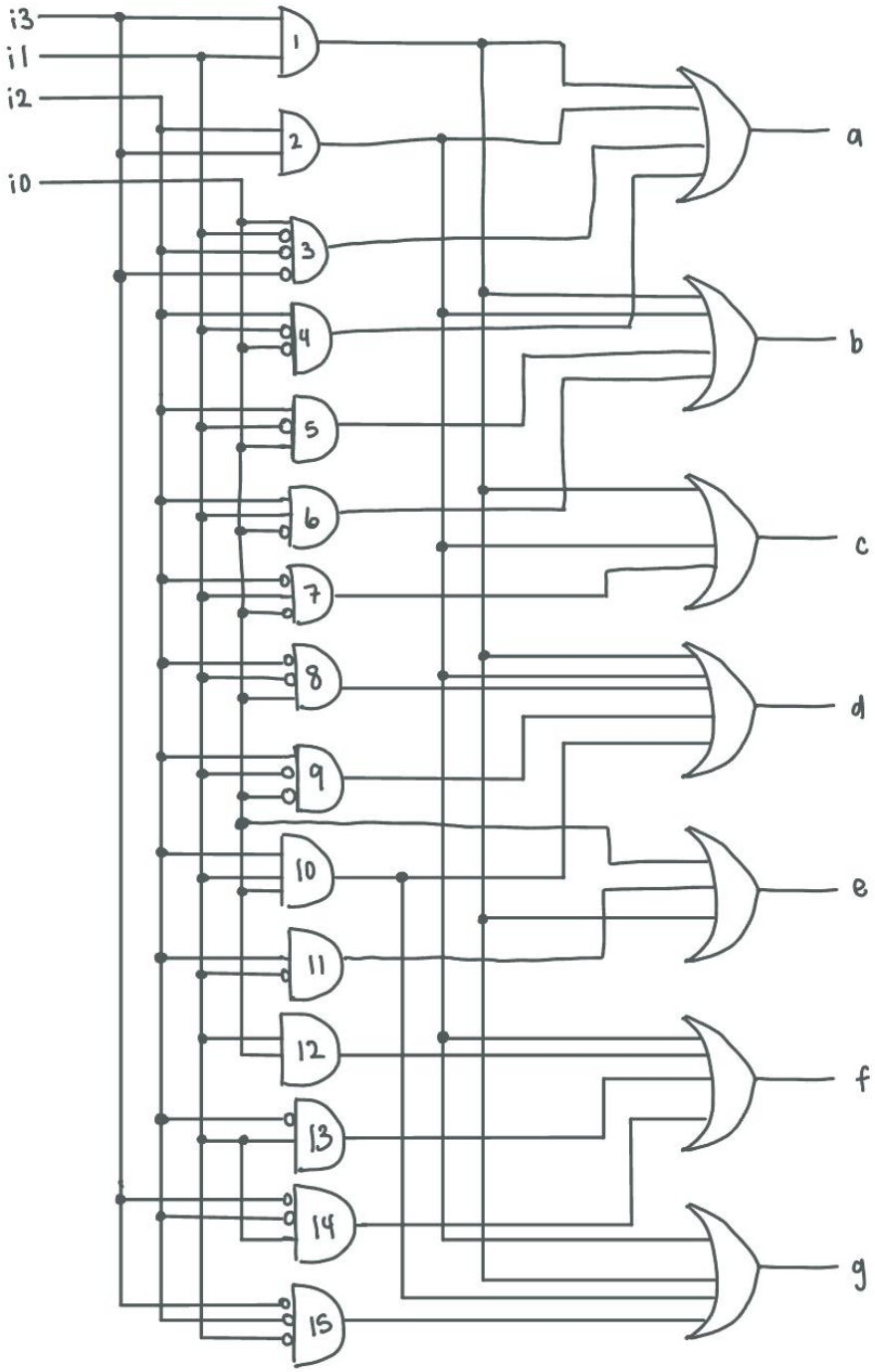
f = i3i2 + i1i0 + i2'i1 + i3'i2'i0



1 2 15 10

g = i3i2 + i3i1 + i3'i2'i1' + i2i1i0

Gate Level Design:



vii. Structural Modeling Verilog Code:

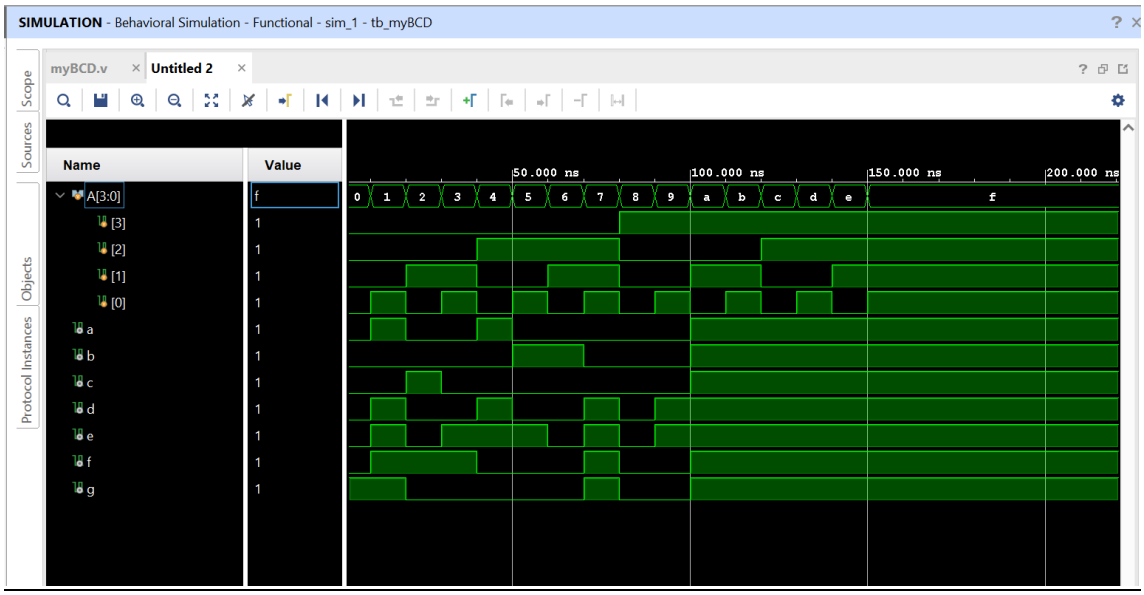
```
`timescale 1ns / 1ps

// module definition
module myBCD(
   input in3, in2, in1, in0,   // input port declarations
   output a, b, c, d, e, f, g, AN0, AN1, AN2, AN3  // output port declarations
   );

   // internal signal declarations
   wire not3, not2, not1, not0,
      combo1, combo2, combo3, combo4,
      combo5, combo6, combo7, combo8,
      combo9, combo10, combo11, combo12,
      combo13, combo14, combo15;

   // assign value 0 to LCD to be used, 1 to rest
   assign AN0 = 0;
   assign AN1 = 1;
   assign AN2 = 1;
   assign AN3 = 1;

   // not gates for each input
   not int0 (not0, in0);
   not int1 (not1, in1);
   not int2 (not2, in2);
   not int3 (not3, in3);
```

```
    // and gates for each product term
    and t1 (combo1, in3, in2);
    and t2 (combo2, in3, in1);
    and t3 (combo3, not3, not2, not1, in0);
    and t4 (combo4, in2, not1, not0);
    and t5 (combo5, in2, not1, in0);
    and t6 (combo6, in2, in1, not0);
    and t7 (combo7, not2, in1, not0);
    and t8 (combo8, not2, not1, in0);
    and t9 (combo9, in2, not1, not0);
    and t10 (combo10, in2, in1, in0);
    and t11 (combo11, in2, not1);
    and t12 (combo12, in1, in0);
    and t13 (combo13, not2, in1);
    and t14 (combo14, not3, not2, in0);
    and t15 (combo15, not3, not2, not1);

    // final output combos
    or outa (a, combo1, combo2, combo3, combo4);
    or outb (b, combo1, combo2, combo5, combo6);
    or outc (c, combo1, combo2, combo7);
    or outd (d, combo1, combo2, combo8, combo9, combo10);
    or oute (e, combo2, in0, combo11);
    or outf (f, combo1, combo12, combo13, combo14);
    or outg (g, combo1, combo2, combo10, combo15);

endmodule
```

Testbench Code:

```
`timescale 1ns / 1ps

// testbench for myBCD module
module tb_myBCD;

   // create inputs of reg type
   reg [3:0] A;
   wire a, b, c, d, e, f, g;   // make outputs wires

   // instantiate module to be simulated
   myBCD uut (.in0(A[0]), .in1(A[1]), .in2(A[2]), .in3(A[3]),  // port declarations
            .a(a), .b(b), .c(c), .d(d), .e(e), .f(f), .g(g));

   initial begin

   for (A = 0; A < 4'b1111; A = A + 1) // use for loop to test all possible input combinations
      #10;

   end
endmodule
```

viii. Simulation Waveform



ix. <u>Constraints file:</u>

Switches

Connects pin V17 (SW0 on the board) to input a in our gate module

set_property PACKAGE_PIN V17 [get_ports {in0}]

Sets the switch to use 3.3V logic

set_property IOSTANDARD LVCMOS33 [get_ports {in0}]

Connects pin V16 (SW1 on the board) to input b in our gate module

set_property PACKAGE_PIN V16 [get_ports {in1}]

Sets the switch to use 3.3V logic

set_property IOSTANDARD LVCMOS33 [get_ports {in1}]

set_property PACKAGE_PIN W16 [get_ports {in2}]

set_property IOSTANDARD LVCMOS33 [get_ports {in2}]

set_property PACKAGE_PIN W17 [get_ports {in3}]

set_property IOSTANDARD LVCMOS33 [get_ports {in3}]

```
#7 segment display
set_property PACKAGE_PIN W7 [get_ports {a}]
	set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W6 [get_ports {b}]
	set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN U8 [get_ports {c}]
	set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V8 [get_ports {d}]
	set_property IOSTANDARD LVCMOS33 [get_ports {d}]
set_property PACKAGE_PIN U5 [get_ports {e}]
	set_property IOSTANDARD LVCMOS33 [get_ports {e}]
set_property PACKAGE_PIN V5 [get_ports {f}]
	set_property IOSTANDARD LVCMOS33 [get_ports {f}]
set_property PACKAGE_PIN U7 [get_ports {g}]
	set_property IOSTANDARD LVCMOS33 [get_ports {g}]

#set_property PACKAGE_PIN V7 [get_ports dp]
	#set_property IOSTANDARD LVCMOS33 [get_ports dp]

set_property PACKAGE_PIN U2 [get_ports {AN0}]
	set_property IOSTANDARD LVCMOS33 [get_ports {AN0}]
set_property PACKAGE_PIN U4 [get_ports {AN1}]
	set_property IOSTANDARD LVCMOS33 [get_ports {AN1}]
set_property PACKAGE_PIN V4 [get_ports {AN2}]
	set_property IOSTANDARD LVCMOS33 [get_ports {AN2}]
set_property PACKAGE_PIN W4 [get_ports {AN3}]
	set_property IOSTANDARD LVCMOS33 [get_ports {AN3}]
```