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Group : EC31

Lab : VLSI lab

Experiment Title: Input and Output Characteristics of NMOS Using Cadence

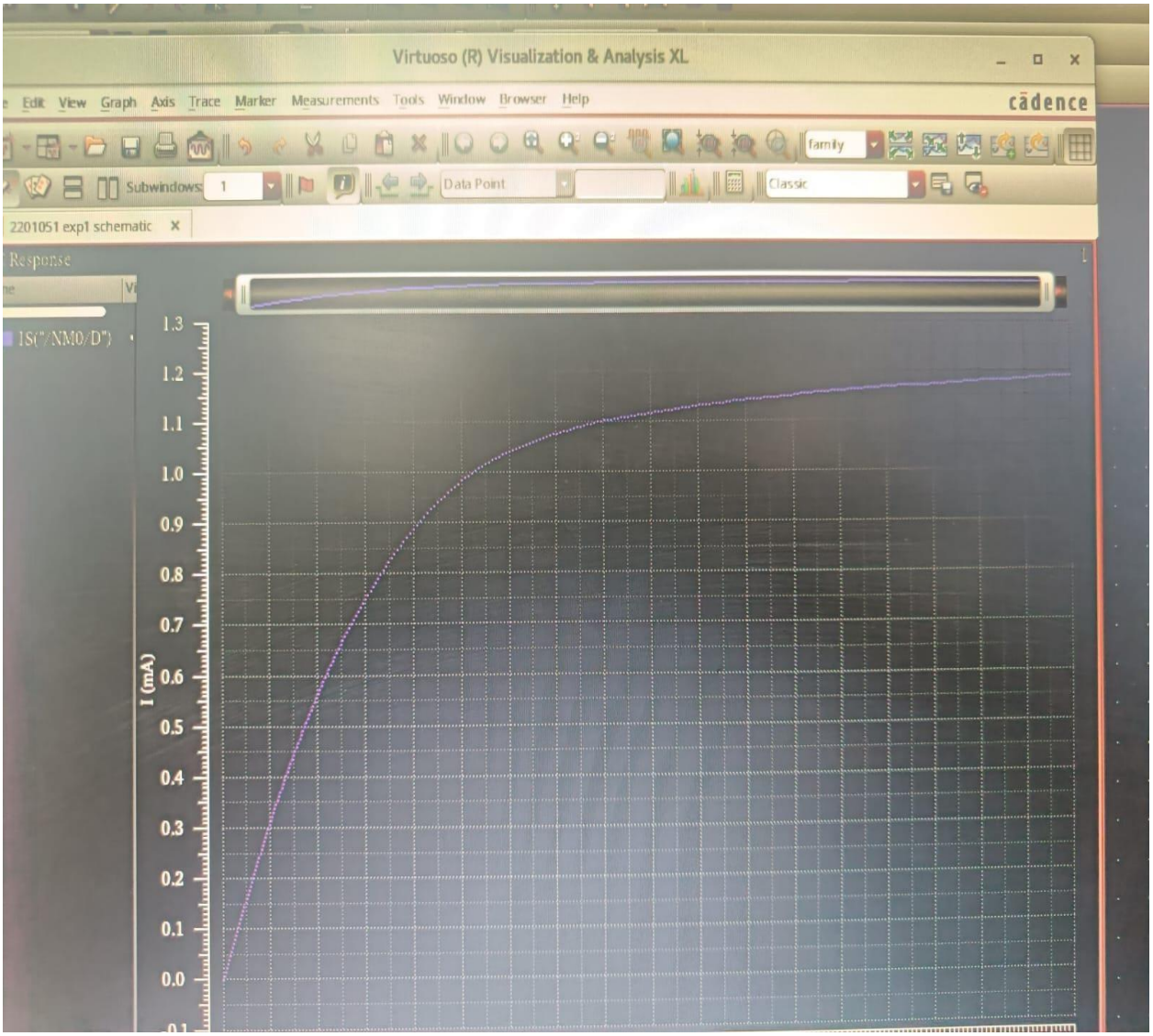
1. **Objective:**

The objective of this experiment is to analyze the input and output characteristics of an NMOS transistor using Cadence Virtuoso. This includes observing the **transfer characteristics (Id vs. Vgs)** and **output characteristics (Id vs. Vds)** of the NMOS transistor.

Circuit Design and Setup:

1. **Schematic Design:**
    - Open Cadence Virtuoso and create a new schematic. ○ Place an NMOS transistor (e.g., from a 180nm/130nm PDK). ○ Connect the **drain** to a DC voltage source **Vds**. ○ Connect the **gate** to a DC voltage source **Vgs**. ○ Connect the **source** to **ground (0V)**.
    - Place a **current probe** at the drain to measure **Id**.
2. **Simulation Setup:**
    - Open **ADE-L/XL** and set up a **DC Analysis**.
    - For **output characteristics (Id vs. Vds):**
        - Sweep **Vds** from 0V to a maximum value (e.g., 2V).
        - Set **Vgs** at multiple fixed values (e.g., 0.5V, 1V, 1.5V, etc.). ○ For **transfer characteristics (Id vs. Vgs):**
        - Sweep **Vgs** from 0V to a maximum value (e.g., 2V) while keeping **Vds** fixed (e.g., 1V).
    - ○ Run the simulations and save the results.

Results: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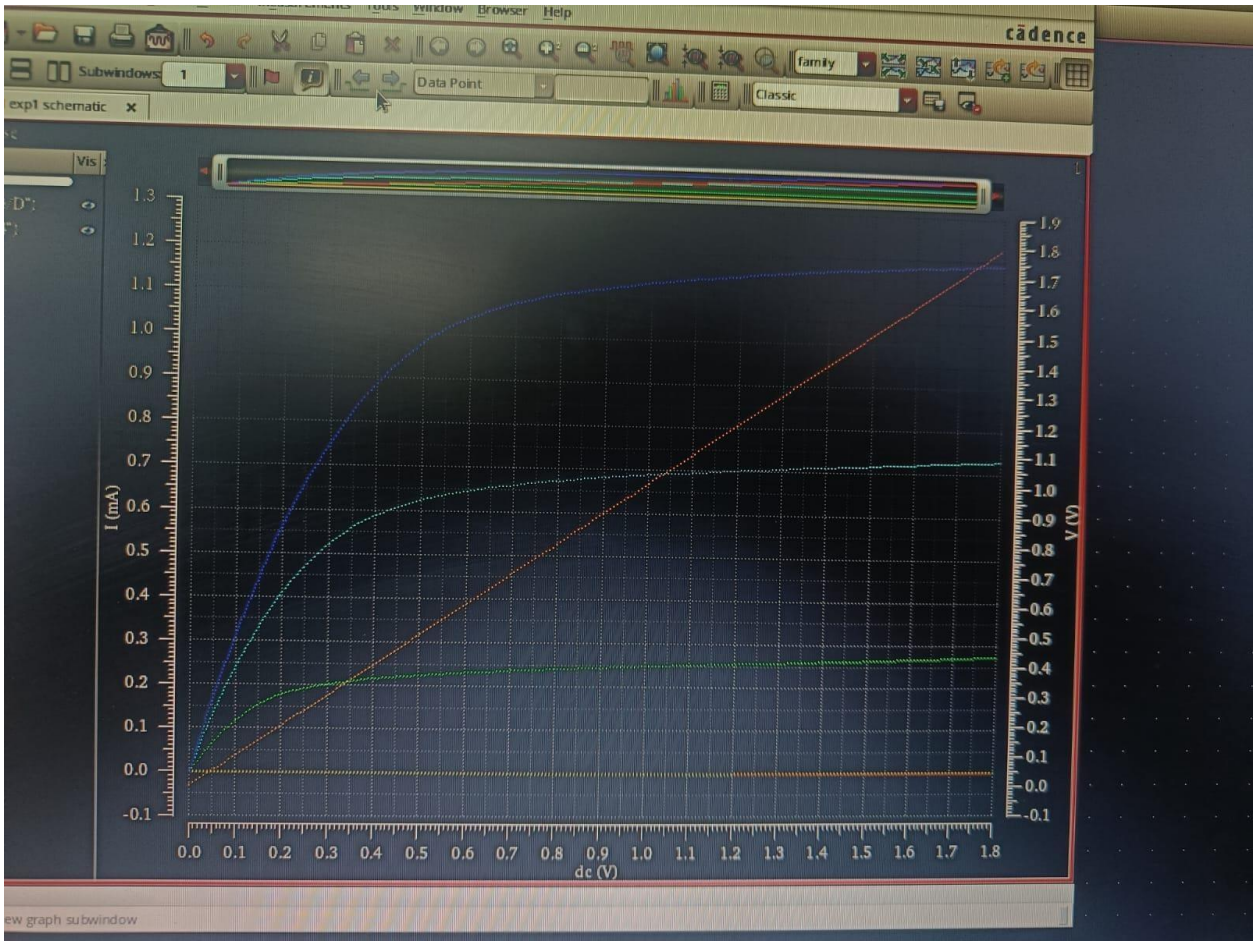
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Observations:

Output Characteristics (Id vs. Vds):

- For low **Vds**, **Id** increases linearly, indicating the **ohmic region**.
- As **Vds** increases, **Id** saturates, indicating the **saturation region**.
- Higher **Vgs** values lead to higher **Id**, following the MOSFET equations.

Transfer Characteristics (Id vs. Vgs):

- **Id** increases exponentially when **Vgs** surpasses the **threshold voltage (Vth)**.
- The transistor remains **off** for **Vgs < Vth**.
- **Id** follows the quadratic relationship with **Vgs** in the saturation region.

Conclusion:

This experiment successfully demonstrated the input and output characteristics of an NMOS transistor using Cadence Virtuoso. The simulation results validated theoretical MOSFET behavior, with **Id vs. Vgs** showing a threshold voltage dependency and **Id vs. Vds** confirming the transition from the ohmic region to saturation.

Experiment 2: Input and Output Characteristics of PMOS Transistor

Objective

To study and plot the input and output characteristics of a PMOS transistor using Cadence Virtuoso.

Tools Used

- Cadence Virtuoso
- Spectre Simulator
- GPDK 180nm PDK (or your used PDK)

Theory

A PMOS transistor is a type of MOSFET where holes are the majority carriers. It turns **ON** when the gate-to-source voltage VGSV_{GS} is **less than** the threshold voltage VthV_{th}.

Regions of Operation

1. **Cut-off:** VSG<VthV_{SG} < V_{th}
2. **Linear (Triode):** VSD<VSG−VthV_{SD} < V_{SG} - V_{th}
3. **Saturation:** VSD≥VSG−VthV_{SD} \geq V_{SG} - V_{th}

Schematic Setup

- **PMOS transistor** (from analogLib)
- Connect **source to VDD**, **gate to DC voltage source**, and **drain to VDS sweep source**.

- Bulk tied to source (VDD).

Simulations Performed

1. Output Characteristics (Id vs VSD)

- **Sweep VSD** from 0 to VDD (e.g., 0 to 1.8V)
- **VSG** fixed at multiple values (e.g., 1.2V, 1.5V, 1.8V)

2. Input Characteristics (Id vs VSG) **Sweep VSG** from 0 to VDD

- **VSD** constant (e.g., VSD = 1.8V)

Steps in Cadence Virtuoso

1. **Design the schematic** as per PMOS biasing.
2. **Launch ADE (Analog Design Environment)**.
3. Choose **DC analysis**:
    - For output: VSD sweep; VSG as parameter.
    - For input: VSG sweep; VSD constant.
4. Run simulation.
5. Use **Calculator** or direct plotting to plot Id vs VSD and Id vs VSG.
6. Annotate curves and export graphs.

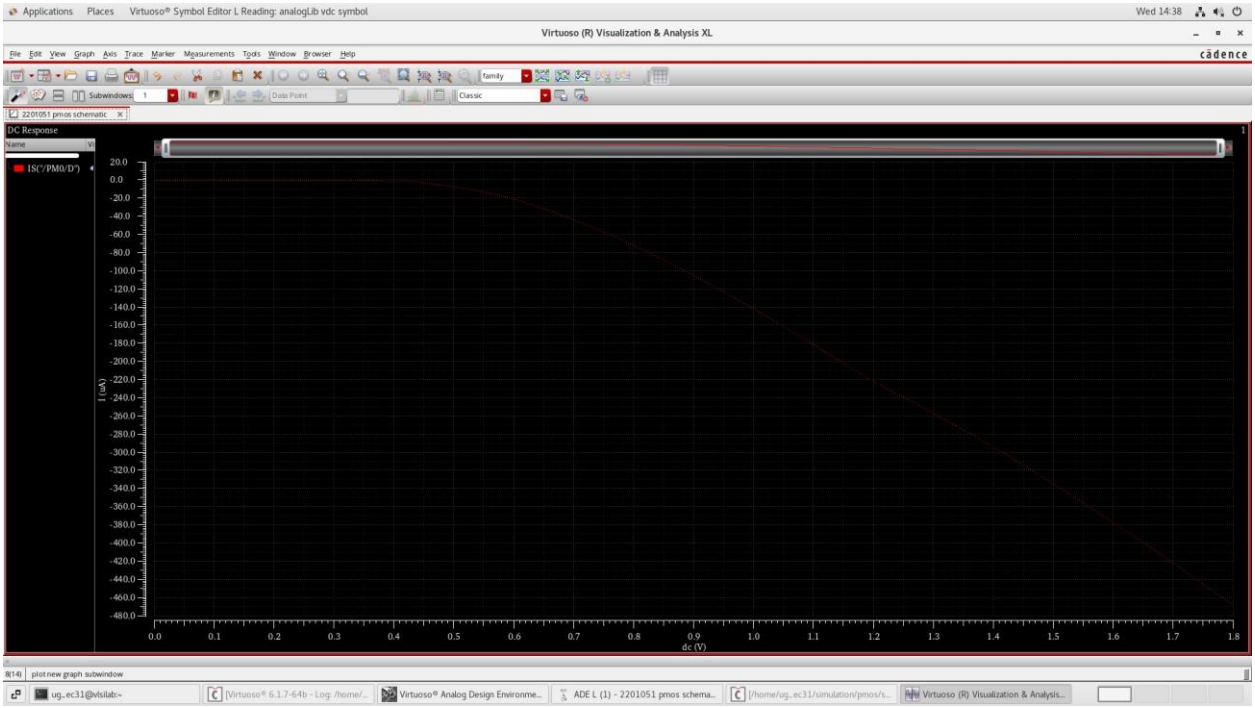
Results

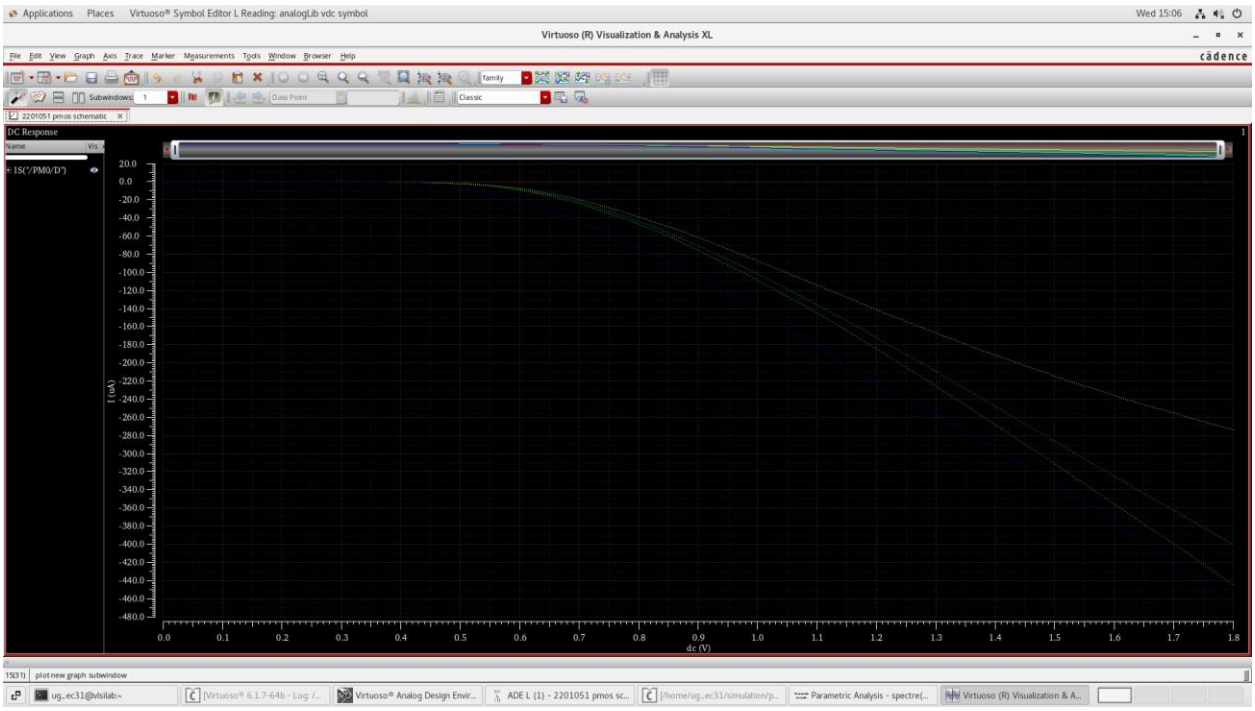
Output Characteristics

- Id increases with VSD initially (linear region), then saturates.
- Higher VSG (more negative gate voltage) increases Id.

Input Characteristics

- Id increases exponentially when VSG increases past threshold (~0.5V).
- Very low current for VSG < Vth.

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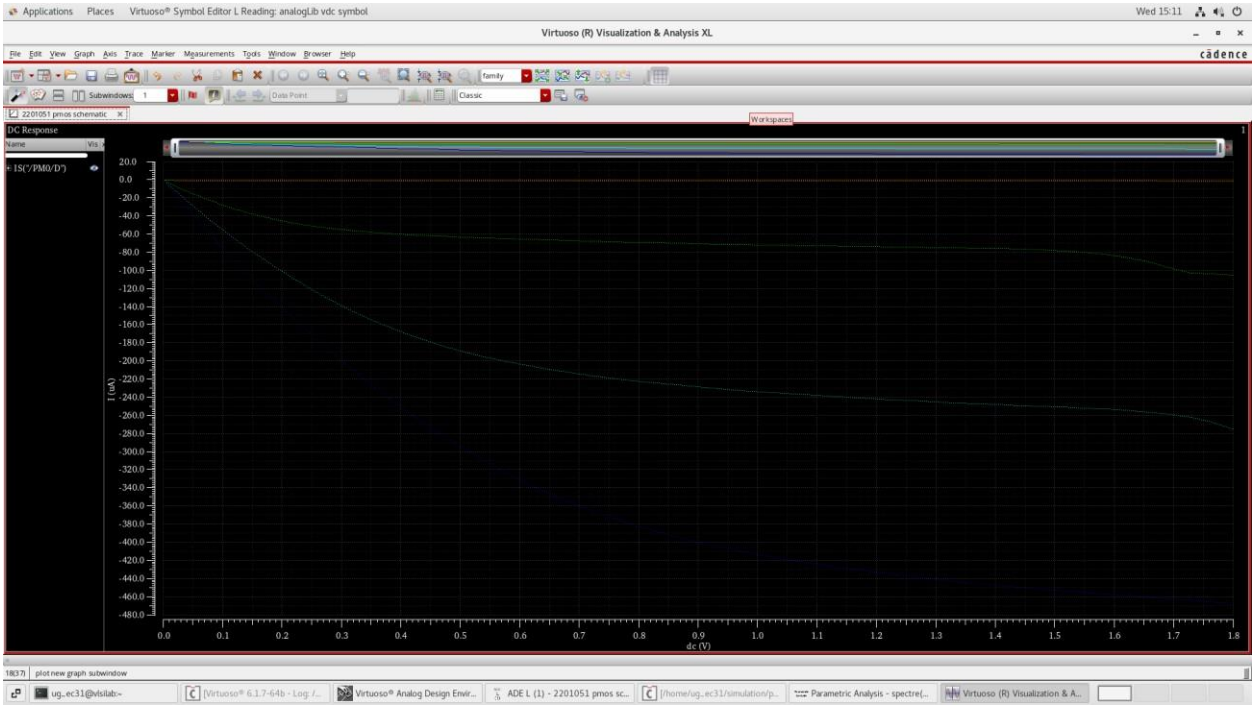
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Conclusion

- PMOS operates in three regions depending on VSG and VSD.
- The characteristics confirm expected PMOS behavior.
- Simulations match theoretical behavior of PMOS.

Observations

- Threshold voltage Vth ~ -0.5V for the PMOS in this PDK.
- PMOS conducts when gate is at lower potential than source.

Experiment 3: **Gain and Phase Response of Common Source Amplifier**

Objective

To analyze the **gain** and **phase response** of a **Common Source (CS) Amplifier** using Cadence Virtuoso.

Tools Used

- Cadence Virtuoso
- Spectre Simulator
- GPDK 180nm PDK (or the PDK you are using)

Theory

The **Common Source amplifier** is a basic analog amplifier configuration using an NMOS transistor. It provides:

- **High voltage gain**
- **180° phase shift** between input and output

Voltage Gain

Av=−gmRDA_v = -g_m R_D

Where:

- gmg_m = transconductance
- RDR_D = drain resistance

The negative sign indicates a **phase inversion**.

Schematic Setup

- **NMOS transistor** (from analogLib) **Biasing**:

- Gate: connected through a resistor to DC voltage (bias) ○ Source: grounded
- Drain: connected to VDD through resistor RDR_D

- **Input**: small AC signal superimposed on gate bias
- **Output**: taken from the drain

Simulation Configuration

1. AC Analysis (Gain & Phase)

- Sweep frequency: 1Hz to 1GHz (log scale)
- AC magnitude: 1V at input (for easy gain reading)

Steps in Cadence Virtuoso

1. **Draw the CS amplifier schematic** with proper biasing.
2. **Launch ADE**.
3. **Set up AC analysis**:
   - AC input source with magnitude 1V
   - Sweep frequency: 1Hz to 1GHz (decade sweep, 10 points/decade) 4. **Run simulation**
5. Use **Calculator**:
   - Gain: v(out)/v(in)
   - Gain in dB: 20*log10(mag(...)) ○ Phase: phase(...)
6. Plot and annotate.

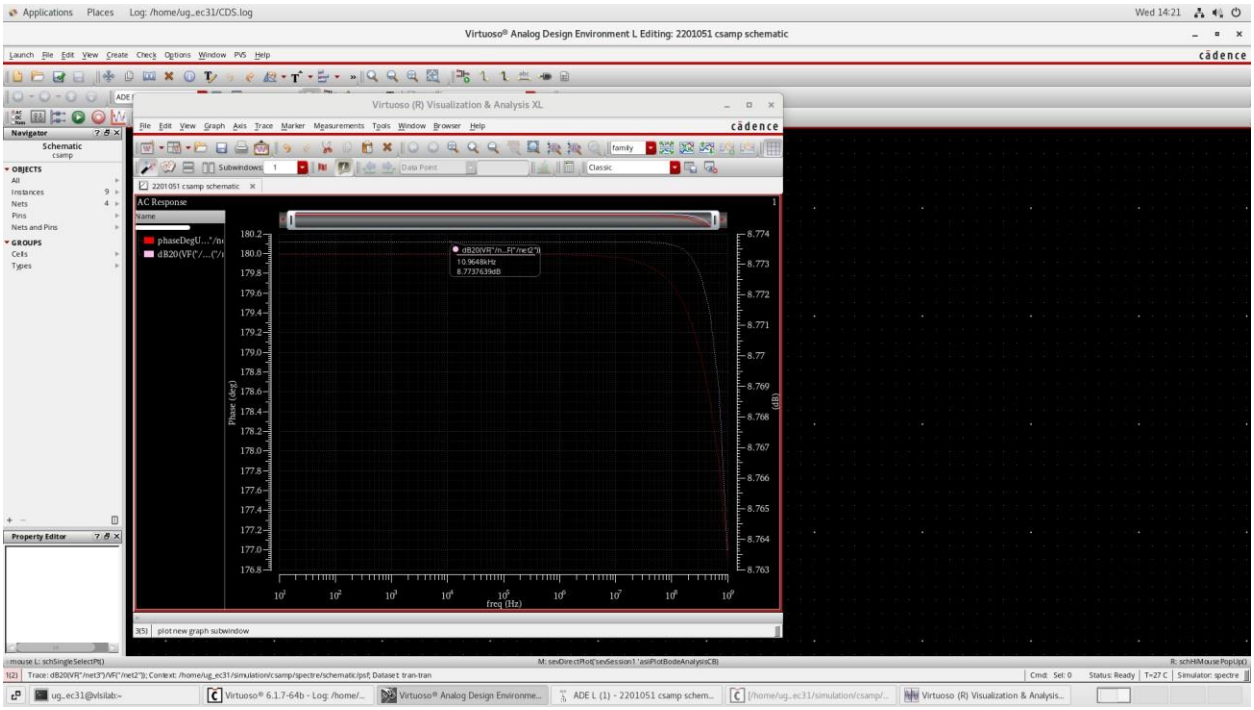
Results

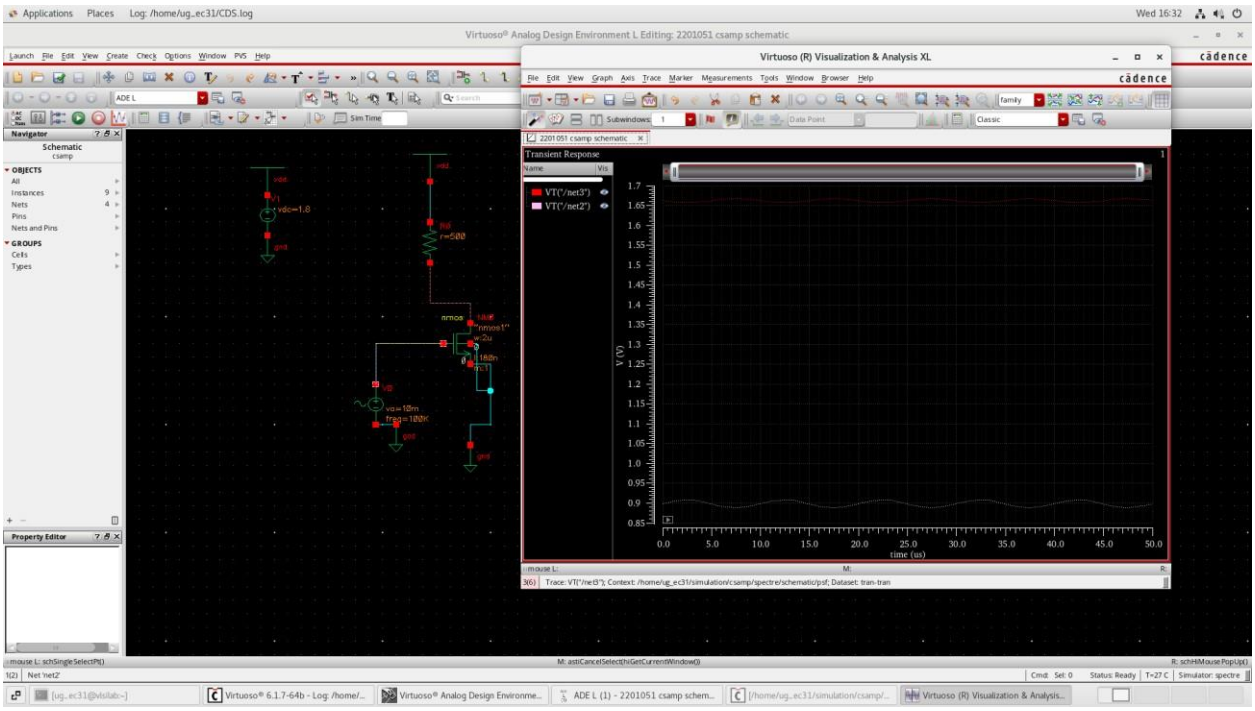
Gain Plot

- Midband gain is approximately constant.
- Low gain at very low and very high frequencies due to coupling and parasitic capacitances.

Phase Plot

- Phase shift is around -180° in midband.
- Shows typical low-pass phase behavior at high frequencies.

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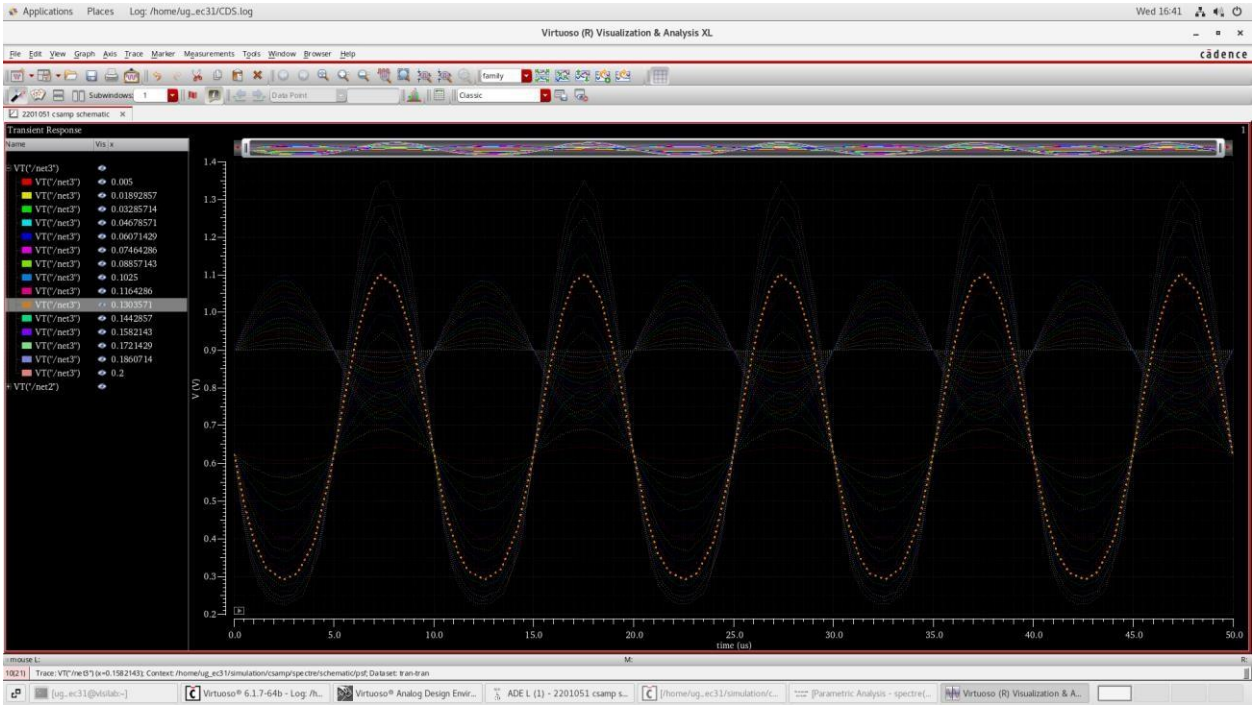
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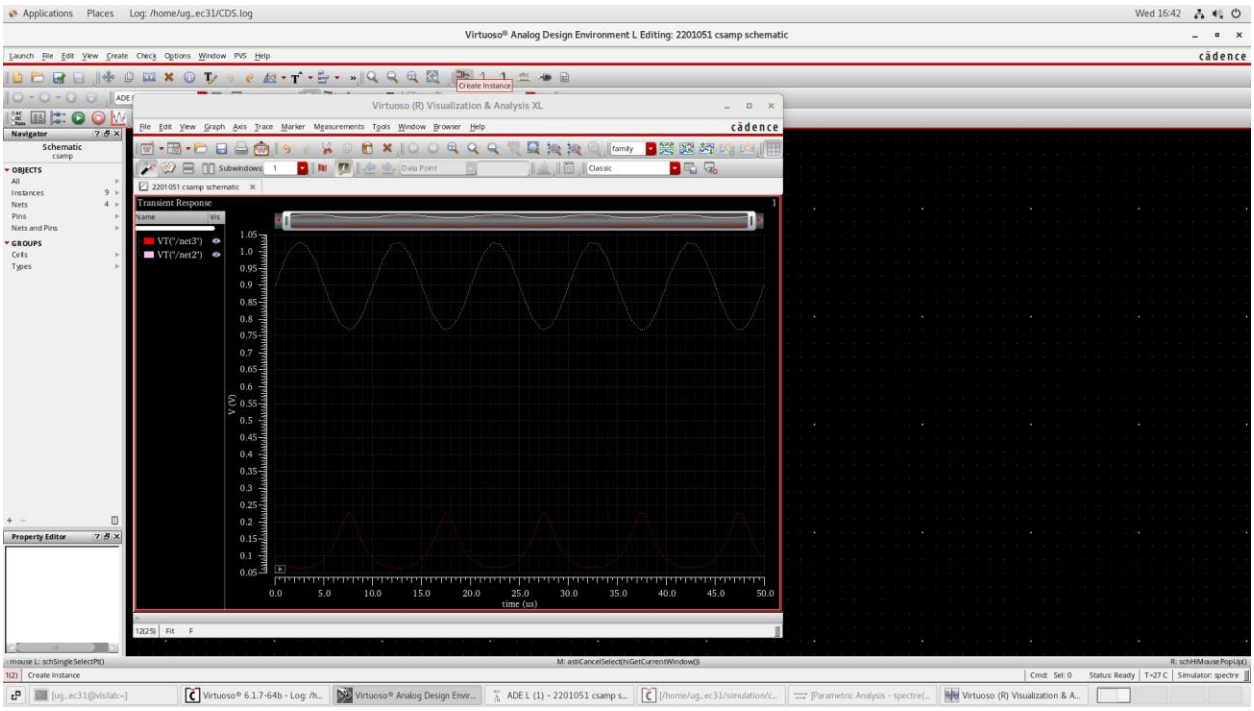


Conclusion

- The CS amplifier exhibits a significant voltage gain in midband frequency.
- Phase shift confirms the inverting nature (~180°).
- Frequency response matches expected behavior of a single-stage CS amplifier.

Observations

- **3-dB bandwidth** indicates the frequency range over which gain is nearly constant.
- **Miller effect** limits high-frequency performance.
- Gain depends on transistor parameters and load resistance.

Experiment 4: **DC Input-Output Characteristics of CMOS Inverter**

Objective

To obtain and analyze the **DC transfer characteristics** of a **CMOS inverter** using Cadence Virtuoso.

Tools Used

- Cadence Virtuoso
- Spectre Simulator
- GPDK 180nm PDK

Theory

A **CMOS inverter** is built using a PMOS and an NMOS transistor:

- **PMOS**: Source connected to **VDD**
- **NMOS**: Source connected to **GND**
- Gates tied together: **input**
- Drains tied together: **output Working Principle**
- **Vin = 0** → PMOS ON, NMOS OFF → **Vout = VDD**
- **Vin = VDD** → PMOS OFF, NMOS ON → **Vout = 0**
- **Vin = VDD/2** → both transistors partially ON → transition region

Schematic Setup

- PMOS and NMOS connected in inverter configuration
- Input connected to DC voltage source (Vin)
- Output taken at common drain node
- PMOS bulk connected to VDD, NMOS bulk to GND

Simulation Configuration

DC Sweep Analysis

- Sweep **Vin** from 0 to VDD (e.g., 0 to 1.8V)
- Measure **Vout** across the same sweep
- Plot **Vout vs Vin**

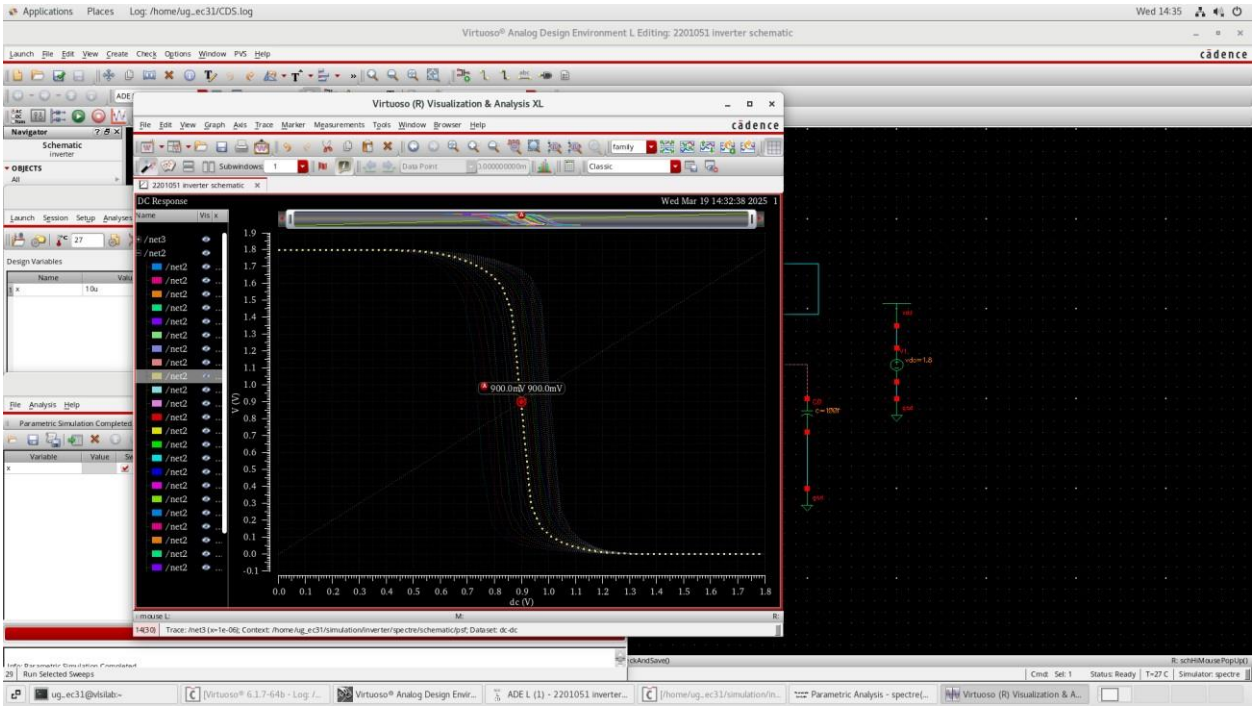
Steps in Cadence Virtuoso

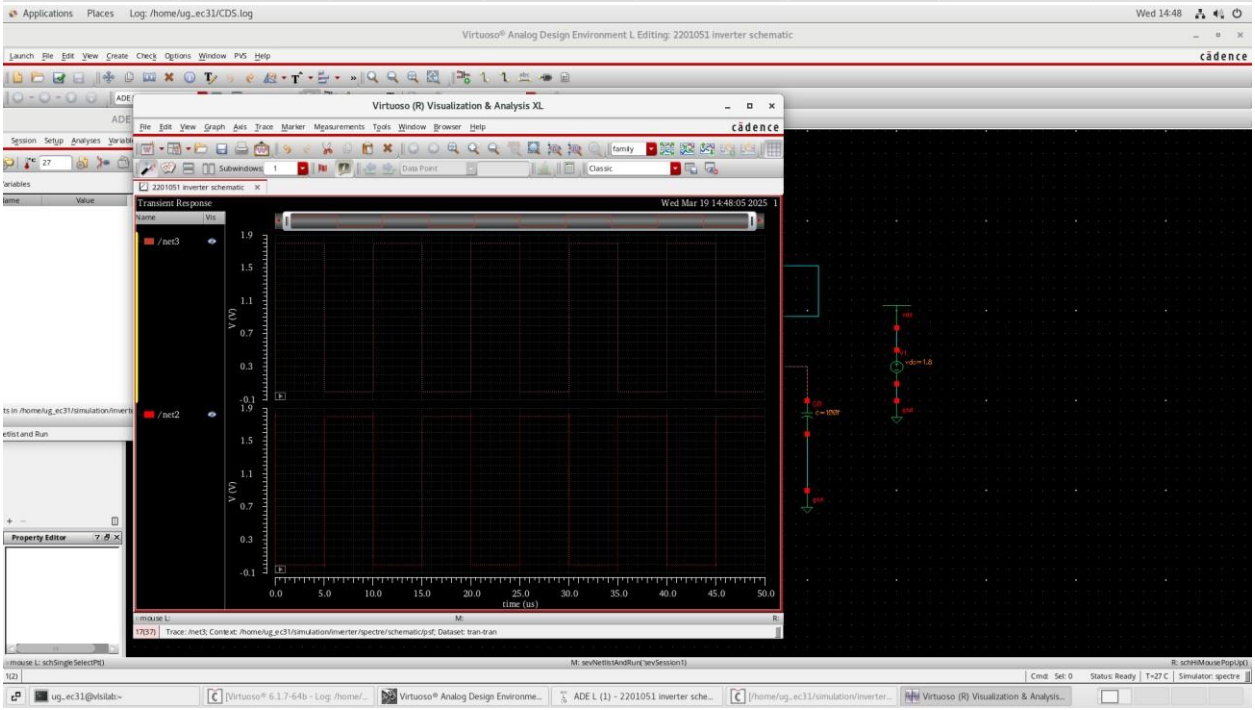
1. **Draw schematic** of CMOS inverter.
2. Connect:
    - Vin to gate of both transistors (sweep source)
    - Vout from common drain - VDD = 1.8V (or as per PDK), GND = 0V
3. Launch **ADE (Analog Design Environment)**.
4. Select **DC sweep**: - Sweep Vin from 0V to 1.8V (or your VDD)
5. Run simulation.
6. Plot **Vout vs Vin**.

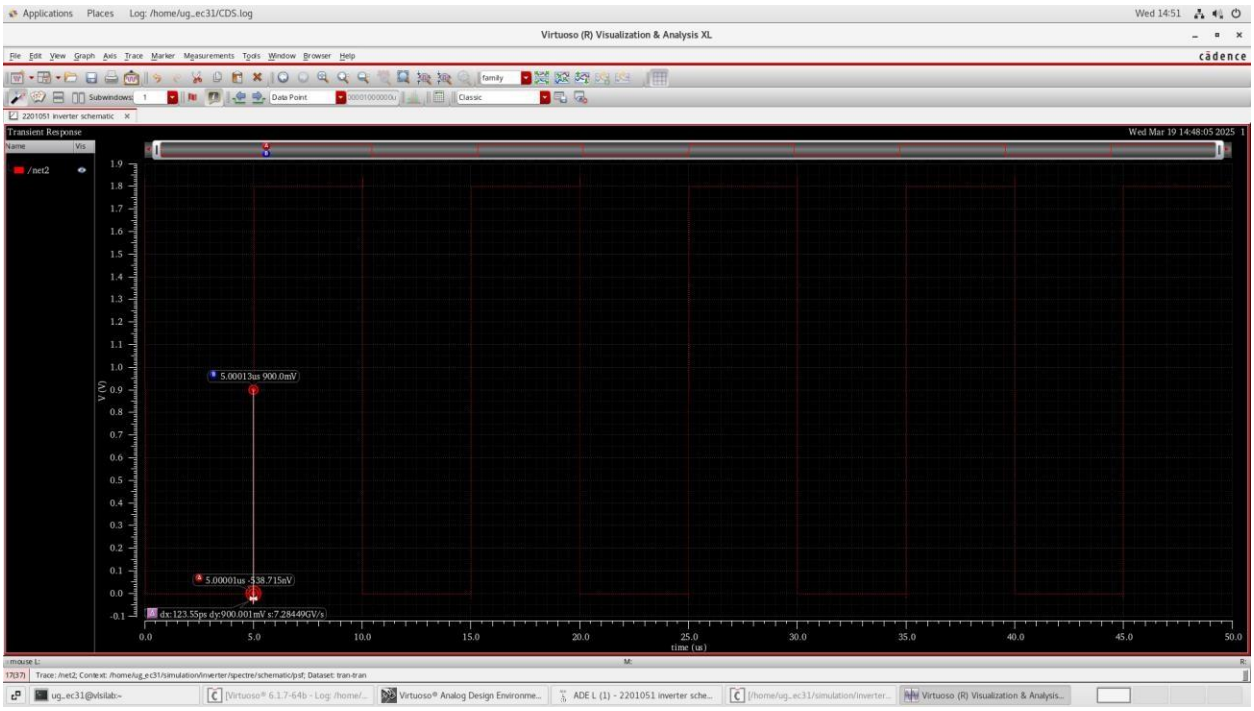
Results

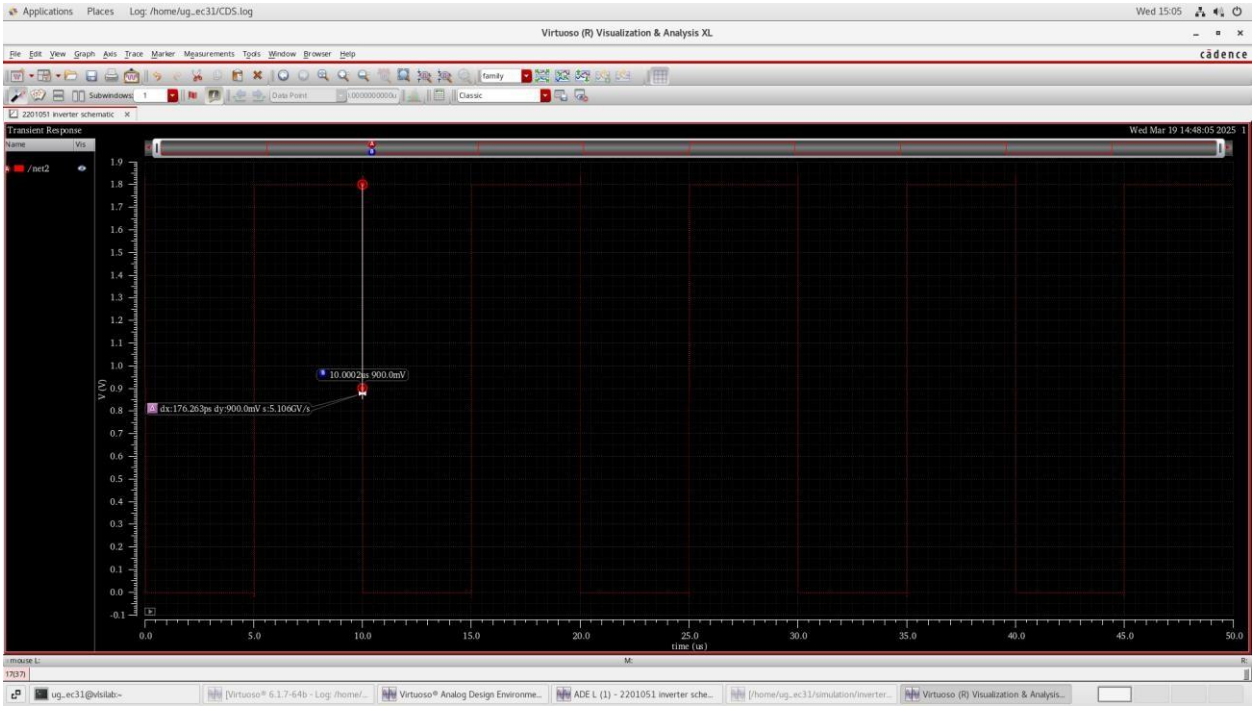
- **Vout vs Vin** plot shows sharp transition.

- Transition point ≈ VDD/2
- Confirms inverter behavior.









Conclusion

- The CMOS inverter exhibits expected switching characteristics.

- Output is high when input is low and vice versa.
- Sharp transition region observed, indicating high gain during switching.

Observations

- **Noise margins** can be estimated from the curve.
- The inverter acts as a NOT gate with rail-to-rail swing.

Experiment 5: **NAND Gate Using CMOS (NMOS and PMOS) – Truth Table Verification**

Objective

To implement a 2-input NAND gate using NMOS and PMOS transistors and verify its truth table using DC analysis in Cadence Virtuoso.

Tools Used

- **Cadence Virtuoso**
- **Spectre Simulator**
- **GPDK 180nm PDK (or your available PDK)**

Theory

A CMOS NAND gate uses:

- Two PMOS transistors in parallel at the pull-up network.

- Two NMOS transistors in series at the pull-down network.

A B Y (NAND)

0 0 1

0 1 1

1 0 1

1 1 0

Schematic Setup

- Pull-up network:
  - Two PMOS transistors in parallel ○ Sources connected to VDD ○ Drains connected to output ○ Gates: connected to A and B Pull-down network:
  - Two NMOS transistors in series ○ Drain of first to output ○ Source of second to GND ○ Gates: connected to A and B
- Inputs: A and B (DC voltage sources)
- Output: Common connection between pull-up and pull-down

Simulation Configuration

DC Sweep (Truth Table Verification)

- Apply all four input combinations: ○ A = 0/1V, B = 0/1V (or 0/1.8V if using 1.8V VDD)
- Observe Vout for each case
- Compare with expected NAND truth table

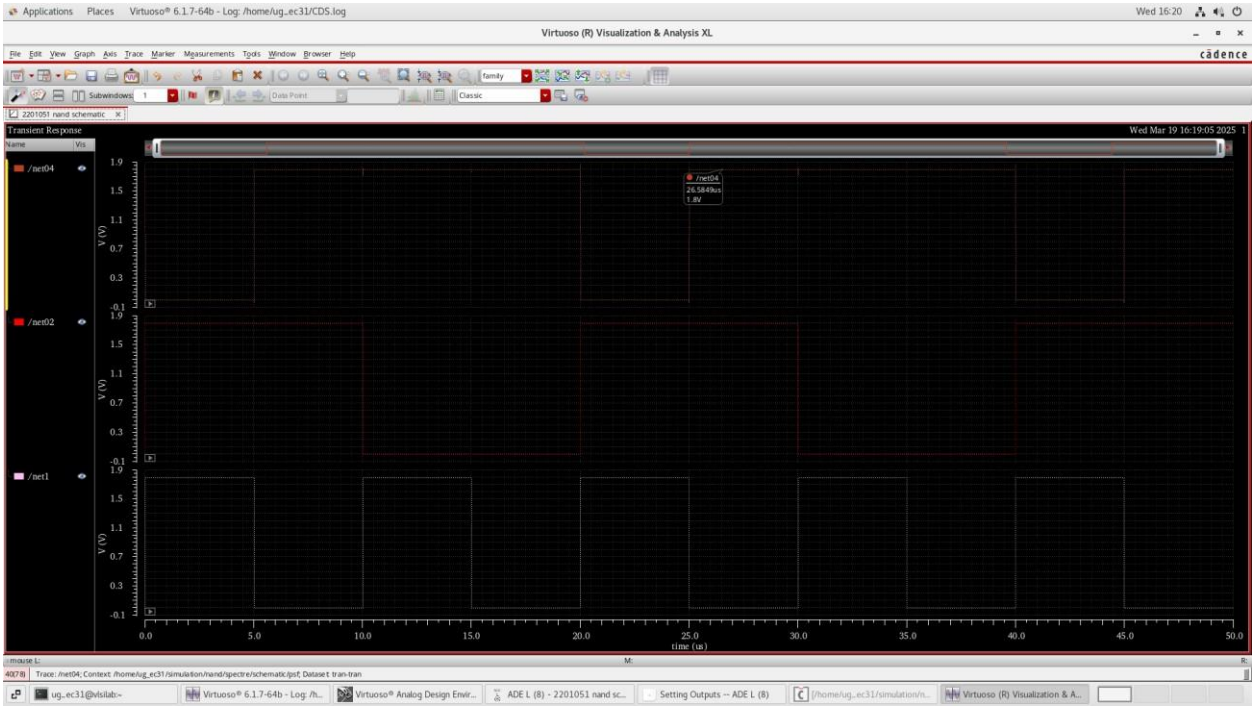
Steps in Cadence Virtuoso

1. Design CMOS NAND gate schematic using PMOS and NMOS from analogLib
2. Add two DC sources: A and B
3. Connect output node to a wire label out
4. In ADE:
    - Use DC sweep with nested sweeps:
        - Sweep A: 0V to VDD
        - Sweep B: 0V to VDD
    - Or manually set A and B to all 4 combinations using Design Variables & parametric sweep
5. Run simulation
6. Plot Vout vs input combinations or check from results table

Results

A	B	Vout (Simulated)	Logic Level
0	0	~VDD (1.8V)	1
0	1	~VDD (1.8V)	1
1	0	~VDD (1.8V)	1

1 1 ~0V 0



Conclusion

- The CMOS NAND gate behaves as expected.
- The output goes LOW only when both inputs are HIGH.
- Truth table is verified successfully using DC simulation.

Observations

- PMOS transistors are ON when input is LOW
- NMOS transistors are ON when input is HIGH
- CMOS logic ensures low static power consumption and sharp transitions

:

Experiment 6: **NOR Gate Using CMOS (NMOS and PMOS) – Truth Table Verification**

Objective

To design and simulate a **2-input NOR gate** using **CMOS technology** (NMOS and PMOS transistors) and verify its **truth table** in **Cadence Virtuoso** using DC analysis.

Tools Used

- Cadence Virtuoso
- Spectre Simulator
- GPDK 180nm PDK

Theory

A **CMOS NOR gate** is built using:

- **PMOS transistors in series** for the **pull-up network**
- **NMOS transistors in parallel** for the **pull-down network**

A B Y (NOR)

0 0 1

0 1 0

1 0 0

1 1 0

Schematic Setup

- **Pull-up network (PMOS in series)**:
    - Sources: connected to VDD ○ Drains: connected together to output ○ Gates: A and B
    - Middle connection between PMOS transistors □ **Pull-down network (NMOS in parallel)**:
    - Drains: connected together to output ○ Sources: to GND ○ Gates: A and B
- **Inputs**: A and B (DC voltage sources)
- **Output**: Taken from node where pull-up and pull-down networks meet

Simulation Configuration

DC Sweep (Truth Table Verification)

- Apply all combinations of A and B: ○ A = 0V or VDD, B = 0V or VDD (e.g., VDD = 1.8V)
- Observe **Vout** for each case
- Compare results with expected **NOR truth table**

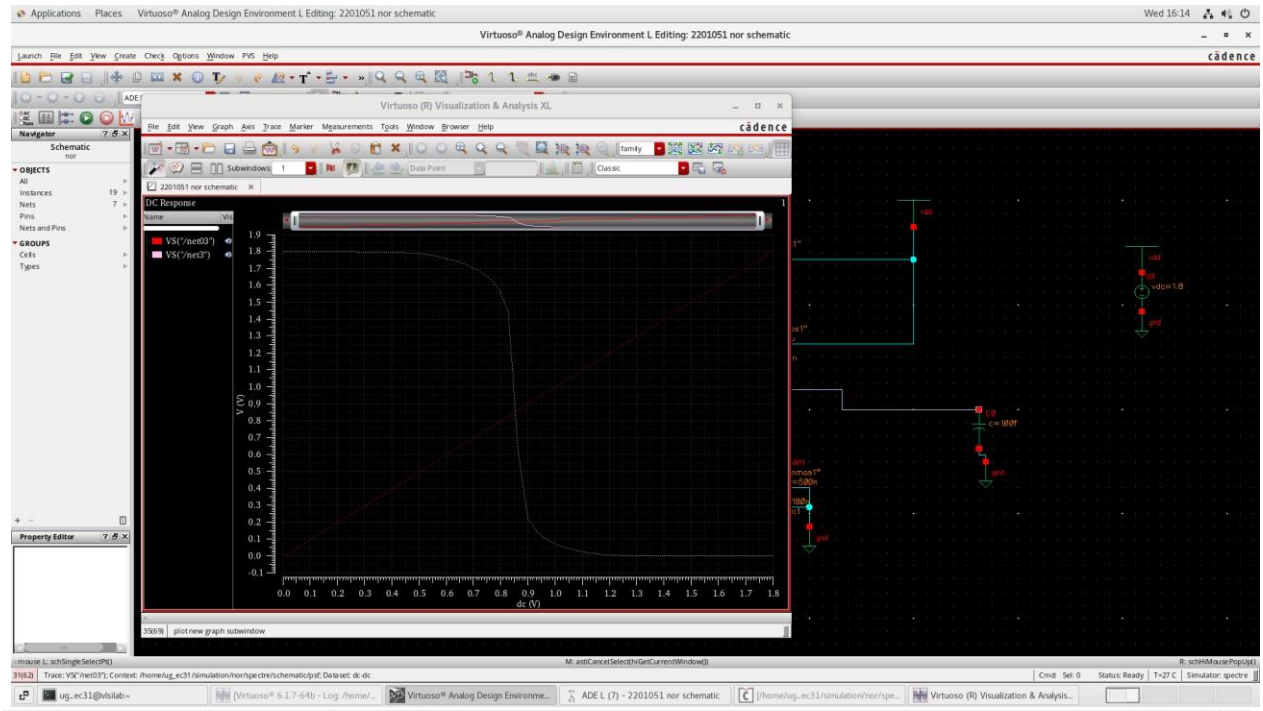
Steps in Cadence Virtuoso

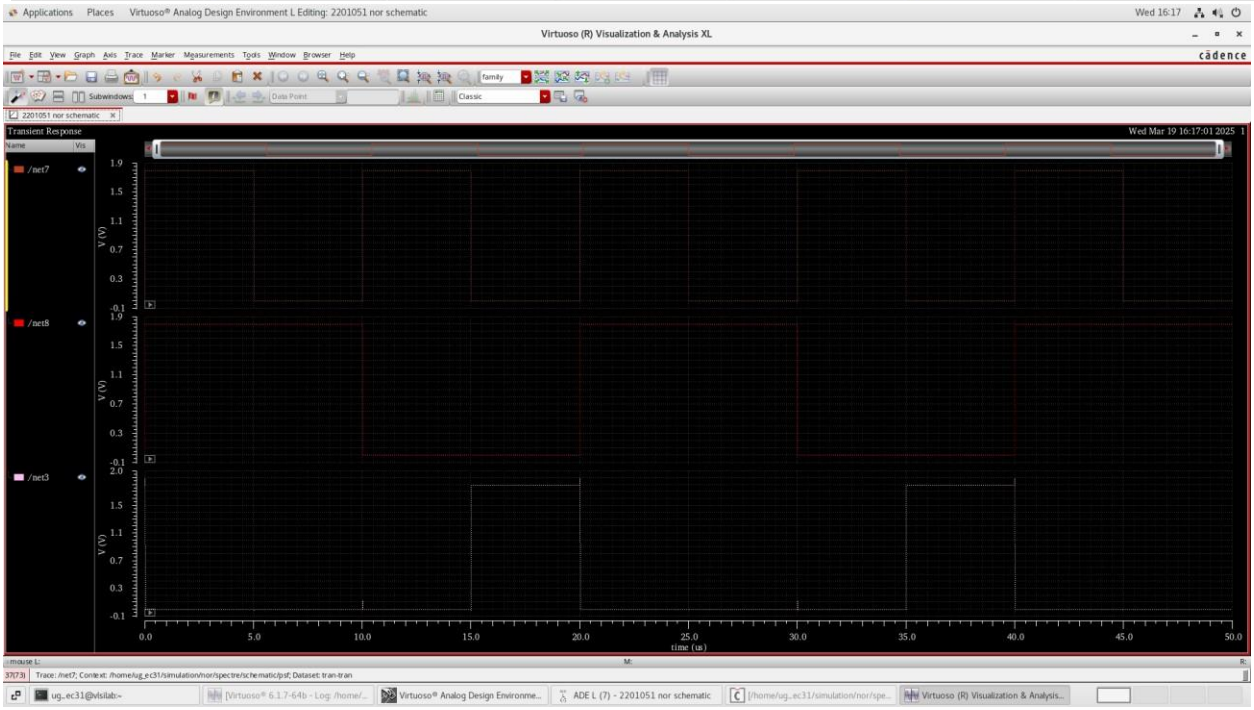
1. **Build CMOS NOR gate** using PMOS (series) and NMOS (parallel)

2. Use **DC voltage sources** for A and B inputs
3. Output node labeled as out
4. In **ADE**:
    - Set **Design Variables** for A and B
    - Run **DC parametric sweep** over combinations:
        - A: 0, 1.8V
        - B: 0, 1.8V
5. Simulate and observe **Vout** for each combination

Results

A	B	Vout (Simulated)	Logic Level
0	0	~VDD (1.8V)	1
0	1	~0V	0
1	0	~0V	0
1	1	~0V	0





Conclusion

- The CMOS NOR gate functions correctly.
- Output is **HIGH** only when **both inputs are LOW**
- Truth table matches theoretical NOR logic behavior

Observations

- **PMOS** turns ON when input is LOW
- **NMOS** turns ON when input is HIGH
- **Series PMOS** ensures output is HIGH only when both inputs are LOW

CMOS design gives **low power** and **full-swing output**

Experiment 7: **D Flip-Flop Functional Verification with 20% and 25% Clock Duty Cycles**

Objective

To design a **D Flip-Flop (DFF)** using CMOS logic and verify its correct behavior with **non-standard clock duty cycles** of **20%** and **25%** using transient simulation in **Cadence Virtuoso**.

Tools Used

- Cadence Virtuoso
- Spectre Simulator
- GPDK 180nm PDK (or your PDK)

Theory

A **D Flip-Flop** (positive-edge triggered) transfers input D to output Q on the **rising edge** of the clock (CLK).

Truth Table

CLK (↑) D Q (next)

Rising 0 0

Rising 1 1

Else x Hold

Duty Cycle

- 20% duty cycle → clock HIGH for 20% of one period
- 25% duty cycle → clock HIGH for 25% of one period

Schematic Setup

- Use : ○ Custom-built CMOS DFF (master-slave latch) □ Inputs:
  - D: pulse or square wave ○ CLK:

    pulse source with:
    - 20% duty cycle
    - 25% duty cycle
- Output: Q

Simulation Configuration

Transient Analysis

- Time: 0 to e.g. 500ns □ Input D: toggling every 50ns
- CLK:
  - **20% duty** ○ **25% duty** □ Observe:
  - Output Q changes only on rising

    edges ○ Q holds value otherwise

Steps in Cadence Virtuoso 1. Create

D Flip-Flop schematic.

2. Add:
    - **Pulse source** for CLK (adjust duty)
    - **Pulse or square source** for D
3. Set up **transient simulation**:
    - Run time: ~500ns
4. Plot D, CLK, and Q.

Repeat simulation with:

- Clock duty cycle = **20%**
- Clock duty cycle = **25%**

Results

Case 1: 20% Duty Cycle

- CLK HIGH for 20ns every 100ns
- Q changes at rising edge
- Q holds otherwise

Case 2: 25% Duty Cycle

- CLK HIGH for 25ns every 100ns
- Q again changes at rising edge only

Conclusion

- The D Flip-Flop **correctly samples D at CLK rising edges**, even under **low duty cycles (20% and 25%)**
- Output Q remains **stable** between edges, confirming **edge-triggered** behavior

Observations

- Duty cycle affects **timing margin** and setup/hold time constraints
- Even with low duty cycle, as long as **rise edge is defined**, DFF functions properly

Experiment 8: Current Mirror Design and Verification in Cadence Virtuoso

Objective

To design and simulate a **basic current mirror** using **NMOS transistors** in **Cadence Virtuoso**, and verify that the output current mirrors the reference current.

Tools Used

- Cadence Virtuoso
- Spectre Simulator
- GPDK 180nm PDK

Theory

A **current mirror** copies a reference current (I_REF) to an output branch using matched transistors. It's widely used in analog ICs for biasing and current control.

Basic NMOS Current Mirror

- **M1**: Diode-connected NMOS (gate and drain shorted)

- **M2**: Output transistor, gate tied to M1's gate
- Both sources connected to **GND**
- Same **W/L ratios** ensure mirrored current:

IOUT=IREFI_{OUT} = I_{REF}

Schematic Setup

- **M1**: Gate and drain connected, reference current sourced via I_REF
- **M2**: Gate connected to M1's gate, drain is output
- Connect both sources to GND
- **Power supply**: VDD = 1.8V
- Use **ideal current source** or **resistor from VDD to drain of M1** to set I_REF

Simulation Configuration DC

Analysis

- Sweep **Vout (M2's drain)** from 0 to VDD
- Observe **Iout** as Vout changes
- Expect constant current when **M2 is in saturation**

Steps in Cadence Virtuoso

1. Draw **basic NMOS current mirror** schematic.
2. Set **M1 and M2** to same W/L (e.g., W = 2µ, L = 180nm)
3. Apply **I_REF** via current source or resistor
4. Sweep **Vout** via DC voltage source
5. In **ADE**, choose **DC sweep**:

    - Sweep Vout from 0 to 1.8V
6. Plot **Iout vs Vout**

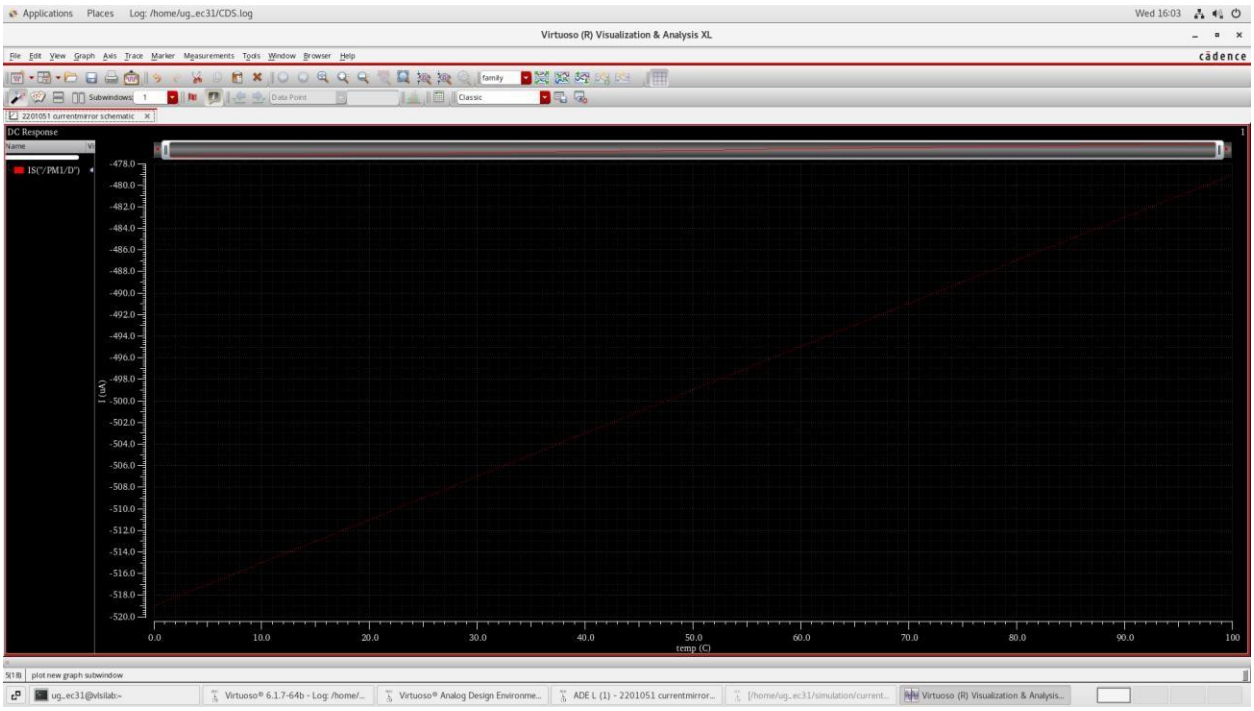
Results

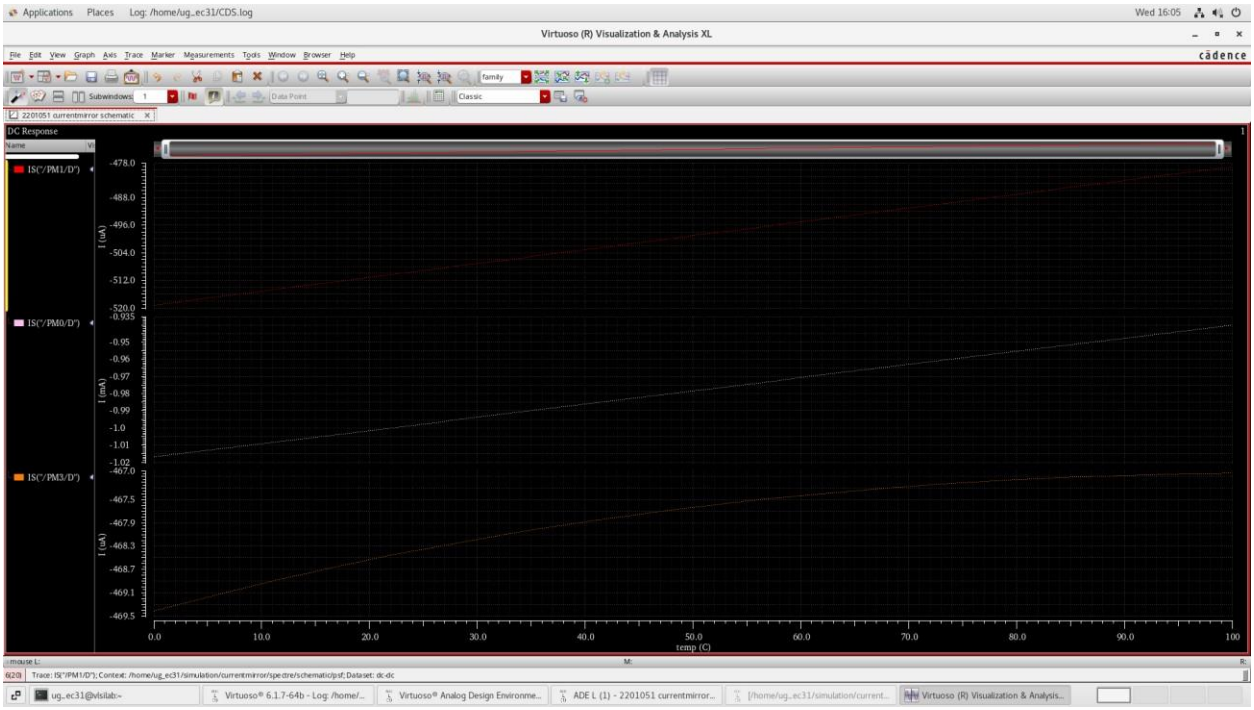
Expected Behavior

- For Vout > Vdsat, **M2** stays in saturation
- **Iout** ≈ **Iref** (flat region in plot)

Plot

- X-axis: Vout (M2's drain)
- Y-axis: Iout (drain current of M2)
- Flat region confirms **current mirroring**


Applications Places Log: /home/ug_ec31/CDS.log
Wed 16:03
Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
2201051 currentmirror schematic
DC Response
IS("/PM1/D")
I (uA)
temp (C)
plot new graph subwindow
Virtuoso® 6.1.7-64b - Log: /home/...
Virtuoso® Analog Design Environme...
ADE L (1) - 2201051 currentmirror...
Virtuoso (R) Visualization & Analysis...


Applications Places Log: /home/ug_ec31/CDS.log
Wed 16:05
Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
2201051 currentmirror schematic
DC Response
IS("/PM1/D")
IS("/PM0/D")
IS("/PM3/D")
I (uA)
I (mA)
temp (C)
Trace: IS("/PM1/D"); Context: /home/ug_ec31/simulation/currentmirror/spectre/schematic/psf; Dataset: dc-dc
Virtuoso® 6.1.7-64b - Log: /home/...
Virtuoso® Analog Design Environme...
ADE L (1) - 2201051 currentmirror...
Virtuoso (R) Visualization & Analysis...

Conclusion

- The current mirror successfully replicates I_REF at the output
- Iout remains **constant over a range of Vout**, indicating M2 stays in **saturation**
- Confirms proper current mirror operation

Observations

- Matching W/L is crucial for accurate mirroring Vout must be high enough to keep M2 in saturation Can scale current by adjusting W/L of M2: