library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

Entity ALU is

Port ( a,b: in STD\_LOGIC\_VECTOR ( 3 downto 0);

Opcode : in STD\_LOGIC\_VECTOR ( 2 downto 0);

Y : out STD\_LOGIC\_VECTOR ( 4 downto 0));

End ALU;

architecture Behavioral of ALU is

SIGNAL as,bs,ys : STD\_LOGIC\_VECTOR(4 downto 0);

Begin

as<='0'&a;

bs<='0'&b;

process(as,bs,opcode,ys)

begin

case opcode is

when "000"=> ys<=as+bs; y(4)<=ys(4);

when "001"=> ys<=as+bs; y(4)<=ys(4);

when "010"=> ys<=as and bs;

when "011"=> ys<=as nand bs;

when "100"=> ys<=as xor bs;

when "101"=> ys<=as xnor bs;

when "110"=> ys<=as or bs;

when others=>ys<= '0' & as (3 downto 0);

end case;

end process;

y(3 downto 0)<=ys(3 downto 0);

end Behavioral;