library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity keypad1 is

port(clk:in std\_logic;

rl:in std\_logic\_vector(3 downto 0);

sl:out std\_logic\_vector(3 downto 0);

segen\_o:out std\_logic\_vector(6 downto 0);

display\_en:out std\_logic\_vector(5 downto 0));

end keypad1;

architecture Behavioral of keypad1 is

signal sl\_s:std\_logic\_vector(3 downto 0):="1110";

signal segen:std\_logic\_vector(6 downto 0):="1111111";

begin

process(clk, sl\_s)

begin

if rising\_edge(clk) then

sl\_s(3)<=sl\_s(2);

sl\_s(2)<=sl\_s(1);

sl\_s(1)<=sl\_s(0);

sl\_s(0)<=sl\_s(3);

end if;

end process;

process(clk, rl, sl\_s)

begin

if rising\_edge(clk) then

case rl is

when "0111"=> if sl\_s="0111" then segen<="0000001";

elsif sl\_s="1011" then segen<="1001111";

elsif sl\_s="1101" then segen<="0010010";

elsif sl\_s="1110" then segen<="0000110";

end if;

when "1011"=> if sl\_s="0111" then segen<="1001100";

elsif sl\_s="1011" then segen<="0100100";

elsif sl\_s="1101" then segen<="0100000";

elsif sl\_s="1110" then segen<="0001111";

end if;

when "1101"=> if sl\_s="0111" then segen<="0000000";

elsif sl\_s="1011" then segen<="0001100";

elsif sl\_s="1101" then segen<="0001000";

elsif sl\_s="1110" then segen<="1100000";

end if;

when "1110"=> if sl\_s="0111" then segen<="0110001";

elsif sl\_s="1011" then segen<="1000010";

elsif sl\_s="1101" then segen<="0110000";

elsif sl\_s="1110" then segen<="0111000";

end if;

when others=> segen<=segen;

end case;

end if;

end process;

sl<=sl\_s;

display\_en<="111101";

segen\_o<=segen;

end behavioral;