Devleena Ghosh, PhD
Computer Science and Engineering
email: devleena.ghosh07@gmail.com, Ph : +91-9474445722

Education

- **Ph.D.** (2016 – 2023) in Computer Science and Engineering, IIT Kharagpur
  - Area of work: Computational biology, Formal modelling and verification, Parameter estimation
  - Thesis title: Computational Methods for Modelling and Analysis of Thyrotropic Regulation Pathway
  - Supervisor: Prof. Chittaranjan Mandal
- **M.Tech** in Computer Science and Engineering, IIT Kharagpur **2011 - 2013** (Summa Cum Laude), CGPA: **9.78**
  - M.Tech Thesis title: Formal Modeling and Verification of Interlocking for Railway Signaling Systems
  - Supervisor: Prof. Chittaranjan Mandal
- **B.E. (Computer Science and Technology)** from IIEST, Shibpur (formerly BESU, Shibpur), West Bengal, India, **2006 - 2010**, with **83.46%**
- **Higher Secondary (10+2)** with **89.9% marks** from W.B.C.H.S.E, India, **2006**
- **Secondary (10)** with **89.12% marks** from W.B.B.S.E, India, **2004**

Research Experience

1. **Computational Methods for Modelling and Analysis of Thyrotropic Regulation Pathway**

   This work is on developing a simple ODE model to capture the behaviour of the Hypothalamus-pituitary-thyroid (HPT) axis and determining subject specific model parameters based on subject specific observed data. The parameter estimation method uses Genetic algorithms on observation clusters when availability of time-series data is scarce. The individualised modelling helps in personalised dosage estimation for hypothyroid subjects. The dosage estimation was carried out using satisfiability-modulo-theory (SMT) based analysis based on hypothyroid observed data. A novel SMT based methodology in combination with Gaussian Process regression and gradient methods to detect parameter identifiable combinations of a structurally unidentifiable model represented as ODE systems or hybrid systems has also been developed.

2. **Developing a tool for application of formal methods in Railway Interlocking**.

   – An auto generated and optimised formal model of the railway interlocking system was validated against some safety properties. The model was generated from the validated input of yard layout and control table. GROOVE graph grammar tool is used for layout validation, NuSMV used for model checking, and Flex, Bison are used to create parser.

3. **Developing Virtual Lab along with a simulation tool for conduction of experiments in Logic Design and Computer Organization**, in Dept. of Computer Science & Engineering, IIT Kharagpur sponsored by MHRD, India. The developed simulation tool is in use to conduct laboratory courses of under and post-graduate level students at IIT Kharagpur.

   – Deployed at http://sit.iitkgp.ernet.in/~coavl/index.html

4. **Iris Recognition** as B.E. final year project.

5. **Automatic Analysis of PET tumor images for Radiotherapy treatment Planning** as part of internship program in Queen's University, Belfast (2008).

Work Experience

- **Visiting Scientist** (Feb 2023 –) at Electronics and Communication Sciences Unit, Indian Statistical Institute, Kolkata
- **Assistant Professor** (Aug 2022 - Feb 2023) at Department of Computer Science & Engineering, Techno Main Salt Lake, Kolkata (under Maulana Abul Kalam Azad University of Technology, West Bengal)
- **Software Engineer** (Aug 2013 - Dec 2015) at **Microsoft India (R&D) Pvt. Ltd.**, Hyderabad, in Visual Studio Online Services (Cloud Load Testing team) (using C#, TypeScript, SQL, Java). Have significant contribution towards making the service scalable to support higher configuration and collaboration with another open source load testing tool.
- **Junior Research Fellow** (Sept 2010 - Jun 2011) in the research project *Virtual Lab for Computer Organization and Architecture*, sponsored by MHRD, Computer Science & Engineering Department, IIT Kharagpur.

Publications

- **Journals:**

  1. Clustering Based Parameter Estimation of Thyroid Hormone Pathway, IEEE/ACM Transactions on Computational Biology and Bioinformatics, pp 343–354, vol. 19, no. 1, Feb 2022; **Devleena Ghosh**, Chittaranjan Mandal
  2. Automatic Generation of Route Control Chart from Validated Signal Interlocking Plan, IEEE Transactions on Intelligent Transportation Systems, pp 6516–6525, vol. 22, no. 10, Oct 2021; Arindam Das, Manoj Gangwar, **Devleena Ghosh**, Chittaranjan Mandal, Anirban Sengupta, M M Waris
  3. COLDVL: A Virtual Laboratory Tool with Novel Features to Support Learning in Logic Design and Computer Organisation, Journal of Computers in Education, pp 461–490, vol. 4, no. 4, Dec 2017; Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal

- **Conferences:**

1. Layout Validation using Graph Grammar and Generation of Yard Specific Safety Properties for Railway Interlocking Verification, 22^{nd} Asia Pacific Software Engineering Conference (APSEC) 2015, pp 330-337, New Delhi, Dec 1-4, 2015, **Devleena Ghosh**, Chittaranjan Mandal
2. A Virtual Laboratory Package to Support Teaching of Logic Design and Computer Organization, 7^{th} International Conference on Technology for Education (T4E) 2015, Warangal, Dec 10-12, 2015, Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal
3. Aiding Teaching of Logic Design and Computer Organization Through Dynamic Problem Generation and Automatic Checker Using COLDVL Tool, 7^{th} International Conference on Technology for Education (T4E) 2015, Warangal, Dec 10-12, 2015, Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal, Indraneel Mitra
4. A Virtual Laboratory for Computer Organisation and Logic Design (COLDVL) and Its Utilisation for MOOCs, 3^{rd} International Conference on MOOC, Innovation and Technology in Education (MITE) 2015, Amritsar, Oct 1-2, 2015, Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal

Awards and Recognitions

- **Institute Silver medal** for being the best student in order of merit for MTech in Department of CSE, IIT Kharagpur.
- MHRD scholarship during PhD at IIT Kharagpur.
- *AIR 126* in GATE 2011 examination.
- *AIR 426* in WBJEE 2006 examination.

Others

- Teaching Assistantship at IIT Kharagpur: Programming & Data Structure, Algorithms, Advanced Algorithms, Switching Circuit and Logic Design, Foundations of Computer Science, Formal Systems.
- Reviewer for: ISEC, PLoS One

Personal Profile

Date of Birth:	7^{th} April,1989
Nationality:	Indian
Permanent Address:	Swan's Compound (Hatar Math), Post - Midnapore, Dist. - Paschim Medinipur, Pin - 721101, West Bengal, India

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I hereby declare that the above particulars are true and correct to the best of my knowledge.

Date: 20^{th} March, 2023 Devleena Ghosh