Devleena Ghosh, PhD

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Education

- **Ph.D** (2016 – 2023) in Computer Science and Engineering, IIT Kharagpur
  - Area of work: Computational biology, Formal modelling and verification, Parameter estimation, Machine learning appilcans
  - Thesis: Computational Methods for Modelling and Analysis of Thyrotropic Regulation Pathway
  - Supervisor: Prof. Chittaranjan Mandal

- **M.Tech** in Computer Science and Engineering, IIT Kharagpur **2011 - 2013** (Silver medal), CGPA: **9.78**
  - Thesis: Formal Modeling and Verification of Interlocking for Railway Signaling Systems
  - Supervisor: Prof. Chittaranjan Mandal

- **B.E. (Computer Science and Technology)** from IIEST, Shibpur (formerly BESU, Shibpur), West Bengal, India, **2006 - 2010**, with **84.5%**

- **Higher Secondary (10+2)** with **89.9% marks** from W.B.C.H.S.E, India, **2006**

- **Secondary (10)** with **89.12% marks** from W.B.B.S.E, India, **2004**

Research

1. **Enhancing Formal Verification with Machine Learning approaches**

   Objective of this work is to find an optimal combination of Bounded Model Checking (BMC) engines for faster property verification in a given hardware design.

2. **Computational Methods for Modelling and Analysis of Thyrotropic Regulation Pathway**

   Mathematical modelling of thyrotropic regulatory pathway provides important understanding on the working of hypothalamus-pituitary-thyroid axis. As part of my PhD work, the objective was to design ordinary differential equation (ODE) models for capturing thyroid physiology for normal and diseased system behaviours and develop methods for parameter estimation and other analysis when *the observational data is noisy and sparse*. The techniques for parameter identifiability analysis are also explored and the detection of identifiable parameter combinations for structurally unidentifiable models has been performed. A combination of formal methods along with machine learning based methods is applied for the analysis of biological models.

3. **Developing a tool for application of formal methods in Railway Interlocking**.

   An auto generated and optimised formal model of the railway interlocking system was validated against some safety properties. The model was generated from the validated input of yard layout and control table. GROOVE graph grammar tool is used for layout validation, NuSMV is used for model checking, and the parser is built using flex, Bison.

4. **Developing Virtual Lab along with a simulation tool for conduction of experiments in Logic Design and Computer Organization**, in Dept. of Computer Science and Engineering, IIT Kharagpur sponsored by MHRD, India. The developed simulation tool is in use to conduct laboratory courses of under and post-graduate level students at IIT Kharagpur.

   Deployed at https://cse.iitkgp.ac.in/~chitta/coldvl/

5. **Iris Recognition** as B.E. final year project.

6. **Automatic Analysis of PET tumor images for Radiotherapy treatment Planning** as part of internship program at Queen's University, Belfast (2008).

Work Experience

- **Visiting Scientist** (Feb 2023 –) at Electronics and Communication Sciences Unit, Indian Statistical Institute, Kolkata

- **Assistant Professor** (Aug 2022 - Feb 2023) at Department of Computer Science and Engineering, Techno Main Salt Lake, Kolkata (affiliated under Maulana Abul Kalam Azad University of Technology, West Bengal)

- **Software Engineer** (Aug 2013 - Dec 2015) at **Microsoft India (R&D) Pvt. Ltd.**, Hyderabad, in Visual Studio Online Services (Cloud Load Testing team). Have significant contribution towards making the service scalable to support higher configuration and collaboration with another open source load testing tool.

- **Junior Research Fellow** (Sept 2010 - Jun 2011) in the research project *Virtual Lab for Computer Organization and Architecture*, sponsored by MHRD, Computer Science and Engineering Department, IIT Kharagpur.

Publications

- **Journals:**

  1. Clustering Based Parameter Estimation of Thyroid Hormone Pathway, IEEE/ACM Transactions on Computational Biology and Bioinformatics, pp 343–354, vol. 19, no. 1, Feb 2022; **Devleena Ghosh**, Chittaranjan Mandal

  2. Automatic Generation of Route Control Chart from Validated Signal Interlocking Plan, IEEE Transactions on Intelligent Transportation Systems, pp 6516–6525, vol. 22, no. 10, Oct 2021; Arindam Das, Manoj Gangwar, **Devleena Ghosh**, Chittaranjan Mandal, Anirban Sengupta, M M Waris

  3. COLDVL: A Virtual Laboratory Tool with Novel Features to Support Learning in Logic Design and Computer Organisation, Journal of Computers in Education, pp 461–490, vol. 4, no. 4, Dec 2017; Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal

- **Conferences:**

  1. Harnessing Multiple BMC Engines together for Efficient Formal Verification, 21st ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE), Hamburg, Germany, September 21-22, 2023, **Devleena Ghosh**, Sumana Ghosh, Raj Kumar Gajavelly and Ansuman Banerjee (*Accepted*)

  2. Layout Validation using Graph Grammar and Generation of Yard Specific Safety Properties for Railway Interlocking Verification, 22nd Asia Pacific Software Engineering Conference (APSEC) 2015, pp 330-337, New Delhi, Dec 1-4, 2015, **Devleena Ghosh**, Chittaranjan Mandal

  3. A Virtual Laboratory Package to Support Teaching of Logic Design and Computer Organization, 7th International Conference on Technology for Education (T4E) 2015, Warangal, Dec 10-12, 2015, Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal

  4. Aiding Teaching of Logic Design and Computer Organization Through Dynamic Problem Generation and Automatic Checker Using COLDVL Tool, 7th International Conference on Technology for Education (T4E) 2015, Warangal, Dec 10-12, 2015, Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal, Indraneel Mitra

5. A Virtual Laboratory for Computer Organisation and Logic Design (COLDVL) and Its Utilisation for MOOCs, 3rd International Conference on MOOC, Innovation and Technology in Education (MITE) 2015, Amritsar, Oct 1-2, 2015, Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal

- **Under revision**

  1. "SMT based parameter identifiable combination detection for non-linear continuous dynamics", Formal Aspects of Computing, **Devleena Ghosh**, Chittaranjan Mandal

  2. "Parameter estimation for the oral minimal model and parameter distinctions between obese and non-obese type 2 diabetes", Journal of Computational Biology, Manoja Rajalakshmi Aravindakshan, **Devleena Ghosh**, Chittaranjan Mandal, K V Venkatesh, Jit Sarkar, Partha Chakrabarti, Sujay K Maity

  3. "Leptin augmented model to include the role of obesity in insulin-glucose pathway for T2DM subjects", Bulletin of Mathematical Biology, Manoja Rajalakshmi Aravindakshan; **Devleena Ghosh**; Chittaranjan Mandal; Venkatesh K V; Jit Sarkar; Sujay Krishna Maity; Partha Chakrabarti

Awards and Recognitions

- **Institute Silver medal** for being the best student in order of merit for MTech in Department of CSE, IIT Kharagpur.
- MHRD scholarship during PhD at IIT Kharagpur.
- *AIR 126* in GATE 2011 examination.
- Selected as part of Electronic Engineers Welcome Scheme (EEWS), 2008 at Institute of Electronica, Communications and Information Technology (ECIT), Queen's University, Belfast

Others

- Subjects taught: Algorithms, Artificial Neural Networks, Operating Systems Laboratory

- Teaching Assistantship at IIT Kharagpur: Programming and Data Structure, Algorithms, Advanced Algorithms, Switching Circuit and Logic Design, Foundations of Computer Science, Formal Systems.

- Reviewer for: ISEC, PLoS One, GLSVLSI

Personal Profile

Date of Birth: 7th April,1989
Nationality: Indian
Permanent Address: Swan's Compound (Hatar Math),
Post - Midnapore, Dist. - Paschim Medinipur,
Pin - 721101, West Bengal, India