DATA BUS — 8 WIRES

ADDRESS BUS — 8 WIRES

CONTROL BUS — IO, RW, IRQ, Clock

CPU

| MBR | MAR | CBR |

| CIR |

ALU

AL	IP
BL	SP
CL	SR
DL	

MBR = Memory Buffer Register
MAR = Memory Address Register
CBR = Conteol Bus Register
CIR = Current Instruction Reg'
IP = Instruction Pointer
SP = Stack Pointer
SR = Status Register

RAM or ROM

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

I/O Ports

16 Ports numbered 0 to F

http://www.softwareforeducation.com/sms32v50_manual/020architecture.htm