

**Department of Electronics and Communication Engineering**

**Complementary Metal-Oxide Semiconductor (CMOS)**

**Project Title:** **10 T SRAM CELL Design Using CMOS Technology(32nm).**

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**What is a 10 T SRAM CELL?**

The **10T SRAM cell** (10-transistor Static Random Access Memory cell) is an advanced SRAM architecture designed to improve stability, read performance, and power efficiency compared to the conventional 6T SRAM cell. While a standard 6T cell is sufficient for many applications, the 10T SRAM cell offers specific advantages that make it suitable for low-power and high-performance memory systems, especially at lower supply voltages, which are common in modern, highly scaled CMOS technology.

**Key Components and Design of a 10T SRAM Cell**

The 10T SRAM cell builds on the standard cross-coupled inverter structure used in a 6T cell, with added transistors to improve read stability and write performance. Its main components include:

1. **Cross-Coupled Inverters**: Like in a 6T cell, the 10T SRAM cell has two CMOS inverters connected in a loop, creating a bistable circuit that stores the logic state ("1" or "0").
2. **Write Access Transistors**: Similar to the 6T SRAM, two NMOS transistors are used to connect the bitlines (BL and BLB) to the storage nodes (Q and QB). These transistors are controlled by the **Wordline (WL)**, allowing data to be written into the cell when the wordline is active.
3. **Read Isolation Transistors**: Unlike the 6T SRAM cell, which uses the same transistors for both reading and writing, the 10T cell includes two additional NMOS transistors to isolate the read operation. This isolation prevents the stored data from being disturbed during a read operation, thus enhancing the read stability of the cell.
4. **Read Assist Transistors**: These extra transistors, including one PMOS and one NMOS, further enhance read performance by selectively precharging the read path. When the read wordline is activated, these transistors ensure a strong and stable read signal is available on the read bitline.

**WINSPICE Netlist**

**6T SRAM CELL-**

\* 6T SRAM Cell NgSpice Netlist Example

\* Global Supply Voltage

VDD VDD 0 DC 1.8

VGND GND 0 0

\* Bitline and Bitline Bar (BL and BLB)

VBLL BL 0 DC 0

VBLB BLB 0 DC 0

\* Wordline Control

VWL WL 0 PULSE(0 1.8 0 1n 1n 10n 20n)

\* 6T SRAM Cell Structure

M1 Q1 BLB VDD VDD PMOS L=180n W=180n

M2 Q2 BL VDD VDD PMOS L=180n W=180n

M3 Q1 Q2 GND GND NMOS L=180n W=90n

M4 Q2 Q1 GND GND NMOS L=180n W=90n

M5 BLB WL Q1 GND NMOS L=180n W=90n

M6 BL WL Q2 GND NMOS L=180n W=90n

\* Transient Analysis

.TRAN 1n 200n

\* DC Operating Point for Leakage Current

.OP

\* Measurement Commands

\* Measure average current from VDD for dynamic power calculation

.MEASURE TRAN I\_vdd AVG I(VDD) FROM=0 TO=200n

\* Measure leakage current in standby mode (use .OP result)

.MEASURE DC I\_leak OP I(VDD)

\* Measure power using instantaneous current and voltage

.MEASURE TRAN P\_avg PARAM='V(VDD)\*I(VDD)'

\* End of Netlist

.end

**2.10 T SRAM CELL-**

\* 10T SRAM Cell NgSpice Netlist Example

\* Global Supply Voltage

VDD VDD 0 DC 1.8

VGND GND 0 0

\* Bitline and Bitline Bar (BL and BLB)

VBLL BL 0 DC 0

VBLB BLB 0 DC 0

\* Wordline and Read Line Control

VWL WL 0 PULSE(0 1.8 0 1n 1n 10n 20n)

VRL RL 0 PULSE(0 1.8 0 1n 1n 10n 20n)

\* 10T SRAM Cell Structure

\* Cross-coupled inverters

M1 Q1 Q2 VDD VDD PMOS L=180n W=180n

M2 Q2 Q1 VDD VDD PMOS L=180n W=180n

M3 Q1 Q2 GND GND NMOS L=180n W=90n

M4 Q2 Q1 GND GND NMOS L=180n W=90n

\* Write access transistors

M5 BL WL Q1 GND NMOS L=180n W=90n

M6 BLB WL Q2 GND NMOS L=180n W=90n

\* Read isolation transistors

M7 Q1 RL Q\_read GND NMOS L=180n W=90n

M8 Q2 RL Q\_read GND NMOS L=180n W=90n

\* Read assist transistors

M9 Q\_read VDD RL VDD PMOS L=180n W=180n

M10 Q\_read GND RL GND NMOS L=180n W=90n

\* Transient Analysis

.TRAN 1n 200n

\* DC Operating Point for Leakage Current

.OP

\* Measurement Commands

\* Measure average current from VDD for dynamic power calculation

.MEASURE TRAN I\_vdd AVG I(VDD) FROM=0 TO=200n

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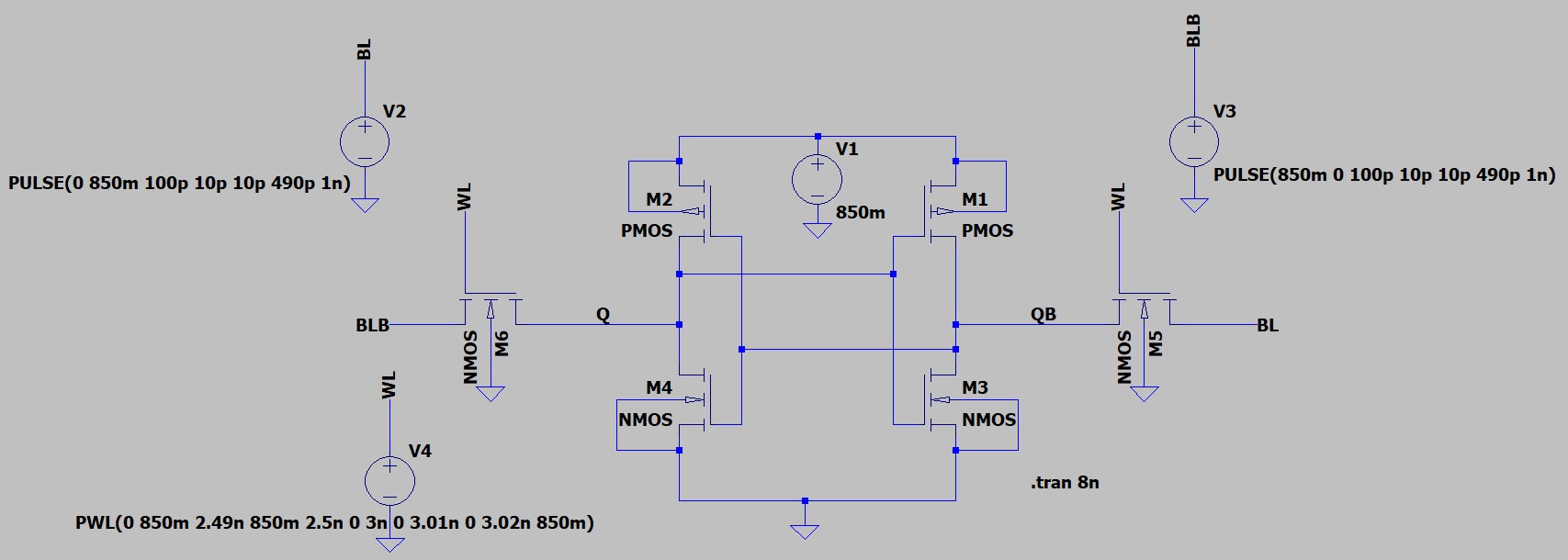
\* Measure power using instantaneous current and voltage

.MEASURE TRAN P\_avg PARAM='V(VDD)\*I(VDD)'

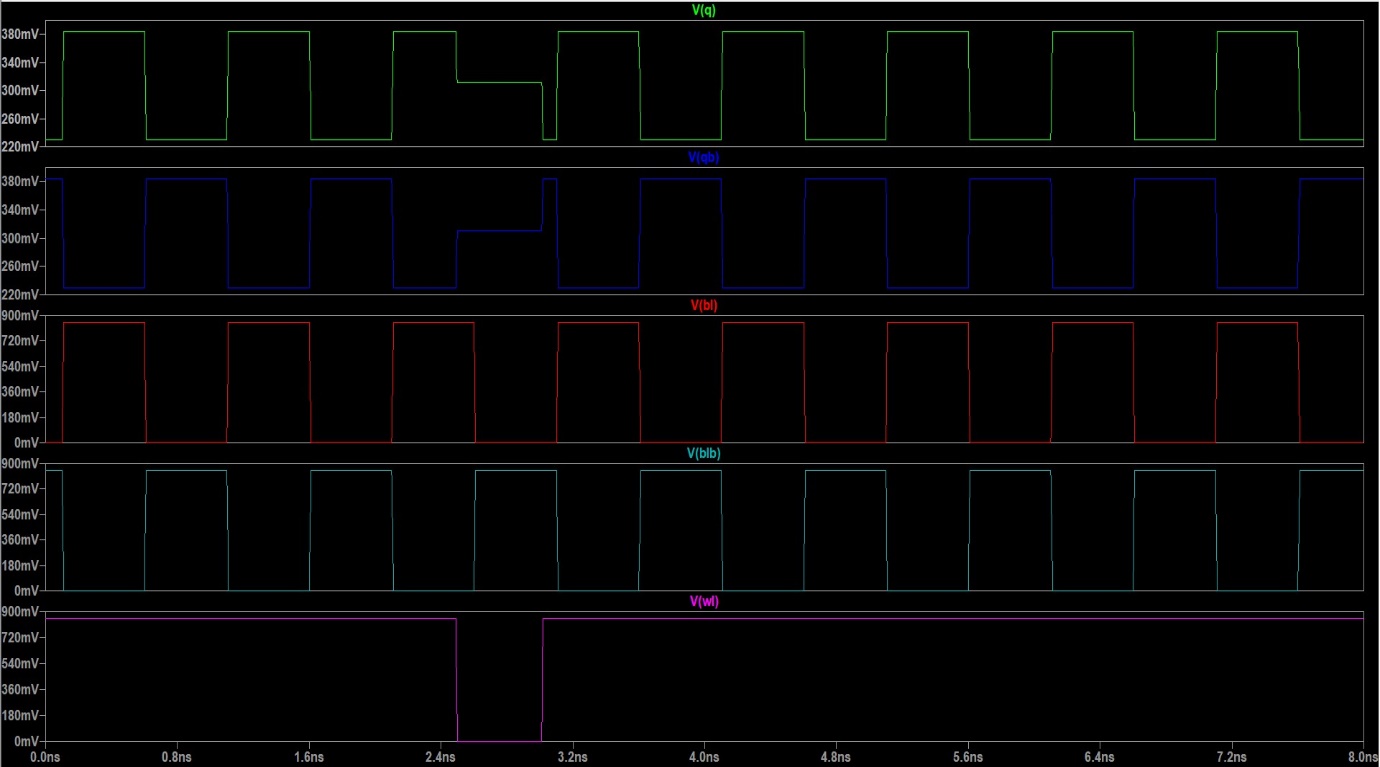
\* End of Netlist

.end

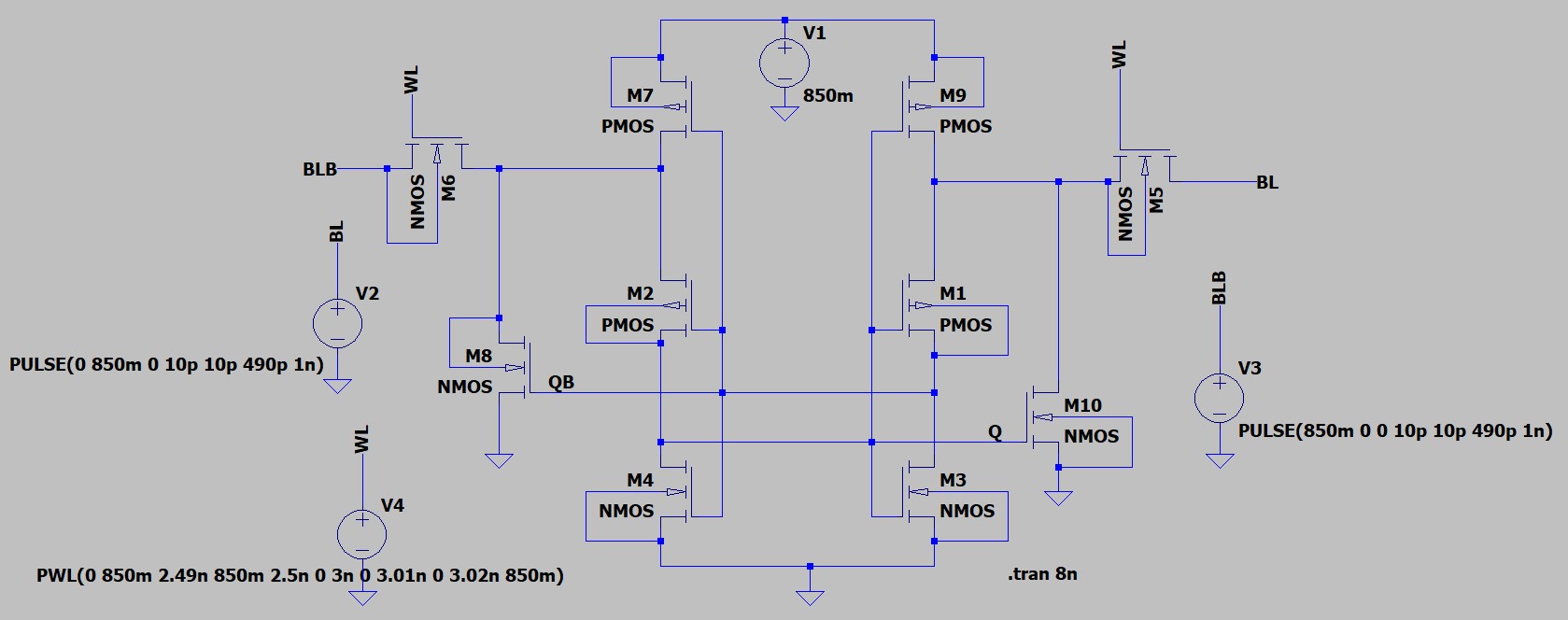
**LT SPICE Layouts and Simulation-**

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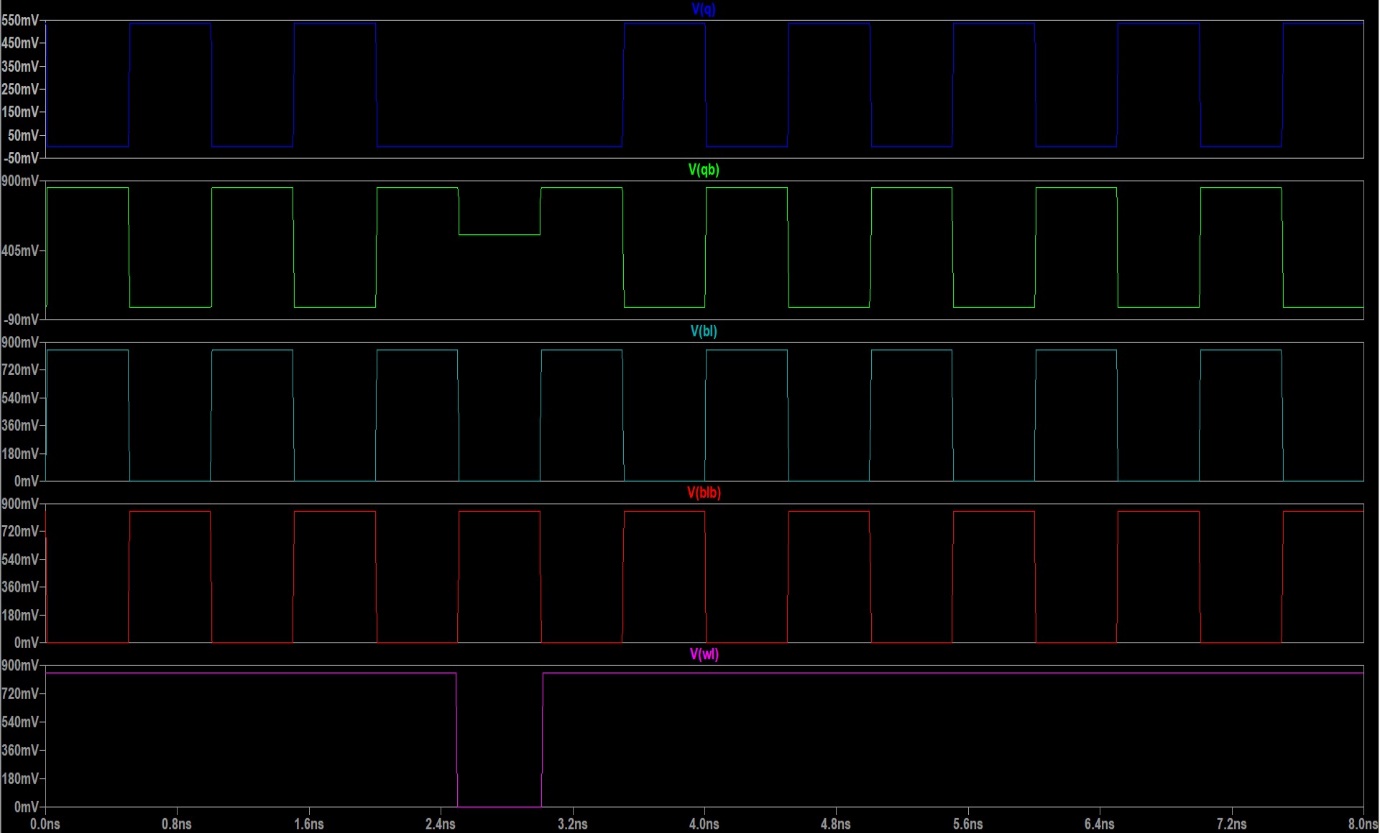
**6T SRAM CELL**

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**Simulation of 6T SRAM CELL**

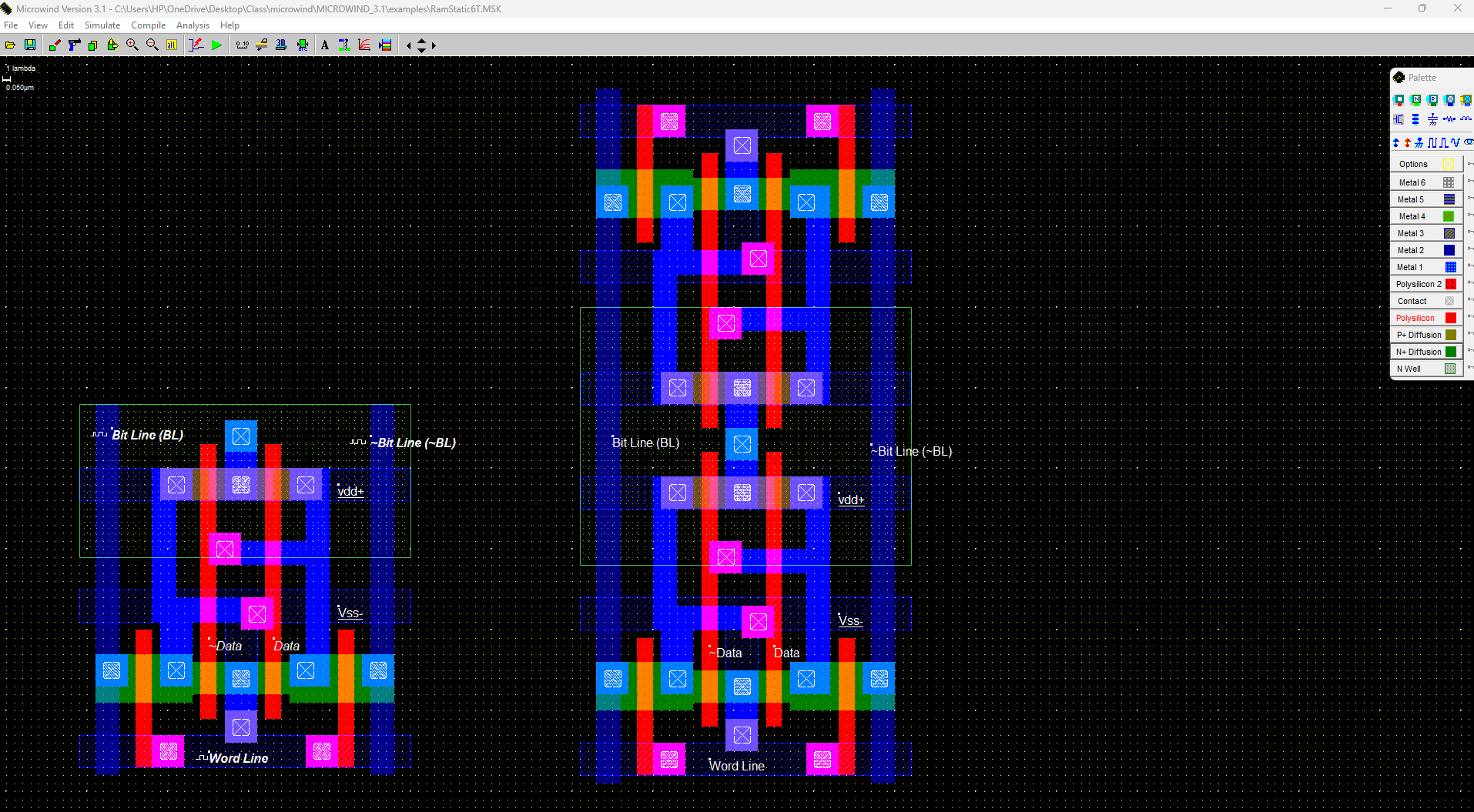
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**10 T SRAM CELL**

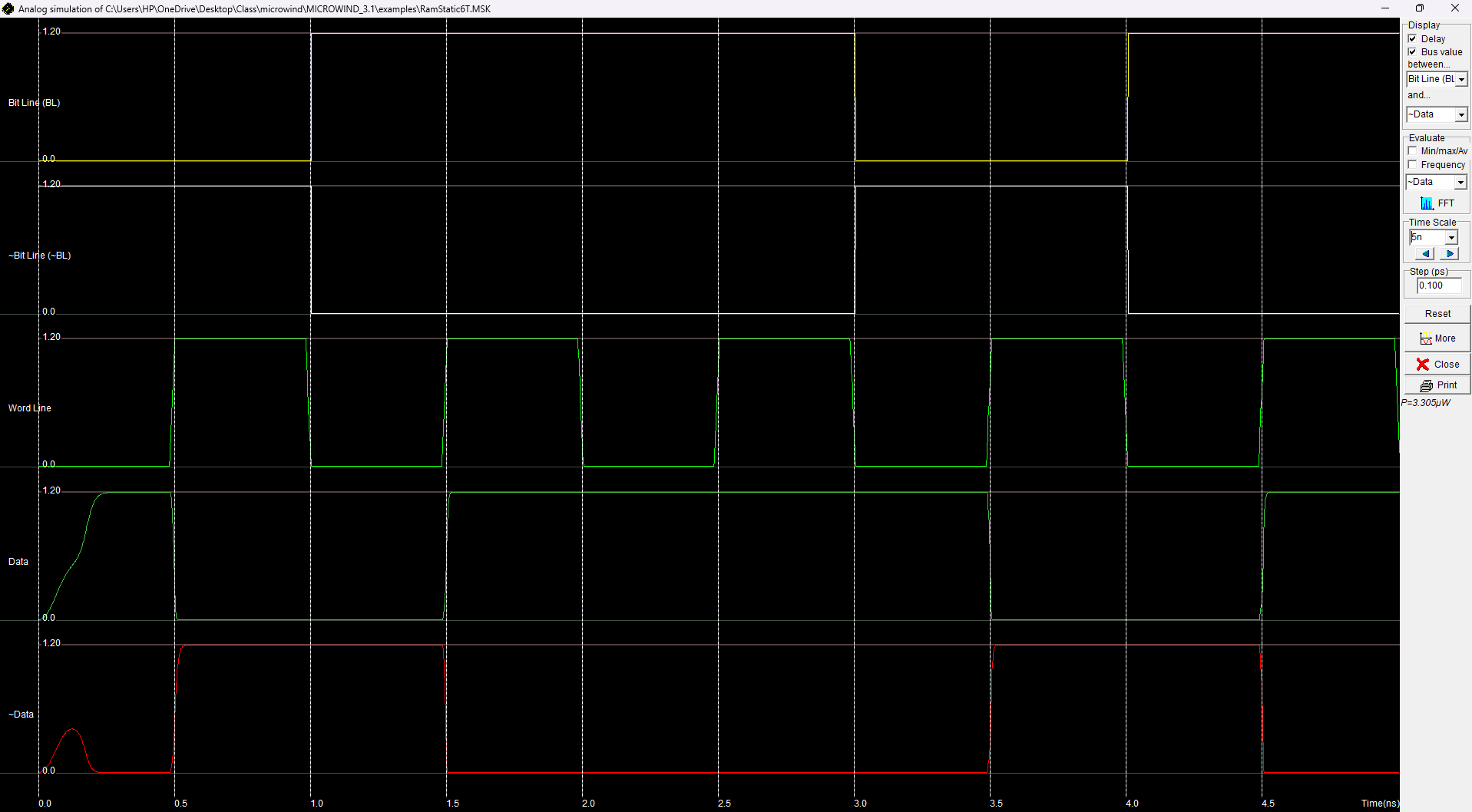
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**Simulation OF 10 T SRAM CELL**

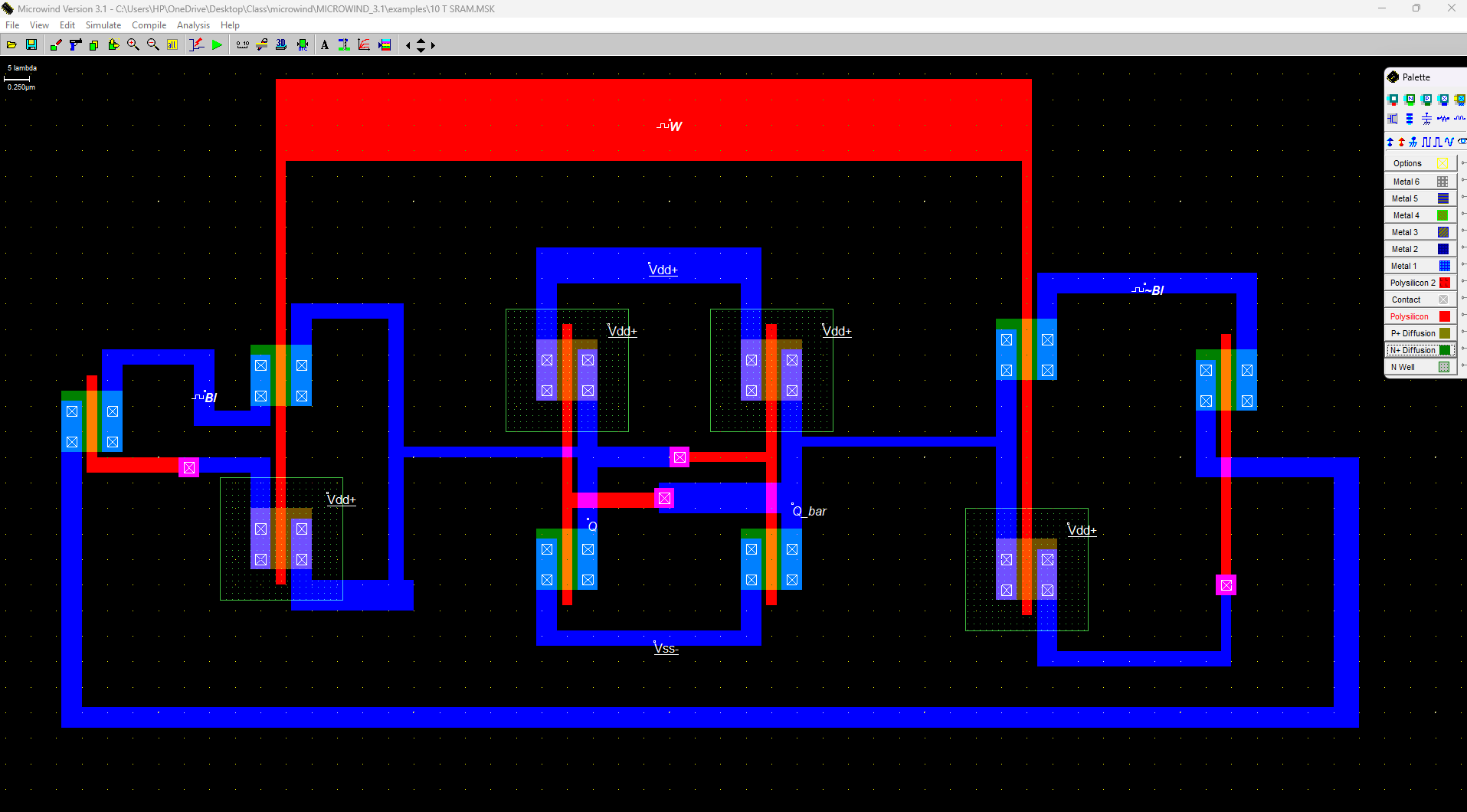
**Microwind Layouts-**



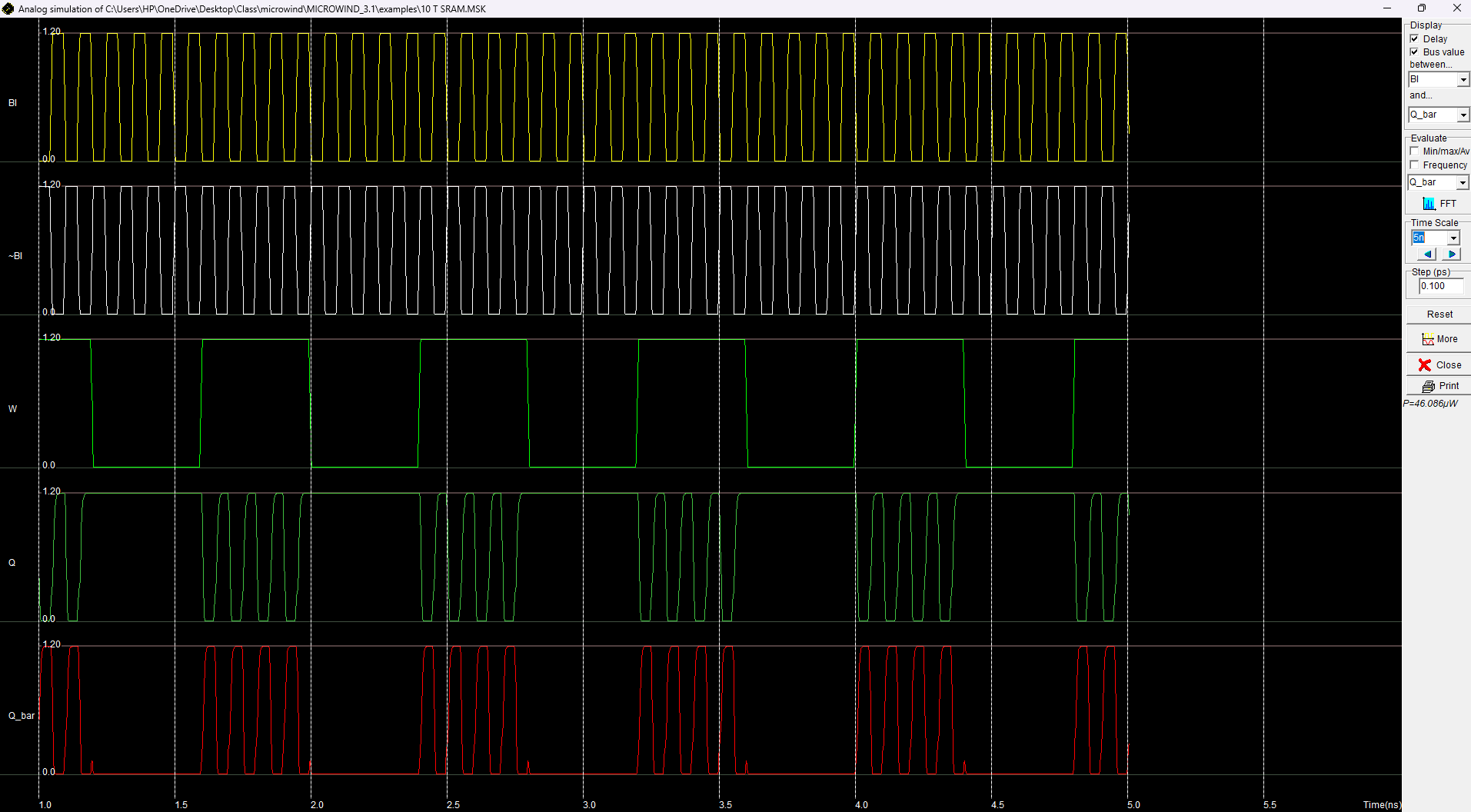
**6T SRAM CELL**

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**Simulation of 6T SRAM CELL**



**10T SRAM CELL**



**Simulation of 10T SRAM CELL**

**Advantages over 6T SRAM CELL-**

**1. Power Consumption**

* 6T SRAM:
  + Read Power: Generally higher due to the need for full bitline precharge to VDDV\_{DD}VDD​ before read operations.
  + Write Power: Moderate, but power spikes can occur as data flips and charges are shared.
  + Standby Power: Low, but leakage current in the standby mode can contribute significantly to power usage, especially in scaled-down nodes (sub-100 nm).
* 10T SRAM:
  + Read Power: Lower than 6T because precharging the bitline to VDD/2V\_{DD}/2VDD​/2 reduces dynamic power consumption.
  + Write Power: Slightly higher due to extra transistors but controlled through selective write transistors.
  + Standby Power: Lower leakage current due to isolated read/write paths and less disturbance in the memory cell during standby.

Comparison Summary: 10T SRAM generally consumes less power during reads and standby but may have a slight increase in write power due to extra transistors.

**2. Leakage Current**

* 6T SRAM:
  + Leakage can be significant, particularly in modern nodes, because all transistors are active during both read and write, and no isolation exists between read/write paths.
  + In a low-power or deep-sleep mode, leakage current can degrade data integrity.
* 10T SRAM:
  + Additional transistors in the 10T cell isolate storage nodes during both read and standby, resulting in a lower leakage current.
  + Reduced soft-error vulnerability due to minimized leakage paths.

Comparison Summary: 10T SRAM has lower leakage current due to the isolation of storage nodes, especially during standby and read operations.

**3. Stability (Read and Write Margins)**

* 6T SRAM:
  + Lower stability during read operations because accessing the bitline directly impacts the storage nodes, which can lead to data flipping in scaled-down technologies.
  + Write margin can be adjusted by sizing transistors, but this can affect read stability negatively, creating a trade-off.
* 10T SRAM:
  + Improved read stability due to the separation of the read path, which prevents the read operation from disturbing the data held in the cell.
  + Write stability is also slightly better, with selective control of write access, reducing the risk of unintended data flipping.

Comparison Summary: 10T SRAM generally has better stability for both read and write operations, as well as a more favorable noise margin.

**4. Performance and Speed**

* 6T SRAM:
  + Typically faster due to its simpler structure and fewer transistors.
  + Some power-performance trade-offs arise if speed is prioritized at the expense of read stability.
* 10T SRAM:
  + Slightly slower due to additional transistors, which increase cell capacitance and delay.
  + More suited for applications where stability and power efficiency are prioritized over raw speed.

Comparison Summary: 6T SRAM tends to be faster, but 10T SRAM provides more reliability, especially in power-constrained environments.

Example Data (Based on Research Papers and Trends)

Here's an example of typical performance metrics, though actual numbers depend heavily on technology and specific design parameters.

| Metric | 6T SRAM (e.g., 65 nm) | 10T SRAM (e.g., 65 nm) |
| --- | --- | --- |
| Read Power | ~50-80 pW/bit | ~30-60 pW/bit |
| Write Power | ~60-90 pW/bit | ~70-100 pW/bit |
| Leakage Current | ~100-150 nA/bit | ~50-100 nA/bit |
| Read Stability (SNM) | Lower (highly variable) | Higher (more robust) |
| Write Stability | Moderate (design dependent) | Improved due to isolation |
| Speed (Access Time) | Faster | Slightly slower |

**Summary of Advantages of 10T Over 6T**

* Power Efficiency: Lower power consumption during read and standby.
* Stability: Improved read and write stability, particularly valuable for low-voltage or noise-sensitive applications.
* Leakage Reduction: Lower leakage current, contributing to longer battery life in low-power applications.
* Noise Immunity: Higher noise margins make it more suitable for aggressive scaling or low-power designs.

**Application-**

The 10T SRAM cell is especially valuable in applications where high stability, low power, and robust read and write operations are essential. Here are some key applications in the electronics industry:

**1. Low-Power Mobile and Wearable Devices**

* Smartphones and tablets demand memory solutions that minimize power usage without sacrificing performance. The reduced leakage current and power efficiency of 10T SRAM cells make them ideal for these devices, which require long battery life.
* Wearable electronics like fitness trackers, smartwatches, and health monitoring devices also benefit from the 10T cell’s low standby power and high reliability, as these devices operate at low voltages and need energy-efficient memory.

**2. Internet of Things (IoT) and Edge Computing**

* IoT devices and edge computing systems are designed for constant connectivity with constrained power and processing capabilities. The low leakage and high stability of 10T SRAM cells make them well-suited for memory in IoT sensors, smart home devices, and industrial IoT applications, where memory stability and low energy consumption are crucial.

**3. Embedded Systems for Automotive and Aerospace**

* Automotive applications, including Advanced Driver Assistance Systems (ADAS), infotainment systems, and other microcontroller-based automotive subsystems, require robust and energy-efficient memory for reliable operation. The high noise margin and low power features of 10T SRAM cells are beneficial in these high-stress environments.
* Aerospace systems, with requirements for stability under extreme conditions, also leverage 10T SRAM cells for critical memory functions, ensuring high reliability and data integrity.

**4. Battery-Powered Medical Devices**

* Many medical devices, such as portable diagnostic tools, implantable devices, and continuous monitoring systems, require long operational life with limited power sources. The 10T SRAM’s energy-efficient and reliable operation makes it suitable for these applications, where memory stability can be life-critical, and power sources like batteries are challenging to replace.

**5. Artificial Intelligence (AI) and Machine Learning (ML) Accelerators**

* AI and ML applications often involve large datasets and require high memory bandwidth and reliability. The 10T SRAM cell can improve memory access stability and efficiency, making it suitable for AI/ML accelerators, which rely on high-performance memory for data processing, caching, and storing weights and parameters.

**6. Low-Voltage Digital Signal Processing (DSP) and Data Processing Units (DPUs)**

* DSPs and DPUs used in applications like image processing, voice recognition, and signal analysis benefit from the 10T SRAM cell's low-voltage operation. It helps reduce overall power consumption in these processors, particularly important for mobile and wearable devices using DSPs for real-time processing.

**7. High-Performance Computing (HPC) Systems and Memory-Intensive Applications**

* In HPC systems, where stable memory access is critical for performance, 10T SRAM cells provide enhanced read stability and low power consumption. They are beneficial in data centers, supercomputers, and servers where power efficiency and thermal management are crucial to operational cost and performance.

**8. Cache Memory for Ultra-Low Power Applications**

* In microcontrollers and microprocessors, where cache memory is essential for high-speed data access, 10T SRAM cells offer low power and improved stability. This makes them an ideal choice for energy-efficient cache memory in applications ranging from consumer electronics to industrial controllers.