# Microcontrollers

Part two of Review

# Microprocessor

*Intel:* 8086, 80286, 80386, 80486, and Pentium

*Motorola:* 68000, 68010, 68020, 68030, 68040

# Microprocessor

## On the chip

   No RAM; No ROM; No I/O ports;

*Intel:* 8086, 80286, 80386, 80486, and Pentium

*Motorola:* 68000, 68010, 68020, 68030, 68040

# Microcontrollers

*Microchip, Motorola, Zilog, Atmel, Dallas Semiconductor:*

- Based on 8051
- Family members of 8051: 8052 and 8031

*Texas Instruments: based on 8751*

*Renesas:* M34501  *Motorola:* 68HC16Z3
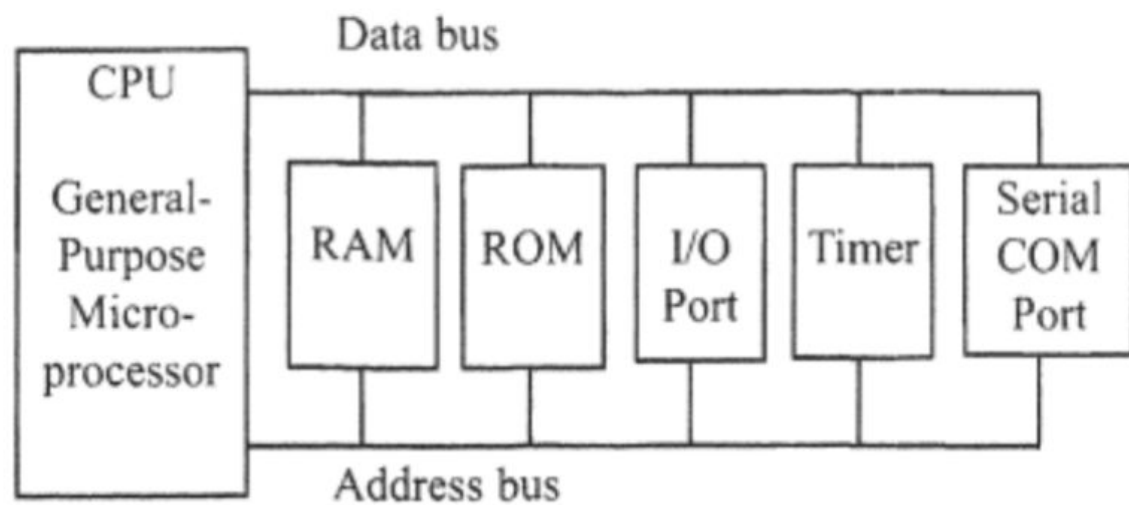
*Sharp:* LH79520
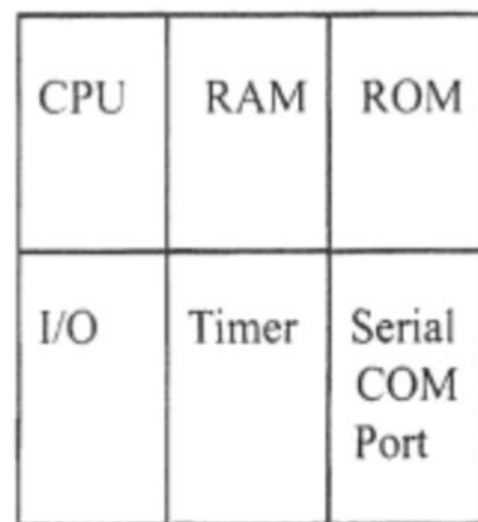
# Microcontroller

CPU

+ RAM + ROM

+ I/O ports + Timers + ...

**On the Chip**

(a) General-Purpose Microprocessor System

(b) Microcontroller
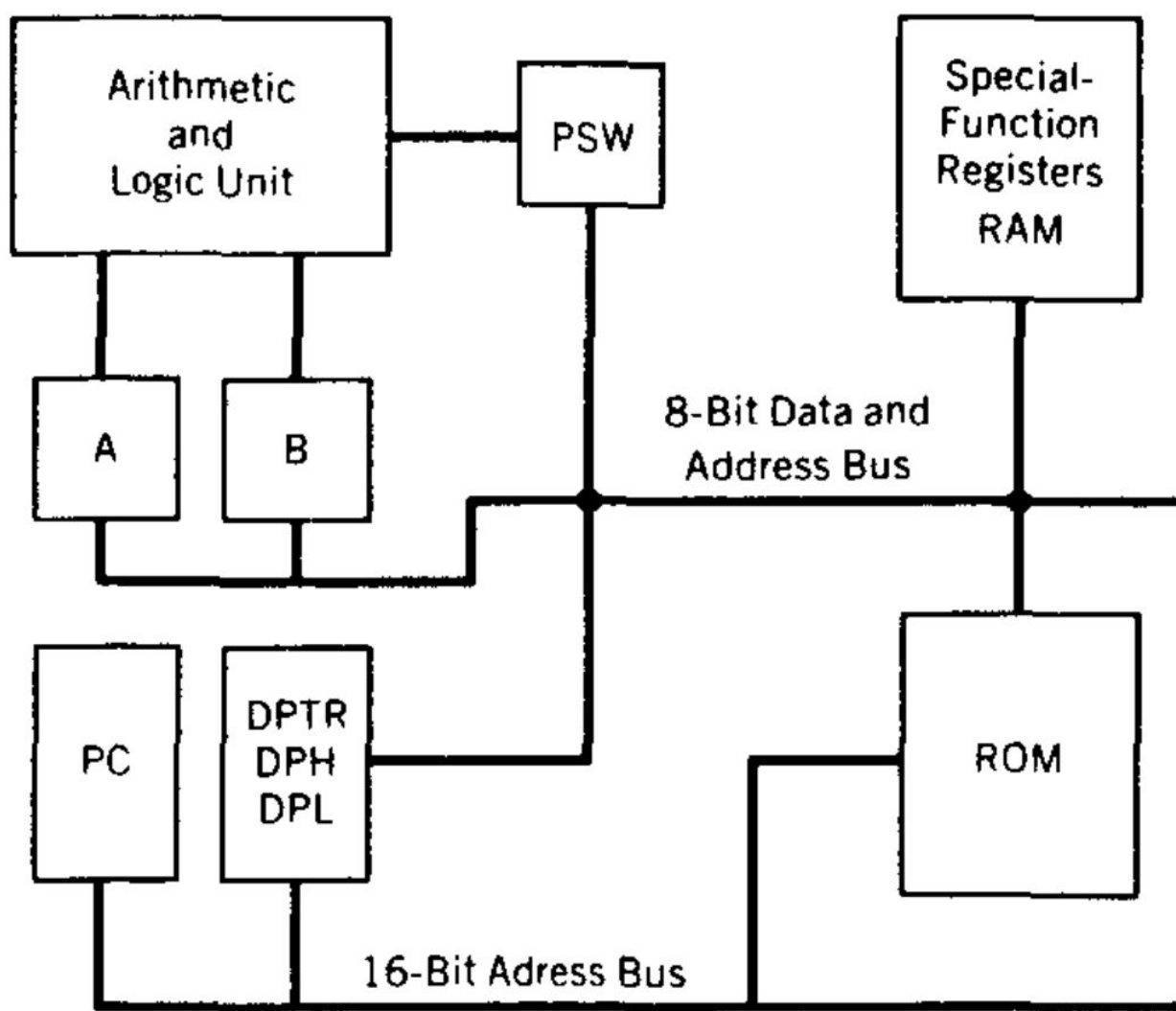
# μCs vs μPs (other diffs)

smaller

cost and space are critical
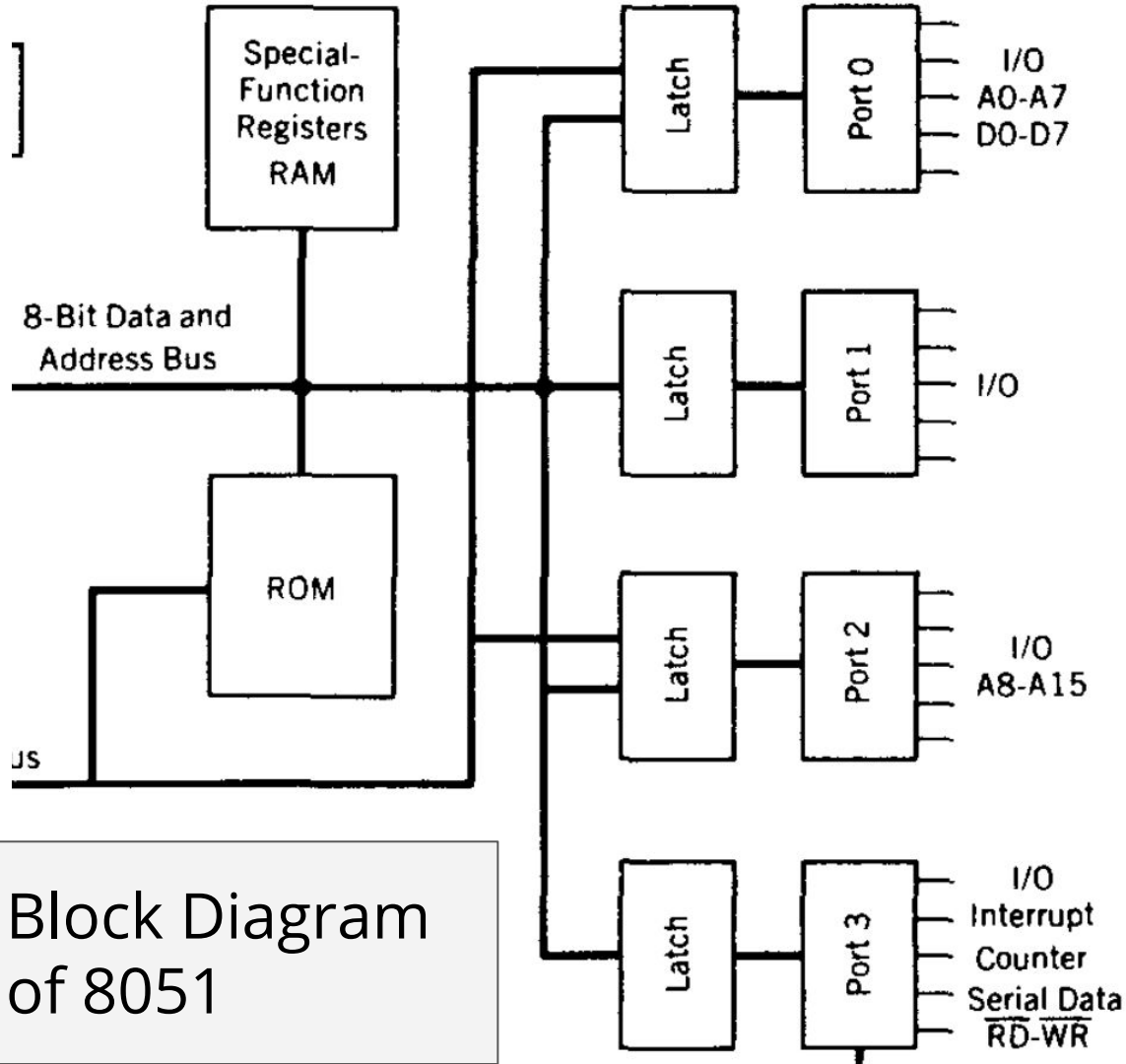
computing power needs are less
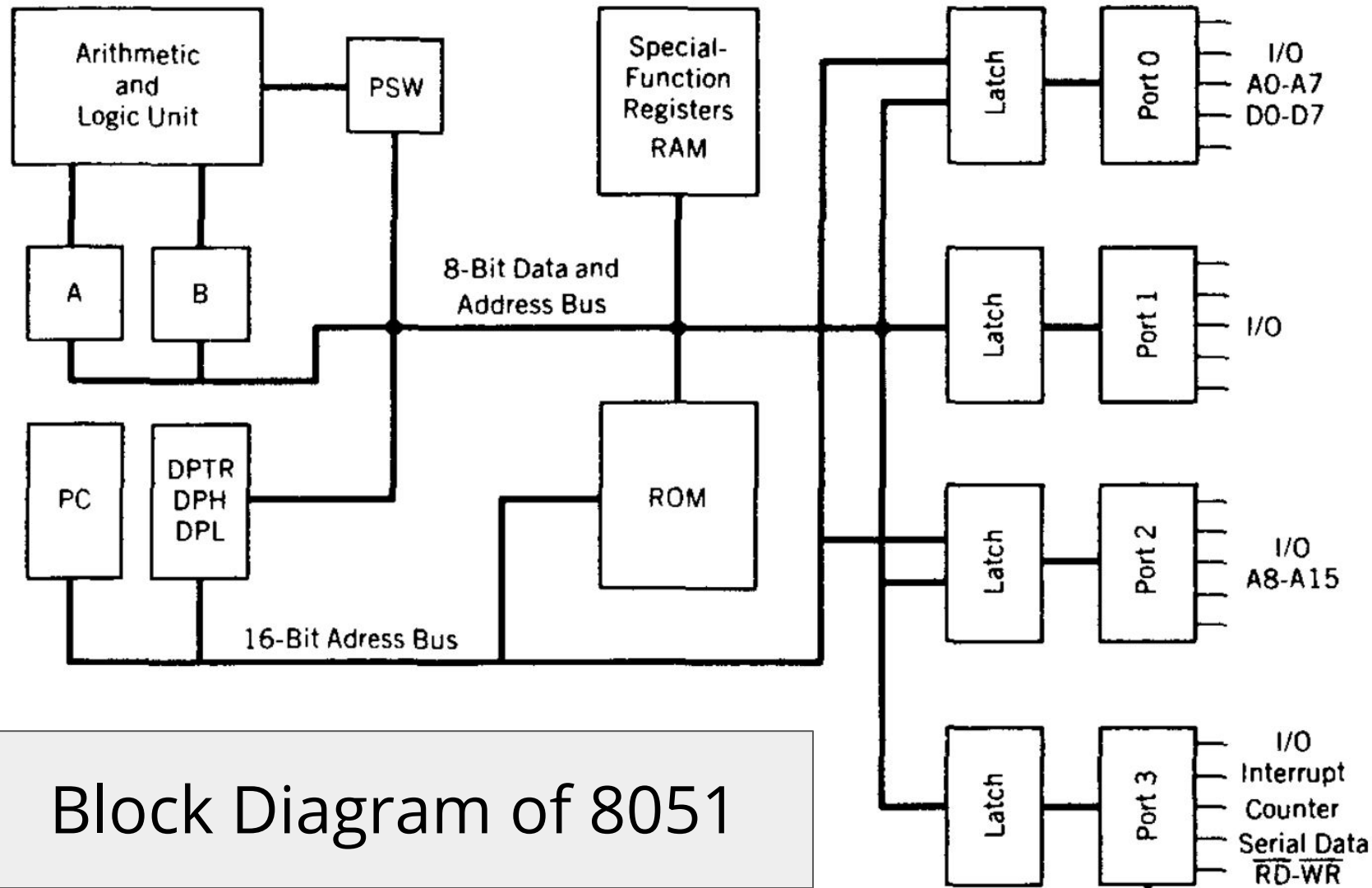
power and price per unit

# 8051 Microcontroller

Internal Architecture

Block Diagram of 8051

Special-Function Registers RAM

8-Bit Data and Address Bus

ROM

Latch — Port 0 — I/O A0-A7 D0-D7

Latch — Port 1 — I/O

Latch — Port 2 — I/O A8-A15
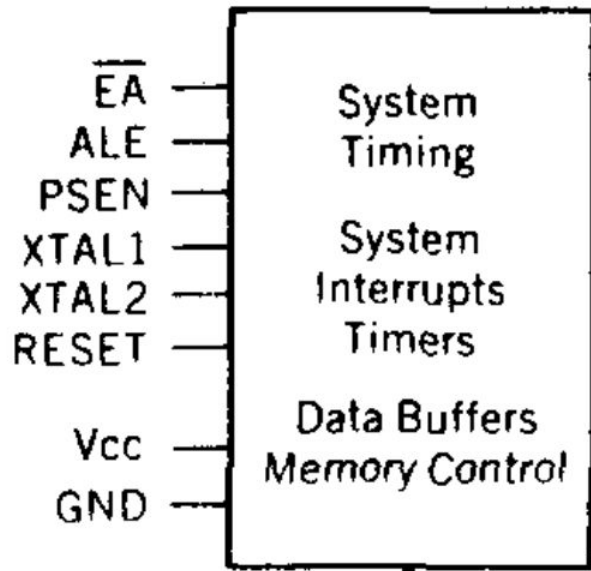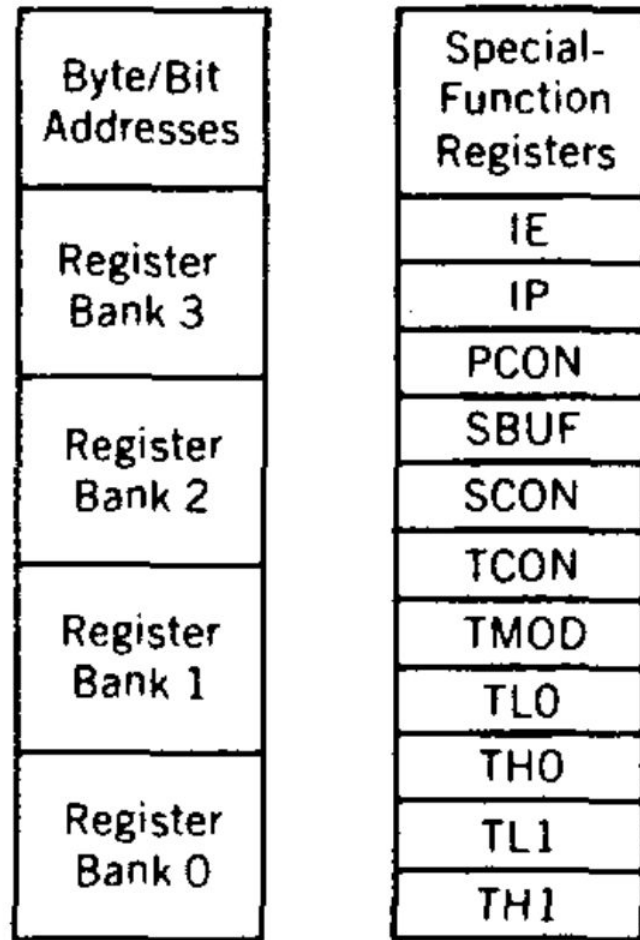
Latch — Port 3 — I/O Interrupt Counter Serial Data RD-WR

Block Diagram of 8051

Block Diagram of 8051

Block Diagram of 8051

**Internal RAM Structure**

Byte/Bit Addresses

| Register Bank 3 |
| Register Bank 2 |
| Register Bank 1 |
| Register Bank 0 |

Special-Function Registers

| IE |
| IP |
| PCON |
| SBUF |
| SCON |
| TCON |
| TMOD |
| TL0 |
| TH0 |
| TL1 |
| TH1 |

Block diagram (left):

EA
ALE
PSEN
XTAL1
XTAL2
RESET

Vcc
GND

System Timing
System Interrupts Timers
Data Buffers Memory Control

**8051 Block Diagram**
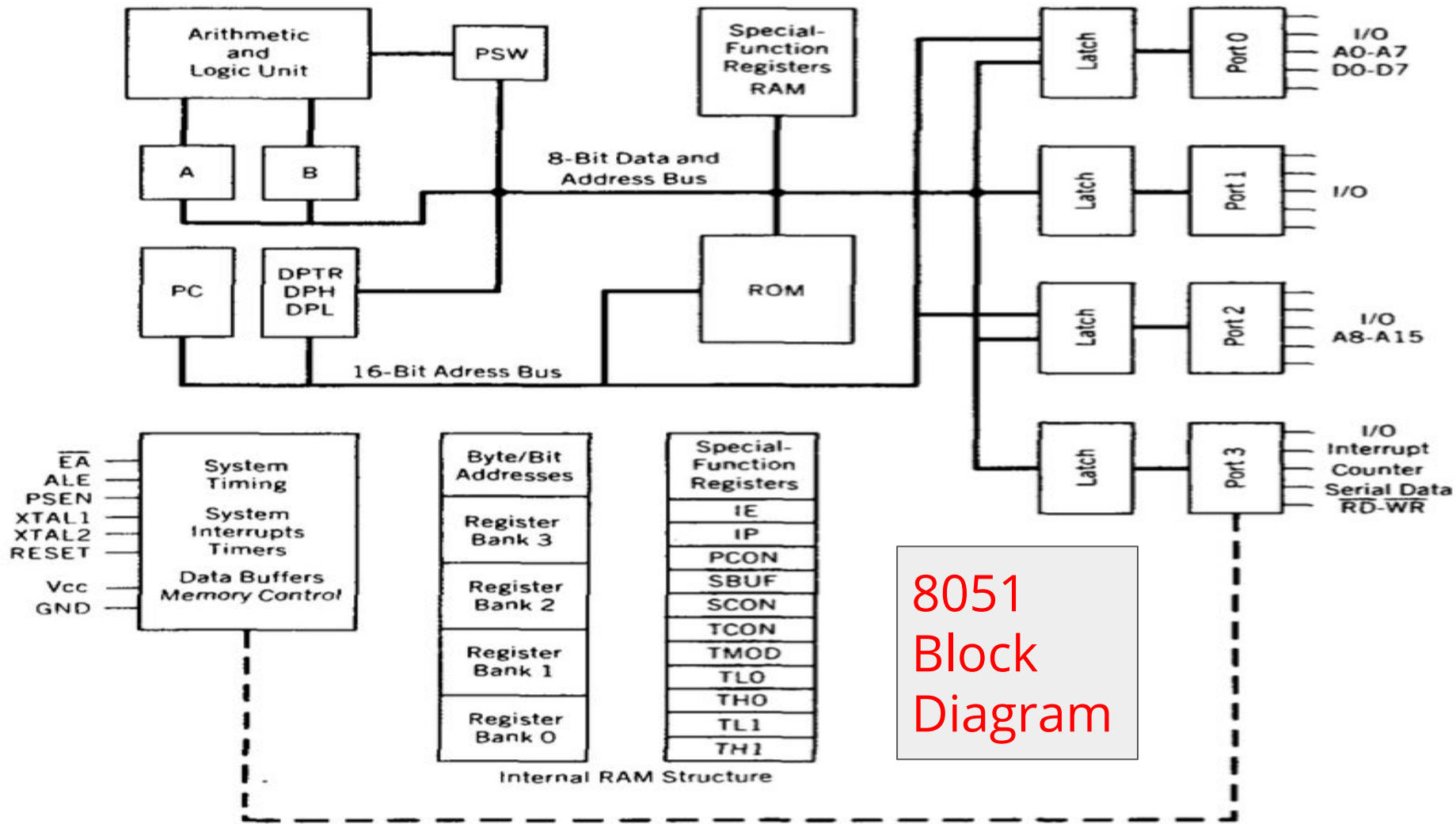
# Internal RAM

# Internal RAM Organization



| | | Working Registers | | Bit Addressable | | General Purpose |
|---|---|---|---|---|---|---|
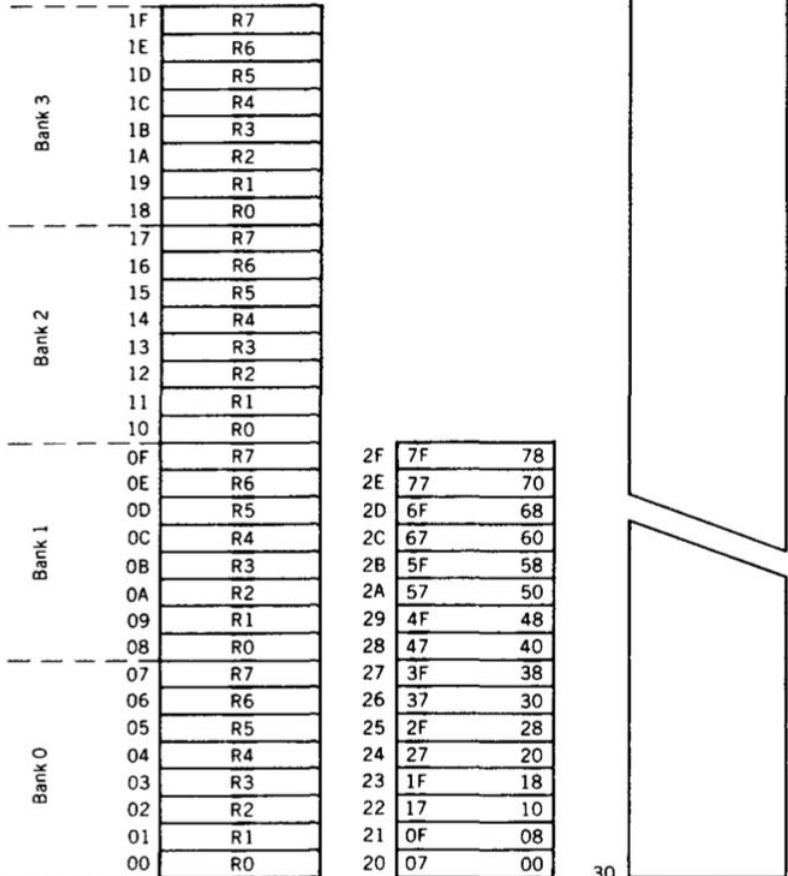
# Internal RAM Organization - Register Banks

| | |
|---|---|
| 11 | R1 |
| 10 | R0 |
| 0F | R7 |
| 0E | R6 |
| 0D | R5 |
| 0C | R4 |
| 0B | R3 |
| 0A | R2 |
| 09 | R1 |
| 08 | R0 |
| 07 | R7 |
| 06 | R6 |
| 05 | R5 |
| 04 | R4 |
| 03 | R3 |
| 02 | R2 |
| 01 | R1 |
| 00 | R0 |

Bank 1

Bank 0

# Internal RAM Organization - Bit/Byte Addressable Area

| | | |
|---|---|---|
| 2F | 7F | 78 |
| 2E | 77 | 70 |
| 2D | 6F | 68 |
| 2C | 67 | 60 |
| 2B | 5F | 58 |
| 2A | 57 | 50 |
| 29 | 4F | 48 |
| 28 | 47 | 40 |
| 27 | 3F | 38 |
| 26 | 37 | 30 |
| 25 | 2F | 28 |
| 24 | 27 | 20 |
| 23 | 1F | 18 |
| 22 | 17 | 10 |
| 21 | 0F | 08 |
| 20 | 07 | 00 |

# Internal RAM Organization
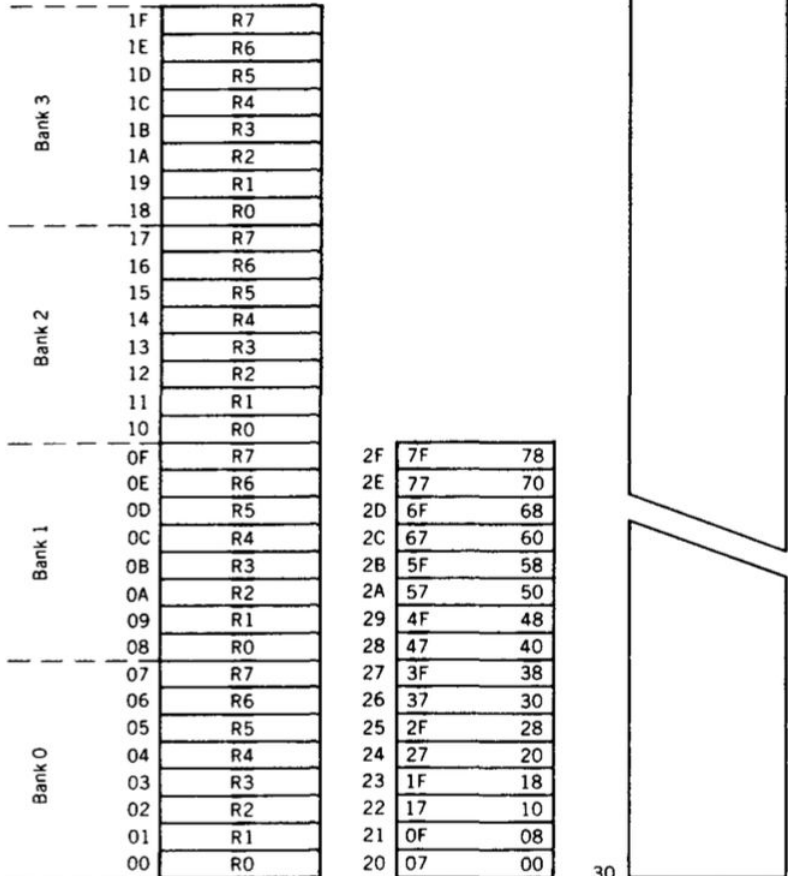
# Internal RAM Organization
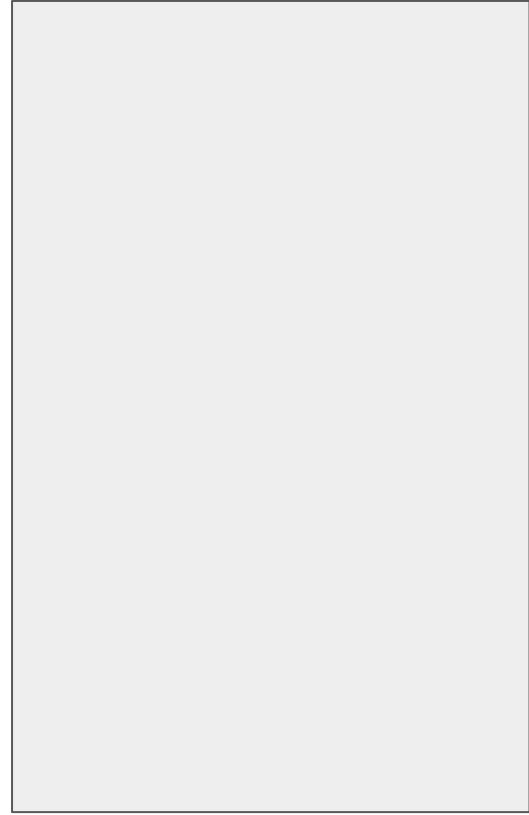-  General Purpose



7F

30

**General Purpose**
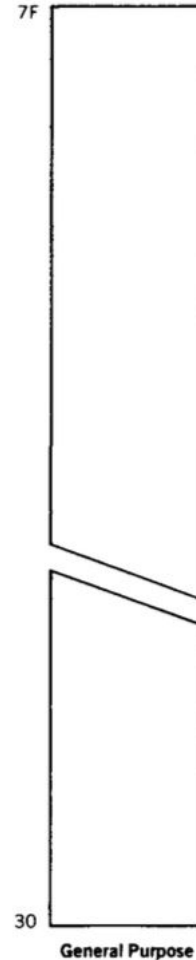
Internal ROM

FFF

000

# Data/Program Architecture

- 8051 is Harvard architecture
    - Program and data memory are different
    - 8051 uses the **same address** for code and data
        - Internal circuitry access the correct memory based on the nature of operation

# Mini Project

Guidelines

# Purpose

To understand Embedded Systems theory better than learning without doing projects.

Plan A

Other Plans

# Plan A - Overview

Use Keil Software Evaluation Version.

- Write small C programs and/or
- Understand a large C program, "Measure"

# Plan A- (Pending) Issues

Limitation of the Keil Evaluation Tool Version.

But you can download the tool to your Windows PC.

# Plan A - Success Strategy

Step-by-Step Introduction in the class to do a project using Keil MicroVision Software

# Other Plans

[EdX Course](#)

# Other Plans

[Free RTOS](#)

# Other Plans

[Simple Scalar Processor Simulator](#)

# Other Plans

[SystemC](SystemC)