The fetch/execute cycle, Instruction decoding and execution

Computer Organization and Architecture

by

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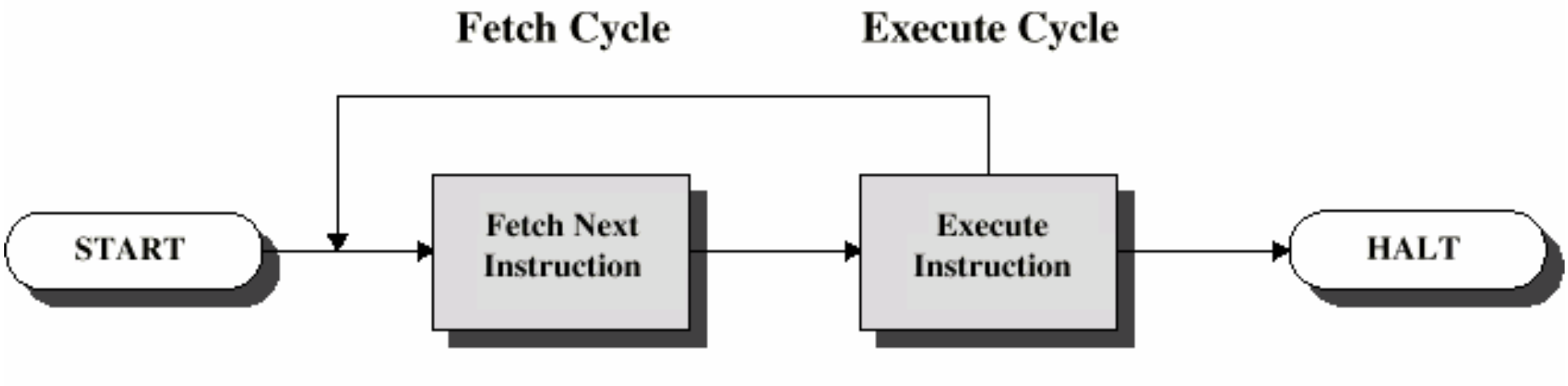
Instruction Cycle

- Two steps:
  - Fetch
  - Execute



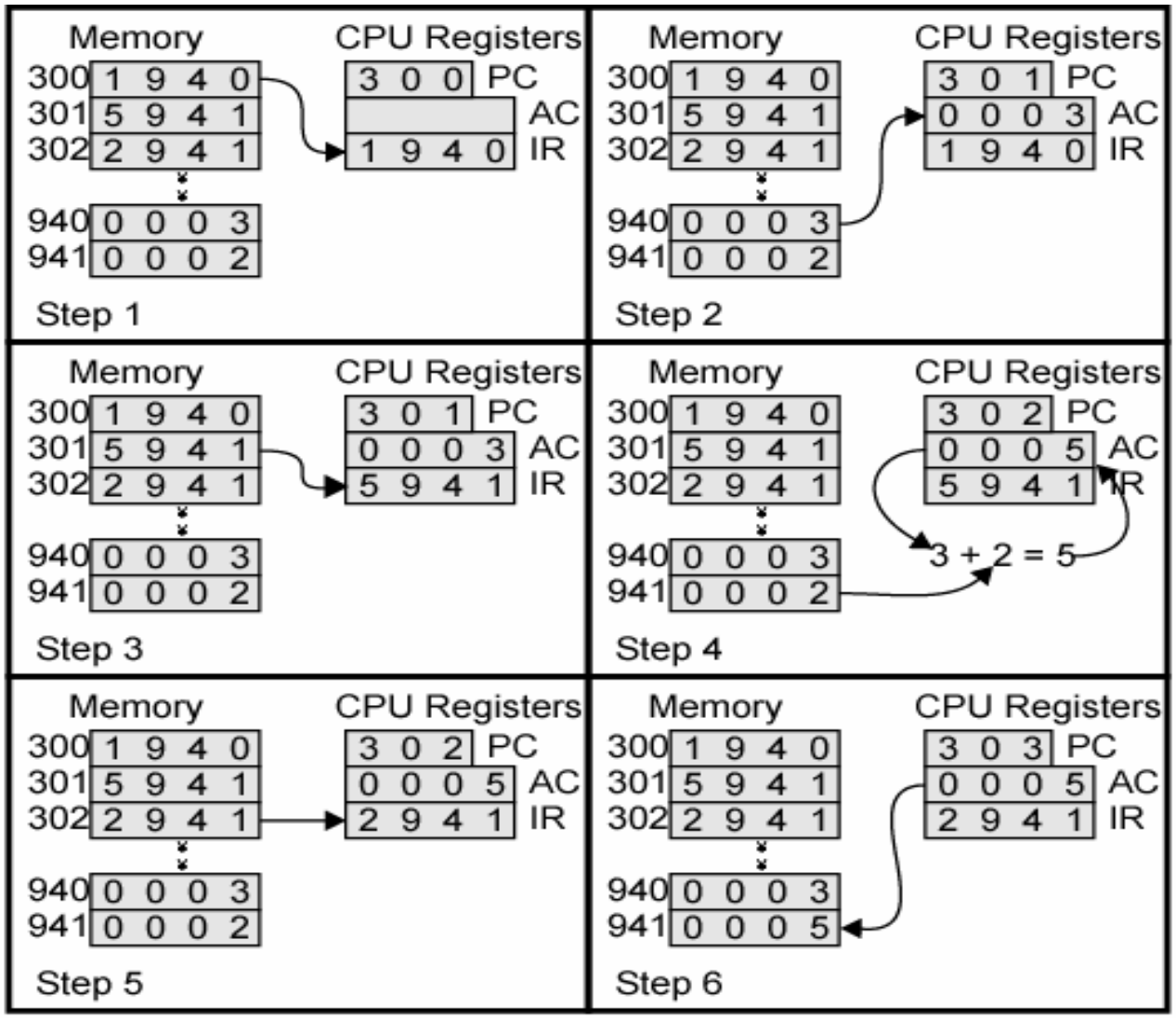
Fetch Cycle

- Program Counter (PC) holds address of next inst. to fetch
- Processor fetches inst. from memory location.
- Increment PC
- Inst. loaded into Instruction Register (IR)
- Processor interprets inst. and performs required actions.

Execute Cycle

- Actions fall into 4 categories
  1. **Processor-memory**
     - data transfer between CPU and main memory
  2. **Processor I/O**
     - Data transfer between CPU and I/O module
  3. **Data processing**
     - Some arithmetic or logical operation on data
  4. **Control**
     - Alteration of sequence of operations
     - e.g. jump
- Combination of above

Example of Program Execution



Explanation

- Step 1:
  - PC=300, the address of the first inst.
  - Inst. (the value 1940 in Hex) is loaded into the IR.
  - PC Incremented.
- Step 2:
  - First 4 bits(First Hex digit) in IR indicate that AC is to be loaded.
  - Remaining 12 bits (3 Hex digits) specify the address (940) from which data are to be loaded.
- Step 3:
  - Next inst. (5941) is fetched from location.
  - PC incremented.

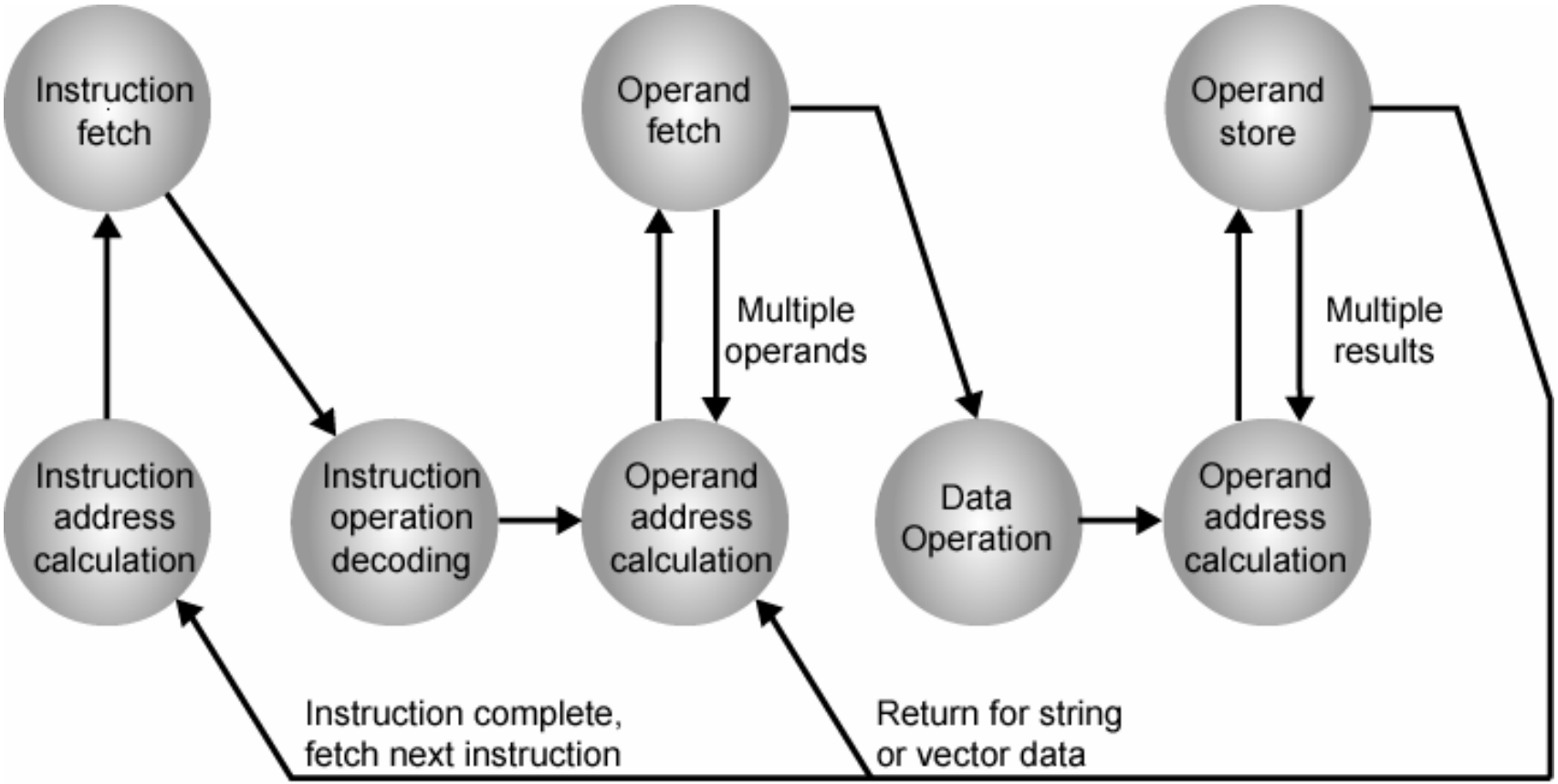
Explanation Conti..

- Step 4:
  - Old contents of the AC and the contents of location 941 are added
  - Result is stored in the AC.
- Step 5:
  - Next inst. (2941) is fetched from location 302
  - PC is incremented.
- Step 6:
  - Contents of the AC are stored in location 941.

Example: (PDP-11 Instruction Expressed Symbolically)

- **ADD B,A**
  - Stores the sum of B and A into memory location A.
  - A single instruction cycle with the following steps occurs:
    - Fetch the ADD instruction.
    - Read the content of memory location A into the processor.
    - Read the content of memory location B into the processor.
    - Add the Two values.
    - Write the result from the processor to memory location A.

Instruction Cycle State Diagram



Explanation

- IAC :
  - Determine the Address of the next inst. to be executed .
  - If each instruction is 16 bits long and memory is organized into 16 bit words, then add 1 to the previous address.
  - If, instead, memory is organized as 8-bit bytes, then add 2 to the previous address.
- Instruction fetch (IF):
  - Read instruction from its memory location into the processor.

Explanation conti……

- Instruction operation decoding (IOD):
  - Analyze instruction to determine
    - type of operation to be performed and
    - operands to be used.
- Operand address calculation (OAC):
  - If the operation involves reference to an operand in memory or available via I/O ,then determine the address of operand.

- Operand Fetch (OF):

  Fetch the operand from memory or read it from I/O.
- Data Operation (DO):

  Perform the operation indicated in the instruction .
- Operand Store (OS):

  write the result into memory or put to I/O.
- **Example:**

PDP-11

ADD A,B results in the following sequence of states:
IAC,IF,IOD,OAC,OF,OAC,OF,DO,OAC,OS.