**ITE 204 Computer Architecture and Organization**

**Model question paper**

Time: 3 hours Max. Marks: 100

Part-A

Answer all of the following (8 x 5marks = 40 marks)

1. What are the salient features of Von Neumann model?
2. How is addition/subtraction performed in ALU? Draw the circuit. Suggest a method to outperform the model.
3. How is data deleted in NAND flash memories?
4. Differentiate between programmed I/O and interrupt I/O techniques.
5. What is SMART technology? Is it error free?
6. Perform 14-32 in two's complement notation.
7. What are the various kinds of cache? What is the expression for average memory access time in two level cache hierarchy? State your assumptions.
8. Consider a quad processor. Design the two level cache for this system.

Part-B

Answer any SIX of the following (6 x 10 marks = 60 marks)

9. Describe the various instruction formats. Which do you recommend in the design of ISA of computer system? Give example of each format.
10. Describe how Booth's multiplication is performed using one example.
11. What is paging? Consider a memory of four frames. The following pages are accessed during process execution.

10, 12, 13, 1, 10, 12, 1, 34, 45, 23, 7, 10, 12, 34

Derive the hit ratio, miss ratio using

a. FIFO
b.OPT
c. LRU

replacement algorithms.

12. Explain DMA. Can a system have multiple DMA controllers?
13. Explain RAID architecture.
14. Show how the following instructions are executed in CPU having one adder/subtractor unit and one logic unit.

add r1, r2, r3
sub r1, r4, r5
xor r1, r6, r7

where the instruction is of the format

opcode destination, source1, source2

Show the hazards in the above program segment.

15. Write notes on

a. interrupts
b. bus arbitration

16. Describe the division algorithm with suitable example.