

ITE204	Computer Architecture and Organization	L	T	P	C
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Prerequisite	Digital Electronics and Microprocessors				
Objectives	<ul style="list-style-type: none"> To Gain an understanding of computer data representation and manipulation To understand the basic organization for data storage and access across various media. To provide knowledge of interfacing techniques and subsystem devices. 				
Outcomes	<p>The students will be able to</p> <ul style="list-style-type: none"> Understand number systems, instruction sets, addressing modes, and data/instruction formats. Write program using assembly language programming. Understand memory control, direct memory access, interrupts, and memory organization 				
Unit I	FUNDAMENTALS OF COMPUTER ARCHITECTURE Organization of the von Neumann machine; Instruction formats; The fetch/execute cycle, instruction decoding and execution; Registers and register files; Instruction types and addressing modes; Subroutine call and return mechanisms; Programming in assembly language; I/O techniques and interrupts; Other design issues.				
Unit II	COMPUTER ARITHMETIC Data Representation, Hardware and software implementation of arithmetic unit for common arithmetic operations: addition, subtraction, multiplication, division(Fixed point and floating point); Conversion between integer and real numbers; The generation of higher order functions from square roots to transcendental functions; Representation of non-numeric data (character codes, graphical data);				
Unit III	MEMORY SYSTEM ORGANIZATION AND ARCHITECTURE Memory systems hierarchy; Coding, data compression, and data integrity; Electronic, magnetic and optical technologies; Main memory organization, Types of Main memories, and its characteristics and performance; Latency, cycle time, bandwidth, and interleaving; Cache memories (address mapping, line size, replacement and write-back policies); Virtual memory systems; Reliability of memory systems; error detecting and error correcting systems.				
Unit IV	INTERFACING AND COMMUNICATION I/O fundamentals: handshaking, buffering; I/O techniques: programmed I/O, interrupt-driven I/O, DMA; Interrupt structures: vectored and prioritized, interrupt overhead, interrupts and reentrant code; Buses: bus protocols, local and geographic arbitration.				
Unit V	DEVICE SUBSYSTEMS External storage systems; organization and structure of disk drives and optical memory; Basic I/O controllers such as a keyboard and a mouse; RAID architectures; Video control; I/O Performance; SMART technology and fault detection; Processor to network interfaces.				
Text Books	<ol style="list-style-type: none"> J. L. Hennessy & D.A. Patterson, Computer architecture: A quantitative approach, Fourth Edition, Morgan Kaufman, 2004. W. Stallings, Computer organization and architecture, Prentice-Hall, 2000 M. M. Mano, Computer System Architecture, Prentice-Hall J. P. Hayes, Computer system architecture, McGraw Hill 				
MoE	Written examinations, seminar, assignments, surprise tests and quizzes				
Recommended by the Board of Studies on					
Date of Approval by the Academic Council					