VIT UNIVERSITY
(Estd. u/s 3 of UGC Act 1956)

Term End Examination - November 2012

Course : ITE205 - Digital Electronics and Microprocessors **Slot: G2+TG2**

Class NBR : 4059/ 4054

Time : Three Hours **Max.Marks:100**

PART – A (8 X 5 = 40 Marks)
Answer ALL the Questions

1. Perform each of the following computations using signed, 8-bit words (7 magnitude bits plus a sign bit) in 1's complement and 2's compliment binary arithmetic:

   a) $(+42)_{10} + (-24)_{10}$ **[3]**

   b) $(-15)_{10} + (-12)_{10}$ **[2]**

2. Realize Boolean function given F(A,B,C)= $\sum m(0,3,4,5,7)$ by using a 4x1 multiplexer **[5]**

3. Tabulate the operation of a positive Edge Triggered S-R flip flop and explain. **[5]**

4. Determine the number of Flip-Flops needed to construct a shift register capable of storing.

   a) A 7-bit binary number. **[1]**

   b) Decimal number up to 16. **[2]**

   c) Hexadecimal Number up to FF. **[1]**

   d) Octal number up to 7777. **[1]**

5. Design a PROM to generate the Boolean functions given **[5]**

   $Y_0 = ABC$

   $Y_1 = \overline{A}\,\overline{B}$

   $Y_2 = A$

   $Y_3 = A\,\overline{B}$

6. Design a sequential circuit using JK flip flop in which output frequency is one fourth of the input frequency. Also sketch the waveforms. **[5]**

7. Explain the Flag Register of Intel 8086 IC with a suitable diagram. **[5]**

8. What are the basic modes that an 8255 can operate? Explain the control word format for BSR mode. **[5]**

PART – B (6 X 10 = 60 Marks)

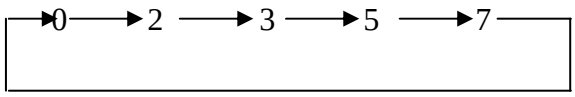
Answer any <u>SIX</u> Questions

9. a) Using K-Map F(A,B,C,D)=∑m(7,9,10,11,12,13,14,15) find SOP and POS expressions **[4]**

   b) Find number 8-cubes, 4-cubes, 2-cubes and singles in both SOP and POS forms **[2]**

   c) Draw SOP and POS circuits **[4]**

10. a) Design and realize Mod-5 Synchronous Counter for the following sequence using JK Flip Flops **[7]**



   b) A shift register has eight Flip-Flops. What are the largest binary number decimal number, hexa decimal number that can be stored in it. **[3]**

11. Design a successive approximation analog to digital converter circuit. **[10]**

12. a) Write a program to move the contents of the memory location 0500H to register BX and to CX. Add immediate byte 05H to the data residing in memory location, whose address is computed using DS=2000H and offset=0600H. Store the result of the addition in 0700H. Assume that the data is located in the segment specified by the data segment register DS which contain 2000H. **[5]**

   b) Design a 4 bit parallel subtractor circuit to subtract the given binary numbers, 1011 & 1110. **[5]**

13. Design a programmable timer using 8253 and 8086. Interface 8253 at an address 0040h for counter 0 and write the following ALPs. The 8086 and 8253 run at 6 MHz and 1.5 MHz respectively. **[10]**

i) To generates a square wave of period 5 ms.

ii) To interrupt the processor after 15 ms.

iii) To derive a monoshot pulse with quasistable state duration 10 ms.

iv) Draw the Interface diagram for the above.

14. a) Design and realize 4 bit SISO shift Register for the data 1101 is given as an input. **[6]**

b) If $\bar{x} + \bar{y} = 0$ then prove the following: **[4]**

$$\bar{x}y + \bar{y}x + xz = x\bar{y} + yz$$

15. a) What are the different addressing modes supported by 8086? Explain each of them with suitable examples. **[8]**

b) Perform division in binary: 11111111 / 101 **[2]**

16. a) Write down the state of six 8086 conditional flags along with the register contents after each of the following instruction is executed. Assume all the flags are reset before execution. **[5]**

MOV AL, AH

ADD BL, CL

ADD CL, DH

OR CX, BX Take AX= 0A443H, BX = 2BC3H, CX = 00A2H, DX= 1EFFAH

b) Calculate the 20 bit physical address, if the segment address is 1055H and the offset address is 5566H. **[5]**

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