VIT UNIVERSITY
(Estd. u/s 3 of UGC Act 1956)

Regular Arrear Examination - December 2013

Course : ITE205 - Digital Electronics and Microprocessor

Time : Three Hours **Max.Marks:100**

PART – A (8 X 5 = 40 Marks)
Answer ALL Questions

1. Perform each of the following computations using signed,8-bit words(7 magnitude bits plus a sign bit)in 1's complement and 2's compliment binary arithmetic:
   a) $(+ 42)_{10} + (- 87)_{10}$ **[3]**
   b) $(- 105)_{10} + (- 120)_{10}$ **[2]**
2. Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers and explain.
3. Derive the characteristic equations of D and JK Flip-Flops.
4. Determine the number of Flip-Flops needed to construct a shift register capable of storing.
   a) A 16-bit binary number **[1]**
   b) Decimal number up to 32 **[2]**
   c) Hexadecimal Number up to FFF? **[1]**
   d) Octal number up to 777? **[1]**
5. Design a PROM to generate the Boolean functions given
   $Y_0 = ABC$
   $Y_1 = \overline{A}\,\overline{B}$
   $Y_2 = A$
   $Y_3 = A\,\overline{B}$
6. Explain the Flag Register of Intel 8086 IC with a suitable diagram.
7. Explain about Control, Data and Address bus for any Micro processor architecture1
8. What are the basic modes that an 8255 can operate? Explain the control word format for BSR mode.

PART – B (6 X 10 = 60 Marks)

Answer any SIX Questions

9. a) Using K-Map F(A,B,C,D)=∑m(7,9,10,11,12,13,14,15) find SOP and POS expressions. **[4]**

   b) Find number 8-cubes,4-cubes,2-cubes and singles in both SOP and POS forms. **[2]**

   c) Draw SOP and POS circuits. **[4]**

10. a) Design a sequential circuit using JK flip flop in which output frequency is one fourth of the input frequency. Also sketch the waveforms. **[5]**

    b) Design and Realize 4 bit SISO shift Register for the following data 1101 is given as an input. **[5]**

11. a) Design a Dual slope A/D Converter. **[5]**

    b) Design Ladder type D/A Converter. **[5]**

12. Write a program to move the contents of the memory location 0600H to register BX and to CX. Add immediate byte 05H to the data residing in memory location,whose address is computed using DS=2000H and offset=0700H. Store the result of the addition in 0800H. Assume that the data is located in the segment specified by the data segment register DS which contain 2000H. **[10]**

13. Design a programmable timer using 8253 and 8086. Interface 8253 at an address 0040h for counter 0 and write the following ALPs. The 8086 and 8253 run at 6 MHz and 1.5 MHz respectively. **[10]**

    i) To generates a square wave of period 1 ms.

    ii) To interrupt the processor after 10 ms.

    iii) To derive a monoshot pulse with quasistable state duration 5 ms.

    iv) Draw the Interface diagram for the above.

14. Find the addressing modes and calculate the physical address for the following instructions. Assume the content in CS =1000H, DS=2000H, ES= 3000H, SS=4000H, SI=1000H, DI=2000H, SP=1000H, BP=2000H and BX=1500H. **[10]**

    i) MOV AX, [1000H]

    ii) MOV AX, [SI]

    iii) MOV AX, 1388H [BX] [SI]

    iv) MOV AX, [BX+2H]

    v) MOV AX, [BX]

15. a) Design a Full Adder using 3x8 line designed decoder. **[5]**

b) Design and explain the operation of 4 : 2 line Encoder using Logic gates. **[5]**

16. a) Write down the state of six 8086 conditional flags along with the register contents after each of the following instruction is executed. Assume all the flags are reset before execution. **[5]**

MOV AL, AH

ADD BL, CL

ADD CL, DH

OR CX, BX Take AX= 0A443H, BX = 2BC3H, CX = 00A2H, DX= 1EFFAH

b) Calculate the 20 bit physical address, if the segment address is 1556H and the offset address is 5550H. **[5]**

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