

# MOSFET – N-Channel, QFET

**400 V, 16 A, 270 mΩ**

## FQP17N40

### Description

This N-Channel Enhancement Mode Power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

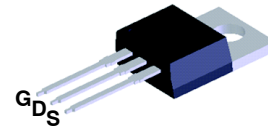
- 16 A, 400 V  $R_{DS(on)} = 270 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 8.0 \text{ A}$
- Low Gate Charge (Typ. 45 nC)
- Low  $C_{TSS}$  (Typ. 30 pF)
- 100% Avalanche Tested
- This Device is Pb-Free.

### ABSOLUTE MAXIMUM RATINGS

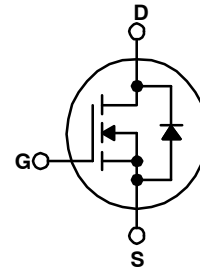
( $T_C = 25^\circ\text{C}$  unless otherwise noted.)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	400	V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ ) – Continuous ( $T_C = 100^\circ\text{C}$ )	16 10.1	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	64	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1000	mJ
$I_{AR}$	Avalanche Current (Note 1)	16	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	17	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5	V/ns
$P_D$	Power Dissipation – ( $T_C = 25^\circ\text{C}$ ) – Derate Above $25^\circ\text{C}$	170 1.35	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	$-55$ to $+150$	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



TO-220-3  
CASE 340AT



### MARKING DIAGRAM

&Z&3&K FQP 17N40
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&Z = Assembly Plant Code  
 &3 = Date Code (Year & week)  
 &K = 2-Digit Lot Code  
 FQP17N40 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
FQP17N40	TO-220-3 (Pb-Free)	1000 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](http://BRD8011/D).

# FQP17N40

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max	0.74	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	400	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to 25°C	–	0.44	–	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, T_C = 125^\circ\text{C}$	–	–	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.0\text{ A}$	–	0.21	0.27	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 8.0\text{ A}$	–	13	–	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	1800	2300	pF
$C_{oss}$	Output Capacitance		–	270	350	pF
$C_{rss}$	Reverse Transfer Capacitance		–	30	40	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 200\text{ V}, I_D = 17.2\text{ A}, R_G = 25\text{ }\Omega$ (Note 4)	–	40	90	ns
$t_r$	Turn-On Rise Time		–	185	380	ns
$t_{d(off)}$	Turn-Off Delay Time		–	90	190	ns
$t_f$	Turn-Off Fall Time		–	105	220	ns
$Q_g$	Total Gate Charge	$V_{DS} = 320\text{ V}, I_D = 17.2\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	–	45	60	nC
$Q_{gs}$	Gate-Source Charge		–	11.4	–	nC
$Q_{gd}$	Gate-Drain Charge		–	21.7	–	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current		–	–	16	A
I <sub>SM</sub>	Maximum Pulsed Drain–Source Diode Forward Current		–	–	64	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 16 A	–	–	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 17.2 A, dI <sub>F</sub> /dt = 100 A/μs	–	290	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	2.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 6.8\text{ mH}$ ,  $I_{AS} = 16\text{ A}$ ,  $V_{DD} = 50\text{ V}$ ,  $R_G = 25\text{ }\Omega$  starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 17.2\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

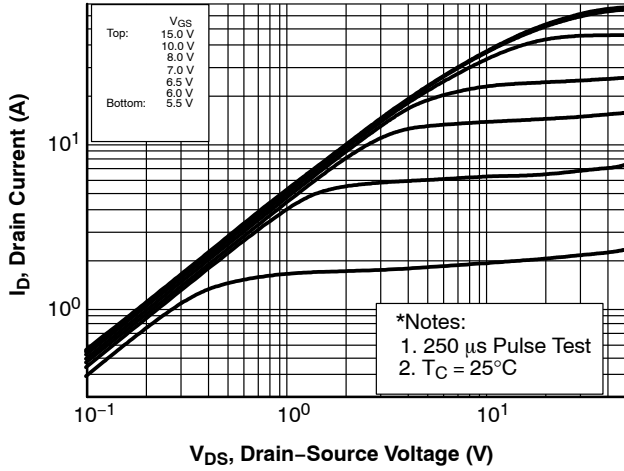


Figure 1. On-Region Characteristics

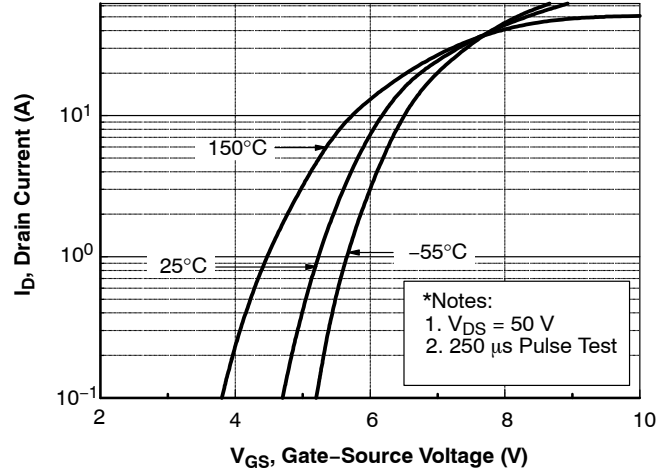


Figure 2. Transfer Characteristics

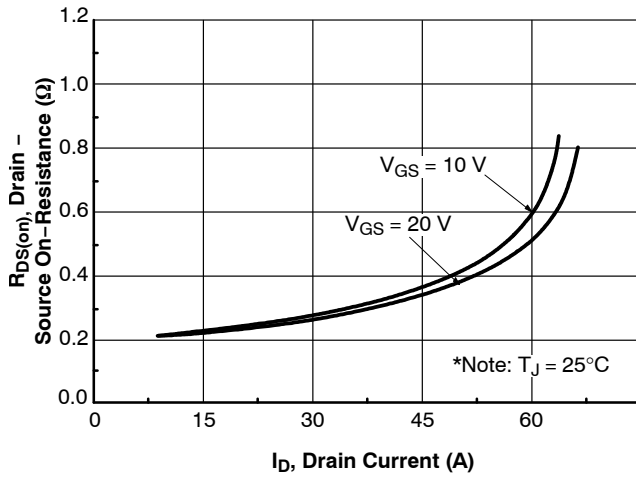


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

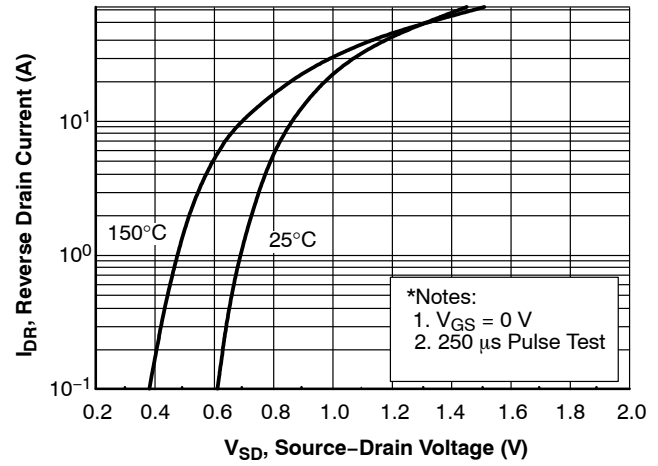


Figure 4. Body Diode Forward Voltage Variation vs Source Current and Temperature

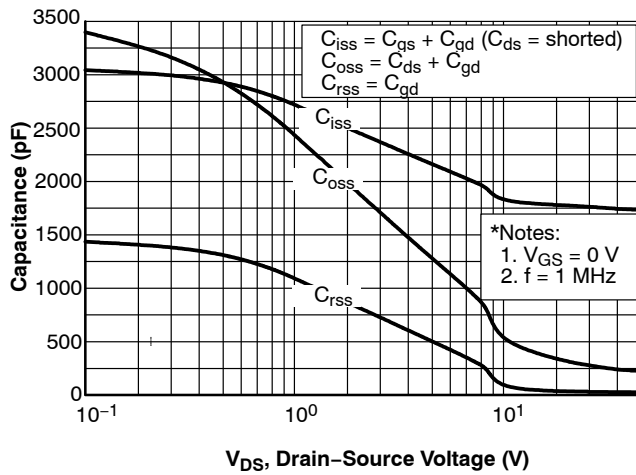


Figure 5. Capacitance Characteristics

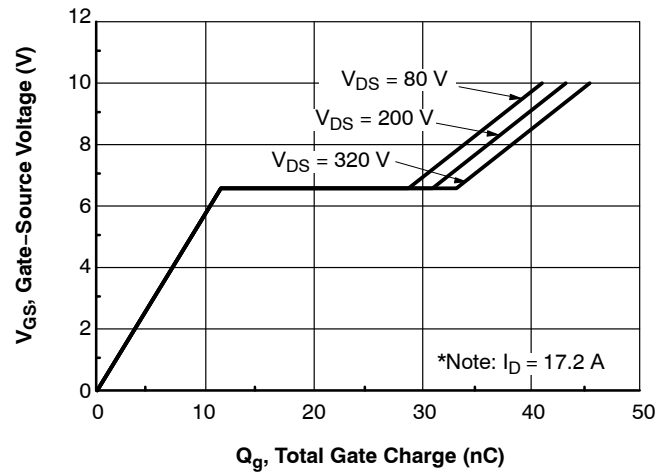


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

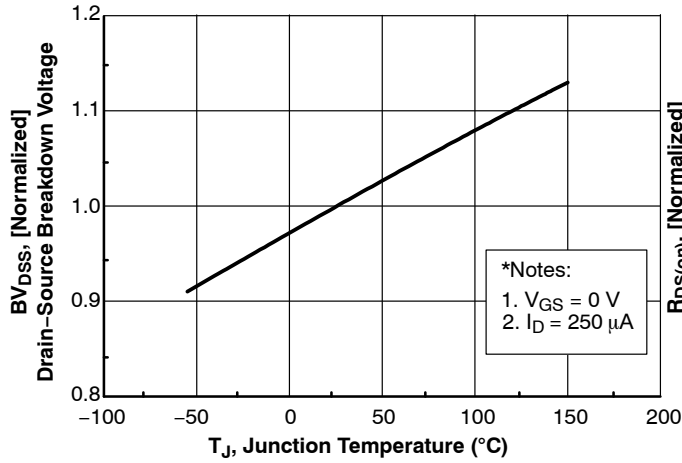


Figure 7. Breakdown Voltage Variation vs Temperature

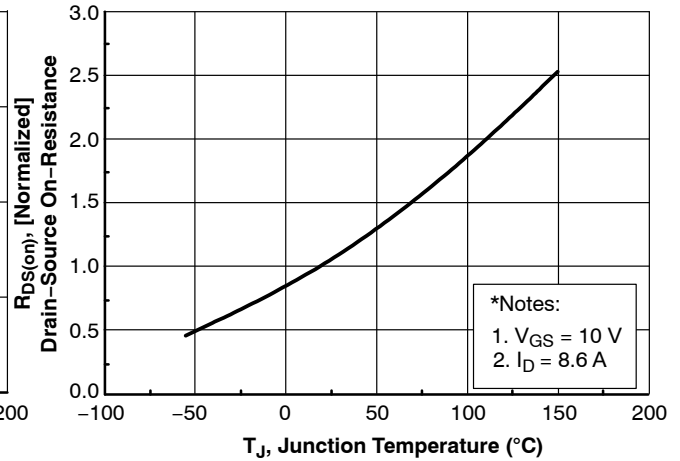


Figure 8. On-Resistance Variation vs Temperature

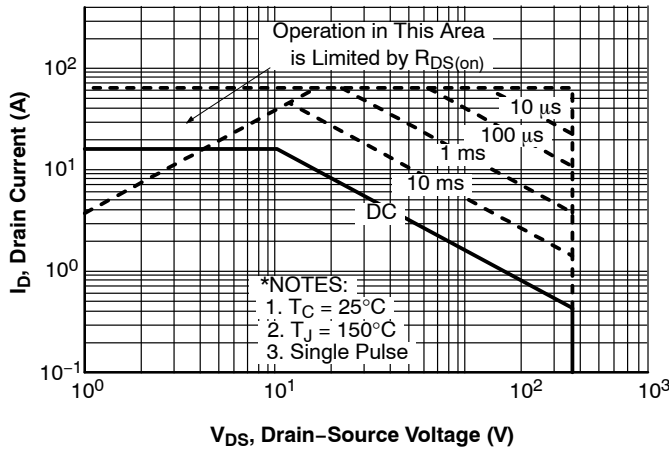


Figure 9. Maximum Safe Operating Area

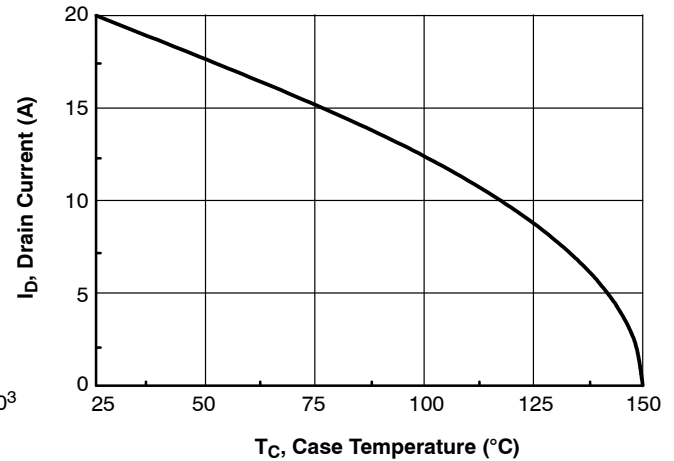


Figure 10. Maximum Drain Current vs. Case Temperature

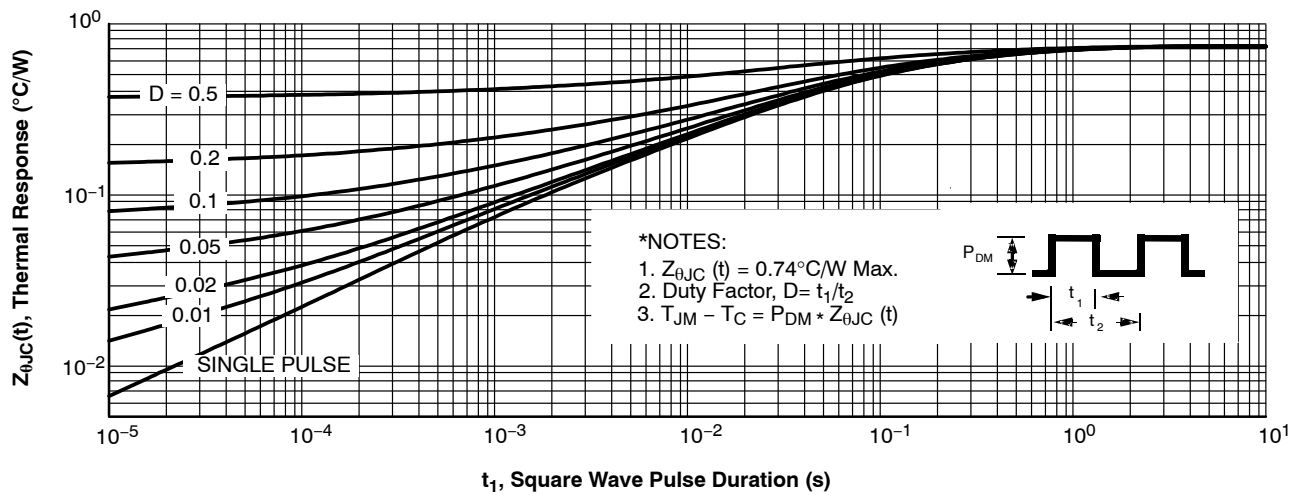


Figure 11. Transient Thermal Response Curve

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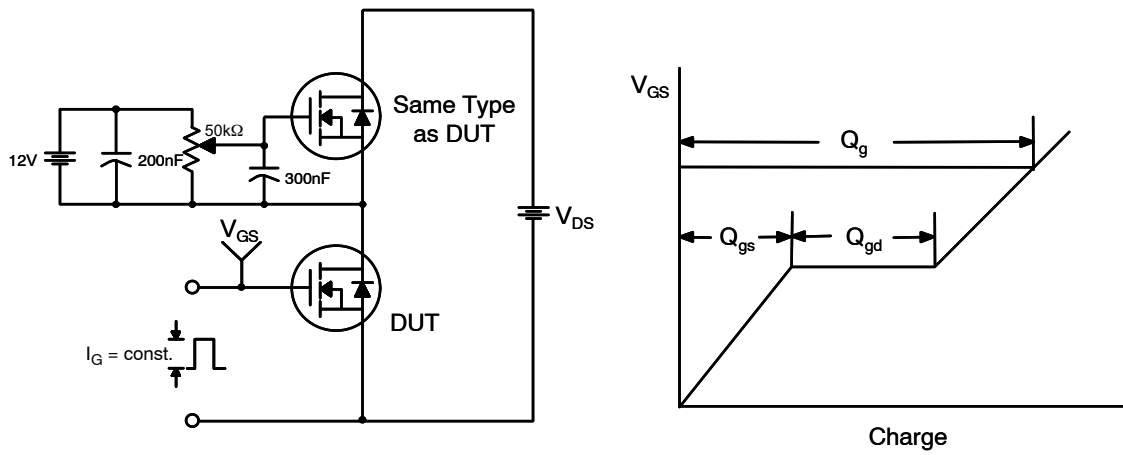


Figure 12. Gate Charge Test Circuit & Waveform

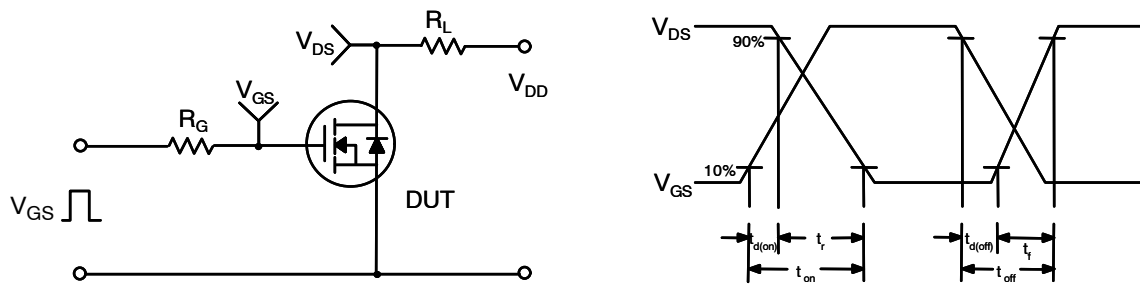


Figure 13. Resistive Switching Test Circuit & Waveforms

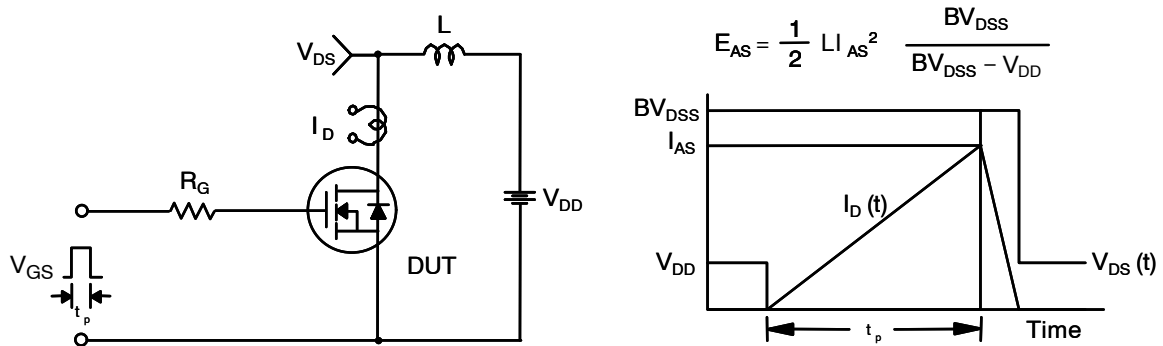


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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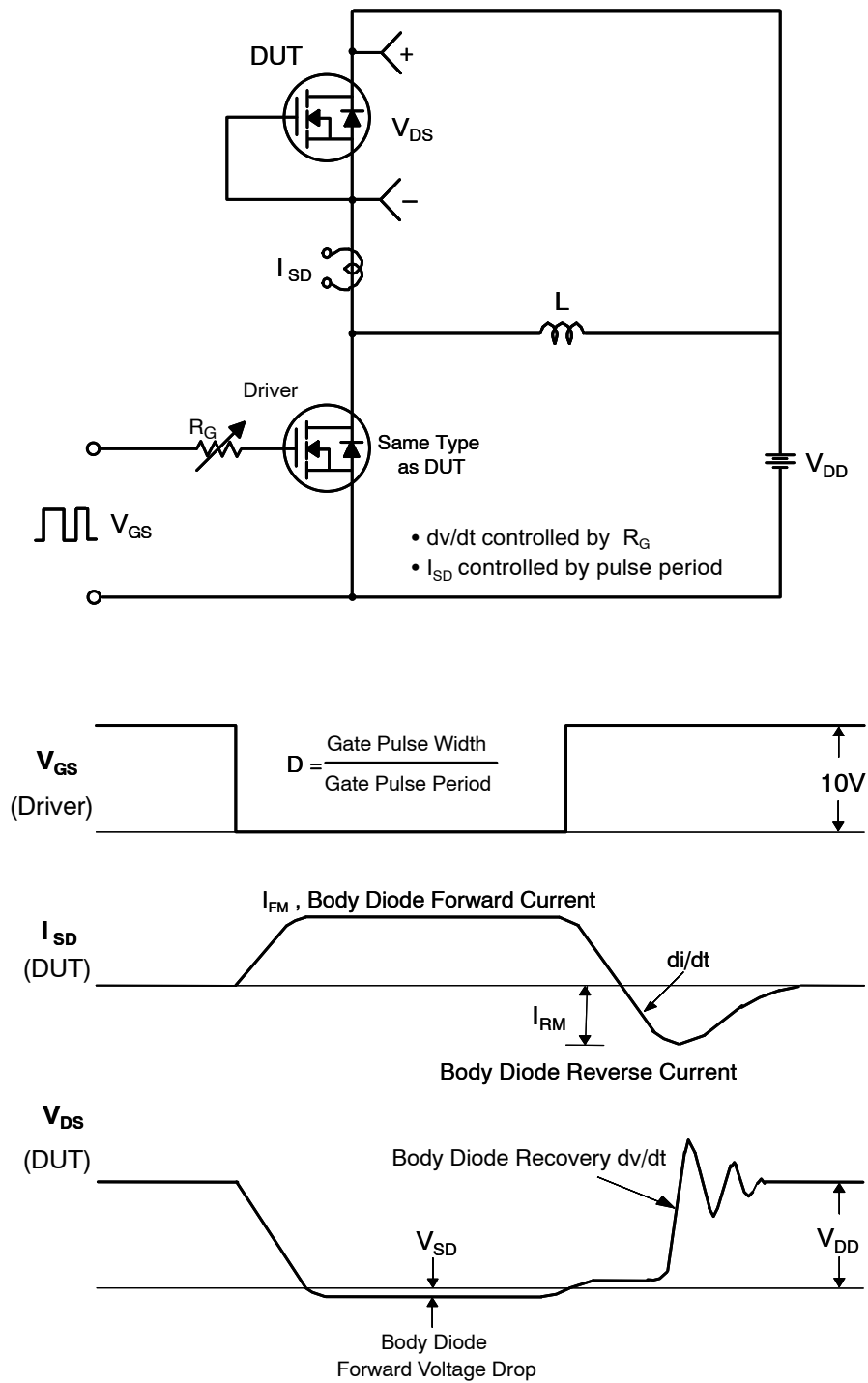
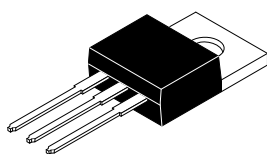


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

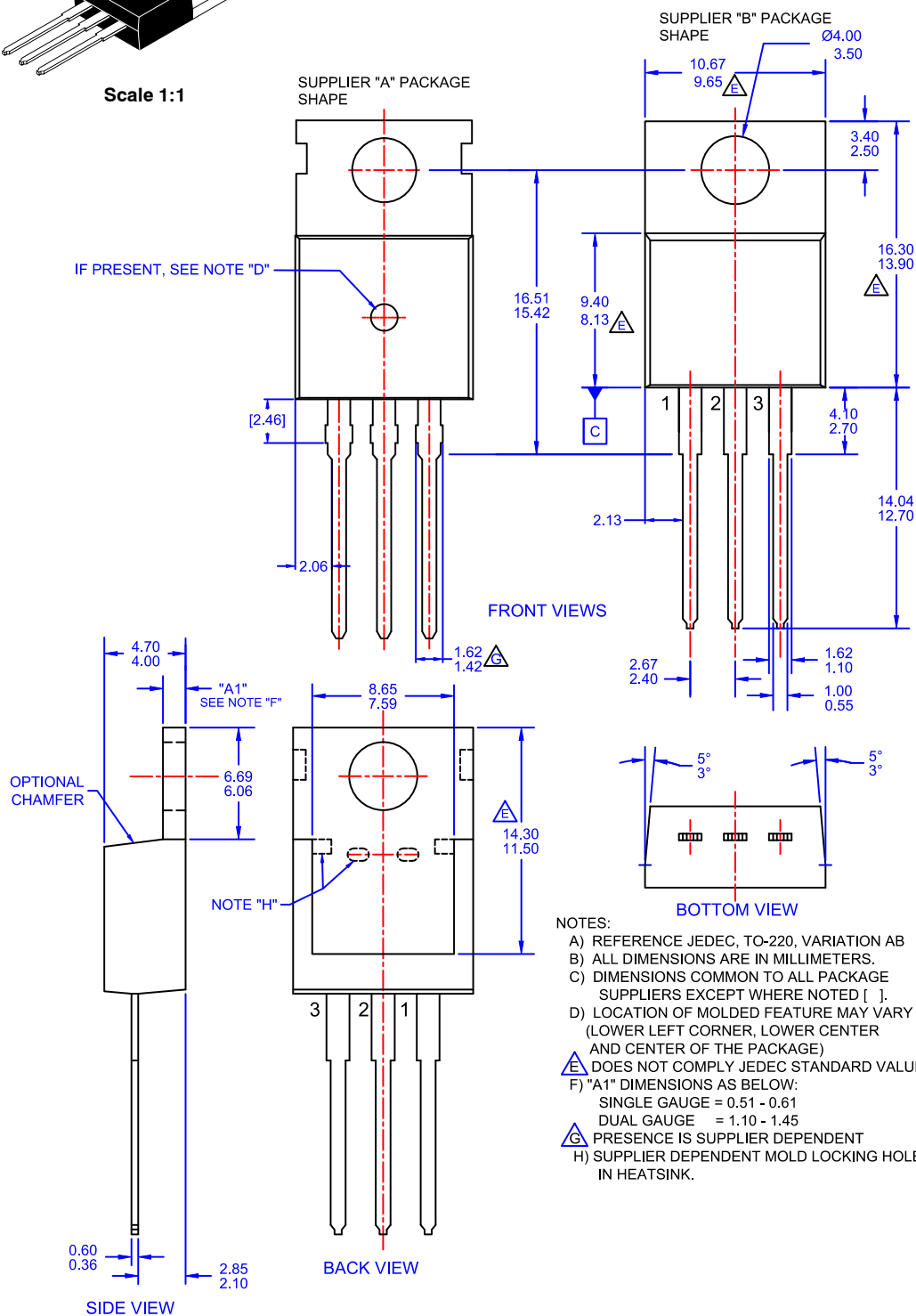
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Scale 1:1

## TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



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