Look-ahead carry Adders, Sub-CO, Unit-2

⇒ It provides fastest Addition Logic and Speed-up addition Process.
⇒ By using "Carry look-ahead Adder" Propagation delay time is reduced.
⇒ Consider Block diagram of a full-adder and its AND-OR-XOR realization by using 2 Half Adders in figure (a) and figure (b) given below

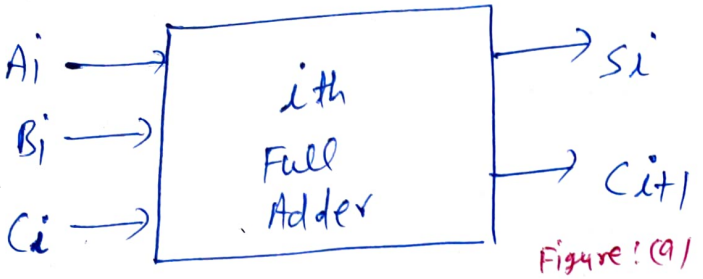

Figure: (a)

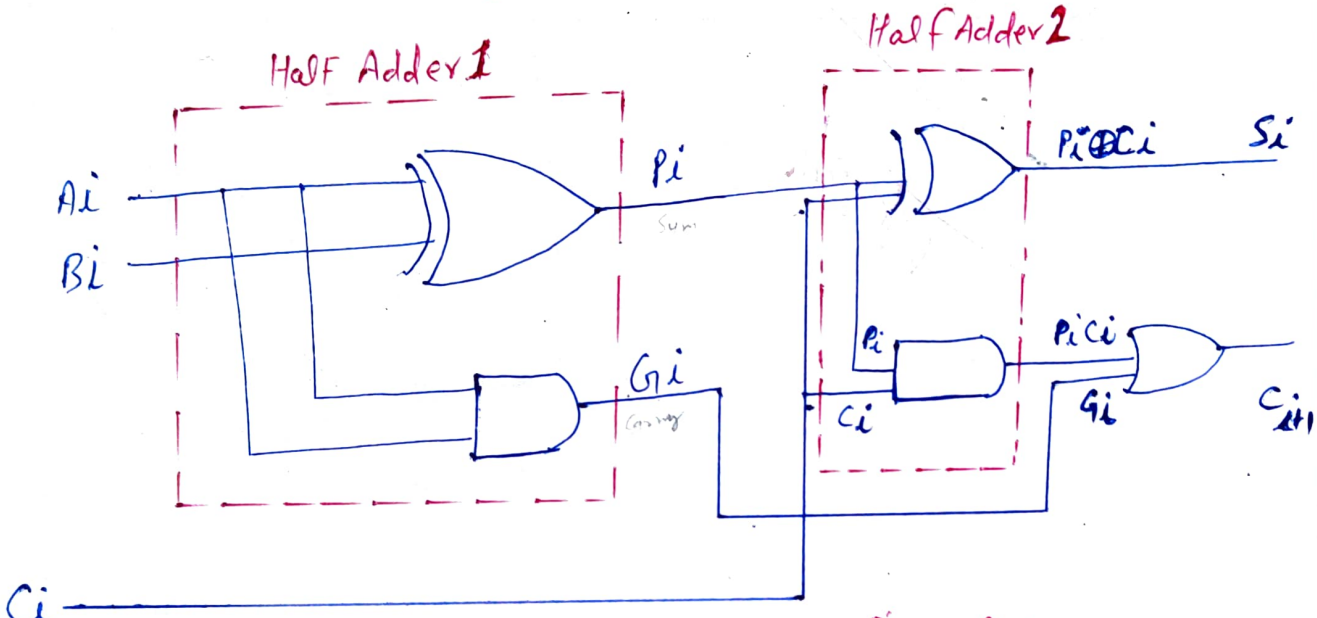

Figure: (b)

From Figure (b):

$$P_i = A_i \oplus B_i \quad \text{--- eq(1)}$$

$$G_i = A_i B_i \quad \text{--- eq(2)}$$

Variable P_i is known as Carry Propagate.
Variable G_i is known as Carry Generate.
Variable C_i is known as Carry output.

$$S_i = P_i \oplus C_i \quad \text{--- eq(3)}$$

$$\boxed{C_{i+1} = G_i + P_i C_i} \quad \text{--- eq(4)}$$

⇒ Time complexity of n-bit Parallel Adder is O(n).
⇒ But the time complexity of Look-ahead Carry adders is O(log n) which is very less.

⇒ The carry output Boolean function of each stage in a 4 stage carry look ahead adder can be expressed by putting $i = 0$; in eq (4):

$$C_1 = G_0 + P_0 C_0 \quad \text{--- eq (5)}$$

$i = 1$; in eq (4):

$$C_2 = G_1 + P_1 C_1$$

$$C_2 = G_1 + P_1 (G_0 + P_0 C_0)$$ By putting the value of C_1 from eq (5)

$$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0 \quad \text{--- eq (6)}$$

$i = 2$; in eq (4):

$$C_3 = G_2 + P_2 C_2$$

$$C_3 = G_2 + P_2 (G_1 + P_1 G_0 + P_1 P_0 C_0) \quad \text{- from eq (6)}$$

$$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \quad \text{--- eq (7)}$$

$i = 3$; in eq (4):

$$C_4 = G_3 + P_3 C_3$$

$$C_4 = G_3 + P_3 (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0) \quad \text{from eq (7)}$$

$$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0 \quad \text{--- eq (8)}$$

Page-2

* From eq no. (8) we observe that C_4 does not have to wait for C_3, C_2 and C_1 to propagate but actually C_4 is propagated at the same as C_3, C_2 and C_1. C_4 does not depend on C_3, C_2 & C_1 and depends on C_0 only as shown in eq (8)
* From eq no. (4), (5), (6), (7) and 8 we observe that Boolean expression for each carry output is the sum of products, so these can be implemented with one level of AND gates followed by a OR gate. They are in SOP forms.

* The figure given below show the implementation of C_4, C_3, C_2 and C_1 for a 4bit carry look-ahead Adder:-

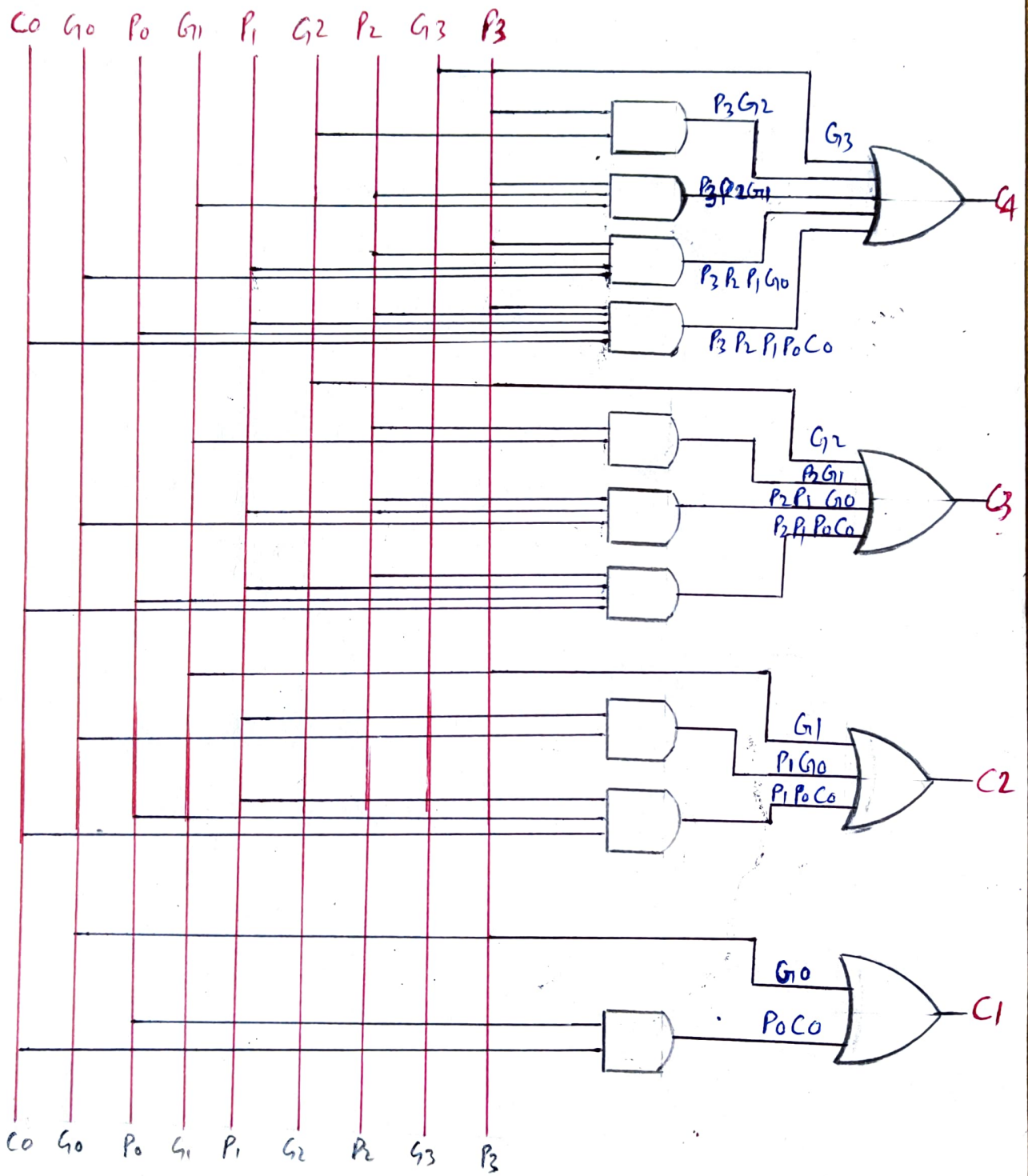

Figure - Circuit Diagram OR Logic Diagram of Look-ahead carry adder

Disadvantages of Look-ahead carry Adder:-

(1) The carry look-ahead Adder circuit becomes complicated as the no. of variables are increased.

(2) The circuit is costly as compared to other types of Adders.

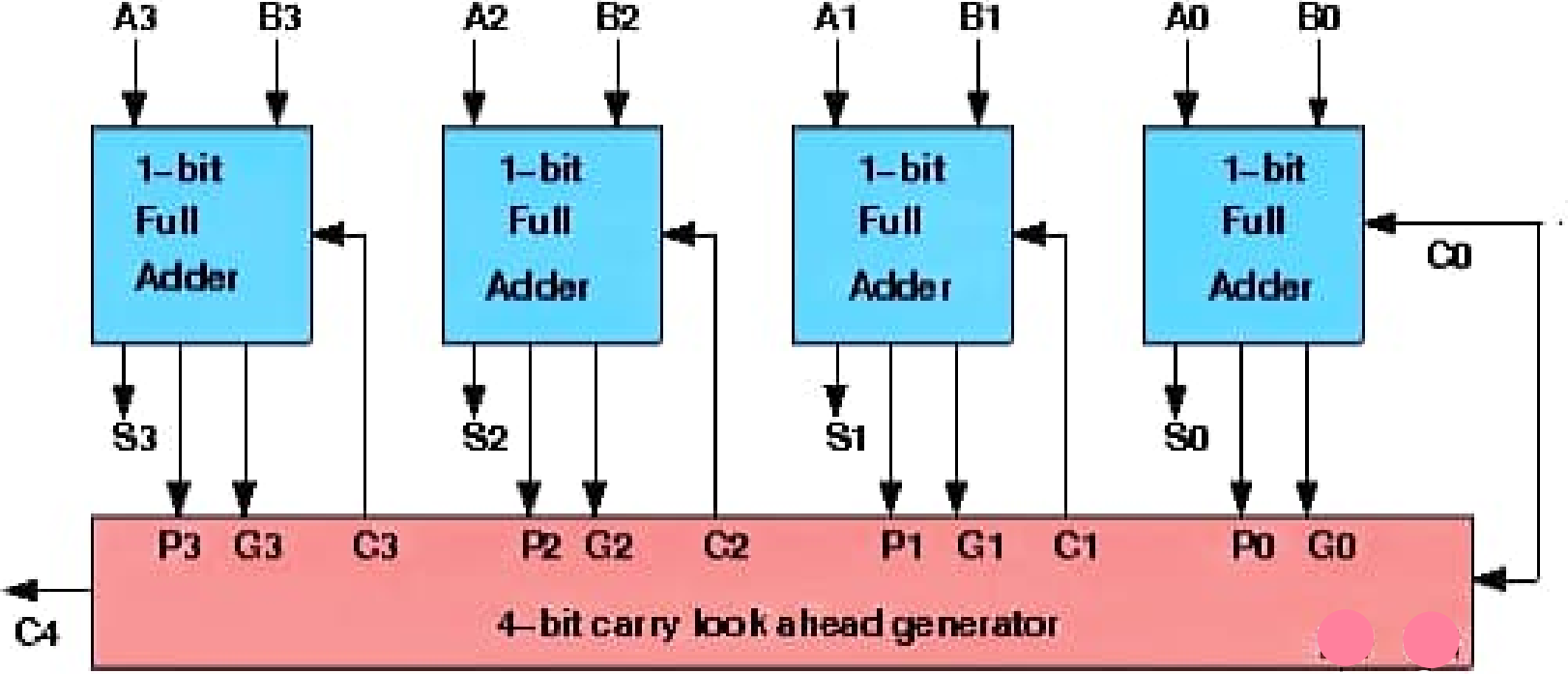

Figure: Block-diagram of "4-bit Look-ahead Carry Adder"