COURSE PACK

SCHEME

The scheme is an overview of work-integrated learning opportunities and gets students out into the real world. This will give what a course entails.

<table>
<tr><td>Course Title</td><td colspan="3">Computer Organization and Architecture</td><td colspan="5">Course Type</td><td colspan="2">Theory</td></tr>
<tr><td>Course Code</td><td colspan="3">E2UC505T</td><td colspan="5">Class</td><td colspan="2">5th Semester B.Tech. Core and All specialization</td></tr>
<tr><td rowspan="6">Instruction delivery</td><td>Activity</td><td>Credits</td><td>Credit Hours</td><td colspan="4" rowspan="2">Total Number of Classes per Semester</td><td colspan="2" rowspan="2">Assessment in Weightage</td></tr>
<tr><td>Lecture</td><td>3</td><td>3</td></tr>
<tr><td>Tutorial</td><td>1</td><td>1</td><td rowspan="3">Theory</td><td rowspan="3">Tutorial</td><td rowspan="3">Practical</td><td rowspan="3">Self-Learning</td><td rowspan="3">CIE</td><td rowspan="3">SEE</td></tr>
<tr><td>Practical</td><td>0</td><td>0</td></tr>
<tr><td>Self-Learning</td><td>0</td><td>6</td></tr>
<tr><td>Total</td><td>4</td><td>10</td><td>45</td><td>15</td><td>0</td><td>90</td><td>50%</td><td>50%</td></tr>
<tr><td rowspan="3">Names of Course Lead, Course</td><td colspan="2">Course Lead:

Course Coordinator</td><td colspan="7">Dr. Brijesh Kumar Singh

Shweta</td></tr>
<tr><td colspan="4">Theory</td><td></td><td colspan="4">Practical</td></tr>
</table>

Coordinators and Instructors	• Aanchal Vij • Aditi Chowdhary • Ashish Kumar Srivastava • Ashish Sharma • Himanshu Sharma • Isha Chopra • John A. • Maneesh Upadhya • Namrata Kumari • Rizwan Khan • Ruby Dahiya • Shweta • Sundara Kumar • Suveg Moudgil • Tarun Maini • Zatin Gupta		NA

COURSE OVERVIEW

Computer Organization and Architecture:

Computer organization and architecture play a pivotal role in the education of computer science students. Understanding the inner workings of a computer system is a practical necessity. This knowledge empowers students to write efficient code, troubleshoot hardware-related issues, design algorithms that harness the full potential of the underlying hardware and also adapt to emerging technologies and innovations.

PREREQUISITE COURSE

PREREQUISITE COURSE REQUIRED	YES	

If, yes please fill in the details

Prerequisite course code	**Prerequisite course name**
G2UC101B	Introduction to Digital System

COURSE OBJECTIVES

This course aims to familiarize students with design principles of computer architectures, emphasizing micro-operations, micro-programmed control units, and the memory and I/O structure of a typical computer system. students will also be exposed to performance analysis and assembly language programming.

COURSE OUTCOMES(COs)

After the completion of the course, the student will be able to

E2UC505T.1	Describe the functions of computer components viz CPU, memory, IO devices and storage systems.
E2UC505T.2	Design bus system for simple computer.
E2UC505T.3	Apply various algorithms for basic arithmetic operations on binary numbers.
E2UC505T.4	Design various types of memory for given specific constraints.
E2UC505T.5	Develop assembly language programs for essential operations using instruction sets of microprocessor 8085.
E2UC505T.6	Design of digital computer for simple specific application.

BLOOM'S LEVEL OF THE COURSE OUTCOMES

Bloom's taxonomy is a set of hierarchical models used for the classification of educational learning objectives into levels of complexity and specificity. The learning domains are cognitive, affective, and psychomotor**.**

Theory

CO No.	Remember **BTL1**	Understand **BTL2**	Apply **BTL3**	Analyse **BTL4**	Evaluate **BTL5**	Create **BTL6**
E2UC505T.1		√				
E2UC505T.2			√			√
E2UC505T.3			√			
E2UC505T.4			**√**			√
E2UC505T.5			√			
E2UC505T.6			√			√

PROGRAM OUTCOMES (POs):

PO1 Computing Science knowledge: Apply the knowledge of mathematics, statistics, computing science and information science fundamentals to the solution of complex computer application problems.

PO2 Problem analysis: Identify, formulate, review research literature, and analyze complex computing science problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and computer sciences**.**

PO3 Design/development of solutions: Design solutions for complex computing problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern computing science and IT tools including prediction and modeling to complex computing activities with an understanding of the limitations.

PO6 IT specialist and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional computing science and information science practice.

PO7 Environment and sustainability: Understand the impact of the professional computing science solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the computing science practice.

PO9 Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 Communication: Communicate effectively on complex engineering activities with the IT analyst community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 Project management and finance: Demonstrate knowledge and understanding of the computing science and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSO's)

PSO1: Have the ability to work with emerging technologies in computing requisite to Industry 4.0.

PSO2: Demonstrate Engineering Practice learned through industry internship and research project to solve live problems in various domains.

COURSE ARTICULATIONMATRIX

The Course articulation matrix indicates the correlation between Course Outcomes and Program Outcomes and their expected strength of mapping in three levels (low, medium, and high).

COs/Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
E2UC505T.1	2	-	-	-	-	-	-	-	-	-		1	-	-
E2UC505T.2	2	2	1	-	-	-	-	-	-	-	-	1	-	-
E2UC505T.3	2	-	-	-	-	-	-	-	-	-	-	1	-	-
E2UC505T.4	2	2	1	-	-	-	-	-	-	-	-	1	-	-
E2UC505T.5	2	2	1	-	-	-	-	-	-	-	-	1	-	-
E2UC505T.6	2	2	1	-	-	-	-	-	-	-	-	1	-	-

Mapping: 1-Low, 2-Medium

COURSE ASSESSMENT

The course assessment patterns are the assessment tools used both in formative and summative examinations.

Type of Course (T)	CIE			Total Marks		Final Marks CIE*0.5+SEE*0.5
	IA1#	MTE	IA2#	CIE	SEE	
THEORY	25	50	25	100	100	100

* Assignment, Quiz, Class teste

COURSE CONTENT

THEORY

Content
Introduction: Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration. Register, bus and memory transfer, Processor organization, general registers organization, stack organization and addressing modes. **Arithmetic and logic unit:** Look ahead carries adders, Fixed point representations and Arithmetic Operations: Addition and Subtraction, Multiplication: Signed operand multiplication, Booth's algorithm and array multiplier. Division and logic operations. **Control Unit:** Instruction types, formats, instruction cycles and sub cycles (fetch and execute etc), micro-operations, execution of a complete instruction. Program Control, Reduced Instruction Set Computer, Pipelining, Parallel Processing, Hardwired and Microprogrammed control unit. **Input / Output:** Peripheral devices, I/O interface, I/O ports, Interrupts: interrupt hardware, types of interrupts and exceptions. Modes of Data Transfer: Programmed I/O, interrupt initiated I/O and Direct Memory Access., I/O channels and processors. Serial Communication: Synchronous & asynchronous communication. **Memory:** Basic concept and hierarchy, semiconductor RAM memories, 2D & 2 1/2D memory organization. ROM memories. Cache memories: concept and design issues & performance, address mapping and replacement Auxiliary memories: magnetic disk, magnetic tape and optical disks Virtual memory: concept implementation **Introduction to 8085 Assembly Language**

LESSON PLAN FOR THEORY COURSES (11 weeks * 4 Hours = 42 Classes+3 Classes=45 Classes)

L. No	T/L	Topics	Skills	Competency
1	L	**INTRODUCTION:** Functional units of digital system and their interconnections	1. Design fundamental components of a computer system. 2. Design common bus system for data transfer in a digital computer	CO1, CO2
2	L	Buses, bus architecture		
3	L	Types of buses and bus arbitration		
4	L	Register, Bus and Memory Transfer		
5	L	Processor Organization		
6	L	General Registers Organization		
7	L	Stack Organization		
8	L	Addressing Modes.		

9	L	**Arithmetic and logic unit:** Look ahead carries adders	1. Develop algorithms for binary addition and subtraction of signed numbers signed numbers 2. Develop algorithms for multiplication of signed numbers 3. Develop algorithms for division of signed numbers	CO3
10	L	Addition and Subtraction		
11	L	Multiplication: Signed operand multiplication,		
12	L	Booth's algorithm.		
13	L	array multiplier.		
14	L	Division and logic operations.		
15	L	Restoring Division Algorithm		
16	L	Non-Restoring Division Algorithm		
17	L	**Control Unit:** Instruction types, formats	1. Design the hardwired control unit, 2. Analyse the performance of various parallel processing mechanism 3. Analyse different types of control unit and their hardware requirements	CO6
18	L	Instruction cycles and sub cycles (fetch and execute etc)		
19	L	Micro-operations, execution of a complete instruction.		
20	L	Reduced Instruction Set Computer		
21	L	Parallel Processing		
22	L	Pipelining		
23	L	Hardwired & Microprogrammed control unit.		
24	L	**Input / Output:** Peripheral devices, I/O interface, I/O ports	1. Apply various inter-communication mechanism between peripheral devices and processor. 2. Design the interrupts handling hardware for the I/O and processor communication	CO1
25	L	Interrupts: interrupt hardware		
26	L	types of interrupts and exceptions		
27	L	Modes of Data Transfer: Programmed I/O		
28	L	Interrupt initiated I/O		
29	L	Direct Memory Access		
30	L	I/O channels and processors		
31	L	Serial Communication: Synchronous & asynchronous communication		

32	L	**Memory and Assembly Language Programming:** Basic concept and hierarchy, semiconductor RAM memories,	1. Analyse the design issues and performance of various types of memory available in memory hierarchy 2. Developing basic assembly language programs.	CO4, CO5
33	L	2D & 2 1/2D memory organization		
34	L	ROM memories. Cache memories: concept and design issues & performance,		
35	L	Address mapping-Direct Addressing		
36	L	Address mapping- Associative		
37	L	Address mapping – Set Associative		
38	L	Auxiliary memories: magnetic disk, magnetic tape and optical disks		
39	L	Virtual memory: concept implementation, Page Replacement Policies		
40	L	Instruction set of 8085 microprocessor		
41	L	To add two 8 bit numbers resulting in 8 bit sum.		
42	L	To add two 8 bit numbers resulting in 16 bit sum.		.
43	L	To subtract two 8 bit numbers		
44	L	To multiply two 8 bit numbers		
45	L	To find the largest number among various data		

BIBLIOGRAPHY

Text Book

1. Computer System Architecture - M. Mano

Reference Books:

1. Hayes, John P. Computer architecture and organization. McGraw-Hill, Inc., 2002. (https://eresources.nlb.gov.sg/printheritage/detail/113de262-0f99-43a3-a14d-fa67771619f6.aspx)
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky Computer Organization, McGraw-Hill, Fifth Edition, Reprint 2012
3. William Stallings, Computer Organization and Architecture-Designing for Performance, Pearson Education, Seventh edition, 2006
4. Heuring, Vincent P., Harry Frederick Jordan, and Miles Murdocca. Computer systems design and architecture. Addison-Wesley, 1997. (https://dl.acm.org/doi/book/10.5555/996242)
5. Kai Hwang & Naresh Jotwani - Advanced Computer Architecture: Parallelism, Scalability, Programmability, Tata McGraw Hill,2003 (https://www.expresslibrary.mheducation.com/product/advanced-computer-architecture-parallelism-scalability-programmability)

SWAYAM/NPTEL/MOOCs Certification

1. https://www.coursera.org/learn/comparch
2. https://nptel.ac.in/courses/106105163
3. https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/

Practice Problems

1.

Show the block diagram of the hardware (similar to Fig. 4-2a) that implements the following register transfer statement:

$$yT_2: \quad R2 \leftarrow R1, \quad R1 \leftarrow R2$$

2.

The outputs of four registers, $R0$, $R1$, $R2$, and $R3$, are connected through 4-to-1-line multiplexers to the inputs of a fifth register, $R5$. Each register is eight bits long. The required transfers are dictated by four timing variables T_0 through T_3 as follows:

$$\begin{aligned} T_0&: \quad R5 \leftarrow R0 \\ T_1&: \quad R5 \leftarrow R1 \\ T_2&: \quad R5 \leftarrow R2 \\ T_3&: \quad R5 \leftarrow R3 \end{aligned}$$

The timing variables are mutually exclusive, which means that only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and to the load input of register $R5$.

3.

Represent the following conditional control statement by two register transfer statements with control functions.

$$\text{If } (P = 1) \text{ then } (R1 \leftarrow R2) \text{ else if } (Q = 1) \text{ then } (R1 \leftarrow R3)$$

4.

What has to be done to the bus system of Fig. 4-3 to be able to transfer information from any register to any other register? Specifically, show the connections that must be included to provide a path from the outputs of register C to the inputs of register A.

5.

Draw a diagram of a bus system similar to the one shown in Fig. 4-3, but use three-state buffers and a decoder instead of the multiplexers.

6.

A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

a. How many selection inputs are there in each multiplexer?
b. What size of multiplexers are needed?
c. How many multiplexers are there in the bus?

7.

The following transfer statements specify a memory. Explain the memory operation in each case.

a. $R2 \leftarrow M[AR]$
b. $M[AR] \leftarrow R3$
c. $R5 \leftarrow M[R5]$

8.

Draw the block diagram for the hardware that implements the following statements:

$$x + yz: \quad AR \leftarrow AR + BR$$

where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function. (Remember that the symbol + designates an OR operation in a control or Boolean function but that it represents an arithmetic plus in a microoperation.)

9

Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input.

$$xyT_0 + T_1 + y'T_2: \quad AR \leftarrow AR + 1$$

10. Represent 25 H, 42 H and 2000 H into binary numbers.

11. What is difference between following two instructions?
MOV BL, 25 H and MOV BL, [25 H]
In above instruction, BL is register available inside processor.

12. In following assembly language program, identify that which type of addressing mode has been used in each of the instructions.

MOV BL, [2000 H]
MOV CL, [3000 H]
ADD BL, CL
ADD BL, 55H
MOV [4000], BL

Here, BL and CL are registers available inside processor.

13. The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?

    (a) 2K x 16; (b) 64K x 8; (c) 16M x 32; (d) 4G X 64.

14. How many 128 x 8 memory chips are needed to provide a memory capacity of 4096 x 16?

15. Show the value of all bits of a 12-bit register that hold the number equivalent to decimal 215 in (a) binary; (b) binary-coded octal; (c) binary-coded hexadecimal; (d) binary-coded decimal (BCD).

16. Perform the arithmetic operations (+42) + (- 13) and (-42) - (- 13) in binary using signed-2's complement representation for negative numbers.

17. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

    a. How many selection inputs are there in each multiplexer?

    b. What size of multiplexers are needed?

    c. How many multiplexers are there in the bus?

18. The 8-bit registers AR, BR, CR and DR initially have the following values:

    AR= 11110010, BR= 11111111, CR=10111001 and DR=11101010. Determine the 8-bit values in each register after execution of the following sequence of micro operations.

$$AR \leftarrow AR + BR$$

$$CR \leftarrow CR \wedge DR, \quad BR \leftarrow BR + 1$$

$$AR \leftarrow AR - CR$$

19. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word in memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

a. How many bits are there in the operation code, the register code part, and the address part?

b. Draw the instruction word format and indicate the number of bits in each part.

c. How many bits are there in the data and address inputs of the memory?

20. The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. (001 = ADD)

    a. What is the instruction that will be fetched and executed next?

    b. Show the binary operation that will be performed in the AC when the instruction is executed.

    c. Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the values of E, I, and the sequence counter SC in binary at the end of the instruction cycle.

21. A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.

22. The following program is stored in the memory unit of the basic computer. Show contents of the AC and PC, at the end, after each instruction is executed. All numbers listed below are in hexadecimal.

10	CLA	
011	ADD	016
012	BUN	014
013	HLT	
014	AND	017
015	BUN	013
016	C1A5	
017	93C6	

23. Write a program to evaluate the arithmetic statement:

$$X = (A + B) * (C + D)$$

a) Using a general register computer with three-address instructions.
b) Using a general register computer with two-address instructions.
c) Using a single-accumulator computer with one-address instructions.
d) Using a stack organized computer with zero-address operation

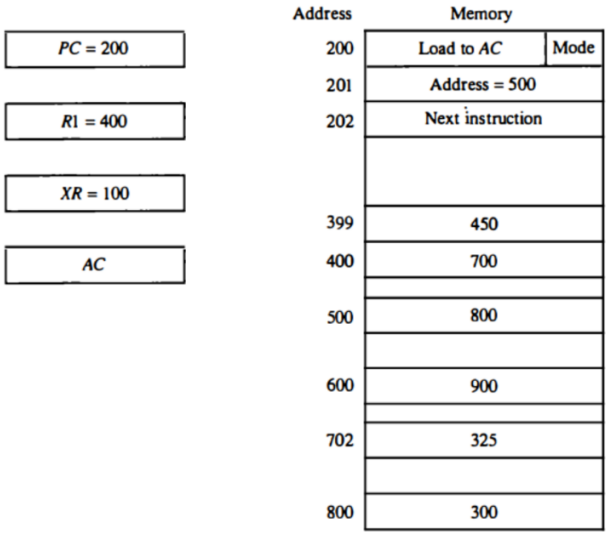
24. Explain the difference between hardwired control and microprogramed control. Is it possible to have a hardwired control associated with a control memory?

25. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the in instruction is in one memory word.

26. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R 1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register.

27 Give five examples of external interrupts and five examples of internal interrupts. What is the difference between a software interrupt and a subroutine call?

28. The two-word instruction at address 200 and 201 is a "load to AC" instruction with an address field equal to 500. The first word of the instruction specifies the operation code and mode, and the second word specifies the address part. PC has the value 200 for fetching this instruction. The content of processor register R 1 is 400, and the content of an index register XR is 100. AC receives the operand after the instruction is executed. The figure lists a few pertinent addresses and shows the memory content at each of these addresses. Calculate the effective address and the operand that must be loaded into AC for (a) Direct, (b) Immediate, (c) Indirect, (d) Relative, (e) Indexed (f) Register (g) Register Indirect (h) Autoincrement, (i) Autodecrement addressing mode.



29. In certain scientific computations it is necessary to perform the arithmetic operation (Ai + Bi) (Ci + Di) with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i = 1 through 6.

30. Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

31. Determine the number of dock cycles that it takes to process 200 tasks in a six-segment pipeline.

32. A no pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

33. A weather forecasting computation requires 250 billion floating-point operations. The problem is processed in supercomputer that can perform 100 megaflops. How long will it take to do these calculations?

34. Perform the arithmetic operations below with binary numbers and with negative number in signed-2"s complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position.

    (a) (+35) + (+40)

    (b) (-35) + (- 40)

35. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers, the multiples and in both cases is + 15.

    (a) (+15) X (+13)

    (b) (+15) X (-13)

36. Explain the difference between the daisy chaining priority and parallel priority interrupts. Draw the diagrams to explain their working.

37. A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. Draw the instruction word format and indicate the number of bits in each part.

38. A computer uses RAM chips of 1024x1 capacity.

(i) How many chips are needed to provide a memory capacity of 1024 bytes?

(ii) How many chips are needed to provide a memory capacity of 16K bytes?

39. How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits).

a. Synchronous serial transmission.

b. Asynchronous serial transmission with two stop bits.

c. Asynchronous serial transmission with one stop bit.

40. a. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

b. How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

c. How many lines must be decoded for chip select? Specify the size of the decoder.

41. The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words in each. Physical memory consists of 4K block of 4K words in each. Formulate the logical and physical address formats.

42. Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bits addresses. Calculate the number of bits needed for cache indexing and the number of tag bits are respectively.

Course Lead Program Chair Dean