# Practice Question Bank- 2

**Course: B.Tech. III Semester** **Course Name: Computer Organization and Architecture**

**Topics Covered**
**Arithmetic and logic unit:** Look ahead carries adders, Fixed point representations and Arithmetic Operations: Addition and Subtraction, Multiplication: Signed operand multiplication, Booth's algorithm and array multiplier. Division and logic operations
**Processor Organization:** General Register Organization, Stack Organization, and Addressing Modes.

## Short Questions

1. Convert the following numerical arithmetic expressions into reverse polish notation and show the stack operations for evaluating the numerical result.

   (5+3) [6 (5+4)/7]

2. Illustrate the influence of number of addresses on T=(R+S) (U+ V) using three addresses, two addresses and zero address instruction.
3. Giving suitable block diagram show major components of CPU.
4. Mark each individual path in the flowchart of addition and subtraction algorithm by a number and then indicate the overall path that the algorithm takes when the following signed-magnitude numbers are computed. In each case gives the value of AVF. The leftmost bit in the following numbers represents the sign bit.

   a. 0 101101 + 0 011111

   b. 1 011111 + 1 101101

   c. 0 101101 – 0 011111

   d. 0 101101- 0 101101

   e. 1 011111- 0 101101

5. What is the reverse polish notation? Explain with an example.
6. Write down a program to evaluate Z = (A + B) * (C + D) * (G + H) by using three address instructions and zero address instructions.
7. Show the contents in hexadecimal of registers PC, AR, DR, IR and SC of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of PC is 80F. The content of memory at address 80F is EB3F. The content of memory at address B3F is 0B96. The content of memory at address B96 is FFFF.
8. Convert the following arithmetic expressions from infix to reverse Polish notation:
   A + B * [C / D + E * ( F - G)]

9. The content of PC in the basic computer is 2BA. The content of AC is 8F24. The content of memory at address 2BA is 92FE. The content of memory at address 2FE is 08A1. The content of memory at address 8A1 is 10B2. What is the instruction that will be fetched and executed? What will be the value of PC, AC, DR, IR, and SC after the execution of the instruction?
10. Describe the algorithm for division of two fixed-point binary numbers in signed-magnitude representation.

**Long Questions**

11. What is the significance of addressing mode? Discuss different types of addressing modes.
12. Explain basic instruction format based on the type reference made by the instruction?
13. Perform the arithmetic operations below with binary numbers and with negative numbers in signed 2's Complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position.
    a. (-35) + (-40)
    b. (-35) - (+40)
14. Show the contents of registers E, A, Q and SC during the process of division of 00001111 by 0011. (use a dividend of eight bits)
15. Write a program to evaluate the arithmetic statement:
    Z = P - Q + R * (S - T) / (U*V)
    (i) Using a single accumulator organized computer with one-address instructions.
    (ii) Using a stack organized computer with zero-address operations
    (iii) Using a general register computer with two-address instructions.
    (iv) Using a general register computer with three-address instructions.