Practice Question Bank- 1

Course: B.Tech. III Semester **Course Name: Computer Organization and Architecture**

Topics Covered

Register Transfer and Micro-operations: Register Transfer Language, Register Transfer, Bus and Memory Transfers, Arithmetic Micro-operations, Logic Micro-operations, Shift Microoperations, Arithmetic logic shift unit
Basic Computer Organizations and Design: Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory - Reference Instructions, Register - Reference Instructions, Input - Output Instructions

Objective type's Question

1. The …… &……. instruction needed in the basic computer in order to set the E flip flop to 1.
2. ……is concerned with the way the hardware component operates and the way they are connected together to form the computer system.
3. The third state in a tri state buffer is ……
4. In a basic computer the type of instruction are _____, _____and _____.
5. In memory reference instruction, the operation bits specify from _____to _____.
6. The devices that provide the means for a computer to communicate with the user or other computers are referred to as:

   (a) CPU (b) ALU

   (c) I/O (d) one of the above

7. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

   (a) 0000 (b) 0010

   (c) 1000 (d) 1111

8. Function of Program Counter

   (a) Holds the address of instruction (b) Holds the address of memory

   (b) Holds the instruction code (c) none of the above.

9. Which of the computer register holds the instruction code?

(a) AR (b) IR

(c) PC (d) DR

10. The symbolic description of transfer from one register to another register is known as _____.

Short Questions:

Q.1. What do you mean by register transfer language (RTL)?

Q.2. Draw a diagram of a bus system using three-state buffers a decoder.

Q.3. Explain P: R3← R5 statement.

Q.4. Draw the block diagram of control unit of basic computer and explain.

Q.5. Draw the block diagram for the hardware that implements the following statement: rT1+sT2T3: AC←AC-BR here AC and BR are two n-bit registers and r, T1. T2, and T3 are control variables.

Q.6. Design a 4-bit combinational circuit incrementer using four full adders.

Q.7. List various registers with their function required for basic computer function.

Q.8. Tabulate various shift micro-operation and design a 4 bit combination circuit shifter.

Q.9. Starting from an initial value of R=10001101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical Shift-right and a circular shift-left.

Q.10. A computer uses a memory unit with 4K words of 16 bits each. A binary instruction code is stored in one word of memory. The instruction has three parts: an indirect bit, an operation code, an address part. Draw the instruction word format and indicate the number of bits in each part.

Q.11. Describe the hardware implementation of logic micro-operation. Draw the diagram of one stage of logic circuit used with AND, OR, NAND and XOR gates.

Q.12. Draw a diagram of bus system for four registers with 8-bit each using three-state buffers and decoder

Q.13. Define Computer Instruction and list different type of instructions.

Q.14. Differentiate between hardwired control and microprogram control.

Q.15. Draw a timing diagram simpler to control timing signals assuming that SC is cleared to a 0 at a time t3 if control signal C7 active

C7t3: SC←0, C7 is activated with the positive clock transition associated with t1.

Long Questions:

Q.1. What are micro-operations? What are its various types? Illustrate the implementation of each category of micro-operations through its block diagram(s).

Q.2. What is a bus? Design a bus system capable of transmitting data from any register from a group or to registers (32-bits each) to any other register in a group of 8 registers (32-bits each). Illustrate the logic through its block diagram?

Q.3. Design an arithmetic circuit with one selection variable S and two n-bit date inputs A and B. The circuit generates the following four arithmetic operations in conjunction will the input carry Cin. Draw the logic diagram for the first two stages.

S	cin=0	cin=1
0	D=A+B	D=A+1
1	D=A-1	D=A+B'+1

Q.4. The output of four registers R0, R1, R2, R3 are connected through 4-to 1 line multiplexers to the inputs of a fifth register R5. Each register is eight bits long. The required transfers are dictated by four timing variables T0 through T3 as follows:

To: R5←R0

T1: R5←R1

T2: R5←R2

T3: R5←R3

Timing variables are mutually exclusive. Draw a block diagram showing the hardware implementation of the register transfers.

Q.5. What are the various phases of an instruction cycle? Give the micro-operations of fetch and decode phases. How the first two register transfer statements are Implemented?

Q.6. Tabulate various memory reference instruction. Explain BUN and BSA.

Q.7. Consider the instruction format of the basic computer for each of the following 16-bit instruction give the equivalent four digits hexadecimal code and explain that what an instruction going to perform.

a. 0001 0000 0010 0100
b. 1011 0001 0010 0100
c. 0111 1000 0000 0000
d. 0111 0000 1000 0000
e. 1111 1000 0000 0000