TEXAS INSTRUMENTS

OPA1641, OPA1642, OPA1644

SBOS484C –DECEMBER 2009–REVISED DECEMBER 2015

OPA164x Sound Plus High-Performance, JFET-Input Audio Operational Amplifiers

1 Features

- Superior Sound Quality
- True Jfet Input Operational Amplifier With Low Input Bias Current
- Low Noise: 5.1 nv/$\sqrt{Hz}$ at 1 kHz
- Ultralow Distortion: 0.00005% at 1 kHz
- High Slew Rate: 20 V/µs
- Unity Gain Stable
- No Phase Reversal
- Low Quiescent Current: 1.8 mA per Channel
- Rail-to-rail Output
- Wide Supply Range: ±2.25 V to ±18 V
- Single, Dual, and Quad Versions Available

2 Applications

- Professional Audio Equipment
- Analog and Digital Mixing Consoles
- Broadcast Studio Equipment
- High-end A/V Receivers
- High-end Blu-ray™ Players

3 Description

The OPA1641 (single), OPA1642 (dual), and OPA1644 (quad) series are JFET-input, ultralow distortion, low-noise operational amplifiers fully specified for audio applications.

The OPA1641, OPA1642, and OPA1644 rail-to-rail output swing allows increased headroom, making these devices ideal for use in any audio circuit. Features include 5.1-nV/$\sqrt{Hz}$ noise, low THD+N (0.00005%), a low input bias current of 2 pA, and low quiescent current of 1.8 mA per channel.

These devices operate over a very wide supply voltage range of ±2.25 V to ±18 V. The OPA1641, OPA1642, and OPA1644 series of operational amplifiers are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

The dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.
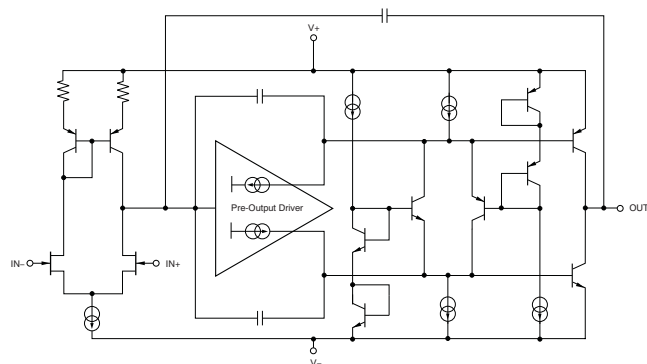
The OPA1641, OPA1642, and OPA1644 are specified from –40°C to +85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1641	SOIC (8)	4.90 mm × 3.90 mm
	MSOP (8)	3.00 mm × 3.00 mm
OPA1642	SOIC (8)	4.90 mm × 3.90 mm
	MSOP (8)	3.00 mm × 3.00 mm
OPA1644	SOIC (14)	8.65 mm × 3.90 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Internal Schematic
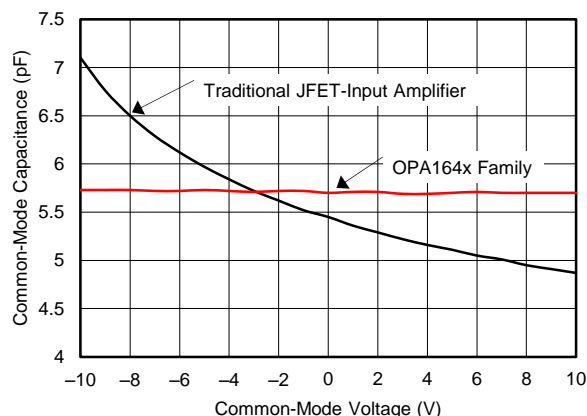

Extremely Stable Input Capacitance

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2010) to Revision C   **Page**

Changes from Revision A (April 2010) to Revision B   **Page**

Changes from Original (December 2009) to Revision A   **Page**

5 Pin Configuration and Functions

OPA1641: D and DGK Packages
8-Pin SOIC and MSOP
Top View
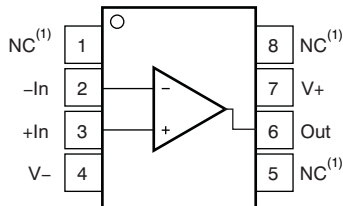
(1) NC denotes no internal connection.

Pin Functions: OPA1641

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	No connection
2	-IN	I	Inverting input
3	+IN	I	Noninverting input
4	V-	—	Negative (lowest) power supply
5	NC	—	No connection
6	OUT	O	Output
7	V+	—	Positive (highest) power supply
8	NC	—	No connection

OPA1642: D and DGK Packages
8-Pin SOIC and MSOP
Top View
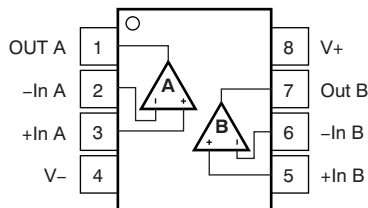
Pin Functions: OPA1642

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output, channel A
2	-IN A	I	Inverting input, channel A
3	+IN A	I	Noninverting input, channel A
4	V-	—	Negative (lowest) power supply
5	+IN B	I	Noninverting input, channel B
6	-IN B	I	Inverting input, channel B
7	OUT B	O	Output, channel B
8	V+	—	Positive (highest) power supply

OPA1644: D and PW Packages
14-Pin SOIC and TSSOP
Top View

Pin Functions: OPA1644

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output, channel A
2	-IN A	I	Inverting input, channel A
3	+IN A	I	Noninverting input, channel A
4	V+	—	Positive (highest) power supply
5	+IN B	I	Noninverting input, channel B
6	-IN B	I	Inverting input, channel B
7	OUT B	O	Output, channel B
8	OUT C	O	Output, channel C
9	-IN C	I	Inverting input, channel C
10	+IN C	I	Noninverting input, channel C
11	V-	—	Negative (lowest) power supply
12	+IN D	I	Noninverting input, channel D
13	-IN D	I	Inverting input, channel D
14	OUT D	O	Output, channel D

Product Folder Links: *OPA1641 OPA1642 OPA1644*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S	Supply voltage		40	V
V_{IN}	Input voltage[2]	(V-) – 0.5	(V+) + 0.5	V
I_{IN}	Input current[2]		±10	mA
$V_{IN(DIFF)}$	Differential input voltage		±VS	V
I_O	Output short-circuit[3]	Continuous		
T_A	Operating temperature	−55	125	°C
T_J	Junction temperature	−65	150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Short-circuit to VS/2 (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+, V-)	4.5 (±2.25)		36 (±18)	V
Specified temperature	−40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		OPA1641, OPA1642		OPA1644	OPA1644	UNIT
		D (SOIC)	DGK (MSOP)	D (SOIC)	DGK (MSOP)	
		8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	180	97	135	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	55	56	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	130	53	66	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9	n/a	19	n/a	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	120	46	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 0 3 V_{RMS}		0.00005%		
				−126		dB
IMD	Intermodulation distortion	G = +1, V_O = 3 V_{RMS}				
		SMPTE/DIN Two-Tone, 4:1 (60 Hz and 7k Hz)		0.00004%		
				−128		dB
		DIM 30 (3 kHz square wave and 15 kHz sine wave)		0.00008%		
				−122		dB
		CCIF Twin-Tone (19 kHz and 20 kHz)		0.00007%		
				−123		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1		11		MHz
SR	Slew rate	G = 1		20		V/µs
	Full-power bandwidth[1]	V_O = 1V_P		3.2		MHz
	Overload recovery time[2]	G = −10		600		ns
	Channel separation (dual and quad)	f = 1 kHz		−126		dB
NOISE						
	Input voltage noise	f = 20 Hz to 20 kHz		f = 10 Hz		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz		f = 100 Hz		nV/√Hz
		f = 100 Hz		f = 1 kHz		nV/√Hz
		f = 1 kHz		5.1		nV/√Hz
I_n	Input current noise density	f = 1 kHz		0.8		fA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±18 V		1	3.5	mV
PSRR	Vs power supply	V_S = ±2.25 V to ±18 V		0.14	2	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current		(V−)−0.1		(V+)−3.5	V
I_{OS}	Input offset current	V_{CM} = (V−) − 0.1 V to (V+) − 3.5 V, V_S = ±18 V	120	126		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V−)−0.1		(V+)−3.5	V
CMRR	Common-mode rejection ratio	V_{CM} = (V−) − 0.1 V to (V+) − 3.5V, V_S = ±18 V	120	126		dB
INPUT IMPEDANCE						
	Differential			10^{13} ‖ 8		Ω ‖ pF
	Common-mode	V_{CM} = (V−) − 0.1 V to (V+) − 3.5 V		10^{13} ‖ 6		Ω ‖ pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V−) + 0.2 V ≤ V_O ≤ (V+) − 0.2 V, R_L = 10 kΩ	120	134		dB
		(V−) + 0.35 V ≤ V_O ≤ (V+) − 0.35 V, R_L = 2 kΩ	114	126		dB

(1) Full power bandwidth = SR/(2π × V_P), where SR = slew rate.
(2) See Figure 19 and Figure 20.

Product Folder Links: *OPA1641 OPA1642 OPA1644*

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from rail	R_L = 2 kΩ, A_{OL} ≥ 114 dB	(V−)+0.2		(V+)−0.2	V
		R_L = 10 kΩ, A_{OL} ≥ 120 dB	(V−)+0.35		(V+)−0.35	V
I_{OUT}	Output current		See *Typical Characteristics*			
Z_O	Open-loop output impedance		See *Typical Characteristics*			
I_{SC}	Short-circuit current	Source				mA
		Sink				mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current (per amplifier)	I_{OUT} = 0 A		1.8	2.3	mA
TEMPERATURE RANGE						
Specified range			−40		85	°C
Operating range			−55		125	°C

6.6 Typical Characteristics

At T_A = 25°C, R_L = 2 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
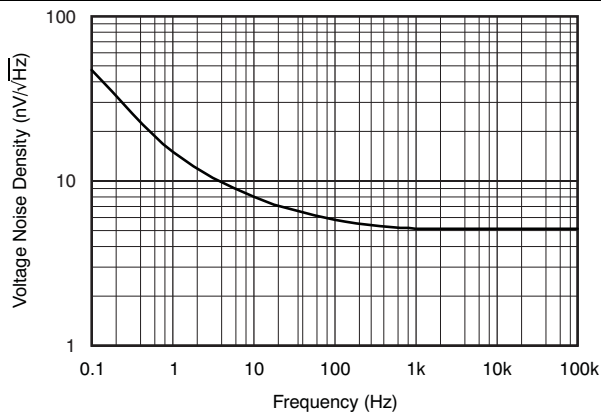

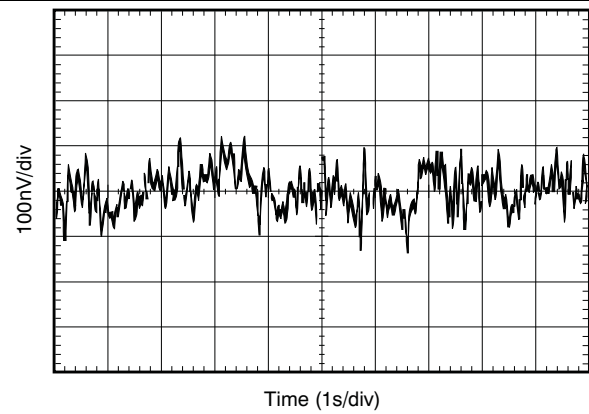Figure 1. Input Voltage Noise Density vs Frequency
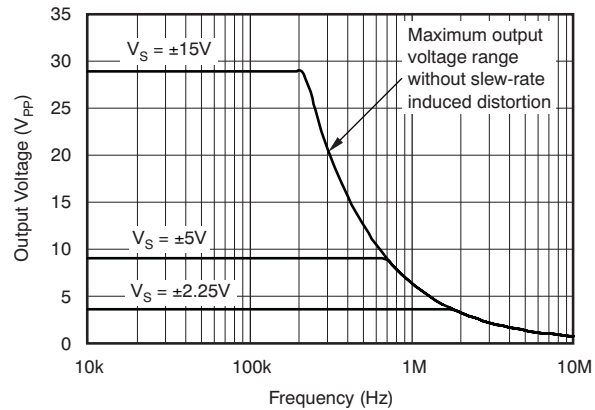

Figure 2. 0.1-Hz to 10-Hz Noise
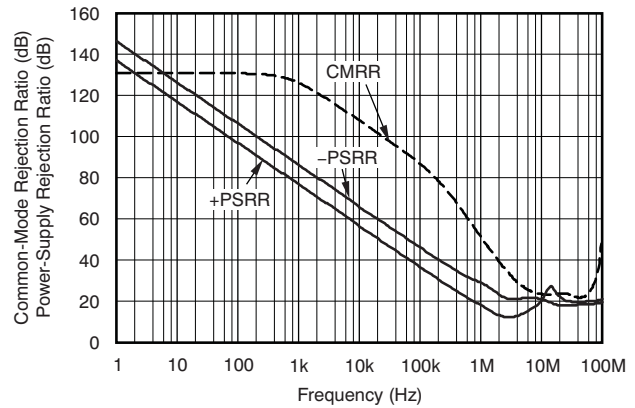

Figure 3. Maximum Output Voltage vs Frequency

Figure 4. CMRR and PSRR vs Frequency
(Referred to Input)

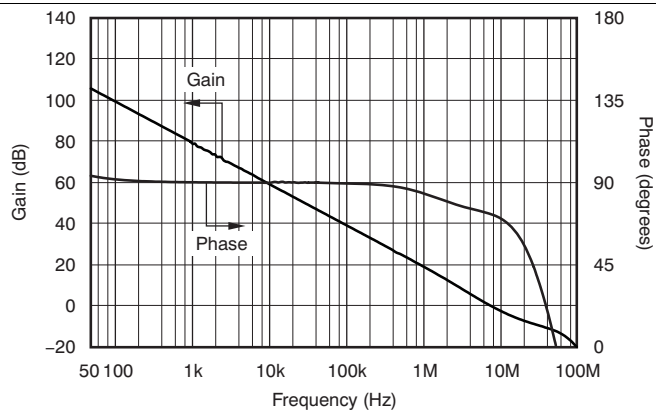Figure 5. Gain and Phase vs Frequency
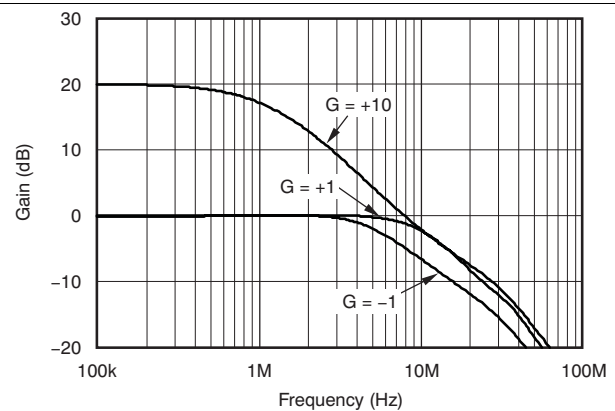

Figure 6. Closed-Loop Gain vs Frequency

Product Folder Links: *OPA1641 OPA1642 OPA1644*

Typical Characteristics (continued)

At T_A = 25°C, R_L = 2 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
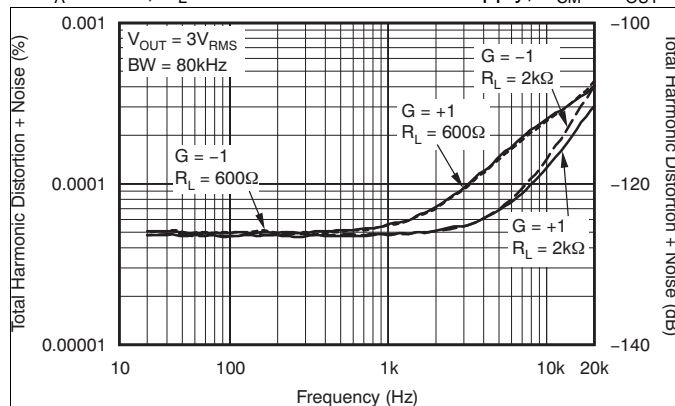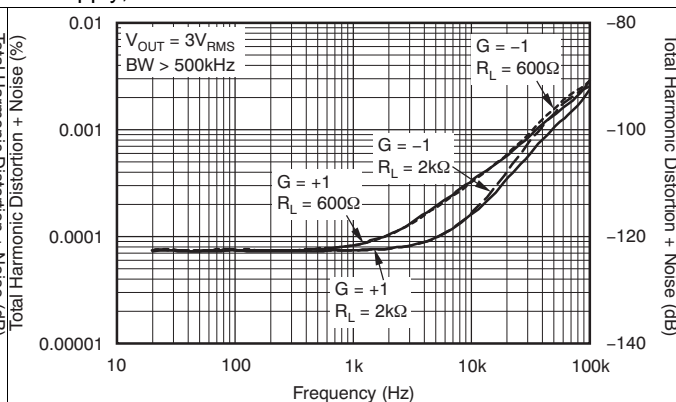

Figure 7. THD+N Ratio vs Frequency

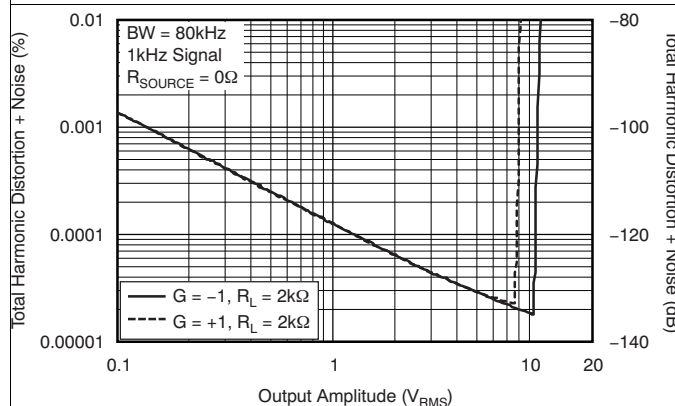Figure 8. THD+N Ratio vs Frequency
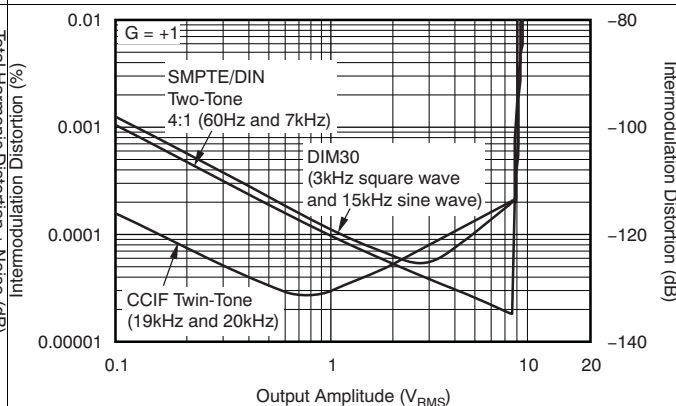

Figure 9. THD+N Ratio vs Output Amplitude

Figure 10. Intermodulation Distortion
vs Output Amplitude

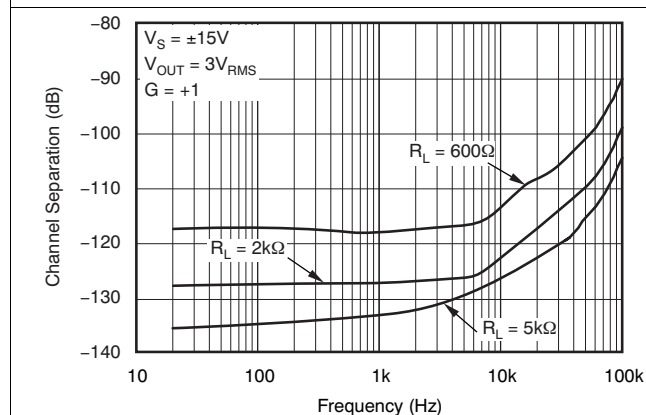

Figure 11. Channel Separation vs Frequency
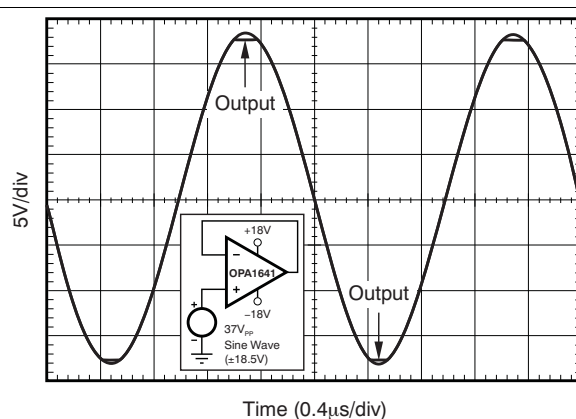

Figure 12. No Phase Reversal

Typical Characteristics (continued)

At T_A = 25°C, R_L = 2 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
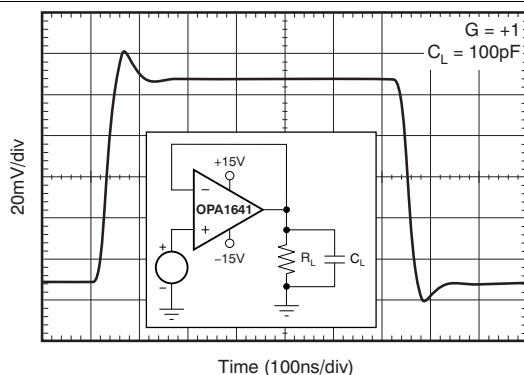

Figure 13. Small-Signal Step Response (100 mV)
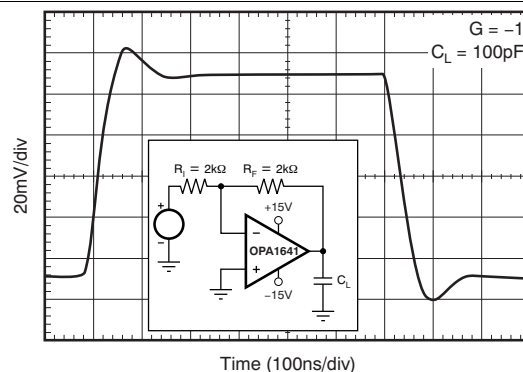

Figure 14. Small-Signal Step Response (100 mV)
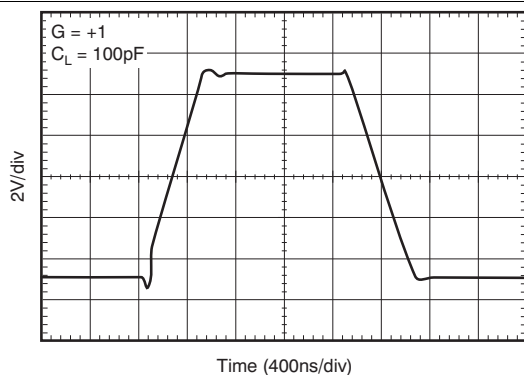
Figure 15. Large-Signal Step Response
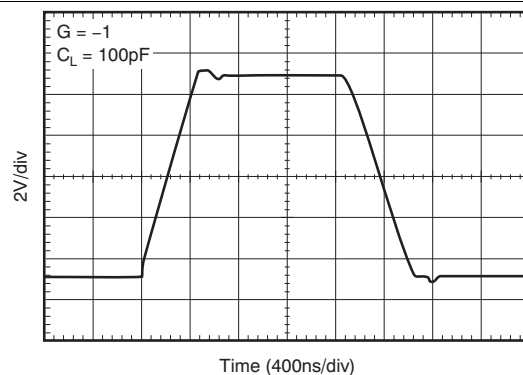
Figure 16. Large-Signal Step Response
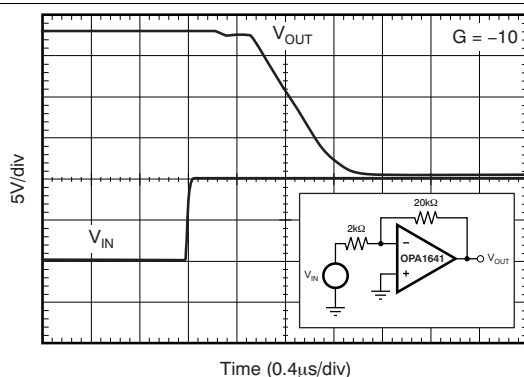
Figure 17. Positive Overload Recovery
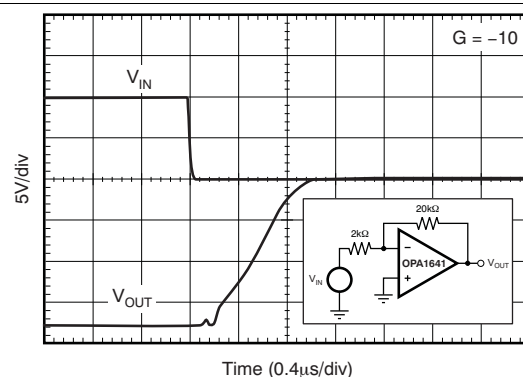
Figure 18. Negative Overload Recovery

Product Folder Links: *OPA1641 OPA1642 OPA1644*

Typical Characteristics (continued)

At T_A = 25°C, R_L = 2 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
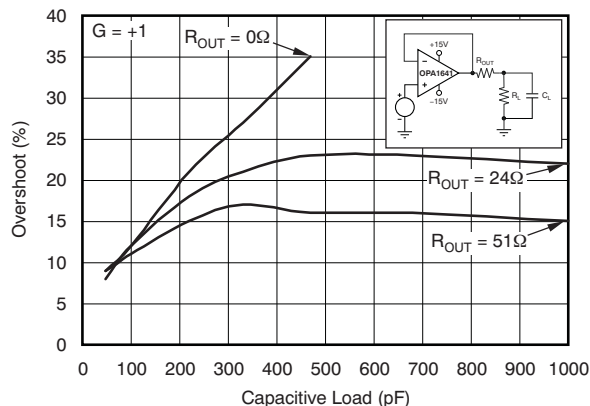
Figure 19. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)
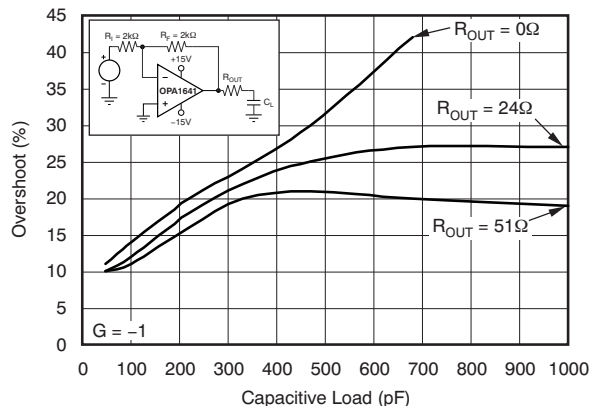
Figure 20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)
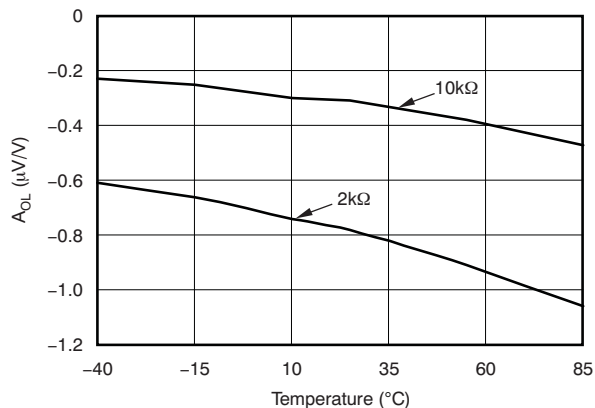
Figure 21. Open-Loop Gain vs Temperature
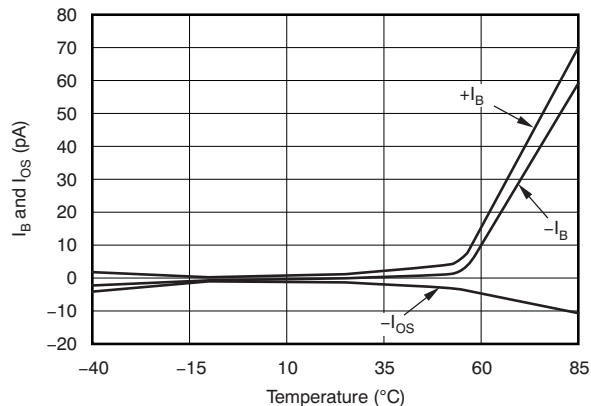
Figure 22. I_B and I_{OS} vs Temperature
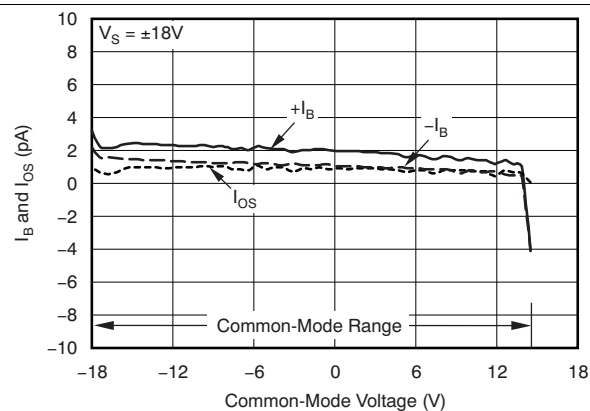
Figure 23. I_B and I_{OS} vs Common-Mode Voltage
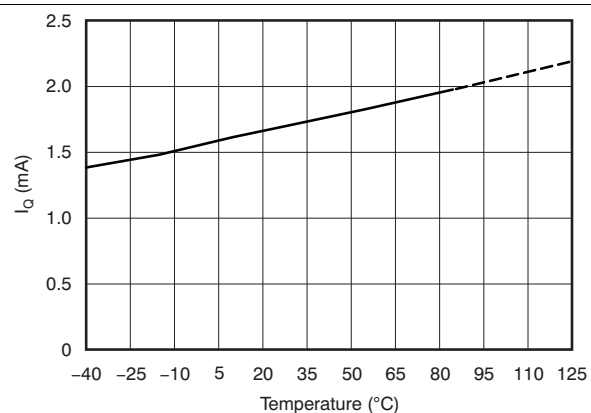
Figure 24. Quiescent Current vs Temperature

Product Folder Links: *OPA1641 OPA1642 OPA1644*

Typical Characteristics (continued)

At T_A = 25°C, R_L = 2 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
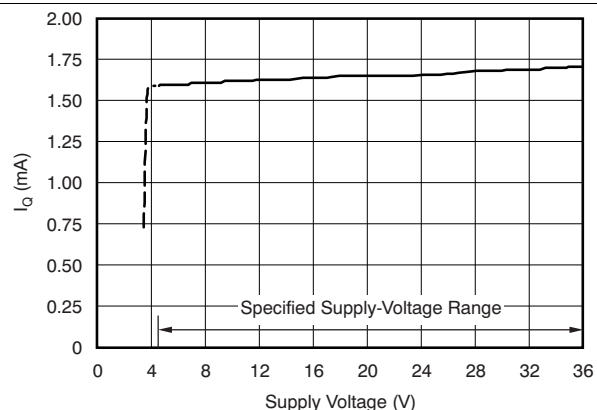
Figure 25. Quiescent Current vs Supply Voltage
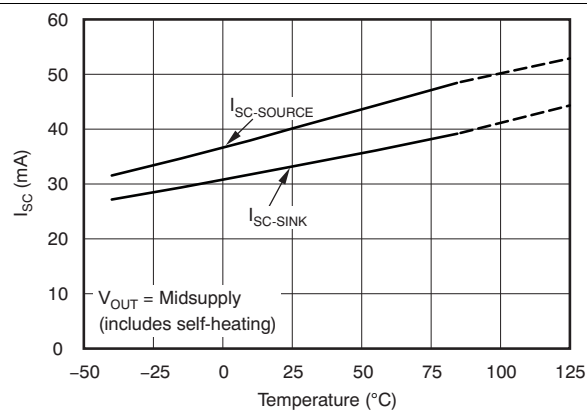
Figure 26. Short-Circuit Current vs Temperature

Figure 27. Output Voltage vs Output Current

Figure 28. Open-Loop Output Impedance vs Frequency

Product Folder Links: *OPA1641 OPA1642 OPA1644*

Feature Description (continued)

Figure 29. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

7.3.2 Output Current Limit

The output current of the OPA164x series is limited by internal circuitry to 36 mA/–30 mA (sourcing and sinking), to protect the device if the output is accidentally shorted. This short circuit current depends on temperature, as shown in Figure 26.

Although it is uncommon for most modern audio applications to require 600-Ω load drive capability, many audio operational amplifier applications continue to specify the total harmonic distortion (THD+N) at 600-Ω load for comparative purposes. Figure 7 and Figure 8 provide typical THD+N measurement curves for the OPA164x series, where the output drives a 3-V_{RMS} signal into a 600-Ω load. However, correct device operation cannot be ensured when driving 600-Ω loads at full supply. Depending on supply voltage and temperature, it may well trigger the output current limit circuitry of the device.

7.3.3 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can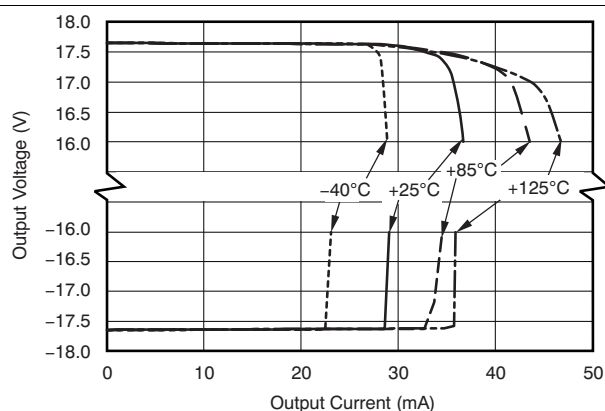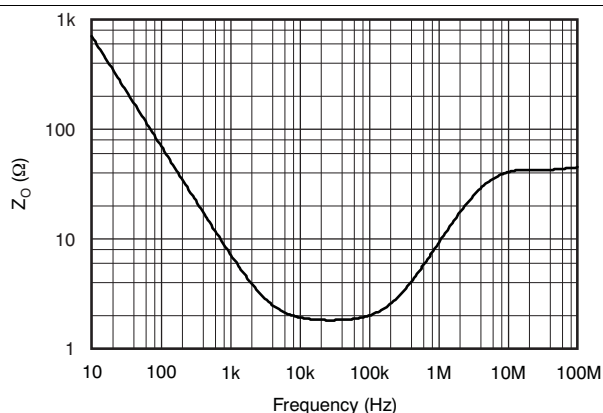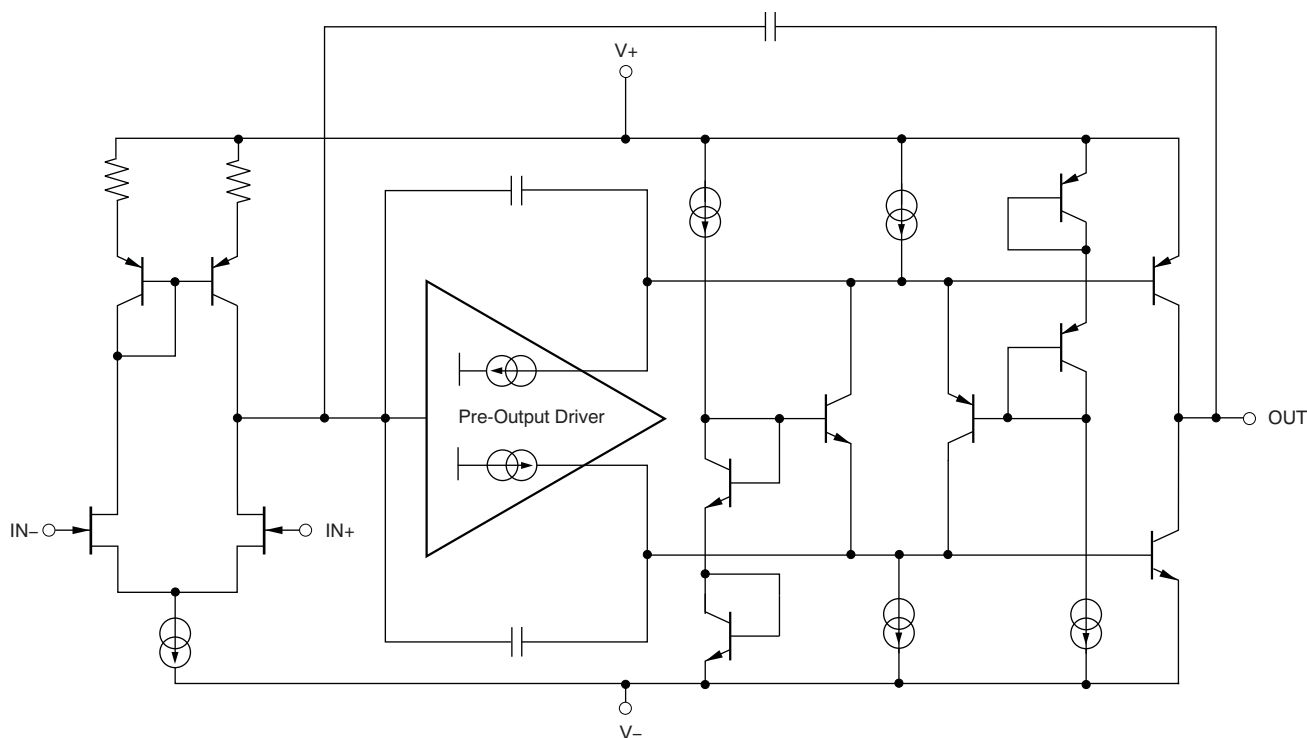 be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download at www.ti.com.

The EMIRR IN+ of the OPA164x is plotted versus frequency as shown in Figure 30. If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA164x unity-gain bandwidth is 11 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

Product Folder Links: *OPA1641   OPA1642   OPA1644*

Feature Description (continued)
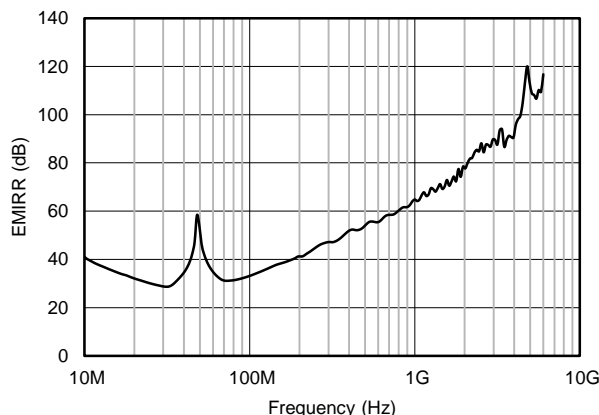
Figure 30. OPA164x EMIRR vs Frequency

Table 1 lists the EMIRR IN+ values for the OPA164x at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPA164x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION / ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite/space operation, weather, radar, UHF	53.1 dB
900 MHz	GSM, radio com/nav./GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	72.2 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	80.7 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio/satellite, S-band	86.8 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	91.7 dB
5 Ghz	802.11a/n, aero comm./nav., mobile comm., space/satellite operation, C-band	96.6 dB

7.3.3.1 EMIRR IN+ Test Configuration

Figure 31 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy. See *EMI Rejection Ratio of Operational Amplifiers* (SBOA128) for more details.

Ambient temperature: 25°C
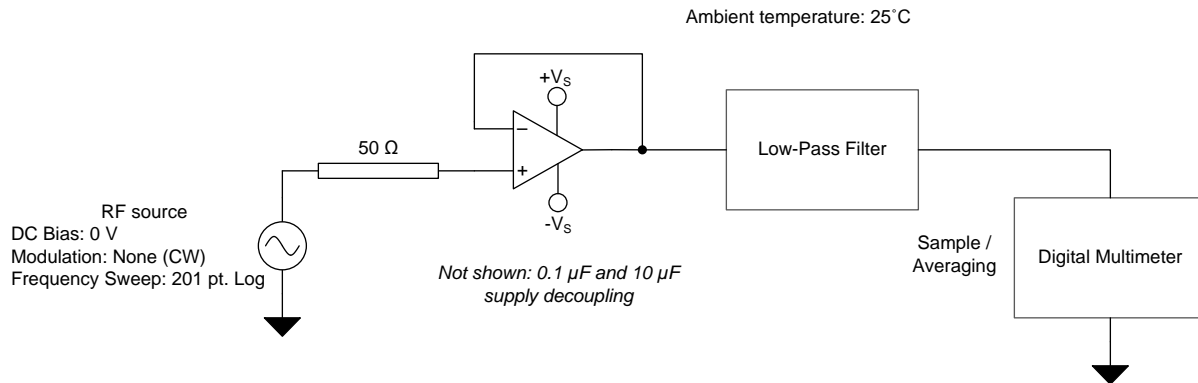
Figure 31. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

7.4.1 Operating Voltage

The OPA1641, OPA1642, and OPA1644 series of operational amplifiers can be used with single or dual supplies from an operating range of V_S = +4.5 V (±2.25 V) and up to V_S = +36 V (±18 V). These devices do not require symmetrical supplies; it only requires a minimum supply voltage of +4.5 V (±2.25 V). For V_S less than ±3.5 V, the common-mode input range does not include midsupply. Supply voltages higher than +40 V can permanently damage the device; see *Absolute Maximum Ratings* for more information. Key parameters are specified over the operating temperature range, T_A = −40°C to +85°C. Key parameters that vary over the supply voltage or temperature range are shown in *Typical Characteristics*.

8 Application and Implementation

8.1 Application Information

The OPA1641, OPA1642, and OPA1644 are unity-gain stable, audio operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. The *Simplified Internal Schematic* shows a simplified schematic of the OPA1641.

Simplified Internal Schematic
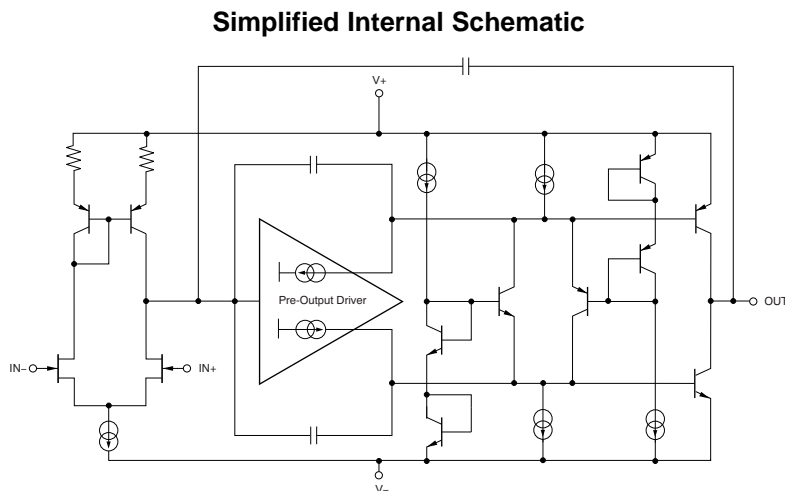
8.1.1 Noise Performance

Figure 32 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA1641, OPA1642, and OPA1644 are shown with total circuit noise calculated. The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA1641, OPA1642, and OPA1644 family has both low voltage noise and extremely low current noise because of the FET input of the operational amplifier. As a result, the current noise contribution of the OPA164x series is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.

The equation in Figure 32 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see *Basic Noise Calculations*.

Application Information (continued)
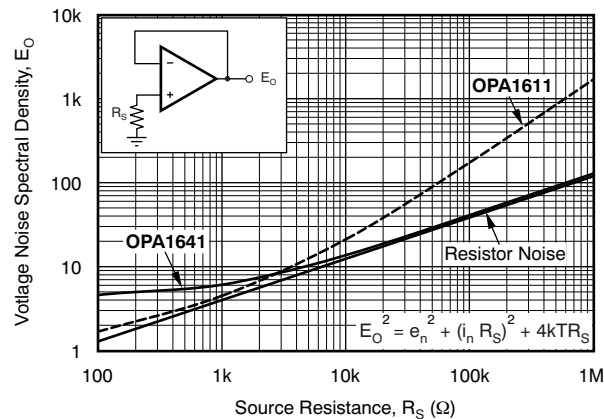
Figure 32. Noise Performance of the OPA1611 and OPA1641 in Unity-Gain Buffer Configuration

8.1.2 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall operational amplifier noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 32. The source impedance is usually fixed; consequently, select the operational amplifier and the feedback resistors to minimize the respective contributions to the total noise.

Figure 33 illustrates both noninverting (A) and inverting (B) operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPA164x means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low impedance feedback resistors will load the output of the amplifier. The equations for total noise are shown for both configurations.

Product Folder Links: *OPA1641 OPA1642 OPA1644*

A) Noise in Noninverting Gain Configuration
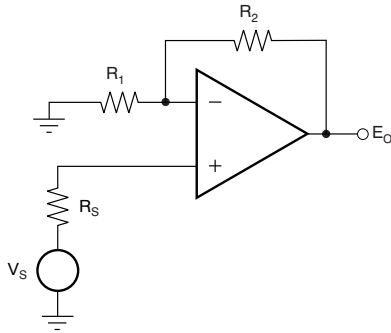
Noise at the output:

$$E_O{}^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n{}^2 + \left(\frac{R_2}{R_1}\right)^2 e_1{}^2 + e_2{}^2 + \left(1 + \frac{R_2}{R_1}\right)^2 e_s{}^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration
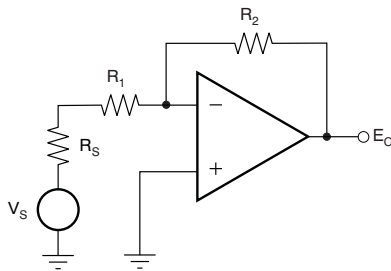
Noise at the output:

$$E_O{}^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n{}^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_1{}^2 + e_2{}^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_s{}^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA164x series op amps at 1kHz, $e_n = 5.1nV/\sqrt{Hz}$

Figure 33. Noise Calculation in Gain Configurations

Product Folder Links: *OPA1641 OPA1642 OPA1644*

8.1.3 Total Harmonic Distortion Measurements

The OPA164x series operational amplifiers have excellent distortion characteristics. THD + Noise is below 0.00005% (G = +1, V_O = 3 V_{RMS}, BW = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see Figure 7).

The distortion produced by the OPA164x series operational amplifiers is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 34) can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. Figure 34 shows a circuit that causes the operational amplifier distortion to be 101 times (or approximately 40 dB) greater than that normally produced by the operational amplifier. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

$$\text{Signal Gain} = 1 + \frac{R_2}{R_1}$$

$$\text{Distortion Gain} = 1 + \frac{R_2}{R_1 \, \| \, R_3}$$

SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω
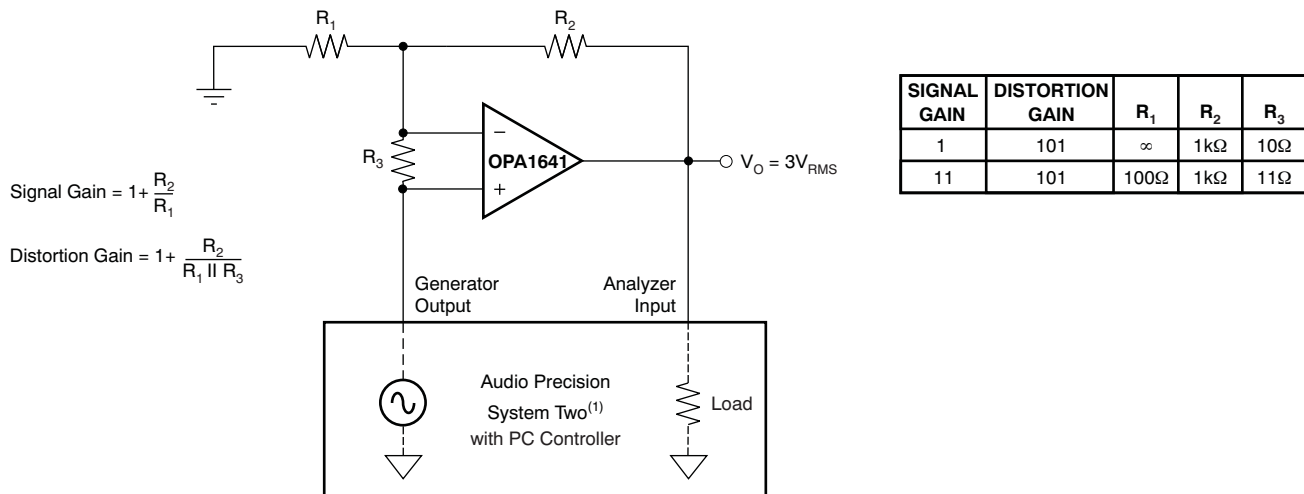
(1)   For measurement bandwidth, see Figure 7 through Figure 10.

Figure 34. Distortion Test Circuit

8.1.4 Source Impedance and Distortion

In traditional JFET-input operational amplifiers, the impedance seen by the positive and negative inputs in noninverting applications should be matched for lowest distortion. Legacy methods for fabricating the JFETs in the FET input stage exhibit a varying input capacitance with applied common-mode input voltage. In inverting configurations, the input does not vary with input voltage because the inverting input is held at virtual ground. However, in noninverting applications, the inputs do vary, and the gate-to-source voltage is not constant. This effect produces increased distortion as a result of the varying capacitance for unmatched source impedances. However, the OPA164x family of amplifiers was designed to maintain a constant input capacitance with varying common-mode voltage to prevent this mechanism of distortion. The variation of input capacitance with common-mode voltage for a traditional amplifier is compared to the OPA164x family in Figure 35.
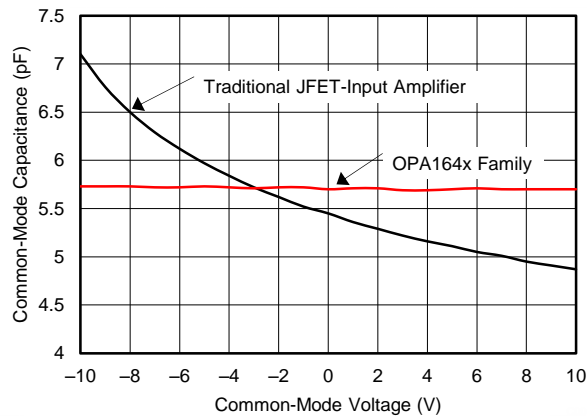
Figure 35. Input Capacitance of the OPA164x Family of Amplifiers Compared to Traditional JFET-input Amplifiers

By stabilizing the input capacitance, the distortion performance of the amplifier is greatly improved for noninverting configurations with high source impedances. The measured performance of an OPA164x amplifier is compared to a traditional JFET-input amplifier in Figure 36. The unity gain configuration, high source impedance, and large signal amplitude produce additional distortion in the traditional amplifier.
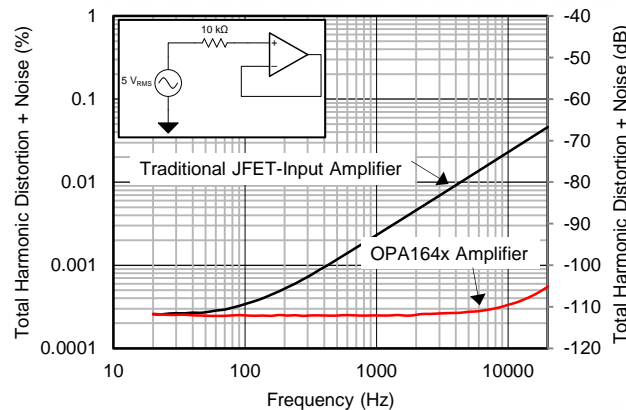
Figure 36. Measured THD+N of the OPA164x Family of Amplifiers Compared to Traditional JFET-input Amplifiers

8.1.5 Capacitive Load and Stability

The dynamic characteristics of the OPA164x have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50Ω, for example) in series with the output.

Figure 19 and Figure 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT}. Also, see Applications Bulletin AB-028, *Feedback Plots Define Op Amp AC Performance* (SBOA015) available for download at www.ti.com for details of analysis techniques and application circuits.

8.1.6 Power Dissipation And Thermal Protection

The OPA164x series of operational amplifiers are capable of driving 2-kΩ loads with power-supply voltages of up to ±18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8 kΩ at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used, as long as the output current does not exceed 13 mA; otherwise, the device short-circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA1641, OPA1642, and OPA1644 series of devices improves heat dissipation compared to conventional materials. PCB layout can also help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36 mA leads to an internal power dissipation of over 600 mW at a supply of ±18 V. In case of a dual OPA1642 in an MSOP-8 package (thermal resistance θ_{JA} = 180°C/W), such a power dissipation would lead the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase would destroy the device.

To prevent such excessive heating that can destroy the device, the OPA164x series has an internal thermal shutdown circuit, which shuts down the device if the die temperature exceeds approximately 180°C. Once this thermal shutdown circuit activates, a built-in hysteresis of 15°C ensures that the die temperature must drop to about 165°C before the device switches on again.

8.1.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 37 illustrates the ESD circuits contained in the OPA164x series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA164x but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one Figure 37 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 37 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage (+V_S) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If +V_S can sink the current, one of the upper input steering diodes conducts and directs current to +V_S. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 37. The Zener voltage must be selected such that the diode does not turn on during normal operation. However, its Zener voltage should be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.
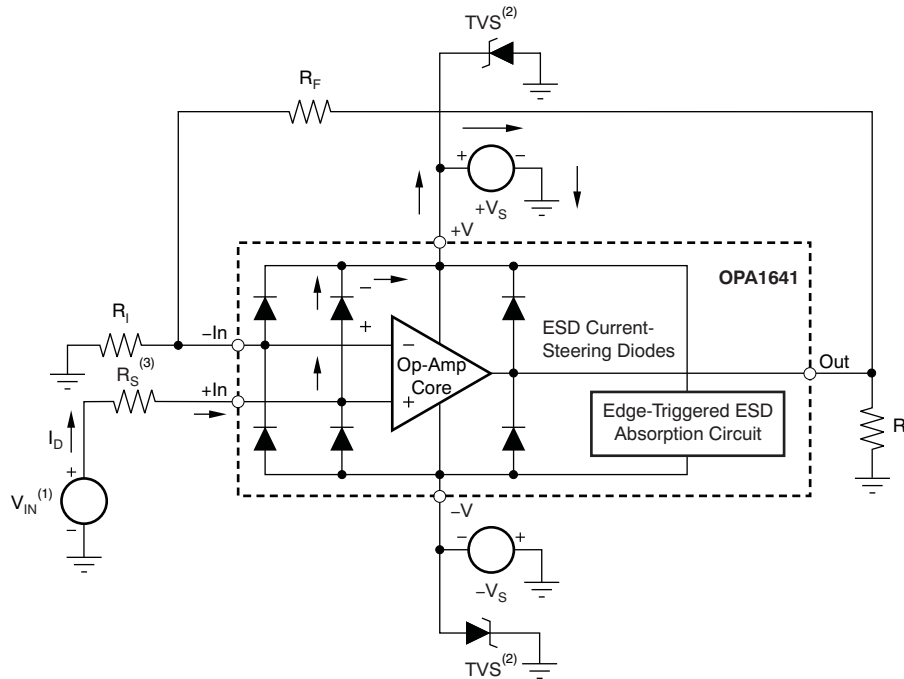
(1) $V_{IN} = +V_S + 500mV$.

(2)   TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3)   Suggested value approximately 1kΩ.

Figure 37. Equivalent Internal ESD Circuitry and the Relation to a Typical Circuit Application

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Product Folder Links: *OPA1641 OPA1642 OPA1644*

8.2 Typical Application

The noise and distortion performance of the OPA164x family of amplifiers is exceptional in applications with high source impedances which makes it an excellent choice in preamplifier circuits for moving magnet phono cartridges. The high source impedance of the cartridge, and high gain required by the RIAA playback curve at low frequency, requires an amplifier with both low input current noise, and low input voltage noise.
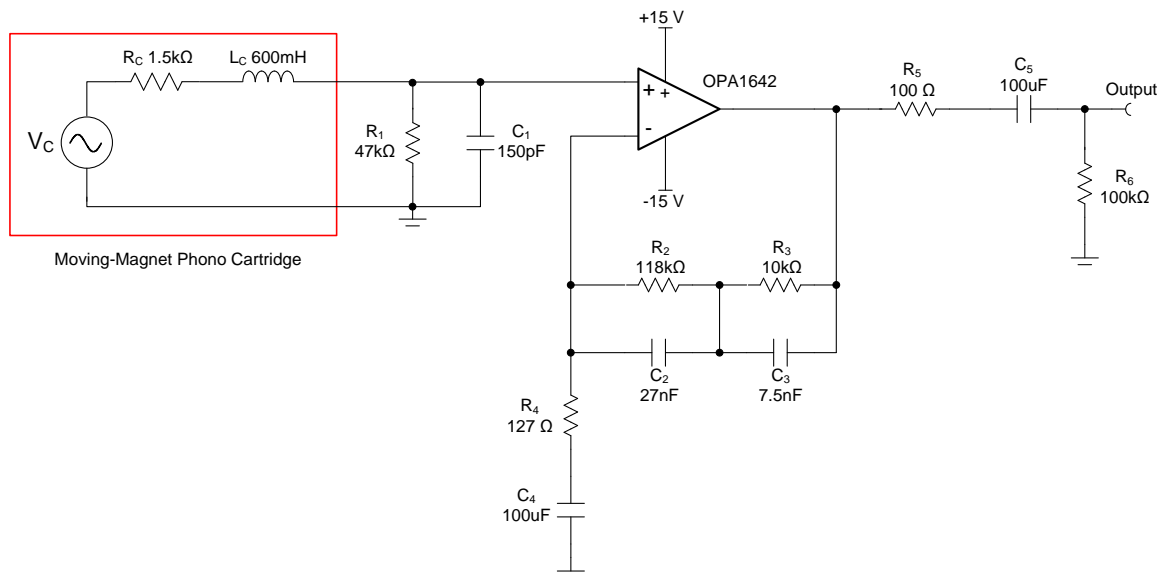
Figure 38. Preamplifier Circuit for Vinyl Record Playback With Moving-Magnet Phono Cartridges (Single Channel Shown)

8.2.1 Design Requirements

- Gain: 40 dB (1 kHz)
- RIAA Accuracy: ±0.5 dB (100 Hz to 20 kHz)
- Power Supplies: ±15 V

8.2.2 Detailed Design Procedure

Vinyl records are recorded using an equalization curve specified by the Recording Institute Association of America (RIAA). The purpose of this equalization curve is to decrease the amount of space occupied by a grove on the record and therefore maximize the amount of information able to be stored. Proper playback of music stored on the record requires a pre-amplifier circuit that applies the inverse transfer function of the recording equalization curve. The combination of the recording equalization and the playback equalization results in a flat frequency response over the audio range as shown in Figure 39.

Typical Application (continued)
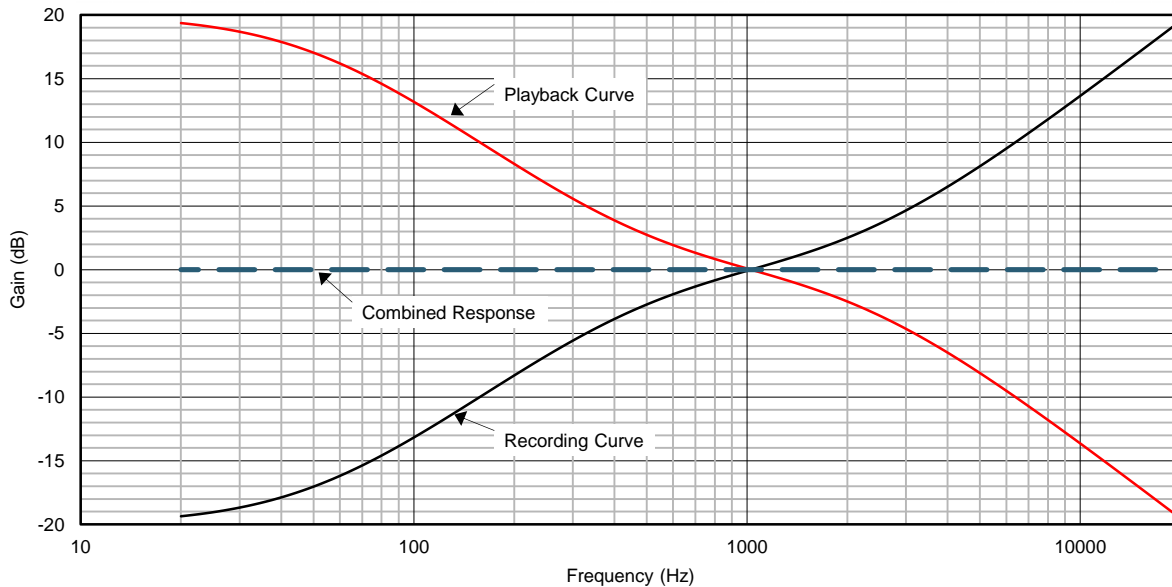
Figure 39. RIAA Recording and Playback Curves Normalized at 1 kHz

The basic RIAA playback curve implements three time constants: 75-µs, 380-µs, and 3180-µs. An IEC amendment was later added to the playback curve and implemented a pole in the curve at 20 Hz with the intent of protecting loudspeakers from excessive low frequency content. Rather than strictly adhering to the IEC amendment, this design moves this pole to a lower frequency to improve low frequency response while still providing protection for loudspeakers.

Resistor R1 and Capacitor C1 are selected to provide the proper input impedance for the moving magnet cartridge. The cartridge loading is specified by the manufacturer in the cartridge datasheet and is absolutely crucial for proper response at high frequency. 47 kΩ is a common value for the input resistor, and the capacitive loading is usually specified to 200 pF to 300 pF per channel. This capacitive loading specification includes the capacitance of the cable connecting the turntable to the preamplifier, as well as any additional parasitic capacitances at the preamplifier input. Therefore, the value of C1 needs to be less than the loading specification to account for these additional capacitances.

The output network consisting of R5, R6, and C5 serves to AC couple the preamplifier circuit to any subsequent electronics in the signal path. 100-Ω resistor R5 limits in-rush current into coupling capacitor C5 and prevents parasitic capacitance from cabling from causing instability. R6 prevents charge accumulation on C5. Capacitor C5 was chosen to be the same value as C4; for simplicity however, its value must be large enough to avoid attenuating low frequency information.

The feedback resistor elements must be selected to provide the correct response within the audio bandwidth. In order to achieve the correct frequency response, the passive components in the above circuit must satisfy the equations:

$$R_2 \times C_2 = 3180\mu s \tag{1}$$

$$R_3 \times C_3 = 75\mu s \tag{2}$$

$$\left(R_2 \| R_3\right) \times \left(C_2 + C_3\right) = 318\mu s \tag{3}$$

R2, R3, and R4 must also be selected to meet the design requirements for gain. The gain at 1 kHz is determined by subtracting 20 dB from gain of the circuit at very low frequency (near dc):

$$A_{1kHz} = A_{LF} - 20dB \tag{4}$$

Therefore the low frequency gain of the circuit must be 60 dB to meet the goal of 40 dB at 1 kHz.

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Typical Application (continued)

Because there are multiple combinations of passive components which satisfy these equations, a spreadsheet or other software calculation tool is the easiest method to examine resistor and capacitor combinations.

$$A_{LF} = 1 + \frac{R_3 + R_2}{R_4} = 1000(60dB)$$

(5)

Capacitor C4 forces the gain of the circuit to unity at dc in order to limit the offset voltage at the output of the pre-amplifier circuit. The high-pass corner frequency created by this capacitor is at:

$$F_{HP} = \frac{1}{2\pi R_4 C_4}$$

(6)

The circuit described here was constructed with 1% tolerance resistors and 5% tolerance NP0/C0G ceramic capacitors without any additional hand sorting. The large value of C4 typically requires an electrolytic type to be used. However, electrolytic capacitors have the potential to introduce distortion into the signal path. This circuit was constructed using a bipolar electrolytic capacitor specifically intended for audio applications.

8.2.3 Application Curves

The deviation from the ideal RIAA transfer function curve is shown in Figure 40 normalized to an ideal gain of 40 dB at 1 kHz. The measured gain at 1 kHz was 0.05 dB less than the design goal, and the maximum deviation from 100 Hz to 20 kHz was 0.18 dB. The deviation from the ideal curve may be improved by hand-sorting resistor and capacitor values to their ideal values. The value of C4 may also be increased to reduce the deviation at low frequency.

A spectrum of the preamplifier output signal is shown in Figure 41 for a 10 mV$_{RMS}$, 1-kHz input signal (1-V$_{RMS}$ output). All distortion harmonics are below the preamplifier noise floor.
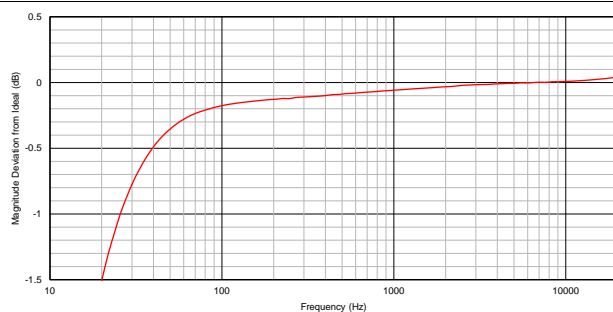
Figure 40. Measured Deviation from Ideal RIAA Response
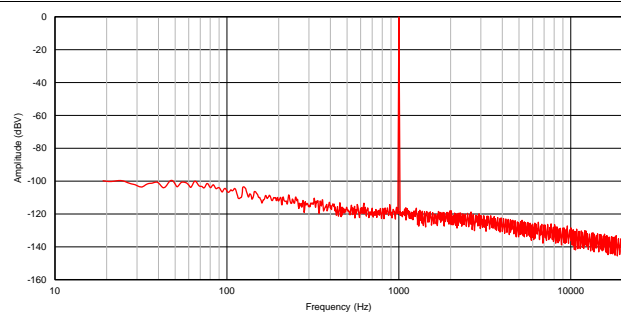

Figure 41. Output Spectrum for a 10 mV$_{RMS}$, 1 kHz Input Signal

9 Power Supply Recommendations

The OPA164xare specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 42, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

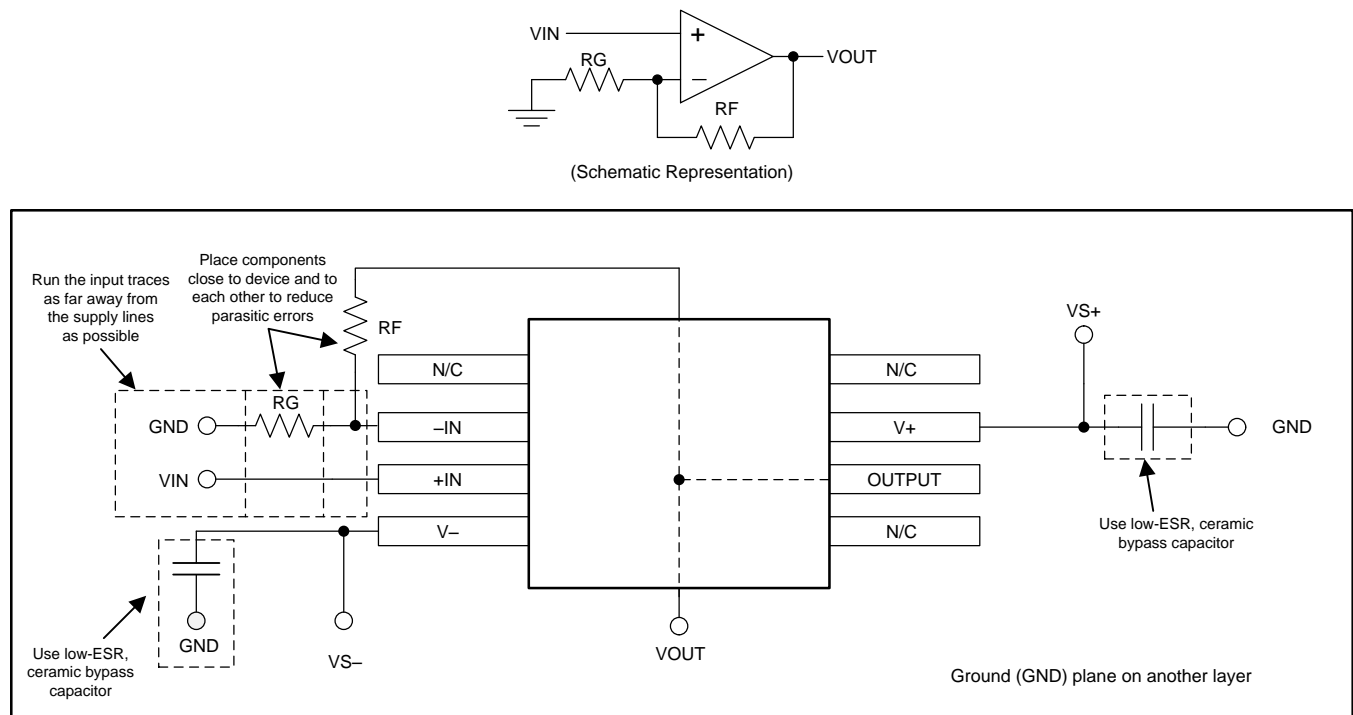(Schematic Representation)

Figure 42. OPA1641 Layout Example

11   Device and Documentation Support

11.1   Device Support

11.1.1   Development Support

11.1.1.1   TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

> **NOTE**
> These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2   TI Precision Designs

TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/, are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.1.1.3   WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2   Documentation Support

11.2.1   Related Documentation

For related documentation see the following:
- *Circuit Board Layout Techniques*, SLOA089
- *Op Amps for Everyone*, SLOD006
- *Operational amplifier gain stability, Part 3: AC gain-error analysis*, SLYT383
- *Operational amplifier gain stability, Part 2: DC gain-error analysis*, SLYT374
- *Using infinite-gain, MFB filter topology in fully differential active filters*, SLYT343
- *Op Amp Performance Analysis*, SBOS054
- *Single-Supply Operation of Operational Amplifiers*, SBOA059
- *Tuning in Amplifiers*, SBOA067
- *Shelf-Life Evaluation of Lead-Free Component Finishes*, SZZA046

11.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA1641	Click here	Click here	Click here	Click here	Click here
OPA1642	Click here	Click here	Click here	Click here	Click here
OPA1644	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.
   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *OPA1641 OPA1642 OPA1644*

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