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TI Designs – Precision: Verified Design

A High-Fidelity Headphone Amplifier for Current Output Audio DACs Reference Design

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Circuit Description

This circuit is designed to convert the differential output current of an audio digital-to-analog converter (DAC) into a single-ended voltage capable of driving low impedance headphones. Two op amps are used as transimpedance amplifiers which convert the DAC output current to a differential voltage. A difference amplifier then converts the differential voltage to single-ended. Two op amps are used in parallel in the output to increase the current available for driving the headphones.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA1612	Product Folder

TI E2E™ Community

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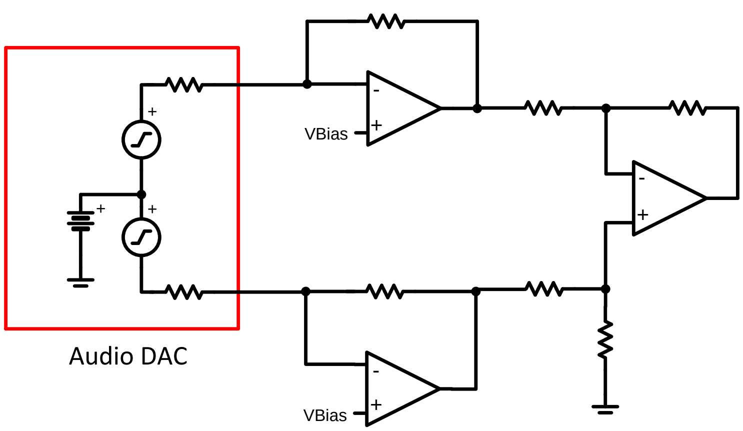

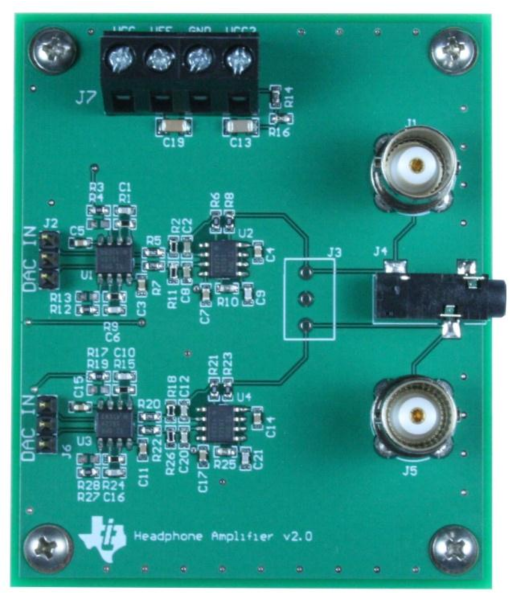

1 Design Summary

The design requirements are as follows:

- Supply Voltage: +/- 5V
- Supply Current: <20mA / channel

The design goals and performance are summarized in Table 1.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Magnitude Variation (20Hz – 20kHz)	.01dB	0.0095dB	0.007dB
Phase Variation (20Hz – 20kHz)	5.0°	3.83°	4.06°
THD+N (1kHz, 10mW, 16 and 32 Ohms)	<.001%	0.000292% (32 Ohms) 0.000413% (16 Ohms)	0.00052% (32 Ohms) 0.00078% (16 Ohms)
Maximum Output Power (Low Distortion Operation)	>50mW	N/A	55mW (32 Ohms) 51.7mW (16 Ohms)

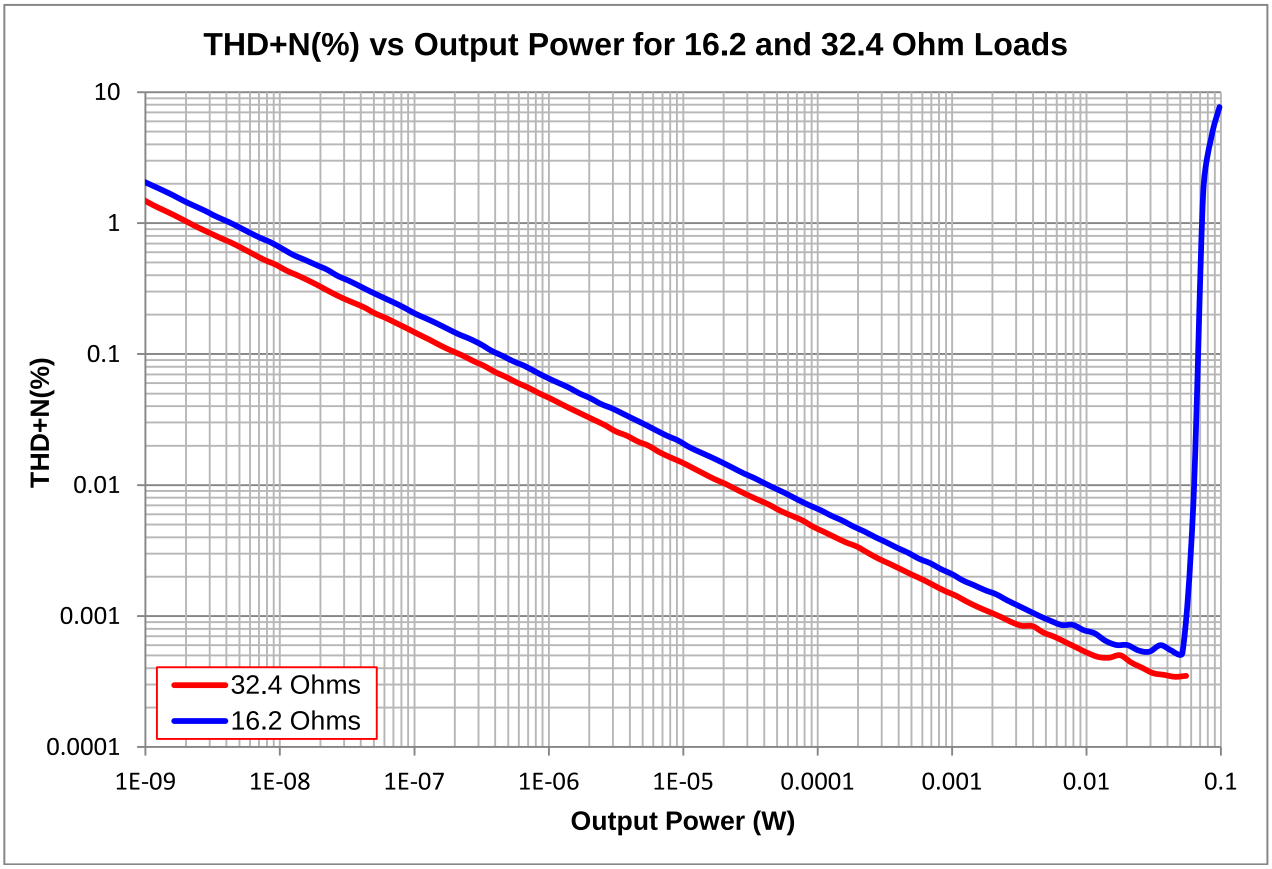

Figure 1: Measured THD+N vs. Output Power

2 Theory of Operation

Many audio digital-to-analog converters (DACs) show improved linearity when used in the current output mode. These DACs provide a differential output current that varies with the input digital audio signal. A headphone output circuit must convert this differential current to a single-ended voltage signal capable of driving headphones at reasonable listening levels. A simplified schematic of the circuit used to accomplish this function is shown below.

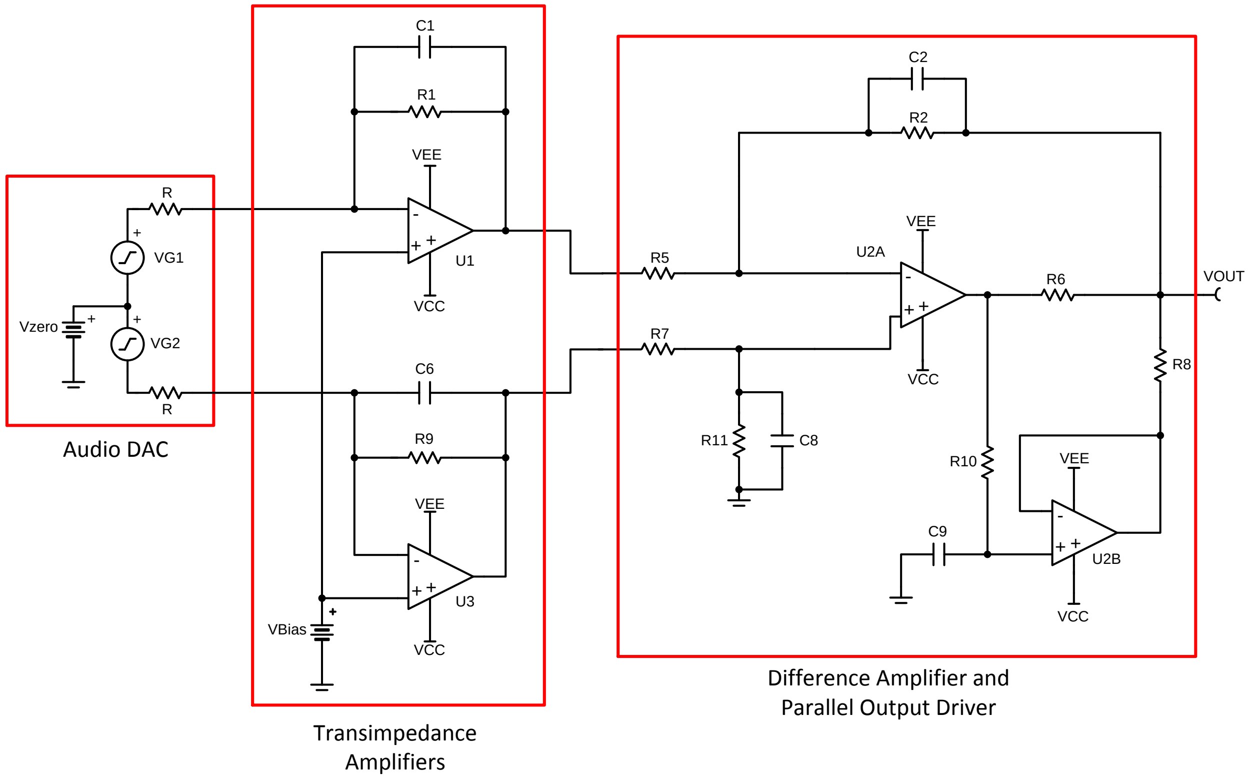

Figure 2: Simplified schematic of DAC output circuit

Two transimpedance amplifiers are used to convert the differential output current from the audio DAC to a differential output voltage. Although the audio DAC has a current output, in reality it is more accurately approximated by differential voltage sources with series resistances. There may also be an offset voltage when the DAC code is 0, represented by Vzero in Figure 2.

Once the differential output current from the DAC has been converted to a differential voltage by the transimpedance amplifiers, it is converted to a single-ended voltage by the difference amplifier. This amplifier must also be capable of driving the headphone impedance.

2.1 Transimpedance Amplifiers

From a noise standpoint, the total DAC output circuit consists of two amplifier stages in series in the signal path. Figure 3 is a simplified block diagram of the signal path, with the two stages represented by amplifiers A_1 and A_2. Each amplifier has two gains: the gain applied to the input signal, G_S, and a noise gain, G_N, which is the gain applied to the amplifier's intrinsic noise, en. The total signal gain of the circuit is simply the individual signal gains, Gs_1 and Gs_2 multiplied together.

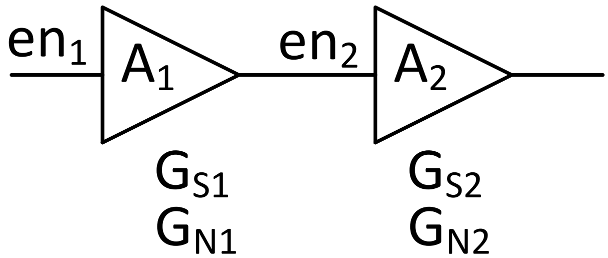

Figure 3: Symbolic representation of cascaded amplifiers

Determining the total noise of the circuit is not quite as simple. The output noise of amplifier A_1 is multiplied by the noise gain of amplifier A_1 and the signal gain amplifier A_2.Therefore the total output noise is given by the equation:

$$en_T = \sqrt{(en_1 G_{N1} G_{S2})^2 + (en_2 G_{N2})^2} \tag{1}$$

Although the noise gain will always be equal to or greater than 1, the signal gain of an amplifier can be made less than 1. This offers an interesting opportunity to reduce the overall noise of the circuit. If the signal gain of the second stage can be made much less than 1, the amount of gain in the first stage can be maximized and the noise of the first stage amplifier dominates the total noise. For this reason, the gain of the transimpedance amplifiers should be as high as possible and the difference amplifier is configured for a signal gain less than one.

The appropriate gain of the transimpedance amplifiers is determined by the output current from the audio DAC and the output voltage swing capability of the op amp selected.

A simplified model of a popular audio DAC is shown in Figure 4.

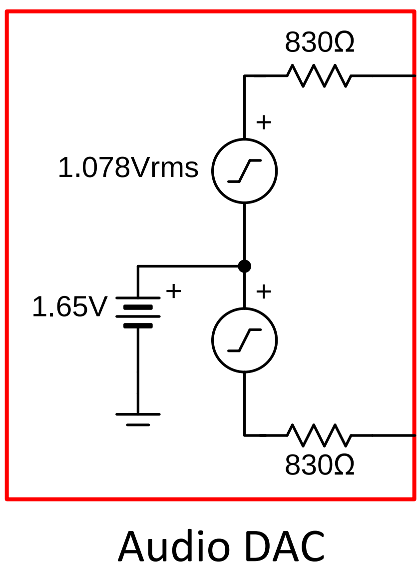

Figure 4: Simplified model of a popular audio D/A converter

In order to calculate the feedback resistors of the transimpedance amplifiers, we must first determine the maximum ac output current from the DAC. For this analysis the contributions of the 1.65V offset can be ignored. The peak single-ended output current is:

$$i_{ac(MAX)} = \frac{1.078Vrms * \sqrt{2}}{830} = 1.836mAp \tag{2}$$

The output voltage of a transimpedance amplifier is given by the equation:

$$|V_{OUT}| = R_F|i_{IN}| \tag{3}$$

R_F is the value of the feedback resistor of the transimpedance amplifier. The maximum value of R_F is determined by the power supply voltages and the linear output swing of the op amp used. This is normally given as a condition of the open loop gain measurement in the op amp datasheet:

PARAMETER		CONDITIONS	OPA1611AI, OPA1612AI MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.2V ≤ V_O ≤ (V+) – 0.2V, R_L = 10kΩ	114	130		dB
	A_{OL}	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 2kΩ	110	114		dB

Figure 5: Datasheet conditions for open loop gain measurement indicate the linear output swing

For example, the op amp specified in Figure 5 is able to maintain linear operation for output voltages within 600mV of its power supplies for 2 kΩ loads. For +/-5V power supplies, the feedback resistor can be calculated to be:

$$R_F = \frac{V_{OUT(MAX)}}{i_{IN}} = \frac{5V - 0.6V}{1.836mA} = 2396.51 \rightarrow 2.37k\Omega \tag{4}$$

A capacitor will be necessary across the feedback resistor in order to compensate for parasitic capacitance at the inverting input of the amplifier. This capacitor will also limit the amount of high-frequency noise from the amplifier or DAC that could be aliased into the audio bandwidth by other circuits.

The capacitance at the inverting input is not known, therefore the capacitor value should be as large as possible without contributing significant phase shift within the audio band. A design goal for this circuit is less than -5°. If we assume that the transimpedance amplifier and difference amplifier stages will contribute equally to this phase shift, then the phase shift from the transimpedance amplifiers should be set to -2.5° at 20kHz. Knowing the phase shift at 20kHz, allows the pole frequency to be calculated:

$$\theta = -tan^{-1}\left(\frac{f}{f_P}\right) \rightarrow f_P = \frac{f}{\tan(-\theta)} = \frac{20000Hz}{\tan(2.5°)} = 458075\ Hz \tag{5}$$

The maximum feedback capacitance can be calculated using the pole frequency and the feedback resistor value:

$$C_F \le \frac{1}{2\pi R_F F_P} \le \frac{1}{2\pi(2370\Omega)(458075Hz)} \le 146.6pF \rightarrow 100pF \tag{6}$$

2.2 Bias Voltage

When the DAC output code is zero, there will still be an output current due to the offset of the DAC. In Figure 2 a voltage, V_{Bias}, is applied to the non-inverting inputs of the transimpedance amplifiers in order to center their outputs at 0V when the DAC code is zero.

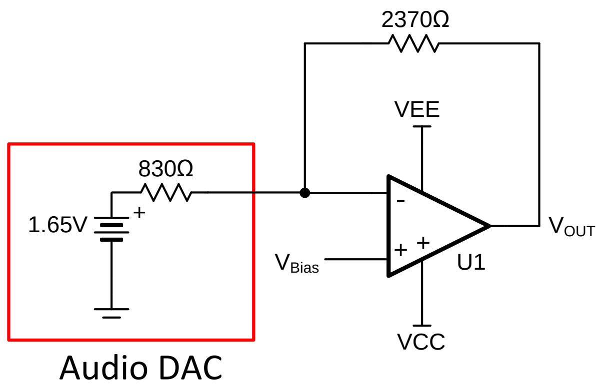

Figure 6: Simplified schematic for bias voltage calculation (single amplifier shown).

The effective circuit when the DAC output code is zero is shown in Figure 6. The appropriate voltage for V_{Bias} can be calculated from the equation:

$$V_{OUT} = 0V = V_{Bias}\left(1 + \frac{2370\Omega}{830\Omega}\right) - 1.65\left(\frac{2370\Omega}{830\Omega}\right)$$

$$\frac{1.65\left(\frac{2370\Omega}{830\Omega}\right)}{\left(1 + \frac{2370\Omega}{830\Omega}\right)} = V_{Bias} \tag{7}$$

$$1.222V = V_{Bias}$$

A resistor divider can be used to provide the bias voltage to the non-inverting inputs of the transimpedance amplifiers.

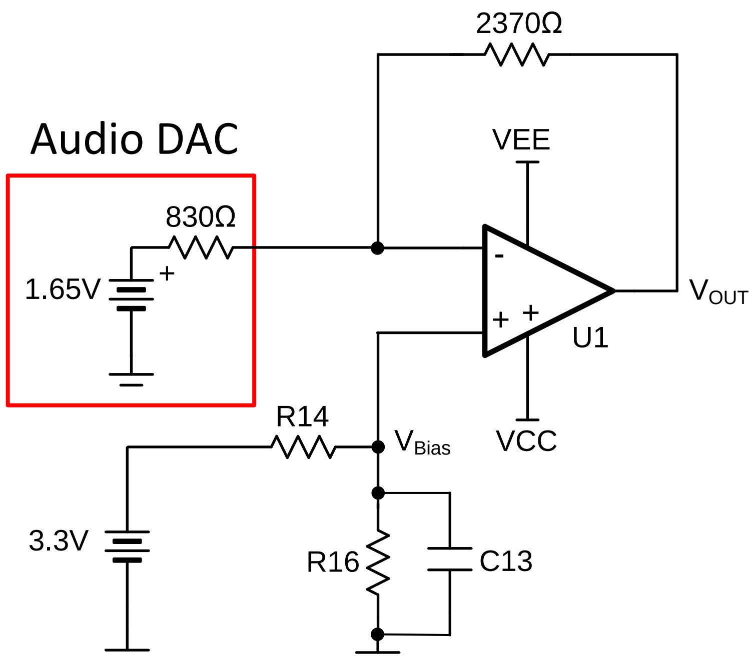

Figure 7: A resistor network is used to produce the bias voltage for the transimpedance amplifiers.

A 3.3V supply is assumed for the resistor divider. R14 and R16 can be calculated to provide the desired bias voltage:

$$V_{Bias} = 1.222V = 3.3V\frac{R_{16}}{R_{14} + R_{16}}$$
$$R_{14} = 1.7005R_{16} \tag{8}$$

The 1% resistor values closest to this ratio are R14: 18.2kΩ, R16: 10.7kΩ. These values will produce a VBias of 1.2218V.

A capacitor should be placed in parallel with R16 to prevent noise from the 3.3V supply from entering the signal path. The corner frequency produced by capacitor C13 is:

$$f_C = \frac{1}{2\pi(R_{14}||R_{16})C_{13}} \tag{9}$$

The corner frequency should be less than 20Hz to attenuate supply noise within the audio bandwidth. C13 is then calculated:

$$C_{13} \geq \frac{1}{2\pi(R_{14}||R_{16})f_C} \geq \frac{1}{2\pi(6.768k\Omega)(20Hz)} \geq 1.18\mu F \tag{10}$$

2.2μF is selected as the value for C13. Larger capacitors may be used but they may require larger PCB footprints and will extend the start-up time of the circuit.

2.3 Difference Amplifier

The difference amplifier portion converts the differential output signal from the transimpedance amplifiers into a single-ended signal and attenuates it to proper amplitude for headphones.

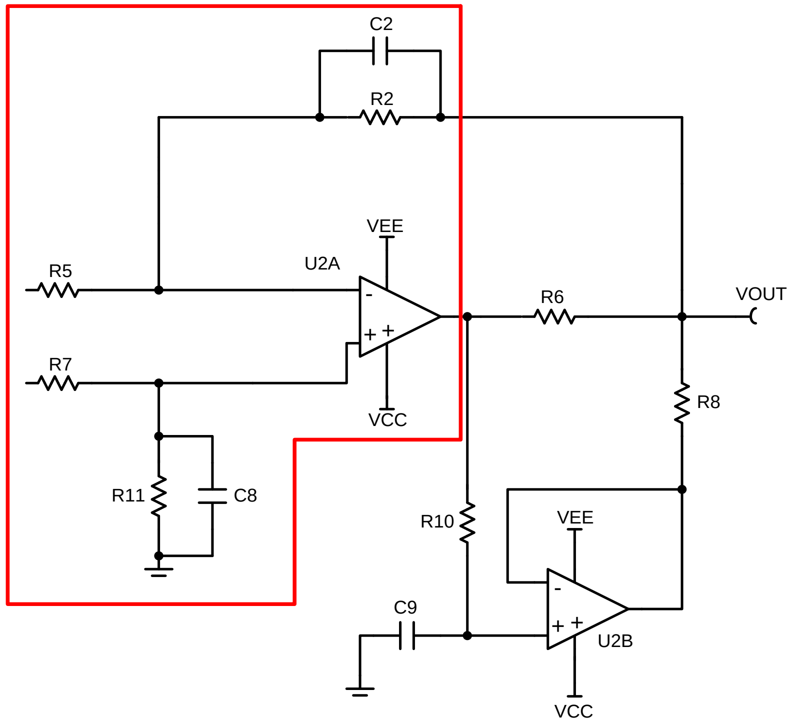

Figure 8: The difference amplifier portion of the output circuit.

The amount of attenuation implemented in the difference amplifier is determined by the desired maximum output voltage level. Headphones used for portable applications typically have low impedances (16 or 32 ohms) and therefore do not require high voltages to produce loud sounds. For example, to deliver 10mW to 32 ohm headphones only requires an output voltage of .566 Vrms.

This output level suggests that the attenuation used in the difference amplifier should be very large in order to achieve the best overall noise performance of the system. However, headphone outputs are often also used to interface portable electronics to larger audio systems through analog auxiliary inputs. For this reason, typical line-level audio (+4 dBu, 1.228Vrms) is used as the maximum output voltage. The attenuation in the difference amplifier is then calculated by dividing the output amplitude by the differential input amplitude.

The full-scale differential input to the difference amplifier is:

$$V_{DIFF} = 2 * 1.078Vrms\left(\frac{R_F}{R_{OUT}}\right) = 2 * 1.078Vrms\left(\frac{2370\Omega}{830\Omega}\right) = 5.7108Vrms \tag{11}$$

R_F is the feedback resistor value used in the transimpedance amplifiers and R_{OUT} is the output resistance of the audio DAC. The attenuation factor is then calculated:

$$A = \frac{V_{OUT}}{V_{DIFF}} = \frac{1.228Vrms}{5.7108Vrms} = .21503 \tag{12}$$

The attenuation factor determines the ratio of resistor values used in the difference amplifier:

$$A = \frac{R_2}{R_5} = \frac{R_{11}}{R_7} \tag{13}$$

These resistor values should be low enough to avoid introducing significant thermal noise, but high enough to not excessively load the transimpedance amplifier outputs. In laboratory testing, a value of 1.6k Ohms for R5 and R7 yielded the best performance. R2 and R11 can thus be calculated:

$$R_2, R_{14} = 1.6k\Omega * A = 344\Omega \rightarrow 348\Omega \tag{14}$$

Capacitors C2 and C8 are necessary to attenuate high frequency noise and may also assist in maintaining stability in the circuit under certain conditions. As mentioned in the transimpedance amplifier section, the values of these capacitors are limited by the phase shift they contribute at audible frequencies. The pole frequency produced by capacitors C2 and C8 is:

$$F_P = \frac{1}{2\pi(R_{2,}R_{11})(C_{2,}C_8)} \tag{15}$$

By setting the pole frequency equal to the value calculated in section 2.1, C2 and C8 can be calculated to meet the goals for phase shift at 20kHz.

$$C_2, C_8 \leq \frac{1}{2\pi R_2 F_P} \leq \frac{1}{2\pi(348\Omega)(458075Hz)} \leq 998.4pF \rightarrow 820pF \tag{16}$$

820pF was selected because it was the next readily-available denomination below the calculated value.

2.4 Parallel Output Driver

The output current capability of the circuit can be improved by using two op amps in parallel to drive the load. This increases the maximum output power into low impedance loads, but also reduces distortion at lower output powers due to reduced loading on the output amplifiers.

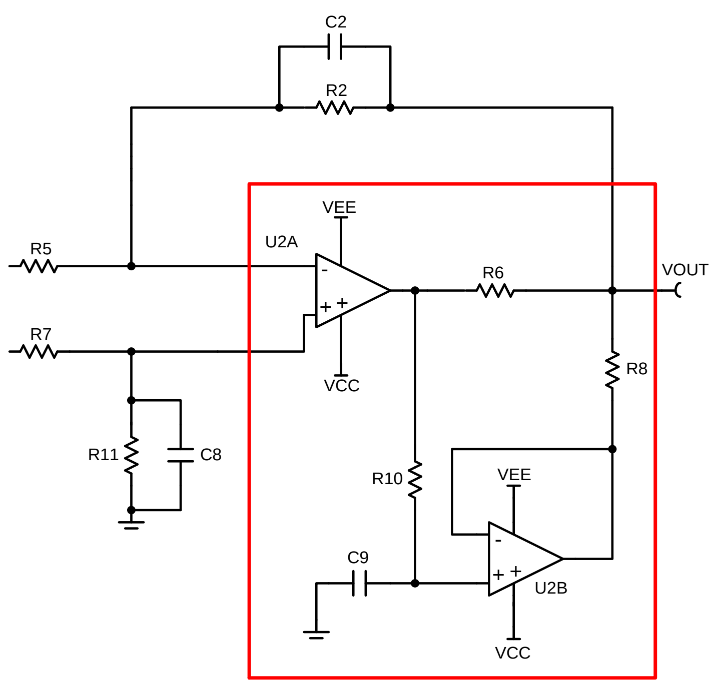

Figure 9: A second op amp is used in parallel to increase the available output current.

Resistors R6 and R8 enable the load current to be shared between amplifiers U2A and U2B. These resistors prevent one amplifier from back-driving current into the other due to differences in their open-loop gains. Also, these resistors reduce dc current that will circulated between the two outputs as a result of the different input offset voltages of the parts. The feedback loop of the difference amplifier is closed after the load sharing resistors in order to preserve the low closed-loop output impedance.

The dc circulating current in the two outputs is given by the equation:

$$i_{dc} = \frac{V_{OS(U2B)}}{R_6 + R_8} \tag{17}$$

Audio op amps are typically not trimmed for low offset, therefore the worst-case offset voltage of U2B may be as high as 2mV for some parts. In order to limit the quiescent power consumption of the total circuit, the dc circulating current is limited to 100µA. The values for R6 and R8 are:

$$R_6 + R_8 = \frac{V_{OS(U2B)}}{i_{dc}} = \frac{2mV}{100\mu A} = 20\Omega \tag{18}$$

Selecting 10 ohms for both resistors ensures that the load current will be split equally between the two amplifiers.

Some op amps may require R10 and C9 to ensure stability. To understand their function, consider that amplifier U2B has both negative and positive feedback. Positive feedback is applied to the non-inverting input of U2B by U2A. The lowpass filter created by R10 and C9 reduces the amount of positive feedback to U2B to improve stability. Unfortunately, this also reduces U2B's contribution to the total output load current which will increase distortion. For this design, we will accept a 0.01dB reduction in the contribution of the parallel amplifier at 20kHz. This allows the corner frequency of the RC circuit to be calculated:

$$G_V = \frac{G_{DC}}{\sqrt{\left(\frac{f}{f_P}\right)^2 + 1}} \rightarrow = .998 = \frac{1}{\sqrt{\left(\frac{20kHz}{f_P}\right)^2 + 1}} \rightarrow f_P = 416555Hz \tag{19}$$

Selecting R10 = 249 ohms, C9 = 1.8nF produces a slightly lower corner frequency (355kHz) with minimal impact at audio frequencies.

3 Component Selection

3.1 Resistors

The feedback resistors in the transimpedance amplifiers (R1, R9) as well as the resistors forming the difference amplifier (R2, R5, R7, R11) should be high tolerance 0.1% resistors for best performance. Choosing high tolerance resistors ensures that the output voltages of the transimpedance amplifiers will be matched very well. High tolerance resistors also maximize the common-mode rejection of the difference amplifier which can reduce dc offset at the headphone output and cancel even harmonic distortion from the transimpedance amplifiers or DAC.

3.2 Capacitors

All capacitors that may have a substantial signal voltage across them (C1, C2, C6, C8, C9) must be C0G/NP0 type ceramics. Other types of ceramic capacitors (X7R, X5R, etc.) will produce large amounts of distortion and degrade the performance of the circuit. Please see references [1] and [2] for more information on this effect.

3.3 Amplifiers

Dual op amps are selected for this design for simplicity of implementation. This allows the two transimpedance amplifiers, and the two output amplifiers, to be in the same package. A quad op amp may reduce the total solution cost, but there are fewer devices to choose from. The minimum requirements for all dual op amps in this circuit are a maximum supply voltage greater than 10V and power supply current of less than 5mA per channel. The audio op amps which meet these requirements are:

Table 2: Dual audio op amps which meet the power supply voltage and current design requirements.

Op Amp	Maximum Supply Voltage	Supply Current per Channel
OPA1612	36V	3.6mA
OPA1602	36V	2.6mA
OPA1662	36V	1.4mA
OPA1652	36V	2.0mA
LME49725	36V	3.0mA
LME49723	36V	3.4mA

Transimpedance Amplifiers

The amount of gain in the transimpedance amplifiers is limited by the op amp's linear swing to its power supply rails. A value of 0.6V was used in section 2.1 to calculate the feedback resistor value. As shown in Table 3, 3 audio op amps meet the basic requirements for the circuit and are able to linearly swing to .6V from the power supplies.

Table 3: Linear output swing of dual audio op amps

Op Amp	Linear Swing to Rail
OPA1612	0.6V
OPA1602	0.6V
OPA1662	0.6V
OPA1652	0.8V
LME49725	>1V
LME49723	>1V

The second requirement for the transimpedance amplifiers is low noise in order to preserve extremely high audio fidelity. Unlike other transimpedance amplifier applications, the source impedance is rather low, being the parallel combination of the 830 ohm DAC output resistors and the 2.37k ohm feedback resistors (R_S = 830 || 2.37k = 614.7 ohms). Furthermore, the feedback resistor is larger than the source resistance, resulting in a noise gain greater than 1:

$$G_{Noise} = 1 + \frac{R_F}{R_I} = 1 + \frac{2.37k\Omega}{830\Omega} = 3.855 \tag{20}$$

The source impedance and noise gain both indicate that the input voltage noise, rather than the input current noise, will be the dominant factor in the total output noise. Comparing the input voltage noise of the three op amps from Table 3 which met the linear output swing requirement shows that the OPA1612 has the lowest voltage noise.

Table 4: Input voltage noise of audio op amps which met output swing requirement

Op Amp	Input Voltage Noise
OPA1612	1.1nV/√Hz
OPA1602	2.5nV/√Hz
OPA1662	3.3nV/√Hz

Output Amplifiers

The most difficult requirement for the output op amps is to maintain low distortion at output current levels above those usually found in small signal design. Table 1 contains the design requirement of THD+N <.001% for an output power of 10mW into either a 16 ohm or a 32 ohm load. It will be more difficult to meet this design requirement into a 16 ohm load because the output current will be larger. To deliver 10mW to a 16 ohm load, the headphone circuit must output:

$$I_{OUT} = \sqrt{\frac{P_{OUT}}{R_L}} = \sqrt{\frac{10mW}{16}} = 25mA_{RMS} \tag{21}$$

Because this output current is shared equally between the two output amplifiers, each will be required to deliver $12.5mA_{RMS}$.

Most datasheets for audio op amps characterize THD+N versus the output amplitude into higher load impedances, such as 2k ohms or 600 ohms. This data can still be used to estimate the linearity of the amplifier into low-impedances loads by first comparing similar output current levels. When driving a 600 ohm load, the op amp will be required to deliver $12.5mA_{RMS}$ when the output voltage is $7.5V_{RMS}$. The THD+N versus output amplitude graph for the OPA1612 shown in Figure 10 gives a THD+N of -140dB (.00001%) in the gain +1 configuration at this output level.

This number must be adjusted to account for the different output voltage levels. The lower signal voltage in the 16 ohm case will degrade the ratio of signal voltage to noise voltage. The output amplitude for 10mW into a 16 ohm load is $.4V_{RMS}$, the degradation in the THD+N (assuming the measurement is noise dominated) is:

$$20\log\left(\frac{0.4}{7.5}\right) = -25.46dB \tag{22}$$

Using this correction term, the estimated THD+N of the OPA1612 will be:

$$-140dB - (-25.46dB) = -114.54dB \rightarrow .000187\% \tag{23}$$

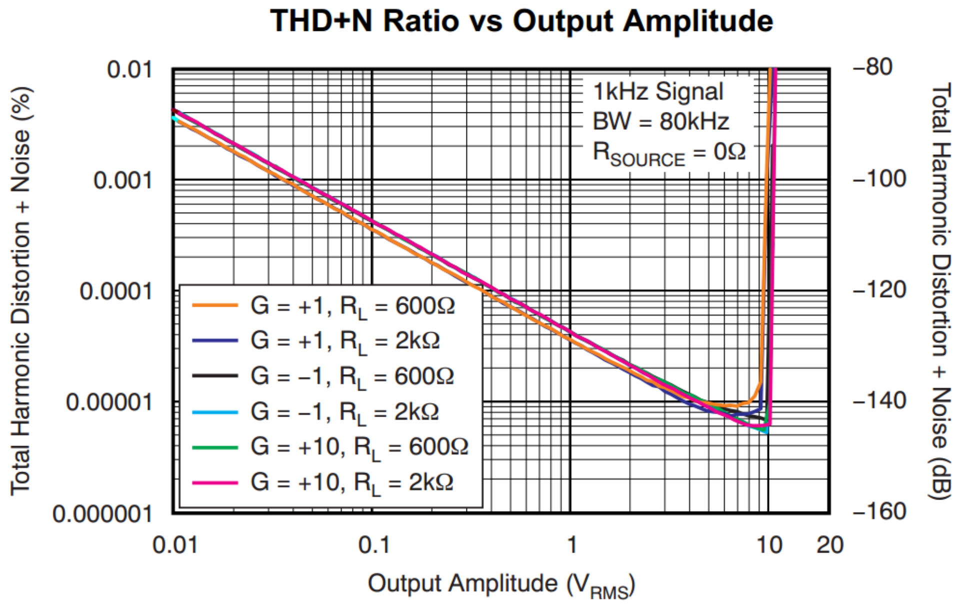

Figure 10: THD+N vs. output voltage from the OPA1612.

This calculation does not include the additional noise from the rest of the circuit, and should only be used to compare candidates for the amplifier. Table 5 compares several dual audio op amps using the method outlined above. The OPA1612 delivers the highest performance of the selected models.

Table 5: A comparison of the predicted THD+N(%) of several audio op amps.

Op Amp	Predicted THD+N (1kHz, 10mW, 16 ohms)
OPA1612	0.000187%
OPA1602	0.000656%
OPA1662	0.0024%
OPA1652	0.0015%
LME49725	0.00045

4 Simulation

The simulation schematic shown in Figure 11 is used for the noise and transfer function simulations. The audio DAC is represented on the left of the schematic in a blue rectangle. For many analyses in TINA-TI™ only a single input signal source can be accommodated, therefore a voltage controlled voltage source (VCVS) with a gain of 1 allows the DAC output voltage to be differential without requiring two voltage sources.

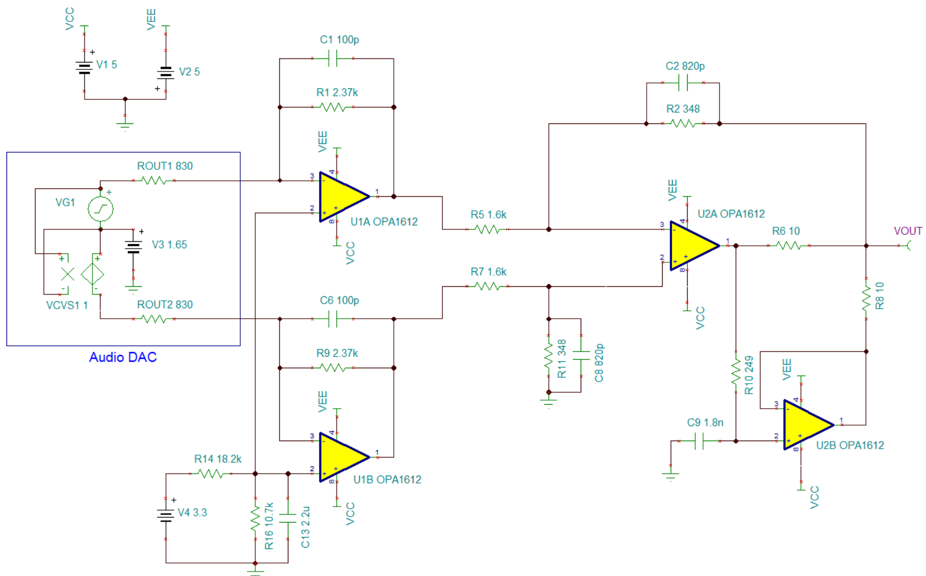

Figure 11: TINA-TI™ simulation schematic for transfer function and noise analysis.

4.1 Transfer Function

An ac transfer characteristic analysis was used to determine the magnitude and phase response of the circuit. At 20kHz the magnitude response was down -0.0095dB and the phase had deviated -3.83 degrees. These results satisfy the design goals listed in section 1.

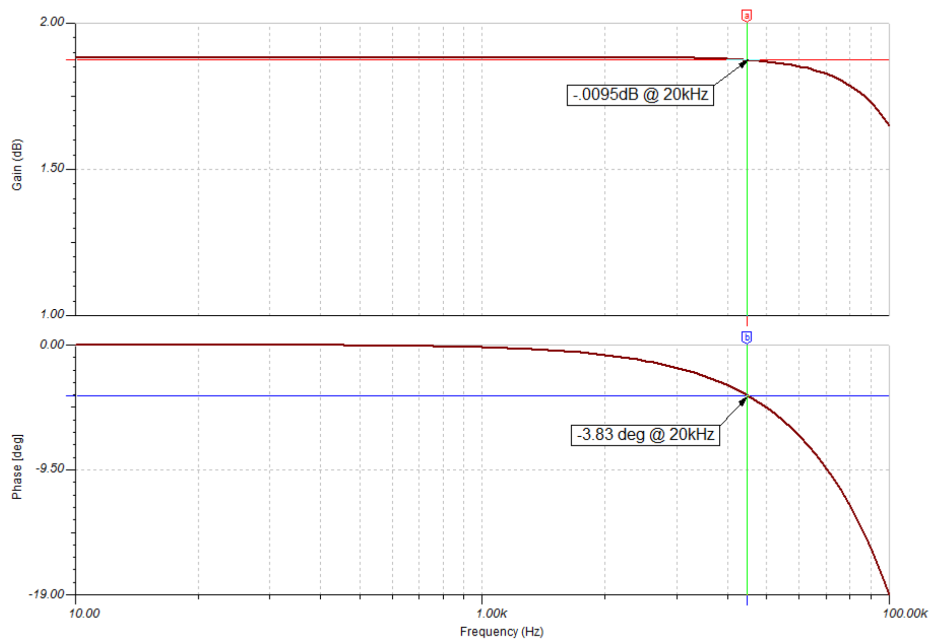

Figure 12: Circuit magnitude and phase response plotted using an ac transfer characteristic simulation.

4.2 Noise

The total output noise was integrated over an 80 kHz bandwidth using the noise analysis function of TINA-TI™. The predicted RMS noise voltage was 1.65 µVrms for an 80 kHz bandwidth.

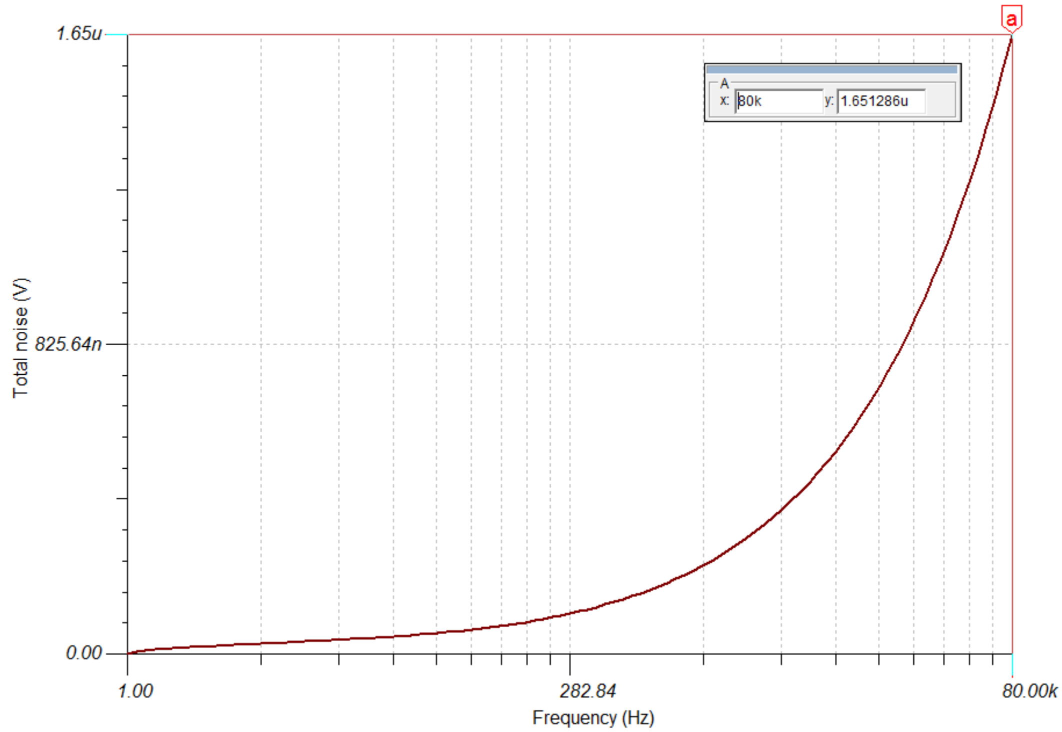

Figure 13: TINA-TI(TM) total noise simulation showing 1.65uVrms noise in an 80kHz bandwidth

Using the RMS noise voltage, the noise contribution to the THD+N figure can be calculated for different output levels using this equation:

$$THD + N(\%) = 100 * \sqrt{\frac{{V_n}^2}{{V_f}^2}} \tag{24}$$

Where V_n is the RMS noise voltage and V_f is the RMS voltage of the fundamental.

Table 6: Predicted noise-dominated THD+N values for 10mW output power into 16 and 32 ohm loads

Load Impedance	Output Voltage at 10mW	Predicted THD+N (Noise Dominated)
16 ohms	.4Vrms	0.000413%
32 ohms	.566Vrms	0.000292%

4.3 Stability- Difference Amplifier

The TINA-TI™ simulation schematic used to test the stability of the difference amplifier is shown in Figure 14. The feedback loop of the difference amplifier (U2A) is broken by inductor LT and a signal is injected by voltage source VG1 through capacitor CT. The loop gain and phase margin are measured by voltage probe AOLB. A network of passive components (labeled headphone impedance approximation) is used to simulate the impedance of many headphones at high frequencies. The inductance of the driver voice coils in the headphones combined with the inductance and capacitance of the cord forms a resonance typically at 1.0-1.5MHz which may cause stability problems. This effect needs to be accounted for in the design of the circuit.

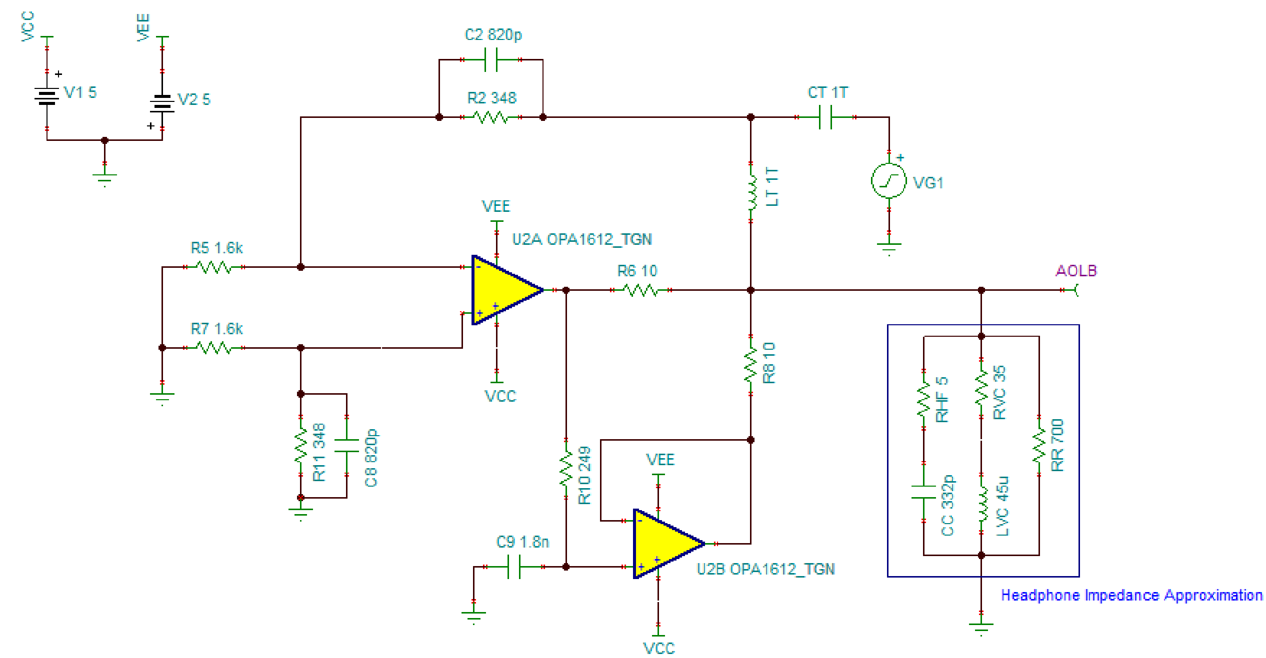

Figure 14: TINA-TI(TM) simulation schematic to determine the phase margin of the difference amplifier

The phase margin of the circuit is determined by performing an ac transfer characteristic simulation and measuring the phase at the loop closure point (0 dB). The phase margin of amplifier U2A is 47.46 degrees with the simulated headphone load, indicating stable operation.

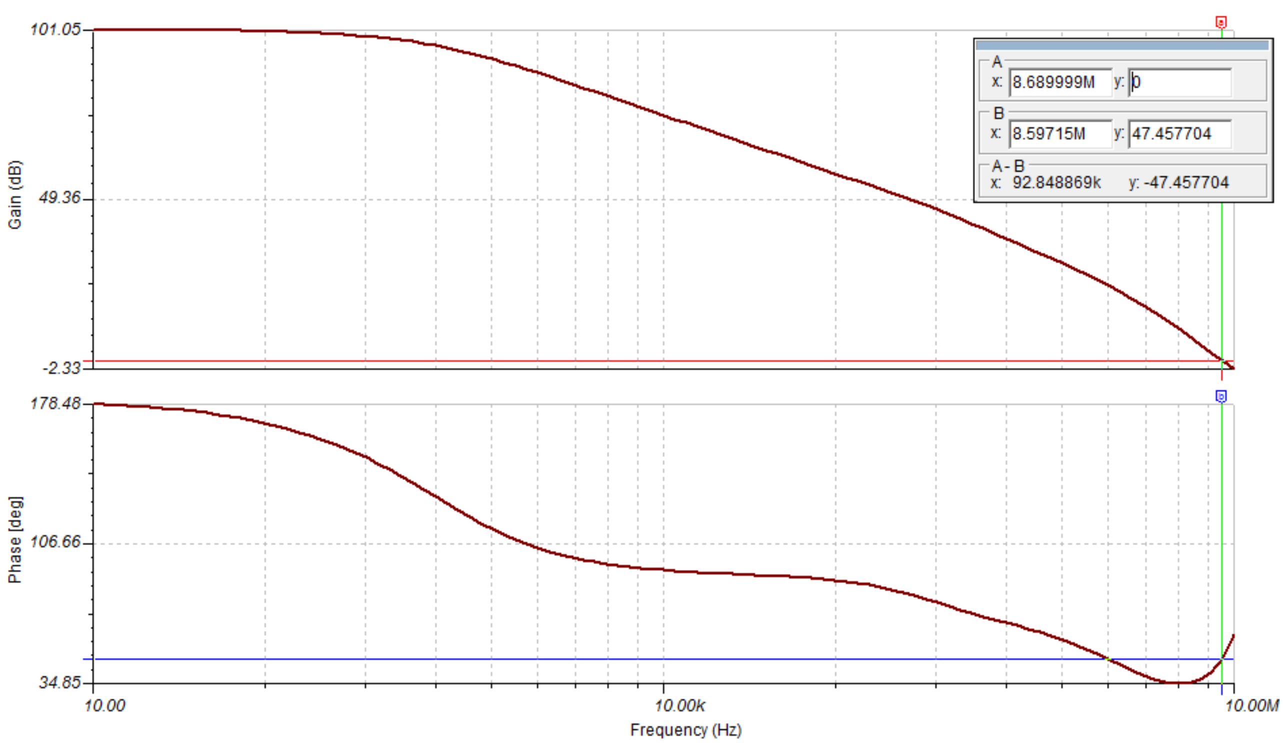

Figure 15: Magnitude and phase response of the difference amplifier loop. The phase margin is 47.46° with a simulated headphone load.

4.4 Stability- Parallel Output Amplifier

The stability of the second amplifier used in parallel with the difference amplifier must also be examined (U2B). This amplifier has both a positive and a negative feedback loop that must be broken for stability analysis. Inductors LT1 and LT2 break the loops, and a differential voltage signal is injected by CT1 and VG1. The loop gain is measured by differential voltage probe AOLB. A differential voltage probe must be used because the net feedback factor is the difference of the positive and negative feedback factors.

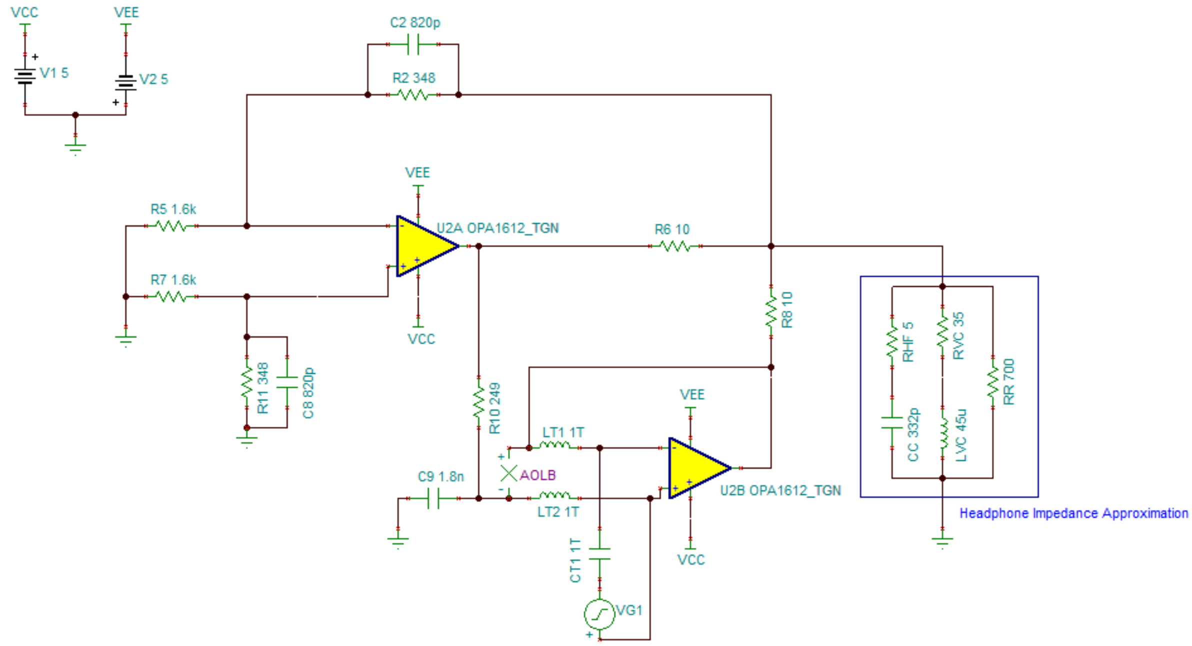

Figure 16: TINA-TI™ schematic for verifying the stability of amplifier U2B.

Unlike many systems, the magnitude of the loop gain for amplifier U2B crosses 0dB at two frequencies: 9.67MHz and 24.82 MHz (Figure 17).

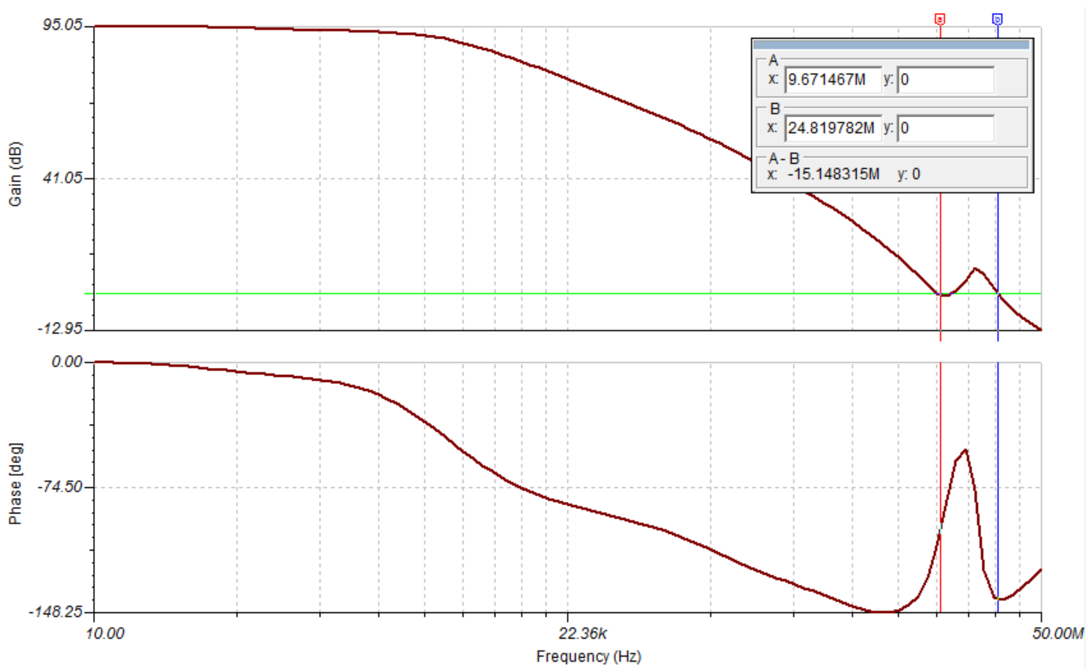

Figure 17: The loop gain magnitude of amplifier U2B crosses 0dB at 2 frequencies.

The phase margin at both 0dB frequencies must be measured to confirm stability. At 9.67MHz the phase margin is 80.2° and at 24.82MHz the phase margin is 40.148°. Both of these values are sufficient for stable operation.

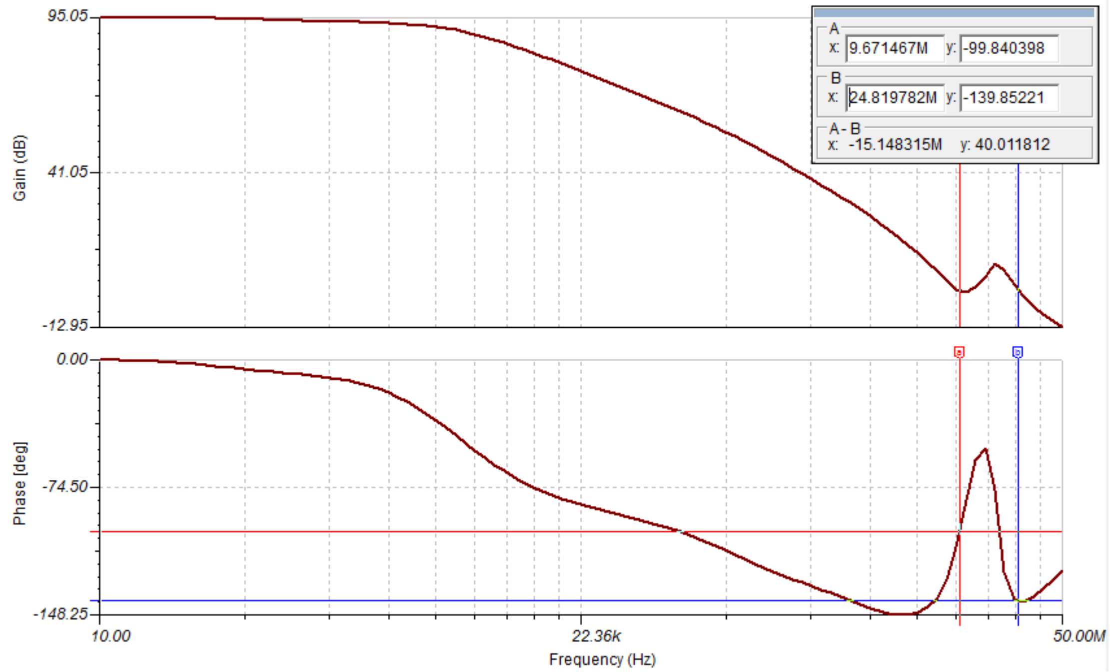

Figure 18: Phase margin measurement at both frequencies where the loop gain is 0dB.

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

The trace lengths in the difference amplifier must be carefully considered in the circuit layout. Recall from section 3.1 that 0.1% resistors were selected in order to maximize the common-mode rejection of the difference amplifier and improve the overall performance of the circuit. The traces used to route signals between these resistors also add resistance, which can degrade the matching between resistors. To maximize circuit performance, the traces from the outputs of the transimpedance amplifier to the difference amplifier should be kept as short as possible and, ideally, of equal length.

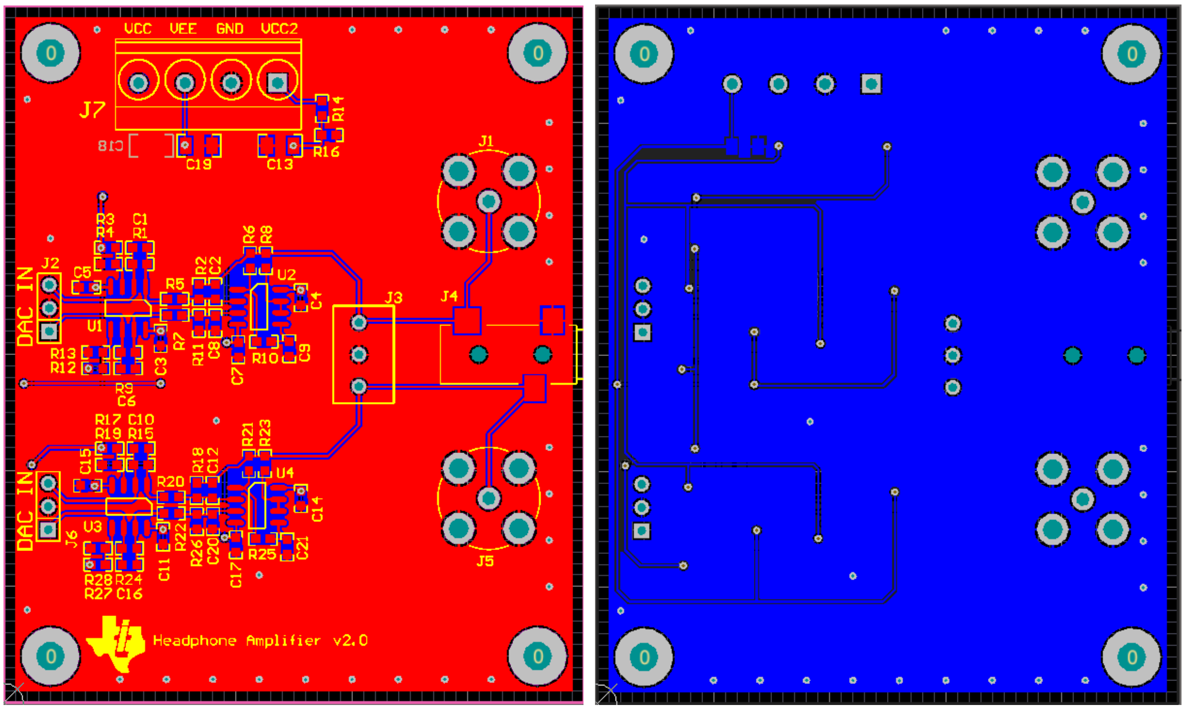

Figure 19: Top layer (left) and bottom layer (right) of the PCB.

6 Verification & Measured Performance

The output of a low-distortion audio analyzer is passed to an OPA1632 fully-differential amplifier in order add a 1.65V common-mode voltage to the signal. This simulates the audio DAC output used for the design calculations. 825 ohm resistors in series with the outputs of the OPA1632 also mimic the DAC output impedance. By operating the OPA1632 in a signal gain of less than 1, some of the noise from the audio analyzer is attenuated, improving the measurement noise floor.

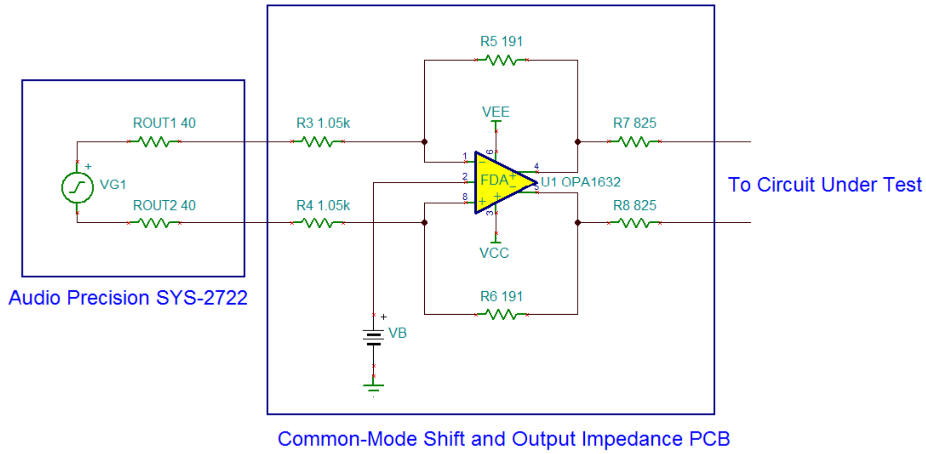

Figure 20: A circuit to adjust the common-mode voltage and output impedance of an audio analyzer.

6.1 Transfer Function

Magnitude Response and Output Impedance

The magnitude response of the headphone amplifier was measured over a bandwidth of 10Hz to 100kHz. At 20kHz, the magnitude response was down 0.007dB.

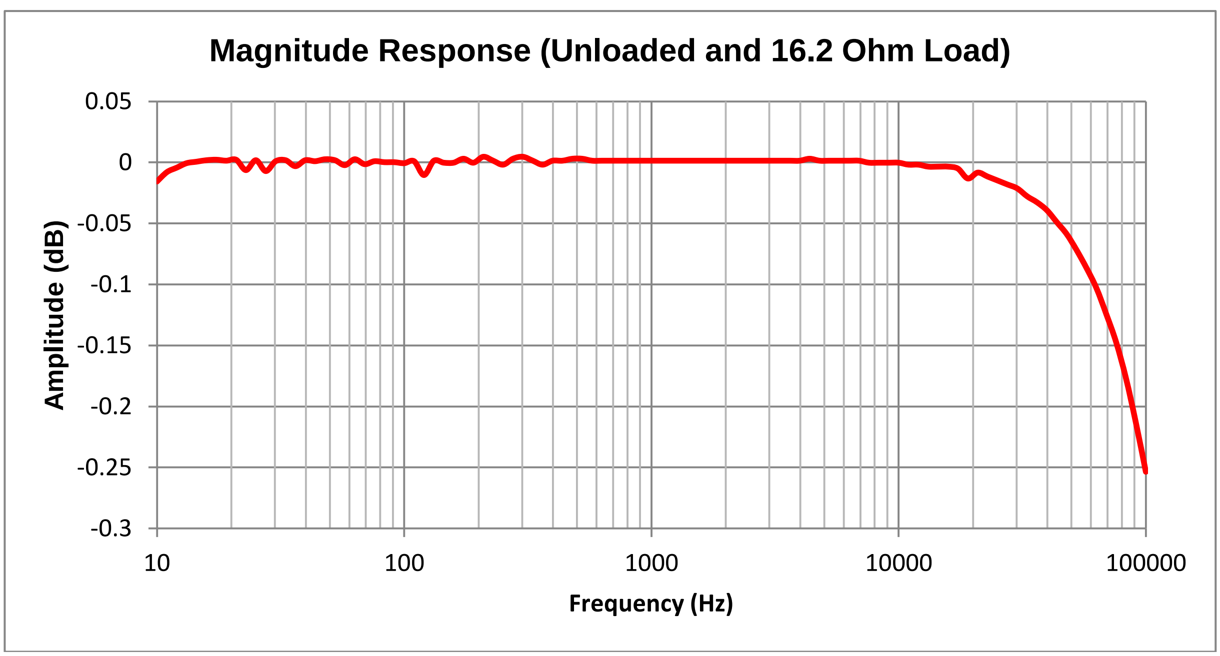

Figure 21: Magnitude response of the headphone amplifier

Phase Response

The phase response was also measured over a bandwidth of 10Hz to 100kHz. At 20kHz the phase has deviated 4.06°.

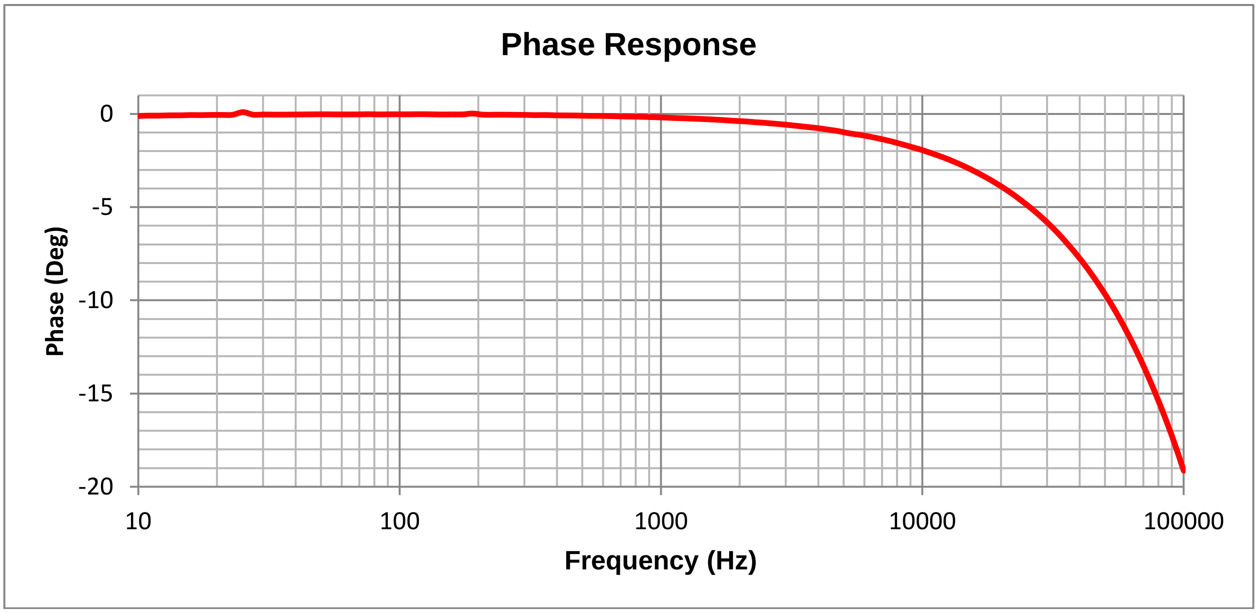

Figure 22: Phase response of the amplifier circuit

6.2 THD+N vs. Output Power

The THD+N versus output power level is shown in Figure 23 for a 1kHz signal. For 10mW of output power, the THD+N is 0.00052% into a 32.4 ohm load, and 0.00078% into a 16.2 ohm load.

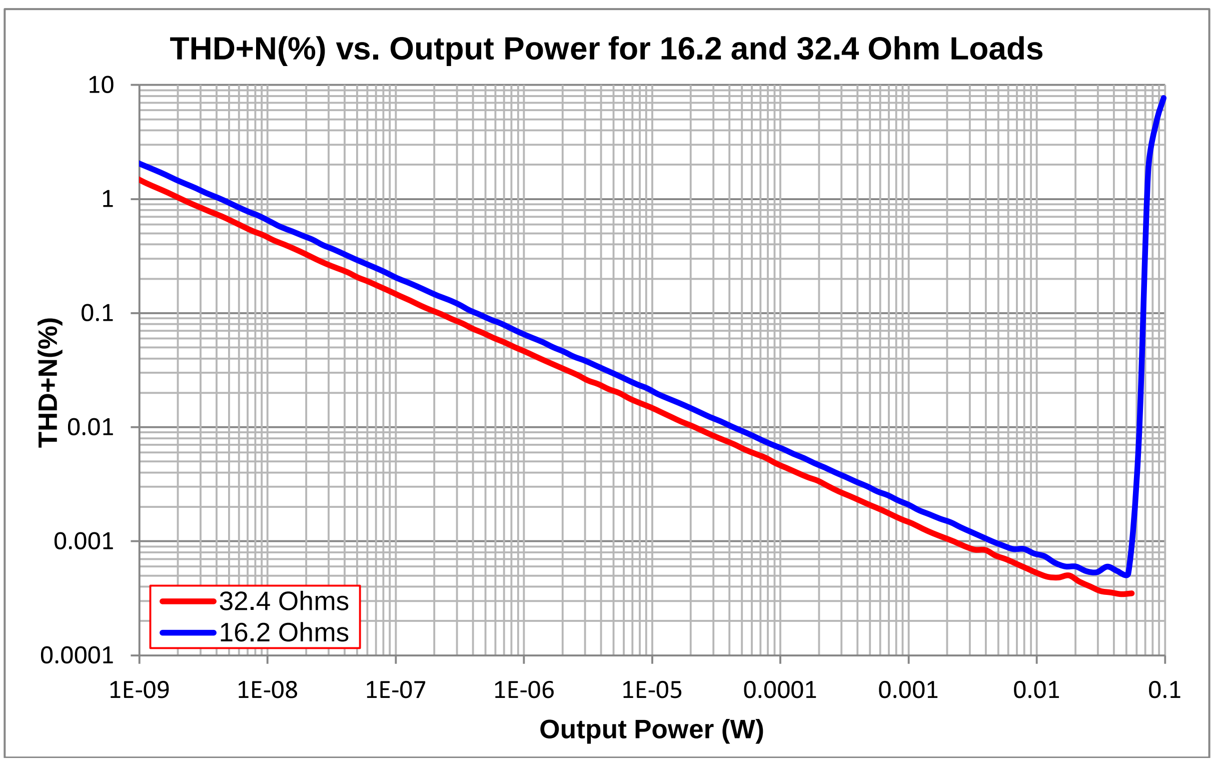

Figure 23: Measured THD+N versus output power (1kHz signal).

The maximum output power into a 32 ohm load is limited by the maximum output voltage of the circuit to 55mW. The THD+N at this output level was 0.00035%. For a 16 ohm load, the maximum output current of the circuit limits the maximum power. The maximum output power before the onset of distortion, into a 16 ohm load, was 51.7mW with a THD+N of 0.00052%.

The constant downward slope of the THD+N vs. Output Power graph indicates that the noise of the circuit is the dominant factor in the THD+N calculation. Therefore, the degraded THD+N measurement for a 16.2 ohm load is not due to additional loading causing distortion. Rather, the smaller output signal voltage required to deliver 10mW into a 16.2 ohm load degrades the signal-to-noise ratio. Also, at these extremely low THD+N levels, the noise of the audio analyzer used for the measurement will affect the result.

6.3 THD+N vs. Frequency

The THD+N was measured from 10Hz to 20kHz at an output power of 10mW into 16.2 and 32.4 ohm loads. At high frequencies the measurement slightly degrades due to the declining open loop gain of the op amp. At 20kHz, the THD+N is 0.0009% for a 32.4 ohm load and 0.0015% for 16.2 ohm loads. The measurement bandwidth was 80kHz.

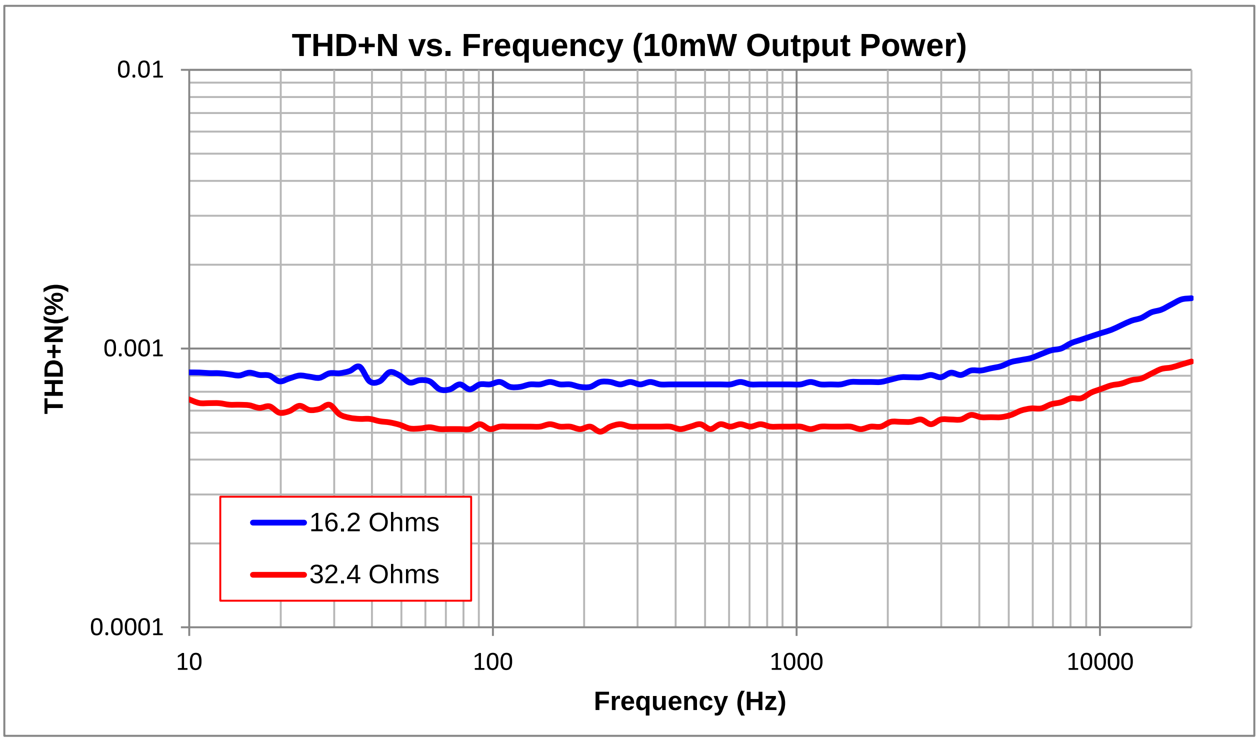

Figure 24: THD+N versus frequency graph for 10mW of output power.

6.4 Output Spectrum

Figure 25 and Figure 26 are Fast Fourier Transforms (FFTs) of the output signal when delivering 10mW at 1kHz to the two different load impedances. Plots such as these are useful for determining which harmonics are largest, which may impact the sound quality perceived by the listener. For the 32.4 ohm load, the 2nd and 3rd harmonics are of similar magnitude , -124.37dB (0.00006%) and -125.05dB (0.000056%) respectively. When the load impedance is decreased to 16.2 ohms, the 2nd harmonic becomes the dominant harmonic with a level of -117.1dB (0.00014%). Spurs visible in the spectrum at frequencies below 1kHz are due to 60Hz mains interference.

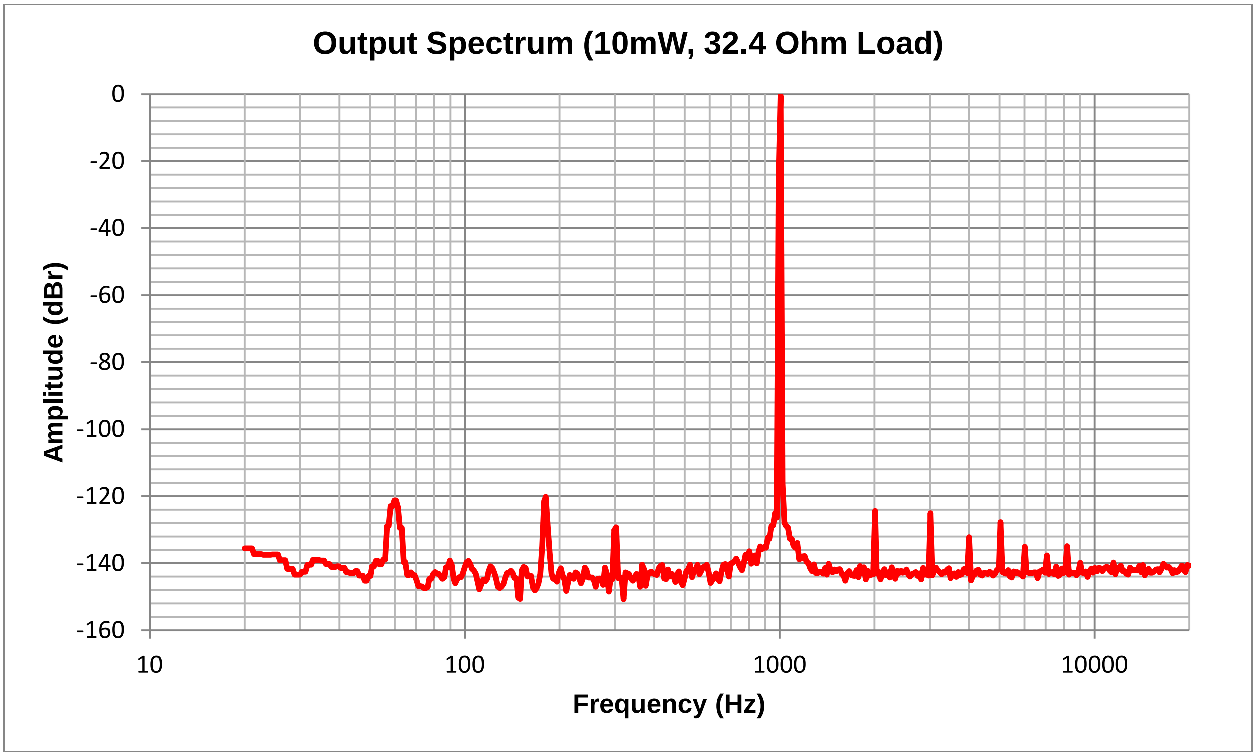

Figure 25: Output spectrum of a 10mW, 1kHz, sine wave into a 32.4 ohm load.

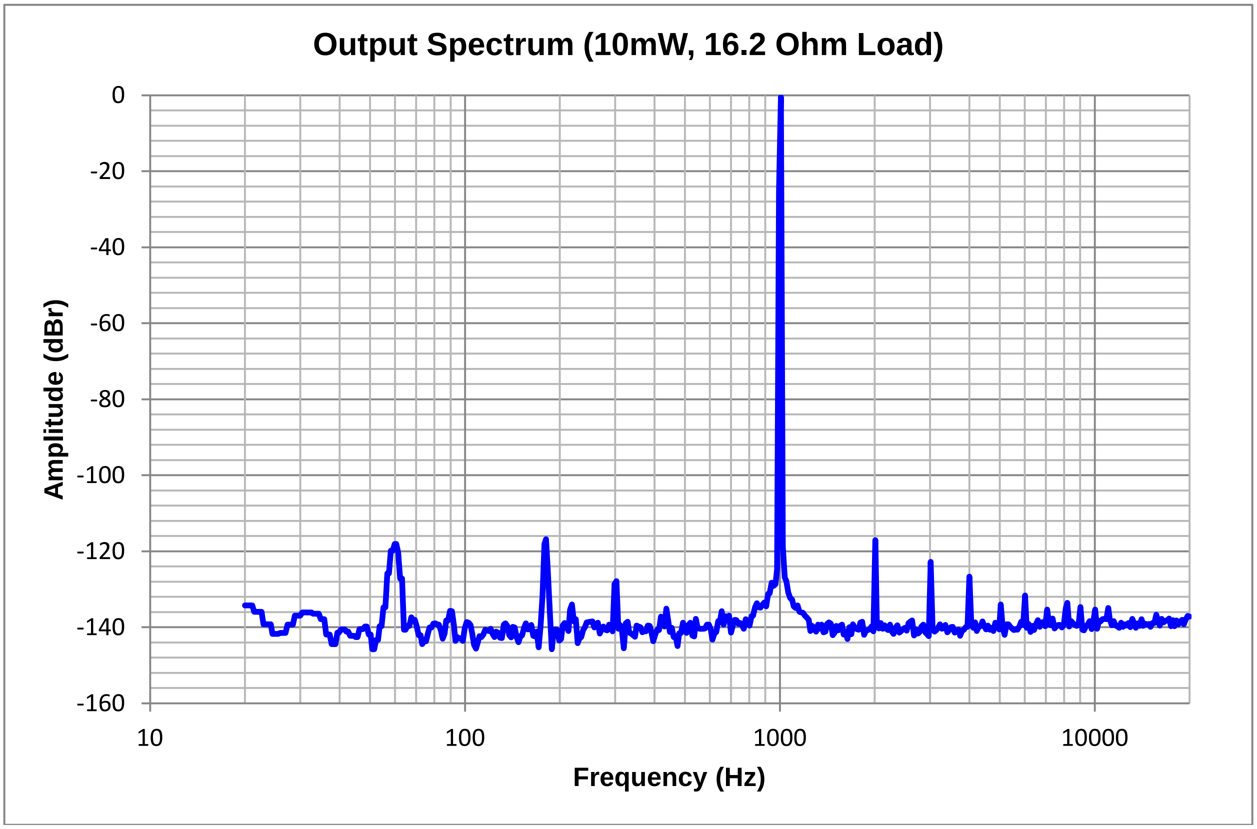

Figure 26: Output spectrum of a 10mW, 1kHz, sine wave into a 16.2 ohm load.

6.5 Verification with Real Headphones

Real headphones are not a resistive load. Over the operating frequency range their impedance may shift between inductive, capacitive, and resistive behavior. This impedance is also modulated by the cone movement and so at any instant in time the impedance of the driver depends on where the voice coil is in its range of motion. The end result is that the current drawn by headphones is not sinusoidal and will produce distortion for headphone amplifier circuits with non-zero output impedance [3]. Therefore, the performance of a headphone amplifier circuit must also be verified using real headphones as a load instead of resistors. A pair of over-the-ear headphones with a 32 ohm nominal impedance were used for testing in this section.

The THD+N was re-measured for increasing output power as shown in Figure 27. At 10mW the THD+N is 0.00053% which is essentially unchanged from the results in Figure 23.

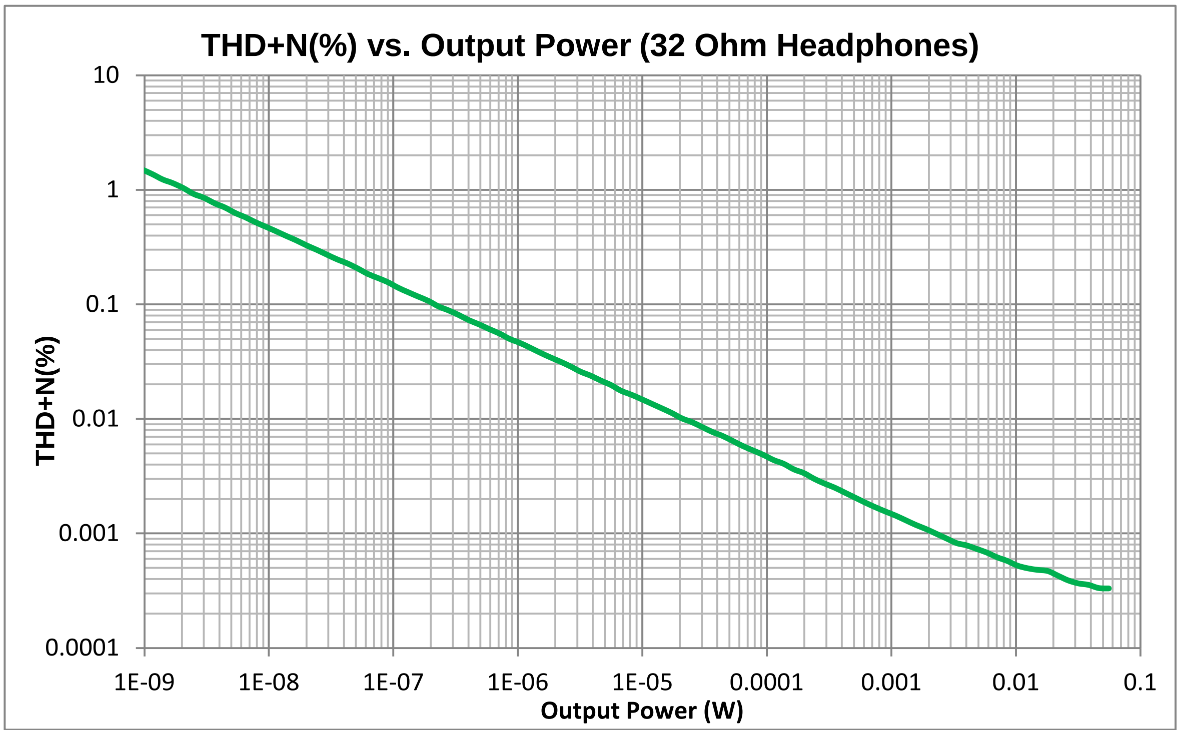

Figure 27: Measured THD+N versus output power in 32 ohm headphones (1kHz signal).

In Figure 28, the THD+N over frequency was measured with 32 ohm headphones as a load. Above 200Hz, the results are unchanged from Figure 24. However, at low frequencies the THD+N increases to a maximum of 0.0048% at 18Hz. At low frequencies, the cone motion of the drivers in the headphones is much larger. Therefore the current waveform in the headphones is much less sinusoidal. Because the output impedance of the headphone circuit is non-zero, the headphone current will produce some distortion. This effect is much larger in headphone amplifiers which have a resistor in series with the output.

Figure 29 shows the output spectrum of a 10mW, 1kHz, sine wave into 32 ohm headphones. Unlike Figure 25, the 3rd harmonic is now the dominant harmonic in the spectrum at -113.98dB (0.0002%).

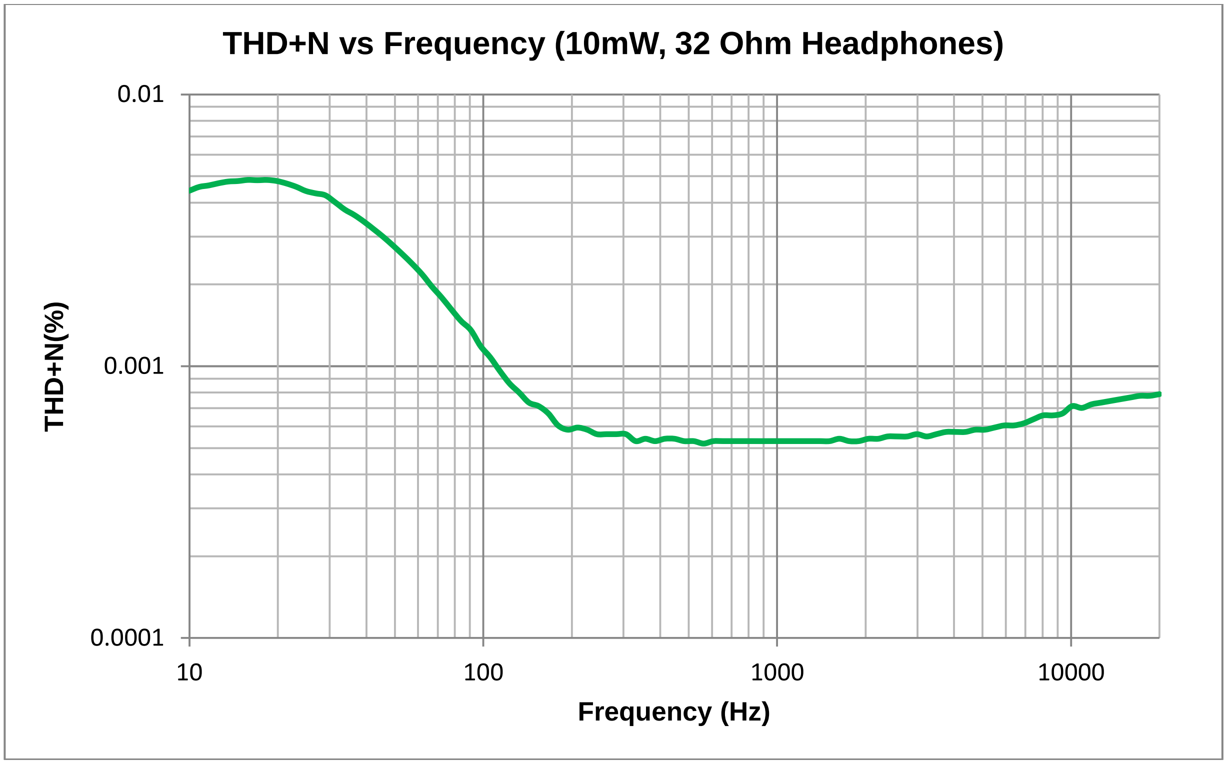

Figure 28: THD+N versus frequency graph for 10mW of output power.

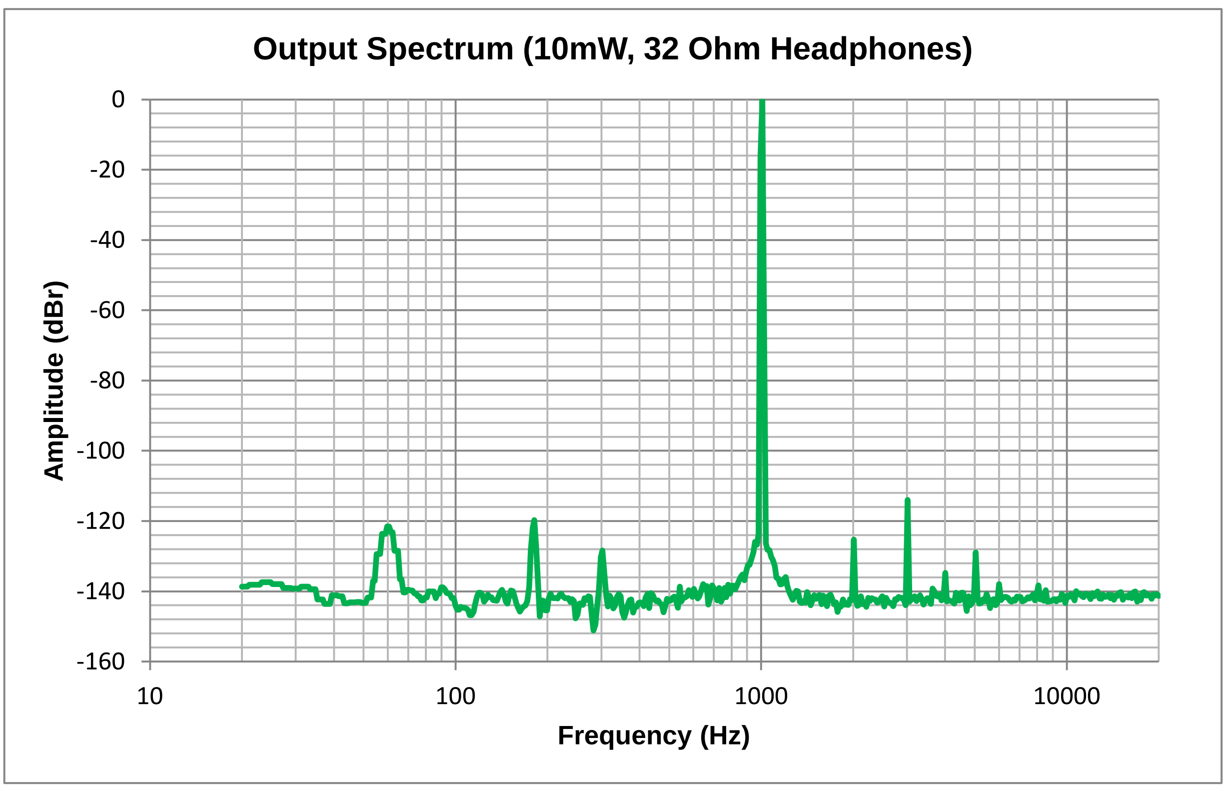

Figure 29: Output spectrum of a 10mW, 1kHz, sine wave into 32 ohm headphones

7 Modifications

A number of modifications can be performed to this schematic in order to reduce cost, or power consumption. Rather than using two op amps in parallel for the output, a single op amp may be used. This will save cost and power consumption, but will sacrifice the amount of output power that can be delivered and will slightly increase distortion (but not noise). Likewise, the OPA1612 may be substituted with many of the op amps in section 3.3 with slightly reduced performance.

8 About the Author

John Caldwell is an applications engineer with Texas Instruments Precision Analog, supporting operational amplifiers and industrial linear devices. He specializes in precision circuit design for sensors, low-noise design and measurement, and electromagnetic interference issues. He received his MSEE and BSEE from Virginia Tech with a research focus on biomedical electronics and instrumentation. Prior to joining TI in 2010, John worked at Danaher Motion and Ball Aerospace.

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3. Siau, John. The Sonic Advantages of Low-Impedance Headphone Amplifiers, http://benchmarkmedia.com/blogs/white-papers/11653109-the-0-ohm-headphone-amplifier, 2001.

Appendix A.

A.1 Electrical Schematic

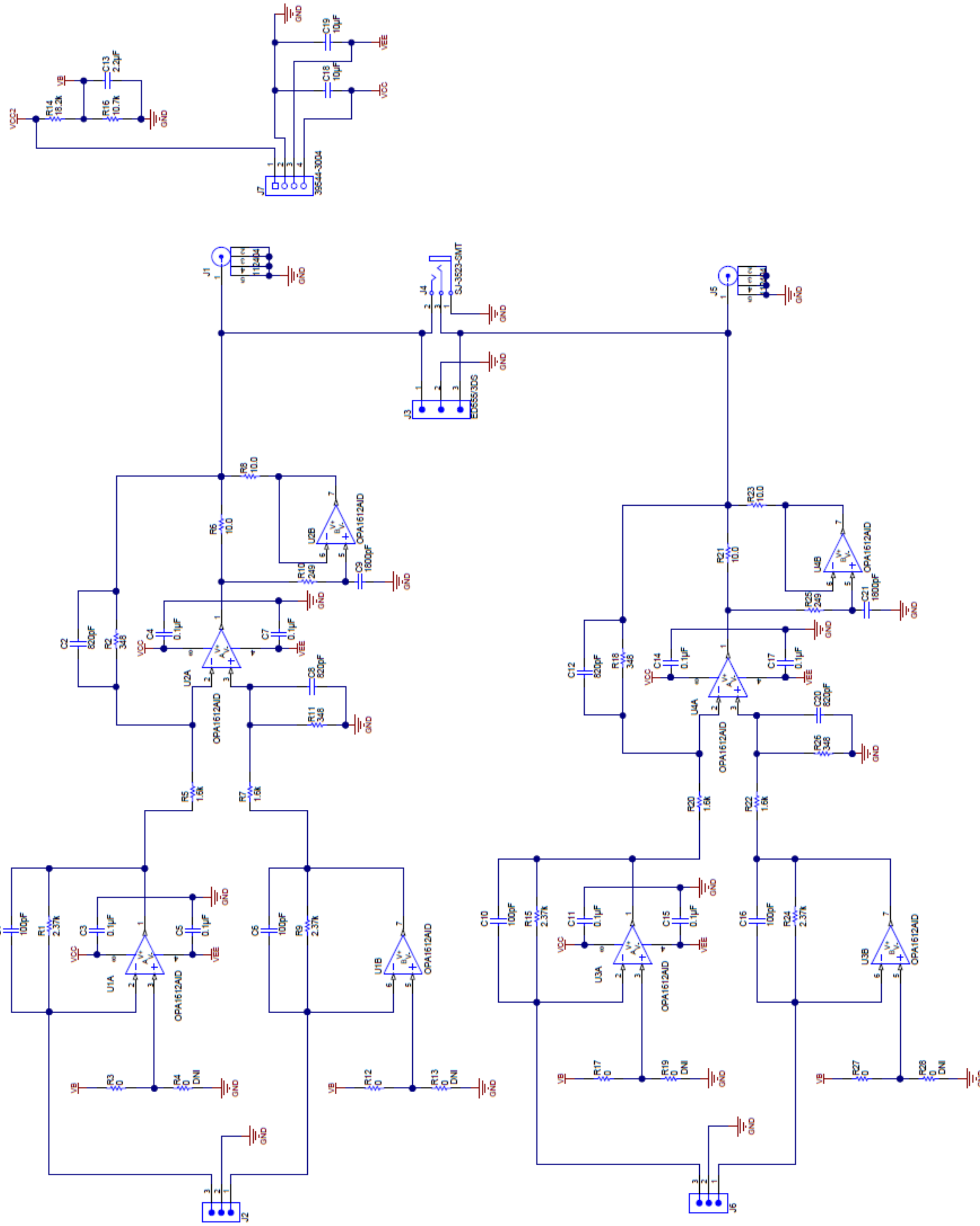

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	Qty	Value	Designator	Description	Manufacturer	Part Number
1	4	100pF	C1, C6, C10, C16	CAP, CERM, 100pF, 25V, +/-10%, X7R, 0603	AVX	06033C101KAT2A
2	4	820pF	C2, C8, C12, C20	CAP, CERM, 820pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A821JAT2A
3	8	0.1uF	C3, C4, C5, C7, C11, C14, C15, C17	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
4	2	1800pF	C9, C21	CAP, CERM, 1800pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H182J
5	1	2.2uF	C13	CAP, CERM, 2.2uF, 25V, +/-10%, X5R, 1206	MuRata	GRM316R61E225KA12D
6	2	10uF	C18, C19	CAP, CERM, 10uF, 16V, +/-20%, X5R, 1206	TDK	C3216X5R1C106M
7	2		J1, J5	Connector, TH, BNC	Amphenol Connex	112404
8	2	1x3	J2, J6	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	Sullins Connector Solutions	PBC03SAAN
9	1		J3	ED555/3DS	On Shore Technology Inc	ED555/3DS
10	1		J4	Connector, Audio Jack, 3.5mm, Stereo, SMD	CUI Inc.	SJ-3523-SMT
11	1		J7	Terminal Block, 4x1, 5.08mm, TH	Molex	39544-3004
12	4	2.37k	R1, R9, R15, R24	RES, 2.37k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06032K37FKEA
13	4	348	R2, R11, R18, R26	RES, 348 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603348RFKEA
14	4	0	R3, R12, R17, R27	RES, 0 ohm, 5%, 0.1W, 0603	Panasonic	ERJ-3GEY0R00V
15	4	1.6k	R5, R7, R20, R22	RES, 1.6k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K60JNEA
16	4	10.0	R6, R8, R21, R23	RES, 10.0 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310R0FKEA
17	2	249	R10, R25	RES, 249 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603249RFKEA
18	1	18.2k	R14	RES, 18.2k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060318K2FKEA
19	1	10.7k	R16	RES, 10.7k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K7FKEA
20	4		U1, U2, U3, U4	Dual Operational Amplifier	Texas Instruments	OPA1612AID

Figure A-2: Bill of Materials

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