Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Title:	**Electronic Circuits I**
Course Number:	**ELE404**
Semester/Year (e.g. F2016)	**W2024**

Instructor:	**Prof. Fei Yuan**
Assignment:	**Design Project**

Due Date	**April 7 2024**
Submission Date	**April 7 2024**

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1. Introduction

The final report of ELE404 is called the Amplifier Design Project as shown in the report below. The project consists of our understanding of using BJTs (Bipolar Junction Transistors) to amplify voltages with multi stage amplifiers with specifications provided. The software used to simulate the circuit was Multisim and the calculations shown are written on a tablet.

2. Objectives

The objective of this project is to design and construct a BJT amplifier that can achieve the required specifications provided below.
Specifications for the circuit are summarized below:

- Power supply: **+10 V** relative to the ground
- Quiescent current drawn from the power supply: no larger than **10 mA**
- **No-load** voltage gain (at 1 kHz): |Avo| = **50 (± 10%)**
- Maximum **no-load output voltage swing** (at 1 kHz): **no smaller than 8 V peak to peak**
- Loaded voltage gain (at 1 kHz and with RL = 1 kΩ): **no smaller than 90% of the no-load voltage gain**
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 kΩ): **no smaller than 4 V peak to peak**

● Input resistance (at 1 kHz): **no smaller than 20 kΩ**

● Amplifier type: **inverting or non-inverting**

● Frequency response: **20 Hz to 50 kHz (−3dB response)**

● Type of transistors: **BJT**

● Number of transistors (stages): **no more than 3**

● Resistances permitted: **values smaller than 220 kΩ** from the **E24 series**

● Capacitors permitted: **0. 1 µF, 1. 0 µF, 2. 2 µF, 4. 7 µF, 10 µF, 47 µF, 100 µF, 220 µF**

● Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE404 lab kit**

3.Summary of Design and Calculations

The design used will be a three stage amplifier with the first stage being a CE, second stage also being a CE and the last stage being a CC leading to a CE-CE-CC layout. With each layout there will be a biasing design with two more resistors being connected to the base node of the BJT where one resistor will be connected to the VCC being 10V and the other being connected to the ground. The reason to add these resistors is to help with the generation of DC biasing voltage at the base of the BJT to make it more stable. The function generator will be used as the source with 1kHz frequency and with that a 600Ω resistor will be connected as source built in resistance as per the requirement as well as the load resistance being 1kΩ. Capacitors will be connected to the start of each stage to block DC current passing through because each stage has a different DC voltage leading to the biasing not being disturbed.

Summary of the values found during calculations are shown below in each table:

R_1	R_2	R_3	R_4	R_5	R_6
210kΩ	40kΩ	172kΩ	40kΩ	33kΩ	200kΩ

Table 1: Biasing Resistor Values

C1	C2	C3	C4
10µF	10µF	10µF	10µF

Table 2: Capacitor Values

RC_1	RC_2	RE_1	RE_2	RE_3
10kΩ	1kΩ	1kΩ	80Ω	600Ω

Table 3: Emitter and Collector Resistor Values

I_B	I_C	β	g_m	r_{BE}
6.26µA	743µA	150	0.0288 S	5.2kΩ

Table 4: CE Stage 1 Important Values

I_B	I_C	β	g_m	r_{BE}
2.88µA	4.3mA	150	0.1538 S	975Ω

Table 5: CE Stage 2 Important Values

I_B	I_C	β	g_m	r_{BE}
119µA	10mA	150	0.3846 S	390Ω

Table 6: CE Stage 3 Important Values

The CE amplifiers being stage 1 and stage 2 will amplify by 10 and 5 respectively and then the CC amplifier will be stage 3 to stabilize the gain and achieve a total of 50 voltage gain. The calculations for each value in the tables are shown below for each stage including R_{in} and many other values needed for each equation which were done on a tablet. The reason for choosing the resistors are shown as well and the assumptions made for the value of resistances were

taken into consideration with previous labs and trial and error in Multisim to achieve the required output. The voltage gain for each is also shown.

Stage 1 : CE Amplifier

Assume $i_C = 750\,\mu A$, $\beta = 150$, $A_V = 10 \Rightarrow A_V = \frac{R_C}{R_E}$, Assume $R_C = 10R_E$

$\therefore g_m = \frac{i_c}{V_t} = \frac{750\times10^{-6}\,A}{26\times10^{-3}\,V} = 0.0288\,S$

$I_B = \frac{I_C}{\beta} = 5\times10^{-6}\,A$

$r_{be} = \frac{\beta}{g_m} = \frac{150}{0.0288\,S} = 5.2k\Omega$

Assume $R_C = 10k\Omega$

$\therefore R_E = \frac{10k\Omega}{10} = 1k\Omega$

KVL @ V_B

$-V_B + R_{E1}I_E + 0.7 = 0$

$V_B = (1000)(755\times10^{-6}) + 0.7$

$V_B = 1.455\,V$

$I_E = I_B + I_C$

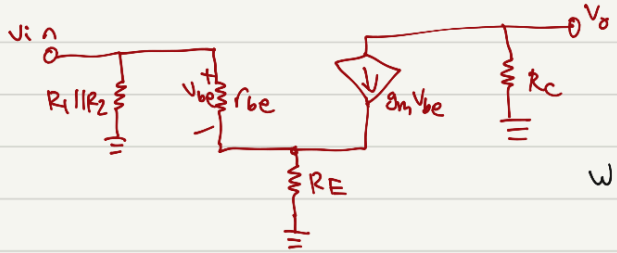
$I_E = (750\times10^{-6} + 5\times10^{-6})A$

$I_E = 755\times10^{-6}\,A$

Voltage Division

$V_B = \left(\frac{R_2}{R_1+R_2}\right)V_{CC} \rightarrow \frac{V_B}{V_{cc}} = \frac{R_2}{R_1+R_2} \rightarrow \frac{R_2}{R_1+R_2} = 0.1455\,V$

Small Signal



$R_C = 10k\Omega$, $R_E = 1k\Omega$

Capacitor C_1 as $10\mu F$ since not needed to be higher with R_1, R_2 being high.

Let $R_1 = 210k\Omega$ since voltage at base should not vary.

KCL @ V_B

$\frac{V_B}{R_2} + \frac{V_B - V_{cc}}{R_1} + I_B = 0$

$\frac{1.455}{R_2} + \frac{1.455-10}{210,000} + (5\mu A) = 0$

$\frac{1.455}{R_2} + (-4.069\times10^{-5} + 5\times10^{-6}) = 0$

$\frac{R_2}{1.455} = -28018.679$

$R_2 \approx 40.767\,k$

$R_2 \approx 40k$

$R_{in} = R_s + [R_1/R_2// r_{be} + (\beta+1)R_{E1}]$

$= 600 + [210k//40k// (5200) + (150+1)(1000)]$

$= 600 + [210k//40k//156.2k]$

$= 600 + 27651.84 = 28251.8441\,\Omega$

Stage 2 : CE Amplifier

Assume $i_C = 4mA$, $\beta = 150$, $A_V = 10 \Rightarrow A_V = \frac{R_C}{R_E}$, Assume $R_C = 10R_E$

$\therefore g_m = \frac{i_c}{V_t} = \frac{4 \times 10^{-3} A}{26 \times 10^{-3} V} = 0.1538\,S$

$I_B = \frac{I_C}{\beta} = 2.67 \times 10^{-5} A$

$r_{be} = \frac{\beta}{g_m} = \frac{150}{0.0288S} = 975\,\Omega$

Assume $R_C = 1k\Omega$

$\therefore R_{E2} = \frac{1k\Omega}{10} = 100\,\Omega$

KVL @ V_B

$-V_B + R_{E2} I_E + 0.7 = 0$

$V_B = (100)(4.027 \times 10^{-3}) + 0.7$

$V_B = 1.103\,V$

$I_E = I_B + I_C$

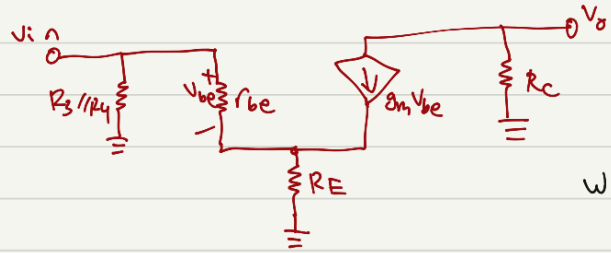
$I_E = 2.67 \times 10^{-5} + 4 \times 10^{-3}$

$I_E = 4.0267 \times 10^{-3} A$

Voltage Division

$V_B = \left(\frac{R_4}{R_3 + R_4}\right) V_{CC} \rightarrow \frac{V_B}{V_{CC}} = \frac{R_4}{R_3 + R_4} \rightarrow \frac{R_4}{R_3 + R_4} = 0.1103$

Small Signal



$R_C = 1k\Omega$, $R_E = 100\Omega$

Capacitor C_2 as $10\mu F$ since not needed to be higher with R_3, R_4 being high.

Let $R_3 = 172k\Omega$ since voltage at base should not vary.

KCL @ V_B

$\frac{V_B}{R_4} + \frac{V_B - V_{CC}}{R_3} + I_B = 0$

$\frac{1.103}{R_4} + \frac{1.103 - 10}{172k\Omega} + 2.67 \times 10^{-5} = 0$

$\frac{1.103}{R_4} = 2.50267 \times 10^{-5}$

$\frac{R_4}{1.103} = 39,957.255$

$R_4 \approx 44072.8523$

$\therefore R_4 \approx 45k\Omega$

Stage 3 : CC Amplifier

Assume $i_c = 10\ mA$, $\beta = 150$ $\quad A_V = 1 = \frac{R_C}{R_E} \Rightarrow R_C = R_E$

$g_m = \frac{i_c}{V_t} = \frac{10 \times 10^{-3}}{26 \times 10^{-3}} = 0.3846\ S$ $\quad I_B = \frac{I_E}{\beta} = 6.67 \times 10^{-5}\ A$

$r_{be} = \frac{\beta}{g_m} = \frac{150}{0.3846\ S} = 390\ \Omega$ $\quad I_E = I_B + I_C$

$I_E = 6.67 \times 10^{-5} + 10 \times 10^{-3}$

$I_E = 0.0100667$

Let $R_C = 600\ \Omega$

$\therefore R_E = 600\ \Omega$

KCL @ V_B

$\frac{V_B}{R_6} + \frac{V_B - V_{CC}}{R_5} + I_B = 0$

Assume $R_5 = 33k\Omega$

$\frac{6.74}{R_6} + \frac{6.74 - 10}{33{,}000} + 6.67 \times 10^{-5} = 0$

$\therefore \frac{R_6}{6.74} = -31164.42\ \Omega \rightarrow R_6 \approx 210k\Omega$

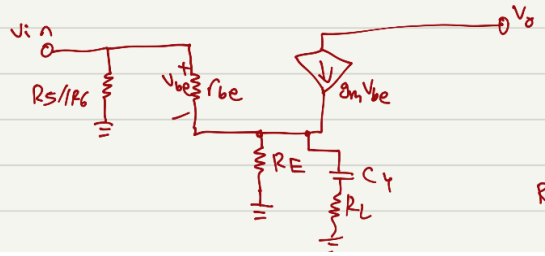
KVL @ V_B

$-V_B + I_E R_E + 0.7 = 0$

$V_B = (10 \times 10^{-3})(600) + 0.7$

$V_B = 6.74\ V$

Small Signal



$C_4 = 10\mu F$

$R_L = 1k\Omega$

$R_E = 600\Omega$

$R_5 // R_6 = 28518.52\ \Omega$

Stage 1: A_{V_1}

$A_{V_1} = \frac{-g_{m_1}(R_{C1} // R_{in2})}{1 + g_{m_1} R_{E_1}}$

$A_{V_1} = \frac{-0.02885\ (10{,}000 // 52564)}{1 + (0.0288)(1000)}$

$A_{V_1} = -3.32976$

Stage 2: A_{V_2}

$A_{V_2} = \frac{-g_{m_2}(R_{C_2} // R_{in3})}{1 + g_{m_2} R_{E_2}}$

$= \frac{-0.1538\ (1000 // 955.76)}{1 + (0.1538)(100)}$

$= \frac{-75.20936}{16.38}$

$A_{V_2} = -4.592$

4. Circuit Design

Figure 1 shows the final design of the BJT amplifier in 3 stages that is simulated with Multisim. It consists of 3 BJTs that are 2N3904, 7 resistors, and 4 electrolytic capacitors. Vcc is 10V that is controlled by the source voltage. **Figure 2a** shows the built circuit in Multisim without load while **Figure 2b** shows the circuit with load.

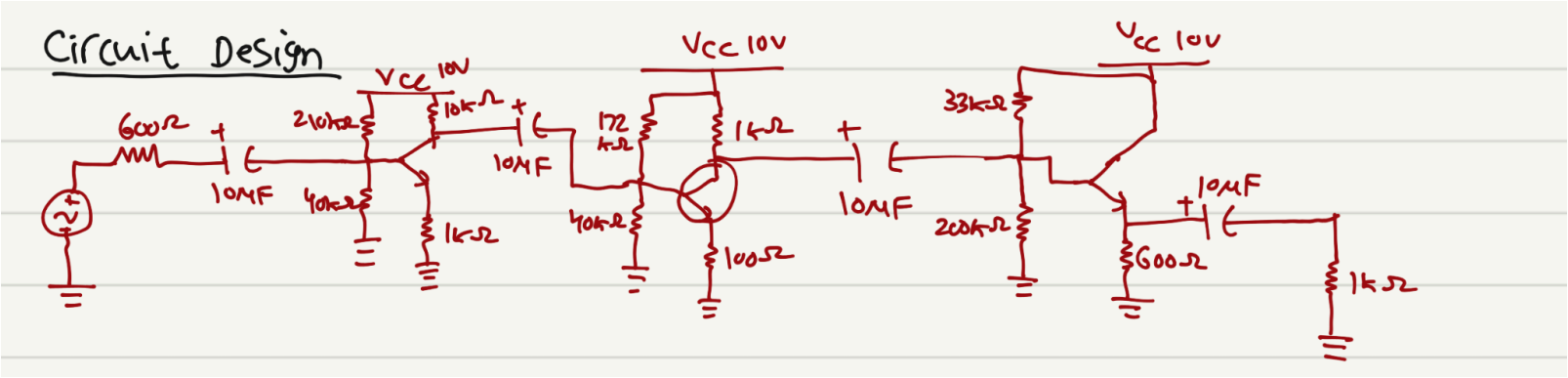


Figure 1: The rough circuit design done on tablet

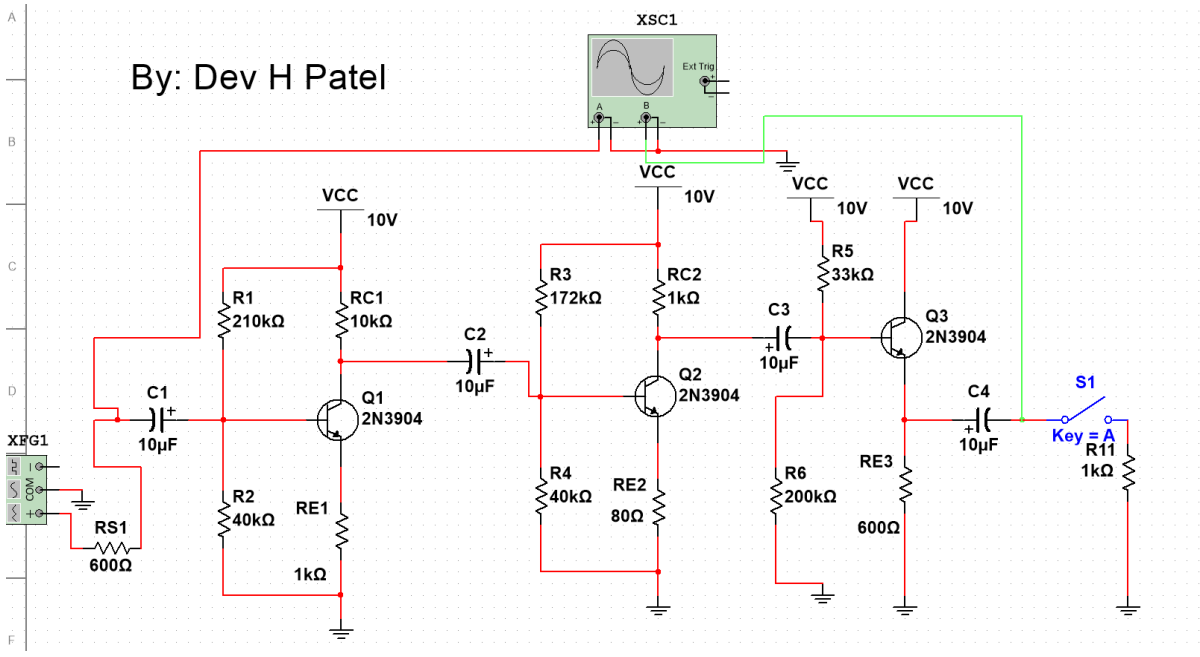


Figure 2a: The Multisim circuit made from **Figure 1** with the circuit having no load

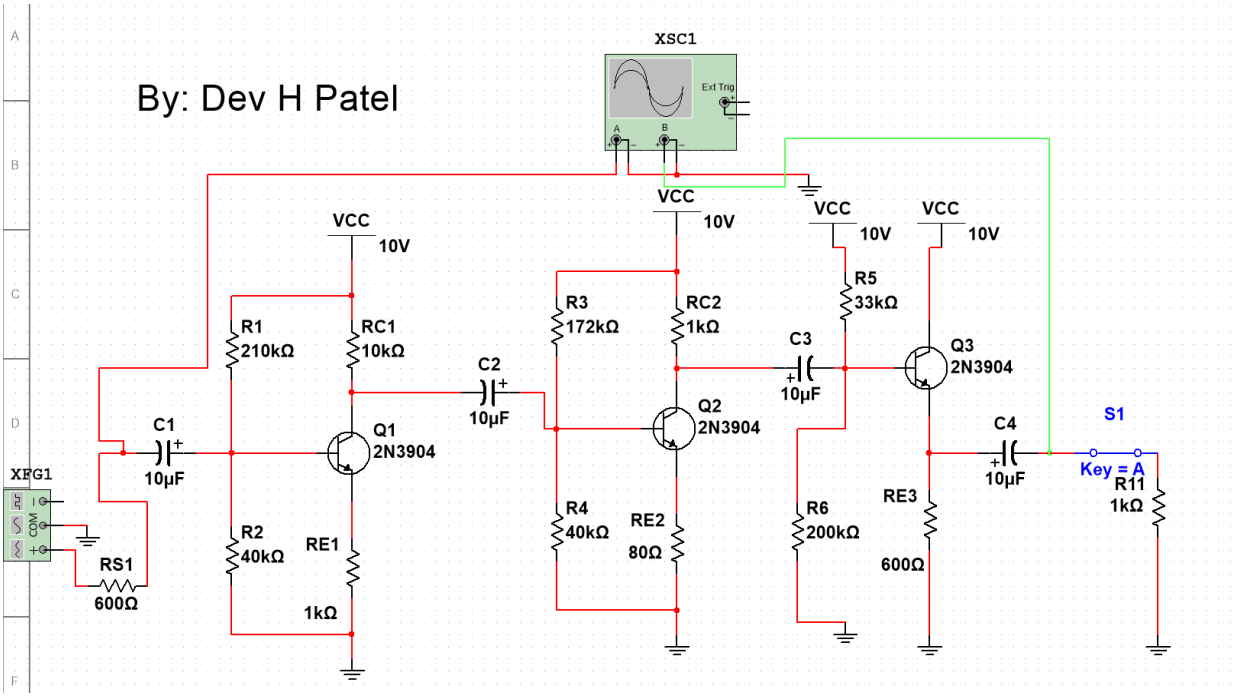


Figure 2b: The Multisim circuit made from **Figure 1** with the circuit having load

5. Experimental Results

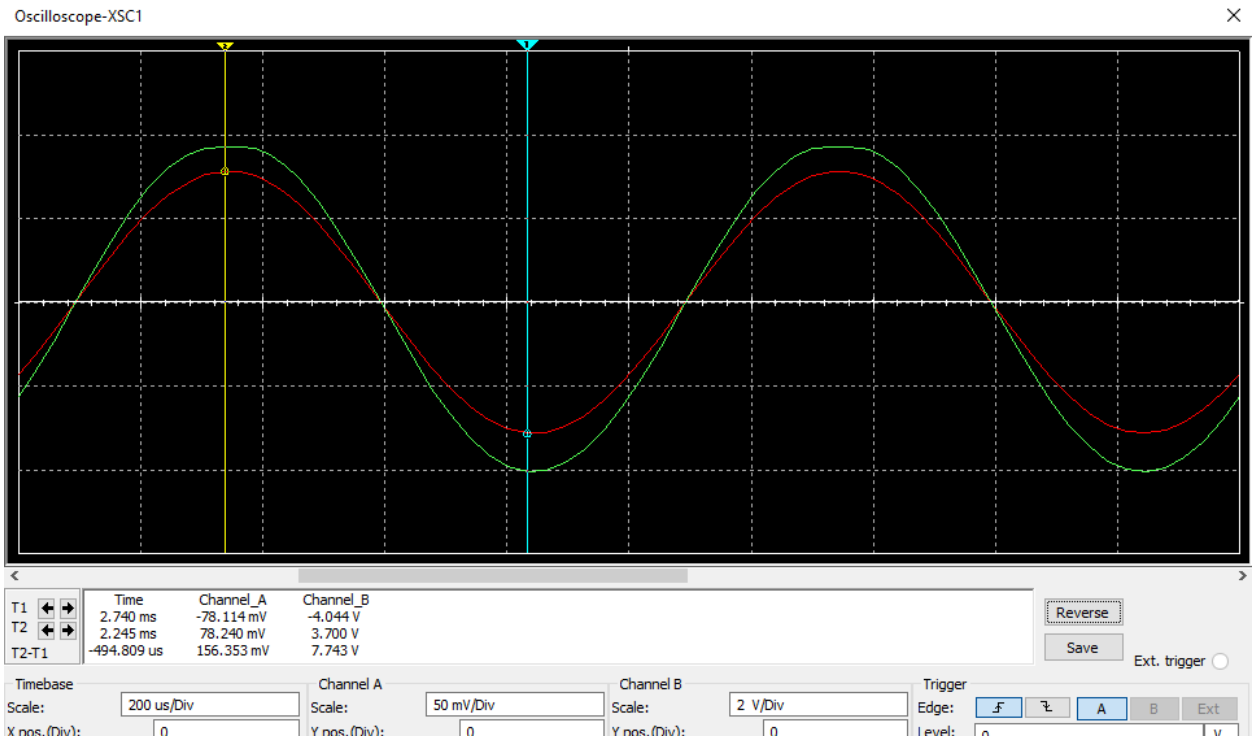


Figure E1: Graph of input and output voltage of **Figure 2a** where no load is connected

$V_{O\ p\text{-}p}$ [V]	$V_{I\ p\text{-}p}$ [V]	A_{vo} [V/V]
7.75	156 mV	49.68

Table E1: Values of **Figure 2a** where no load is connected where f=1kHz and RL = ∞

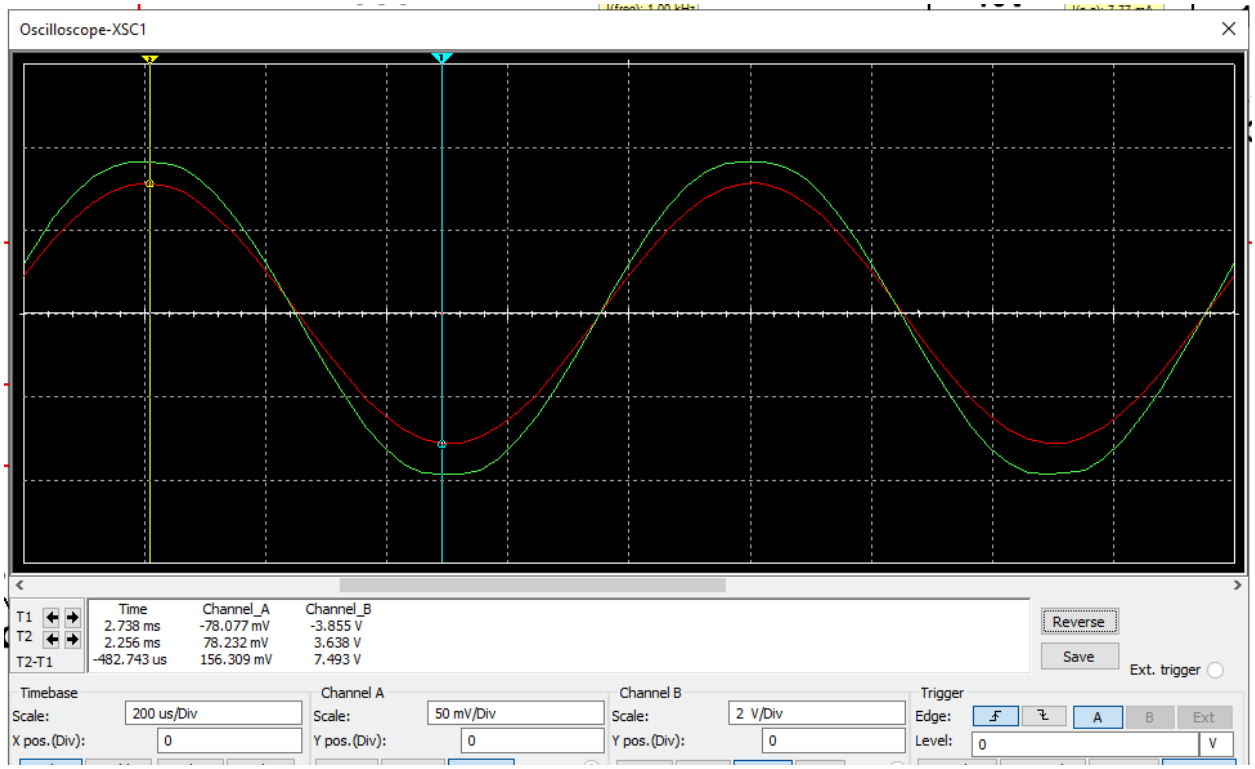


Figure E2: Graph of input and output voltage of **Figure 2b** where a load is connected

$V_{O\ p\text{-}p}$ [V]	$V_{I\ p\text{-}p}$ [V]	A_{v} [V/V]
7.51	157 mV	47.83

Table E2: Values of **Figure 2b** where no load is connected where f=1kHz and RL = 1kΩ

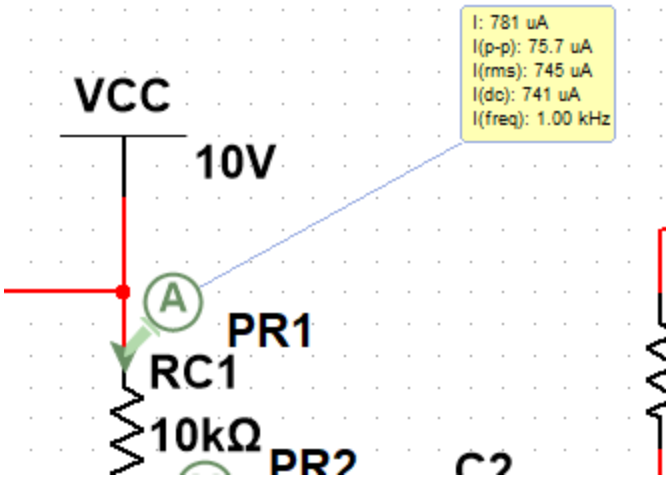


Figure E3: Quiescent current drawn from the power supply

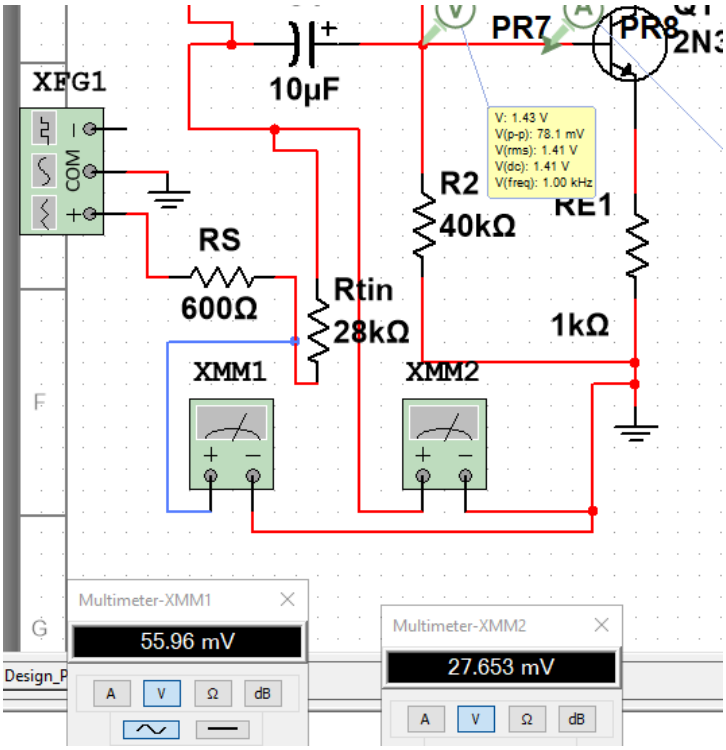


Figure E4: Values for V_t and V_i with $R_{t,in}$

$$R_i = R_{t,in}\left(\frac{v_i}{v_t - v_i}\right)$$

R_i (Calculated) (kΩ)	$R_{t,\,in}$ (kΩ)	V_t (rms)	V_i (rms)	R_i (kΩ)
28.25	28	55.96 mV	27.653 mV	27.35

Table E3: Values used to find R_{in}

6. Conclusion and Remarks

$$e\% = \frac{calculated\ value - measured\ value}{measured\ value} \times 100$$

Specification	Calculated	Measured	% Error	Success
Quiescent current: no larger than 10 mA;	750 µA	753 µA	0.40	Yes
|Avo| = 50 (± 10%);	50	49.68	0.64	Yes
Maximum no-load output voltage swing	8V	7.75V	3.23	Yes
Loaded voltage gain: **no smaller than 90% of Avo**	45	47.83	5.92	Yes
Maximum loaded output voltage swing	7V	7.53V	7.04	Yes
Input resistance: **no smaller than 20 kΩ**;	28.25kΩ	27.35kΩ	3.29	Yes

The specifications were all met for the design with all the percent errors being under 10%. The multisim values seem to be off by the calculated values due to the fact that the resistors had to be changed in each stage to achieve the specifications required. This happened due to the biasing or how the assumptions were made for some resistors in order to achieve the specifications required meaning those estimations caused this error but they were still met with minor errors. The calculations were also off, maybe due to rounding errors. Therefore, the format of a CE-CE-CC design was successful meeting the specifications included in the manual and calculations were all effective to the final goal.

7. References

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[1] Dept. of Electrical, Computer, & Biomedical Eng, “Design Project” Toronto Metropolitan University, Toronto