Digital Receiver Design Report

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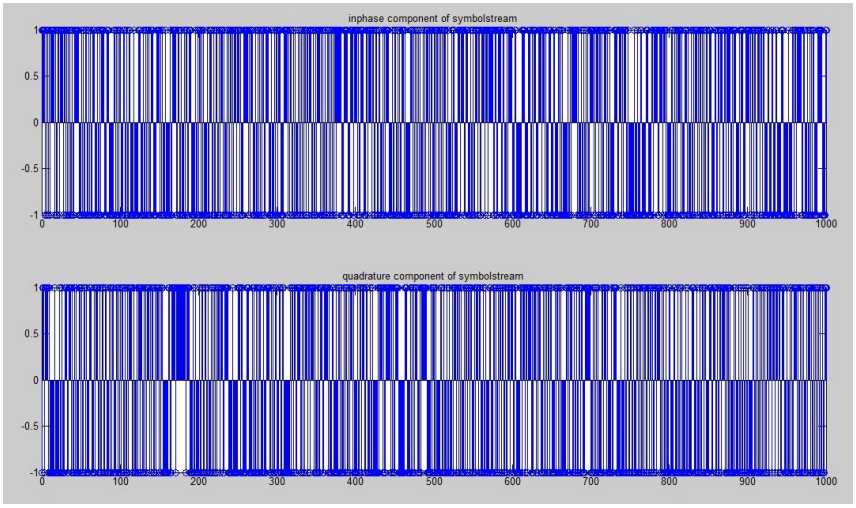
To design the digital receiver, the first component is Analog-to-Digital Converter. It not only produces a sampled-time version of the continuous-time signal but also quantizes the amplitude so that latter operations are based on discrete-time processing.

In order to design the receiver digitally, I first focus on two components: carrier phase synchronizer and symbol timing synchronizer. Analog version of carrier phase synchronizer uses adjusted quadrature sinusoids by downconverting received signal and using a carrier phase PLL to compensate the phase error to sinusoids. However, another solution uses fixed frequency quadrature sinusoids and phase compensation is performed at the output of matched filter with "CCW Rotation". As the sampled matched filter outputs form a discrete-time sequence, this approach is purely discrete-time approach.

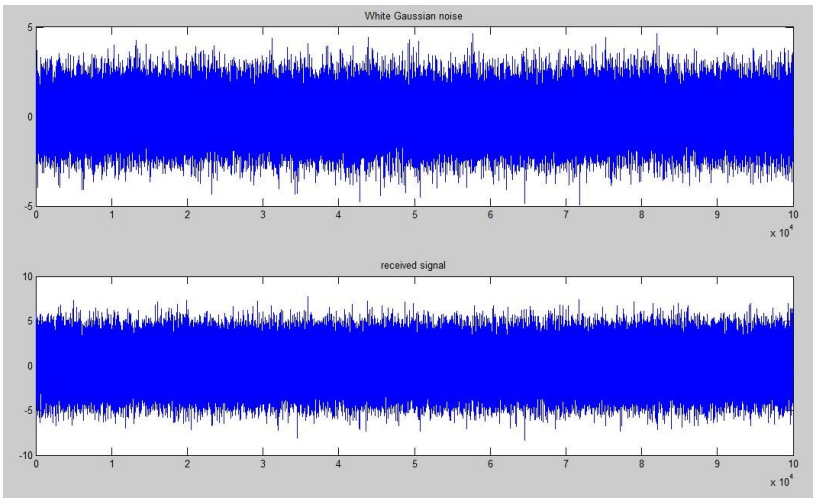
Moreover, analog version of symbol timing synchronizer intends to produce a clock signal aligned with the data transitions so it uses a symbol timing PLL consisting of timing error detector, loop filter and voltage controlled clock. But for digital version, the goal is to produce N samples at the matched filter outputs during each symbol interval such that one of the samples is aligned with maximum eye opening. Simply converting continuous-time processing to discrete-time processing by sampling will lead to problems like hardware overhead for feedback path, transport delay of matched filter reducing response time of the timing recovery loop and higher level of phase noise contributed by VCC. So I use another method which addresses these issues by sampling the received signal at a fixed rate that is asynchronous with the symbol rate and estimating the time delay solely from the asynchronous samples at the output matched filter. The symbol timing synchronizer will move the samples to the desired time instants by interpolator and interpolation control.

In the simulation, I use 4QAM modulation, 1000 symbols, symbol length T of 1s, carrier frequency 10Hz, sampling rate of 100 samples/symbol, raised cosine pulse as shaping pulse, white Gaussian noise with power of 1dB, quantization with 3 bits partitioning and initial carrier phase offset of 30 degree. The results are as follows:

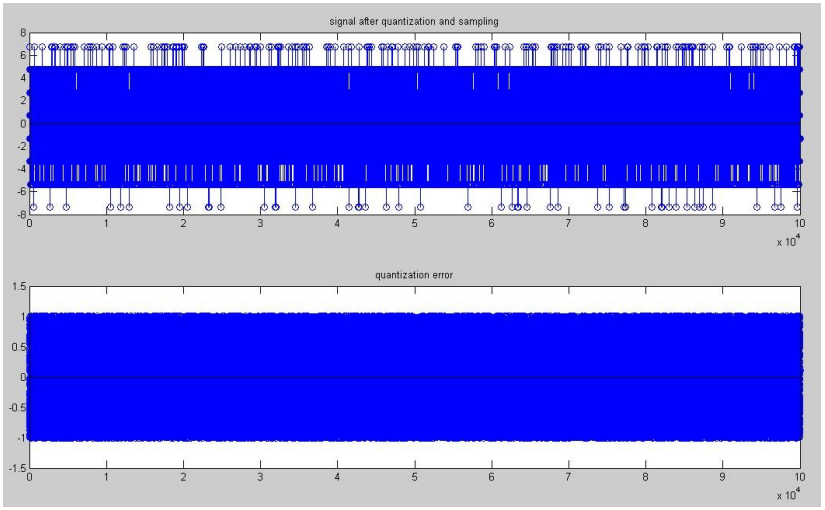
1. Symbolstream:



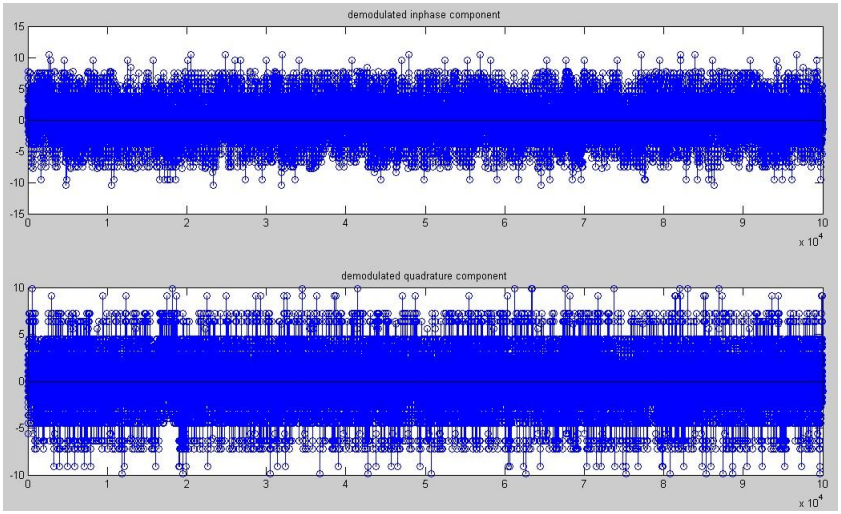
2. Noise and received signal:



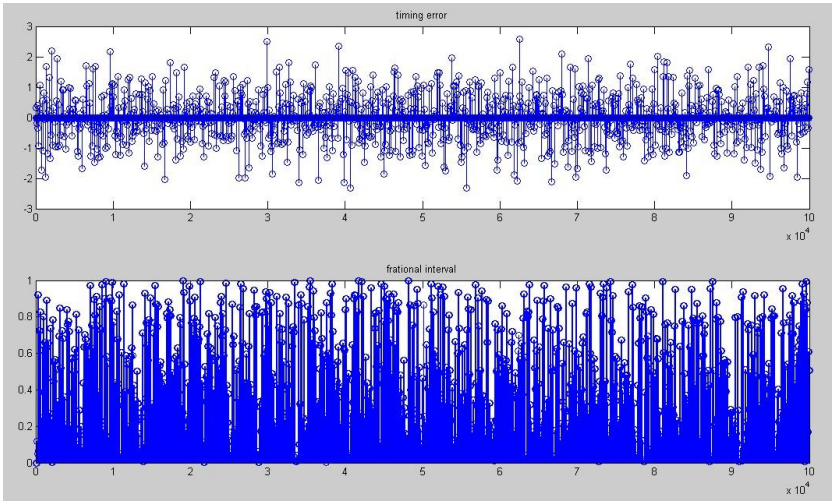
3. Quantization and sampling:

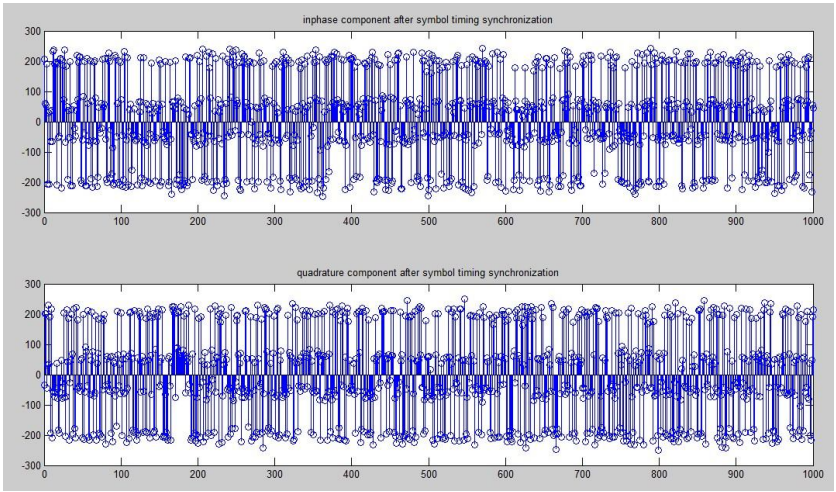


4. Demodulation:

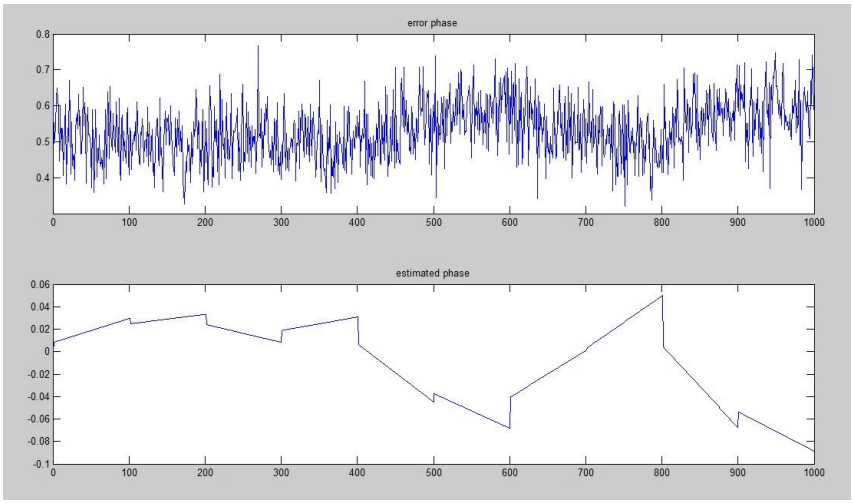


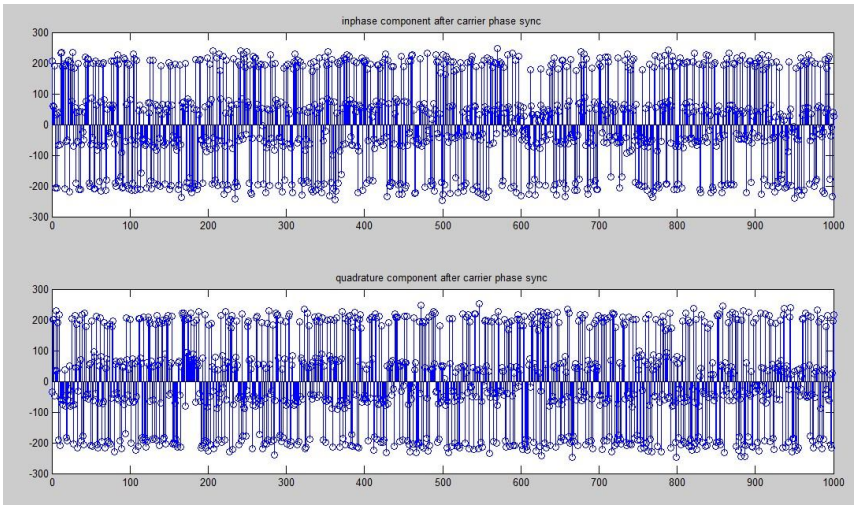
5. Symbol timing synchronization:



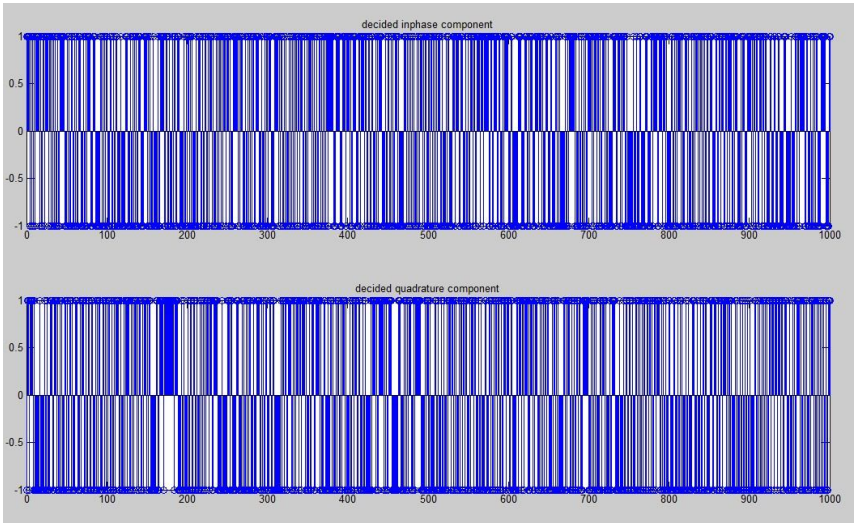


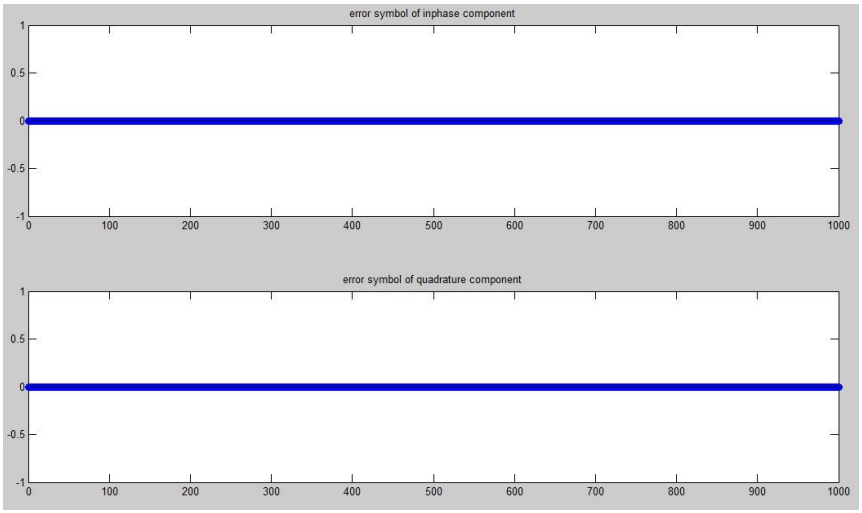
6. Carrier phase synchronization:





7. Final decision and error symbol:




error symbol of inphase component
1
0.5
0
-0.5
-1
0
100
200
300
400
500
600
700
800
900
1000
error symbol of quadrature component
1
0.5
0
-0.5
-1
0
100
200
300
400
500
600
700
800
900
1000