LSE – FIUBA – Arquitectura de uC

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  Memory Protection Unit (MPU)

Memory Protection Unit (MPU)

- Es un periférico opcional para CM3 y CM4.
- Se puede dividir el mapa de memoria en 8 regiones, con diferentes privilegios de acceso.
- Previene que las aplicaciones de usuario corrompan datos utilizados por el SO u otras aplicaciones.
- Lo mismo se aplica a los periféricos.
- Detecta accesos inesperados, como por ejemplo stack overflows.

Mapa de memoria

Table 3. LPC176x/5x memory usage and details

Address range	General Use	Address range details and description	
0x0000 0000 to 0x1FFF FFFF	On-chip non-volatile memory	0x0000 0000 - 0x0007 FFFF	For devices with 512 kB of flash memory.
		0x0000 0000 - 0x0003 FFFF	For devices with 256 kB of flash memory.
		0x0000 0000 - 0x0001 FFFF	For devices with 128 kB of flash memory.
		0x0000 0000 - 0x0000 FFFF	For devices with 64 kB of flash memory.
		0x0000 0000 - 0x0000 7FFF	For devices with 32 kB of flash memory.
	On-chip SRAM	0x1000 0000 - 0x1000 7FFF	For devices with 32 kB of local SRAM.
		0x1000 0000 - 0x1000 3FFF	For devices with 16 kB of local SRAM.
		0x1000 0000 - 0x1000 1FFF	For devices with 8 kB of local SRAM.
	Boot ROM	0x1FFF 0000 - 0x1FFF 1FFF	8 kB Boot ROM with flash services.
0x2000 0000 to 0x3FFF FFFF	On-chip SRAM (typically used for peripheral data)	0x2007 C000 - 0x2007 FFFF	AHB SRAM - bank 0 (16 kB), present on devices with 32 kB or 64 kB of total SRAM.
		0x2008 0000 - 0x2008 3FFF	AHB SRAM - bank 1 (16 kB), present on devices with 64 kB of total SRAM.
	GPIO	0x2009 C000 - 0x2009 FFFF	GPIO.
0x4000 0000 to 0x5FFF FFFF	APB Peripherals	0x4000 0000 - 0x4007 FFFF	APB0 Peripherals, up to 32 peripheral blocks, 16 kB each.
		0x4008 0000 - 0x400F FFFF	APB1 Peripherals, up to 32 peripheral blocks, 16 kB each.
	AHB peripherals	0x5000 0000 - 0x501F FFFF	DMA Controller, Ethernet interface, and USB interface.
0xE000 0000 to 0xE00F FFFF	Cortex-M3 Private Peripheral Bus	0xE000 0000 - 0xE00F FFFF	Cortex-M3 related functions, includes the NVIC and System Tick Timer.

MPU Type Register

Table 3. Region attribute and size registers

Field	Name	Description
[28]	XN	Instruction access disable bit, 1= disable instruction fetches.
[26:24]	AP	Data access permissions, allows you to configure read/write access for User and Privileged mode.
[21:19]	TEX	Type extension field, allows you to configure memory access type, for example strongly ordered, peripheral.
[18]	S	Shareable.
[17]	C	Cacheable.
[16]	B	Bufferable.
[15:8]	SRD	Sub-region disable field (see *Sub-regions*).
[5:1]	REGION SIZE	Region size of the region be configured, for example 4K, 8K.
[0]	SZENABLE	Region enable bit.

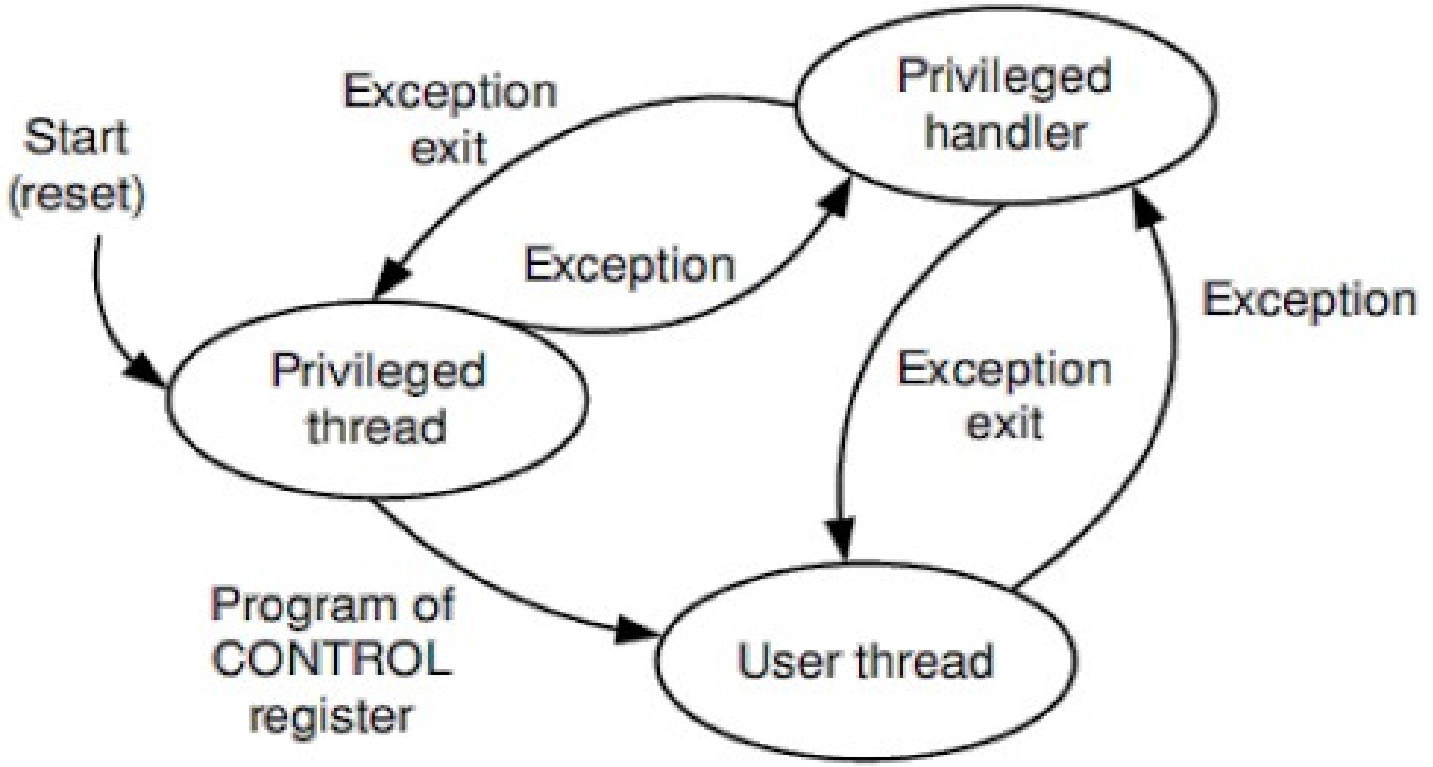
Valores posibles del registro de permisos

Table 4.47. AP encoding

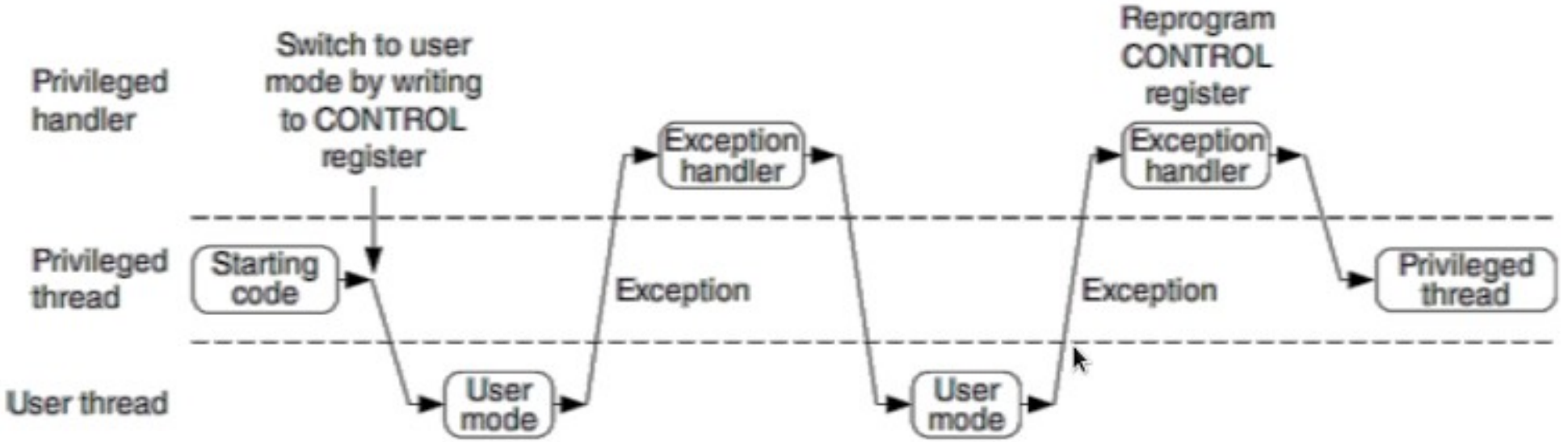
AP[2:0]	Privileged permissions	Unprivileged permissions	Description
000	No access	No access	All accesses generate a permission fault
001	RW	No access	Access from privileged software only
010	RW	RO	Writes by unprivileged software generate a permission fault
011	RW	RW	Full access
100	Unpredictable	Unpredictable	Reserved
101	RO	No access	Reads by privileged software only
110	RO	RO	Read only, by privileged or unprivileged software
111	RO	RO	Read only, by privileged or unprivileged software

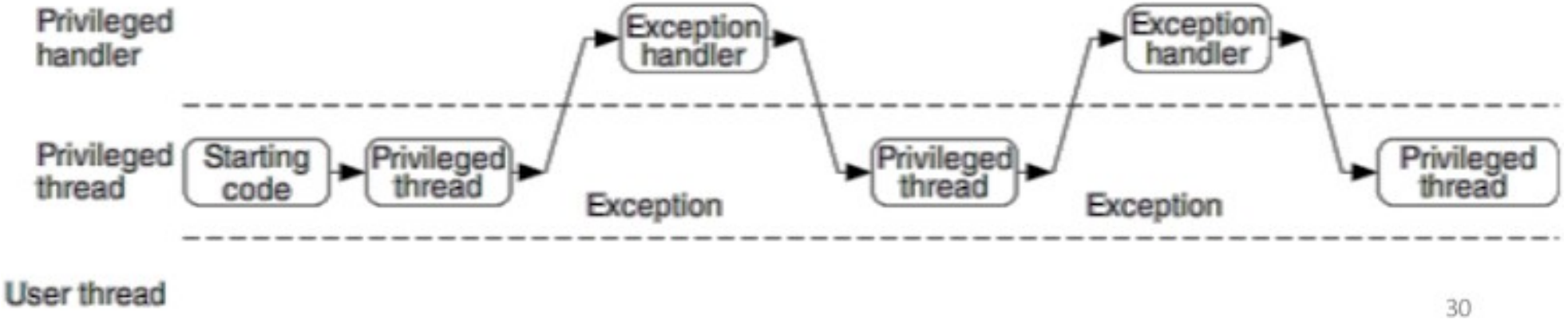
Modos de Operación

	Privileged	*User*
When running an exception handler	Handler mode	
When not running an exception handler (e.g., main program)	Thread mode	Thread mode



Modos de Operación - Ejemplos



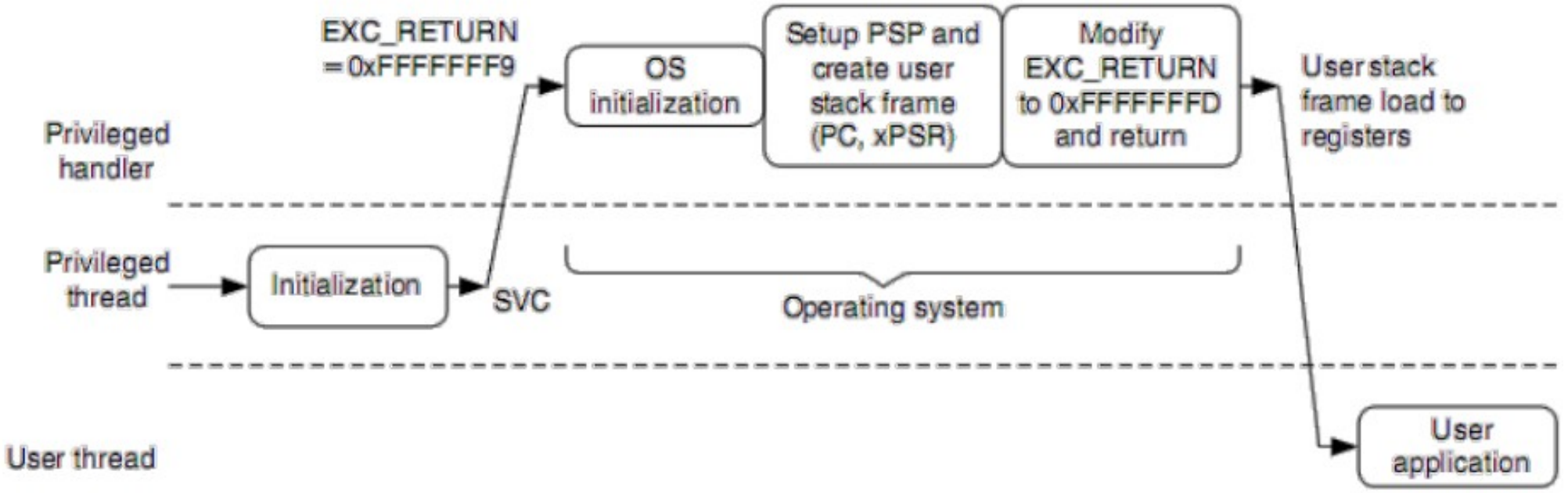


Excepciones

Exception Number	Exception Type	Priority (Default to 0 if Programmable)	Description
0	NA	NA	No exception running
1	Reset	–3 (Highest)	Reset
2	NMI	–2	NMI (external NMI input)
3	Hard fault	–1	All fault conditions, if the corresponding fault handler is not enabled
4	MemManage fault	Programmable	Memory management fault; MPU violation or access to illegal locations
5	Bus fault	Programmable	Bus error (prefetch abort or data abort)
6	Usage fault	Programmable	Program error
7–10	Reserved	NA	Reserved
11	SVCall	Programmable	Supervisor call
12	Debug monitor	Programmable	Debug monitor (break points, watchpoints, or external debug request)
13	Reserved	NA	Reserved
14	PendSV	Programmable	Pendable request for system service
15	SYSTICK	Programmable	System tick timer
16	IRQ #0	Programmable	External interrupt #0
17	IRQ #1	Programmable	External interrupt #1
...	...	...	...
255	IRQ #239	Programmable	External interrupt #239

Ejemplos Avanzados

- Inicializando un Sistema Operativo en un Cortex-M3

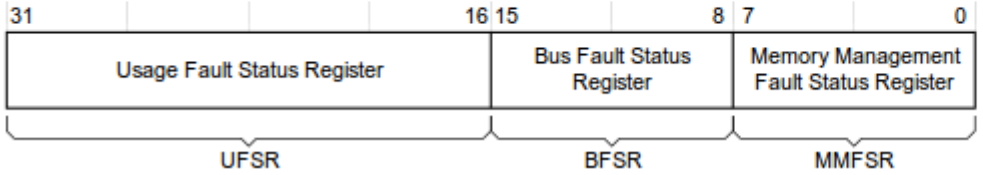


Repasando:

* La MPU permite proteger regiones de memoria mediante permisos de acceso
* Se inicia el programa en modo privilegiado
* Al escribir el registro MPU_CTRL se switchea el programa a modo usuario
* Las interrupciones siempre corren en modo privilegiado
* Se accede al MPU por medio de registros en memoria
* Se puede configurar hasta 8 regiones de de memoria protegida
* Se pueden solapar las regiones de memoria
* Cada región se puede sub dividir en 8 sub-regiones
* Al solaparse las regiones de memoria prevalece los permisos de la que tiene mayor N°
* Cuando se produce una violacion de memoria se dispara una MemManage Fault
*

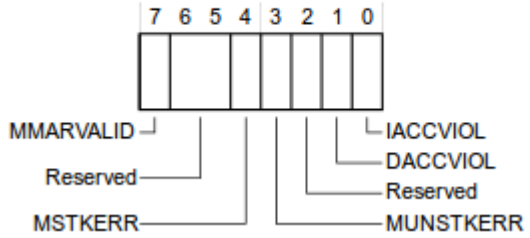
4.3.10. Configurable Fault Status Register

The CFSR indicates the cause of a MemManage fault, BusFault, or UsageFault. See the register summary in Table 4.12 for its attributes. The bit assignments are:



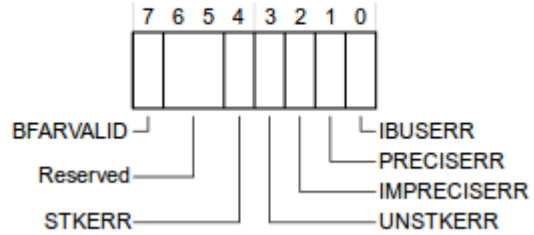
MemManage Fault Status Register

The flags in the MMFSR indicate the cause of memory access faults. The bit assignments are:



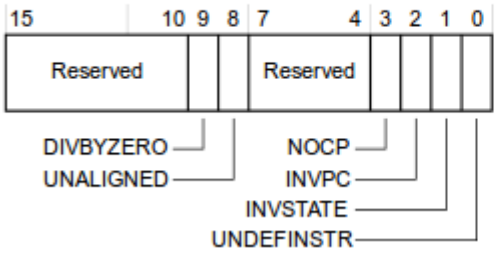
BusFault Status Register

The flags in the BFSR indicate the cause of a bus access fault. The bit assignments are:



UsageFault Status Register

The UFSR indicates the cause of a UsageFault. The bit assignments are:



http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0552a/BIHHHDDJ.html

Cortex-M3 Devices Generic User Guide

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0552a/BIHJJABA.html

Application Note 179

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dai0179b/CHDFDFIG.html

Ejemplos

https://github.com/scottellis/lpc17xx.cmsis.driver.library/tree/master/Examples/Cortex-M3/MPU

https://blog.feabhas.com/2013/02/setting-up-the-cortex-m34-armv7-m-memory-protection-unit-mpu