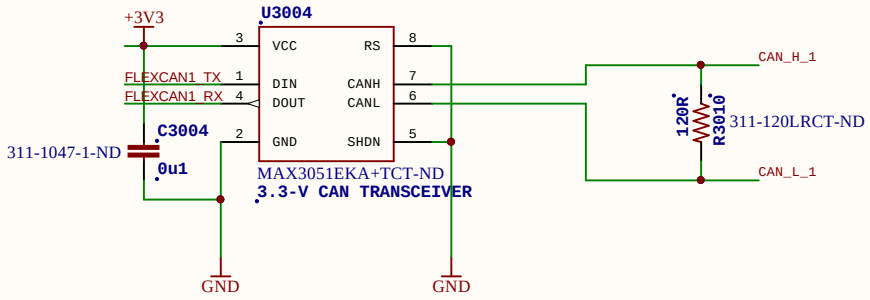

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Size A4	Number	Revision
Date: 17/05/2016		Sheet of
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Project

Variant: PCA_0012_INTEL_CB

17/05/2016

VersionRevision

RELEASED 23-OCT-2015

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

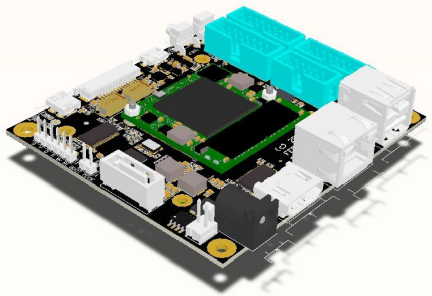
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

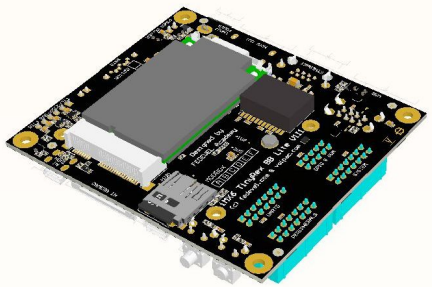
DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW



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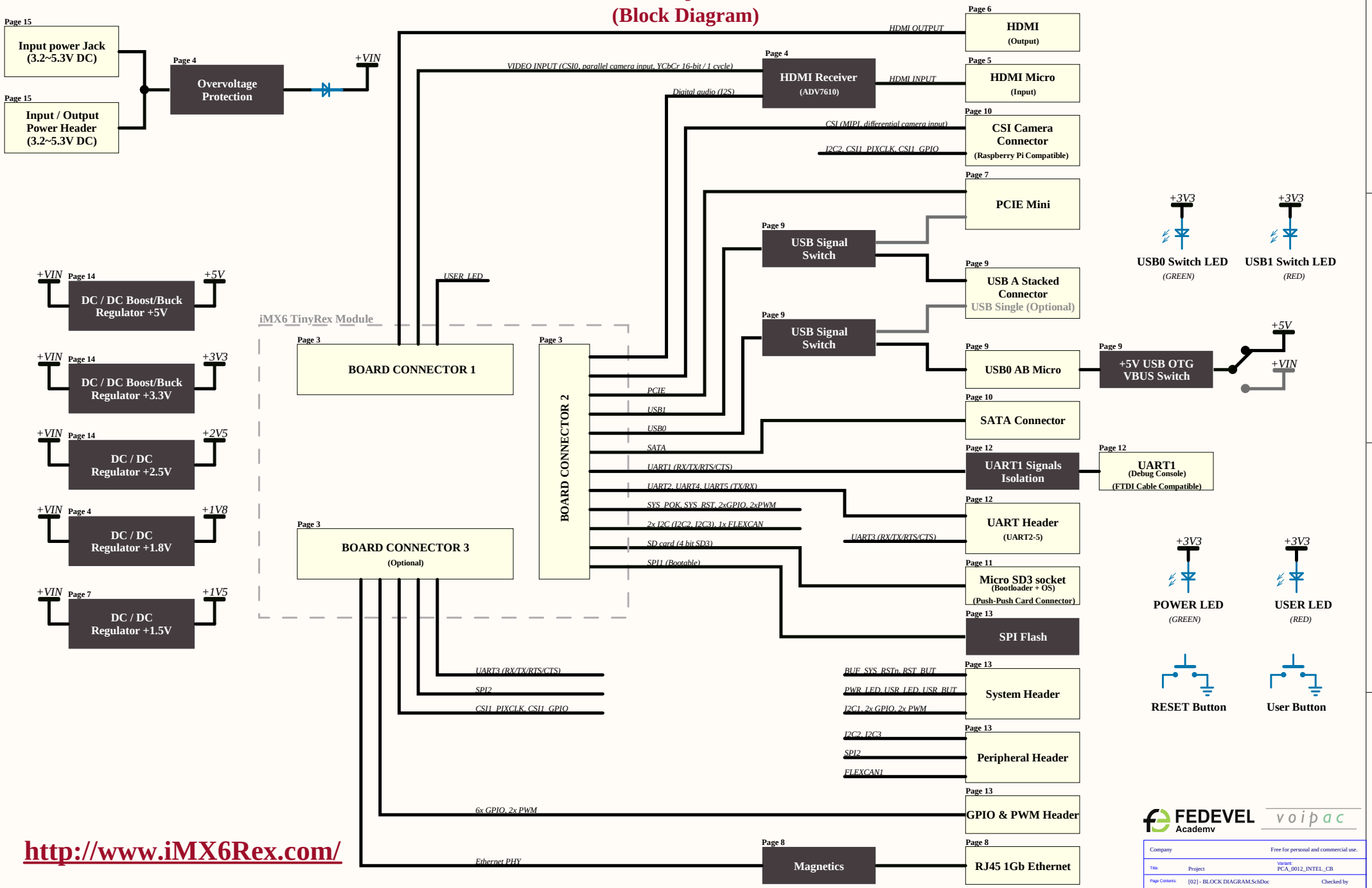
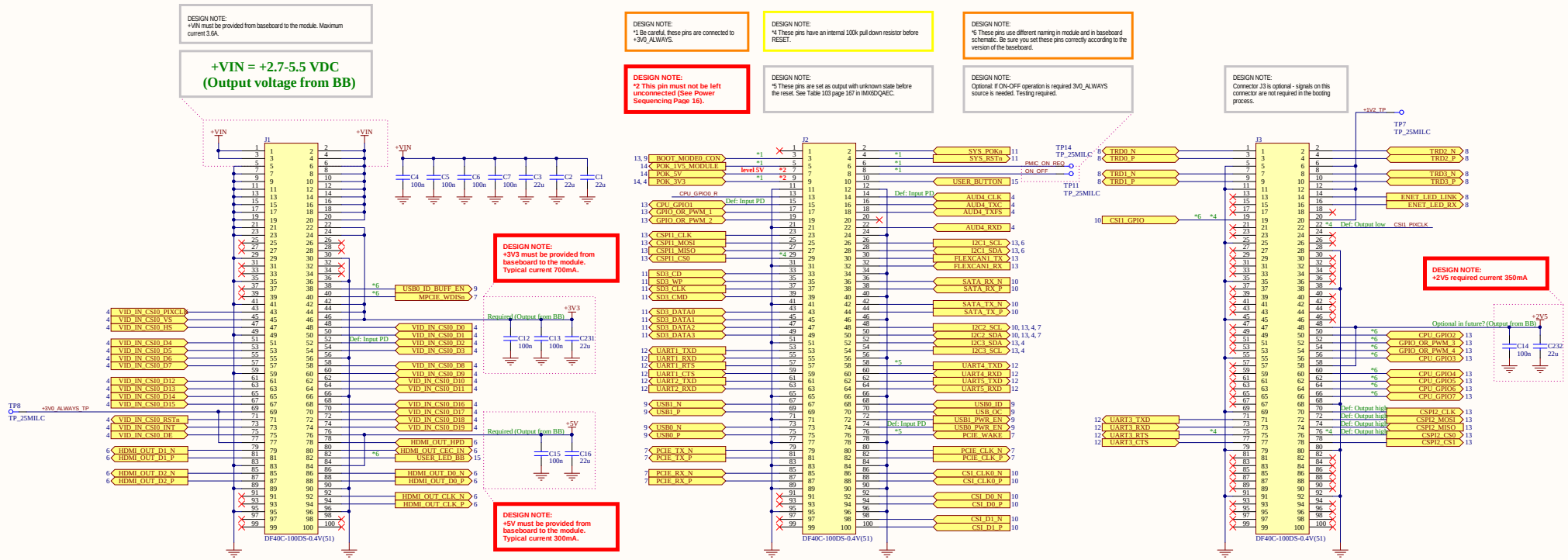
Project
(Block Diagram)



CONNECTORS



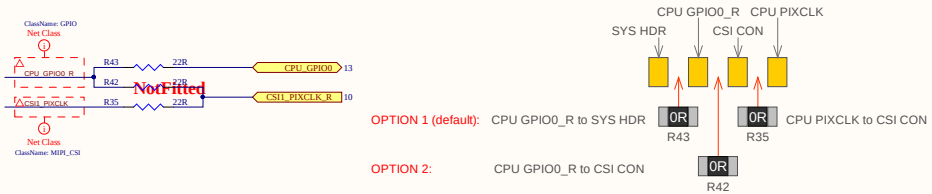
LAYOUT NOTE:
If 1.5mm standoff Board to Board connector is used, do not place any components under the module.

DESIGN NOTE:
Mating connector default: DF40C-100DP-0.4V[51]
http://www.digikey.com/product-detail/en/DF40C-100DP-0.4V%2851%29/H11614TR-ND/1969475

DESIGN NOTE:
Maximum current for the board to board connector is 0.3A per contact.

CPU_GPIO0 & CSI1_PIXCLK Routing

DESIGN NOTE:
Use one of the options to fit series resistors according to the picture below.



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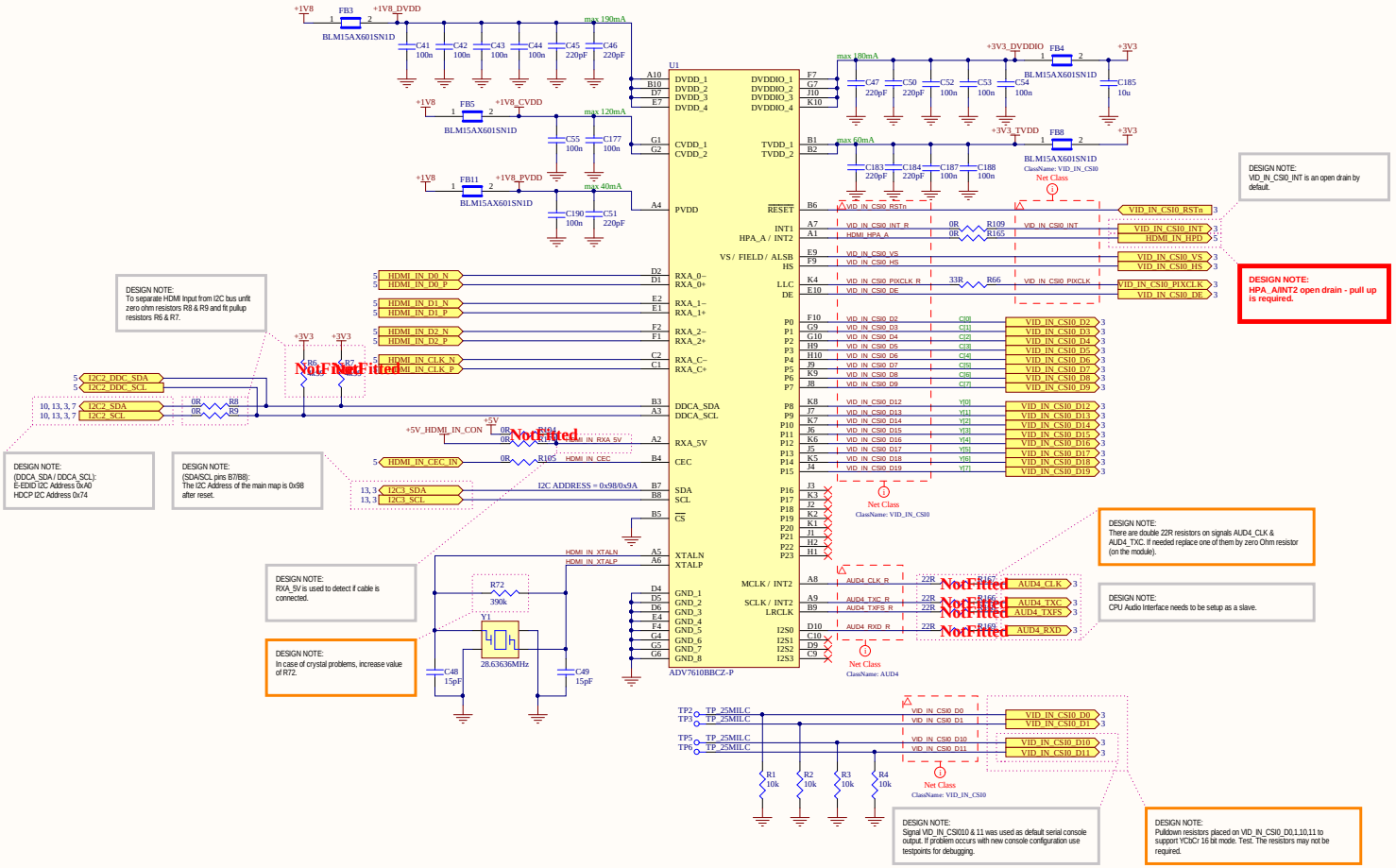
HDMI Video Input



DESIGN NOTE:
To separate HDMI Input from I2C bus unfit zero ohm resistors R8 & R9 and fit pullup resistors R6 & R7.

DESIGN NOTE:
(DDCA_SDA / DDCA_SCL):
E-EDID I2C Address 0xA0
HDCP I2C Address 0x74

DESIGN NOTE:
(SDA/SCL pins B7/B8):
The I2C Address of the main map is 0x98 after reset.

DESIGN NOTE:
RXA_5V is used to detect if cable is connected.

DESIGN NOTE:
In case of crystal problems, increase value of R72.

DESIGN NOTE:
VID_IN_CSI0_INT is an open drain by default.

DESIGN NOTE:
HPA_A/INT2 open drain - pull up is required.

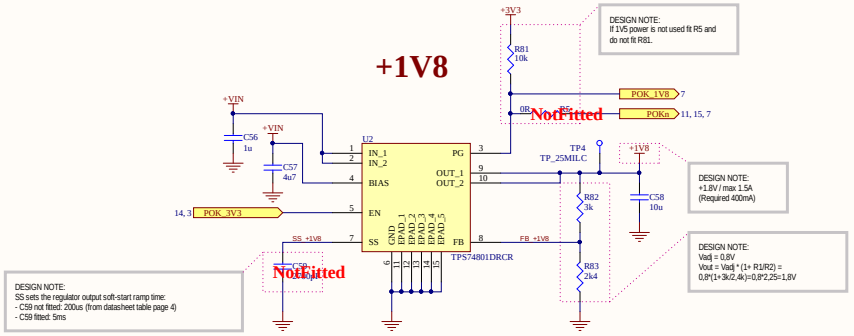
DESIGN NOTE:
There are double 22R resistors on signals AUD4_CLK & AUD4_TXC. If needed replace one of them by zero Ohm resistor (on the module).

DESIGN NOTE:
CPU Audio Interface needs to be setup as a slave.

DESIGN NOTE:
Signal VID_IN_CSI0/10 & 11 was used as default serial console output. If problem occurs with new console configuration use testpoints for debugging.

DESIGN NOTE:
Pulldown resistors placed on VID_IN_CSI0_D0,1,10,11 to support YCbCr 16 bit mode. Test. The resistors may not be required.

+1V8



DESIGN NOTE:
If 1V5 power is not used fit R5 and do not fit R81.

DESIGN NOTE:
+1.8V / max 1.5A
(Required 400mA)

DESIGN NOTE:
Vadj = 0,8V
Vout = Vadj * (1+ R1/R2) =
0,8*(1+3k/2,4k)=0,8*2,25=1,8V

DESIGN NOTE:
SS sets the regulator output soft-start ramp time:
- C59 not fitted: 200us (from datasheet table page 4)
- C59 fitted: 5ms

DESIGN NOTE:
IMX6 IPU Sensor Interface Signal Mapping

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 1 cycle	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
IPUx_CSIx_DATA00	—	—	—	—	—	—	—	0	C[0]
IPUx_CSIx_DATA01	—	—	—	—	—	—	—	0	C[1]
IPUx_CSIx_DATA02	—	—	—	—	—	—	—	C[0]	C[2]
IPUx_CSIx_DATA03	—	—	—	—	—	—	—	C[1]	C[3]
IPUx_CSIx_DATA04	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
IPUx_CSIx_DATA05	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
IPUx_CSIx_DATA06	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
IPUx_CSIx_DATA07	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
IPUx_CSIx_DATA08	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
IPUx_CSIx_DATA09	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
IPUx_CSIx_DATA10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
IPUx_CSIx_DATA11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
IPUx_CSIx_DATA12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
IPUx_CSIx_DATA13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
IPUx_CSIx_DATA14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
IPUx_CSIx_DATA15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
IPUx_CSIx_DATA16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
IPUx_CSIx_DATA17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
IPUx_CSIx_DATA18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
IPUx_CSIx_DATA19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

1 IPUx_CSIx stands for IPUx_CSI0 or IPUx_CSI1
2 The MSB bits are duplicated on LSB bits implementing color extension
3 The two MSB bits are duplicated on LSB bits implementing color extension
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB 16 bits— Supported in two ways: (1) As a "generic data" input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr 16 bits— Supported as a "generic-data" input, with no on-the-fly processing.
7 YCbCr 16 bits— Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

DESIGN NOTE:
ADV7610 SDR Output Modes

OP_FORMAT_SEL[7:0]	SDR 4:2:2					SDR 4:4:4
	0x0	0x0A	0x80	0x8A		0x40
Pixel Output	8-Bit SDR ITU-R uT.656 Mode 0	12-Bit SDR ITU-R BT.656 Mode 2	16-Bit SDR ITU-R BT.656 4:2:2 Mode 0	24-Bit SDR ITU-R BT.656 4:2:2 Mode 2	24-Bit SDR 4:4:4 Mode 0	
P23	High-Z	Y3, Cb3, Cr3	High-Z	Y3	R7	
P22	High-Z	Y2, Cb2, Cr2	High-Z	Y2	R6	
P21	High-Z	Y1, Cb1, Cr1	High-Z	Y1	R5	
P20	High-Z	Y0, Cb0, Cr0	High-Z	Y0	R4	
P19	High-Z	High-Z	High-Z	Cb3, Cr3	R3	
P18	High-Z	High-Z	High-Z	Cb2, Cr2	R2	
P17	High-Z	High-Z	High-Z	Cb1, Cr1	R1	
P16	High-Z	High-Z	High-Z	Cb0, Cr0	R0	
P15	Y7, Cb7, Cr7	Y11, Cb11, Cr11	Y7	Y11	G7	
P14	Y6, Cb6, Cr6	Y10, Cb10, Cr10	Y6	Y10	G6	
P13	Y5, Cb5, Cr5	Y9, Cb9, Cr9	Y5	Y9	G5	
P12	Y4, Cb4, Cr4	Y8, Cb8, Cr8	Y4	Y8	G4	
P11	Y3, Cb3, Cr3	Y7, Cb7, Cr7	Y3	Y7	G3	
P10	Y2, Cb2, Cr2	Y6, Cb6, Cr6	Y2	Y6	G2	
P9	Y1, Cb1, Cr1	Y5, Cb5, Cr5	Y1	Y5	G1	
P8	Y0, Cb0, Cr0	Y4, Cb4, Cr4	Y0	Y4	G0	
P7	High-Z	High-Z	Cb7, Cr7	Cb11, Cr11	B7	
P6	High-Z	High-Z	Cb6, Cr6	Cb10, Cr10	B6	
P5	High-Z	High-Z	Cb5, Cr5	Cb9, Cr9	B5	
P4	High-Z	High-Z	Cb4, Cr4	Cb8, Cr8	B4	
P3	High-Z	High-Z	Cb3, Cr3	Cb7, Cr7	B3	
P2	High-Z	High-Z	Cb2, Cr2	Cb6, Cr6	B2	
P1	High-Z	High-Z	Cb1, Cr1	Cb5, Cr5	B1	
P0	High-Z	High-Z	Cb0, Cr0	Cb4, Cr4	B0	

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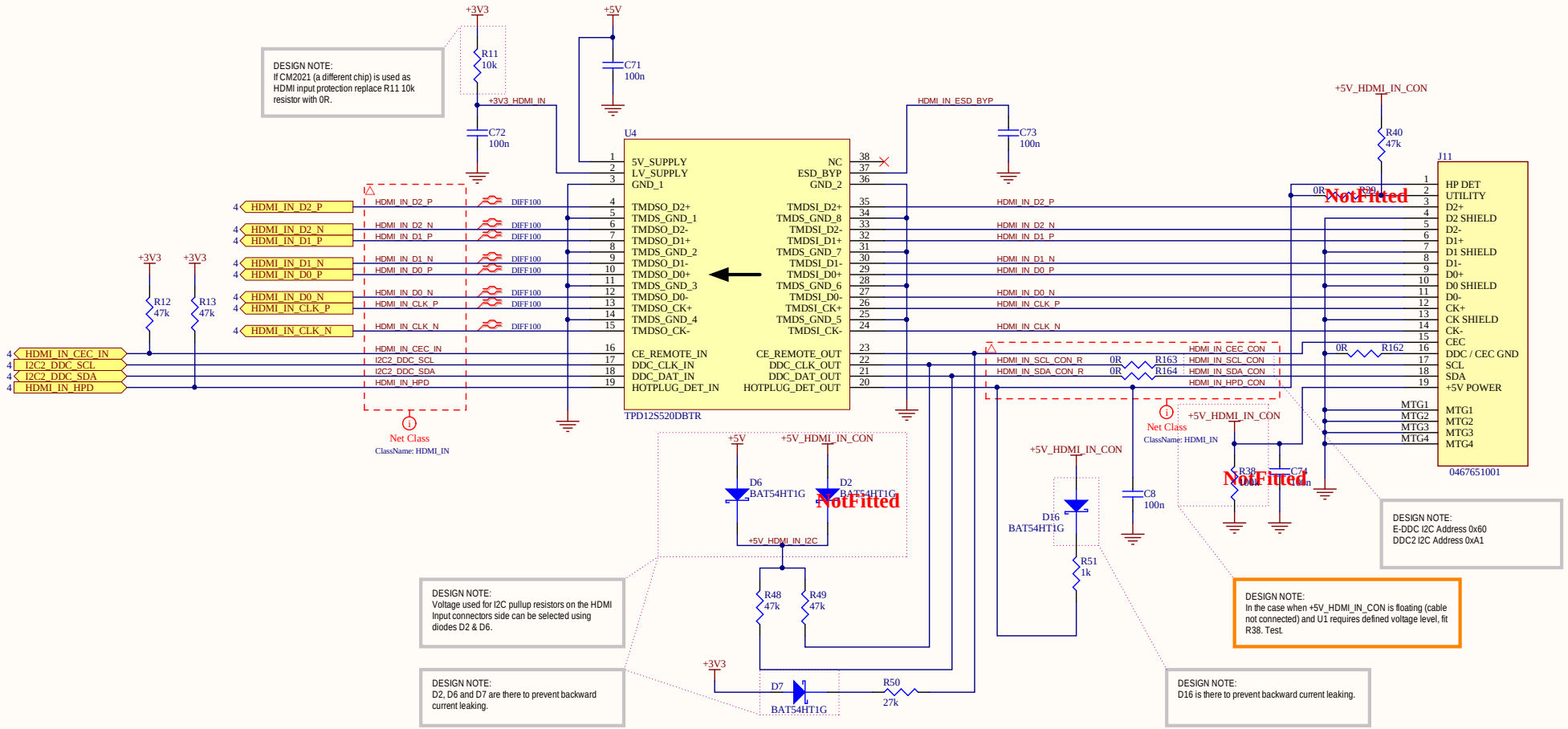
HDMI Input Connector



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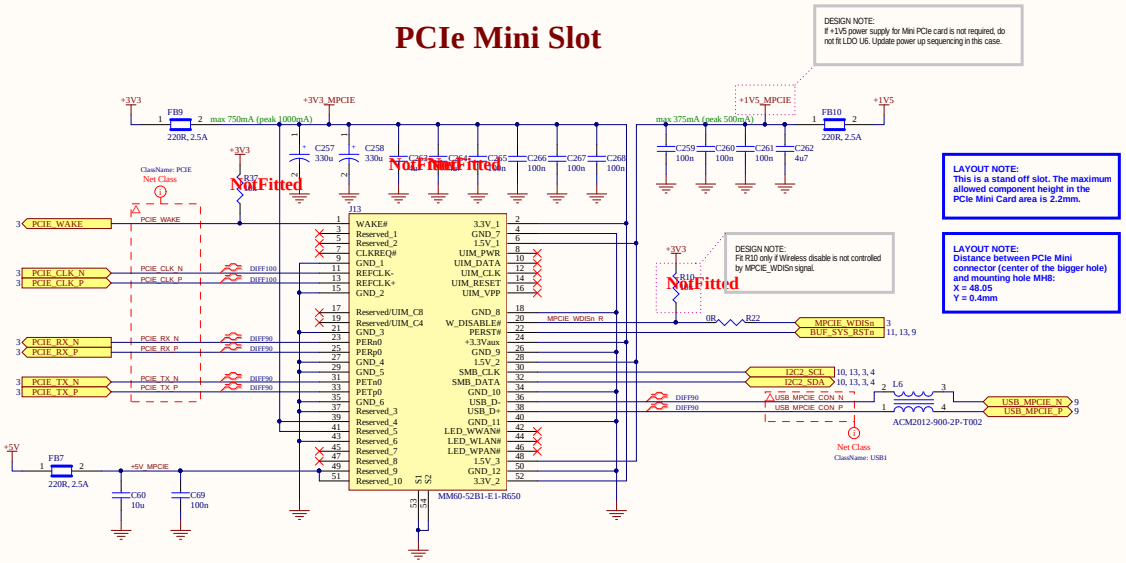
PCIE MINI

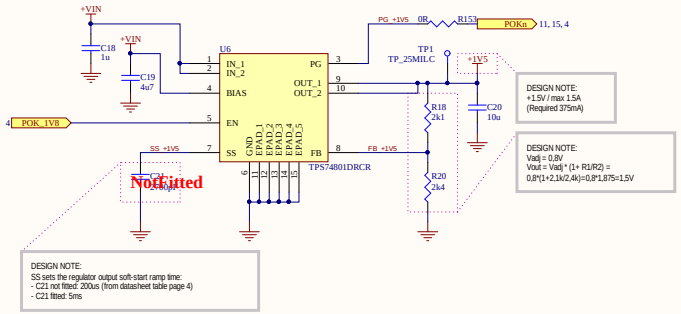
PCIe Mini Slot



LAYOUT NOTE:
This is a stand off slot. The maximum allowed component height in the PCIe Mini Card area is 2.2mm.

LAYOUT NOTE:
Distance between PCIe Mini connector (center of the bigger hole) and mounting hole MH8:
X = 48.05
Y = 0.4mm

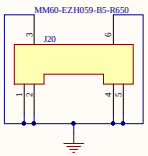
PCIe Mini +1V5 power



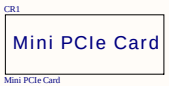
PCIe Mini Card Latch

LAYOUT NOTE:
Distance between PCIe Mini connector and latch (hole to hole - the bigger ones):
X = 50.3mm
Y = 0.4mm

See also:
https://jae-connectors.com/en/pdf_download_exec.cfm?param=SJ105219.pdf



3D Model of PCIe Mini Card



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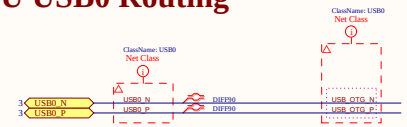
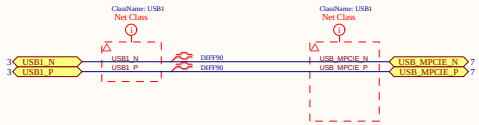
USB

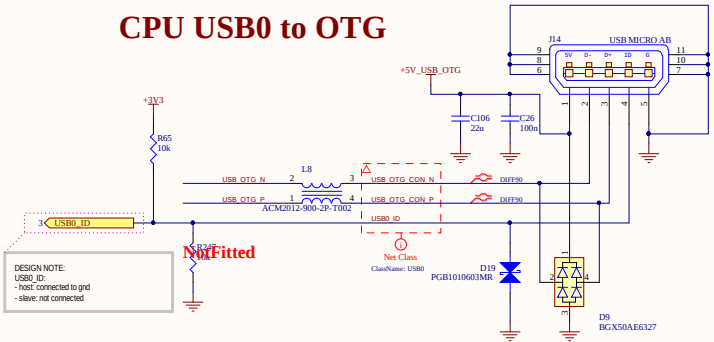
CPU USB0 Routing



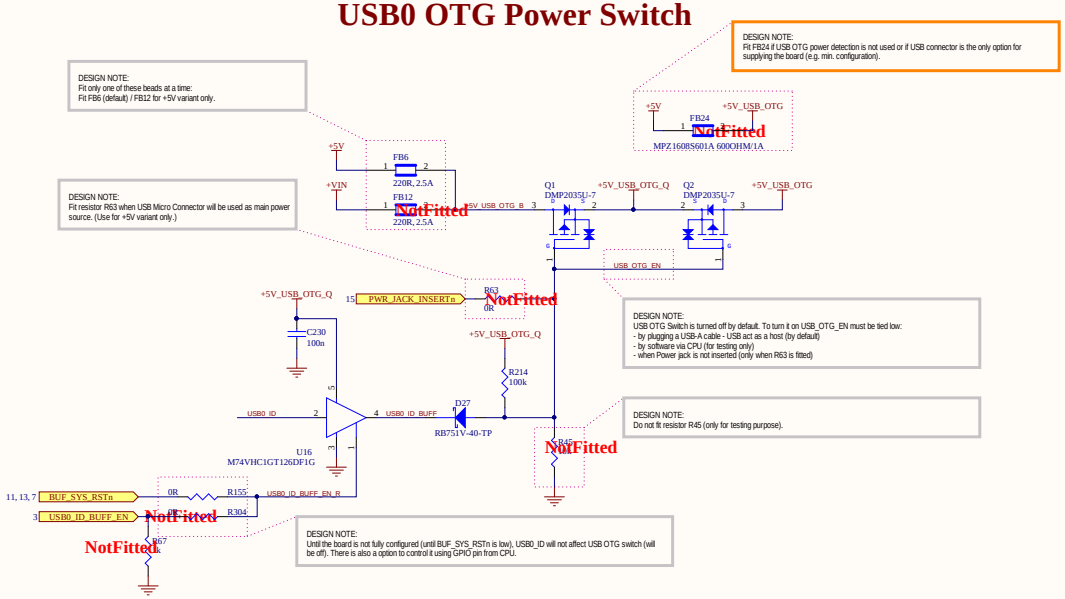
CPU USB1 Routing



CPU USB0 to OTG



USB0 OTG Power Switch



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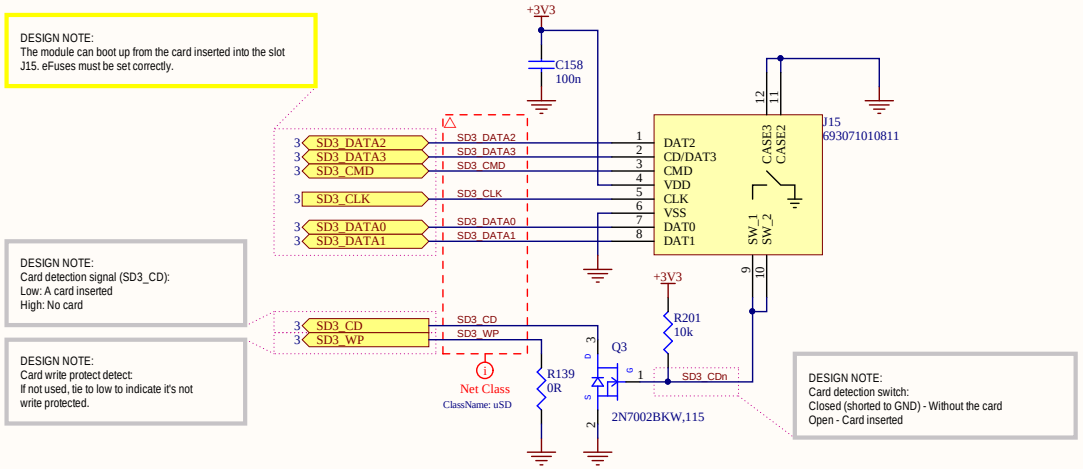
SD CARD, BUFFERS

Micro SD Slot



3D Model of Micro SD Card

CR2

Micro SD Card

Micro SD Card

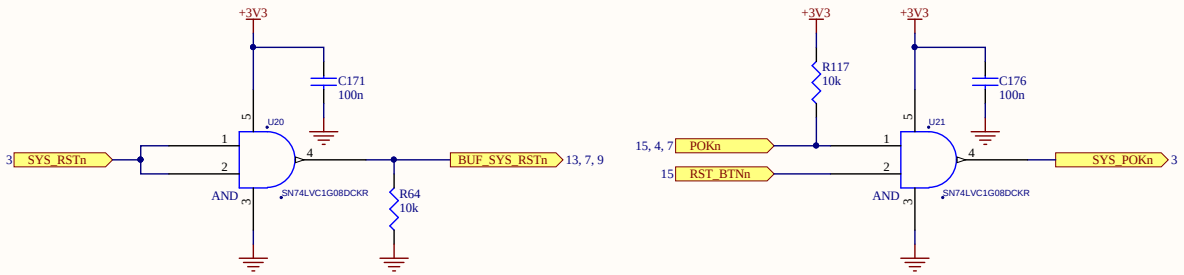
Software

FIRMWARE_FOR_CARD_IN_J15

FIRMWARE
uBOOT + OS

iMX6 TinyRex uBOOT+OS 1.0

RESET BUFFERS



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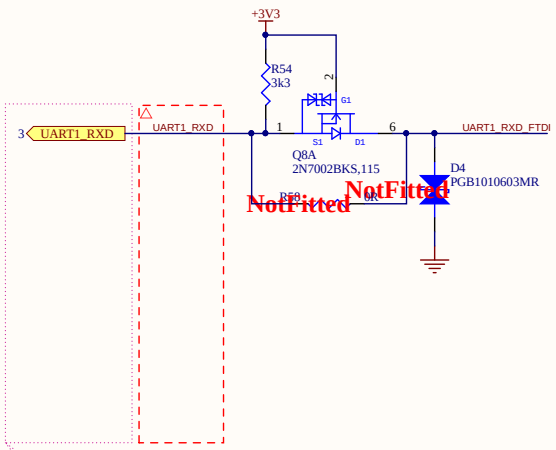
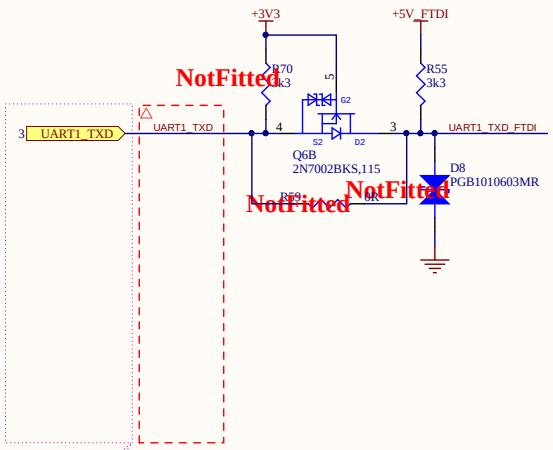
UARTS

UART 1 - Debug console (+3V3)

Buffers for CPU Input Pins



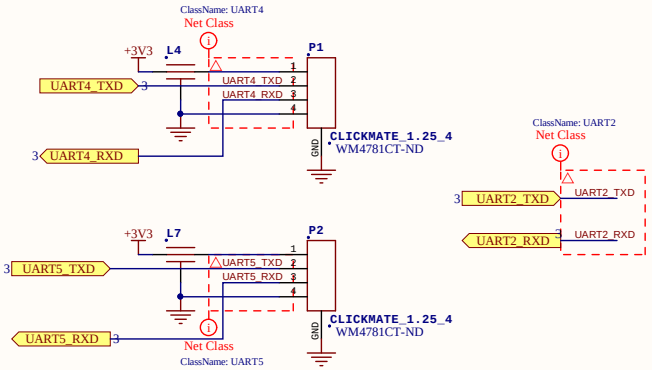
Buffers for CPU Output Pins



DESIGN NOTE:
Buffers for UART1 are designed to isolate the CPU when the board is turned off and cable is still connected. Without an isolation plugged cable can prevent CPU from booting.

DESIGN NOTE:
If isolation function is not needed, buffers can by bypassed using resistors R58-R61.

UART Header



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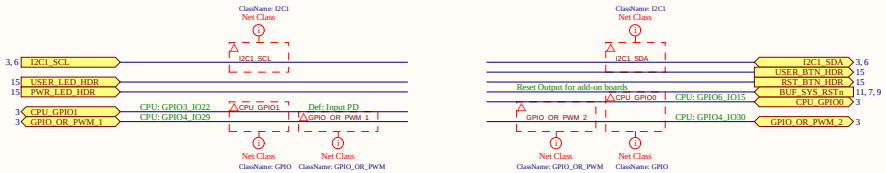
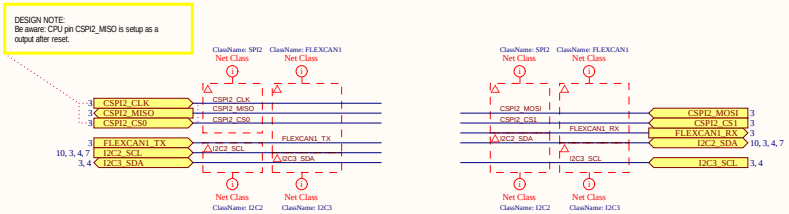
HEADERS, SPI

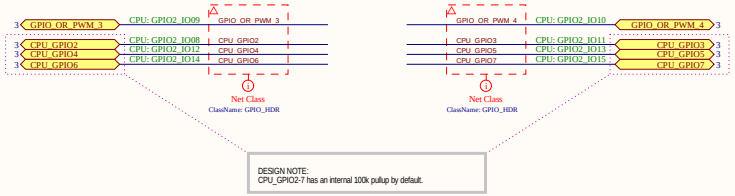
SYSTEM HEADER



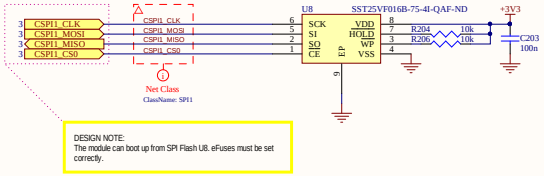
PERIPHERAL HEADER



GPIO & PWM HEADER



SPI NOR FLASH



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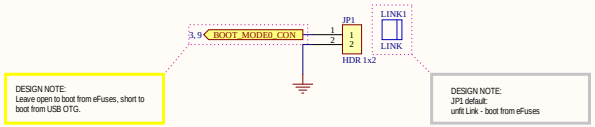

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Title: Project		Variant: PCA_0012_INTEL_CB
Page Contents: [13] - HEADERS, SPI.SchDoc		Checked by
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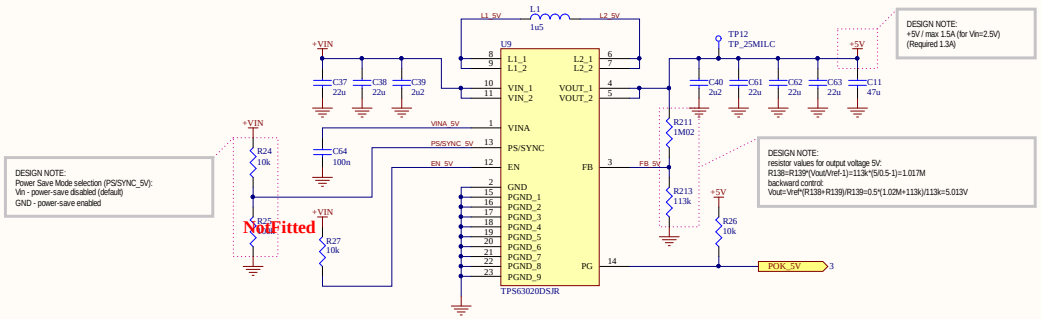
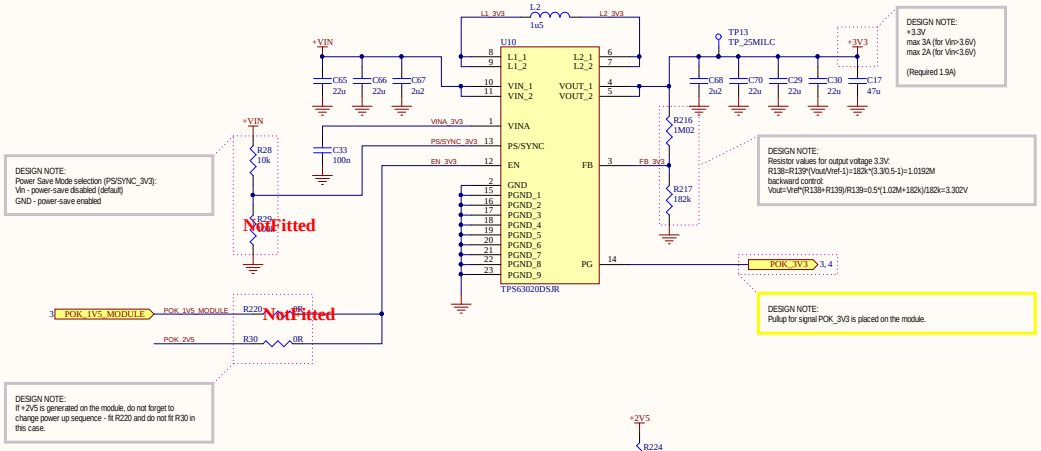
Date: 17/05/2016	Designed by www.fedevel.com	Sheet 13 of 18

POWERS +5V, +3V3, +2V5

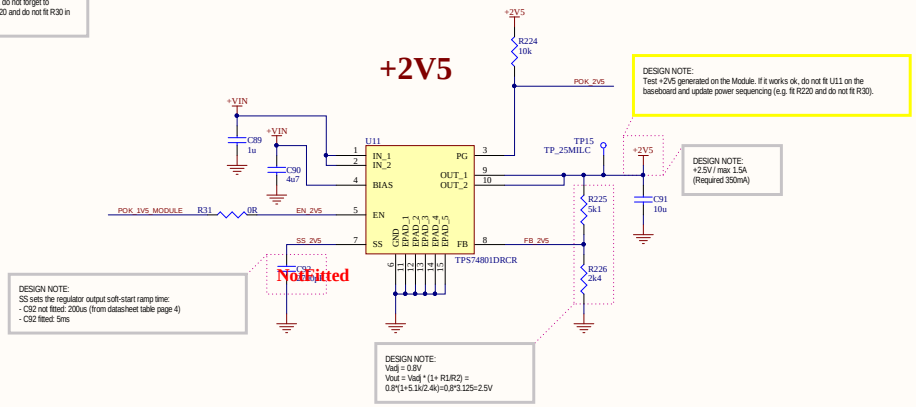
+5V



+3V3



+2V5



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Company		Free for personal and commercial use.
Title: Project		Variant: PCA_0012_INTEL_CB
Page Contents:	[14] - PWR 5V, 3V3, 2V5.SchDoc	Checked by
Size:	DWG NO	Revision: VersionRevision
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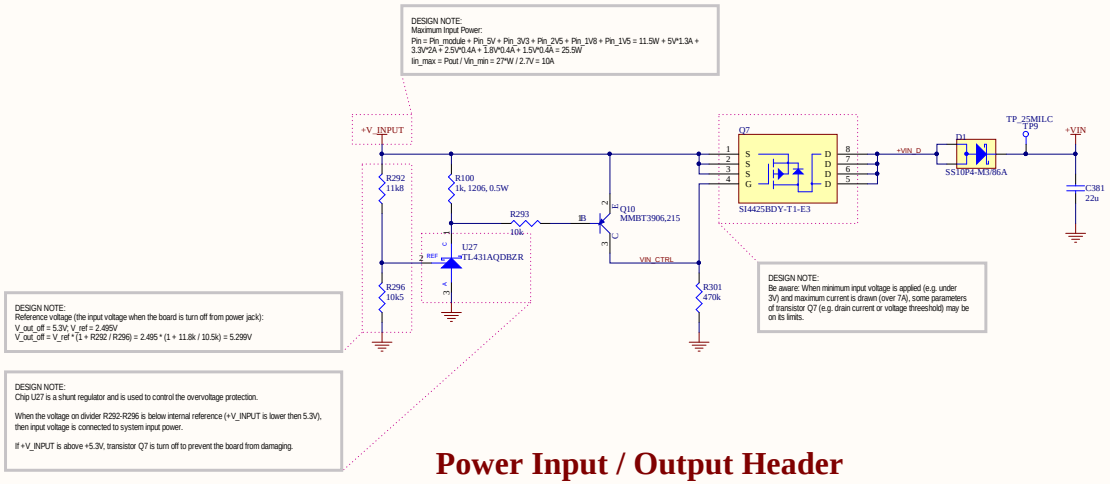
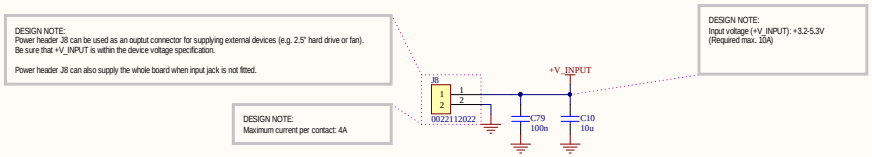
PWR IN, LEDS, BUTTONS, MECH

Power Input (+3.2 to +5.3V DC)

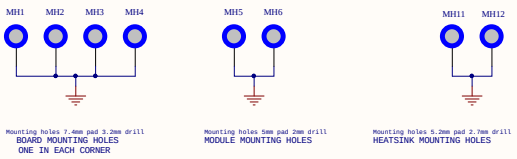


Power Input / Output Header



Mechanical

Mounting Holes



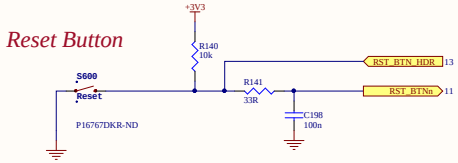
Module Mounting Accessories

Fiducials

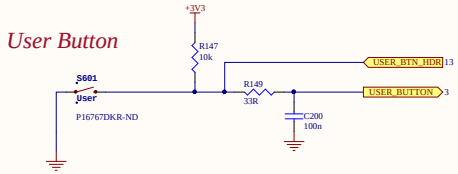
Gnd Testpoint

Buttons

Reset Button

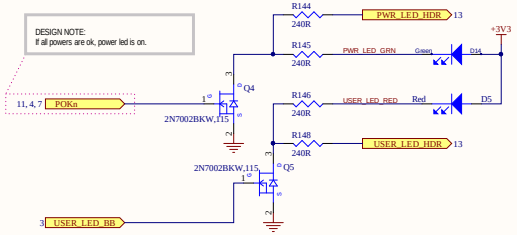


User Button



LEDs

Power & User LEDs



PCB

iMX6 TinyRex Module 3D Model

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Title:	Project	Variant: PCA_0012_INTEL_CB	
Page Contents:	[15] - PWR IN, LEDS, BUTTONS, MECH.SchDoc	Checked by	
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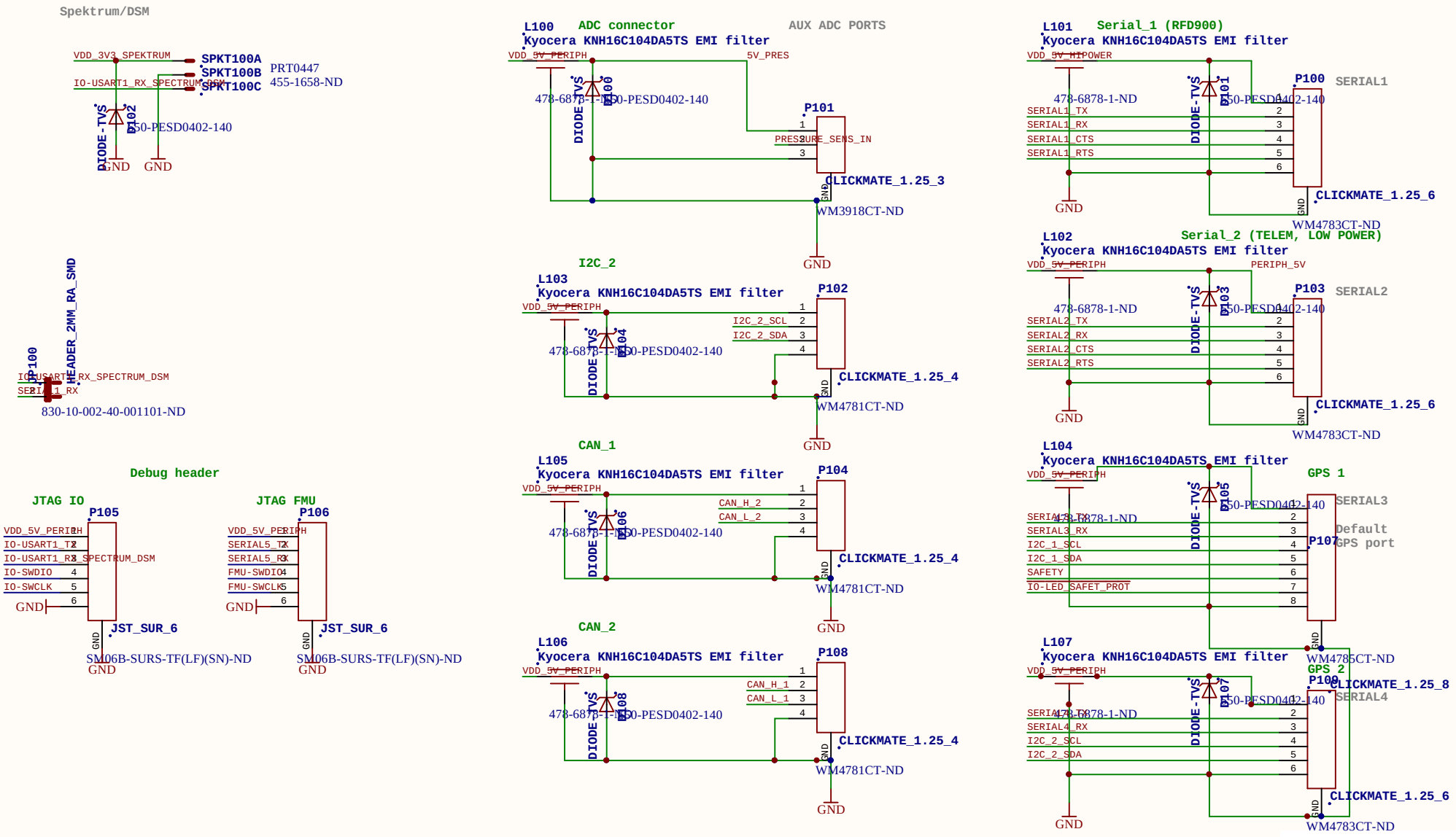

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Date: 17/05/2016	Time: 11:36:31 AM
Sheet:* of: *	Drawn By: Philip Rowse
Approved: *	Checked By: *
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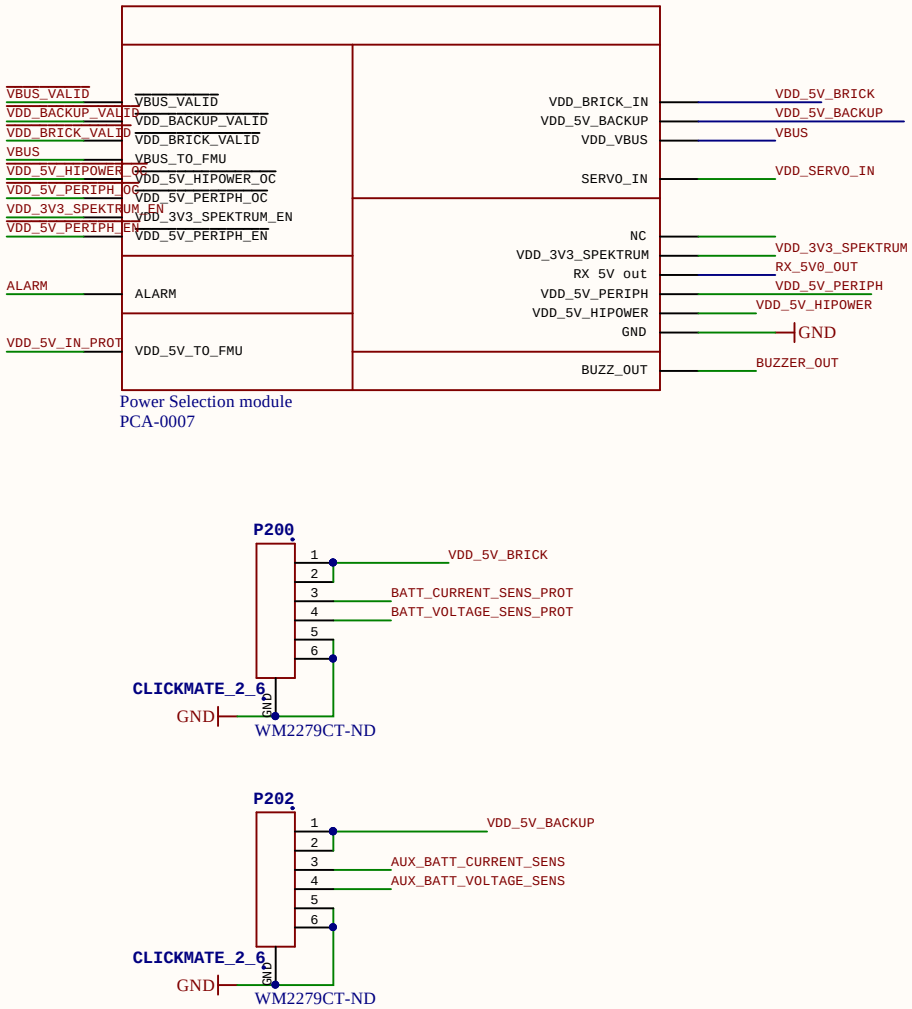

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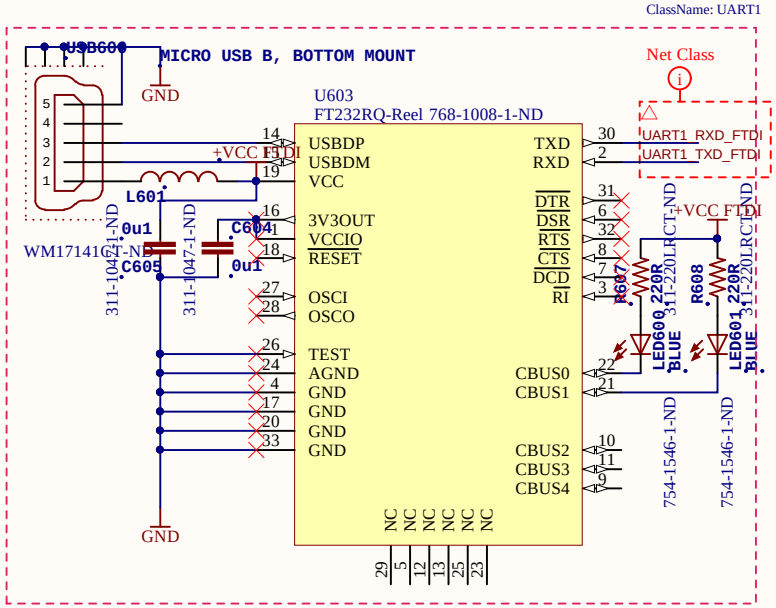

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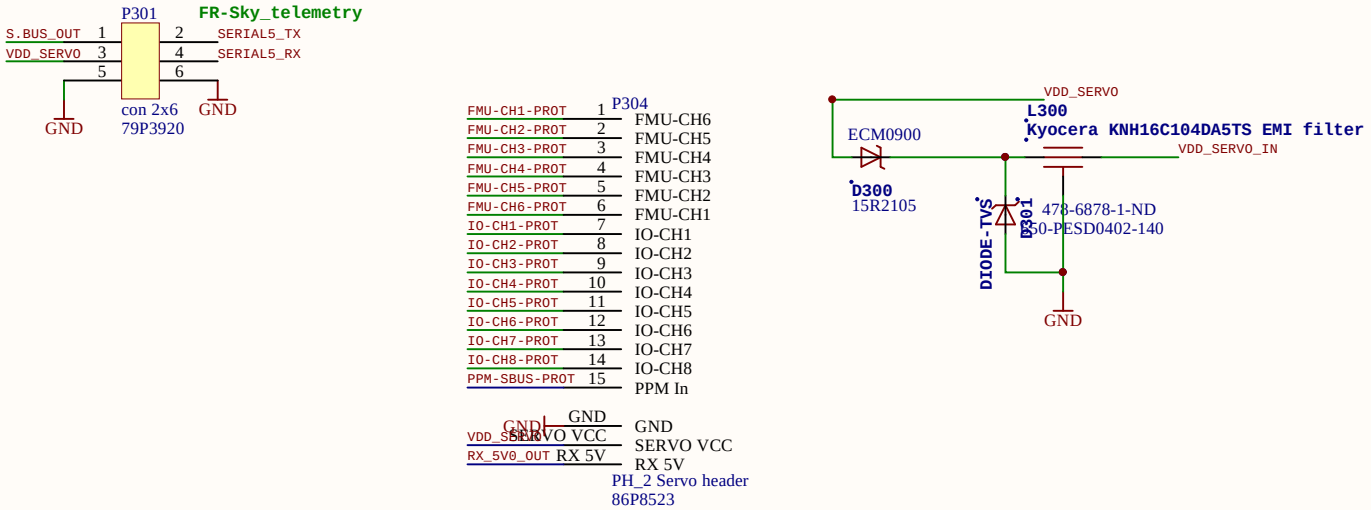

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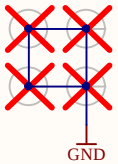

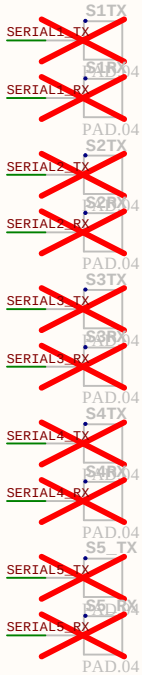

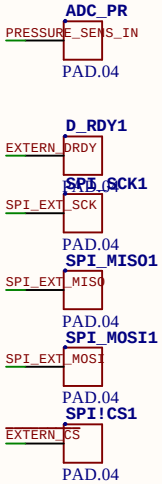

Fiducials for machine vision alignment.

Title: [21] - TEST POINTS.SchDoc		
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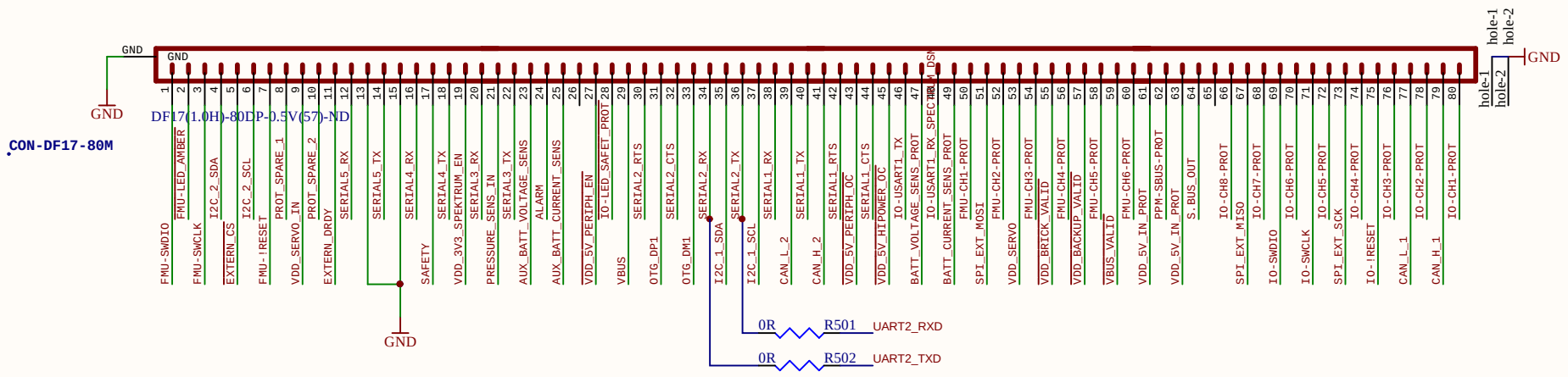

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