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NAND Flash Interface Interoperability

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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NAND FLASH INTERFACE INTEROPERABILITY

(From JEDEC Board Ballot JCB-25-54, formulated under the cognizance of the JC-42.4 Subcommittee on Nonvolatile Memory Devices, item number 1863.11).

1 Scope

This standard was jointly developed by JEDEC and the Open NAND Flash Interface Workgroup, hereafter referred to as ONFI. This standard defines a standard NAND flash device interface interoperability standard that provides means for system be designed that can support Asynchronous SDR, Synchronous DDR and Toggle DDR NAND flash devices that are interoperable between JEDEC and ONFI member implementations.

2 Terms, Definitions, Abbreviations, and Conventions

2.1 Terms and Definitions

address: A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172 and JESD88.)

NOTE 1 In a nonvolatile memory array, the address consists of characters, typically hexadecimal, to identify the row and column location of the memory cell(s).

NOTE 2 For NAND nonvolatile memory devices, the row address is for a page, block, or logical unit number (LUN); the column address is for the byte or word within a page.

NOTE 3 The least significant bit of the column address is zero for the source synchronous data interface.

asynchronous: Describing operation in which the timing is not controlled by a clock.

NOTE For a NAND nonvolatile memory, asynchronous also means that data is latched with the WE_n signal for the write operation and the RE_n signal for the read operation.

block: A continuous range of memory addresses. (Ref. IEC 748-2 and JESD88.)

NOTE 1 The number of addresses included in the range is frequently equal to 2^n , where n is the number of bits in the address.

NOTE 2 For nonvolatile memories, a block consists of multiple pages and is the smallest addressable memory segment within a memory device for the erase operation.

column: In a nonvolatile memory array, a series of memory cells whose sources and/or drains are connected via a bit line.

NOTE 1 Depending on the nonvolatile memory array, the bit line is accessed via the column select transistor, the column address decoder, or other decoding scheme.

NOTE 2 In nonvolatile memory device, a column decoder accesses a bit (x1), byte (x8), word (x16), or Dword (x32) either individually or within a page.

NOTE 3 In a typical schematic of a memory array, the column is in the vertical direction.

2.1 Terms and Definitions (cont'd)

Dword (x32): A sequence of 32 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 31; the most significant bit is shown on the left. When shown as words, the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes, the least significant byte is byte 0 and the most significant byte is byte 3.

NOTE 2 See **Figure 2.5-1** for a description of the relationship between bytes, words, and Dwords.

latching edge: The rising or falling edge of a waveform that initiates a latch operation.

NOTE 1 For a NAND nonvolatile memory the latching edge is the edge of the CK or DQS signal on which the contents of the data bus are latched for the source synchronous data interface.

NOTE 2 For a NAND nonvolatile data cycles, the latching edge is both the rising and falling edges of the DQS signal.

NOTE 3 For a NAND nonvolatile command and address cycles, the latching edge for the source synchronous interface is the rising edge of the CK signal.

NAND defect area: A designated location within the NAND memory where factory defects are identified by the manufacturer.

NOTE 1 The location is a portion of either the first page and/or the last page of the factory-marked defect block, this defect area in each page is defined as (# of data bytes) to (# of data bytes + # of spare bytes -1).

NOTE 2 For an 8-bit data access NAND memory device, the manufacturer sets the first byte in the defect area of the first or last page of the defect block to a value of 00h.

NOTE 3 For a 16-bit data access NAND memory device, the manufacturer sets the first word in the defect area of the first or last page of the defect block to a value of 0000h.

NAND nonvolatile memory device: The packaged NAND nonvolatile memory unit containing one or more NAND targets.

NOTE This is referred to as "device" in this standard.

NAND row address: An address referencing the LUN, block, and page to be accessed.

NOTE 1 The page address uses the least significant row address bits.

NOTE 2 The block address uses the middle row address bits.

NOTE 3 The LUN address uses the most significant row address bits.

page: The smallest nonvolatile memory array segment, within a device, that can be addressed for read or program operations.

page register: A register used to transfer data from a page in the memory array for a read operation or to transfer data to a page in the memory array for a program operation.

read request (for a nonvolatile memory): A data output cycle request from the host that results in a data transfer from the device to the host.

source synchronous (for a nonvolatile memory): Describing an operation in which the strobe signal (DQS) is transmitted with the data to indicate when the data should be latched.

NOTE The strobe signal (DQS) is similar in concept to an additional data bus bit.

2.1 Terms and Definitions (cont'd)

status register (SR[x]): A register within a particular LUN containing status information about that LUN.

NOTE SR[x] refers to bit "x" within the status register.

target: A nonvolatile memory component with a unique chip enable (CE_n) select pin.

word (x16): A sequence of 16 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A word may be represented as 16 bits or as two adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 15; the most significant bit is shown on the left. When shown as bytes, the least significant byte (lower) is byte 0 and the most significant byte is byte 2.

NOTE 2 See **Figure 2.5-1** for a description of the relationship between bytes, words, and Dwords.

2.2 Abbreviations

DDR: Abbreviation for "double data rate".

LUN (logical unit number): The minimum memory array size that can independently execute commands and report status.

N/A: Abbreviation for "not applicable". Fields marked as "na" are not used.

O/M: Abbreviation for Optional/Mandatory requirement. When the entry is set to "M", the item is mandatory. When the entry is set to "O", the item is optional.

2.3 Conventions

2.3.1 Active-low Signals

While the preferred method for indicating a signal that is active when low is to use the over-bar as in \overline{CE} , the difficulty in producing this format has resulted in several alternatives meant to be equivalents. These are the use of a CE reverse solidus (\) or the trailing underscore (_) following the signal name as in $CE\backslash$ and $CE_$. In this publication "_n" is used to indicate an active low signal (i.e., an inverted logic sense).

2.3.2 Signal Names

The names of abbreviations, initials, and acronyms used as signal names are in all uppercase (e.g., CE_n). Fields containing only one bit are usually referred to as the "name bit" instead of the "name field". Numerical fields are unsigned unless otherwise indicated.

2.3.3 Precedence in Case of Conflict

If there is a conflict between text, figures, state machines, timing diagrams, and/or tables, the precedence shall be state machine, timing diagrams, tables, figures, and text.

2.4 Keywords

Several keywords are used to differentiate between different levels of requirements or suggestions.

mandatory: A keyword indicating items to be implemented as defined by a standard. Users are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the standard.

may: A keyword that indicates flexibility of choice between stated alternatives or possibly nothing with no implied preference.

optional: A keyword that describes features that are not required by the specification. However, if any optional feature defined by the specification is implemented, that feature shall be implemented in the way defined by the specification.

reserved: A keyword indicating reserved bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, or field may be cleared to zero or in accordance with a future extension to this publication. A host should not read/use reserved information.

shall: A keyword indicating a mandatory requirement.

should: A keyword indicating flexibility of choice with a strongly preferred alternative. This is equivalent to the phrase "it is recommended".

2.5 Byte, Word, and Dword Relationships

Figure 2.5-1 illustrates the relationship between bytes, words, and Dwds

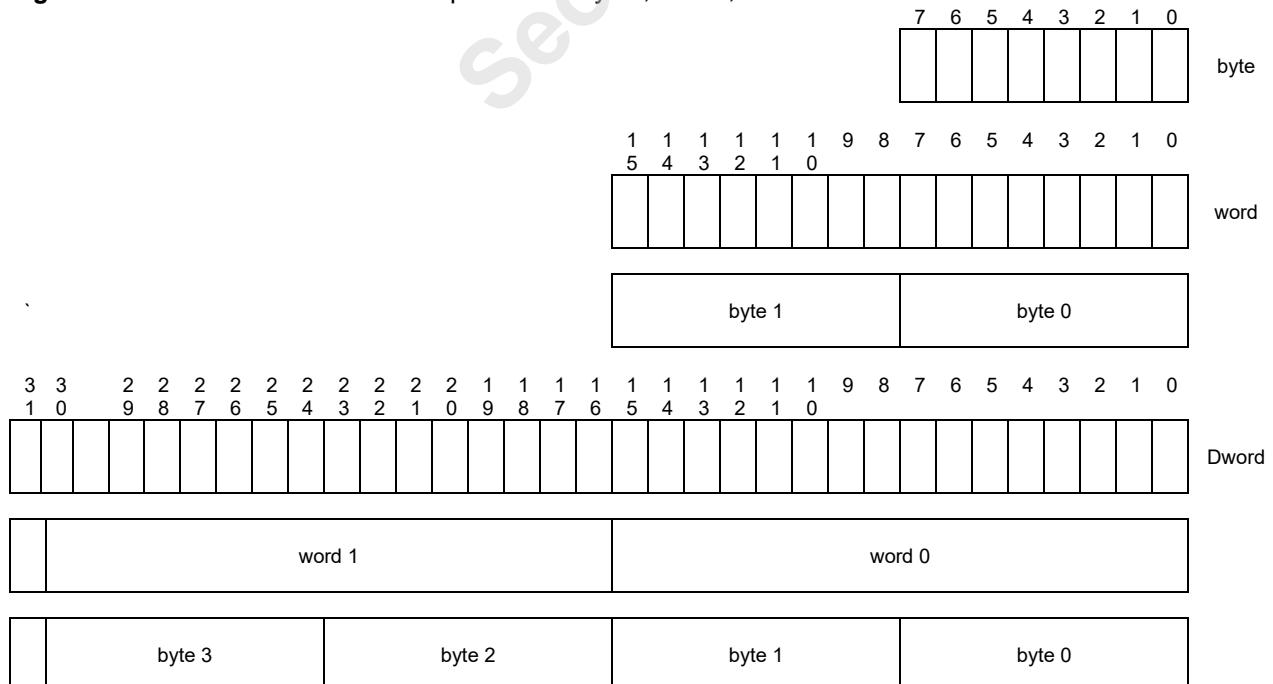


Figure 2.5-1 — Byte, Word, and Dword Relationships

2.6 Pin Description (Conventional Protocol)

Table 2.6-1 — Pin Description

Name	Input/ Output	Description
IO0 ~ IO7(~ IO15) DQ0 ~ DQ7 DQ0_x ~ DQ7_x	I/O	<p>DATA INPUTS/OUTPUTS These signals are used to input command, address and data, and to output data during read operations. The signals float to high-z when the chip is deselected or when the outputs are disabled. IO0 ~ IO15 are used in a 16-bit wide target configuration. With multi-channel support, IO0_0~IO7_0 and IO0_1~IO7_1 are used for IOs of channel 0 and IOs of channel 1 respectively. Also known as DQ0~DQ7 for Toggle DDR and Synchronous DDR.</p> <p>The number after the underscore represents the channel. For example, DQ0_0 indicates DQ0 of channel-0 and DQ0_1 does DQ0 of channel-1.</p>
CLE_x	I	<p>COMMAND LATCH ENABLE The CLE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).</p>
ALE_x	I	<p>ADDRESS LATCH ENABLE The ALE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).</p>
CEx_x_n	I	<p>CHIP ENABLE The CEx_x_n input is the target selection control. When CEx_x_n is high and the target is in the ready state, the target goes into a low-power standby state. When CEx_x_n is low, the target is selected.</p> <p>The number after the first underscore represents the channel. For example, CE0_0_n indicates CE0_n of channel-0 and CE0_1_n does CE0_n of channel-1.</p>
WE_x_n	I	<p>WRITE ENABLE The WE_x_n input controls write to the I/O port. For Toggle DDR commands, addresses are latched on the rising edge of the WE_x_n pulse.</p>
R/B_x_n	O	<p>READY/BUSY OUTPUT The R/B_x_n output indicates the status of the target operation. When low, it indicates that one or more operations are in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.</p>
RE_x_n (RE_x_t)	I	<p>READ ENABLE The RE_x_n input is the serial data-out control. Toggle DDR Data is valid after the falling edge and rising edge of RE_x_n which also increments the internal column address counter by each one.</p>
RE_x_c	I	<p>Complement of Read Enable This is the complementary signal to Read Enable</p>
DQS_x (DQS_x_t)	I/O	<p>Data Strobe The data strobe signal that indicates the data valid window for Toggle DDR and Synchronous DDR data interface. Output with read data, input with write data. Edge-aligned with read data, centered in write data.</p>
DQS_x_c	I/O	<p>Complement of Data Strobe This is the complementary signal to Data Strobe.</p>
DBI_x	I/O	<p>Data Bus Inversion Optional pin/function for NAND device to reduce power consumption and power/noise during data input/output. The device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not.</p>

Table 2.6-1 — Pin Description (cont'd)

Name	Input/ Output	Description
WP_x_n ^{3,4}	I	WRITE PROTECT The WP_x_n disables the Flash array program and erase operations.
ODT_x_n ^{3,4}	I	ODT (On Die Termination) Pin This signal enables and disables termination on the NAND DQ, DQS, RE bus according to the specified set feature settings.
Vcc	I	POWER VCC is the power supply for device.
VccQ	I	I/O POWER The VccQ is the power supply for input and/or output signals.
VccQL	I	I/O POWER The VccQL is the power supply for input and/or output signals when PI-LTT mode is enabled.
Vss	I	GROUND The Vss signal is the power supply ground.
VssQ	I	I/O GROUND The VssQ signal is the ground for input and/or output signals
VSPx	n/a	Vendor Specific The function of these signals is defined and specified by the NAND vendor. Any VSP signal not used by the NAND vendor shall not be connected internal to the device.
VREFQ_DNU	n/a	VREFQ Do Not Use (DNU). External voltage reference optionally used on JESD230F or older NAND devices but not used by JESD230G NAND devices. This signal is a placeholder of the ball location of external VREFQ on the package ball map to prevent the balls from being used inadvertently for other purposes.
V _{PP}	I	High Voltage Power The V _{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g., improve power efficiency)
RZQ_x	Supply	Reference pin for ZQ calibration This is used on ZQ calibration and RZQ ball shall be connected to Vss through 300 ohm resistor
ENi / ENo	I/O	Enumeration pins These pins may be used for ONFI NAND
R	n/a	Reserved. These pins shall not be connected by host.
RFU	n/a	Reserved for Future Use These pins may be assigned for certain functions in the future
NU	n/a	Not Usable A pin that is not to be used in normal applications and that may or may not have an internal connection.
NC	n/a	No (internal) connection A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.

Table 2.6-1 — Pin Description (cont'd)

- NOTE 1 All Vcc, VccQ, VccQL, and Vss pins of each device shall be connected to common power supply outputs.
- NOTE 2 All Vcc, VccQ, VccQL, Vss, and VssQ shall not be disconnected.
- NOTE 3 Some vendors define WP_x_n pin as multi-function. User can use ODT_x_n instead of WP_x_n via set-feature. The default mode of this multi-function pin is WP_x_n.
- NOTE 4 WP/ODT mode selection should be set to WP before power-off to make the pin working as Write Protect for protecting against data corruption at power-off.

2.7 Pin Description (SCA Protocol)

Table 2.7-1 — Pin Description

Name	Input/ Output	Description
SCA_x	I	<p>Separate Command Address Pin</p> <p>This signal allows the NAND to select on power-up whether or not to enable the SCA protocol. When the SCA (Separate Command Address) protocol is enabled, the CLE_x, ALE_x, CEx_x_n, and WE_x_n signals in the conventional protocol are renamed as CA[1]_x, CA[0]_x, CA_CEx_x_n, and CA_CLK_x, respectively.</p>
IO0 ~ IO7(~ IO15) DQ0 ~ DQ7 DQ0_x ~ DQ7_x	I/O	<p>DATA INPUTS/OUTPUTS</p> <p>These signals are used to input data, and to output data during read operations. The input/output data signals are enabled/disabled via packets on the CA bus, and float to high-z when the chip is deselected or when the outputs are disabled. IO0 ~ IO15 are used in a 16-bit wide target configuration. With multi-channel support, IO0_0~IO7_0 and IO0_1~IO7_1 are used for IOs of channel 0 and IOs of channel 1 respectively. Also known as DQ0~DQ7 for Toggle DDR and Synchronous DDR.</p> <p>The number after the underscore represents the channel. For example, DQ0_0 indicates DQ0 of channel-0 and DQ0_1 does DQ0 of channel-1.</p>
CA[1:0]_x	I/O	<p>COMMAND/ADDRESS PACKET</p> <p>CA bus signals control the command/address packet type according to the SCA header definition table.</p>
CA_CEx_x_n	I	<p>COMMAND/ADDRESS BUS ENABLE</p> <p>The CA_CEx_x_n input enables the CA bus for the LUNs connected to that CA_CEx_x_n. When CA_CEx_x_n is low, the target CA bus is selected. When CA_CEx_x_n is high and the target is in the ready state, the target goes into a low-power standby state. When CA_CEx_x_n is high in the middle of a CA packet transaction, the packet transaction is aborted and the LUNs on the CA_CEx_x_n restart their command pointers. The number after the first underscore represents the channel. For example, CE0_0_n indicates CE0_n of channel-0 and CE0_1_n does CE0_n of channel-1.</p>
CA_CLK_x	I	<p>COMMAND/ADDRESS CLOCK</p> <p>The CA_CLK_x signal is a clock input. The CA bus signals are latched on the rising and falling edges of the CA_CLK_x pulse. The CA_CLK_x signal is default LOW while WE_x_n signal in the conventional protocol is default HIGH.</p>
ODT_x_n ^{3,4}	I	<p>ODT (On Die Termination) Pin</p> <p>This signal enables and disables termination on the NAND DQ, DQS, RE bus according to the specified set feature settings.</p>
R/B_x_n	O	<p>READY/BUSY OUTPUT</p> <p>The R/B_x_n output indicates the status of the target operation. When low, it indicates that one or more operations are in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.</p>
RE_x_n (RE_x_t)	I	<p>READ ENABLE</p> <p>The RE_x_n input is the serial data-out control. Toggle DDR Data is valid after the falling edge and rising edge of RE_x_n which also increments the internal column address counter by each one.</p>
RE_x_c	I	<p>Complement of Read Enable</p> <p>This is the complementary signal to Read Enable</p>

Table 2.7-1 — Pin Description (cont'd)

Name	Input/ Output	Description
DQS_x (DQS_x_t)	I/O	Data Strobe The data strobe signal that indicates the data valid window for Toggle DDR and Synchronous DDR data interface. Output with read data, input with write data. Edge-aligned with read data, centered in write data.
DQS_x_c	I/O	Complement of Data Strobe This is the complementary signal to Data Strobe.
DBI_x	I/O	Data Bus Inversion Optional pin/function for NAND device to reduce power consumption and power/noise during data input/output. The device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not.
WP_x_n ³	I	WRITE PROTECT The WP_x_n disables the Flash array program and erase operations.
Vcc	I	POWER VCC is the power supply for device.
VccQ	I	I/O POWER The VccQ is the power supply for input and/or output signals.
VccQL	I	I/O POWER The VccQL is the power supply for input and/or output signals when PI-LTT mode is enabled.
Vss	I	GROUND The Vss signal is the power supply ground.
VssQ	I	I/O GROUND The VssQ signal is the ground for input and/or output signals
VSPx	n/a	Vendor Specific The function of these signals is defined and specified by the NAND vendor. Any VSP signal not used by the NAND vendor shall not be connected internal to the device.
VREFQ_DNU	n/a	VREFQ Do Not Use (DNU). External voltage reference optionally used on JESD230F or older NAND devices but not used by JESD230G NAND devices. This signal is a placeholder of the ball location of external VREFQ on the package ball map to prevent the balls from being used inadvertently for other
V _{PP}	I	High Voltage Power The V _{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g., improve power efficiency)
RZQ_x	Supply	Reference pin for ZQ calibration This is used on ZQ calibration and RZQ ball shall be connected to Vss through 300 ohm resistor
R	n/a	Reserved. These pins shall not be connected by host.
RFU	n/a	Reserved for Future Use These pins may be assigned for certain functions in the future
NU	n/a	Not Usable A pin that is not to be used in normal applications and that may or may not have an internal connection.

Table 2.7-1 — Pin Description (cont'd)

Name	Input/ Output	Description
NC	n/a	No (internal) connection A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.

NOTE 1 All Vcc, VccQ, VccQL, and Vss pins of each device shall be connected to common power supply outputs.
NOTE 2 All Vcc, VccQ, VccQL, Vss and VssQ shall not be disconnected.

3 NAND Interface General Information

3.1 NAND Interface Spec Overview

Table 3.1-1 — NAND Interface Comparison Table

Interface Items	JESD230E	JESD230F	JESD230G / JESD230G.01
VCC	2.5 V/3.3 V (Optional)	2.5 V/3.3 V (Optional)	2.5 V
VCCQ	1.2 V	1.2 V	1.2 V
VCCQL	N/A	N/A	1.2 V or 0.6 V (optional)
DQ (Bus Width)	X8	X8	X8
Max Data Rate	~2.4 Gbps	~3.6 Gbps ⁹	~4.8 Gbps
OCD Topology	HSUL/CTT/LTT ^{1,2,3}	HSUL/CTT/LTT ^{1,2,3}	HSUL/LTT ^{1,3} (Required) PI-LTT ⁴ (optional)
Vref	Internal VrefQ is allowed for CTT ² > 200 Mbps, External VrefQ is optional for CTT ² > 200 Mbps, Internal VrefQ is required for LTT ³	Internal VrefQ is allowed for CTT ² > 200 Mbps, External VrefQ is optional for CTT ² > 200 Mbps, Internal VrefQ is required for LTT ³	Internal VrefQ is required for LTT ³ and PI-LTT ⁴
Input Path Topology	Matched DQS	Matched DQS or Unmatched DQS (see vendor datasheet)	Unmatched DQS
ODT ⁵ Control	ODT (nWP) pin or Matrix Termination	ODT (nWP) pin or Matrix Termination	ODT (nWP) pin or Matrix Termination for conventional protocol, NTO packet for SCA ⁶ protocol
Ron CAL	ZQ	ZQ	ZQ
CMD/ADDR IO	SDR (nWE sync, ~40 MHz – ~100 MHz)	SDR (nWE sync, ~40 MHz – ~100 MHz)	SCA protocol (Required) Conventional protocol: SDR (nWE sync, ~40 MHz – ~100 MHz) (optional),
DBI ⁷	Optional	Optional	Optional
Training	Write/Read DQ/DCC ⁸ /Internal VrefQ	Write/Read DQ/DCC ⁸ /Internal VrefQ, WDCA (optional), Write Training Monitor (optional), Per-pin VrefQ Adjustment (required), DQS oscillator (required), DFE (required)	Write/Read DQ/DCC ⁸ /Internal VrefQ, WDCA (required), RDCA (optional), Per-pin VrefQ Adjustment (required), DQS oscillator (required), DFE (required)
Differential Signaling on Power-up	Disabled	Vendor specific (see vendor datasheet)	Vendor specific (see vendor datasheet)
Equalization	Not Required	Optional and vendor specific	DFE 1-tap (required), DFE 4-tap (optional)
Fast Set/Get Features	Not Supported	Optional	Optional
ESD	N/A	N/A	HBM 1000 V / CDM 250 V
NOTE 1	HSUL: High Speed Unterminated Logic		
NOTE 2	CTT: Center Tapped Termination		
NOTE 3	LTT: Low Tapped Termination		
NOTE 4	PI-LTT: Power Isolated Low Tapped Termination		
NOTE 5	ODT: On Die Termination		
NOTE 6	SCA: Separate Command Address		
NOTE 7	DBI: Data Bus Inversion		
NOTE 8	DCC: Duty Cycle Correction		
NOTE 9	3.6 GT/s is not mandatory, NAND vendors may only support up to 3.2 GT/s (see vendor datasheet).		

3.2 Supported Features and Operating Conditions Versus Data Transfer Rate

Table 3.2-1 — Supported Features and Operating Conditions Versus Data Transfer Rate

Feature		~200Mbps	~400Mbps	~800Mbps	~1200Mbps ~1600Mbps ~2000Mbps ~2400Mbps	~2800Mbps ~3200Mbps	~3600Mbps ~4000Mbps ~4400Mbps ~4800Mbps					
VccQ		1.2 V										
PI-LTT (VccQL) (Optional)	NAND	0.6 V (Optional)										
	Host	0.6 V (Optional)										
I/O Type	Single-ended Signaling for DQS and RE ¹	NAND	Not supported	Not Supported								
	Differential Signaling for DQS and RE ¹	Host	Not supported ⁷									
ZQ Calibration		NAND	Supported									
		Host	Required ²	Required								
Training (DCC)		NAND	Not Supported			Required						
		Host										
Training (Read)		NAND	Supported									
		Host	Optional		Required							
Training (Write)		NAND	Supported									
		Host	Required									
Training (WDCA)		NAND	Optional				Supported					
		Host	Optional				Required					
Training (RDCA)		NAND	Optional				Optional					
		Host	Optional				Supported					
Training (Per-Pin VrefQ, 40h/41h)		NAND	Optional				Supported					
		Host	Optional				Required					
Training (Int VrefQ. 23h)		NAND	Supported									
		Host	Required									
On Die (NAND) Termination	CTT	NAND	Not Supported ³									
		Host	Not Supported ²									
	LTT	NAND	Supported									
		Host	Optional ⁴									
	PI-LTT (Optional)	NAND	Optional									
	Host	Optional ⁴										

Table 3.2-1 — Supported Features and Operating Conditions Versus Data Transfer Rate (cont'd)

Feature			~200Mbps	~400Mbps	~800Mbps	~1200Mbps	~1600Mbps	~2000Mbps	~2400Mbps	~2800Mbps	~3200Mbps	~3600Mbps	~4000Mbps	~4400Mbps	~4800Mbps	
Internal VrefQ	LTT	NAND				Supported ⁵										
		Host				Supported ⁵										
	PI-LTT (Optional)	NAND				Supported ⁵										
		Host				Supported ⁵										
Equalization (DFE)		NAND				Optional and Vendor Specific						Supported				
		Host				Optional and Vendor Specific						Required				
DQS Oscillator		NAND				Optional and Vendor Specific						Supported				
		Host				Optional and Vendor Specific						Supported				
Pausing Data Input/Output		NAND			Optional							Not supported				
		Host			Optional							Not supported				
Warm-up cycle		NAND			Optional							Supported				
		Host			Optional							Supported	Required			
Conventional protocol (command/address)		NAND				Optional ⁶										
		Host				Optional										
SCA protocol (command/address)		NAND				Required										
		Host				Supported										
<ul style="list-style-type: none"> • Optional = Host or NAND can Support or Not Support • Supported = Host or NAND supports feature but may not be required to use (dependency on application) • Required = Host or NAND is required to support feature and required to use the feature 																
NOTE 1	For LTT mode, Differential Signaling is always required, even below 200 Mbps.															
NOTE 2	Optional for controllers that also support JESD230F NAND devices															
NOTE 3	Supported on JESD230F devices, Not Supported on JESD230G devices															
NOTE 4	Host can enable/disable On Die (NAND) Termination															
NOTE 5	The host NAND shall power-up with the LTT interface enabled and with internal VrefQ. The host shall ensure that the NAND internal VrefQ is within the NAND minimum internal VrefQ allowable range allowed for the LTT/PI-LTT interface prior to enabling the LTT/PI-LTT interface, and at any time while the LTT/PI-LTT interface is active. External VrefQ shall always be disabled when the device runs in LTT/PI-LTT modes															
NOTE 6	Conventional protocol might not be supported on future JESD230G and later devices.															
NOTE 7	JESD230G compliant NAND controllers are required to power-up with differential DQS/RE for data input enabled (i.e., controller driving DQS_t, DQS_c, RE_t, and RE_c signals to their default states). However, to enable backward compatibility with JESD230F NAND devices (which can power-up with single-ended DQS/RE), it is recommended that JESD230G controllers, use single-ended DQS when read data from the NAND as power-up default (i.e., use DQS_t and ignore DQS_c) and provide a controller setting to enable using DQS_c for NAND reads at a later time.															

4 Physical Interface

4.1 Input Specifications

4.1.1 AC/DC Levels

4.1.1.1 LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals

Table 4.1-1 — LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals

Parameter	Symbol	Up to 1800Mbps	2000Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps 4000Mbps 4400Mbps 4800Mbps	Notes	Unit
DC input high for control signals	$V_{IH.CNT(DC)}$	0.7*VccQ	0.3*VccQ	0.8*VccQ	1	V
DC input low for control signals	$V_{IL.CNT(DC)}$					
AC input high for control signals	$V_{IH.CNT(AC)}$					
AC input low for control signals	$V_{IL.CNT(AC)}$					
DC input high for DQ-related signals (Unterminated)	$V_{IH.DQrel.unterm(DC)}$	0.5*VccQ	0.080	0.5*VccQ	2, 3, 7	V
DC input low for DQ-related signals (Unterminated)	$V_{IL.DQrel.unterm(DC)}$					
AC input high for DQ-related signals (Unterminated)	$V_{IH.DQrel.unterm(AC)}$					
AC input low for DQ-related signals (Unterminated)	$V_{IL.DQrel.unterm(AC)}$					
DC input high for DQ-related signals (Terminated)	$V_{IH.DQrel(DC)}$	$V_{cent_DQ_{rel}} + 0.080$	$V_{cent_DQ_{rel}} + 0.060$	$V_{cent_DQ_{rel}} + 0.060$	2, 4, 5	V
DC input low for DQ-related signals (Terminated)	$V_{IL.DQrel(DC)}$	$V_{cent_DQ_{rel}} - 0.080$	$V_{cent_DQ_{rel}} - 0.060$			

Table 4.1-1 — LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals (cont'd)

Parameter	Symbol	Up to 1800Mbps	2000Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps 4000Mbps 4400Mbps 4800Mbps	Notes	Unit
AC input high for DQ-related signals (Terminated)	V _{IH} .DQrel (AC)	V _{cent} _DQ _{rel} + 0.100		V _{cent} _DQ _{rel} + 0.085	2, 4, 6	
AC input low for DQ-related signals (Terminated)	V _{IL} .DQrel (AC)	V _{cent} _DQ _{rel} - 0.100		V _{cent} _DQ _{rel} - 0.085		
NOTE 1 Control signals are CE_n, WE_n, ODT_n/WP_n, ALE and CLE for conventional interface, and CA_CE_n, CA_CLK, CA[1:0], and SCA for SCA interface. NOTE 2 DQ-related signals are RE_t, RE_n, DQS_t, DQS_c, DQ[7:0] and DBI. For RE_t, RE_n, DQS_t, and DQS_c these are single-ended signal requirements. NOTE 3 Termination is disabled during command cycles, address cycles and during data input/output cycles when ODT from the NAND (target and non-target) and the controller are disabled. NOTE 4 V _{cent} _DQ _{rel} shall be regarded as V _{cent} _RE, V _{cent} _DQS, and V _{cent} _DQ for RE_t/RE_c, DQS_t/DQS_c, and DQ[7:0] signals, respectively. NOTE 5 For DQ signals, DC signal requirements are replaced with the Rx Mask NOTE 6 For DQ signals, AC signal requirements are replaced with the VIHL_AC specification. NOTE 7 NAND vendors may support a higher VIL.DQrel.unterm or lower VIH.DQrel.unterm specification. See vendor datasheet.						

Table 4.1-2 — LTT Interface Differential AC and DC Input Levels and Cross-Point

Parameter	Symbol	Up to 1800Mbps	2000Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps 4000Mbps 4400Mbps 4800Mbps	Notes	Unit
DC differential input	V _{ID} (DC)	0.160	0.160	0.120	1	V
AC differential input	V _{ID} (AC)	0.200	0.200	0.170		
AC differential input cross-point	V _{IX}	VREFDQ ± 0.064	VREFDQ ± 0.064	VREFDQ ± 0.054	2	
NOTE 1 VID(DC) and VID(AC) specify the input differential voltage VTR-VCP required for switching where VTR is the 'true' input signal while VCP is the 'complementary' input signal. The minimum values are equal to VIH(DC) – VIL(DC) and VIH(AC) – VIL(AC) respectively. NOTE 2 For LTT, the typical value of V _{IX} is expected to be about VREFDQ of the NAND Flash Memory internal setting value by VREF Training and V _{IX} is expected to track variations in VREFDQ. VIX indicates the voltage at which differential input signals must cross. NOTE 3 VIX value for unterminated condition is VSP						

4.1.1.2 PI-LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related

Table 4.1-3 — PI-LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals

Parameter	Symbol	Up to 1800Mbps	2000Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps 4000Mbps 4400Mbps 4800Mbps	Notes	Unit
DC input high for control signals	$V_{IH.CNT(DC)}$		0.7*VccQ		1	V
DC input low for control signals	$V_{IL.CNT(DC)}$		0.3*VccQ			
AC input high for control signals	$V_{IH.CNT(AC)}$		0.8*VccQ			
AC input low for control signals	$V_{IL.CNT(AC)}$		0.2*VccQ			
DC input high for DQ-related signals (Unterminated)	$V_{IH.DQrel.unterm(DC)}$		0.85*VccQL		2, 3, 7	V
DC input low for DQ-related signals (Unterminated)	$V_{IL.DQrel.unterm(DC)}$		0.080			
AC input high for DQ-related signals (Unterminated)	$V_{IH.DQrel.unterm(AC)}$		0.90*VccQL			
AC input low for DQ-related signals (Unterminated)	$V_{IL.DQrel.unterm(AC)}$		0.060			
DC input high for DQ-related signals (Terminated)	$V_{IH.DQrel(DC)}$	$V_{cent_DQ_{rel}} + 0.080$	$V_{cent_DQ_{rel}} + 0.060$		2, 4, 5	V
DC input low for DQ-related signals (Terminated)	$V_{IL.DQrel(DC)}$	$V_{cent_DQ_{rel}} - 0.080$	$V_{cent_DQ_{rel}} - 0.060$			
AC input high for DQ-related signals (Terminated)	$V_{IH.DQrel(AC)}$	$V_{cent_DQ_{rel}} + 0.100$	$V_{cent_DQ_{rel}} + 0.085$		2, 4, 6	V
AC input low for DQ-related signals (Terminated)	$V_{IL.DQrel(AC)}$	$V_{cent_DQ_{rel}} - 0.100$	$V_{cent_DQ_{rel}} - 0.085$			

Table 4.1-3 — PI-LTT Interface Single-Ended AC DC Input Levels for Control and DQ-Related Signals (cont'd)

NOTE 1	Control signals are CE_n, WE_n, ODT_n/WP_n, ALE and CLE for conventional interface, and CA_CE_n, CA_CLK, CA[1:0] and SCA for SCA interface.
NOTE 2	DQ-related signals are RE_t, RE_n, DQS_t, DQS_c, DQ[7:0], and DBI. For RE_t, RE_n, DQS_t, and DQS_c, these are single-ended signal requirements.
NOTE 3	Termination is disabled during command cycles, address cycles and during data input/output cycles when ODT from the NAND (target and non-target) and the controller are disabled.
NOTE 4	Vcent_DQrel shall be regarded as Vcent_RE, Vcent_DQS, and Vcent_DQ for RE_t/RE_c, DQS_t/DQS_c, and DQ[7:0] signals, respectively.
NOTE 5	For DQ signals, DC signal requirements are replaced with the Rx Mask
NOTE 6	For DQ signals, AC signal requirements are replaced with the VIHL_AC specification.
NOTE 7	NAND vendors may support a higher VIL.DQrel.unterm or lower VIH.DQrel.unterm specification. See vendor datasheet.

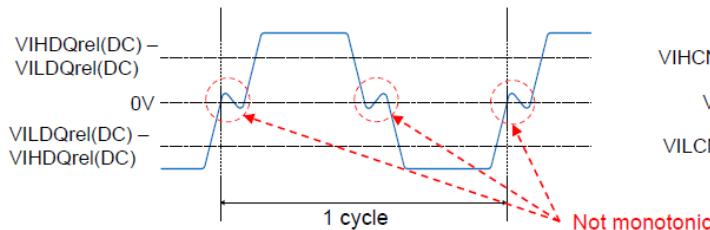
Table 4.1-4 — PI-LTT Interface Differential AC and DC Input Levels and Cross-Point

Parameter	Symbol	Up to 1800Mbps	2000Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps 4000Mbps 4400Mbps 4800Mbps	Notes	Unit
DC differential input	V _{ID} (DC)	0.160	0.160	0.120	1	V
AC differential input	V _{ID} (AC)	0.200	0.200	0.170		
AC differential input cross-point	V _{IX}	VREFDQ ± 0.064	VREFDQ ± 0.064	VREFDQ ± 0.054	2	
NOTE 1 VID(DC) and VID(AC) specify the input differential voltage VTR-VCP required for switching where VTR is the 'true' input signal while VCP is the 'complementary' input signal. The minimum values are equal to VIH(DC) – VIL(DC) and VIH(AC) – VIL(AC) respectively.						
NOTE 2 For PI-LTT, the typical value of V _{IX} is expected to be about VREFDQ of the NAND Flash Memory internal setting value by VREF Training and V _{IX} is expected to track variations in VREFDQ. VIX indicates the voltage at which differential input signals must cross.						
NOTE 3 VIX value for unterminated condition is VSP						

4.1.2 Input Waveform Definition

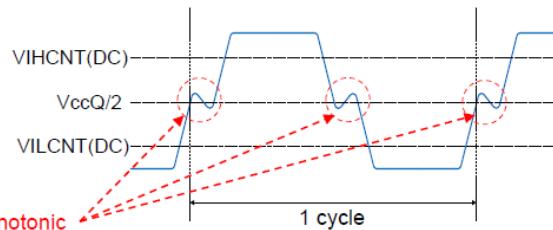
NAND circuitry becomes more and more susceptible to input waveform as interface speed goes up. The input waveform of "DQS_t-DQS_c", "RE_t-RE_c", and WE_n_x(CA_CLK_x) shall be monotonic slope. The range to keep monotonic slope in unterminated condition is VSP.

Input waveform of "DQS_t – DQS_c" and "RE_t – RE_c"



Waveform between "VIHDQrel(DC) - VILDQrel(DC)" and "VILDQrel(DC) - VIHDQrel(DC)" must be monotonic slope

Input waveform of WE_n(CA_CLK)



Waveform between VIHCNT(DC) and VILCNT(DC) must be monotonic slope

Figure 4.1-1— Input Waveform Definition

4.1.3 NAND DQ Rx Mask Specifications

The DQ input receiver (Rx) mask defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property and is not the valid data-eye. The DQ Rx mask for voltage and timing is shown in **Figure 4.1-2** and is applied per individual DQ pin. The DQ Rx mask is evaluated at the die pads and Rx mask values are guaranteed with DFE disable case only. When DFE is enabled, DFE setting versus coefficient values will be supplied by the NAND vendor. User can apply the coefficient to/on the input signal measured at the NAND die pads. The exact pass/fail criteria after co-efficient application can be supplied by the NAND vendor.

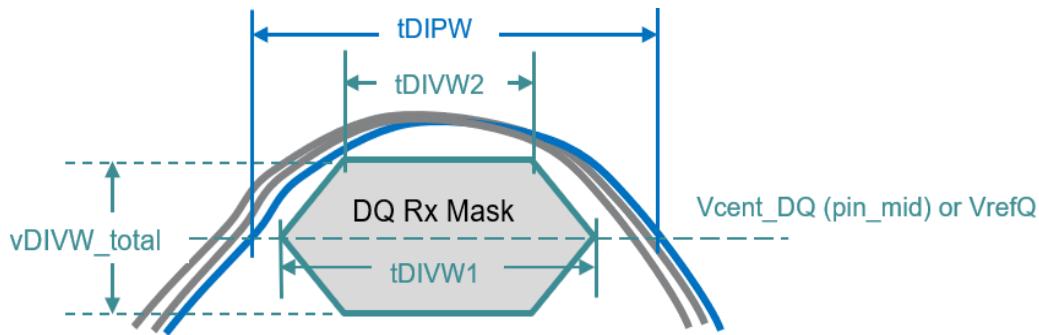


Figure 4.1-2 — DQ Rx Mask Definition

V_{cent_DQ} (pin_mid) is defined as the midpoint between the largest V_{cent_DQ} voltage level and the smallest V_{cent_DQ} voltage level across all DQ pins for a given NAND die.

Each V_{cent_DQ} is defined by the center (i.e., widest opening) of the cumulative data input eye as depicted in **Figure 4.1-3**.

Since the DQ Rx mask is centered around V_{cent_DQ} (pin_mid), any pin-to-pin V_{cent_DQ} variation must be accounted for in the DQ Rx Mask.

Similarly, $V_{cent_RE_t}$, $V_{cent_RE_c}$, $V_{cent_DQS_t}$, and $V_{cent_DQS_c}$ are defined by the center of the cumulative data input eye for RE_t, RE_c, DQS_t, and DQS_c, respectively. $V_{cent_RE_t}$ and $V_{cent_RE_c}$ are collectively denoted as V_{cent_RE} . $V_{cent_DQS_t}$ and $V_{cent_DQS_c}$ are collectively denoted as V_{cent_DQS} .

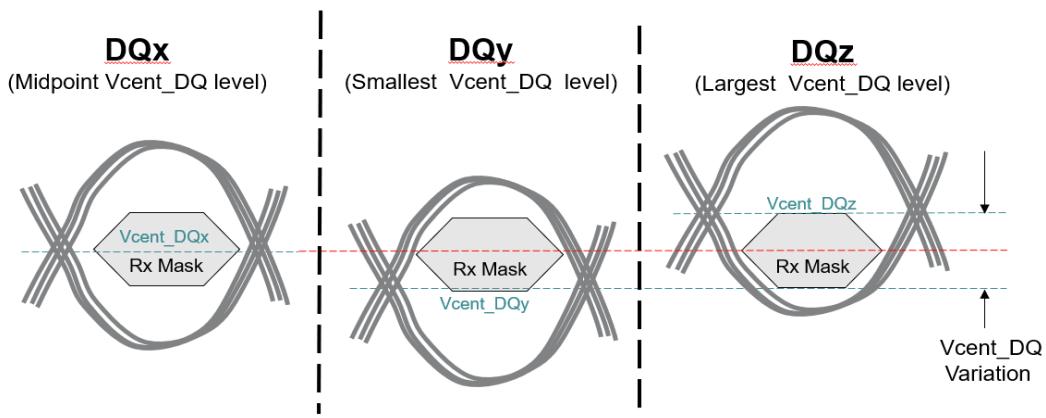


Figure 4.1-3 — V_{cent_DQ} (Pin_mid) Definition

4.1.3 NAND DQ Rx Mask Specifications (cont'd)

Table 4.1-5 — NAND LTT/PI-LTT Interface Rx Mask Specifications

Parameter	Symbol	Up to 1200Mbps	1200Mbps 1600Mbps 1800Mbps 2000Mbps	2200Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps ³	4000Mbps 4400Mbps 4800Mbps	Unit					
DQ Rx Mask Voltage Total	vDIVW	160	160	160	120	120	mV					
DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)	tDIVW1	0.48	0.48	0.48	0.41	0.41	UI					
DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	tDIVW2	0.30	0.30	0.30	0.23	0.23	UI					
DQ Input Pulse Width at Vcent_DQ (pin_mid)	tDIPW	0.62	0.62	0.62	0.66	0.66	UI					
DQ Rx minimum pulse width	tDIHL ⁴	tDIPW – (tDIVW1-tDIVW2)										
NOTE 1	Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where Internal VrefQ without Vref training is used.											
NOTE 2	Up to 1600 Mbps, use of Rx mask specifications is optional. See vendor datasheet whether Rx mask specifications are supported by the device at that data rate.											
NOTE 3	DQ Rx mask parameters (vDIVW_total, tDIVW1, tDIVW2, and tDIPW) are defined as 120 mV, 0.48UI, 0.3UI, and 0.66UI, respectively, on JESD230F devices											
NOTE 4	The DQ minimum pulse width is defined at the Vcent_DQ ± vDIVW_total/2. This parameter is not tested in production and verified by design.											

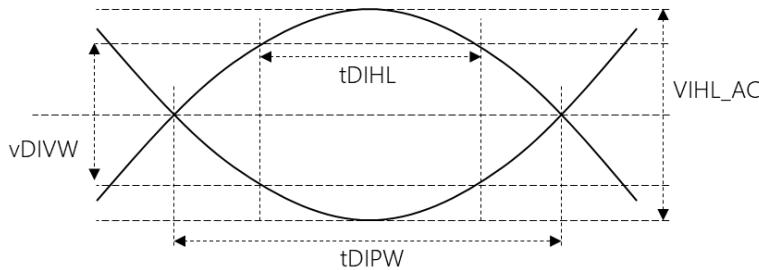


Figure 4.1-4 — DQ Minimum Pulse Width Definition (tDIHL)

4.1.4 Controller DQ Rx Mask Specifications

The Controller DQ RX Mask specifications in this clause are applicable to controllers that support the data rates listed in **Table 4.1-6**.

Table 4.1-6 — Controller LTT/PI-LTT Interface Rx Mask Specifications

Parameter	Symbol	2000Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps	4000Mbps 4400Mbps 4800Mbps	Unit
DQ Rx Mask Voltage Total	vDIVW_total	160	120	100	mV
DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)	tDIVW1	0.40	0.40	0.35	UI
DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	tDIVW2	0.25	0.25	0.18	UI
DQ Input Pulse Width at Vcent_DQ (pin_mid)	tDIPW	0.50	0.50	0.45	UI

NOTES:

- 1) The controller DQ Rx mask specification is only for reference and smaller value might be required depending on system. System designers should use IBIS model to close overall system timings

4.1.5 LTT Interface (1.2V VccQ) and PI-LTT Interface (0.6V VccQL) VIHL_AC Definition

The minimum DQ AC input pulse amplitude (pk-pk) is given by the VIHL_AC specification.

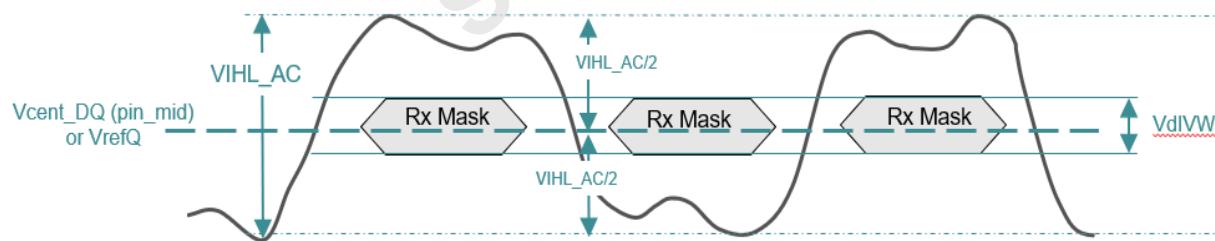


Figure 4.1-5 — VIHL_AC Definition

Table 4.1-7 — VIHL_AC Specifications

Parameter	Symbol	Up to 1800Mbps	2000Mbps 2400Mbps 2800Mbps 3200Mbps	3600Mbps 4000Mbps 4400Mbps 4800Mbps	Notes	Unit
DQ AC input pulse amplitude pk-pk	VIHL_AC_LTT	200	200	170	1, 2, 3	mV
	VIHL_AC_PI-LTT	200	200	170		

4.1.5 LTT Interface (1.2V VccQ) and PI-LTT Interface (0.6V VccQL) VIHL_AC Definition (cont'd)

Table 4.1-7 — VIHL_AC Specifications (cont'd)

NOTE 1	The DQ only input pulse amplitude must meet or exceed VIHL_AC at any point over the total UI, except when no transitions are occurring for that UI.
NOTE 2	VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). Vcent_DQ (pin_mid) is replaced by VrefQ as the center reference level in the case where Internal VrefQ without Vref training is used.
NOTE 3	There are no timing requirements above or below VIHL_AC levels.

4.1.6 NAND Minimum Internal VrefQ Allowable Range

Table 4.1-8 — NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Internal VrefQ Value1 and Value2 Settings (1.2V VccQ, 0.6V VccQL)

Interface	Parameter	Symbol	Min	Max	Notes	Unit	
LTT	Minimum allowable range upper limit	VrefQ_LTT_HI	-	40%	1, 2, 3	VccQ	
	Minimum allowable range lower limit	VrefQ_LTT_LO	160	-		mV	
PI-LTT	Minimum allowable range upper limit	VrefQ_PI-LTT_HI	-	60%	1, 2, 3	VccQL	
	Minimum allowable range lower limit	VrefQ_PI-LTT_LO	80	-		mV	
NOTE 1	The host shall not set the NAND internal VrefQ to a setting beyond the allowable range even during Write Training Internal VrefQ training.						
NOTE 2	These specs define the allowable range for NAND internal VrefQ settings but do not represent the needed settings for high speed operations. The needed settings for high speed operations are obtained from either NAND vendor recommendation or through Internal VrefQ Training.						
NOTE 3	Some NAND device may offer a wider allowable range. See vendor datasheet.						

Table 4.1-9 — NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Internal VrefQ Value3 Settings (1.2V VccQ, 0.6V VccQL)

Interface	Parameter	Symbol	Min	Max	Notes	Unit	
LTT	Minimum allowable range upper limit	VrefQ_LTT_HI	-	31.75%	1, 2, 3	VccQ	
	Minimum allowable range lower limit	VrefQ_LTT_LO	160	-		mV	
PI-LTT	Minimum allowable range upper limit	VrefQ_PI-LTT_HI	-	50%	1, 2, 3	VccQL	
	Minimum allowable range lower limit	VrefQ_PI-LTT_LO	80	-		mV	
NOTE 1	The host shall not set the NAND internal VrefQ to a setting beyond the allowable range even during Write Training Internal VrefQ training.						
NOTE 2	These specs define the allowable range for NAND internal VrefQ settings but do not represent the needed settings for high speed operations. The needed settings for high speed operations are obtained from either NAND vendor recommendation or through Internal VrefQ Training.						
NOTE 3	Some NAND device may offer a wider allowable range. See vendor datasheet.						

4.2 Output Specifications

4.2.1 Output Drive and ODT Strengths

4.2.1.1 LTT Interface Drive Strengths

4.2.1.1.1 LTT Interface Pull-Down

Table 4.2-1 — LTT Interface Allowed Pull-Down Drive Strengths

R _{ONPD}	
[ohm]	Unit
25	RZQ/12
37.5 (PDDS Location2 Default)	RZQ/8
42.9	RZQ/7
50 (PDDS Location1 Default)	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1

NOTES:

- 1) For R_{ONPD} values, 37.5 Ω and 50 Ω are mandatory while the rest are vendor specific.
- 2) With ZQ Calibration, R_{ONPD} tolerance from the nominal value is ±15% (when measured at a pad voltage of V_{OH,nom})
- 3) The default value when PDDS bit locations are in Location1 (see Feature Address 22h) is 50 Ω while the default value when PDDS bit locations are in Location2 (see Feature Address 10h) is 37.5 Ω.
- 4) Since the default output pull-down drive strength values may be different among NAND vendors, the NAND LTT pull-down shall be configured by the host to the desired value prior to enabling the LTT interface.

4.2.1.1.2 LTT Interface Pull-Up

Table 4.2-2 — Allowable V_{OH,LTT,nom} Configurations (LTT)

V _{OHPu,nom}	V _{OH,nom} (mV) @1.2v V _{CCQ}	Min	Nom	Max	Unit
V _{CCQ} /3 (default)	400	0.85	1.0	1.15	V _{OH,LTT,nom}
V _{CCQ} /2.5 (optional)	480	0.85	1.0	1.15	V _{OH,LTT,nom}

NOTES:

- 1) V_{OH,LTT,nom} = V_{CCQ}/3 is mandatory and shall be the default, while V_{OH,LTT,nom} = V_{CCQ}/2.5 is optional.
- 2) V_{OH,nom} accuracy requirements are after ZQ calibration with an RZQ of 300 ohm ±1%
- 3) V_{OH,nom} accuracy requirements only apply at valid CH_ODT values

4.2.1.1.2 LTT Interface Pull-Up (cont'd)

Table 4.2-3 — Allowable CH_ODT Configurations (LTT)

Channel ODT Setting		VOH.LTT,nom	
[ohm]	Unit	VccQ/3	VccQ/2.5
25	RZQ/12	Valid	Valid
37.5	RZQ/8	Valid	Valid
42.9	RZQ/7	Valid	Valid
50	RZQ/6	Valid (default)	Valid
60	RZQ/5	Valid	Valid
75	RZQ/4	Valid	Valid
100	RZQ/3	Valid	Valid
150	RZQ/2	Valid	Valid
300	RZQ/1	Valid	Valid

NOTES:

- 1) Support for CH_ODT value of 50 Ω when VOH.LTT,nom = VccQ/3 is mandatory and shall be the default setting. Support for other CH_ODT values is vendor specific.
- 2) Support for VOH.LTT,nom = VccQ/2.5 is optional. When VOH.LTT,nom = VccQ/2.5 is supported by a device, the CH_ODT configurations that are supported as well as the default value are vendor specific.

4.2.1.2 LTT Interface ODT

Table 4.2-4 — Allowable NAND ODT Rtt Values for LTT Interfaces

Rtt	
[ohm]	Unit
25	RZQ/12
37.5	RZQ/8
42.9	RZQ/7
50	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1
Disabled (Default)	N/A

NOTES:

- 1) The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific.

4.2.1.2 LTT Interface ODT (cont'd)

Table 4.2-5 — ODT Accuracy Specifications

Interface	V _{OUT}	Min	Nom	Max	Notes	Unit
LTT	0.1*V _{CCQ}	0.75	1.0	1.15	1	RZQ/n
	0.33*V _{CCQ}	0.85	1.0	1.15		
	0.5*V _{CCQ}	0.85	1.0	1.35		

NOTE 1 All values are after ZQ calibration.

4.2.1.3 PI-LTT Interface Drive Strengths

4.2.1.3.1 PI-LTT Interface Pull-Down

Table 4.2-6 — PI-LTT Interface Allowed Pull-Down Drive Strengths

R _{ONPD}	
[ohm]	Unit
37.5 (PDDS Location2 Default)	RZQ/8
42.9 (optional)	RZQ/7
50 (PDDS Location1 Default)	RZQ/6
60 (optional)	RZQ/5
75 (optional)	RZQ/4
100 (optional)	RZQ/3
150 (optional)	RZQ/2
300 (optional)	RZQ/1

NOTES:

- 1) For R_{ONPD} values, 37.5 Ω and 50 Ω are mandatory while the rest are vendor specific.
- 2) With ZQ Calibration, R_{ONPD} tolerance from the nominal value is ±15% (when measured at a pad voltage of V_{OH_nom})
- 3) The default value when PDDS bit locations are in Location1 (see Feature Address 22h) is 50 Ω while the default value when PDDS bit locations are in Location2 (see Feature Address 10h) is 37.5 Ω.
- 4) Since the default output pull-down drive strength values may be different among NAND vendors, the NAND PI-LTT pull-down shall be configured by the host to the desired value prior to enabling the PI-LTT interface.

4.2.1.3.2 PI-LTT Interface Pull-Up

Table 4.2-7 — Allowable VOH.PI-LTT,nom Configurations (PI-LTT)

VOHpu,nom	VOH.PI-LTT,nom (mV) @0.6v VccQL	Min	Nom	Max	Unit
VccQL/2 (default)	300	0.85	1.0	1.15	VOH.PI-LTT, nom

NOTES:

- 1) VOH.PI-LTT,nom = VccQL/2 is mandatory and shall be the default
- 2) VOH.nom accuracy requirements are after ZQ calibration
- 3) VOH,nom accuracy requirements only apply at valid CH_ODT values

Table 4.2-8 — Allowable CH_ODT Configurations (PI-LTT)

Channel ODT Setting		VOH.PI-LTT,nom
[ohm]	Unit	VccQL/2
37.5	RZQ/8	Valid
42.9	RZQ/7	Valid
50	RZQ/6	Valid (default)
60	RZQ/5	Valid
75	RZQ/4	Valid
100	RZQ/3	Valid
150	RZQ/2	Valid
300	RZQ/1	Valid

NOTES:

- 1) Support for CH_ODT value of 50 Ω when VOH.PI-LTT,nom = VccQL/2 is mandatory and shall be the default setting. Support for other CH_ODT values is vendor specific.

4.2.1.4 PI-LTT Interface ODT

Table 4.2-9 — Allowable NAND ODT Rtt Values for PI-LTT Interfaces

Rtt	
[ohm]	Unit
37.5	RZQ/8
42.9	RZQ/7
50	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1
Disabled (Default)	N/A

NOTES:

- 1) The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific.

Table 4.2-10 — ODT Accuracy Specifications

Interface	VOUT	Min	Nom	Max	Notes	Unit
PI-LTT	0.5*VccQL	0.85	1.0	1.15	1	RZQ/n
NOTE 1 All values are after ZQ calibration.						

4.2.2 Output Levels for Unterminated Single-Ended DQ-Related Signals

Table 4.2-11 — Single-Ended AC and DC Output Levels for Unterminated DQ-Related Signals (LTT)

Interface	Parameter	Symbol	Min	Max	Notes	Unit		
LTT	DC Output High DQ-related signals (Unterminated)	$V_{OH.DQrel.unterm}(DC)$	0.5*VccQ	-	1, 2, 3	V		
	DC Output Low DQ-related signals (Unterminated)	$V_{OL.DQrel.unterm}(DC)$	-	0.080				
	AC Output High DQ-related signals (Unterminated)	$V_{OH.DQrel.unterm}(AC)$	0.5*VccQ	-				
	AC Output Low DQ-related signals (Unterminated)	$V_{OL.DQrel.unterm}(AC)$	-	0.060				
NOTE 1 DQ-Related signals are DQS_t/DQS_c, DQs, and DBI								
NOTE 2 Evaluated using Output Timing Reference Load for Unterminated Channel, with default PDSS and CH_ODT settings								
NOTE 3 These specs shall be met when tRC(avg) \geq 30 ns.								

4.2.2 Output Levels for Unterminated Single-Ended DQ-Related Signals (cont'd)

Table 4.2-12 — Single-Ended AC and DC Output Levels for Unterminated DQ-Related Signals (PI-LTT)

Interface	Parameter	Symbol	Min	Max	Notes	Unit
PI-LTT	DC Output High DQ-related signals (Unterminated)	$V_{OH.DQrel.unterm}(DC)$	0.85*VccQL	-	1, 2, 3	V
	DC Output Low DQ-related signals (Unterminated)	$V_{OL.DQrel.unterm}(DC)$	-	0.080		
	AC Output High DQ-related signals (Unterminated)	$V_{OH.DQrel.unterm}(AC)$	0.9*VccQL	-		
	AC Output Low DQ-related signals (Unterminated)	$V_{OL.DQrel.unterm}(AC)$	-	0.060		

NOTE 1 DQ-Related signals are DQS_t/DQS_c, DQs, and DBI
 NOTE 2 Evaluated using Output Timing Reference Load for Unterminated Channel, with default PDDS and CH_ODT settings
 NOTE 3 These specs shall be met when tRC(avg) \geq 30 ns.

4.2.3 Output Timing Reference Loads

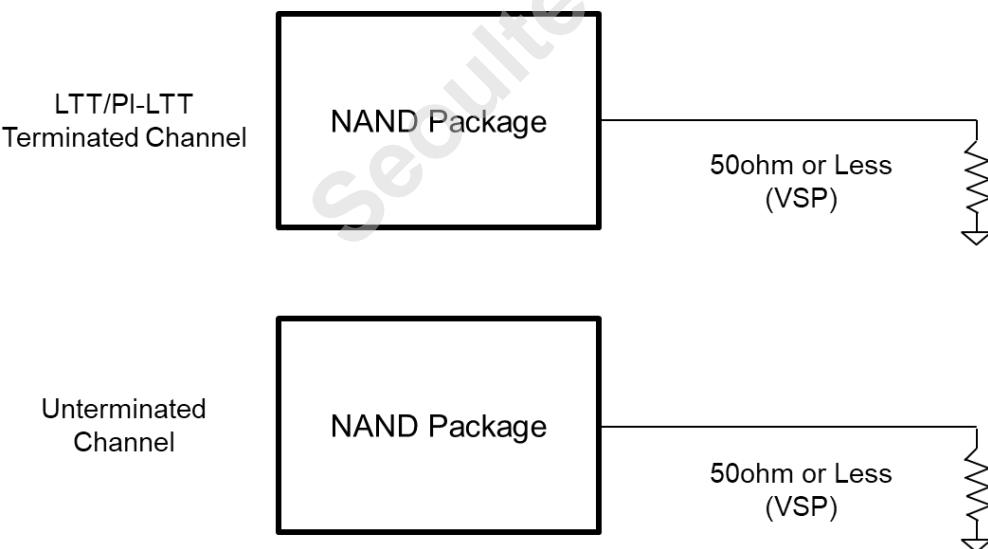


Figure 4.2-1 — Output Timing Reference Loads for Timing

The “Output Timing Reference Loads” are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to their system environment.

4.2.3 Output Timing Reference Loads (cont'd)

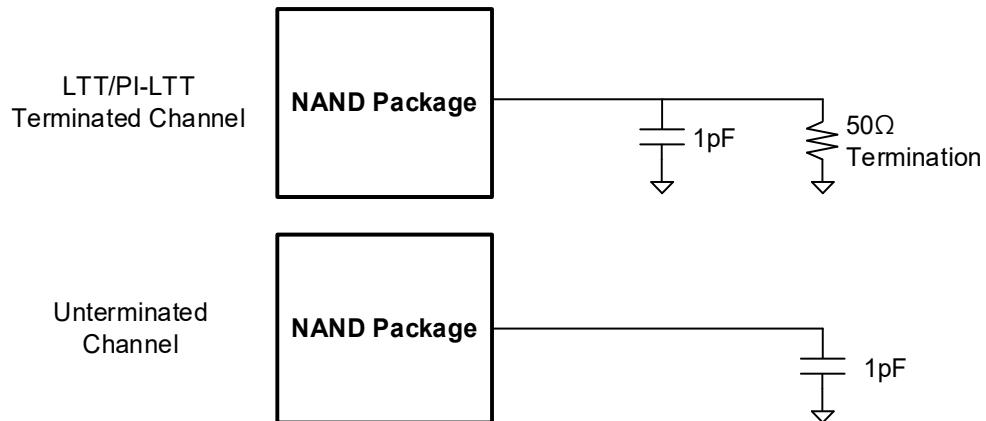


Figure 4.2-2 — Output Reference Loads for Slew Rate

The “Output Reference Loads for Slew Rate” are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester.

4.2.4 Single-Ended Output Slew Rate

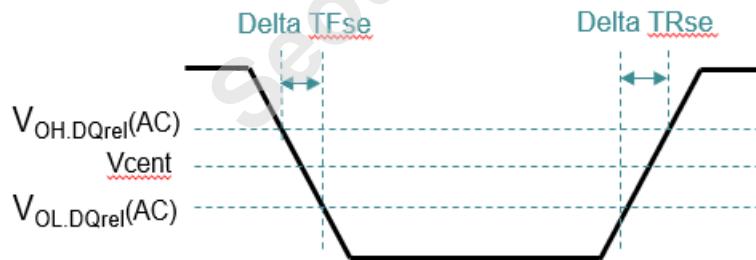


Figure 4.2-3 — Output Slew Rate Measurement

Table 4.2-13 — Single-Ended Output Slew Rate Measurement Levels for Terminated DQ-Related Signals

Description	Measured From	Measured To	Defined By
Single-ended output slew rate for falling edge	$V_{OH,DQrel(AC)}$	$V_{OL,DQrel(AC)}$	$[V_{OH,DQrel(AC)} - V_{OL,DQrel(AC)}] / \Delta TFse$
Single-ended output slew rate for rising edge	$V_{OL,DQrel(AC)}$	$V_{OH,DQrel(AC)}$	$[V_{OH,DQrel(AC)} - V_{OL,DQrel(AC)}] / \Delta TRse$

NOTES:

- 1) The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific.

4.2.4 Single-Ended Output Slew Rate (cont'd)

Table 4.2-14 — Single-Ended Output Slew Rate Measurement Levels for Terminated DQ-Related Signals

Interface	Parameter	Symbol	Level	Unit
LTT	AC Output high for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OH,Dqrel}$ (AC)	$0.8*V_{OH,LTT,nom}$	V
	AC Output low for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OL,Dqrel}$ (AC)	$0.2*V_{OH,LTT,nom}$	
PI-LTT	AC Output high for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OH,Dqrel}$ (AC)	$0.8*V_{OH,PI-LTT,nom}$	V
	AC Output low for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OL,Dqrel}$ (AC)	$0.2*V_{OH,PI-LTT,nom}$	

NOTES:

- 1) The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific.
- 2) Measured with Output Timing Reference Load for Terminated Channel

4.2.5 Output Specifications for R/B# Signal

Table 4.2-15 — AC/DC Specifications for R/B# Signal (LTT)

Parameter	Symbol	1.2V VccQ (LTT)	Notes	Unit
DC Output high for control signals (optional)	$V_{OH,CNT}$ (DC)	$0.7*V_{ccQ}$ (min)	1, 2	V
DC Output low for control signals	$V_{OL,CNT}$ (DC)	$0.3*V_{ccQ}$ (max)		
AC Output high for control signals (optional)	$V_{OH,CNT}$ (AC)	$0.8*V_{ccQ}$ (min)		
AC Output low for control signals (optional)	$V_{OL,CNT}$ (AC)	$0.2*V_{ccQ}$ (max)		
NOTE 1 Control signals are R/B_n				
NOTE 2 $V_{OL,CNT(DC)}$ (max) is specified with an IOL (R/B_n) of 3 mA				

4.2.5 Output Specifications for R/B# Signal (cont'd)

Table 4.2-16 — AC/DC Specifications for R/B# Signal (PI-LTT)

Parameter	Symbol	0.6V VccQL (PI-LTT)	Notes	Unit
DC Output high for control signals (optional)	$V_{OH,CNT}(\text{DC})$	0.7*VccQ (min)	1, 2	V
DC Output low for control signals	$V_{OL,CNT}(\text{DC})$	0.3*VccQ (max)		
AC Output high for control signals (optional)	$V_{OH,CNT}(\text{AC})$	0.8*VccQ (min)		
AC Output low for control signals (optional)	$V_{OL,CNT}(\text{AC})$	0.2*VccQ (max)		
NOTE 1 Control signals are R/B_n				
NOTE 2 $V_{OL,CNT}(\text{DC})$ (max) is specified with an IOL (R/B_n) of 3 mA				

4.3 AC Overshoot/Uncertain Requirements

The device may have AC overshoot or undershoot from V_{CCQ} and V_{SSQ} levels. **Table 4.3-1** and **Table 4.3-2** define the maximum values that the AC overshoot or undershoot may attain. These values apply for 1.2V VccQ and 0.6V VccQL levels for LTT and PI-LTT, respectively.

Table 4.3-1 — LTT and PI-LTT interface AC Overshoot/Uncertain Specifications (~200 MHz - ~600 MHz)

Parameter	Maximum Value						Unit
	~200 MHz	~266 MHz	~333 MHz	~400 MHz	~533 MHz	~600 MHz	
Max. peak amplitude allowed for overshoot area	0.40	0.30	0.24	0.20	0.15	0.13	V
Max. peak amplitude allowed for undershoot area	0.40	0.30	0.24	0.20	0.15	0.13	
Max. overshoot area above VccQ/VccQL	0.40	0.30	0.24	0.20	0.15	0.13	V*ns
Max. undershoot area below VssQ	0.40	0.30	0.24	0.20	0.15	0.13	
NOTE 1 This standard is intended for devices with no clamp protection and is guaranteed by design.							

4.3 AC Overshoot/Undershoot Requirements (cont'd)

**Table 4.3-2—LTT and PI-LTT interface AC Overshoot/Undershoot Specifications
(~800 MHz - ~1200 MHz)**

Parameter	Maximum Value					Unit
	~800 MHz	~900 MHz	~1000 MHz	~1100 MHz	~1200 MHz	
Max. peak amplitude allowed for overshoot area	0.30					
Max. peak amplitude allowed for undershoot area	0.30					
Max. overshoot area above VccQ/VccQL	0.10	0.09	0.08	0.073	0.067	V*ns
Max. undershoot area below VssQ	0.10	0.09	0.08	0.073	0.067	
NOTE 1 This standard is intended for devices with no clamp protection and is guaranteed by design.						

**Table 4.3-3—LTT and PI-LTT interface AC Overshoot/Undershoot Specifications
(~1400 MHz - ~2400 MHz)**

Parameter	Maximum Value						Unit
	~1400 MHz	~1600 MHz	~1800 MHz	~2000 MHz	~2200 MHz	~2400 MHz	
Max. peak amplitude allowed for overshoot area	0.30						
Max. peak amplitude allowed for undershoot area	0.30						
Max. overshoot area above VccQ/VccQL	0.057	0.050	0.044	0.04	0.036	0.033	V*ns
Max. undershoot area below VssQ	0.057	0.050	0.044	0.04	0.036	0.033	
NOTE 1 This standard is intended for devices with no clamp protection and is guaranteed by design.							

4.3 AC Overshoot/Undershoot Requirements (cont'd)

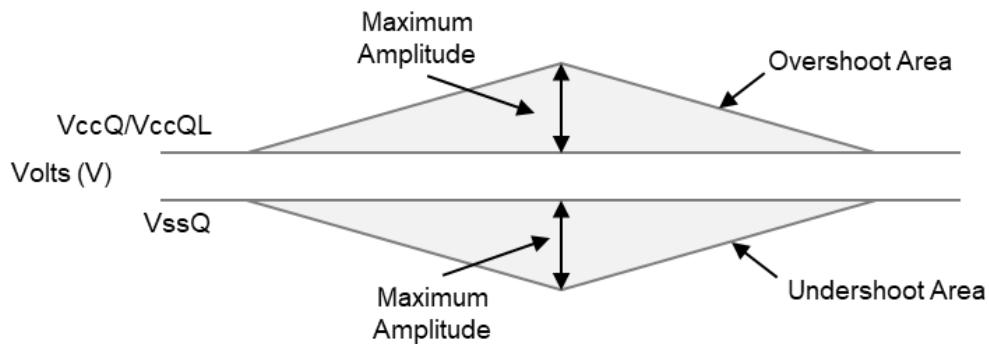


Figure 4.3-1 — Overshoot/Undershoot Diagram

4.4 Recommended DC Operating Conditions

4.4.1 DC Supply Voltage

Table 4.4-1 — Supply Voltage Parameter Description

Parameter	Symbol	Low Freq Voltage Spec (TBD) Freq: DC to 2 MHz			
		Min	Typ	Max	Units
Supply voltage for 2.5 V devices	V _{CC} ^{2,3}	2.35	2.5	2.75	V
Supply voltage for 1.2 V I/O signaling	V _{CCQ} ^{2,3}	1.14	1.2	1.26	V
Supply voltage for 0.6 V I/O signaling	V _{CCQL} ^{2,3}	0.57	0.6	0.63	V
Ground voltage supply	V _{SS}	0	0	0	V
Ground voltage supply for I/O signaling	V _{SSQ}	0	0	0	V
External voltage supply	V _{PP} ¹	10.8	12.0	13.2	V
NOTE 1 The maximum external voltage supply (I _{PP}) is 15 mA per LUN.					
NOTE 2 AC noise requirements on V _{CC} , V _{CCQ} , and V _{CCQL} are following					
a) From DC to 20 MHz, the AC noise shall be less than +/- 3% of nominal voltage. b) From 20 MHz to 2400 MHz, the AC noise shall be less than +/- 3% of nominal voltage. If the AC noise is more than +/- 1% of the nominal voltage, a different vendor specific AC Timing value may be specified. c) More than 2400 MHz, the AC noise shall be less than +/- 3% of the nominal voltage. With AC and DC noise together, the supply value at the NAND ball shall stay within the Min-Max range specified in this table.					
NOTE 3 AC noise is included in V _{CC} , V _{CCQ} , and V _{CCQL} Min/Max range.					

4.4.1 DC Supply Voltage (cont'd)

Table 4.4-1a — Supply Voltage Parameter Description

Parameter	Symbol	Z(f) Spec (TBD) Freq: 2 MHz to 10 MHz		Z(f) Spec (TBD) Freq: 20 MHz	
		Zmax	Unit	Zmax	Unit
Supply voltage for 2.5 V devices	Vcc ^{1,2}	TBD	-	TBD	-
Supply voltage for 1.2 V I/O signaling	VccQ ^{1,2}	10 (TBD)	mΩ	20 (TBD)	mΩ
Supply voltage for 0.6 V I/O signaling	VccQL ^{1,2}	10 (TBD)	mΩ	20 (TBD)	mΩ
External voltage supply	Vpp ^{1,2}	TBD	-	TBD	-

NOTE 1 Z(f) is defined for all pins per voltage domain.
 NOTE 2 Z(f) does not include the NAND package and silicon die.

4.4.2 DC Output Leakage Current Requirements for 1.2V VccQ and 0.6V VccQL

Table 4.4-2 — DC Output Leakage Current Requirements (ILO) for Conditions for 1.2V VccQ and 0.6V VccQL

Symbol	Parameter	Max
ILOpd	Pull-Down Output leakage current, VOUT=VccQ, VccQL	20 μA ^{1, 2}
ILOpu	Pull-Up Output leakage current, VOUT=0V	20 μA ^{1, 2}
NOTE 1 Absolute leakage value per DQ pin per NAND die. The following signals are required to meet output leakage (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, DBI, R/B_n, CA[1:0], RZQ (without ZQ Ext-Resistance))		
NOTE 2 DQ, DBI, R/B_n, and CA[1:0] are disabled; ODT disabled		

4.5 Absolute Maximum DC Ratings

Stresses greater than those listed in **Table 4.5-1** may cause permanent damage to the device. This is a stress rating only. Operation beyond the recommended operating conditions specified in **Table 4.1-1** is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability. **Table 4.5-1** defines the voltage on any pin relative on Vss and/or VssQ for devices based on their Vcc, VccQ, and VccQL typical voltages.

Table 4.5-1 — Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Units
VPP Supply Voltage	V _{pp}	-0.6 to +16	V
<i>V_{cc} = 2.5 V and V_{ccQ} = 1.2 V nominal</i>			
VCC Supply Voltage	V _{cc}	-0.3 to +3.2	V
Voltage Input	V _{IN}	-0.2 to +1.5	V
VCCQ Supply Voltage	V _{ccQ}	-0.2 to +1.5	V
<i>V_{cc} = 2.5 V and V_{ccQL} = 0.6 V nominal</i>			
VCC Supply Voltage	V _{cc}	-0.3 to +3.2	V
Voltage Input	V _{IN}	-0.2 to +1.5	V
VCCQL Supply Voltage	V _{ccQL}	-0.2 to +1.5	V
<i>V_{cc} = 1.8 V and V_{ccQ} = 1.2 V nominal</i>			
VCC Supply Voltage	V _{cc}	-0.2 to +2.4	V
Voltage Input	V _{IN}	-0.2 to +2.4	V
VCCQ Supply Voltage	V _{ccQ}	-0.2 to +1.5	V

4.6 Electrostatic Discharge Sensitivity Characteristics

Table 4.6-1 — Electrostatic Discharge Sensitivity Characteristics

Symbol	Parameter ¹	Min	Max	Unit
ESD _{HBM}	Human Body Model (HBM) ²	1000	-	V
ESD _{CDM}	Charged-device model (CDM) ³	250	-	V
NOTE 1 State-of-the-art basic ESD control measures have to be in place when handling devices				
NOTE 2 Refer to ESDA / JEDEC Joint Standard JS-001 for measurement procedures				
NOTE 3 Refer to ESDA / JEDEC Joint Standard JS-002 for measurement procedures				

5 Package and Addressing

SCA balls allow the NAND to select on power-up whether to enable the Conv. of SCA protocol. The subsequent figures show the location of the SCA balls on different NAND package ball maps.

5.1 BGA-63 (Single x8 / x16 BGA)

Figure 5.1-1 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 8-bit data access for the synchronous DDR data interface.

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C		WP_n	ALE	VSS	CE0_n	NC	R/B0_n			
D		VCC	W/R_n or RE_0_n	CLE	CE1_n	CE2_n	R/B1_n			
E		NC	NC	NC	NC	CE3_n	R/B2_n			
F		NC	NC	VREFQ	NC	VSS	R/B3_n			
G		VSP3	VCC	VSP1	NC	NC	VSP2			
H		NC	DQ0	DQS_c	CK_c	CK or WE_0_n	VCCQ			
J		NC	DQ1	DQS	VCCQ	DQ5	DQ7			
K		VSSQ	DQ2	DQ3	DQ4	DQ6	VSSQ			
L	NC	NC							NC	NC
M	NC	NC							NC	NC

NOTE 1 WE_n is located at ball H7 when a Synchronous DDR capable part is used in asynchronous SDR mode.

Figure 5.1-1 — Ball Assignments for 8-Bit Data Access, Synchronous DDR Data Interface

5.2 BGA-100 (Dual x8 BGA)

Figure 5.2-1 defines the ball assignments for devices using NAND Dual x8 BGA packaging with dual 8-bit data access for the Toggle DDR or Synchronous DDR data interface. The minimum package size is 12x18 mm and the maximum package size is 14x18 mm.

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R								R	
C										
D		R	VSP	VSP2_1	WP_1_n	VSP1_1	VSP0_1	VSP	R	
E		R	VSP	VSP2_0	WP_0_n	VSP1_0	VSP0_0	VSP	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H										
J		VSSQ	VCCQ	VREFQ_1	VREFQ_0	R/B0_1_n	R/B1_0_n or ENo	VCCQ	VSSQ	
K		DQ0_1	DQ2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	DQ5_1	DQ7_1	
L		DQ0_0	DQ2_0	ALE_0	CE1_0_n or ENi	CE0_1_n	CE0_0_n	DQ5_0	DQ7_0	
M		VCCQ	VSSQ	VCCQ	CLE_1	W/R_1_n or RE_1_n	VCCQ	VSSQ	VCCQ	
N		DQ1_1	DQ3_1	VSSQ	CLE_0	W/R_0_n or RE_0_n	VSSQ	DQ4_1	DQ6_1	
P		DQ1_0	DQ3_0	DQS_1_c	DQS_1	RE_1_c	CK_1 or WE_1_n	DQ4_0	DQ6_0	
R										
T	R								R	
U	R	R							R	R

Figure 5.2-1 — Ball Assignments for Dual 8-Bit Data Access, Toggle DDR or Synchronous DDR Data interface

5.3 BGA-152/132/136 (Quad x8 BGA)

Figure 5.3-1 to **Figure 5.3-3** define the ball assignments for devices using NAND Dual x8 BGA Evolutionary packaging with dual 8-bit data access for the Toggle DDR or Synchronous DDR data interface. 152 BGA is a standard package and 132/136 BGA are the subset packages of 152 BGA for the small size package. NC balls indicate mechanical support balls with no internal connection. NU balls at four corner areas indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore, it is recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application. PI-LTT with VccQL is not supported for 152/132/136BGA.

5.3 BGA-152/132/136 (Dual x8 BGA) (cont'd)

The BGA package uses MO-304.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NU	NU	NU	NU						NU	NU	NU	NU
D	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
E	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
F			DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_1	DQ6_1	DQ7_1		
G			VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ		
H			ENo or NU or CE2_0_n	ENi or NU or CE3_0_n	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	SCA_0 or NU		
J			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
K			SCA_1 or NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU or CE3_1_n	VDDi or NU or CE2_1_n		
L			VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ		
M			DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
N	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 or (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU	NU
P	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
R	NU	NU	NU	NU						NU	NU	NU	NU
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

**Figure 5.3-1 — NAND Dual x8 BGA-152 Package Ball Assignments for Dual 8-Bit Data Access,
Toggle DDR or Synchronous DDR Data Interface**

5.3 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NU	NU	NU						NU	NU	NU
D	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU
E	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R 1_n	VSSQ	DQ5_1	VSSQ	NU
F		DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_1	DQ6_1	DQ7_1	
G		VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ	
H		ENo or NU or CE2_0_n	ENi or NU or CE3_0_n	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	SCA_0 or NU	
J		VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS	
K		SCA_1 or NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU or CE3_1_n	VDDi or NU or CE2_1_n	
L		VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ	
M		DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0	
N	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R 0_n		DQS_0 or (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU
P	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU
R	NU	NU	NU						NU	NU	NU
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

Figure 5.3-2 — NAND Dual x8 BGA-132 Package Ball Assignments for Dual 8-Bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.3 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
--	---	---	---	---	---	---	---	---	---	----	----	----	----

A	NC	NC	NC	NC						NC	NC	NC	NC
B	NU	NU	NU	NU						NU	NU	NU	NU
C	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
D	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
E		DQ0_1	DQ1_1	DQS_1_c	RE_1_c			WE_1_n or CK_1	VREFQ_1	DQ6_1	DQ7_1		
F		VSSQ	VCCQ	ALE_1	CLE_1			CE3_1_n	CE2_1_n	VCCQ	VSSQ		
G		ENo or NU	ENi or NU	WP_1_n or ODT_1_n	NU			CE1_1_n	CE0_1_n	RZQ_1	SCA_0 or NU		
H		VSS	VCC	R/B0_0_n	R/B1_0_n			R/B1_1_n	R/ B0_1_n	VCC	VSS		
J		SCA_1 or NU	RZQ_0	CE0_0_n	CE1_0_n			NU or Vpp	WP_0_n or ODT_0_n	NU	VDDi or NU		
K		VSSQ	VCCQ	CE2_0_n	CE3_0_n			CLE_0	ALE_0	VCCQ	VSSQ		
L		DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0			RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
M	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU	NU
N	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
P	NU	NU	NU	NU						NU	NU	NU	NU
R	NC	NC	NC	NC						NC	NC	NC	NC

Figure 5.3-3 — NAND Dual x8 BGA-136 Package Ball Assignments for Dual 8-Bit Data Access,
Toggle DDR or Synchronous DDR Data Interface

5.4 BGA-316 (Quad x8 BGA)

Figure 5.4-1 to **Figure 5.4-2** define ball assignments for devices using NAND Quad x8 BGA for the Toggle DDR or Synchronous DDR data interface. For devices supporting PI-LTT, some VccQ balls are replaced with VccQL. BGA-316 supports up to 32 CEs for future extendibility regarding the number of die stacks, thus **Figure 5.4-1** illustrates the standard package with 16 CEs and **Figure 5.4-2** shows the extended type of the package with 32 CEs. NC balls indicate mechanical support balls with no internal connection. NU balls at the corner areas indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any support ball locations may or may not be populated with a ball depending on the NAND Flash Vendor's actual package size. Therefore, it is recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQL	VSS	VREFQ	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQL	VSS	ENi or NU	ENO or NU	VPP	NC	NC
D	NC	VCC	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VSS	VCC	NC
E	NC	VCCQL	VSS	VSP	VSP	DQ5_2	DQ5_0			DBI_2 or NU	R/B2_n	RZQ_2	VSS	VSS	RFU	NC
F	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_0 or NU	R/B0_n	RZQ_0	VSS	VSS	VSS	NC
G	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			WP_0_n or ODT_0_n	WP_2_nor ODT_2_n	CE1_2_n	CE3_2_n or VccQL	VSS	VCC	NC
H	NC	VCC	VSS	VCCQL	VSS	DQS_2_c	DQS_0_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n or VccQ	VSS	SCA_0 or NU	NC
J	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	VSS	VSS	NC
K	NC	VCCQL	VSS	VSS	DQ2_2	DQ2_0	RE_2_n (RE_2_t) or W/R_2_n			RE_0_n (RE_0_t) or W/R_0_n	ALE_0	CE0_0_n	CE2_0_n	VSS	VCC	NC
L	NC	VDDi	VREFQ	VSP	DQ1_2	DQ1_0	WE_2_n or CK_2			WE_0_n or CK_0	DQ0_1	DQ0_3	VSP	VSS	VCCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_n or CK_1			WE_3_n or CK_3	DQ1_1	DQ1_3	VSP	VREFQ	VDDi	NC
N	NC	VCC	VSS	CE2_1_n	CE0_1_n	ALE_1	RE_1_n (RE_1_t) or W/R_1_n			RE_3_n (RE_3_t) or W/R_3_n	DQ2_1	DQ2_3	VSS	VSS	VCCQL	NC
P	NC	VSS	VSS	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	SCA_1 or NU	VSS	CE3_1_n or VccQ	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQL	VSS	VCC	NC
T	NC	VCC	VSS	CE3_3_n or VccQL	CE1_3_n	WP_3_n or ODT_3_n	WP_1_n or ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	VSS	VSS	RZQ_1	R/B1_n	DBI_1 or NU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	VSS	VSS	RZQ_3	R/B3_n	DBI_3 or NU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQL	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQL			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREFQ	VSS	VCCQL	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 5.4-1 — NAND Quad x8 BGA-316 Package Ball Assignments for Quad 8-Bit Data Access with Up to 16 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.4 BGA-316 (Quad x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQL	VSS	VREFQ	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQL	VSS	ENor NU	ENor NU	VPP	NC	NC
D	NC	VCCQ	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VCC	VCC	NC
E	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_2orNU	R/B0_2_n	RZQ_2	CE6_2_n	CE7_2_n	RFU	NC
F	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DBI_0orNU	R/B0_0_n	RZQ_0	CE6_0_n	CE7_0_n	VSS	NC
G	NC	VCC	VSS	VCCQL	VSS	DQS_2_c	DQS_0_c			WP_0_n or ODT_0_n	WP_2_nor ODT_2_n	CE1_2_n	CE3_2_n or VccQL	CE5_2_n	VCC	NC
H	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n or VccQ	CE5_0_n	SCA_0 or NU	NC
J	NC	VCCQ	VSS	VSS	DQ2_2	DQ2_0	RE_2_n (RE_2_t) or WR_2_n			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	CE4_2_n	VSS	NC
K	NC	VDDI	VREFQ	VSP	DQ1_2	DQ1_0	WE_2_nor CK_2			RE_0_n (RE_0_t) or WR_0_n	ALE_0	CE0_0_n	CE2_0_n	CE4_0_n	VCC	NC
L	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_nor CK_1			WE_0_nor CK_0	DQ0_1	DQ0_3	VSP	VSS	VOCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_nor CK_1			WE_3_nor CK_3	DQ1_1	DQ1_3	VSP	VREFQ	VDDI	NC
N	NC	VCC	CE4_1_n	CE2_1_n	CE0_1_n	ALE_1	RE_1_n (RE_1_t) or WR_1_n			RE_3_n (RE_3_t) or WR_3_n	DQ2_1	DQ2_3	VSS	VSS	VCCQL	NC
P	NC	VSS	CE4_3_n	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	SCA_1 or NU	CE5_1_n	CE3_1_n or VccQ	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQL	VSS	VCC	NC
T	NC	VCC	CE5_3_n	CE3_3_n or VccQL	CE1_3_n	WP_3_nor ODT_3_n	WP_1_nor ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	CE7_1_n	CE6_1_n	RZQ_1	R/B0_1_n	DBI_1orNU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	CE7_3_n	CE6_3_n	RZQ_3	R/B0_3_n	DBI_3orNU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQL	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQL			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	NC	NC	NC	NC	VCC	REFQ	VSS	VCCQL	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 5.4-2—NAND Quad x8 BGA-316 Package Ball Assignments for Quad 8-Bit Data Access with Up to 32 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.5 BGA-272/252 (Quad x8 BGA)

Figure 5.5-1 and **Figure 5.5-2** define the ball assignments for devices using NAND Quad x8 BGA for the Toggle DDR or Synchronous DDR data interface. For devices supporting PI-LTT, some VccQ balls are replaced with VccQL and CE3_x_n balls are replaced with VccQ (optional). NC balls indicate mechanical support balls with no internal connection. NU balls at four corner areas indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore, it is recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application. These BGA packages use MO-210.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NU									NU	NC	NC	NC
B	NC	NC	NU	VccQ or VccQL	VSS	VSS	VSS			VCC	VccQ or VccQL	VSS	VCCQ	NU	NC	NC
C	NC	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU	NC
D	NU	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC	NU
E		VSS	VSS	VSS	DQ3_0	DQS_2_(DQS_2_t)	DQS_0_(DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VccQ or VccQL	
F		VccQ or VccQL	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ (TBD)	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ	
G		VCCQ	VSS	VSS	VSP0_R	VSP2_R or VccQL	VSS			WE_0_n or CK_0	CE1_0_n	CE3_0_n (TBD)	R/B0_0_n	R/B1_0_n	VSS	
H		ENi or NU	ENo or NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n or CK_2	CE1_2_n	CE3_2_n (TBD)	R/B0_2_n	R/B1_2_n	VSP6_R	
J																
K		VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_n (RE_0_t) or W/R_0_n	RE_0_c			OE0_2_n	OE0_0_n	OE2_2_n	OE2_0_n	VSP4 or VDDI	VPP	
L		SCA_0 or NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_n (RE_2_t) or W/R_2_n	RE_2_c			VREFQ	VREFQ	VSS	VSS	VSS	VSS	
M		VSS	VSS	VSS	VSS	VREFQ	VREFQ			RE_3_c	RE_3_n (RE_3_t) or W/R_3_n	CLE_3	ALE_3	WP_3_n or ODT_3_n	SCA_1 or NU	
N		VPP	VSP5 or VDDI	OE2_1_n	OE2_3_n	OE0_1_n	OE0_3_n			RE_1_c	RE_1_n (RE_1_t) or W/R_1_n	CLE_1	ALE_1	WP_1_n or ODT_1_n	VCC	
P		VSP7_R	R/B1_3_n	R/B0_3_n	OE3_3_n (TBD)	CE1_3_n	WE_3_n or CK_3			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU	
R		VSS	R/B1_1_n	R/B0_1_n	OE3_1_n (TBD)	CE1_1_n	WE_1_n or CK_1			VSS	VSP3_R or VccQL	VSP1_R	VSS	VSS	VCCQ	
T		VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ (TBD)			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VccQ or VccQL	
U		VccQ or VccQL	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1_(DQS_1_t)	DQS_3_(DQS_3_t)	DQ3_1	VSS	VSS	VSS	
V		NU	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC	NU
W		NU	VCC	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC	NU
Y		NC	NU	VCC	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU	NC
AA		NC	NC	NU	VCCQ	VSS	VccQ or VccQL	VCC		VSS	VSS	VccQ or VccQL	NU	NC	NC	NC
AB		NC	NC	NC	NU							NU	NC	NC	NC	NC

Figure 5.5-1 — NAND Quad x8 BGA-272 Package Ball Assignments for Quad 8-Bit Data Access with Up to 16 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.5 BGA-272/252 (Quad x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	NU									NU	NC	NC
B	NC	NU	VccQ or VccQL	VSS	VSS	VSS			VCC	VccQ or VccQL	VSS	VCCQ	NU	NC
C	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU
D	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC
E	VCC	VSS	VSS	VSS	DQ2_2	DQ2_0			DQ5_2	DQ5_0	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	DQ3_0	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VccQ or VccQL
G	VccQ or VccQL	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ (TBD)	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ
H	VCCQ	VSS	VSS	VSP0 R	VSP2 R or VccQL	VSS			WE_0_n or CK_0	CE1_0_n	CE3_0_n (TBD)	R/B0_0_n	R/B1_0_n	VSS
J	ENi or NU	ENO or NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n or CK_2	CE1_2_n	CE3_2_n (TBD)	R/B0_2_n	R/B1_2_n	VSP6 R
K	VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_n (RE_0_t) or W/R_0_n	RE_0_c			CE0_2_n	CE0_0_n	CE2_2_n	CE2_0_n	VSP4 or VDDi	VPP
L	SCA_0 or NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_n (RE_2_t) or W/R_2_n	RE_2_c			VREFQ	VREFQ	VSS	VSS	VSS	VSS
M	VSS	VSS	VSS	VSS	VREFQ	VREFQ			RE_3_c	RE_3_n (RE_3_t) or W/R_3_n	CLE_3	ALE_3	WP_3_n or ODT_3_n	SCA_1 or NU
N	VPP	VSP5 or VDDi	CE2_1_n	CE2_3_n	CE0_1_n	CE0_3_n			RE_1_c	RE_1_n (RE_1_t) or W/R_1_n	CLE_1	ALE_1	WP_1_n ODT_1_n	VCC
P	VSP7 R	R/B1_3_n	R/B0_3_n	CE3_3_n (TBD)	CE1_3_n	WE_3_n or CK_3			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU
R	VSS	R/B1_1_n	R/B0_1_n	CE3_1_n (TBD)	CE1_1_n	WE_1_n or CK_1			VSS	VSP3 R or VccQL	VSP1 R	VSS	VSS	VCCQ
T	VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ (TBD)			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VccQ or VccQL
U	VccQ or VccQL	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	DQ3_1	VSS	VSS	VSS
V	VSS	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC
W	VCC	VSS	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC
Y	NU	VCC	VSS	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU
AA	NC	NU	VCCQ	VSS	VccQ or VccQL	VCC			VSS	VSS	VSS	VccQ or VccQL	NU	NC
AB	NC	NC	NU								NU	NC	NC	

Figure 5.5-2 — NAND Quad x8 BGA-252 Package Ball Assignments for Quad 8-bit Data Access with Up to 16 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.6 BGA-178/154/146 (Dual x8 BGA)

Figure 5.6-1, Figure 5.6-2, and Figure 5.6-3 define the ball assignments for devices using NAND Dual x8 BGA for the Toggle DDR or Synchronous DDR data interface. For devices supporting PI-LTT, some VccQ balls are replaced with VccQL and CE3_x_n balls are replaced with VccQ (optional). NC balls indicate mechanical support balls with no internal connection. NU balls indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore, it is recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application.

The package size of BGA-178 is 13.5x13.5 mm with 0.8 mm ball pitch and uses MO-216. The package size of BGA-154 is either 11.5x13.5 mm or 12.8x13.5 mm with 0.8 mm ball pitch and uses MO-210. The package size of BGA-146 is either 10x18 mm or 10x14 mm with 0.8 mm ball pitch and uses MO-210.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	NC	NC								NC	NC	NC	NC
B	NC	NU	NU	NU								NU	NU	NU	NC
C	NC	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU	NC
D	NC	NU	VCCQ	VCC	RFU	VPP	PSL_0_ZQ_0	VREF_0	SCA_1 or NU	VSP	VSP	VCC	VCCQ	NU	NC
E	NC	NU	VSS	DQ5_0	VccQ or VccQL	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VccQ or VccQL	DQ2_1	VSS	NU	NC
F	NC	NU	VccQ or VccQL	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VccQ or VccQL	NU	NC
G		NU	VCC	RE_0_n W/R_0_n	RE_0_c	WE_0_n CLK_0	CE3_0_n or VccQ	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU	
H															
J		NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n or VccQ	WE_1_n CLK_1	RE_1_c	RE_1_n W/R_1_n	VCC	NU	
K	NC	NU	VccQ or VccQL	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VccQ or VccQL	NU	NC
L	NC	NU	VSS	DQ2_0	VccQ or VccQL	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VccQ or VccQL	DQ5_1	VSS	NU	NC
M	NC	NU	VCCQ	VCC	VSP	VSP	SCA_0 or NU	VREF_1	PSL_1_ZQ_1	VPP	RFU	VCC	VCCQ	NU	NC
N	NC	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU	NC
P	NC	NU	NU	NU									NU	NU	NC
R	NC	NC	NC	NC									NC	NC	NC

Figure 5.6-1 — NAND Dual x8 BGA-178 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.6 BGA-178/154/146 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC								NC	NC	NC
B	NU	NU	NU								NU	NU	NU
C	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU
D	NU	VCCQ	VCC	RFU	VPP	PSL_0 ZQ_0	VREF_0	SCA_1 or NU	VSP	VSP	VCC	VCCQ	NU
E	NU	VSS	DQ5_0	VccQ or VccQL	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VccQ or VccQL	DQ2_1	VSS	NU
F	NU	VccQ or VccQL	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VccQ or VccQL	NU
G	NU	VCC	RE_0_n W/R_0_n	RE_0_c	WE_0_n CLK_0	CE3_0_n or VccQ	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU
H													
J	NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n or VccQ	WE_1_n CLK_1	RE_1_c	RE_1_n W/R_1_n	VCC	NU
K	NU	VccQ or VccQL	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VccQ or VccQL	NU
L	NU	VSS	DQ2_0	VccQ or VccQL	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VccQ or VccQL	DQ5_1	VSS	NU
M	NU	VCCQ	VCC	VSP	VSP	SCA_0 or NU	VREF_1	PSL_1 ZQ_1	VPP	RFU	VCC	VCCQ	NU
N	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU
P	NU	NU	NU								NU	NU	NU
R	NC	NC	NC								NC	NC	NC

**Figure 5.6-2 — NAND Dual x8 BGA-154 Package Ball Assignments for Dual 8-bit Data Access,
Toggle DDR or Synchronous DDR Data Interface**

5.6 BGA-178/154/146 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC	NC				NC	NC	NC	NC
B	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
C	NU	VCCQ	VSS	VCCQ or VccQL	VSS		VCC	VCCQ or VccQL	VSS	VCCQ	NU
D	VCCQ	VCC	DQ2_0	DQ3_0	DQS_0_t		RE_0_n W/R_0_n	DQ4_0	DQ5_0	VCC	VCCQ
E	VSS	VSP	VccQ or VccQL	VSS	DQS_0_c		RE_0_c	VSS	VccQ or VccQL	RFU	VSS
F	VCCQ or VccQL	VSP	DQ0_0	DQ1_0	DBI_0 or NU		WE_0_n CLK_0	DQ6_0	DQ7_0	VPP	VPP
G	VSS	SCA_0 or NU	WP_0_n ODT_0_n	ALE_0	CLE_0		CE3_0_n or VccQ	CE2_0_n	CE1_0_n	PSL_0 ZQ_0	VSS
H	VCC	VREF_1	CE0_1_n	R/B0_1_n	R/B1_1_n		R/B1_0_n	R/B0_0_n	CE0_0_n	VREF_0	VCC
J	VSS	PSL_1 ZQ_1	CE1_1_n	CE2_1_n	CE3_1_n or VccQ		CLE_1	ALE_1	WP_1_n ODT_1_n	SCA_1 or NU	VSS
K	VPP	VPP	DQ7_1	DQ6_1	WE_1_n CLK_1		DBI_1 or NU	DQ1_1	DQ0_1	VSP	VCCQ or VccQL
L	VSS	RFU	VccQ or VccQL	VSS	RE_1_c		DQS_1_c	VSS	VccQ or VccQL	VSP	VSS
M	VCCQ	VCC	DQ5_1	DQ4_1	RE_1_n W/R_1_n		DQS_1_t	DQ3_1	DQ2_1	VCC	VCCQ
N	NU	VCCQ	VSS	VCCQ or VccQL	VCC		VSS	VCCQ or VccQL	VSS	VCCQ	NU
P	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
R	NC	NC	NC	NC				NC	NC	NC	NC

Figure 5.6-3 — NAND Dual x8 BGA-146 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.7 CE_n to R/B_n Mapping

There may be two independent 8-bit data buses in some JEDEC packages (i.e., the BGA-152 package). There may be four independent 8-bit data buses in some JEDEC packages (i.e., the BGA-316 and BGA-272 packages).

Any signal with a channel (i.e., 8-bit data bus) designator (for example, "x" for CE0_x_n) could not be used by another channel. For example, CE0_0 cannot be used on any channel other than channel 0 or R/B0_1 cannot be used for any channel other than channel 1.

In some package configurations, there are multiple CE_n signals per R/B_n signal. **Table 5.7-1** describes the R/B_n signal that each CE_n uses in the case when there are two R/B_n signals and more than one CE_n per 8-bit data bus. **Table 5.7-2** describes the R/B_n signal that each CE_n uses in the case when there is a single R/B_n signal per 8-bit data bus. **Table 5.7-3** provides the case when there is a single CE_n and two R/B_n signals per 8-bit data bus. For packages that only support two 8-bit data buses, R/B0_2_n, R/B1_2_n, R/B0_3_n, and R/B1_3_n shall be ignored.

Table 5.7-1 — R/B_n Signal Use Per CE_n with Two R/B_n Signals Per Channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE2_0_n, CE4_0_n, CE6_0_n
R/B0_1_n	CE0_1_n, CE2_1_n, CE4_1_n, CE6_1_n
R/B0_2_n	CE0_2_n, CE2_2_n, CE4_2_n, CE6_2_n
R/B0_3_n	CE0_3_n, CE2_3_n, CE4_3_n, CE6_3_n
R/B1_0_n	CE1_0_n, CE3_0_n, CE5_0_n, CE7_0_n
R/B1_1_n	CE1_1_n, CE3_1_n, CE5_1_n, CE7_1_n
R/B1_2_n	CE1_2_n, CE3_2_n, CE5_2_n, CE7_2_n
R/B1_3_n	CE1_3_n, CE3_3_n, CE5_3_n, CE7_3_n

Table 5.7-2 — R/B_n Signal Use Per CE_n with a Single R/B_n Signal Per Channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE1_0_n, CE2_0_n, CE3_0_n, CE4_0_n, CE5_0_n, CE6_0_n, CE7_0_n
R/B0_1_n	CE0_1_n, CE1_1_n, CE2_1_n, CE3_1_n, CE4_1_n, CE5_1_n, CE6_1_n, CE7_1_n
R/B0_2_n	CE0_2_n, CE1_2_n, CE2_2_n, CE3_2_n, CE4_2_n, CE5_2_n, CE6_2_n, CE7_2_n
R/B0_3_n	CE0_3_n, CE1_3_n, CE2_3_n, CE3_3_n, CE4_3_n, CE5_3_n, CE6_3_n, CE7_3_n

5.7 CE_n to R/B_n Mapping (cont'd)

Table 5.7-3 — R/B_n Signal Use Per CE_n with a Two R/B_n Signals Per Channel and One CE_n Per Channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n
R/B0_1_n	CE0_1_n
R/B0_2_n	CE0_2_n
R/B0_3_n	CE0_3_n
R/B1_0_n	CE0_0_n
R/B1_1_n	CE0_1_n
R/B1_2_n	CE0_2_n
R/B1_3_n	CE0_3_n

R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs on the corresponding NAND Target or Volume. In the case that more than one NAND target or Volume share an R/B_n signal, R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs connected to the shared R/B_n signal. For example, R/B0_0 is logical AND of the SR[6] values for all LUNs that share R/B0_0. Thus, R/B_n reflects whether any LUN is busy on a particular NAND Target or if there are multiple NAND Targets that share R/B_n, R/B_n reflects whether any LUN is busy on any of the shared NAND Targets.

6 Command Sets for NAND Flash memory

6.1 Basic Command Definition

Table 6.1-1 outlines the commands defined for NAND Flash memory.

The value specified in the first command cycle identifies the command to be performed. Some commands have a second command cycle as specified in **Table 6.1-1**. Typically, commands that have a second command cycle include an address.

Table 6.1-1 — Command Set

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target Level Commands
Page Read	M	00h	30h		Y	
Copyback Read	O	00h	35h		Y	
Change Read Column	M	05h	E0h		Y	
Read Cache Random	O	00h	31h		Y	
Read Cache Sequential	O	31h	na		Y	
Read Cache End	O	3Fh	na		Y	
Block Erase	M	60h	D0h		Y	
Page Program	M	80h	10h		Y	
Copyback Program	O	85h	10h		Y	
Change Write Column	O	85h	na		Y	
Get Features	O	EEh	na			Y
Set Features	O	EFh	na			Y
Page Cache Program	O	80h	15h		Y	
Read Status	M	70h	na	Y		
Read Unique ID	O	EDh	na			Y
Reset	M	FFh	na	Y	Y	Y
Synchronous Reset	O	FCh	na	Y	Y	Y
Reset LUN	O	FAh		Y	Y	

NOTE 1 LUNSEL packet and SCE / SCP /SCT packets for Other LUN are not allowed during command sets sequence in **Table 6.1-1** and in **Table 6.2-1**.

NOTE 2 If 12h CMD is included in command set sequence, LUNSEL packet and SCE / SCP /SCT packets for Other LUN are allowed after 12h command is issued.

NOTE 3 For case without 2nd cycle among 2nd command set, LUNSEL packet and SCE / SCP /SCT packets for other LUN are not allowed during from 1st cycle to last address.

6.2 Primary and Secondary Command Definition for the Advanced Operation

Table 6.2-1 defines the Primary and Secondary Commands. Primary commands are the recommended implementation for a particular command. Secondary commands are an alternate implementation approach that is allowed for backwards compatibility. Commands may be used with any data interface (asynchronous SDR, Toggle DDR, or Synchronous DDR).

Table 6.2-1 — Primary and Secondary Commands

Command	O/M	1st Cycle	2nd Cycle
Multi-plane Read	M	00h	32h
	O	60h	30h
Multi-plane Read Cache Random	M	00h	31h
	O	60h	3Ch
Multi-plane Copyback Read	M	00h	35h
	O	60h	35h
Random Data Out	O	00h 05h	n/a E0h
	O	06h	E0h
Multi-plane Program	O	80h or 81h	11h
	O	80h	11h
Multi-plane Copyback Program	O	85h or 81h	11h
	O	85h	11h
Multi-plane Block Erase	M	60h	n/a or D1h
Read Status Enhanced	M	78h	n/a
	O	F1h/F2h	n/a

6.3 Get Feature for Each LUN

Figure 6.3-1 shows Get Feature for each LUN operation timing diagram. This operation requires two address cycles. The LUN address comes first followed by the Feature address. The two address cycles cannot be interchanged. Writing two addresses is what distinguishes this command from the standard Get Feature operation which requires a single Feature address.

When the LUN address is issued, 00h is used for LUN0 and 01h is for LUN1.

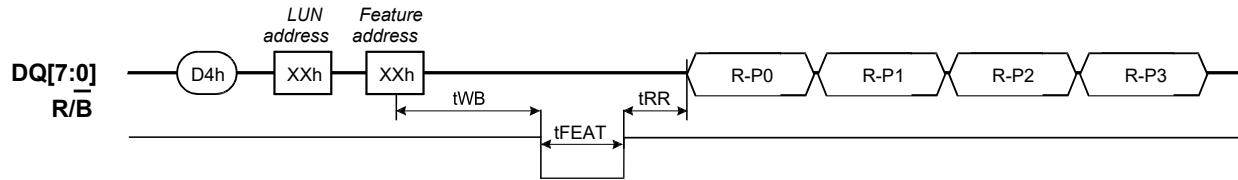


Figure 6.3-1 — Get Feature for Each LUN Sequence

6.4 Set Feature for Each LUN

Figure 6.4-1 depicts Set Feature for each LUN operation timing diagram. This operation requires two address cycles. The LUN address comes first followed by the Feature address. The two address cycles cannot be interchanged. Writing two addresses is what distinguishes this command from the standard Set Feature operation which requires a single Feature address.

When the LUN address is issued, 00h is used for LUN0 and 01h is for LUN1.

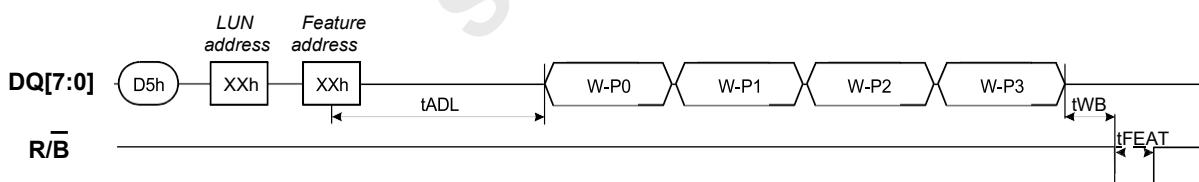


Figure 6.4-1 — Set Feature for Each LUN Sequence

7 Feature Address Registers

7.1 Feature Address 02h (Interface Configuration Register)

Table 7.1-1 — Feature Table for Interface Configuration Register [02h]

Sub Feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0		
B0	ODT Self-Termination (with Rtt Value)		Reserved		RE (CMPR)	DQS (CMRD)	Reserved			
B1	# of Latency DQS cycle for WRITE				# of Latency DQS cycle for READ					
B2	VSP	VOH for LTT/PI-LTT (optional)	DBI for WRITE	DBI for READ	Internal VrefQ Value Setting (Read Only)	Interface Type				
B3	Reserved					SCA_DQMIRR (optional)	SCA_OUT (optional)			

B0[1] for complementary/differential DQS

0 (default) = disable DQS_c
1 = enable DQS_c

B0[2] for complementary/differential RE

0 (default) = disable RE_c
1 = enable RE_c

B2[1:0] for Interface Type

00b = Reserved
01b (default) = LTT Interface
10b = PI-LTT Interface
11b = Reserved

B2[3:2] for Internal VrefQ Value Setting (Read Only)

00b = NAND Uses Value1 Range/Step Size
01b = NAND Uses Value2 Range/Step Size
10b = NAND Uses Value3 Range/Step Size
11b = Reserved

B2[4] for DBI for Read

0 (default) = DBI for Read is disabled
1 = DBI for Read is enabled

B2[5] for DBI for Write

0 (default) = DBI for Write is disabled
1 = DBI for Write is enabled

B2[6] for VOH for LTT/PI-LTT (Optional)

0 (default) = VccQ/3 for LTT, VccQL/2 for PI-LTT
1 = VccQ/2.5 for LTT (Optional)

B3[0] (SCA_OUT) optional bit for SCA protocol CA output packet format

0 (default) = single-byte CA output format
1 = multi-byte CA output format

7.1 Feature Address 02h (Interface Configuration Register) (cont'd)

B3[1] (SCA_DQMIRR) optional bit for SCA protocol DQ mirror function enable/disable
 0 (default) = DQ mirror function disabled
 1 = DQ mirror function enabled

7.2 Feature Address 05h

User can switch between WP and ODT functions via set-feature.

Table 7.2-1 — Feature Table for WP/ODT Mode Selection [05h]

Sub Feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0-2	Reserved (0)							
B3	Reserved (0)	WP/ODT Mode Selection	Reserved (0)					

B3[6] for WP and ODT selection mode
 0 (default) = WP Operation
 1 = ODT Operation
 B3[6] for WP and ODT selection mode: Reserved (0) in the SCA protocol

7.3 Feature Address 10h

Table 7.3-1 — Feature Table for LTT Pull-down Drive Strength (Optional Location2) [10h]

Sub Feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Reserved				LTT ¹⁾ Pull-Down Driver Strength Settings (Optional Location2 for LTT PDSS: See Vendor Datasheet)			
B1 – B3	Reserved							

NOTE 1 CTT and LTT Pull-Down Driver Strength Setting are configured via FA 10h on JESD230F devices

7.4 Feature Address 20h

To be used for DCC training, Read Training, and Write training (Tx side).

Table 7.4-1 — Feature Table for DCC, Read Training, Write Training (Tx side) [20h]

Sub Feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Reserved (0)				DCC Factory Setting	DCCI_EN	DCCE_EN	
B1	Reserved (0)							
B2	Reserved (0)		Read Training Defined Pattern Length	Write Training Data Size [3:0] 0000 : 08 Bytes 0001 : 16 Bytes 0010 : 24 Bytes 0011 : 32 Bytes 0100 : 40 Bytes 0101 : 48 Bytes 0110 : 56 Bytes				

Table 7.4-1 – Feature Table for DCC, Read Training, Write Training (Tx side) [20h] (cont'd)

Sub Feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B2			Reserved (0)	Read Training Defined Pattern Length	Write Training Data Size [3:0] (Cont'd) 0111 : 64 Bytes 1000 : 72 Bytes 1001 : 80 Bytes 1010 : 88 Bytes 1011 : 96 Bytes 1100 : 104 Bytes 1101 : 112 Bytes 1110 : 120 Bytes 1111 : 128 Bytes			
B3					Reserved (0)			

B0[0] for the enabler of explicit DCC Training using Set Feature [1: Turn on training, 0: turn off training]
default=0.

B0[1] for the enabler of implicit DCC Training during warm up cycles [1: Enable, 0: Disable] default=0. Host can set DCC En/Disable=Disable if host doesn't need DCC with low frequency operation.

B0[2] is for DCC factory setting. This is an optional function for the NAND device, please refer to the vendor datasheet to see if DCC factory setting is supported or not. If set to a 1, then the factory DCC settings would be used by the LUN. If cleared to 0, then the DCC calibrated settings would be used by the LUN.

B2[3:0] are read only bits for data size for write training (up to 128 bytes)

B2[4] read only bit for data pattern length for read training [1: 32 Bytes, 0: 16 Bytes]

7.5 Feature Address 21h

To be used for Write Training (Rx side)

Table 7.5-1 — Feature Table for Write Training (Rx side) [21h]

Sub Feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0				Reserved (0)		Write Training Rx with Internal VrefQ Training (Optional)	All LUN	Factory setting
B1	St_dq3[1]	St_dq3[0]	St_dq2[1]	St_dq2[0]	St_dq1[1]	St_dq1[0]	St_dq0[1]	St_dq0[0]
B2	St_dq7[1]	St_dq7[0]	St_dq6[1]	St_dq6[0]	St_dq5[1]	St_dq5[0]	St_dq4[1]	St_dq4[0]
B3					Reserved (0)			

B0[0] keep input path settings as determined by training/reset to factory settings [1 = factory setting; 0 = trained value]

B0[1] Enables All LUN option. This is an optional function for the NAND device, please refer to the vendor datasheet if All LUN Write Training (Rx side) is supported or not. If this bit is set to a 1 prior to Write Training (Rx side) then the LUN address cycle is ignored and the write training is performed by all enabled LUNs which have this bit set.

B0[2] for Write Training (Rx side) With Internal VrefQ Training (Optional)

0 (default) = Disabled

1 = Write Training (Rx side) with Internal VrefQ Training for LTT and PI-LTT

7.5 Feature Address 21h (cont'd)

B1[7:0] Status bits for dq[3:0]

B2[7:0] Status bits for dq[7:4]

B1[1:0]:

00: Centering of dqs to dq0 data eye is successful.

01: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too slow with respect to dqs/dqsn

10: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too fast with respect to dqs/dqsn

11: Centering of dqs/dqsn to dq0 data eye failed for unknown reasons

B1[3:2], B1[5:4], B1[7:6], B2[1:0], B2[3:2], B2[5:4], B2[7:6] represent the status of dq[7:1] similar to B1[1:0] for dq0.

7.6 Feature Address 22h

Table 7.6-1 — Feature Table for LTT/PI-LTT CH_ODT, Pull-down Drive Strength (Optional Location1), and ODT Control Configuration [22h]

Sub Feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0			
B0	LTT/PI-LTT Pull-Down Driver Strength (PDDS) (Optional Location1 for LTT PDDS: See Vendor Datasheet)					Channel ODT (CH_ODT) Value for VOH Calibration (For LTT/PI-LTT Pull-up Driver Strength)					
B1	LTT/PI-LTT Target ODT Value for DQ/DQS Input ¹					LTT/PI-LTT Non-Target ODT Value for DQ/DQS Input ^{1, 2}					
B2	LTT/PI-LTT Target ODT Value for RE Input ¹					LTT/PI-LTT Non-Target ODT Value for RE Input ^{1, 2}					
B3	Reserved					LTT/PI-LTT Non-Target ODT Value for DQ/DQS Output ^{1, 2}					
NOTE 1	These fields are applicable to ODT Control Type1 NAND Devices (i.e., ODT control is done via ODT_n pin) with the conventional protocol enabled										
NOTE 2	These fields may also be used for Non-Target ODT value configurations when the SCA protocol is enabled.										

7.7 Feature Address 23h

Table 7.7-1 — Feature Table for Internal VrefQ for NAND Devices that Support Value1 or Value2 or Value3 Settings [23h]

Sub-feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Internal VrefQ Value1/Value2/Value3 Settings (LTT/PI-LTT)							Reserved
B1	Reserved							
B2	Reserved							
B3	Reserved							
NOTE 1	The NAND internal VrefQ shall not be set to a setting beyond the allowable range even during Write Training.							
NOTE 2	NAND is not required to implement VrefQ beyond the NAND Minimum Internal VrefQ Allowable Range							

7.7 Feature Address 23h (cont'd)

Table 7.7-2 — Internal VrefQ Value1 Range, Step Size, and Tolerance (LTT: VccQL=1.2V)

Internal VrefQ Value1 Range/Step Size				
Parameter	Min	Typ	Max	Unit
Default	TBD			VccQL
Vref_min	0%	-	-	VccQL
Vref_max	-	-	63.50%	VccQL
Vref_step	0.35%	0.50%	0.65%	VccQL
Vref_Set_Tol	-1.75%	0%	1.75%	VccQL

Table 7.7-3 — Internal VrefQ Value1 Range, Step Size, and Tolerance (PI-LTT: VccQL=0.6V)

Internal VrefQ Value1 Range/Step Size				
Parameter	Min	Typ	Max	Unit
Default	TBD			VccQL
Vref_min	0%	-	-	VccQL
Vref_max	-	-	63.50%	VccQL
Vref_step	0.35%	0.50%	0.65%	VccQL
Vref_Set_Tol	-2.63%	0%	2.63%	VccQL

Table 7.7-4 — Internal VrefQ Value2 Range, Step Size, and Tolerance (LTT: VccQL=1.2V)

Internal VrefQ Value2 Range/Step Size				
Parameter	Min	Typ	Max	Unit
Default	TBD			VccQL
Vref_min	0%	-	-	VccQL
Vref_max	-	-	99.22%	VccQL
Vref_step	0.58%	0.78%	0.98%	VccQL
Vref_Set_Tol	-1.95%	0%	1.95%	VccQL

Table 7.7-5 — Internal VrefQ Value2 Range, Step Size, and Tolerance (PI-LTT: VccQL=0.6V)

Internal VrefQ Value2 Range/Step Size				
Parameter	Min	Typ	Max	Unit
Default	TBD			VccQL
Vref_min	0%	-	-	VccQL
Vref_max	-	-	99.22%	VccQL
Vref_step	0.58%	0.78%	0.98%	VccQL
Vref_Set_Tol	-2.93%	0%	2.93%	VccQL

7.7 Feature Address 23h (cont'd)

Table 7.7-6 — Internal VrefQ Value1 Setting Versus Value as % of VccQL (LTT: 1.2V/PI-LTT: 0.6V)

Code	VrefQ (% of VccQL)						
0000000b	0.00	0100000b	16.00	1000000b	32.00	1100000b	48.00
0000001b	0.50	0100001b	16.50	1000001b	32.50	1100001b	48.50
0000010b	1.00	0100010b	17.00	1000010b	33.00	1100010b	49.00
0000011b	1.50	0100011b	17.50	1000011b	33.50	1100011b	49.50
0000100b	2.00	0100100b	18.00	1000100b	34.00	1100100b	50.00
0000101b	2.50	0100101b	18.50	1000101b	34.50	1100101b	50.50
0000110b	3.00	0100110b	19.00	1000110b	35.00	1100110b	51.00
0000111b	3.50	0100111b	19.50	1000111b	35.50	1100111b	51.50
0001000b	4.00	0101000b	20.00	1001000b	36.00	1101000b	52.00
0001001b	4.50	0101001b	20.50	1001001b	36.50	1101001b	52.50
0001010b	5.00	0101010b	21.00	1001010b	37.00	1101010b	53.00
0001011b	5.50	0101011b	21.50	1001011b	37.50	1101011b	53.50
0001100b	6.00	0101100b	22.00	1001100b	38.00	1101100b	54.00
0001101b	6.50	0101101b	22.50	1001101b	38.50	1101101b	54.50
0001110b	7.00	0101110b	23.00	1001110b	39.00	1101110b	55.00
0001111b	7.50	0101111b	23.50	1001111b	39.50	1101111b	55.50
0010000b	8.00	0110000b	24.00	1010000b	40.00	1110000b	56.00
0010001b	8.50	0110001b	24.50	1010001b	40.50	1110001b	56.50
0010010b	9.00	0110010b	25.00	1010010b	41.00	1110010b	57.00
0010011b	9.50	0110011b	25.50	1010011b	41.50	1110011b	57.50
0010100b	10.00	0110100b	26.00	1010100b	42.00	1110100b	58.00
0010101b	10.50	0110101b	26.50	1010101b	42.50	1110101b	58.50
0010110b	11.00	0110110b	27.00	1010110b	43.00	1110110b	59.00
0010111b	11.50	0110111b	27.50	1010111b	43.50	1110111b	59.50
0011000b	12.00	0111000b	28.00	1011000b	44.00	1111000b	60.00
0011001b	12.50	0111001b	28.50	1011001b	44.50	1111001b	60.50
0011010b	13.00	0111010b	29.00	1011010b	45.00	1111010b	61.00
0011011b	13.50	0111011b	29.50	1011011b	45.50	1111011b	61.50
0011100b	14.00	0111100b	30.00	1011100b	46.00	1111100b	62.00
0011101b	14.50	0111101b	30.50	1011101b	46.50	1111101b	62.50
0011110b	15.00	0111110b	31.00	1011110b	47.00	1111110b	63.00
0011111b	15.50	0111111b	31.50	1011111b	47.50	1111111b	63.50

7.7 Feature Address 23h (cont'd)

Table 7.7-7 — Internal VrefQ Value1 Setting Versus Value as % of VccQL (LTT: 1.2V/PI-LTT: 0.6V)

Code	VrefQ (% of VccQL)						
0000000b	0.00	0100000b	25.00	1000000b	50.00	1100000b	75.00
0000001b	0.78	0100001b	25.78	1000001b	50.78	1100001b	75.78
0000010b	1.56	0100010b	26.56	1000010b	51.56	1100010b	76.56
0000011b	2.34	0100011b	27.34	1000011b	52.34	1100011b	77.34
0000100b	3.13	0100100b	28.13	1000100b	53.13	1100100b	78.13
0000101b	3.91	0100101b	28.91	1000101b	53.91	1100101b	78.91
0000110b	4.69	0100110b	29.69	1000110b	54.69	1100110b	79.69
0000111b	5.47	0100111b	30.47	1000111b	55.47	1100111b	80.47
0001000b	6.25	0101000b	31.25	1001000b	56.25	1101000b	81.25
0001001b	7.03	0101001b	32.03	1001001b	57.03	1101001b	82.03
0001010b	7.81	0101010b	32.81	1001010b	57.81	1101010b	82.81
0001011b	8.59	0101011b	33.59	1001011b	58.59	1101011b	83.59
0001100b	9.38	0101100b	34.38	1001100b	59.38	1101100b	84.38
0001101b	10.16	0101101b	35.16	1001101b	60.16	1101101b	85.16
0001110b	10.94	0101110b	35.94	1001110b	60.94	1101110b	85.94
0001111b	11.72	0101111b	36.72	1001111b	61.72	1101111b	86.72
0010000b	12.50	0110000b	37.50	1010000b	62.50	1110000b	87.50
0010001b	13.28	0110001b	38.28	1010001b	63.28	1110001b	88.28
0010010b	14.06	0110010b	39.06	1010010b	64.06	1110010b	89.06
0010011b	14.84	0110011b	39.84	1010011b	64.84	1110011b	89.84
0010100b	15.63	0110100b	40.63	1010100b	65.63	1110100b	90.63
0010101b	16.41	0110101b	41.41	1010101b	66.41	1110101b	91.41
0010110b	17.19	0110110b	42.19	1010110b	67.19	1110110b	92.19
0010111b	17.97	0110111b	42.97	1010111b	67.97	1110111b	92.97
0011000b	18.75	0111000b	43.75	1011000b	68.75	1111000b	93.75
0011001b	19.53	0111001b	44.53	1011001b	69.53	1111001b	94.53
0011010b	20.31	0111010b	45.31	1011010b	70.31	1111010b	95.31
0011011b	21.09	0111011b	46.09	1011011b	71.09	1111011b	96.09
0011100b	21.88	0111100b	46.88	1011100b	71.88	1111100b	96.88
0011101b	22.66	0111101b	47.66	1011101b	72.66	1111101b	97.66
0011110b	23.44	0111110b	48.44	1011110b	73.44	1111110b	98.44
0011111b	24.22	0111111b	49.22	1011111b	74.22	1111111b	99.22

7.7 Feature Address 23h (cont'd)

Table 7.7-8 — Internal VrefQ Value3 Range, Step Size, and Tolerance (LTT: VccQL=1.2V)

Internal VrefQ Value3 Range/Step Size				
Parameter	Min	Typ	Max	Unit
Default	Vendor Specific			VccQL
Vref_min	Vendor Specific			VccQL
Vref_max	Vendor Specific but has to be greater than NAND Minimum Internal VrefQ Allowable max values			VccQL
Vref_step	Vendor specific. Vendor can specify Vref_step Typ to be within 0.25% - 0.75% of VccQ			VccQL
Vref_Set_Tol	-1.75%	0%	1.75%	VccQL

Table 7.7-9 — Internal VrefQ Value3 Range, Step Size, and Tolerance (PI-LTT: VccQL=0.6V)

Internal VrefQ Value3 Range/Step Size				
Parameter	Min	Typ	Max	Unit
Default	Vendor Specific			VccQL
Vref_min	Vendor Specific			VccQL
Vref_max	Vendor Specific but has to be greater than NAND Minimum Internal VrefQ Allowable max values			VccQL
Vref_step	Vendor specific. Vendor can specify Vref_step Typ to be within 0.25% - 0.75% of VccQL			VccQL
Vref_Set_Tol	-2.63%	0%	2.63%	VccQL

For NAND devices that support Value3 Settings:

- VREFI is the VrefQ voltage inside the NAND. VREFI is calculated in the following manner:
$$\text{VREFI} = (\text{VrefQ Setting}) * \text{Vref_step} + \text{Vref_min}$$
.
- VrefQ Setting can range from 0 ~ 255 (8b)
- If the calculated VREFI \geq Vref_max, then actual VREFI = Vref_max
- A table showing feature address register setting versus the expected actual VREFI value can be derived using the formula above and represented in the vendor datasheet

7.8 Feature Address 24h (WDCA)

Table 7.8-1 — Feature Table for Write Duty Cycle Adjustment [24h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Reserved			WDCA Step Control				
B1	Reserved							
B2	Reserved							
B3	Reserved							

B0[4:0] for WDCA Step Control

00000b: 0step (default)

00001b: +1step

00010b: +2steps

00011b: +3steps

00100b ~ 01111b: +4steps ~ +15steps (Optional)

10000b: 0step

10001b: -1step

10001b: -2steps

10011b: -3steps

10100b ~ 11111b: -4steps ~ -15steps (Optional)

7.9 Feature Address 26h (DQS Oscillator)

Table 7.9-1 — Feature Table for DQS Oscillator [26h]

Subfeature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	DQS Oscillator Count – LSB (Read Only)							
B1	DQS Oscillator Count – MSB (Read Only)							
B2	Reserved							
B3	Reserved							

7.10 Feature Address 27h (DFE)

Table 7.10-1 — Feature Table for DFE [27h]

Subfeature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Pre-drive for read		Pre-drive for write	Reserved		DFE coefficient control		
B1				Reserved				
B2				Reserved				
B3				Reserved				

B0[2:0] for DFE coefficient control

- 000b (default) = disabled
- 001b = +1 step
- 010b = +2 steps
- 011b = +3 steps
- 100b = +4 steps (optional)
- 101b = +5 steps (optional)
- 110b = +6 steps (optional)
- 111b = +7 steps (optional)

B0[5:4] for Pre-drive enable for write (NAND DFE)

- 00b (default) = disabled
- 01b = Pre-drive 2UI
- 10b = Pre-drive 4UI (optional)
- 11b = Pre-drive 8UI (optional)

B0[7:6] for Pre-drive enable for read (Controller DFE)

- 00b (default) = disabled
- 01b = Pre-drive 2UI
- 10b = Pre-drive 4UI (optional)
- 11b = Pre-drive 8UI (optional)

7.11 Feature Address 28h (RDCA)

Table 7.11-1 — Feature Table for RDCA [28h]

Subfeature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0		Reserved			RDCA Step Control			
B1				Reserved				
B2				Reserved				
B3				Reserved				

B0[4:0] for RDCA Step Control

- 00000b: 0step (default)
- 00001b: +1step
- 00010b: +2steps
- 00011b: +3steps
- 00100b ~ 01111b: +4steps ~ +15steps (Optional)
- 10000b: 0step
- 10001b: -1step
- 10001b: -2steps
- 10011b: -3steps
- 10100b ~ 11111b: -4steps ~ -15steps (Optional)

7.12 Feature Address 40h and 41h (Per-Pin VrefQ Adjustment via Offset)

NAND device supports per-pin VrefQ adjustment via the offset. The base NAND VrefQ setting is provided by FA23h while FA40h and FA41h provide the pin specific offset information.

Table 7.12-1 — Feature Table for Per-Pin VrefQ Adjustment DQ0-DQ7 [40h]

Subfeature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	
B0	VREF Offset for DQ1					VREF Offset for DQ0			
B1	VREF Offset for DQ3					VREF Offset for DQ2			
B2	VREF Offset for DQ5					VREF Offset for DQ4			
B3	VREF Offset for DQ7					VREF Offset for DQ6			

NOTE 1 Per-Pin VrefQ adjustment via absolute setting (optional) is supported via FA40h, 41h, and 42h on JESD230F devices

Table 7.12-2 — Feature Table for Per-Pin VrefQ Adjustment DBI [41h]

Subfeature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	
B0	Reserved					VREF Offset for DBI			
B1	Reserved								
B2	Reserved								
B3	Reserved								

For each VREF Offset setting in FA40h and FA41h the decoding is as follows:

- 0000b: 0 step offset (default)
- 0001b: +1 step offset
- 0010b: +2 steps offset
- 0011b: +3 steps offset
- 0100b – 0111b: +4 ~ +7 steps offset
- 1000b: 0 step offset
- 1001b: -1 step offset
- 1010b: -2 steps offset
- 1011b: -3 steps offset
- 1100b – 1111b: -4 ~ -7 steps offset

8 Data Interface and Timing

8.1 Test Conditions

8.1.1 LTT/PI-LTT Interface Devices

The testing conditions that shall be used to verify compliance with a particular timing mode are shown in **Table 8.1-1**. The test conditions are the same regardless of the number of LUNs per Target.

Table 8.1-1 — Testing Conditions (LTT/PI-LTT)

Parameter	LTT	PI-LTT
Positive input transition	VIL.LTT (DC) to VIH.LTT (AC)	VIL.PI-LTT (DC) to VIH.PI-LTT (AC)
Negative input transition	VIH.LTT (DC) to VIL.LTT (AC)	VIH.PI-LTT (DC) to VIL.PI-LTT (AC)
Minimum input slew rate (only for DQS_x_t/c and RE_x_n/c ¹)	1 V/ns to 7 V/ns for ≤3.6 Gbps 1.5 V/ns to 7 V/ns for >3.6 Gbps	1 V/ns to 7 V/ns for ≤3.6 Gbps 1.5V/ns to 7V/ns for >3.6 Gbps
Input timing levels	crosspoint	crosspoint
Output timing levels	crosspoint	crosspoint
Driver strength	Default ²	Default ²
Output reference load	“50 Ohms or Less(VSP)” to Vss	“50 Ohms or Less(VSP)” to Vss

NOTE 1 Input slew rate is only valid for strobe signals such as DQS_x_t/c and RE_x_n/c, not for DQ.
 NOTE 2 Default value is 37.5 or “50 ohms or Less(VSP)” for pull-down, and “50 ohms or Less(VSP)” Channel ODT setting for the pull-up.

The testing conditions used for output slew rate testing are specified in **Table 8.1-2**. Output slew rate is verified by design and characterization; it may not be subject to production test. The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate. Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal. The differential parameters are used when the DQS signal is configured to operate as a differential signal.

Table 8.1-2 — Testing Conditions for Output Slew Rate (LTT)

Parameter	Single-Ended	Differential
VOL(AC)	0.2 * VOH.LTT,nom	0.2 * VOH.LTT,nom
VOH(AC)	0.8 * VOH.LTT,nom	0.8 * VOH.LTT,nom
VOLDiff(AC)	-0.6 * VOH.LTT,nom	-0.6 * VOH.LTT,nom
VOHDiff(AC)	0.6 * VOH.LTT,nom	0.6 * VOH.LTT,nom
Positive output transition	VOL (AC) to VOH (AC)	VOLDiff(AC) to VOHDiff(AC)
Negative output transition	VOH (AC) to VOL (AC)	VOHDiff(AC) to VOLDiff(AC)

Table 8.1-2 — Testing Conditions for Output Slew Rate (LTT) (cont'd)

Parameter	Single-Ended	Differential
tRISE ¹	Time during rising edge from VOL(AC) to VOH(AC)	—
tFALL ¹	Time during falling edge from VOH(AC) to VOL(AC)	—
tRISEdiff ²	—	Time during rising edge from VOLdiff(AC) to VOHdiff(AC)
tFALLdiff ²	—	Time during falling edge from VOHdiff(AC) to VOLdiff(AC)
Output slew rate rising edge	$[VOH(AC) - VOL(AC)] / tRISE$	$[VOHdiff(AC) - VOLdiff(AC)] / tRISEdiff$
Output slew rate falling edge	$[VOH(AC) - VOL(AC)] / tFALL$	$[VOHdiff(AC) - VOLdiff(AC)] / tFALLdiff$
Output reference load	1 pF to VssQ	1 pF to VssQ
NOTE 1	Refer to Figure 8.1-1 .	
NOTE 2	Refer to Figure 8.1-2 .	
NOTE 3	2 pF reference load for data rates up to 3200 MT/s and 1 pF for data rates > 3200 MT/s	

Table 8.1-3 — Testing Conditions for Output Slew Rate (PI-LTT)

Parameter	single-ended	differential
VOL(AC)	$0.2 * VOH.PI-LTT,nom$	$0.2 * VOH.PI-LTT,nom$
VOH(AC)	$0.8 * VOH.PI-LTT,nom$	$0.8 * VOH.PI-LTT,nom$
VOLDiff(AC)	$-0.6 * VOH.PI-LTT,nom$	$-0.6 * VOH.PI-LTT,nom$
VOHdiff(AC)	$0.6 * VOH.PI-LTT,nom$	$0.6 * VOH.PI-LTT,nom$
Positive output transition	VOL (AC) to VOH (AC)	VOLDiff(AC) to VOHdiff(AC)
Negative output transition	VOH (AC) to VOL (AC)	VOHdiff(AC) to VOLDiff(AC)
tRISE ¹	Time during rising edge from VOL(AC) to VOH(AC)	—
tFALL ¹	Time during falling edge from VOH(AC) to VOL(AC)	—
tRISEdiff ²	—	Time during rising edge from VOLDiff(AC) to VOHdiff(AC)
tFALLdiff ²	—	Time during falling edge from VOHdiff(AC) to VOLDiff(AC)
Output slew rate rising edge	$[VOH(AC) - VOL(AC)] / tRISE$	$[VOHdiff(AC) - VOLDiff(AC)] / tRISEdiff$
Output slew rate falling edge	$[VOH(AC) - VOL(AC)] / tFALL$	$[VOHdiff(AC) - VOLDiff(AC)] / tFALLdiff$
Output reference load	1 pF to VssQ	1 pF to VssQ
NOTE 1	Refer to Figure 8.1-1 .	
NOTE 2	Refer to Figure 8.1-2 .	
NOTE 3	2 pF reference load for data rates up to 3200 MT/s and 1 pF for data rates > 3200 MT/s	

8.1.1 LTT/PI-LTT Interface Devices (cont'd)

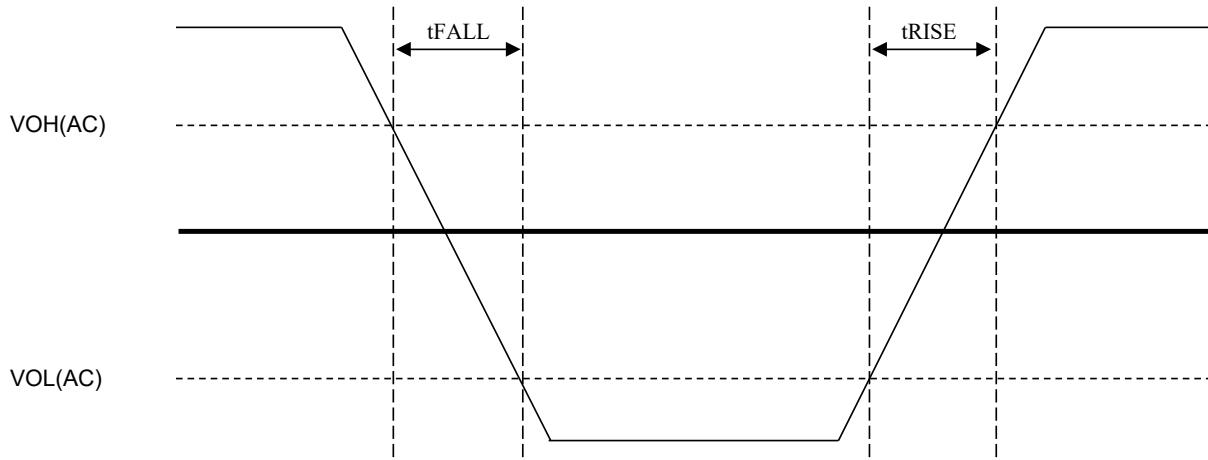


Figure 8.1-1 — t_{RISE} and t_{FALL} Definition for Output Slew Rate, (Single-ended)

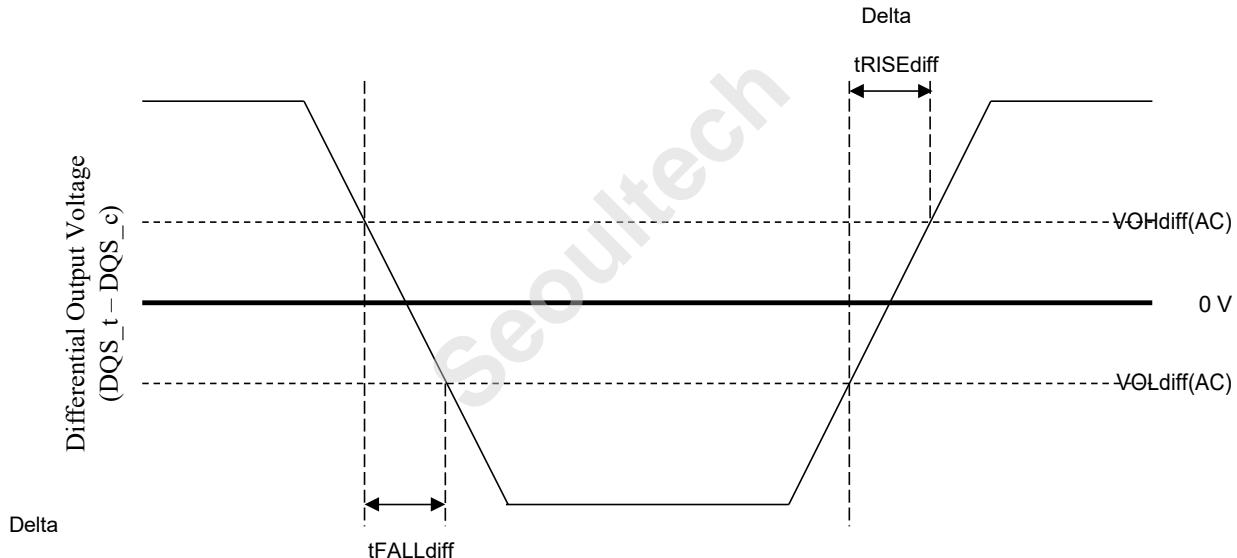


Figure 8.1-2 — $t_{RISEdiff}$ and $t_{FALLdiff}$ Definition for Output Slew Rate, (Differential)

The output slew rate matching ratio is specified in **Table 8.1-4**. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling is faster than the rising edge, then divide the falling slew rate by the rising slew rate. The output slew rate mismatch is verified by design and characterization; it may not be subject to production test.

Table 8.1-4 — Output Slew Rate Matching Ratio (LTT/PI-LTT)

Parameter	Max
Output Slew Rate Matching Ratio (Pull-up to Pull-down), without ZQ calibration	1.4
Output Slew Rate Matching Ratio (Pull-up to Pull-down), with ZQ calibration	1.3

8.2 ZQ Calibration

ZQ calibration is required to make the driver strength of LUNs attached to the same channel consistent and it helps improve the signal integrity. ZQ calibration is highly recommended to be used for higher speed over 400 Mbps

8.2.1 ZQ Calibration Command Sets

If a device supports ZQ calibration, Long ZQ calibration and Short ZQ calibration shall be supported.

Table 8.2-1 — Long ZQ Calibration and Short Calibration Commands

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target level Commands
Long ZQ calibration	M	F9h	-			
Short ZQ calibration	M	D9h	-			

8.2.2 ZQ Calibration Process

ZQ calibration shall be performed after the driver strength setting and it shall be re-calibrated when the driver strengths are changed. ZQ calibration shall be done when the target device does not perform any other operation. If VREFQ is used, VREFQ shall be also enabled before ZQ calibration performs.

F9h is used for an initial ZQ calibration and D9h is for a run-time ZQ calibration. The initial ZQ calibration takes 1us as maximum and the run-time ZQ calibration does 0.3 μ s as maximum. RZQ ball of the BGA package shall be connected to Vss through 300 ohm resistor (300 ohm +/- 1% tolerance external resistor).

During busy period for ZQ calibration, any command including Read Status shall not be issued. The host shall check Busy/Ready status via R/Bn pin or shall wait the specified period of time (i.e., tZQCL or tZQCS) to ensure the ZQ calibration is done. After the device turns into Ready state, the host shall issue Read Status to check the pass/fail of the calibration. If Reset command is issued during ZQ calibration, the state of the devices is not guaranteed and host needs to re-run the ZQ calibration. Before executing short ZQ calibration operation, long ZQ calibration shall be completed successfully, without any abortion by Reset, at least once after power-up. When ZQ calibration is aborted by a Reset command, it will take maximum 10 μ s (i.e., tRST) to complete the reset operation. If Reset operation is done during long ZQ calibration, the ZQ calibrated value will return to the factory default one. If Reset is done during short ZQ calibration, the ZQ calibrated value will return to the vendor specific value. If ZQ calibration operation fails, the ZQ calibrated value will return to the vendor specific value.

During the ZQ calibration, all devices are connected to the DQ bus should be in high impedance, therefore the on-die-termination is off.

Commands for ZQ calibration are followed by one cycle of LUN selection. 00h for LUN select points LUN0 and 01h does LUN1. **Figure 8.2-1** illustrates the sequence of ZQ calibration.

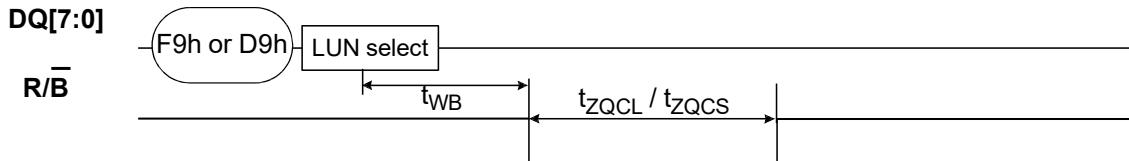


Figure 8.2-1 — ZQ Calibration Sequence

8.3 Package Electrical Specifications and Pad Capacitance

The requirements in this clause apply to devices that support the VccQ=1.2 V and VccQL=0.6 V. The requirements in this clause are optional when the device supports I/O speeds 533 MT/s or less and required when the device supports I/O speeds greater than 533 MT/s.

ZIO applies to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c. TdIO RE applies to RE_t and RE_c. TdIO and TdIOMismatch apply to DQ[7:0], DQS_t, and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (i.e., package channel), but not required across all channels on a given package.

Table 8.3-1 — Package Electrical Specification

Symbol	Parameter	≤400 MT/s		533 MT/s		667 MT/s		800 MT/s to 1200 MT/s		1333 MT/s to 3600 MT/s		3600 MT/s to 4800 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Z _{IO}	Input/Output Zpkg	35	90	35	90	35	90	35	90	35	90	30	80	ohms
T _d _{IO}	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	-	130	-	115	ps
T _d _{IO} RE	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	-	130	-	115	ps
T _d _{IO} Mismatch	Input/Output Pkg Delay Mismatch	-	50	-	40	-	40	-	40	-	40	-	40	ps
D Z _{IO} DQS	Delta Zpkg for DQS_t and DQS_c	-	10	-	10	-	10	-	10	-	10	-	10	ohms
D T _d _{IO} DQS	Delta Pkg Delay for DQS_t and DQS_c	-	10	-	10	-	10	-	10	-	10	-	10	ps
D Z _{IO} RE	Delta Zpkg for RE_t and RE_c	-	10	-	10	-	10	-	10	-	10	-	10	ohms
D T _d _{IO} RE	Delta Pkg Delay for RE_t and RE_c	-	10	-	10	-	10	-	10	-	10	-	10	ps
NOTE 1 The package parasitic(L and C) are validated using package only samples. The capacitance is measured with Vcc, VccQ, Vss, VssQ shorted with all other signal pins floating. The inductance is measured with Vcc, VccQ, Vss, and VssQ shorted and all other signal pins shorted at the die side(not pin).														
NOTE 2 Package only impedance (ZIO) is calculated based on the Lpkg and Cpkg total for a given pin where: $ZIO(\text{total per pin}) = \sqrt{L_{\text{pkg}}/C_{\text{pkg}}}$														
NOTE 3 Package only delay(TdIO) is calculated based on Lpkg and Cpkg total for a given pin where: $TdIO(\text{total per pin}) = \sqrt{L_{\text{pkg}} \cdot C_{\text{pkg}}}$														
NOTE 4 Mismatch for TdIO (TdIOMismatch) is value of Pkg Delay of fastest I/O minus the value of Pkg Delay for slowest I/O.														
NOTE 5 Delta for DQS is Absolute value of ZIO(DQS_t)-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO(DQS_t)-TdIO(DQS_c) for delay(Td)														
NOTE 6 Delta for RE is Absolute value of ZIO(RE_t)-ZIO(RE_c) for impedance(Z) or absolute value of TdIO(RE_t)-TdIO(RE_c) for delay(Td)														

8.3 Package Electrical Specifications and Pad Capacitance (cont'd)

Table 8.3-2 — Pad Capacitances Apply to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c

Symbol	Parameter	<=400 MT/s		533 MT/s to 1200 MT/s		1200 MT/s to 2400 MT/s		2400 MT/s to 3600 MT/s		3600 MT/s to 4800 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C _{IO}	Input/Output Capacitance	-	2.5	-	2.5	-	1.6	-	1.6	-	1.2	pF
C _{ZQ}	ZQ capacitance	-	2.875	-	2.875	-	2.875	-	2.875	-	2.875	pF
D C _{IO DQS}	Delta Input/Output Capacitance DQS_t and DQS_c	0	0.2	0	0.2	0	0.2	-	0.2	-	0.2	pF
D C _{IO RE}	Delta Input/Output Capacitance for RE_t and RE_c	0	0.2	0	0.2	0	0.2	-	0.2	-	0.2	pF
<p>NOTE 1 These parameters are not subject to a production test. It is verified by design and characterization. The capacitance is measured according to JEP147 ("Procedure For Measuring Input Capacitance Using a Vector Network Analyzer(VNA)") with Vcc, VccQ, VccQL, Vss, and VssQ applied and all other pins floating (except the pin under test). VccQ = VccQL = 1.2 V, VBIAS = 0.2 V and on-die termination off for LTT interface. VccQ = 1.2 V, VccQL = 0.6 V, VBIAS = 0.15 V and on-die termination off for PI-LTT interface.</p> <p>NOTE 2 These parameters apply to monolithic die, obtained by de-embedding the package L and C parasitics.</p> <p>NOTE 3 Delta for DQS is the absolute value of C_{IO}(DQS_t) - C_{IO}(DQS_c).</p> <p>NOTE 4 Delta for RE is the absolute value of C_{IO}(RE_t) - C_{IO}(RE_c).</p>												

8.4 tCD Parameter

Table 8.4-1 — Timing Parameter Description

Parameter	Description
tCD	CE setup time to DQS(DQS_t) low after CE has been high for greater than 1 μ s

Table 8.4-2 — tCD Timing Parameter

Parameter	200 MHz		266 MHz		333 MHz		400 MHz		533 MHz		600 MHz		Unit
	Min	Max											
tCD ¹	100	-	100	-	100	-	100	-	100	-	100	-	ns
NOTE 1 If host is unable to track CE high time, then host shall use tCD timing.													

8.5 Additional Timing Parameter for I/O Speed Greater than 400 MT/s

Table 8.5-1 — Timing Parameter Description

Parameter	Description
tWHR2	WE High to RE Low for Random data out
tADL	Address to Data Loading Time
tCR	CE Low to RE Low
tCR2	CE Low to RE Low when CE has been high for a period greater than or equal to 1 μ s. If host is unable to track CE high time, then host shall use tCR2 timing for tCR parameter.

Table 8.5-2 — Timing Parameters Shall be Used for NAND Device that are Capable of I/O Speed Greater than 400 MT/s

Parameter	Min	Max	Unit
tWHR2	400	-	ns
tADL	412	-	ns
tCR	10	-	ns
tCR2	100	-	ns

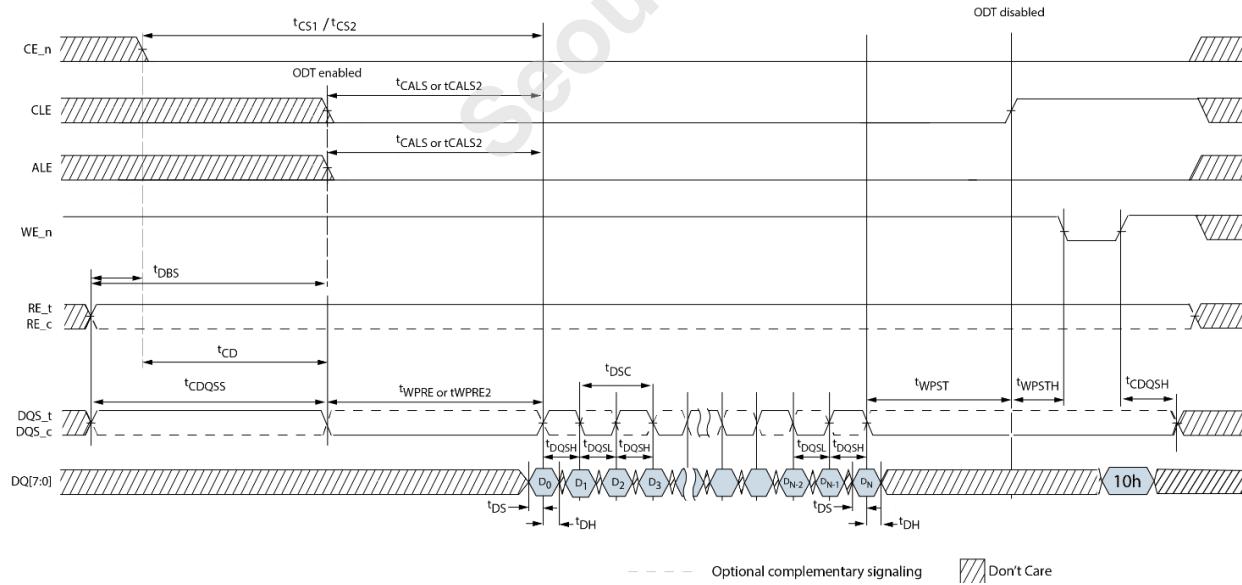


Figure 8.5-1 — Timing Parameter Description

8.6 VccQ and VccQL Power-On/Off

When users boot up or power down a NAND device, VccQ must be equal or higher than VccQL. NAND devices only allow the four cases power-on/off described in **Figure 8.6-1**.

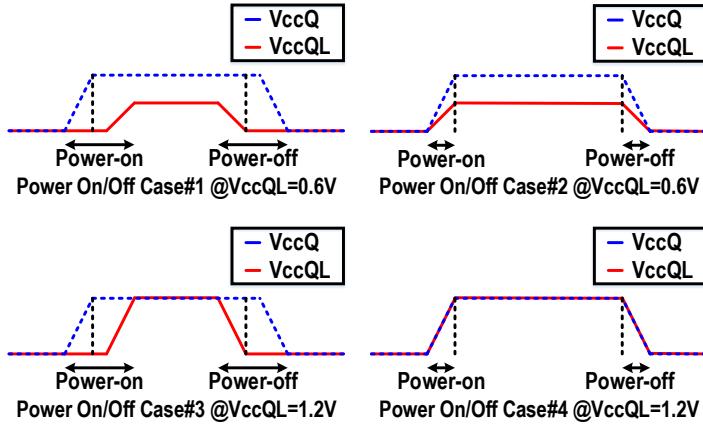


Figure 8.6-1 — VccQ and VccQL Power-On/Off when Boot-Up or Power-Down

8.7 Data Training

8.7.1 ODT Disable and Re-Enable

8.7.1.1 Need for ODT Control during LTT/PI-LTT Interface Training

ODT termination causes signal swing on the channel to be smaller than that of an unterminated channel.

ODT termination is typically enabled during data input and data output bus cycles. Set Feature commands have data input cycles and for some NAND devices, ODT will turn on during these data input cycles. Read Status has data output cycles and for some NAND devices, ODT will turn on during these data output cycles.

Once the LTT/PI-LTT interface has been enabled, the NAND and controller internal VrefQ will still be at an untrained state and the smaller signal swing with ODT can cause failure of Set Feature or Read Status and Get Feature sequences.

Efficient ODT disable/re-enable control methods are needed to control ODT termination while the LTT/PI-LTT interface is still being configured and trained.

8.7.1.2 ODT Control NAND Device Types

NAND devices fall under the following types:

- Type1 NAND Device: Employ Pin/Hardware based ODT Control
- Type2 NAND Device: Employ Command based ODT Control

On Type1 devices, ODT control is done via pin or the ODT control is already built into the NAND hardware itself and no additional command for ODT control is needed. Type1 devices shall ignore 1Bh and 1Ch commands.

8.7.1.2 ODT Control NAND Device Types (cont'd)

For reference, Pin based ODT and 1Bh/1Ch command based ODT control methods are not supported in the SCA protocol.

On Type2 devices, ODT control is done via commands (i.e., Matrix Termination). Type2 devices shall support one of the following options for ODT disable and re-enable:

- 1Bh/1Ch Commands:
 - 1Bh turns OFF target and non-target ODT operations
 - 1Ch re-enables target and non-target ODT operations
- Vendor Specific Command/Address sequence

8.7.1.3 ODT Disable (1Bh) and ODT Re-Enable (1Ch) Commands

ODT Disable (1Bh) and ODT Re-Enable (1Ch) commands are used on Type2 NAND devices for ODT termination control.

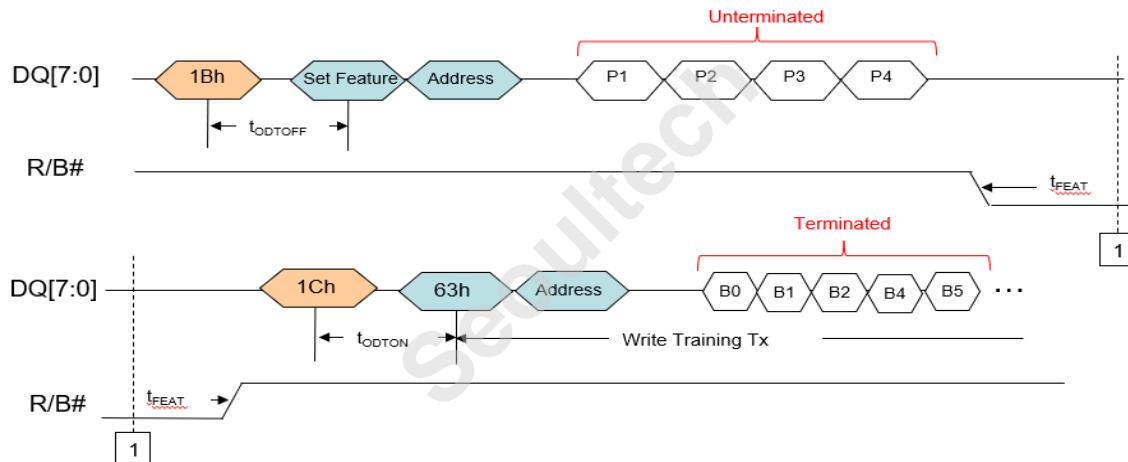


Figure 8.7-1 — ODT Disable (1Bh) and ODT Re-Enable (1Ch) Commands Timing Diagram

Table 8.7-1 — tODTOFF and tODTON Specifications

Parameter	Symbol	Min	Max	Notes	Unit
ODT Disable (1Bh) command to next command	tODTOFF	100	-		ns
ODT Re-Enable (1Ch) command to next command	tODTON	100	-		ns

8.7.2 Interface Initialization and Training Flows

Interface initialization shall be done before training at slower interface speeds such as high speed interface setting, driver strength setting and ZQ calibration. After power-up, LTT interface is enabled with NAND internal VrefQ by default and all the initial interface settings would be configured via FA02h, FA10h, and FA22h.

In NAND devices supporting PI-LTT (optional feature), PI-LTT mode can be enabled via set feature command or automatically detected. In order to support any case, controller shall implement set feature command to enable PI-LTT interface.

Training features shown in this clause shall be supported by NAND devices operating over 800 MT/s in heavily loaded systems. If the host uses the NAND device over 800 MT/s, the host shall complete all the trainings defined in the clause when training is required. **Figure 8.7-2** shows when each training shall be done after power-on for devices that support LTT/PI-LTT interface.

DCC Training is the feature for the NAND to compensate duty cycle mismatch of RE_t/c signal. Read/Write DQ Training is the feature for the host to align DQS and DQ signals caused by un-matched DQS-DQ path. ODT shall be turned off via ODT disable command or ODT pin prior to issuing set feature command to configure settings during each training operation, and ODT shall be turned on via ODT enable command or ODT pin prior to issuing training command sequences (i.e., random data out sequence for DCC training, 63h command for write training).

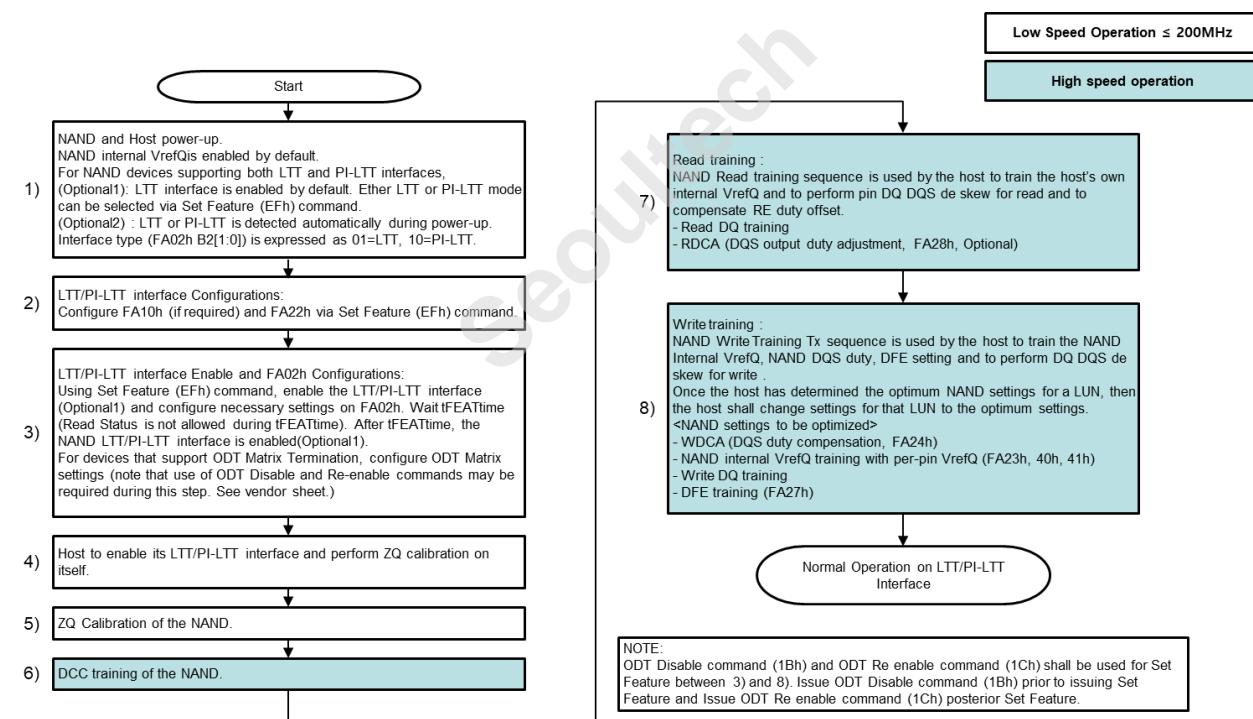


Figure 8.7-2 — LTT/PI-LTT Interface Configurations and Training Flow

8.7.2 Interface Initialization and Training Flows (cont'd)

The following are Read Status, Read ID, Get Feature, and Random Data out command restrictions during the LTT/PI-LTT interface training flows:

- 1) Read Status, Read ID, Get Feature and Random Data out commands are not allowed during and in between 1(NAND-side LTT/PI-LTT interface enable) and 4(Controller-side LTT/PI-LTT interface enable)
- 2) Read Status and Get Feature commands are allowed during 5(NAND-side ZQ calibration), 6(NAND-side DCC training) and prior to 7(Read Training) completion, subject to the following conditions:
 - ODT on the NAND-side must be turned off prior to data output cycles (i.e., through ODT Disable command or ODT pin)
 - ODT on the controller-side must also be turned-off prior to Read Status/Read ID/Get Features/Random Data out sequence
 - Read Status/Read ID/Get Features/Random Data out must be done at a $t_{RC}(\text{avg}) \geq 30$ ns. The output signals shall meet Single-Ended AC and DC Output Levels for Unterminated DQ-Related Signals specifications when evaluated using Output Timing Reference Load for Unterminated Channel, and with default PDSS and default CH_ODT settings
- 3) Read Status, Read ID, Get Feature and Random Data out commands are allowed after 7(Read Training) completion without having to disable ODT on NAND-side or Controller-side prior to Read Status/Read ID/Get Features/Random Data out sequence.

8.7.3 DCC Training

DCC Training shall be performed after the ZQ calibration is completed. This clause defines two types of DCC. One is explicit DCC and the other is implicit DCC.

Explicit DCC is initiated by the host to issue specific command sequence defined in clause **8.7.3.1** or **8.7.3.2**. Either or both Explicit DCC shall be supported by the NAND devices operating over 800 MT/s.

Implicit DCC is optional feature for the NAND devices and is initiated by the host to set DCCI_EN enable which is assigned in B0[1] of Feature Address 20h. If DCCI_EN is enabled, the NAND device carries out DCC training to update the training result during warm up cycles where “warm up cycles” is sometimes referred to “DQS latency”. Implicit DCC may require specific number of warm up cycles to be set and it shall be given by vendor datasheet.

8.7.3.1 DCC (RE_t/c) Training Using Set Feature

DCC training using Set Feature is initiated by the host to set DCCE_EN enable which is assigned in B0[0] of Feature Address 20h. When this is enabled, DCCI_EN which is assigned in B0[1] is “don’t care”. On power-up, DCCE_EN shall be disabled. The host shall enable it to perform DCC Training. Refer to Feature Address description for more information.

After Set Feature, the host shall issue the Random Data Out command with address information based on the Set Feature command used to enable the DCC training feature. If the Set Feature command used was an EFh command, then the addresses for the Random Data Out command sequence shall be filled with 00h. If the Set Feature command used was the D5h (Set Feature for Each LUN) command, then the addresses for the Random Data Out command sequence must have the same LUN address that was used during the D5h command. If LUN address is not used in the Random Data Out sequence, then fix all column address to “00h”. The host shall then calibrate RE_t and RE_c by sending those signals for a page size. (Page size shall be given by vendor datasheet.)

8.7.3.1 DCC (RE_t/c) Training Using Set Feature (cont'd)

During the data output cycles produced by these RE_t and RE_c toggles, the DQ and DQS of the LUNs under training may be driven or Hi-Z depending on the NAND vendor DCC Training implementation. Refer to the NAND vendor datasheet to see if DQ and DQS are driven or Hi-Z during this time. The data for these data output cycles shall be invalid and ignored by the host. When doing multi-LUN DCC training for LUN's which share the same channel, the DQ and DQS signals of the LUNs involved in the training shall be Hi-Z during the data output cycles of the Random Data Out sequence to avoid bus contention.

After sending RE_t and RE_c for page size length, Status Check shall be performed to confirm whether DCC is Pass or Fail via SR[0]. If fail, the host shall issue Random Data Out command and resend RE_t and RE_c signals to calibrate again. If EFh is used, all the LUNs under the Target perform DCC (All LUN DCC). If D5h command is used, selected LUN under the Target performs DCC (Single LUN DCC). The device may support either or both All LUN DCC and Single LUN DCC. See vendor's datasheet. After completing Explicit DCC using Set Feature, DCCE_EN shall be set to 0.

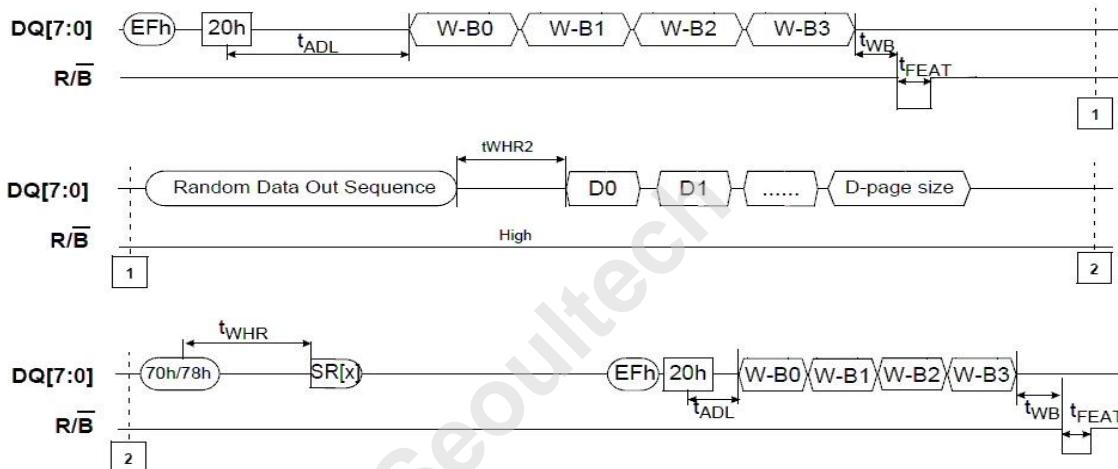


Figure 8.7.3 — DCC (RE_t/c) Training using Set Feature

8.7.3.2 DCC (RE_t/c) Training Using Command (Optional)

DCC training using a command can be initiated using CMD18h followed by LUN Address. After issuing LUN address, the host shall calibrate RE_t and RE_c by toggling these signals for a page size. (Page size shall be given by vendor data sheet). The data returned by the device is vendor specific data pattern so that there is no impact of data pattern on DCC training. After sending the required number of RE_t and RE_c signals, Status Check shall be performed to confirm whether DCC is Pass or Fail. If status is a Fail, user has to issue RESET command (FFh) wait for the RESET command to execute and then re-issue the Command based DCC sequence.

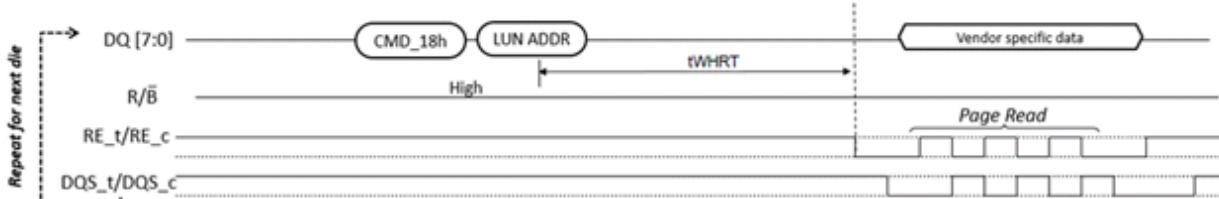


Figure 8.7.4 — DCC (RE_t/c) Training using Command (Optional)

Timing specs of RE_t/RE_c during DCC page read will follow normal Read timing as per vendor datasheet.

8.7.4 Read DQ Training

Read DQ Training is the function that outputs a 16 bit user-defined pattern on each of the DQ pins. It means a total of 16 bytes is output by the NAND device (note some vendors may provide a 32 byte pattern).

Read DQ Training is initiated by issuing a [Read DQ Training] command 62h followed by LUN Address then three address cycles. Three address cycles are 1st address (8bit invert mask), 2nd address (first eight bit pattern) and 3rd address (second eight bit pattern). **Figure 8.7-5** shows example data pattern (i.e., 1st 35h, 2nd 5Ah, 3rd 82h address).

Pin	Inverse Setting		0~15															16~31 (Optional)														
	(Mask)		1 st Input DATA : 5Ah								2 nd Input DATA : 82h								Swap 1st,2nd data of DQ4~7 ↔ DQ0~3 (Optional)													
DQ0	1 (Inverse)	35h	1	0	1	0	0	1	0	1	1	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	0	
DQ1	0		0	1	0	1	1	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	0	
DQ2	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	1	
DQ3	0		0	1	0	1	1	0	1	0	0	1	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	1	
DQ4	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	0	0		
DQ5	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	1	
DQ6	0		0	1	0	1	1	0	1	0	0	1	0	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	1
DQ7	0		0	1	0	1	1	0	1	0	0	1	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	1	

Figure 8.7-5 — Example of User Defined Pattern for Read Training

If '1' is indicated by a bit in 1st address, DQx corresponding to a bit shall be inverted and the NAND device outputs data pattern designated by 2nd and 3rd addresses masked I/O following in invert mask indicated by 1st address by RE, /RE toggling, the data will be inverted by masked I/O. For DBI pin behavior during Read DQ Training, refer to clause **8.9.3 DBI Behavior During Read DQ Training**.

If host issue RE, /RE toggling for more than the vendor defined pattern length, data will be wrapped.

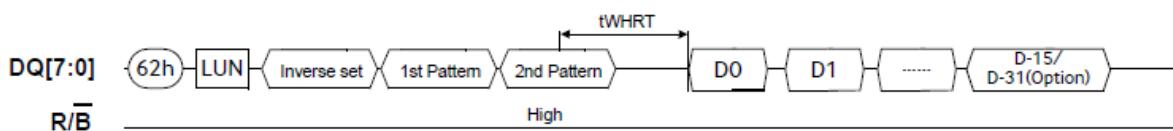


Figure 8.7-6 — Read DQ Training

During Read DQ Training, the controller shall optimize its own internal VrefQ voltage (required on LTT interface) and also optimize the strobe point of DQ signals by DQS. tDVWp is the output valid window for a single DQ pin while tDVWd is the output valid window of all DQ pins taken as a group. The NAND may require DCC training to meet tDVWp or tDVWd specifications. In order for a system to take advantage of the wider per-pin data-eye opening (tDVWp) though, the system must be able to adjust each DQ pin relative to DQS during Read DQ Training.

8.7.4 Read DQ Training (cont'd)

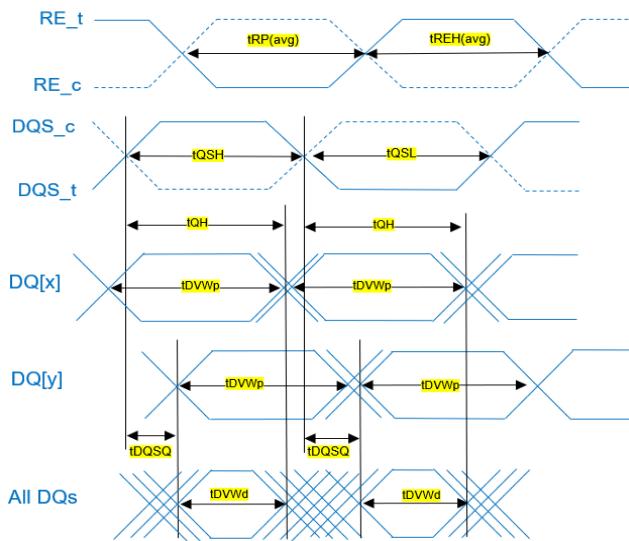


Figure 8.7-7 — Read Data Output Valid Window Timings

8.7.5 Read Duty Cycle Adjustment (RDCA, Optional)

Read Duty Cycle Adjustment (RDCA) is an optional feature that provides a way to compensate input RE_t/c duty cycle distortion at the NAND device. The RDCA feature is recommended to apply for the offset compensation of the duty cycle mismatch after DCC training and is controlled via FA28h.

8.7.6 Write DQ Traini12ng (Tx Side)

To perform Write training at Tx side, the controller shall issue 63h command followed LUN address. After issuing LUN address, the host shall input data pattern and confirm whether the input is successfully done by checking the output by NAND in following sequence.

Data sizes for Write DQ are pre-defined by NAND. The host shall recognize the data sizes by Get Feature (Feature Address = 20h, B2) and shall input and output the data based on the size.

After writing data to the NAND with 63h command, the data can be read back with 64h command followed by LUN address and the results shall be compared with “expected” data to see if further training (DQ delay) is needed. For DBI pin behavior during Write DQ Training (Tx Side) refer to clause **8.9.2 DBI Behavior During Write DQ Training (Tx Side)**. If fewer data than pre-defined data bytes are written, then unwritten registers will have un-defined data when read back. If over pre-defined data bytes write/read were executed, the data are also un-defined and invalid.

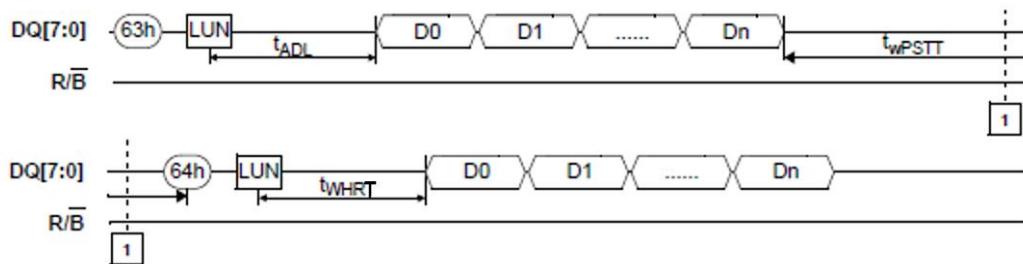


Figure 8.7-8 — Write DQ Training (Tx side)

8.7.6.1 NAND Internal VrefQ Training

The controller shall find the optimum internal VrefQ level for each NAND die by performing internal VrefQ scan and using the Write Training Tx sequence to produce a pass/fail result each scanned internal VrefQ level. Once the optimum level has been found, the host shall configure the NAND to use that level.

The host shall not set the NAND internal VrefQ to a setting beyond the allowable internal VrefQ range during Write Training Internal VrefQ training.

See Feature Address 23h for NAND internal VrefQ, step size, range, and accuracy requirements.

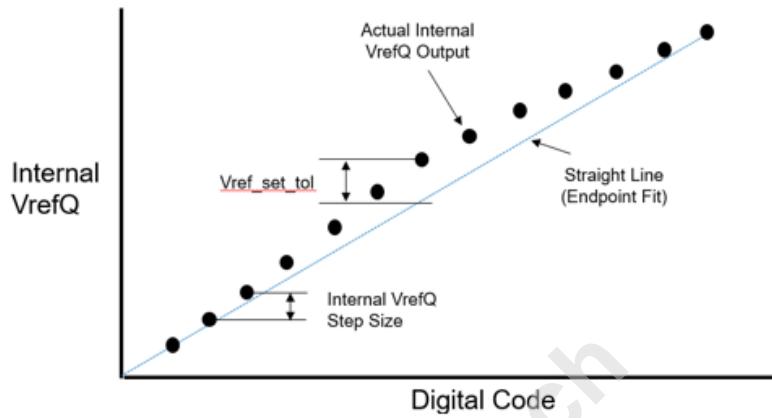
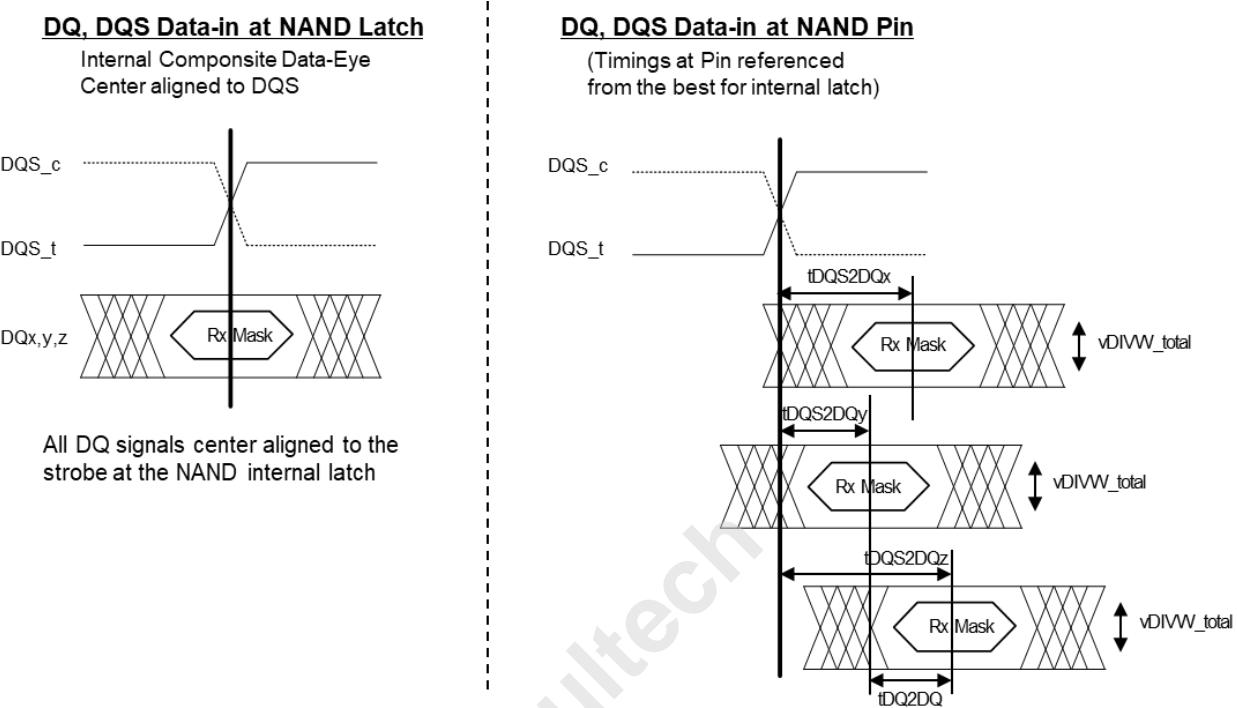


Figure 8.7-9 — NAND Internal VrefQ Characteristics

8.7.6.2 Timing De-skew of Each DQ Versus DQS

The controller shall also find the optimum input timing by timing scan between each DQ to DQS_c/DQS_t and shall compensate input timing of each DQ and DQS to be the optimum per pin per chip.



NOTES:

1. tDQS2DQ is measured at the center(midpoint) of the tDIVW window
2. DQz represents the max tDQS2DQ in this example
3. DQy represents the min tDQS2DQ in this example

Figure 8.7-10 — Write DQ Training (Tx Side) Timing De-skew at NAND Latch Versus NAND Pin

The device uses an unmatched DQS-DQ path to enable high-speed performance. The DQS strobe must be trained to arrive at the DQ latch center-aligned with the data eye. The DQ receiver is located at the DQ pad and has a shorter internal delay than the DQS signal. The DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and write DQ training is accomplished by delaying the DQ signals relative to DQS such that the data eye arrives at the NAND internal latch centered on the DQS transition.

The DQ-to-DQS tDQS2DQ and tDQ2DQ timings are measured from the DQS_t/DQS_c cross-point to the center of the DQ Rx Mask. The timings at the pins are referenced with respect to all DQ signal center-aligned at the NAND internal latch. The data-to-data offset is defined as the difference between the min and max tDQS2DQ for a given component.

As temperature and voltage change on the NAND die, the DQS clock tree will shift and may require retraining. The DQS oscillator feature is used to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time.

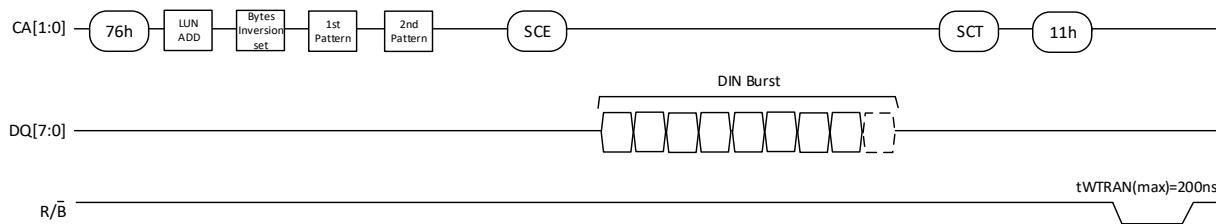
8.7.6.2 Timing De-skew of Each DQ Versus DQS (cont'd)

Table 8.7-2 — DQ Rx Timing Specification in Unmatched DQ-DQS Receiver

Parameter	Symbol	Min	Max	Unit	Notes
DQ to DQS offset	tDQS2DQ	100	1100	ps	-
DQ to DQ offset	tDQ2DQ	-	150	ps	-
DQ to DQS offset temperature variation	tDQS2DQ_temp	-	0.85	ps/°C	1, 2
DQ to DQS offset voltage variation	tDQS2DQ_volt	-	0.85	ps/mV	1, 2
NOTE 1	tDQS2DQ max. delay variation as a function of temperature and voltage variation				
NOTE 2	Temperature and voltage variation are included in tDQS2DQ Min/Max range.				

8.7.7 Write DQ Training (Rx Side, Optional)

To perform Write training at Rx side, the controller shall issue 76h command followed by LUN address. After issuing LUN address, the host shall issue 3 address cycles for data pattern format. The definition of these 3 address cycles is the same as the ones mentioned in read training. After the 3 address cycles, the host shall issue data input with the same pattern determined by the 3 address cycles for 1 full page. The input data shall be wrapped around the data pattern length (16 or 32) until a full-page data is issued. The training sequence shall be ended by 11h command and the NAND will perform write training during the R/B_n time (tWRTN). The host may poll the R/B_ status by status command to check the completion of the training operation. The status of the training for each DQ can be checked by issuing Get Feature by LUN with address 21h (B1 and B2). The complete byte definition is given in the Feature Address 21h table.



DIN Burst: Data Input with the same pattern specified in 3 address cycle wrapping around the data pattern length (16 or 32) for 1 full page

Figure 8.7-11 — Write DQ Training (Rx Side) Optional

If Write Training (Rx Side) passes, then the host may skip Write Training (Tx Side).

8.7.7 Write DQ Training (Rx Side, Optional) (cont'd)

The flow chart in **Figure 8.7-12** is an example of the process for doing Write Training on the Rx side.

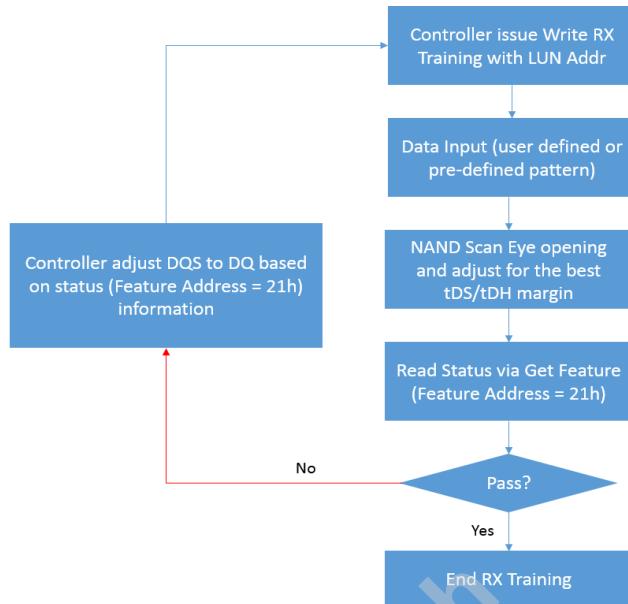


Figure 8.7-12 — Flow Chart for Write DQ Training (Rx Side)

8.7.7.1 Write DQ Training (Rx Side) With Internal VrefQ Training (Optional and LTT/PI-LTT Interface Only)

Write DQ Training (Rx Side) with Internal VrefQ Training is an optional feature used only on the LTT/PI-LTT interface. It is enabled by setting Feature Address 21h B0[2]=1. On the CTT Interface, Feature Address 21h B0[2] is ignored by the NAND.

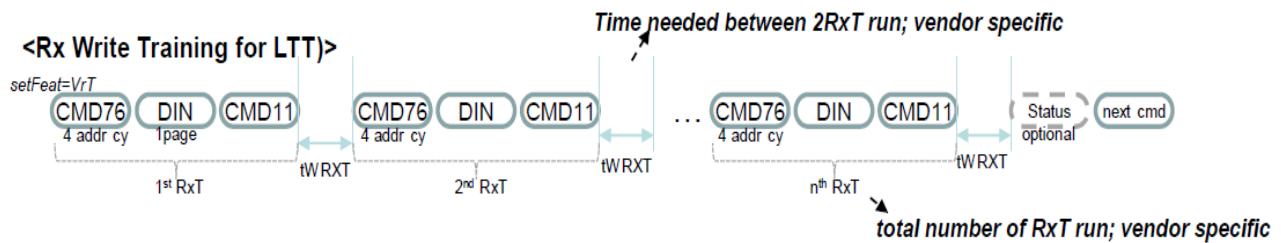


Figure 8.7-13 — Write DQ Training (Rx Side) with Internal VrefQ Training Mode Sequence

An RxT sequence is defined as a CMD76h (4 address cycles) – DIN (1 page) – CMD11h sequence. At the end of each RxT sequence, a wait time of tWRXT(min) of 200 ns is required. The host repeats the RxT sequence an n number of times, where n is vendor specific. Status Reads (Read Status and Get Features commands) are available after the whole sequence has completed (after the tWRXT time of the nth RxT iteration has completed).

If Write Training (Rx Side) passes, then the host may skip Write Training (Tx Side). After the training has completed, the host shall clear Feature Address 21h B0[2] = 0.

8.7.8 Write Duty Cycle Adjustment (WDCA)

Write Duty Cycle Adjustment (WDCA) is the feature that provides a way to compensate for input DQS duty cycle loss at the NAND device. The WDCA feature is controlled via FA24h.

Figure 8.7-14 shows the NAND interface training flow with WDCA. The controller repeats between configuring WDCA settings and performing Write Training sequence to find the optimum WDCA setting.

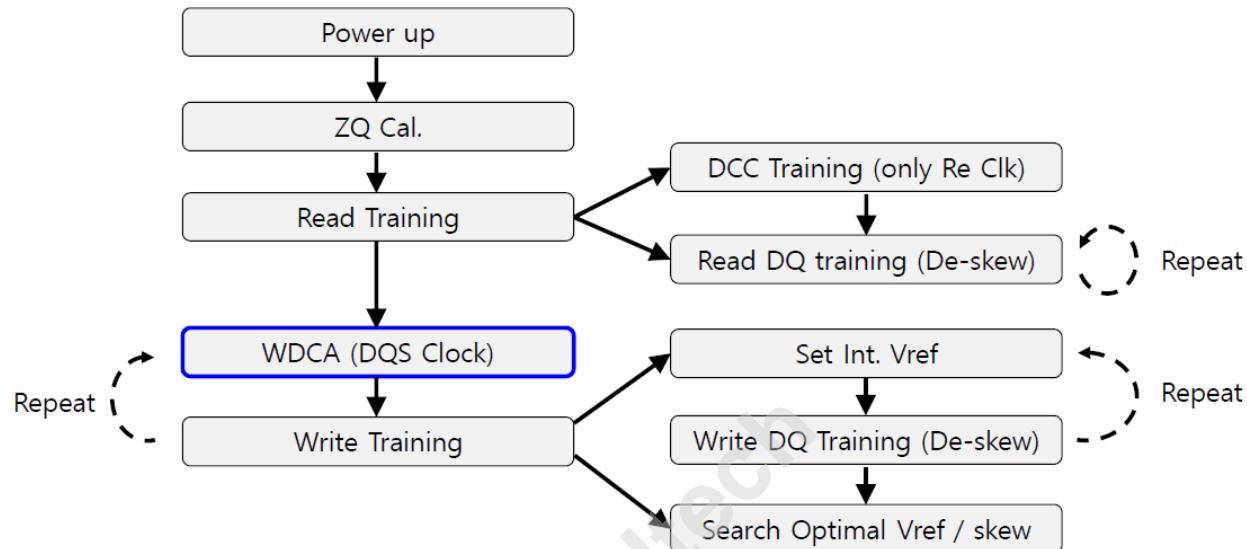


Figure 8.7-14 — Data Training Flow with WDCA

8.7.9 Write Training Monitor

With voltage and temperature changes on the system, there is a need for a method to monitor whether the last obtained optimum training settings are still sufficient to produce low error rates on the interface. A method to monitor sufficiency of the last obtained optimum settings is described in **Figure 8.7-15** and **Figure 8.7-16**.

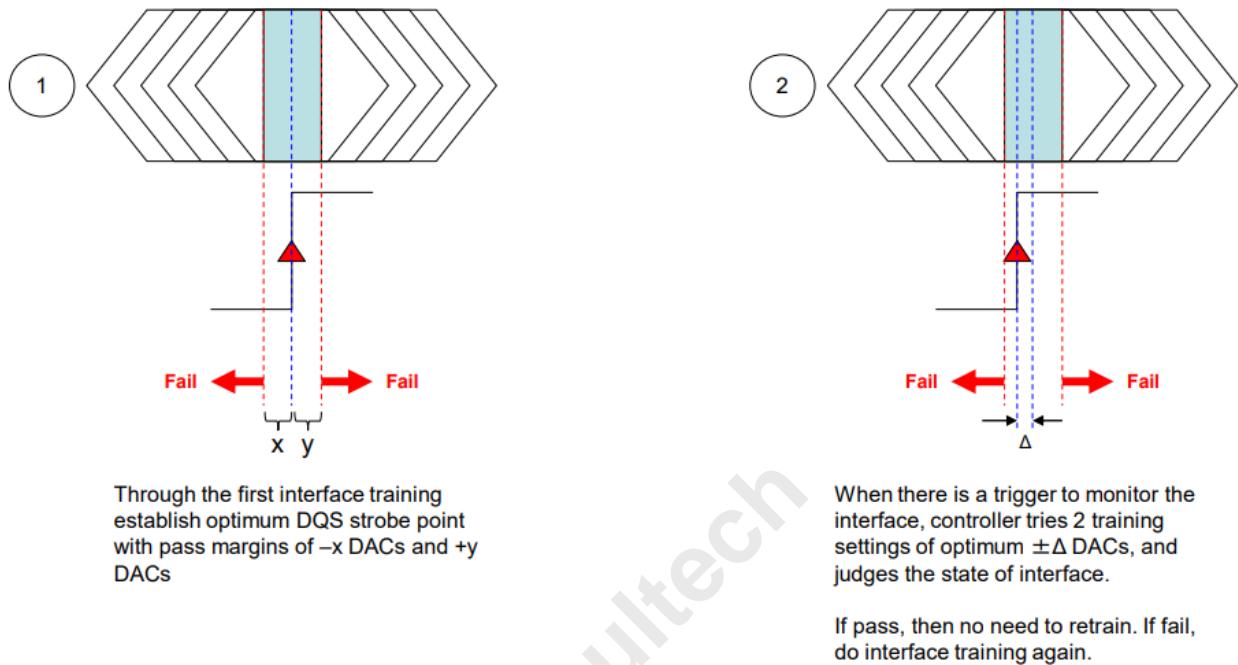


Figure 8.7-15 — Write Training Monitoring Method

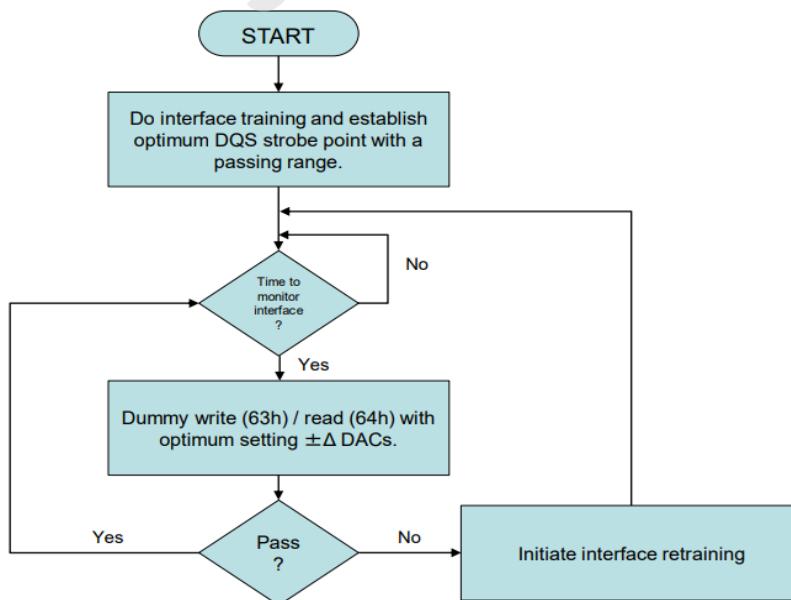


Figure 8.7-16 — Write Training Monitor Flowchart

8.7.10 Per-Pin VrefQ Adjustment

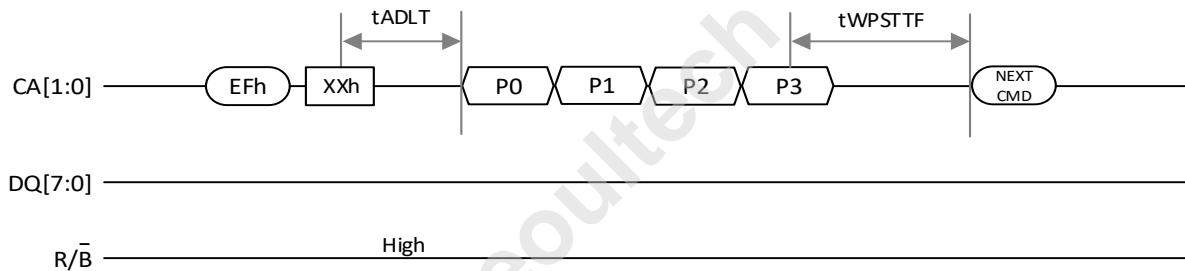
Per-pin VrefQ adjustment is the feature that allows NAND devices to compensate for pin-pin timing variation. Per-pin VrefQ adjustment may be implemented by NAND vendors in the way of Per-Pin VrefQ Adjustment via Offset.

With this implementation, the base NAND VrefQ setting is provided by FA23h while FA40h and FA41h provide the pin specific offset information. The final VrefQ setting for a pin is determined by the base setting from FA23h and the offset information from FA40h/41h.

8.7.11 Fast Set/Get Feature

Fast Set/Get Feature is an optional feature that reduces training time overhead related to configuring FA23h/FA24h during Internal VrefQ/WDCA training. The feature does not require a different command opcode but is automatically invoked when the controller issues a Set Features (EFh), Set Features for Each LUN (D5h), Get Features (EEh) or Get Features for Each LUN (D4h) command to specific feature address registers (FA23h / FA24h / FA27h / FA28h / FA40h / FA41h / FA26h (VSP)) on a NAND device which supports Fast Set/Get Feature.

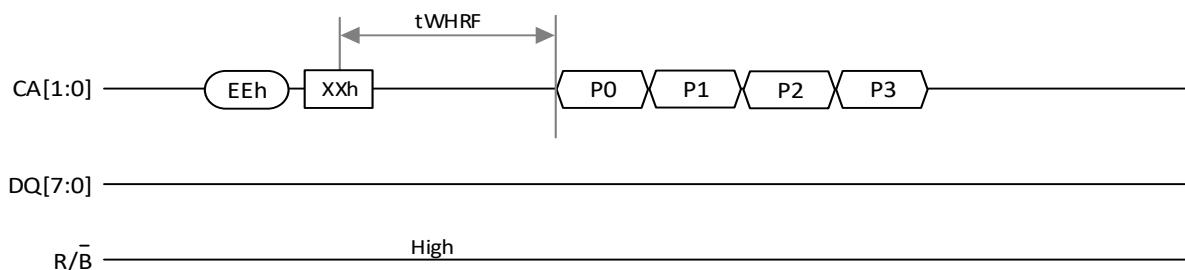
Figure 8.7-17 shows the Fast Set Feature command sequence using a Set Features (EFh) command:



NOTE 1 Fast Set Feature behavior may also be invoked by a Set Feature for Each LUN (D5h) command.

Figure 8.7-17 — Fast Set Feature Sequence with Set Features (EFh) Command

Figure 8.7-18 shows the Fast Get Feature command sequence using a Get Features (EEh) command:



NOTE 1 Fast Get Feature behavior may also be invoked by a Get Feature for Each LUN (D4h) command.

Figure 8.7-18 — Fast Set Feature Sequence with Get Features (EEh) Command

8.7.12 Decision Feedback Equalization (DFE)

NAND devices supporting higher data rates than 3200 MT/s require equalization to compensate channel characteristics and help improve Rx margin. Before write data burst operation, NAND devices with 1-tap DFE enabled require 2UI DQ pre-drive to 0. This pre-drive set pre-condition of DFE circuits. The write latency DQS cycle must be set accordingly if DFE pre-drive is enabled.

DFE coefficient and pre-drive conditions can be set via set feature command (FA27h). A 1-tap DFE is supported and a 4-tap DFE is optional with 4UI or 8UI (optional) DQ pre-drive to 0.

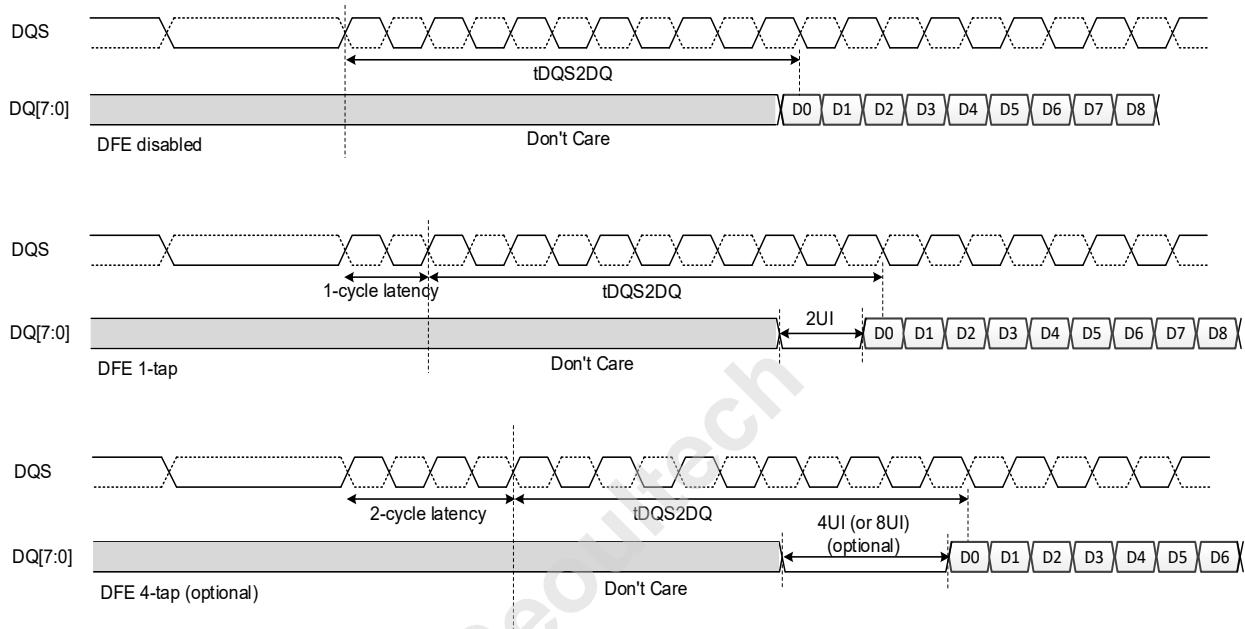


Figure 8.7-19 — DFE Pre-Drive Requirement For Data Input

The FA 27h P1[7:6] bits control the DQ output pre-drive from the NAND. DQ output pre-drive forces the NAND outputs to 0 for a specific number of UI. This is useful in cases where the controller supports DFE and requires the DQ signals to be pre-driven to 0 for DFE circuitry initialization. Prior to configuring the DFE DQ pre-drive settings for data output in FA 27h, the host must have first configured the number of warmup cycles for data output in FA02h to a setting that is greater than or equal to the number of output pre-drive cycles (1 warmup cycle = 2UI pre-drive). The **Figure 8.7-20** DQ signals are being pre-driven by the NAND to zero for 2UI and 4 UI cases.

8.7.12 Decision Feedback Equalization (DFE) (cont'd)

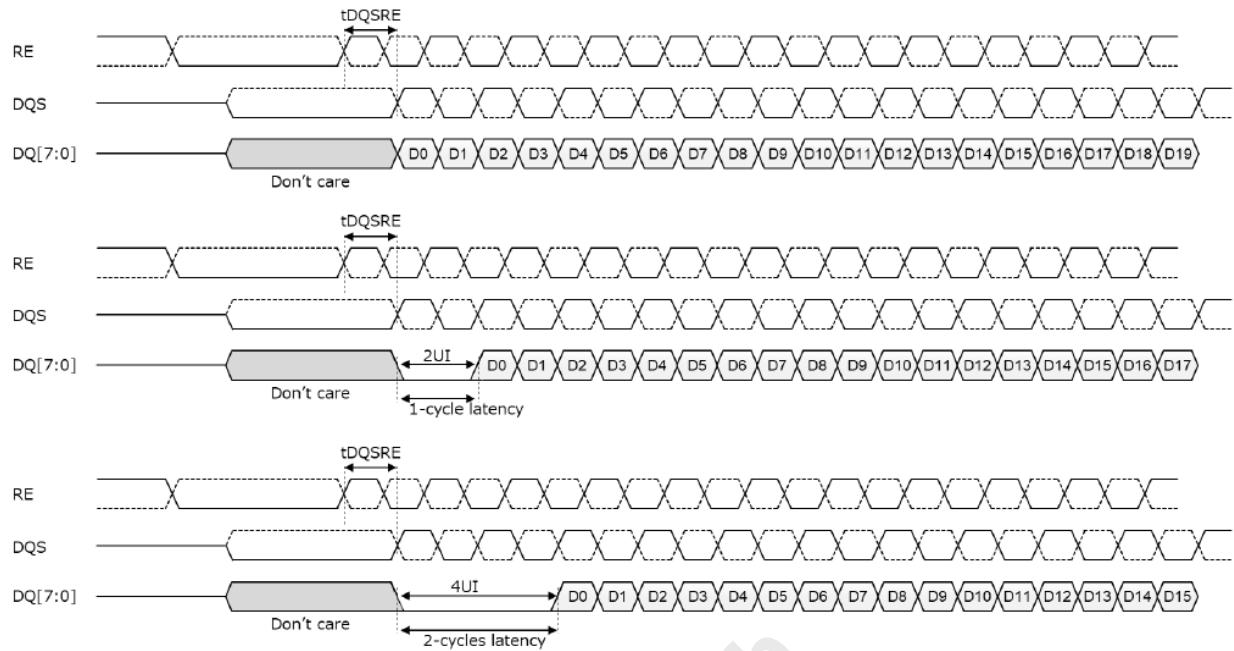


Figure 8.7-20 — DFE Pre-Drive Requirement For Data Output

8.7.13 DQS Oscillator

As voltage and temperature change on the NAND die, the DQS clock tree delay will shift and may require re-training. NAND device includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS oscillator count value reported by NAND device can be used by the memory controller to periodically train DQS to the DQ data valid window.

The DQS Oscillator is initiated using command 0Bh followed by LUN address (00h for single LUN, 01h for All LUN). Host shall wait time ($t_{OSC_{ready}}$) such that NAND internal DQS oscillator is ready and host cannot issue any command on the same CE during $t_{OSC_{ready}}$. The DQS oscillator can be started by issuing 00h address cycle, which will start an internal oscillator that counts the number of times a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator can be stopped by issuing 00h address cycle. When the DQS oscillator is stopped, the results of the oscillator counter are automatically stored in B0[7:0] and B1[7:0] of FA26h and host can read these values using get feature (FA26h). B0[7:0] contains the least significant bits (LSBs) of the result for t_{DQS2DQ} . B1[7:0] contains the most significant bits (MSBs) of the result for t_{DQS2DQ} . And next CMD can be issued after waiting oscillator completion time ($t_{OSCPOST}$). If a user issues any command other than 'Get feature or Get Feature by LUN' right after $t_{OSCPOST}$, the previous DQS oscillator counter result will be invalid because the voltage and temperature environment can be different between DQS oscillator and other operations.

During the DQS oscillator internal operation from start to stop address cycles, an interleaving operation except for FFh on the same CE_n/CA_CE_n is not allowed.

When user wants to perform DQS oscillator, the user should keep CE# 'Low' during DQS oscillator operation. If a NAND enters a low power standby state while DQS oscillator is operating, a NAND will stop operating the oscillator and the counter results stored in FA26h B0[7:0] and B1[7:0] are invalid and shall be ignored.

8.7.13 DQS Oscillator (cont'd)

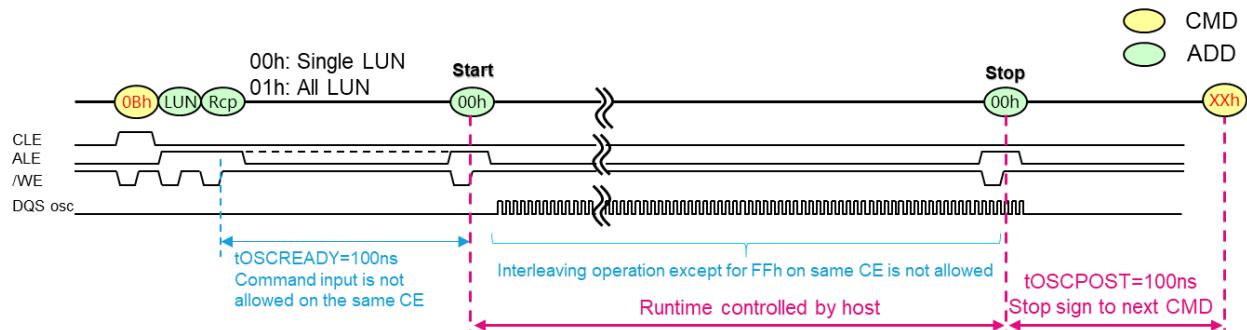


Figure 8.7-21 — DQS Oscillator Operation Sequence and Timing for Conventional Protocol

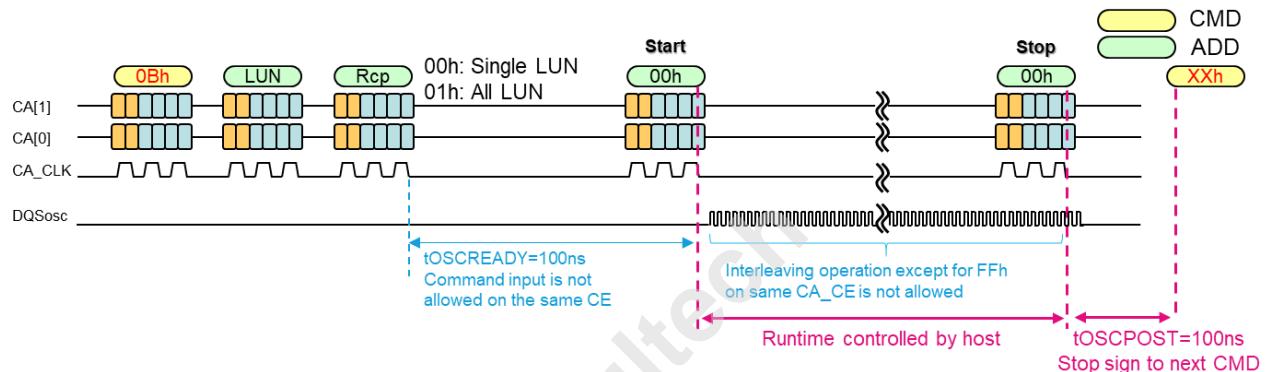


Figure 8.7-22 — DQS Oscillator Operation Sequence and Timing for SCA Protocol

Table 8.7-3 — DQS Oscillator Operation Mode

CMD	1 st Address cycle	2 nd Address cycle	DQS Oscillator Operation
0Bh	LUN address (XXh)	00h	Operation in the selected single LUN
0Bh	00h	01h	Operation in all LUN

Table 8.7-4 — tOSC_{ready} Specifications

Parameter	Symbol	Min	Max	Unit
Minimum time controller needs to provide during DQS Osc sequence, between Single LUN/All LUN address cycle to the 00h Start address cycle	tOSC _{ready}	100	-	ns

8.7.13 DQS Oscillator (cont'd)

The controller may adjust the accuracy of the result by running the DQS Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

- DQS oscillator granularity error = $2*t_{DQS2DQ} / \text{Runtime}$

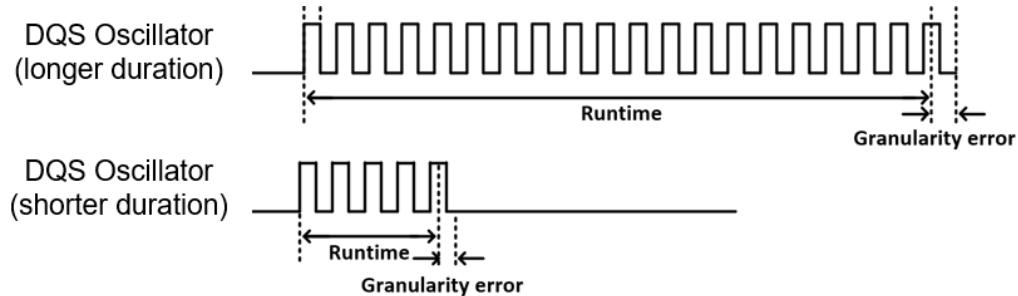


Figure 8.7-23 — DQS Oscillator Granularity Error

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. Therefore, the total accuracy of the DQS oscillator counter is given by the following equation:

- 'DQS Oscillator accuracy = $1 - \text{Granularity Error} - \text{Matching Error}$ '

The NAND flash DQS oscillator counter will count to its maximum value($=2^{16}-1= FFFFh$) and stop. The longest runtime for the oscillator that will not overflow the counter registers can be calculated as follows:

Longest t_{DQS2DQ} runtime interval = $2^{16} * [2*t_{DQS2DQ}(\min)] = 2^{16} * [2*100 \text{ ps}] = 13.1072 \mu\text{s}$.

Users should set DQS oscillator runtime below longest t_{DQS2DQ} runtime interval for the counter code not to be overflowed."

8.7.13.1 DQS Oscillator Matching Error

The DQS Oscillator matching error is defined as the difference between the DQS Oscillator circuit (t_{DQSosc}) and the actual DQS clock tree (t_{DQS2DQ}) across voltage and temperature.

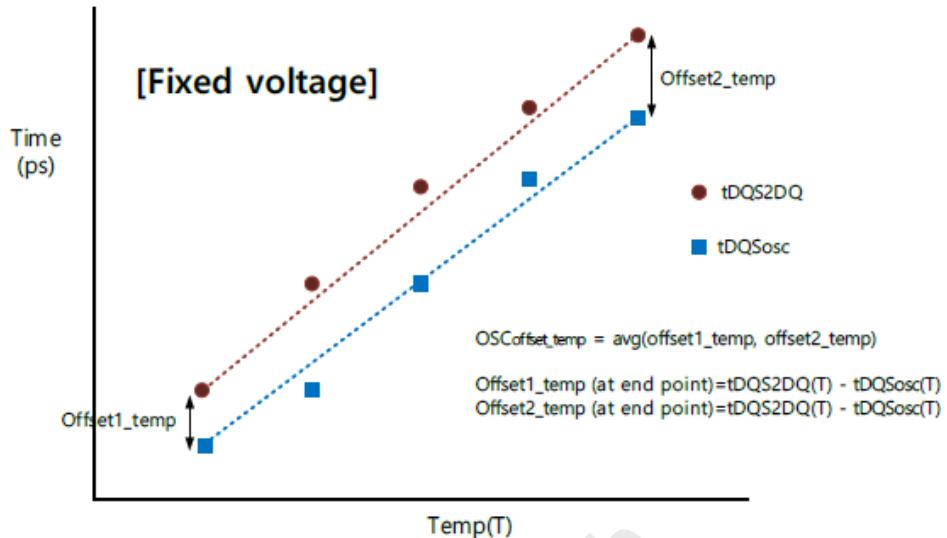


Figure 8.7-24 — DQS Oscillator Offset_temp

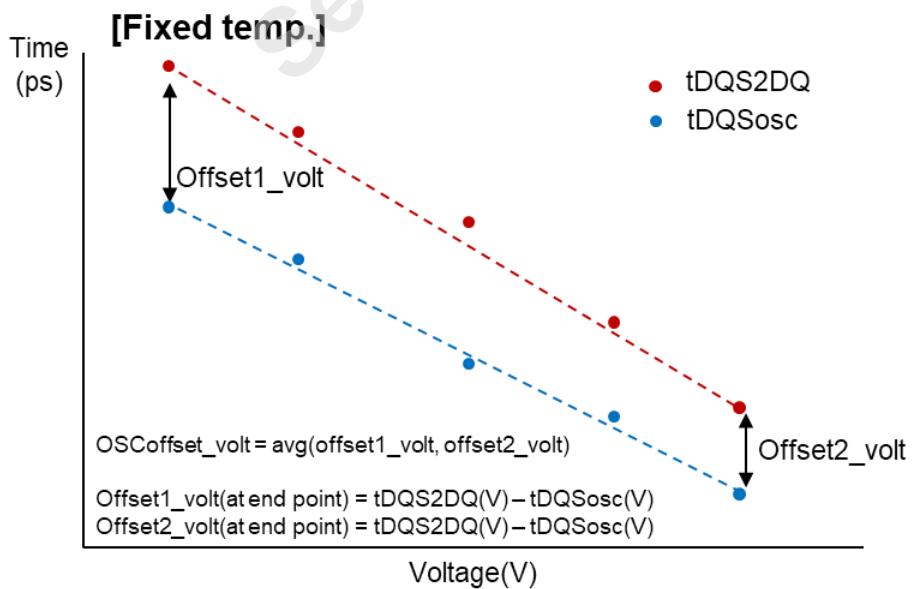


Figure 8.7-25 — DQS Oscillator Offset_volt

8.7.13.1 DQS Oscillator Matching Error (cont'd)

Table 8.7-5 — DQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Unit	Notes
DQS Oscillator Matching Error: voltage variation	OSC _{match_volt}	-25	25	ps	1, 2
DQS Oscillator Matching Error: temperature variation	OSC _{match_temp}	-25	25	ps	1, 2
DQS Oscillator Offset for voltage variation	OSC _{offset_volt}	-200	200	ps	2
DQS Oscillator Offset for temperature variation	OSC _{offset_temp}	-200	200	ps	2
NOTE 1	The OSC _{match} is the matching error between the actual DQS and DQS oscillator over voltage and temperature.				
NOTE 2	This parameter will be characterized or guaranteed by design				

8.8 Pausing Data Input/Output

The pausing of data output may be done in the middle of a data output burst by pausing RE_n (RE_t/RE_c) and holding the signal(s) static high or low until the data burst is resumed. The pausing of data input may also be done in the middle of a data input burst by pausing DQS (DQS_t/DQS_c) and holding the signal(s) static high or low until the data burst is resumed. The data burst can be considered paused if DQS (DQS_t/DQS_c) or RE_n (RE_t/RE_c) is paused such that the current I/O frequency is not maintained for the data burst. WE_n shall be held high during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause.

Pausing in the middle of a data input or data output burst is only allowed up to the 800 MT/s data rate. Above 800 MT/s, for signal integrity reasons, pausing in the middle of a data input or data output burst is not allowed, and if the data burst is interrupted, the host is required to exit first the data burst prior to resuming it.

A data burst is exited when any of ALE, CLE or CE_n is driven to 1. After a data burst has been exited, if warmup cycles are enabled, then warmup cycles are required when re-starting the data burst.

Refer to vendor datasheet for details on re-issuing warmup cycles when exiting and re-starting data bursts. After a data burst has been exited, ODT also may be disabled, however, if needed to meet the signal integrity needs of the system, ODT must be re-enabled prior to re-starting the data burst. If the host desires to end the data burst, after exiting the data burst, a new command is issued.

Figure 8.8-1 is an example of exiting a data input burst with a CLE=1 and resuming the data input burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data input burst is resumed.

8.8 Pausing Data Input/Output (cont'd)

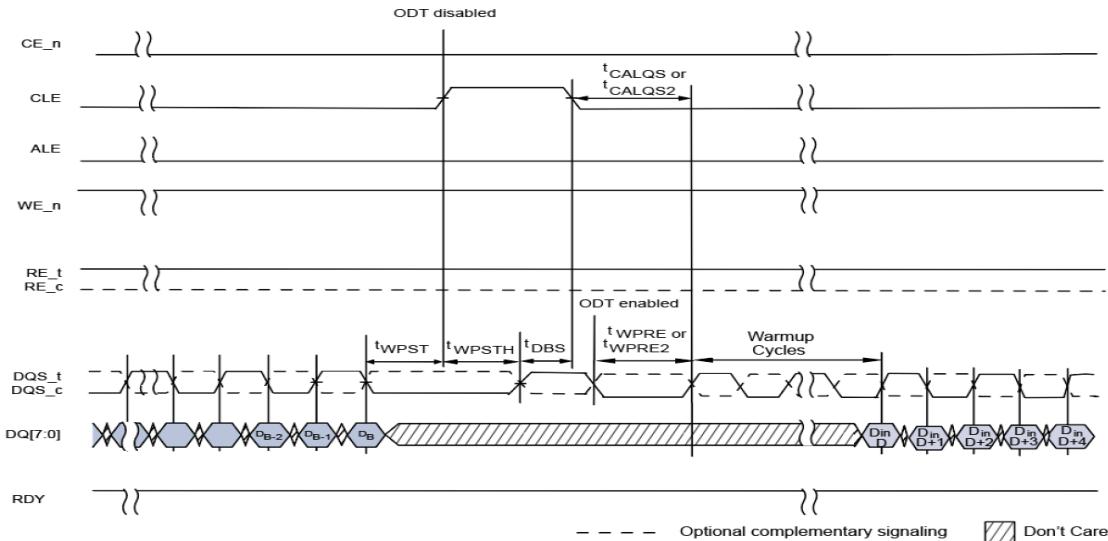


Figure 8.8-1 — Example of Data Input Burst Exit with CLE=1 and Resume with CLE=0

Figure 8.8-2 is an example of exiting a data output burst with a CLE=1 and resuming the data output burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data output burst is resumed.

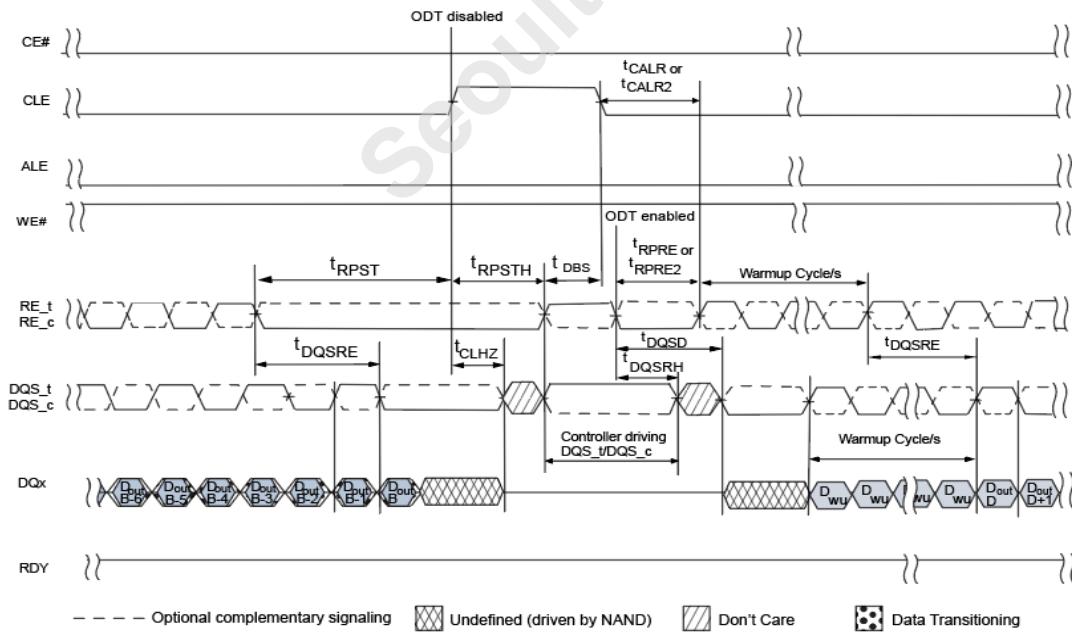
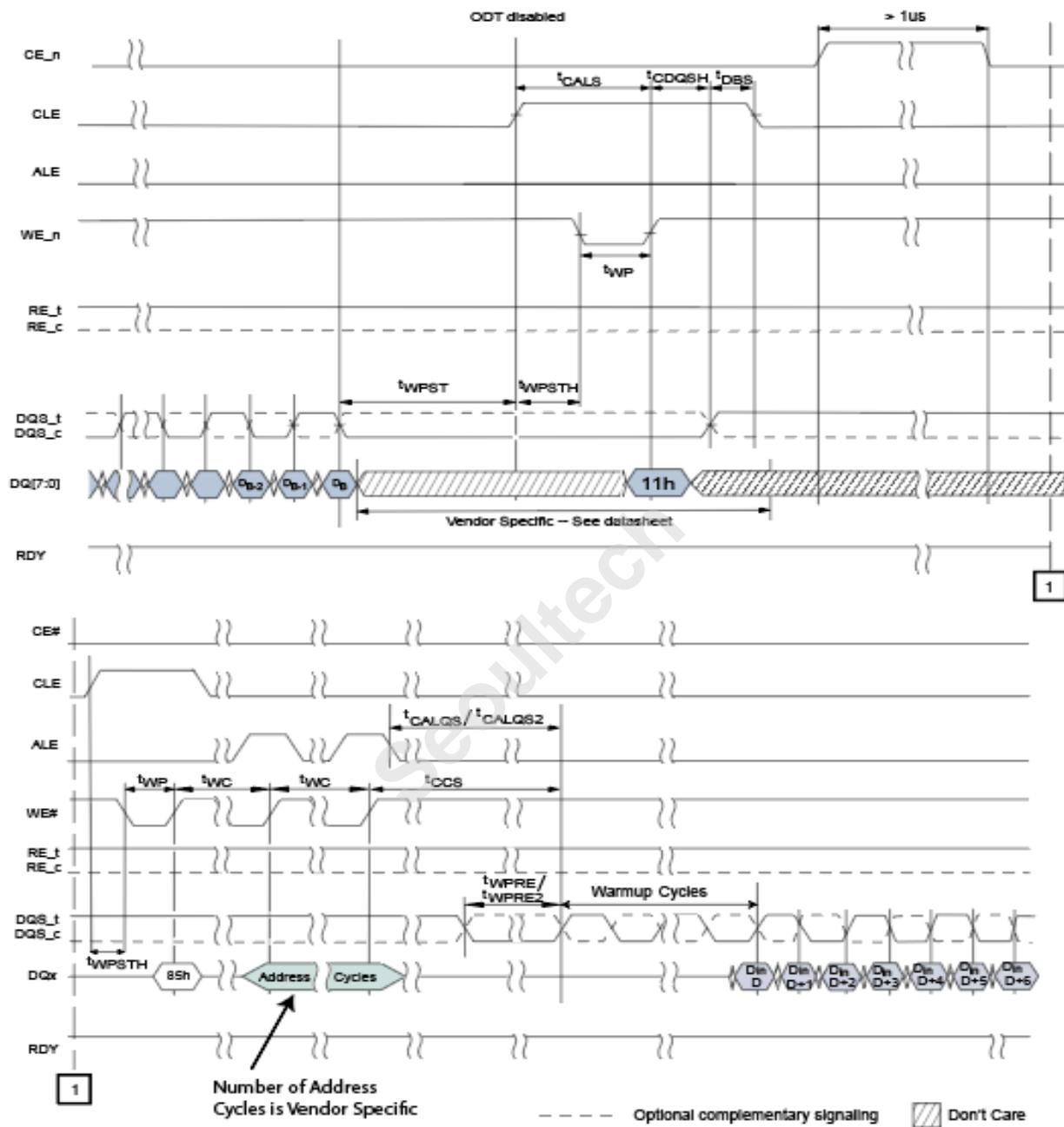


Figure 8.8-2 — Example of Data Output Burst Exit with CLE=1 and Resume with CLE=0

For devices that support >800 MT/s, if the input burst is exited and CE_n is brought high for >1 μ s, the host may be required to issue vendor specific command (e.g., 11h) to exit and end the data burst (see vendor datasheet). To restart the exited data input burst, a Change Write Column command shall be issued. For devices that support >800 MT/s, to restart an exited data output burst when CE_n has been high for >1 μ s, a Change Read Column command shall be issued.

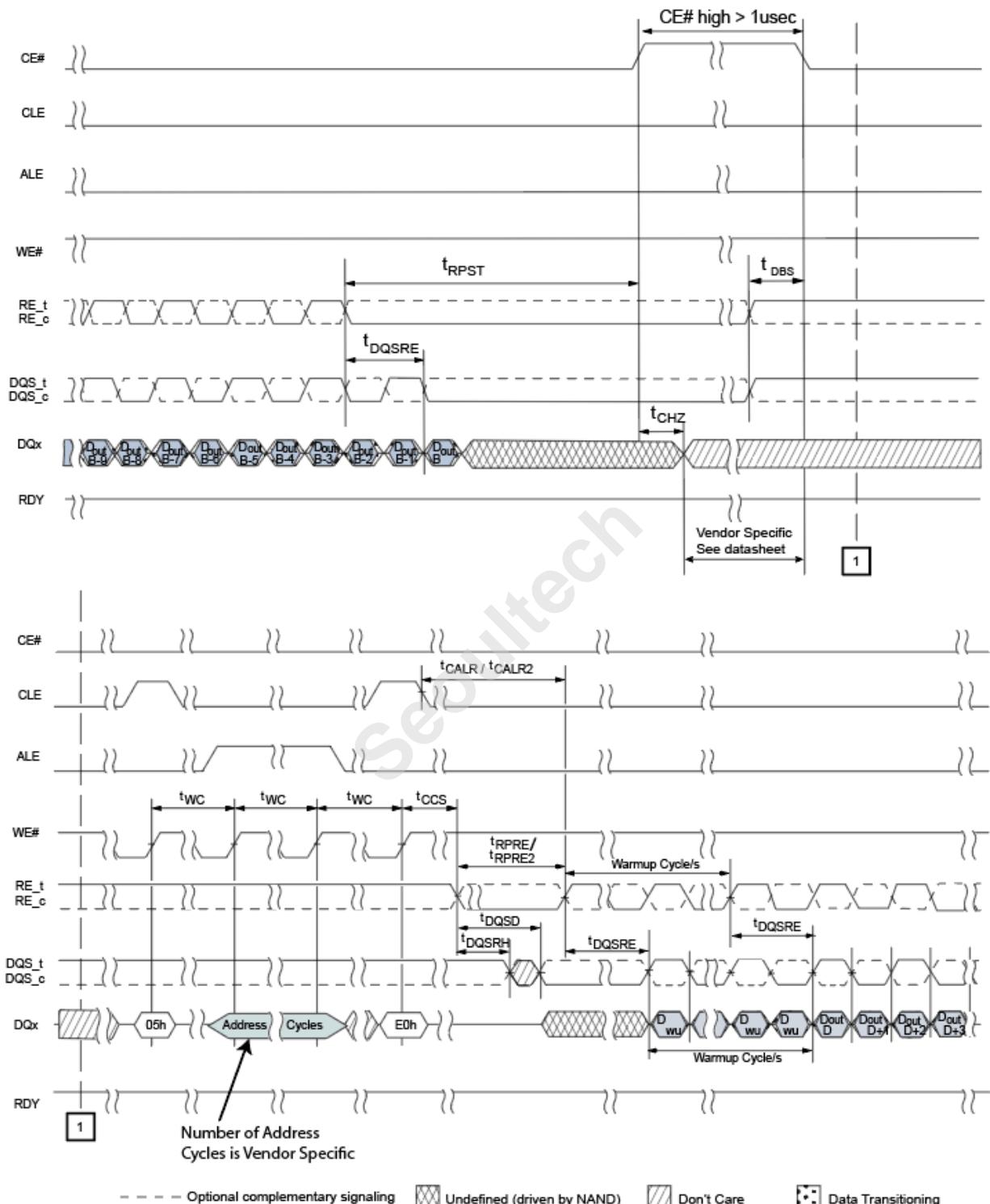
8.8 Pausing Data Input/Output (cont'd)



NOTE 1 Over 1 μ s CE_n High case, DQS_t, and DQS_c states after data burst are optional. See vendor datasheet.

Figure 8.8-3 — Example of Data Input Exit With CE_n High >1 μ s for Devices Supporting >800 MT/s

8.8 Pausing Data Input/Output (cont'd)



NOTE 1 Over 1 μ s CE_n High case, RE_t, and RE_c states after data burst are optional. See vendor datasheet.

Figure 8.8-4 — Example of Data Output Exit With CE_n High >1 μ s for Devices Supporting >800 MT/s

8.9 Data Bus Inversion (DBI) Purpose and Function

Data Bus Inversion (DBI) is an optional function for NAND device to reduce power consumption and power/bus noise during data input/output. The device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not.

DBI signal through DBI pin shall be synchronized with DQ signals. DBI is regarded as DQ, such that specifications such as AC parameters and Interface training shall be applied to DBI.

DBI signal shall be either 0 or 1 during data input/output, where 0 indicates the DQ signals in the same cycle are not inverted and 1 indicates the DQ signals in the same cycle are inverted. In the case where NAND device output DQ with DBI, the device shall invert DQ signal with setting DBI to 1 if the number of 1's of DQ signals is more than 4. Otherwise, if the number of 1's is equal to or less than 4, the device shall not invert DQ signal with setting DBI to 0.

DBI function shall be activated/deactivated by Set Feature.

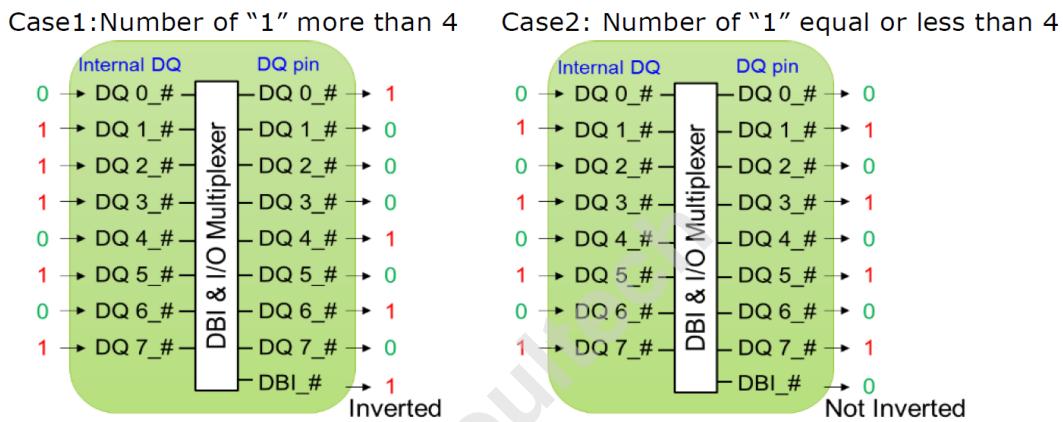


Figure 8.9-1 — DBI Function Illustration

8.9.1 DBI Behavior During Different Modes of Operation

Table 8.9-1 shows the NAND DBI encoding behavior on the DQ[7:0] pins and the DBI pin behavior in different modes of operation when DBI is enabled.

Table 8.9-1 — DBI Encoding of DQ[7:0] and DBI Pin Behavior During Different Modes of Operation

Mode of Operation	DQ[7:0] Behavior (With or Without DBI Encoding)	DBI Pin Behavior (Encoding flag/9th DQ pin/ "0")
Command/address	Without DBI encoding	"0"
Data Input	With DBI encoding	Encoding flag
Data Output	With DBI encoding	Encoding flag
SET Feature/ GET Feature/ Read ID/ Read Status	Without DBI encoding	"0"
Write DQ Training (Tx side)	Without DBI encoding	9th DQ pin
Read DQ Training	Without DBI encoding	9th DQ pin

8.9.2 DBI Behavior During Write DQ Training (Tx Side)

The host shall recognize the Write DQ Training (Tx Side) data size of the NAND by GET Feature to Feature Address 20h B2[3:0] and shall input and output data during Write DQ Training (Tx Side) based on that information.

With DBI enabled during Write DQ Training (Tx Side), the DBI pin acts like a 9th DQ pin and the data on DQ[7:0] are not affected by the values on the DBI pin and vice-versa. If the data that was input to the LUN during a 63h command sequence for example was the one shown in **Table 8.9-2**, then if the LUN successfully captured the data, the same data pattern will be output by the LUN on the DQ[7:0] and DBI pins during the 64h command sequence.

Table 8.9-2 — Write DQ Training (Tx side) Example with DBI

Pin	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
DQ7	1	1	1	0	0	0	1	1
DQ6	0	1	1	1	1	0	1	0
DQ5	1	0	0	1	1	0	0	1
DQ4	1	1	0	1	0	1	0	1
DQ3	1	0	1	0	1	0	1	0
DQ2	1	0	0	0	0	1	1	1
DQ1	0	0	1	1	0	0	1	0
DQ0	0	0	0	0	0	1	0	0
DBI	0	1	0	1	1	0	1	1

8.9.3 DBI Behavior During Read DQ Training

With DBI enabled during Read DQ Training, the DBI pin outputs data in a similar fashion as a DQ pin with an Inverse Mask value of “0”. The example in **Table 8.9-3** illustrates this behavior:

Table 8.9-3 — Read DQ Training Example with DBI

Pin	Order	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		1 st Pattern = 1Fh								2 nd Pattern = 7Fh							
	Inverse Mask	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ7	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ6	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ5	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ4	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ3	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ2	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DBI	**	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0

NOTE ** The inverse mask does not apply to the DBI pin. The DBI pin outputs data in a similar fashion as a DQ pin with an Inverse Mask value of “0”.

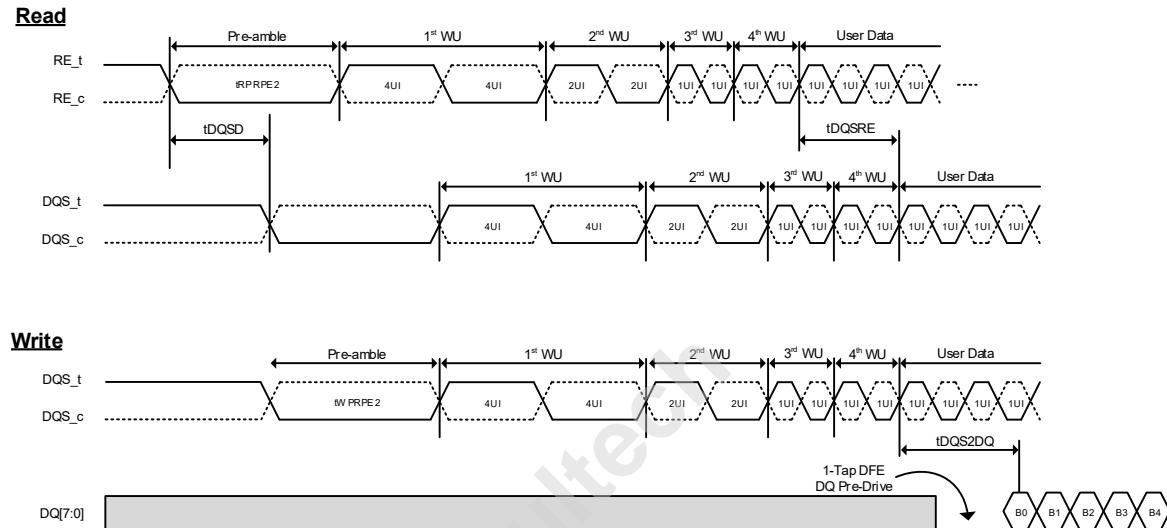
8.10 Progressive Warmup Cycle

As data rates increase, it becomes increasingly difficult to guarantee the correct number of differential signal toggles if the channel is not progressively warmed up.

Incorrect detection of number differential signal toggles can result in missing initial byte/s of data and data burst misalignment.

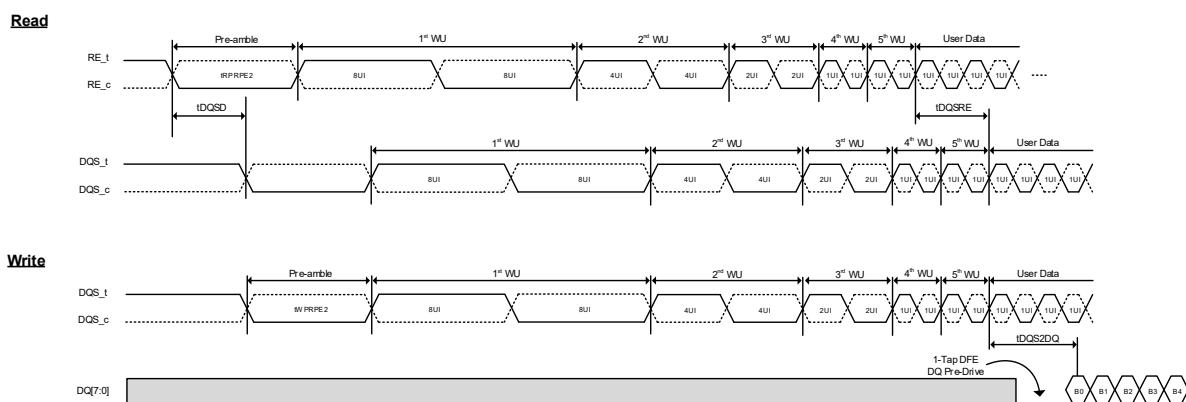
It is recommended (but optional) for the host to issue progressive warmup cycle timings at >3600 MT/s.

Examples of progressive warmup cycle schemes are explained in **Figure 8.10-1** and **Figure 8.10-2**.



NOTE WU=Warmup cycle.

Figure 8.10-1 — 4-2-1-1 Progressive Warmup Cycle for Read/Write Example (Recommended)



NOTE WU=Warmup cycle.

Figure 8.10-2 — 8-4-2-1 Progressive Warmup Cycle for Read/Write Example

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8.10 Progressive Warmup Cycle (cont'd)

Table 8.10-1 — Progressive Warmup Cycle Pattern According to Number of Warmup Cycles

$\leq 3.6 \text{ Gbps}$			$> 3.6 \text{ Gbps}$		
1 cycle	2 cycle	4cycle	1 cycle	2 cycle	4cycle
1UI	1UI x2	1UI x4	2UI ⁽¹⁾ or 1UI	2UI-1UI ⁽¹⁾ or 1UI x2	4-2-1-1 UI ⁽¹⁾ or 8-4-2-1 UI or 1UI x4
NOTE 1 Recommended					

9 Low Latency NAND

9.1 Low Latency NAND Overview

Low Latency NAND is NAND flash memory with faster random access time (t_R). Low Latency NAND has three classes defined by random access time.

9.2 Low Latency NAND Parameter Table

Table 9.2-1 — Low Latency NAND Parameter Table

Category	Item	Unit	Low Latency NAND										
			Class A	Class B	Class C								
Power	Vcc	V	3.3 V or 2.5 V										
	VccQ	V	1.2 V										
	Vpp	V	12 V (Optional)										
Organization	# of Plane	EA	32P or 16P or 8P										
	Page Size	KB	4 KB or 2 KB										
Performance	Page Read Time	μs (Avg.)	3 μs	5 μs	7 μs								
	Page Program Time	μs (Avg.)	100 μs	100 μs	300 μs								
	Block Erase Time	ms (Avg.)	5 ms	5 ms	5 ms								
Interface	JEDEC Link	-	JESD230 (Low Latency NAND supports IO speed defined in JESD230)										
	Wide IO	-	X8										
Package	Low Latency NAND supports all packages which are defined in JESD230 specification (132BGA / 152BGA / 168BGA / 316BGA and so on)												
NOTE 1 There are three grades for Low Latency NAND according to read time: 3 μs page read time for Class A, 5 μs page read time for Class B, and 7 μs page read time for Class C													
NOTE 2 Low Latency NAND supports IO speed defined in JESD230													

10 SCA Protocol

10.1 SCA Protocol Introduction

With increasing data transfer rates on the NAND interface, the command/address transfer time has not improved accordingly. To address this problem, the Separate Command Address (SCA) protocol has been defined. Compared to the legacy conventional (Conv.) protocol, the SCA protocol separates command/address (CA) and data busses, allowing concurrent command/address (CA) and data traffic, improving NAND interface efficiency.

10.2 SCA Versus Conv. Protocol Comparison Summary Table

Table 10.2-1 — SCA versus Conv. Protocol Comparison Summary Table

Description	Conv. Protocol	SCA Protocol
NAND Pins	<ul style="list-style-type: none">• ALE, CE#, CLE, WE#• Pins above are input-only	<ul style="list-style-type: none">• CA[0], CA_CE#, CA[1], CA_CLK• SCA• CA_CE#, CA_CLK and SCA pins are input-only while CA[1:0] are bi-directional
Pin signaling	HSUL	HSUL
CA bus input protocol	SDR	DDR
CA bus input pins used	DQ[7:0] (CA bus same as DQ bus)	CA[1:0]
CA bus input cycle time	10 ns (t _{WC} min)	4 ns (t _{CACI} min) ¹
CA bus input header cycles	None	1
CA bus output protocol	SDR	Sync DDR
CA bus output pins used	DQ[7:0] (CA bus same as DQ bus)	CA[1:0]
CA bus output cycle time	Variable (prior to data training DQ bus traffic must be at slow data rate, after data training, traffic may occur at faster data rate)	10 ns (t _{CACO} min)
DQ bus pins for data	DQ[7:0]	DQ[7:0]
DQ bus control	CE#	Command packets (SCE/SCP/SCT/NTO)
Protocol enable/disable	Conv. protocol enabled by default on legacy NAND devices that only support Conv. protocol	Value of SCA pad on NAND die / SCA balls on the raw NAND package on power-up determine whether Conv. or SCA protocol enabled
Program Command Sequence	80h-Addr-12h-SCE-DIN-SCT-LUNSel(opt)-10h-tPROG	80h-Addr-12h-SCE-DIN-SCT-LUNSel(opt)-10h-tPROG
Non-target ODT Scheme	ODT# (nWP) pin, Matrix ODT	Non-Target ODT (NTO) Packet

NOTE 1 Signal integrity analysis required to determine if minimum tCACI may be used on the system.

10.3 SCA Versus Conv. Protocol Signals

When the SCA protocol is enabled, several signals on the NAND interface change functionality and/or signal name.

Figure 10.3-1 shows the signal differences between the Conv. and SCA protocols at the NAND die (LUN) level:

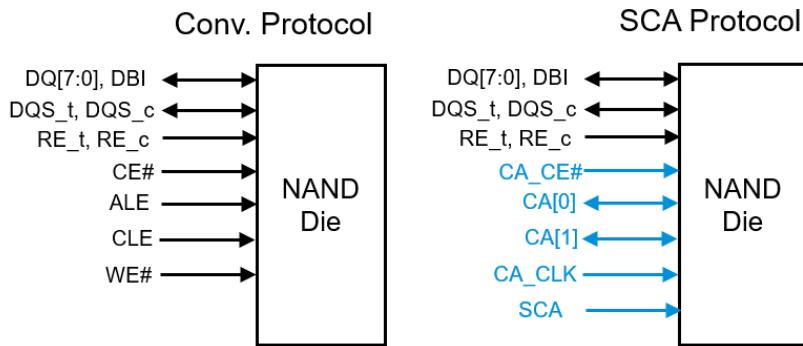


Figure 10.3-1 — SCA Versus Conv. Protocol Signals – NAND Die Level

The CE# signal in the Conv. protocol is renamed as CA_CE# in the SCA protocol to better reflect its SCA function. The WE# signal in the Conv. protocol is renamed as CA_CLK in the SCA protocol to better reflect its SCA function. The input-only ALE signal in the Conv. protocol becomes the bi-directional CA[0] signal in the SCA protocol, while the input-only CLE signal in the Conv. protocol becomes the bi-directional CA[1] signal in the SCA protocol.

Figure 10.3-2 shows the signal differences between the Conv. protocol versus the SCA protocol at the NAND package level using a 2-CH ODP NAND package with 4 CE# (2 CE# per package channel) as an example. As can be seen in this example, at the NAND package level, with the SCA protocol enabled, there can be multiple CA_CE# signals for each package channel. Note: NAND packages may vary in number of channels per package and number of CE#s per package. Also, SCA_0 and SCA_1 signals may be unconnected to each other at the package level as shown in **Figure 10.3-2**, or connected to each other at the package level (not shown in **Figure 10.3-2**).

10.3 SCA Versus Conv. Protocol Signals (cont'd)

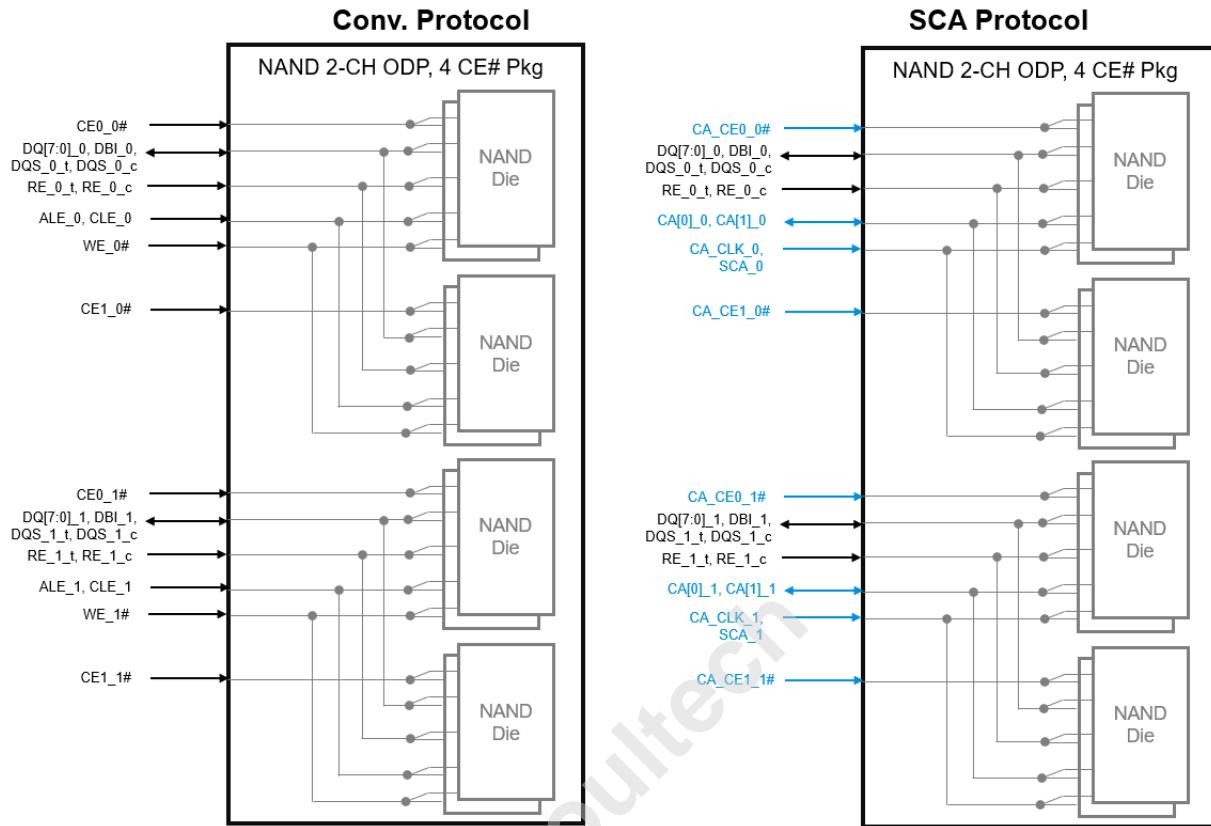


Figure 10.3-2 — SCA versus Conv. Protocol Signals – NAND Package Level

10.4 SCA Protocol CA Bus and DQ Bus Definition and Control

When the SCA protocol is enabled, the term “CA Bus” shall collectively refer to the CA[1:0] and CA_CLK signals and the term “DQ Bus” shall collectively refer to the DQ[7:0], DBI, DQS_t, DQS_c, RE_t, and RE_c signals.

In contrast to the Conv. protocol where the DQ, DQS, RE, and DBI signals and control signals (ALE, CLE, WE#) are all enabled/disabled using the CE# signal, in the SCA protocol the CA_CE# signal only enables/disables the CA bus for the LUNs connected to that CA_CE#, while the DQ bus for those LUNs are enabled/disabled via packets on the CA bus. The difference in DQ bus control between Conv. and SCA protocols is illustrated in **Figure 10.4-1**.

10.4 SCA Protocol CA Bus and DQ Bus Definition and Control (cont'd)

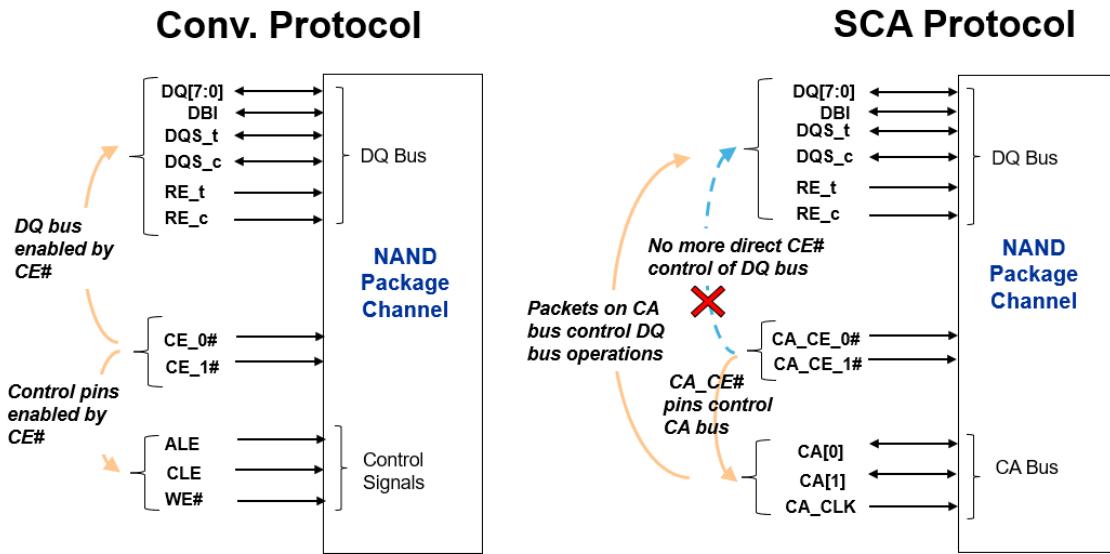


Figure 10.4-1 — Conv. Versus SCA Protocol Control of Control Pins/CA Bus and DQ Bus

10.5 SCA Protocol Enable/Disable

The SCA or Conv. protocol is enabled based on the connection of the SCA pad/SCA balls at power-up. **Table 10.5-1** shows the protocol that is enabled versus the SCA pad/ball connection:

Table 10.5-1 — CA Protocol Versus SCA Pad/Ball Connection

Protocol Enabled	SCA Pad/SCA Ball Connection
Conv. Protocol (optional)	Vss or Float
SCA Protocol	VccQ

See SCA Package Balls clause for the location of SCA balls on the different NAND packages. When there are multiple SCA balls on a package, all SCA balls must have the same connection (i.e., all Vss, all Float, or all VccQ).

10.6 SCA Protocol Power-up Considerations

When the SCA protocol is enabled, the WE# signal becomes the CA_CLK signal. The WE# signal in the Conv. protocol is default HIGH while the CA_CLK signal in the SCA protocol is default LOW. Thus, when powering-up with the SCA protocol enabled, special consideration is needed to initialize the CA_CLK signal LOW prior to asserting CA_CE# LOW.

CA_CLK may be powered-up LOW (see **Figure 10.6-1 Case1**). However, if CA_CLK is powered-up HIGH (see **Figure 10.6-1 Case 2**), CA_CLK must be driven LOW t_{WLCEL_CA} prior to the first CA_CE# LOW toggle after power-up.

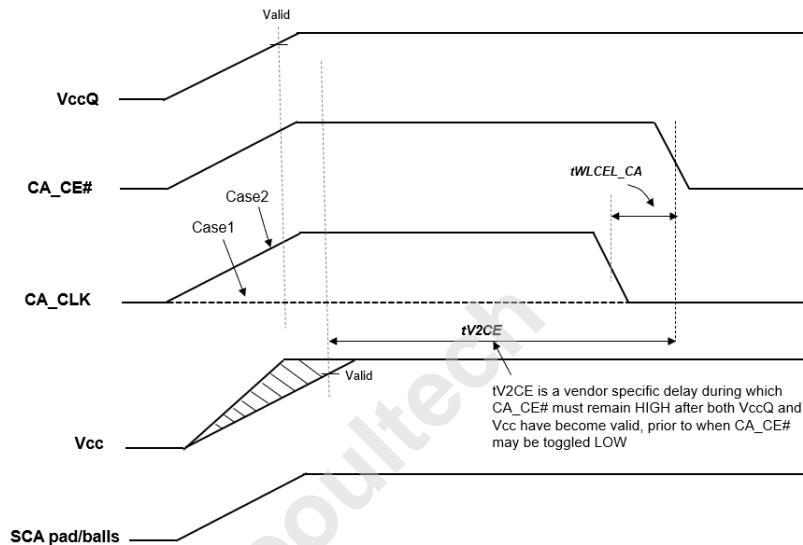


Figure 10.6-1 — SCA Protocol Power-up CA_CLK and CA_CE# Considerations

10.7 SCA Packets and Packet Structure

Communication between the host and the NAND on the CA bus is done via packets. There are 3 CA packet structures defined in the SCA protocol:

- CA input packet structure
- CA output packet structure with single-byte output format
- CA output packet structure with multi-byte output format (optional for NAND vendors to support)

10.7.1 CA Input Packet Structure

CA input packets are used to communicate command, address, and other information from the host to the NAND. The structure of CA input packets is shown in **Figure 10.7-1**.

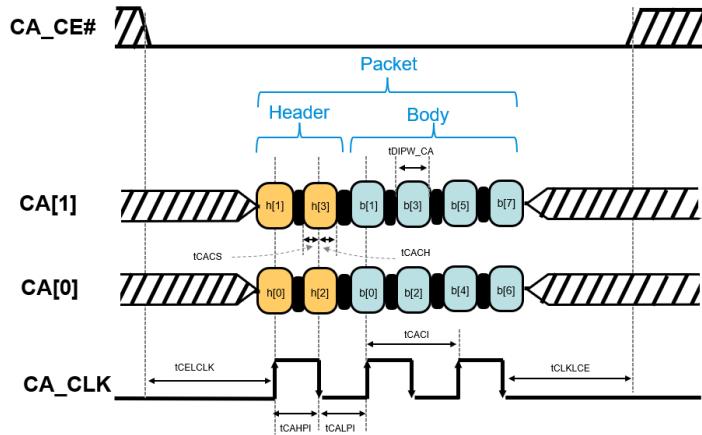


Figure 10.7-1 — SCA CA Input Packet Structure

Each CA input packet begins with 4 bits of header information. The header allows the NAND to distinguish between different CA input packet types. See the SCA Header Definition clause for the different packet types.

After the 4-bit header, 8 bits of packet body follows. The information in the packet body depends on the CA input packet type. A command packet for example contains command opcodes in the body while an address packet contains address information.

10.7.2 CA Output Packet Structure with Single Byte Output Format (Default)

CA output packets are used to communicate information from the NAND to the host. There are 2 CA output packet formats in the SCA protocol: single-byte output format and multi-byte output format. NAND vendor support for single-byte output format is mandatory, while NAND vendor support for multi-byte output format is optional.

The CA output packet format in NAND devices is controlled by the optional SCA_OUT bit in FA 02h B3[0]. **Table 7.1-1** shows NAND FA 02h register definition:

10.7.2 CA Output Packet Structure with Single Byte Output Format (Default) (cont'd)

The single-byte output format is the power-on default format for NAND devices.

The single-byte output format is shown in **Figure 10.7-2**.

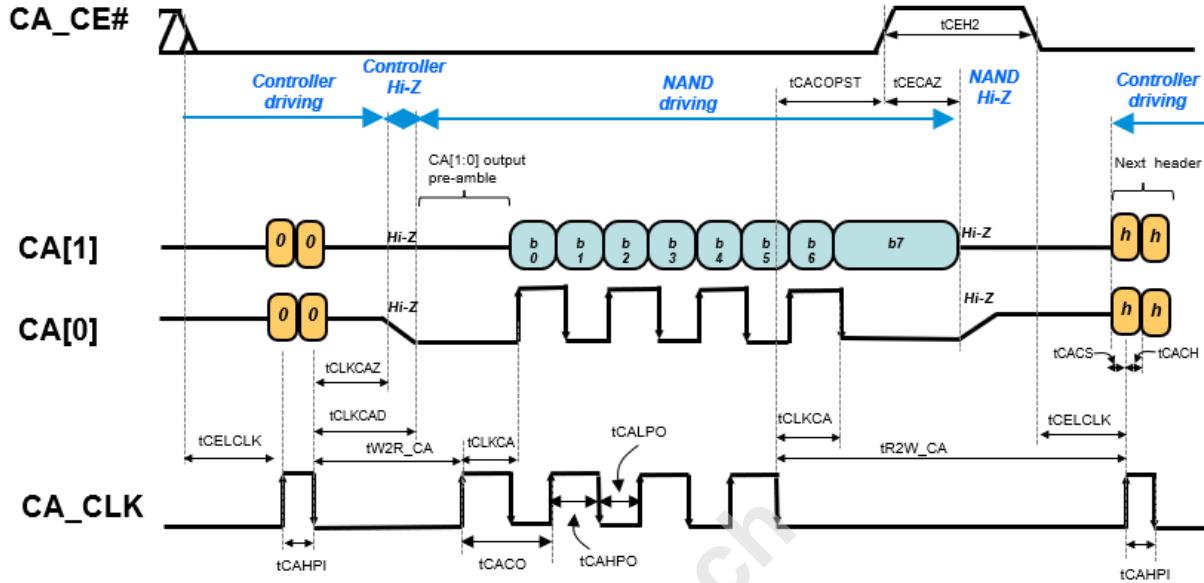


Figure 10.7-2 — SCA CA Output Packet with Single-Byte Output Format Structure

The CA output packet begins with the host inputting the CA output header to the NAND, this puts the NAND in CA output mode. After inputting the header, the host shall then Hi-Z the CA[1:0] signals by tCLKCAZ. The NAND then starts driving CA[1:0] with “00b” pre-preamble data after tCLKCAD. After W2R_CA, the host toggles CA_CLK which produces a bit of output on CA[1] and the corresponding toggle on the CA[0] signal (which acts as a strobe signal during CA output mode). The host toggles CA_CLK until a byte of information has been outputted. To make the NAND exit CA output mode, the host toggles CA_CE# high, after which the NAND shall Hi-Z the CA[1:0] signals by tCECAZ. The controller may then drive CA[1:0] again after tCECAZ has elapsed to issue the next header.

10.7.2 CA Output Packet Structure with Single Byte Output Format (Default) (cont'd)

For command sequences that produce multiple bytes of output on the CA bus (i.e., Get Feature, Get Feature by LUN, Read ID), when the single-byte output format is enabled, a CA output header from the controller is required for every byte of output from the NAND. This is shown in the following Get Feature (EEh) sequence example (**Figure 10.7-3**), where multiple CA output headers are needed to output the 4 bytes of register information:

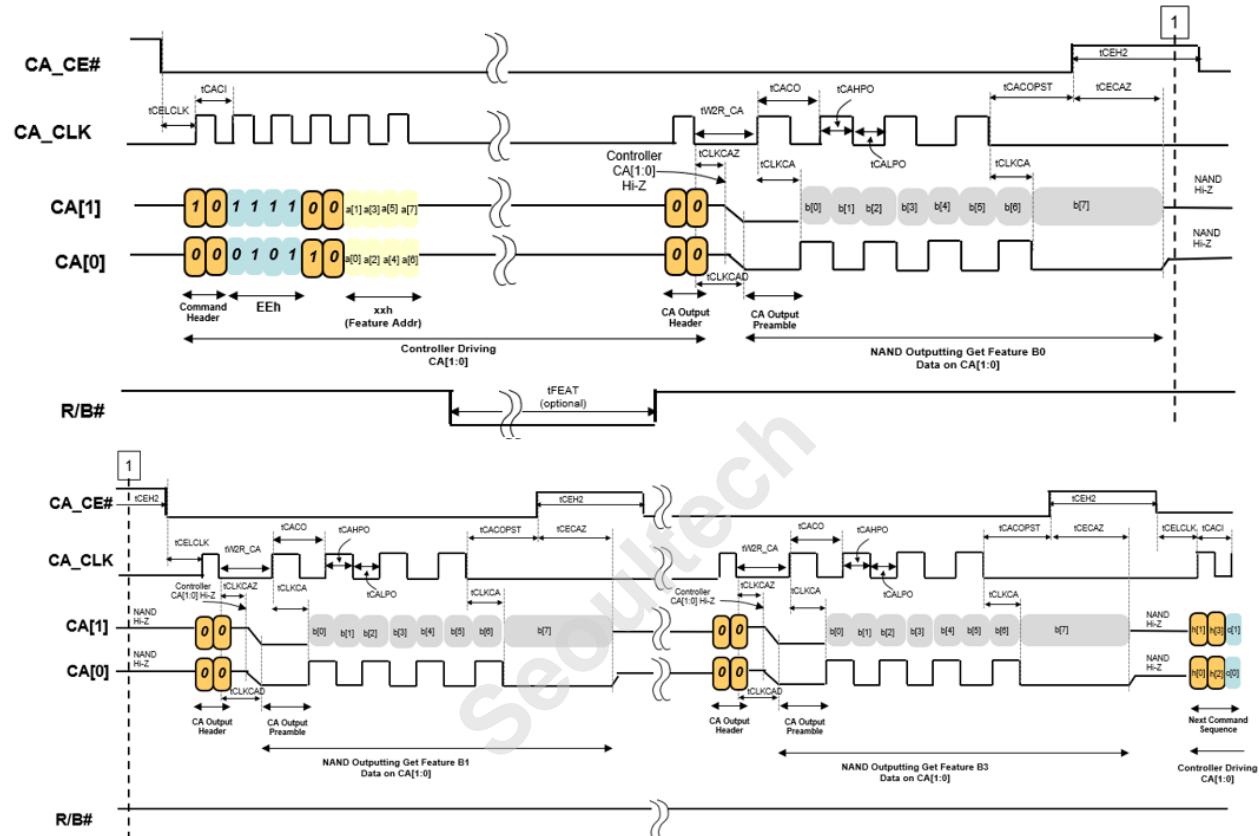


Figure 10.7-3 — Get Feature (EEh) with Single-Byte CA Output Packet Format

10.7.3 CA Output Packet Structure with Multi-Byte Output Format (Optional for NAND Vendors to Support)

When the multi-byte CA output packet format is enabled (SCA_OUT = 1), during command sequences that produce multiple bytes of output from the NAND on the CA bus, the NAND outputs multiple bytes of data on the CA bus with just a single header issuance from the controller. This is shown in the Get Feature (EEh) sequence in **Figure 10.7-4**.

10.7.3 CA Output Packet Structure with Multi-Byte Output Format (Optional for NAND Vendors to Support) (cont'd)

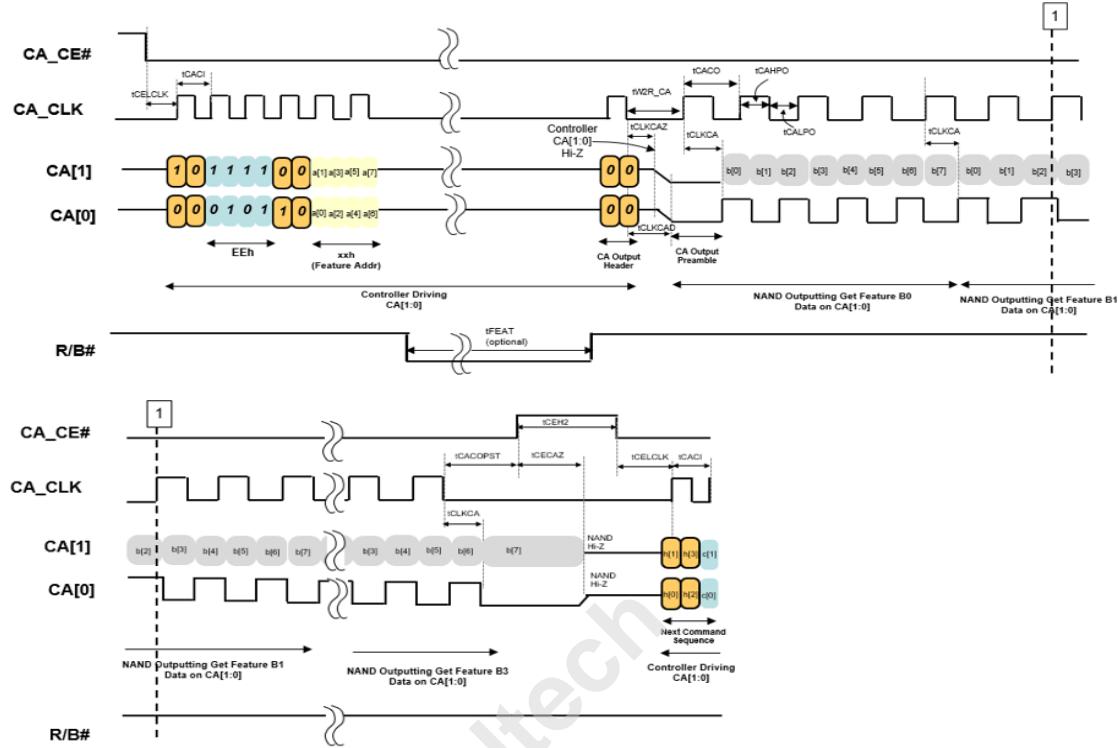


Figure 10.7-4 — Get Feature (EEh) with Multi-Byte CA Output Packet Format

Thus, for command sequences with multiple bytes of CA bus output from the NAND (i.e., Get Feature, Get Feature by LUN, Read ID), the multi-byte CA output packet format is more efficient versus the single-byte CA output packet format. However, for command sequences that produce only one byte of output from the NAND (i.e., Read Status), single-byte and multi-byte CA output format bus efficiencies are the same.

Similar to the single-byte CA output case, CA output mode is entered via CA Data Output header and CA output mode is exited by bringing CA_CE# high.

10.7.4 Additional CA[1:0] Output Timing Specifications

Figure 10.7-5 shows additional CA[1:0] timing specifications during the CA output burst. These timing specifications are applicable for both single-byte and multi-byte CA output packet formats:

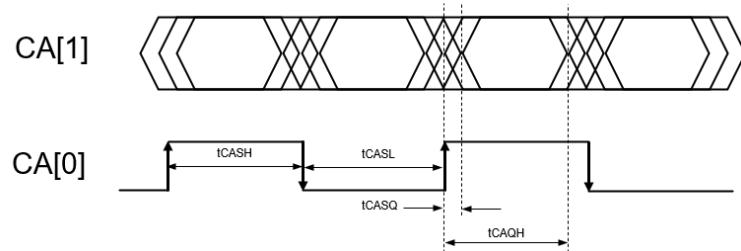


Figure 10.7-5 — Additional CA[1:0] Output Timing Specifications

10.8 SCA Header Definition

Table 10.8-1 shows the different SCA headers and corresponding packet types currently defined in the SCA protocol:

Table 10.8-1 — SCA Header Definition Table

Header Rising Edge		Header Falling Edge		CA Packet Type	CA Packet Structure
CA[1] (h[1]) (CLE)	CA[0] (h[0]) (ALE)	CA[1] (h[3]) (CLE)	CA[0] (h[2]) (ALE)		
0	0	0	0	CA Data Output	Output
0	0	0	1	VSP	VSP
0	0	1	0	CA Data Input	Input
0	0	1	1	VSP	VSP
0	1	0	0	Address	Input
0	1	0	1	Reserved	Reserved
0	1	1	0	Reserved	Reserved
0	1	1	1	Reserved	Reserved
1	0	0	0	Command	Input
1	0	0	1	VSP	VSP
1	0	1	0	VSP	VSP
1	0	1	1	Non-Target ODT (NTO)	Input
1	1	0	0	LUN Selection (LUNSel) (optional)	Input
1	1	0	1	Select Chip Enable (SCE)	Input
1	1	1	0	Select Chip Pause (SCP)	Input
1	1	1	1	Select Chip Terminate (SCT)	Input

10.9 DQ Bus Control Packets

In the SCA protocol, DQ bus operations are controlled via Select Chip Enable (SCE), Select Chip Pause (SCP), Select Chip Terminate (SCT), and Non-Target ODT (NTO) packets.

10.9.1 Select Chip Enable (SCE) Packet

The Select Chip Enable (SCE) packet is used to start or resume a data burst on the DQ bus. The data burst is started or resumed on the addressed LUN on the CA_CE_n.

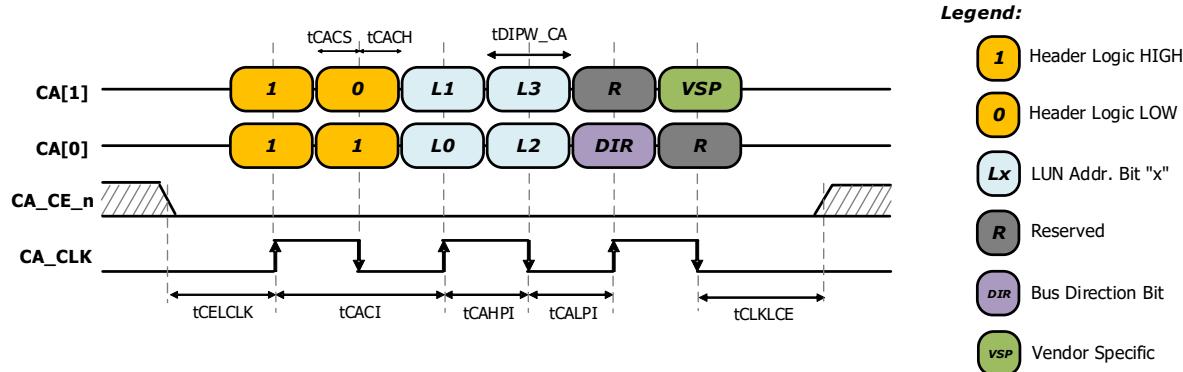


Figure 10.9-1 — Select Chip Enable (SCE) Packet

The DIR (Burst Direction Bit) is required to be supported by the controller while it is optional to be supported by NAND devices. When the DQ bus burst enabled by the SCE packet is in the data input direction for the NAND, the controller shall input '1' on the DIR bit. When the burst enabled by the SCE packet is in the data output direction for the NAND, the controller shall input '0' on the DIR bit.

For each reserved bit, the host shall input '0b'. When DQ warmup cycles are enabled, DQ warmup cycles occur after any SCE packet issuance, regardless of whether the SCE is the first one for the data burst, or a succeeding one that resumes a paused data burst (data burst paused by a prior SCP packet).

10.9.2 Select Chip Pause (SCP) Packet

The Select Chip Pause (SCP) packet is used to pause an on-going data burst on the DQ bus. The data burst is paused on the addressed LUN on the CA_CE_n. Once the data burst on a LUN has been paused, it may be resumed by the controller at a later time by issuing an SCE packet to the LUN.

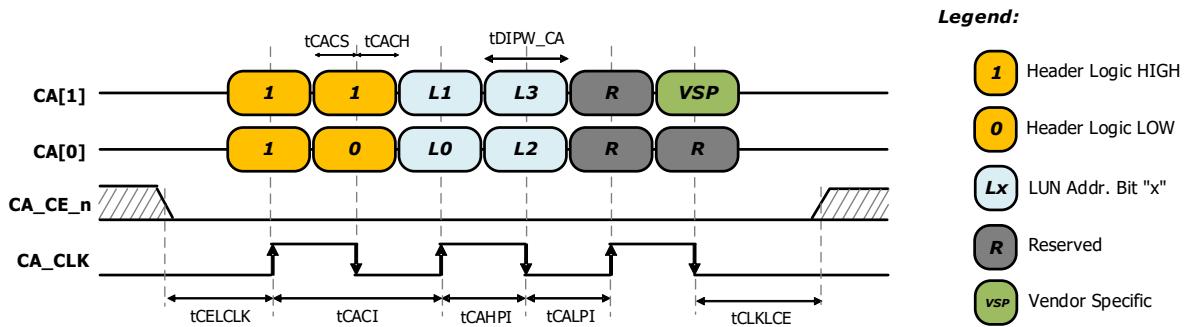
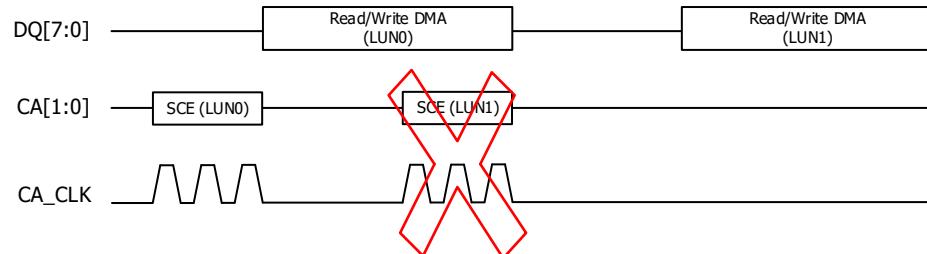


Figure 10.9-2 — Select Chip Pause (SCP) Packet

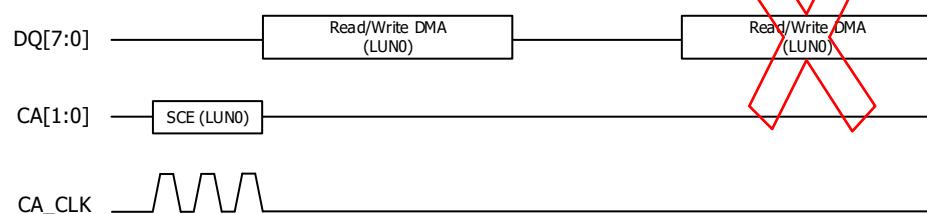
For each Reserved bit, the host shall input '0b'. SCP packet is required when pausing data for both resume data burst on a LUN and start a data burst on other LUN. Consecutive issuance of SCE packet without SCP packet is not allowed.

10.9.2 Select Chip Pause (SCP) Packet (cont'd)

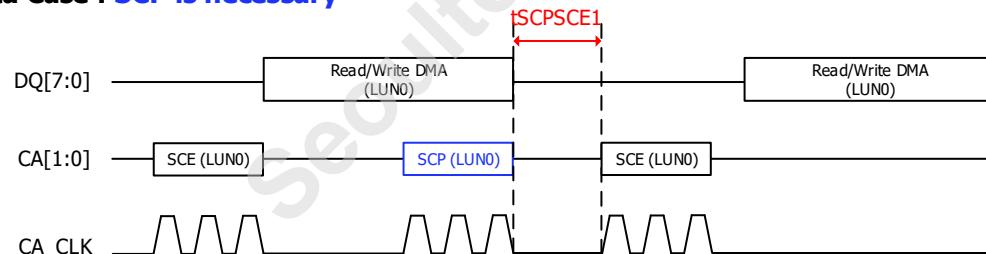
Pausing data + Interleaving Case



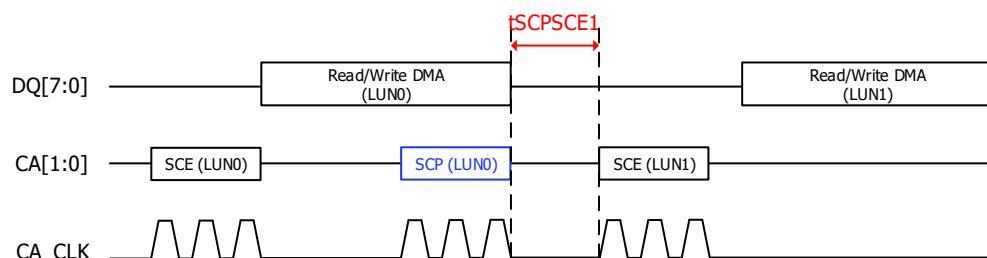
Pausing data Case



Pausing data Case : SCP is necessary



Pausing data + Interleaving Case¹⁾: SCP is needed



NOTE 1 Supporting of Pausing data + Interleaving case is vendor specific. Please follow each vendor's datasheet for more detail guidance..

Figure 10.9-3 — Proper Sequence of SCE Packet issuance with SCP Packet

10.9.3 Select Chip Terminate (SCT) Packet

The Select Chip Terminate (SCT) packet is used to terminate an on-going data burst on the DQ bus. The data burst is terminated on the addressed LUN on the CA_CE_n. Once the data burst on the LUN has been terminated, it cannot be resumed again by an SCE packet.

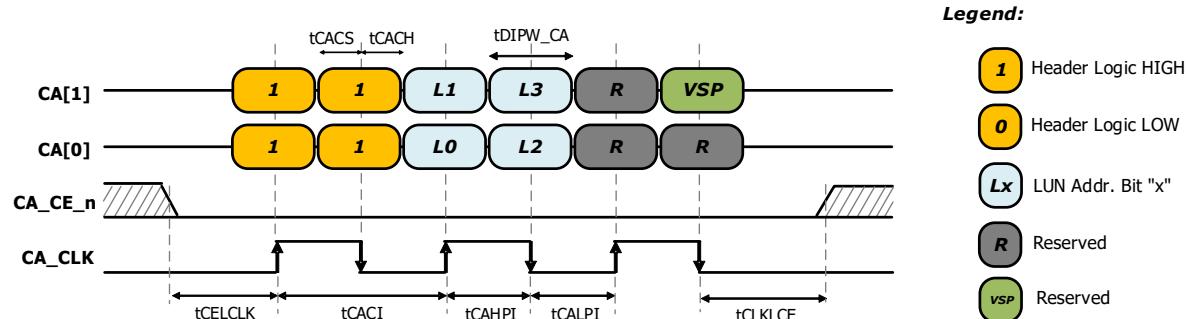


Figure 10.9-4 — Select Chip Terminate (SCT) Packet

For each Reserved bit, the host shall input '0b'.

To terminate a paused data burst (data burst paused with the SCP packet), the data burst must be resumed first by an SCE packet prior to issuance of the SCT packet.

10.9.4 Data Input Burst Sequence

The SCE packet is used to start/resume a data input burst on the DQ bus while SCP or SCT packets are used to pause or end a data input burst, respectively. **Figure 10.9-5** and **Figure 10.9-6** show data input burst sequence on the DQ bus and some of the relevant timings related to the sequence:

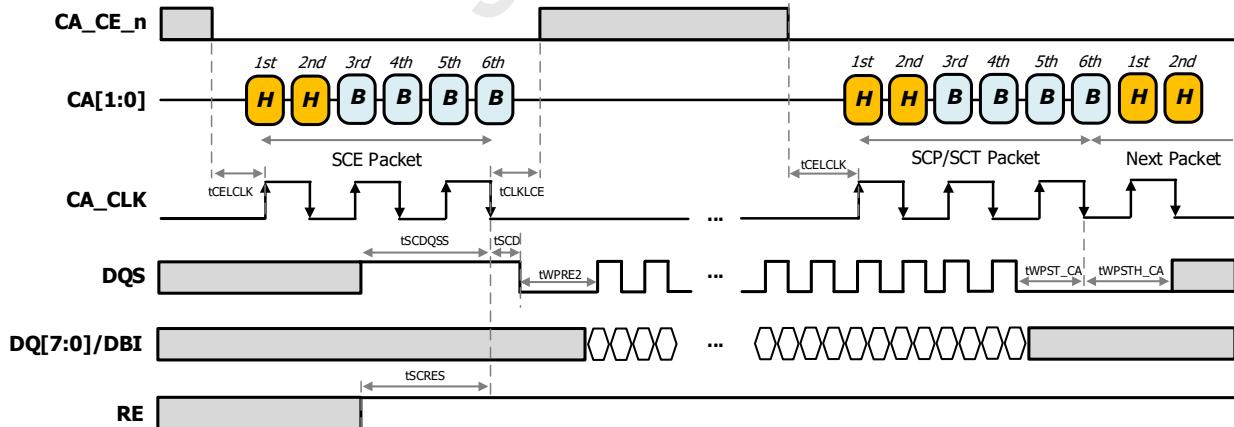


Figure 10.9-5 — Data Input Burst Sequence

10.9.4 Data Input Burst Sequence (cont'd)

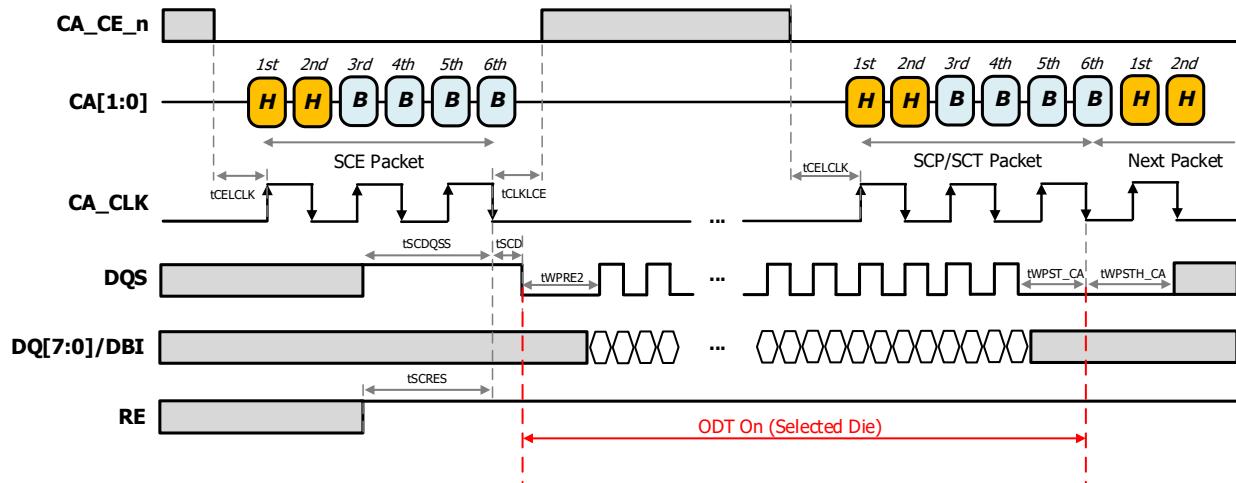


Figure 10.9-6 — Data Input Burst Sequence with ODT (Self-Termination)

10.9.5 Data Output Burst Sequence

The SCE packet is used to start/resume a data output burst on the DQ bus, while SCP or SCT packets are used to pause or end a data output burst, respectively. **Figure 10.9-7** and **Figure 10.9-8** show data output burst sequence on the DQ bus and some of the relevant timings related to the sequence:

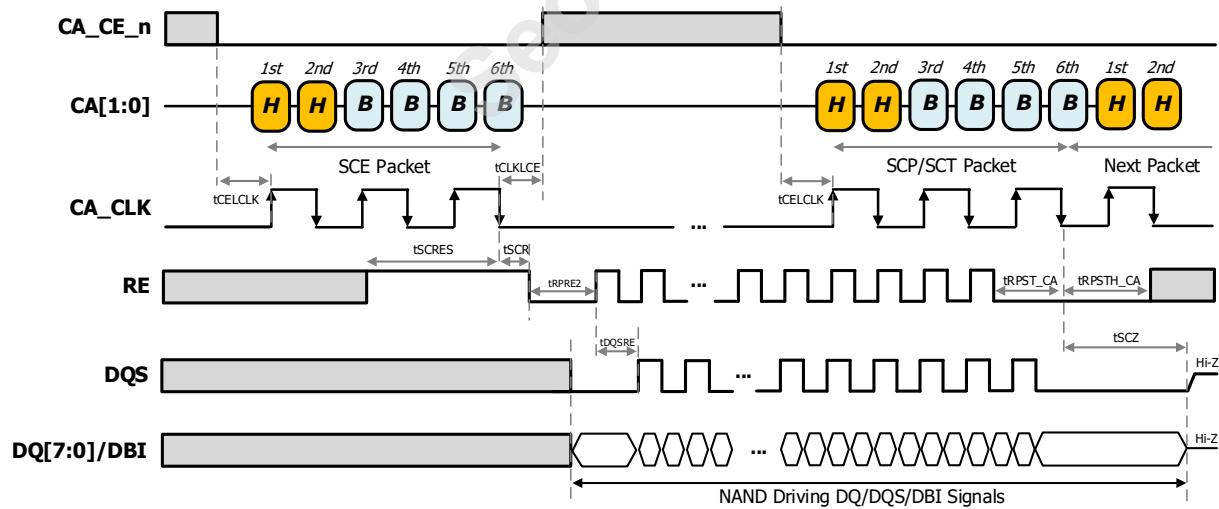


Figure 10.9-7 — Data Output Burst Sequence

10.9.5. Data Output Burst Sequence (cont'd)

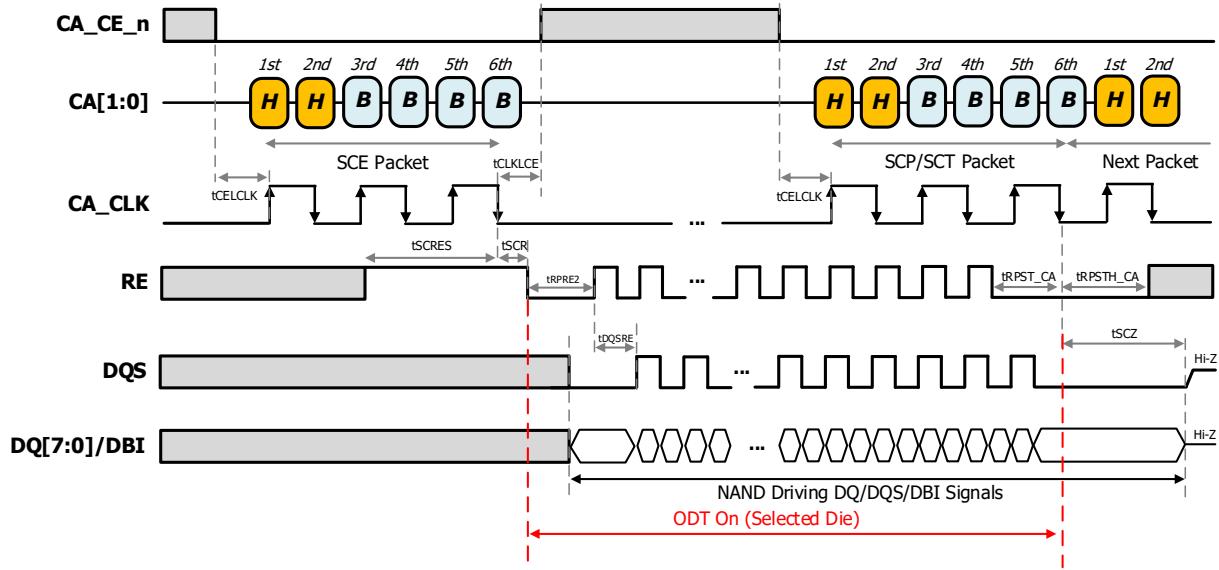


Figure 10.9-8 — Data Output Burst Sequence with ODT (Self-Termination)

10.9.6 Data Output Sequence Restrictions

After the latency time associated with a LUN-level or plane-level NAND array read command (i.e., tR), a Change Read Column Enhanced or Change Read Column (if supported by NAND vendor) command is required to be issued prior to the SCE command that enables the output of array data from the LUN.

Figure 10.9-9 shows the proper sequence where a Change Read Column Enhanced / Change Read Column (if supported by NAND vendor) command is issued after the array read latency time (i.e., tR), prior to the SCE command:

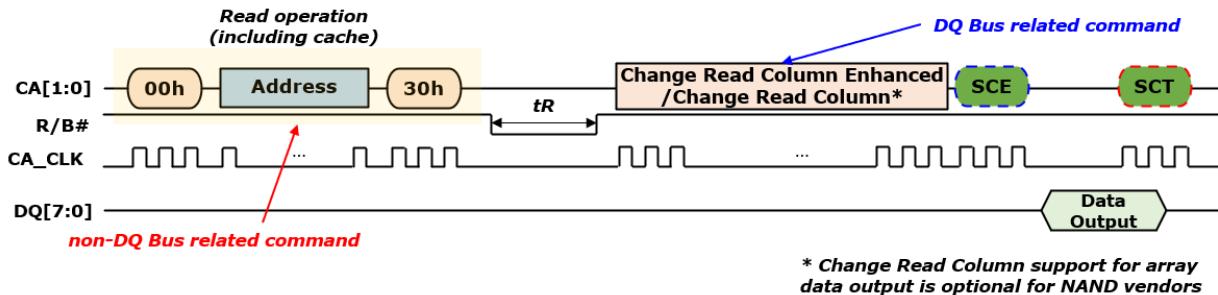


Figure 10.9-9 — Proper Data Output Sequence

Note that for CE#-level array read commands (e.g., Read Parameter Page), NAND vendors may require the use of Change Read Column instead of Change Read Column Enhanced command after the end of the read latency time, prior to the SCE command for data output.

10.9.6. Data Output Sequence Restrictions (cont'd)

Figure 10.9-10 shows an example of an illegal data output sequence due to missing Change Read Column Enhanced / Change Read Column (if supported by NAND vendor) command between the end of read latency time (i.e., tR) and the SCE command:

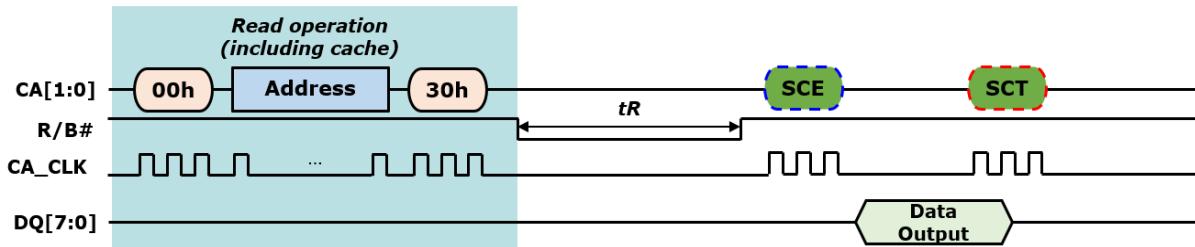


Figure 10.9-10 — Illegal Data Output Sequence Due to Missing Change Read Column Enhanced / Change Read Column

Issuing a 00h command instead of Change Read Column Enhanced or Change Read Column (if supported by NAND vendor) command to enable output of array data is also not allowed. **Figure 10.9-11** shows an example of an illegal data output sequence which uses 00h for array read data output.

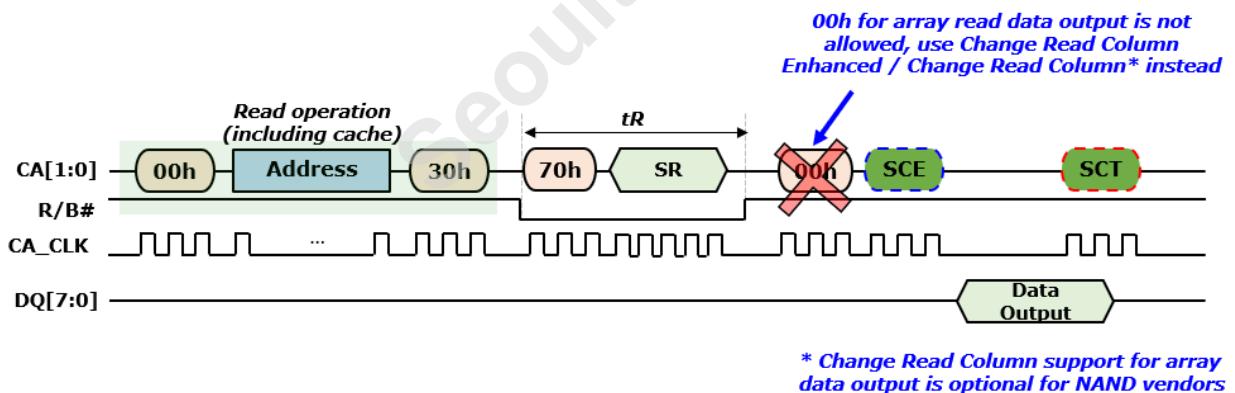


Figure 10.9-11 — Illegal Data Output Sequence Due to Use of 00h Instead of Change Read Column Enhanced / Change Read Column

10.9.7 Non-Target ODT (NTO) Packet

The Non-Target ODT (NTO) packet is used to control non-target ODT operations on the DQ bus.

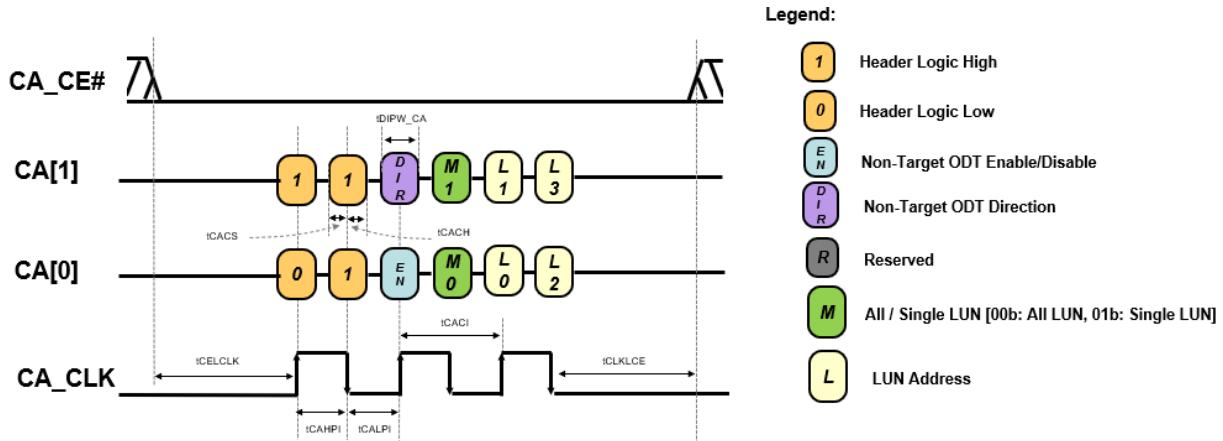


Figure 10.9-12 — Non-Target ODT (NTO) Packet

To enable (assert) non-target ODT, the host shall input a '1' on the EN bit. To disable (de-assert) non-target ODT, the host shall input a '0' on the EN bit.

When EN = 1 and the Non-Target ODT Direction (DIR) bit is cleared to '0', non-target ODT for data output burst is enabled. When EN = 1 and the Non-Target ODT Direction (DIR) bit is set to '1', non-target ODT for data input burst is enabled.

The M[1:0] and L[3:0] bits are optional for NAND vendors to support but are required for controller vendors to support. When NAND devices in the system do not support M[1:0] and L[3:0] bit functionality, the host shall drive M[1:0] and L[3:0] bits LOW.

When M[1:0] and L[3:0] bits are supported by the NAND, and when M[1:0] = 00b, the NTO packet enables/disables non-target ODT on all LUNs on the CA_CE# that have been configured to provide non-target ODT (the NTO packet LUN address bits are ignored).

When M[1:0] and L[3:0] bits are supported by the NAND, and when M[1:0] = 01b, the NTO packet enables/disables non-target ODT on a specific LUN on the CA_CE#. The LUN address bits L[3:0] select which LUN on the CA_CE# responds to the NTO packet. The L[3:0] decoding is such that when L[3:0] = 0h, then LUN0 responds to the NTO packet, when L[3:0] = 1h, then LUN1 responds, when L[3:0] = 2h, then LUN2 responds, and so on.

10.9.7 Non-Target ODT (NTO) Packet (cont'd)

Figure 10.9-13 is an example showing the use of NTO packets in asserting and de-asserting non-target ODT on a 4 package/4 CA_CE# channel system.

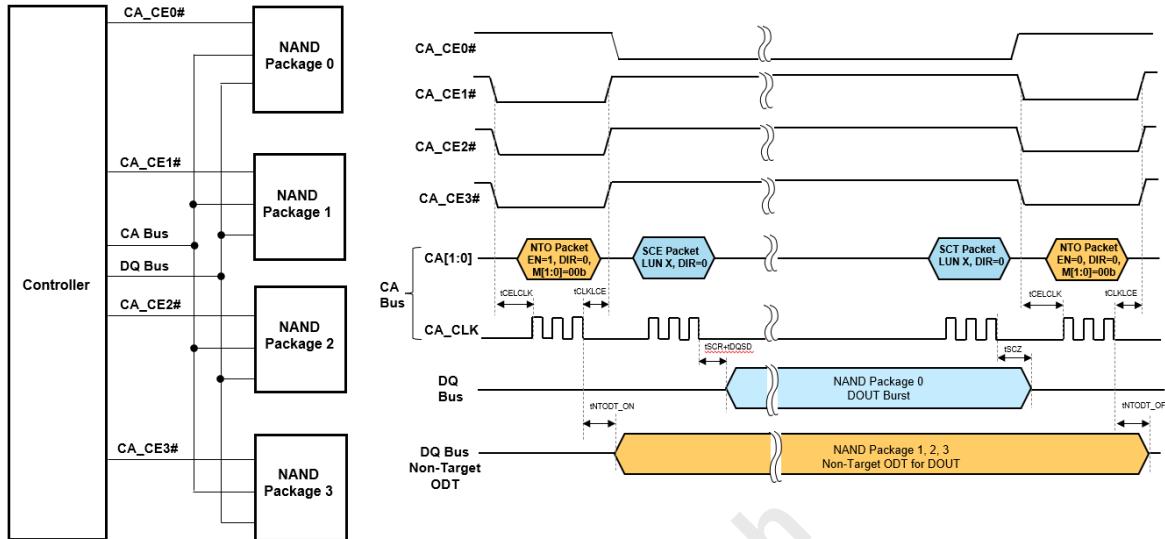


Figure 10.9-13 — NTO Packet Usage All LUN in CA_CE# Example

As can be seen in **Figure 10.9-13**, in order to enable or disable non-target ODT on NAND Packages 1, 2, and 3 with a single NTO packet issuance, the CA_CE# signals for those packages are all asserted when the NTO packet is issued. In order to provide a constant non-target ODT value during the entire data burst, the NTO packets encapsulate the SCE/SCT packets. Also, in the example above, with M[1:0]=00b in the NTO packets, all LUNs on the CA_CE# that were asserted during the NTO packet issuance, and which were pre-configured to provide non-target ODT, respond to the NTO packet. Issuing an NTO packet with M[1:0]=00b (all LUN mode) to the die with the data burst is prohibited.

Figure 10.9-14 shows an example of the use of the single LUN option (M[1:0]=01b) to achieve LUN granularity in non-target ODT control. An NTO packet with M[1:0] = 00b is initially issued to CA_CE1# to enable non-target ODT on the LUNs on CA_CE1#. Afterwards, another NTO packet with M[1:0]=01b and L[3:0]=1h is issued to CA_CE0# to enable non-target ODT on CA_CE0# LUN1. After burst completion, the non-target ODT is then disabled on CA_CE0# LUN1 and on the LUNs on CA_CE1#. Issuing an NTO packet with M[1:0]=01b (single LUN mode) to the die with the data burst is prohibited.

10.9.7 Non-Target ODT (NTO) Packet (cont'd)

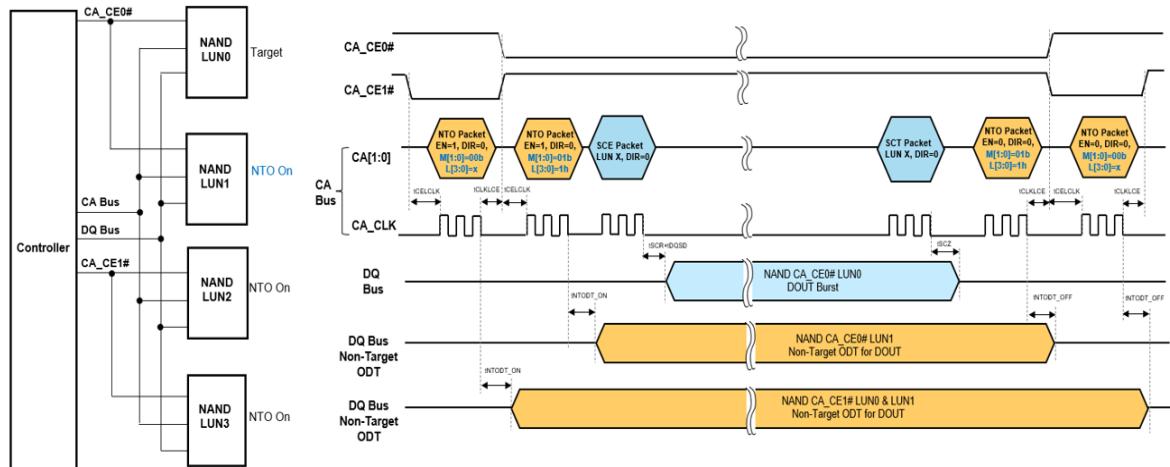


Figure 10.9-14 — NTO Packet Usage with LUN Granularity Example

10.10 LUN Selection (LUNSel) Packet (Optional)

The LUN Selection (LUNSel) packet is used to give LUN context to subsequent commands, or to feedforward LUN/Plane information to improve subsequent command latencies. NAND vendor support for the LUNSel packet is optional.

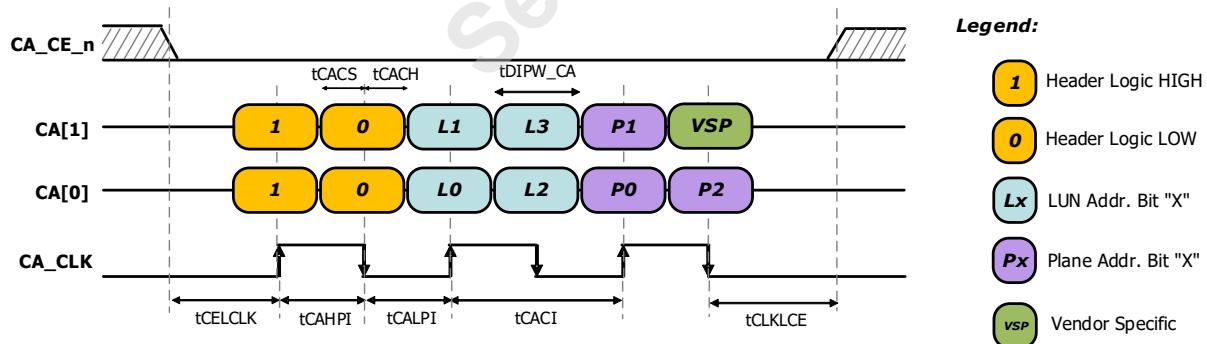


Figure 10.10-1 — LUNSel Packet

10.10 LUN Selection (LUNSel) Packet (Optional) (cont'd)

After LUNSel packet issuance, the tLUNSEL_CA specification is required to be met prior to issuance of the next packet:

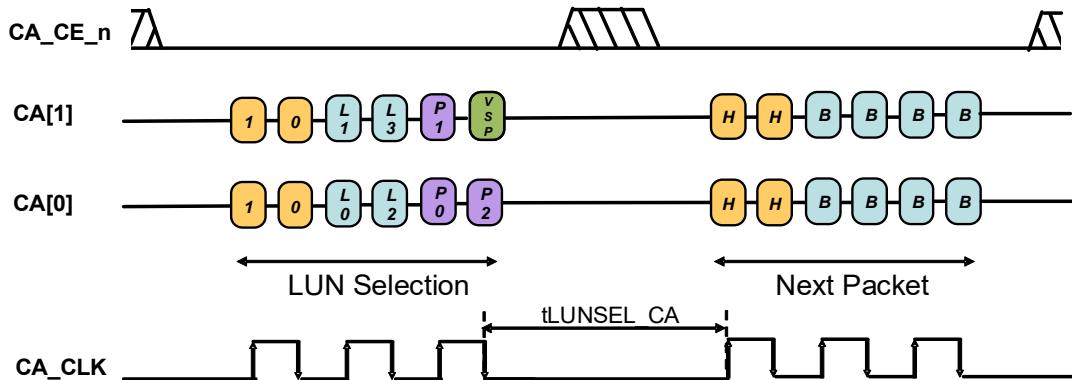


Figure 10.10-2 — tLUNSEL_CA Requirement

Figure 10.10-3 shows optional use of the LUNSel packet in a program sequence to give LUN address context to the subsequent program confirm (10h) command. The figure also shows optional use of the LUNSel packet in front of the Program Page (80h) and Change Read Column (06h-E0h) command sequences to feedforward the LUN/plane address and improve latencies related to these command sequences.

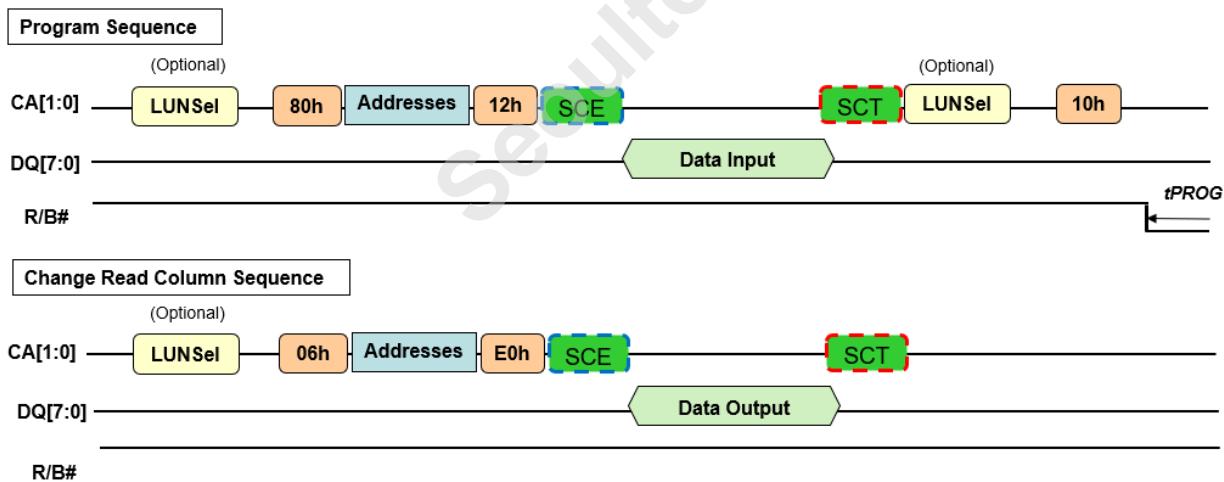


Figure 10.10-3 — LUNSel Packet Usage

NAND vendors may support all or a subset of these optional LUNSel packet usages (see vendor datasheet).

10.11 Command Pointer Reset Sequence

The command pointer reset sequence allows the host to abort an on-going CA bus packet transaction on a CA_CE# by bringing CA_CE# high. When CA_CE# is brought HIGH in the middle of a packet transaction, the packet transaction is aborted and the LUNs on the CA_CE# restart their command pointers. The host must then restart packet transactions to the LUNs on the CA_CE#, beginning with header cycle input of the next packet:

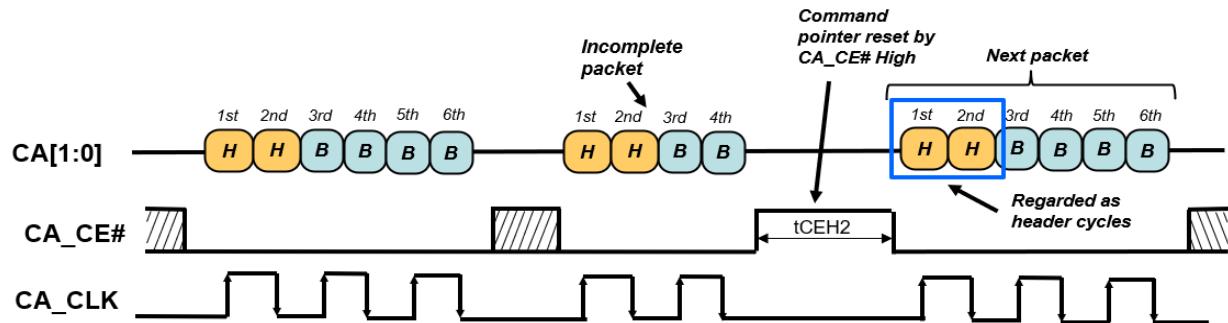


Figure 10.11-1 — Command Pointer Reset Sequence

10.12 Miscellaneous Command Sequences

10.12.1 Set Feature Sequence

Figure 10.12-1 shows the SCA protocol Set Feature (EFh) sequence.

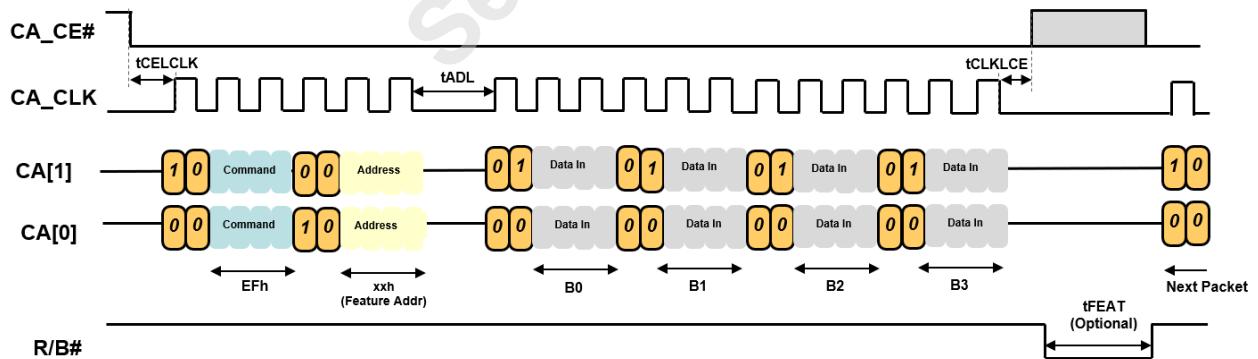


Figure 10.12-1 — Set Feature (EFh) Sequence

10.12.2 Program Sequence

Figure 10.12-2 shows program sequences for both Conv. and SCA protocols. tCDL is defined as command-to-data loading time and value is included in **Table 10.17-1 — SCA Protocol AC Timings**.

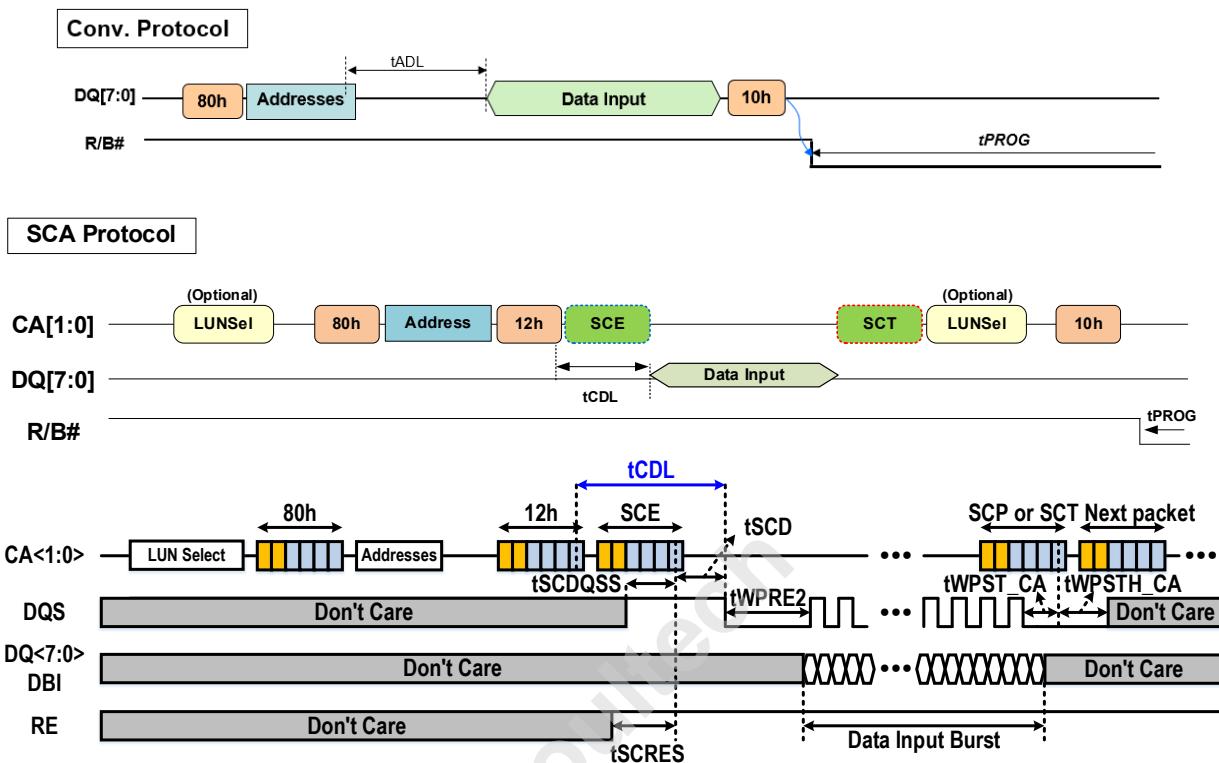


Figure 10.12-2 — Conv. and SCA Protocol Program Sequences

The SCA protocol program sequence requires the use of a 12h command packet after address input. It also requires the use of SCE/SCP/SCT packets for the data input burst and the optional LUNSel packet may be required (see NAND vendor datasheet) prior to the 80h command packet and/or prior to the program execution command packet (i.e., 10h).

10.12.3 Read Status Enhanced Sequence

Figure 10.12-3 shows the SCA protocol Read Status Enhanced (78h) sequence:

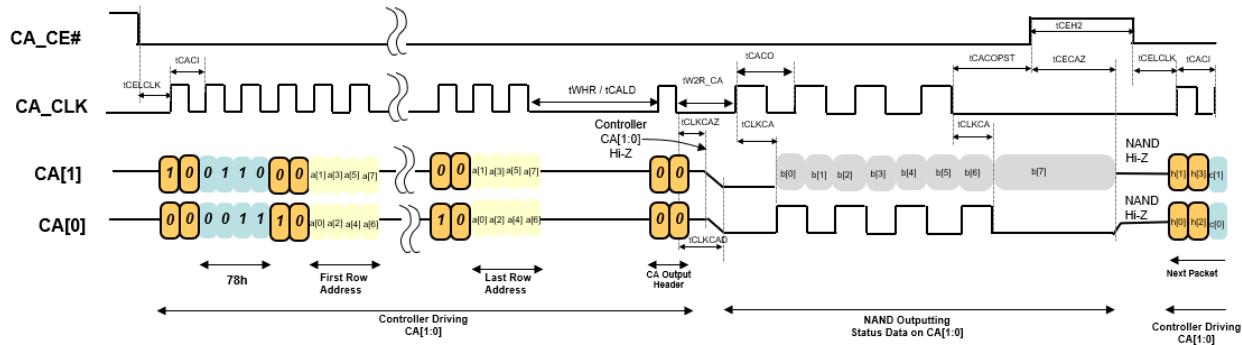


Figure 10.12-3 — Read Status Enhanced (78h) Sequence

10.12.4 Change Read Column / Change Read Column Enhanced Sequence

Figure 10.12-4 shows the start of a Change Read Column / Change Read Column Enhanced sequence on a CA_CE# with 2 LUNs.

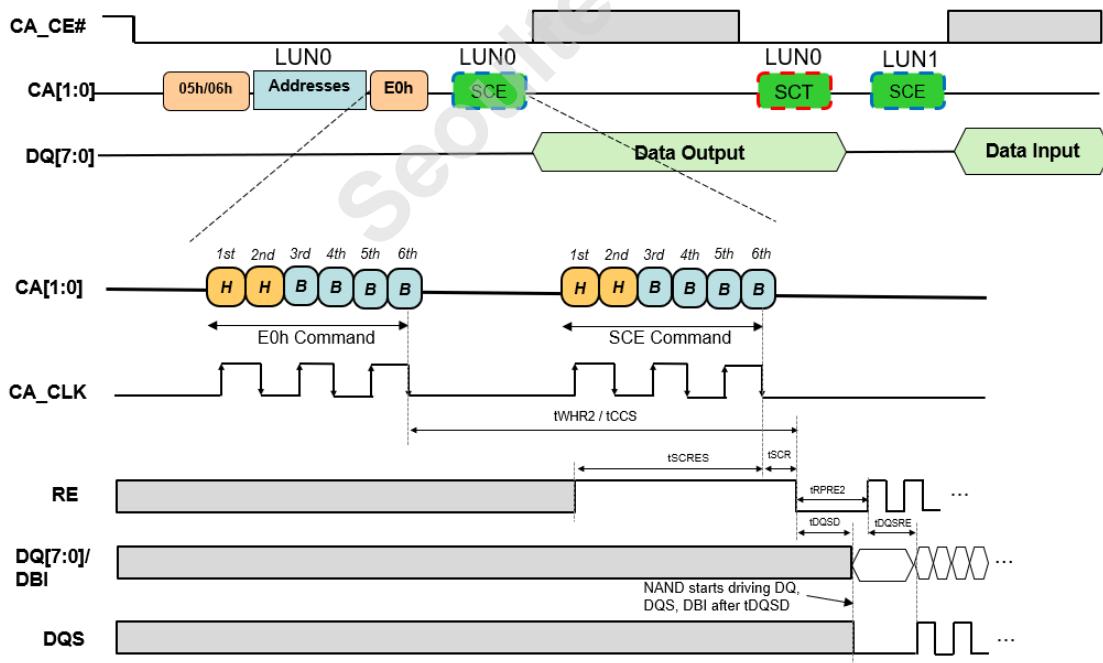


Figure 10.12-4 — Start of Change Read Column / Change Read Column Enhanced Sequence

10.12.4 Change Read Column / Change Read Column Enhanced Sequence (cont'd)

Figure 10.12-5 shows the end of the Change Read Column / Change Read Column Enhanced sequence on LUN0, back-to-back with an SCE packet that starts a data input burst on LUN1.

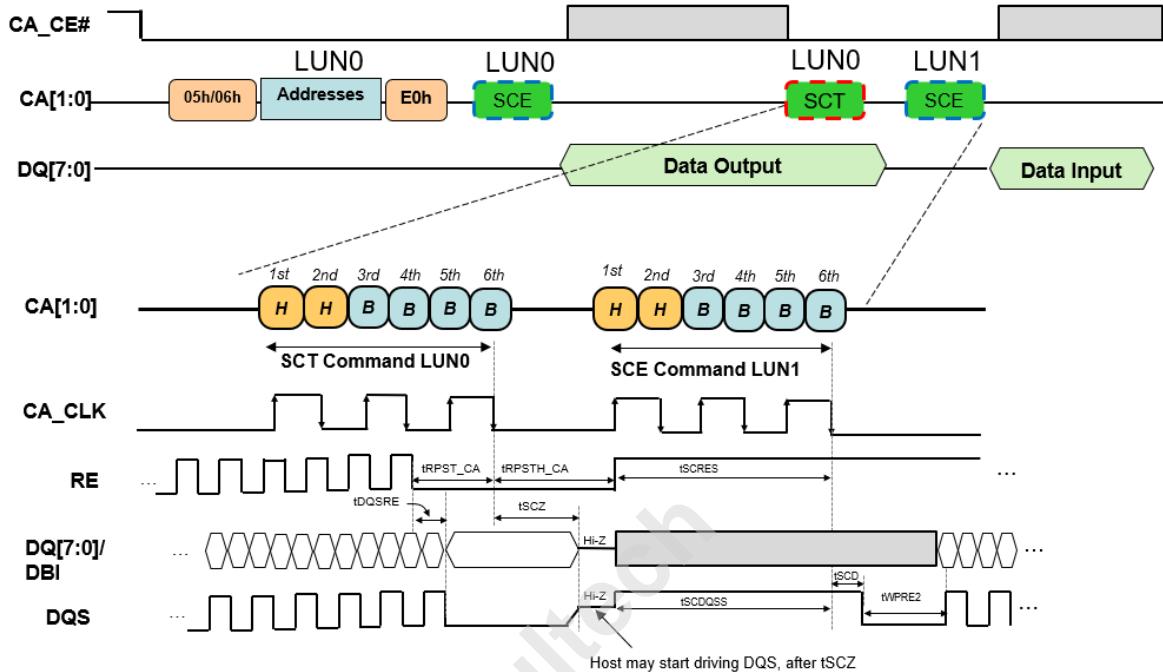
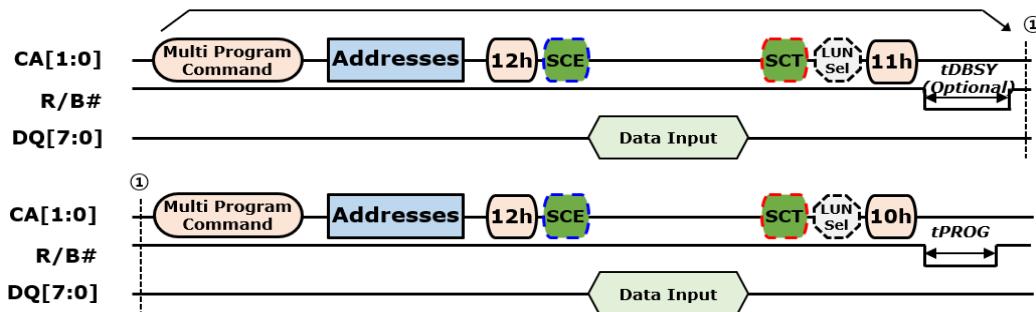


Figure 10.12-5 — End of Change Read Column / Change Read Column Enhanced Sequence

10.12.5 Multi-Plane Program Sequence

Figure 10.12-6 shows the SCA Protocol Multi-Plane Program Sequence format.



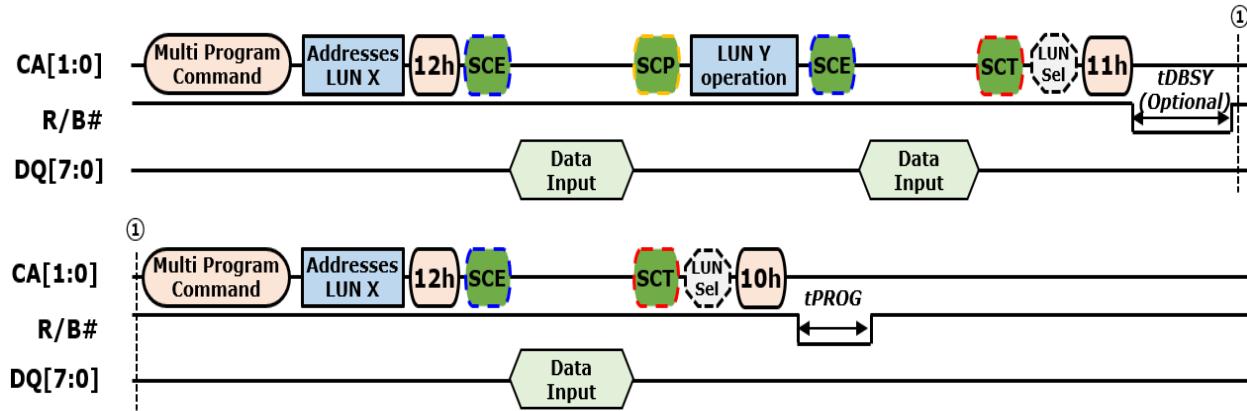
NOTES :

- 1) **Figure 10.12-6** shows the command sequence for the last page in a multi-plane program sequence
- 2) Number of address cycles may vary across NAND vendors
- 3) Different program/confirm command op-codes may be supported by NAND vendors (see vendor datasheet)
- 4) The tDBSY busy time may also be optional (see vendor datasheet)

Figure 10.12-6 — SCA Multi-Plane Program Sequence

10.12.5 Multi-Plane Program Sequence (cont'd)

Figure 10.12-7 shows an example of an allowed sequence where a command sequence to a different LUN (LUN Y) is interleaved while a data input burst is paused on a LUN (LUN X).



NOTE 1 Pausing the data burst is not needed when interleaving commands to another LUN. The example above just shows it is possible to interleave commands to another LUN after issuing an SCP to a LUN.

Figure 10.12-7 — Example of Allowed SCA Multi-Plane Program Sequence with LUN Interleaving During Data Input Burst Pause

Figure 10.12-8 shows an example of sequences that are not allowed while there is a paused data input burst on a LUN.

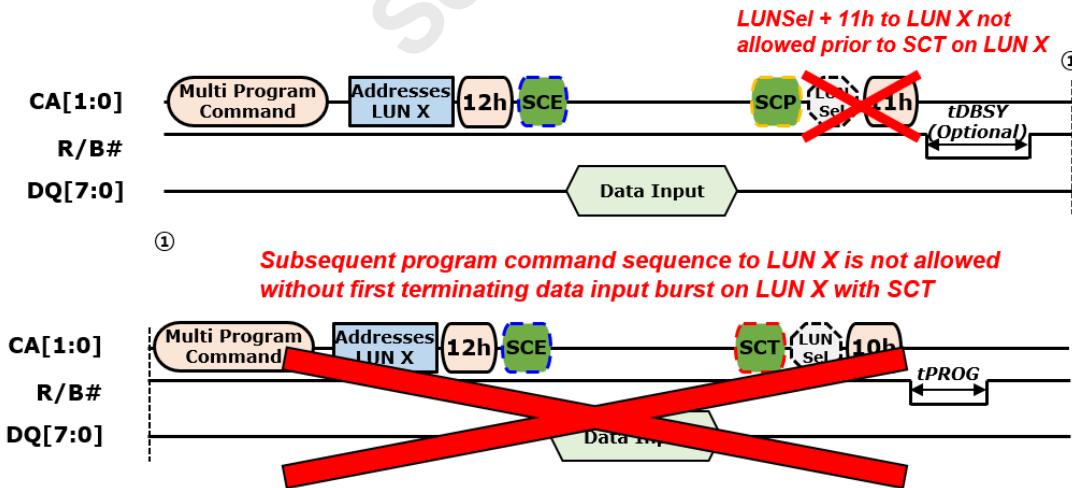
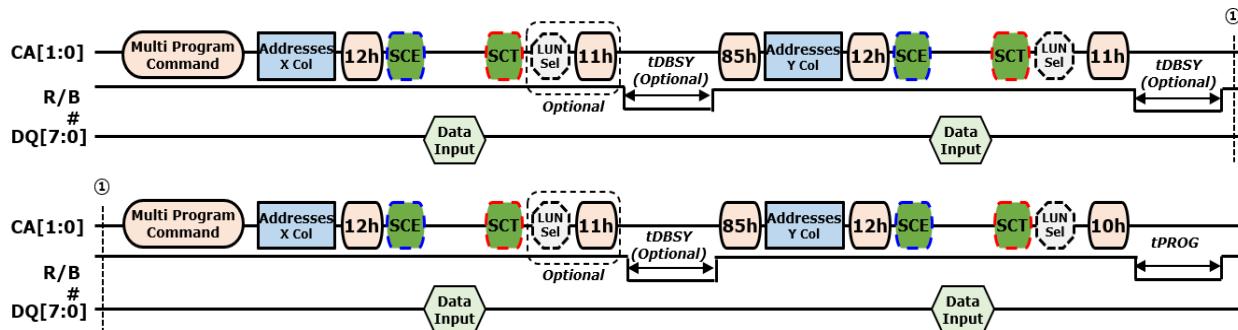


Figure 10.12-8 — Example of Sequences Not Allowed when a LUN has Paused Data Input Burst

10.12.6 Multi-Plane Program Sequence with Change Row Address

Figure 10.12-9 shows the format for an SCA Protocol Multi-Plane Program Sequence with Change Row Address.



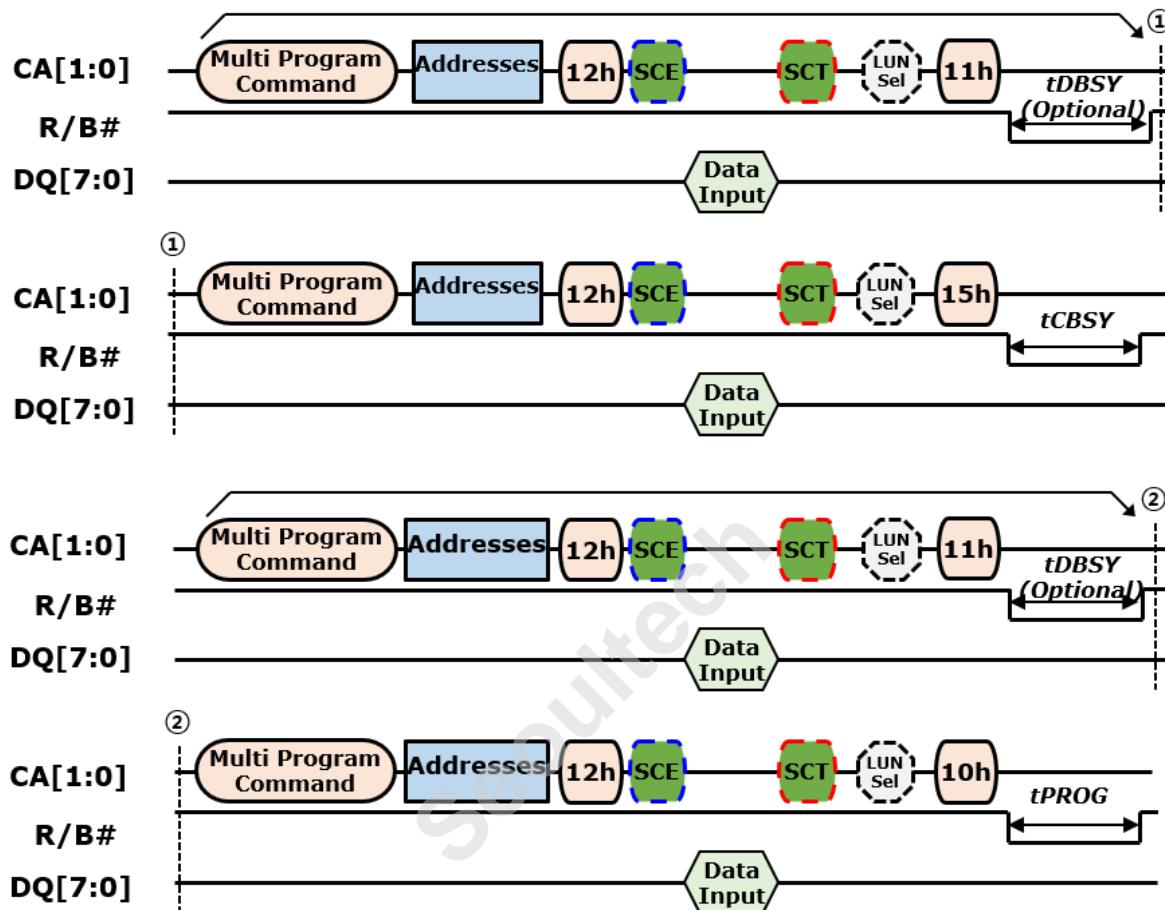
NOTES :

- 1) **Figure 10.12-9** shows the command sequence for the last page in a multi-plane program sequence
- 2) Number of address cycles may vary across NAND vendors
- 3) Different program/confirm command op-codes may be supported by NAND vendors (see vendor datasheet)
- 4) The tDBSY busy time may also be optional (see vendor datasheet)
- 5) NAND vendors may optionally require a LUNSel-11h prior to the Change Row Address (85h-Addresses-12h) sequence (see vendor datasheet)

Figure 10.12-9 — SCA Multi-Plane Program Sequence with Change Row Address

10.12.7 Multi-Plane Cache Program Sequence

Figure 10.12-10 shows the SCA Multi-Plane Cache Program Sequence format.



NOTES:

- 1) Figure 10.12-10 shows the command sequence for the last 2 pages in a multi-plane cache program sequence
- 2) Number of address cycles may vary across NAND vendors
- 3) Different program/cache confirm command op-codes may be supported by NAND vendors (see vendor datasheet)
- 4) The tDBSY busy time may also be optional (see vendor datasheet)

Figure 10.12-10 — SCA Multi-Plane Cache Program Sequence

10.13 Command Interleaving

10.13.1 DQ and Non-DQ Related Commands

Commands to the NAND may be classified into two:

- a) DQ related commands
- b) Non-DQ related commands

DQ related commands are not allowed to be issued to a die that is still executing a prior DQ related command, has a paused data burst (by SCP command), or already has a queued up DQ related command awaiting data burst execution.

Non-DQ related commands may be issued to a die that is still executing a prior DQ related command, or already has a queued up DQ related command awaiting data burst execution (subject to NAND vendor specific restrictions).

Table 10.13-1 lists examples of DQ bus related and non-DQ bus related commands:

Table 10.13-1 — Examples of DQ Related and Non-DQ Related Commands

DQ Bus Related Commands	Non-DQ Bus Related Commands
Reads from NAND Cache Register / Page Register	Read Status Commands
Writes to NAND Cache Register / Page Register	Set Feature / Set Feature by LUN ¹⁾
NAND Column Address Change Commands	Get Feature / Get Feature by LUN
Program Commands	Read ID
Erase Commands	Resets
ZQ Calibration DCC training via 18h command / Read DQ Training (62h) / Write DQ Training (63h/64h)	Array Read (with NAND vendor specific restrictions)
NOTE 1 Set Feature / Set Feature by LUN sequences which change DQ bus input/output options (e.g., warmup cycles, ODT or other DQ bus settings) are prohibited to be issued to LUNs that have on-going DQ bus input/output operations or actively providing ODT on the channel.	

10.13.2 Command Interleaving Examples

Figure 10.13-1 illustrates improper interleaving of DQ related commands on a CA_CE# with 2 LUNs.

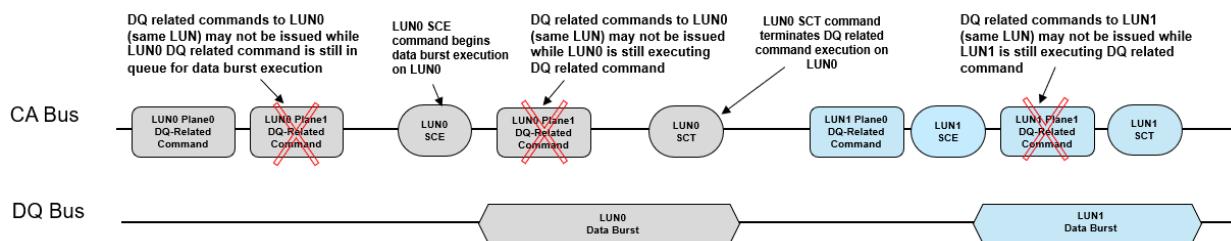


Figure 10.13-1 — Improper DQ Related Command LUN Interleaving Example

10.13.2 Command Interleaving Examples (cont'd)

Figure 10.13-2 illustrates proper interleaving of DQ related commands on a CA_CE# with 2 LUNs.

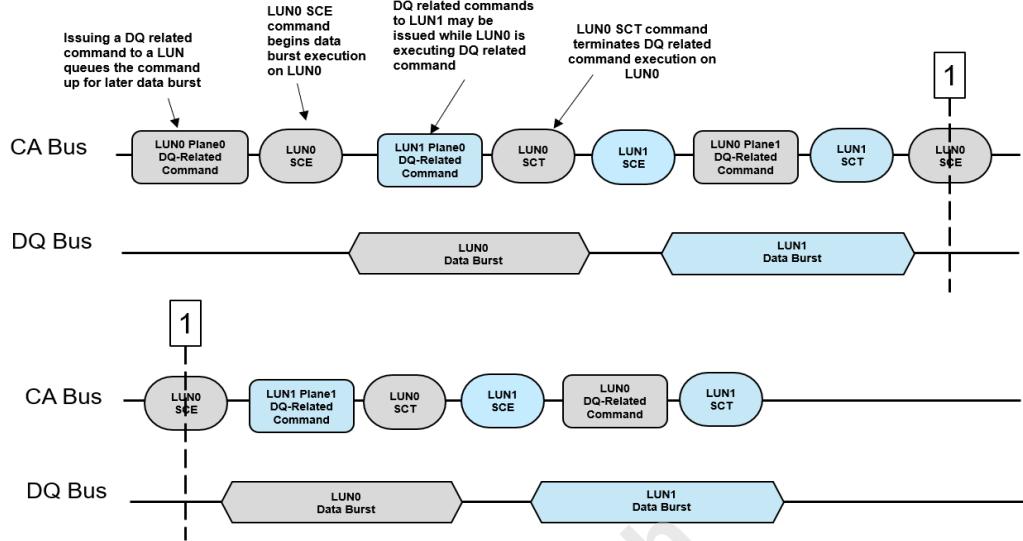


Figure 10.13-2 — Proper DQ Related Command LUN Interleaving Example – Single CA_CE#

Figure 10.13-3 shows another example of proper LUN interleaving this time on a channel with multiple CA_CE#'s and multiple LUNs per CA_CE#.

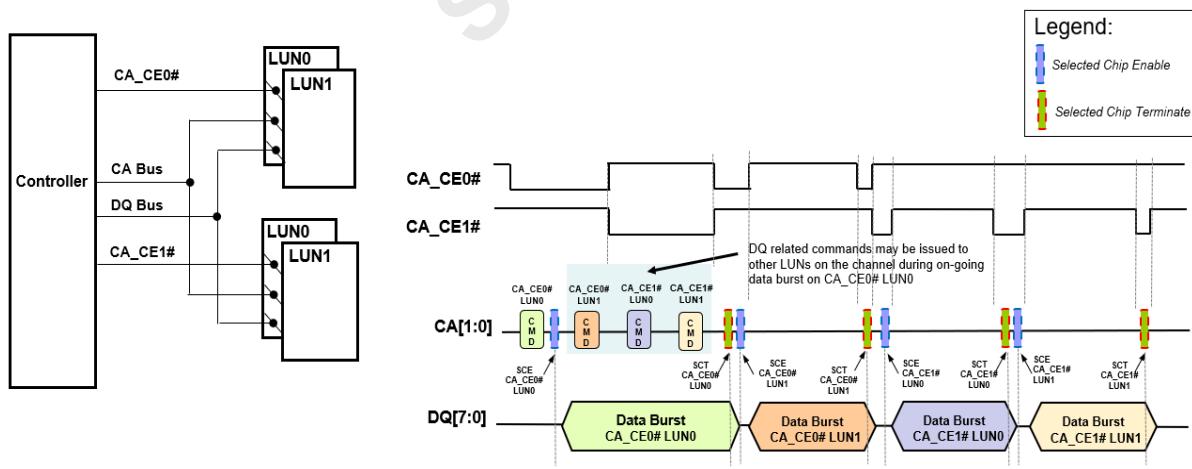


Figure 10.13-3 — Proper DQ Related Command LUN Interleaving Example - Multiple CA_CE#

10.13.2 Command Interleaving Examples (cont'd)

Figure 10.13-4 shows an example of proper interleaving of non-DQ related commands with DQ related commands on a CA_CE# with at least 3 LUNs.

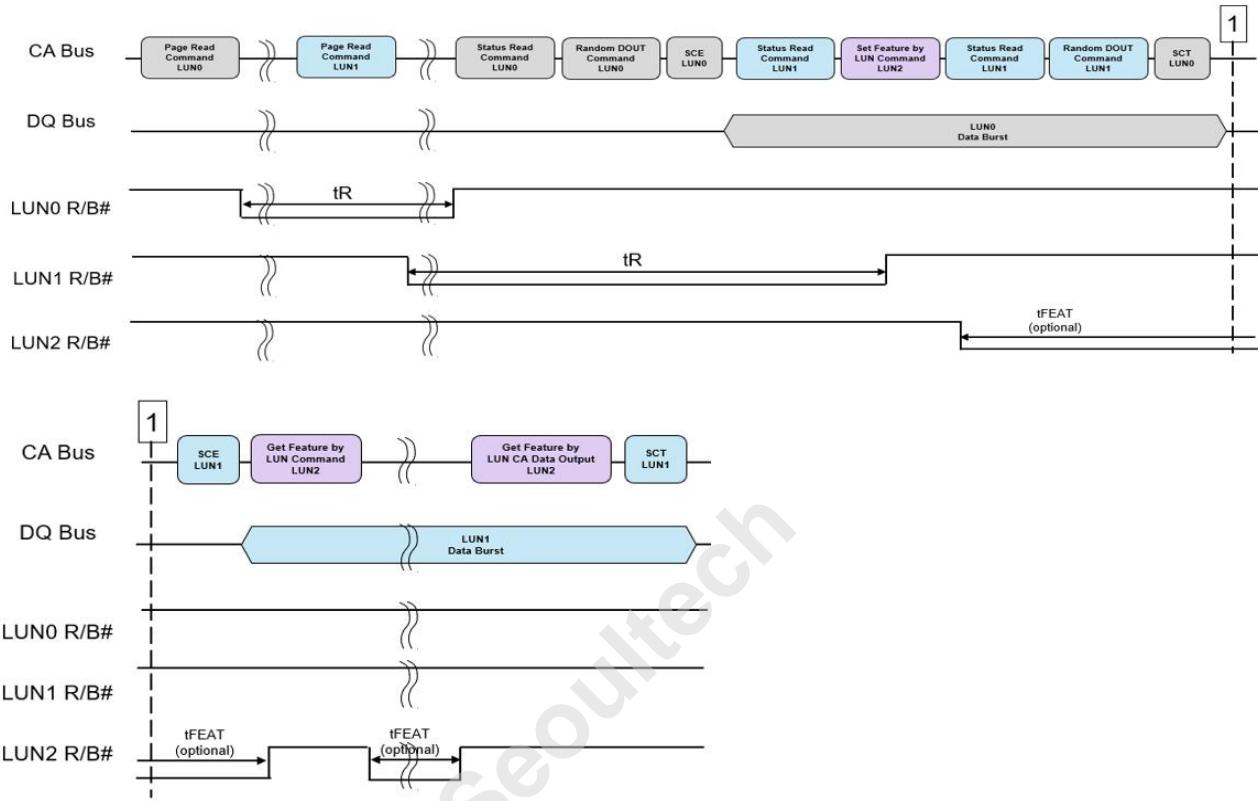


Figure 10.13-4 — Proper DQ and Non-DQ Related Command LUN Interleaving Example

10.13.3 Status Reads / LUN Interleaving During Get Feature / Get Feature by LUN

Status Reads during Get Feature / Get Feature by LUN tFEAT are subject to NAND vendor specific restrictions (see NAND vendor device datasheet).

Status Reads or LUN interleaving during Get Feature / Get Feature by LUN sequences that do not have any busy time, are not allowed.

For Get Feature / Get Feature by LUN sequences that have a busy time, the following sequence to retrieve Get Feature / Get Feature by LUN data after Status Reads to same LUN may be supported:

10.13.3 Status Reads / LUN Interleaving During Get Feature / Get Feature by LUN (cont'd)

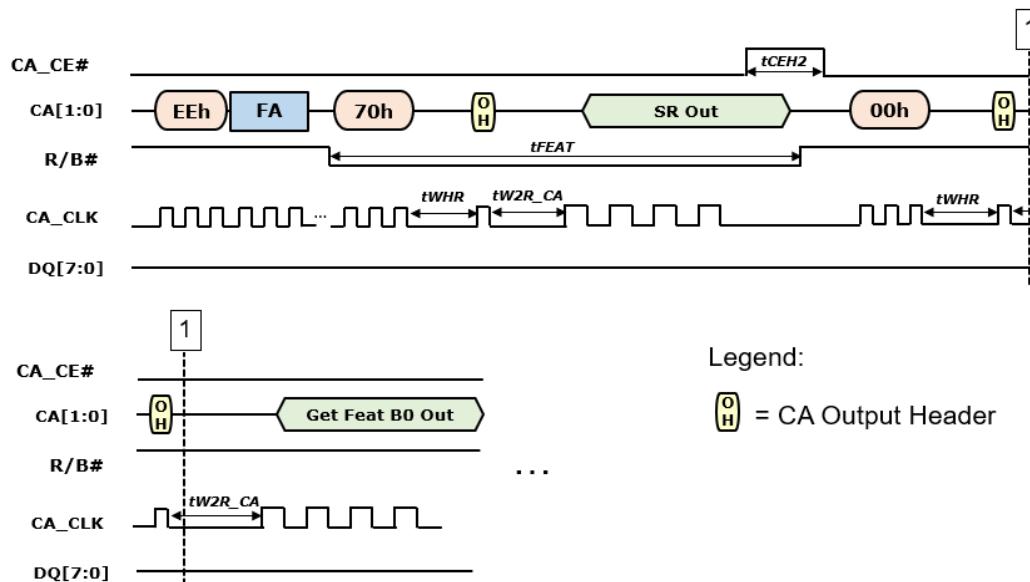


Figure 10.13-5 — Get Feature Data Retrieval after Read Status to Same LUN

For Get Feature / Get Feature by LUN sequences that have a busy time, the following sequence to retrieve Get Feature / Get Feature by LUN data after LUN Interleaving may be supported.

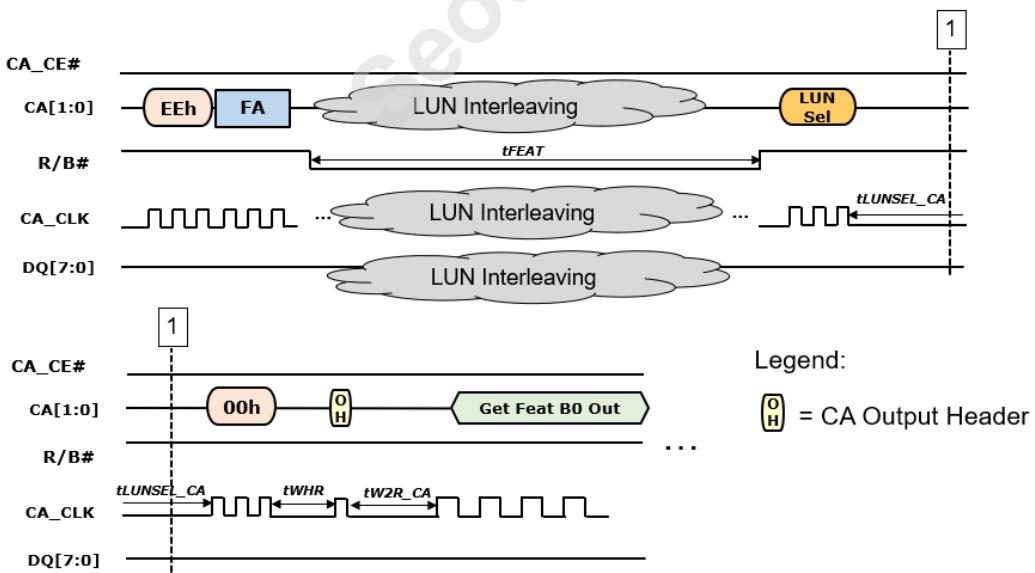


Figure 10.13-6 — Get Feature Data Retrieval after LUN Interleaving

10.14 CA Training Feature Address Register (FA 25h) (Optional)

The FA 25h register can optionally be implemented by NAND vendors to provide a mechanism for the controller to train the CA bus. The host may write a data pattern to FA 25h (via Set Feature or Set Feature by LUN sequence) and read the written data pattern back out (via Get Feature or Get Feature by LUN sequence). The register bits in FA 25h do not affect any NAND functionality and the sole purpose is for CA bus training.

Table 10.14-1 — Feature Table for SCA Protocol CA Bus Training Register [25h]

Sub-feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0					B0 data pattern			
B1					B1 data pattern			
B2					B2 data pattern			
B3					B3 data pattern			

10.15 SCA DQ Mirror Mode Bit (Optional)

Table 7.1-1 shows the FA 02h register with the optional SCA_DQMIRR bit at FA 02h B3[1]. In the SCA protocol, since the CA bus is separate from the DQ bus, it allows DQ mirror mode to be configured via Set Feature sequence on the CA bus.

When SCA_DQMIRR = '0', then the DQ mirror function is disabled on the NAND. If SCA_DQMIRR = '1', then the DQ mirror function is enabled on the NAND.

When the DQ mirror function is enabled, DQ[0] is logically interpreted by the NAND as DQ[7], DQ[1] as DQ[6], DQ[2] as DQ[5], DQ[3] as DQ[4], DQ[4] as DQ[3], DQ[5] as DQ[2], DQ[6] as DQ[1] and DQ[7] as DQ[0].

10.16 SCA Protocol AC and DC Levels

Table 10.16-1 — SCA Protocol AC and DC Levels

Category	Spec	Min	Max	Unit
CA Input Specs	V _{IH.CA(AC)}	0.8*VccQ	-	V
	V _{IH.CA(DC)}	0.7*VccQ	-	
	V _{IL.CA(AC)}	-	0.2*VccQ	
	V _{IL.CA(DC)}	-	0.3*VccQ	
CA Output Specs	V _{OH.CA(DC)}	0.7*VccQ	-	
	V _{OL.CA(DC)}	-	0.3*VccQ	

NOTES:

- 1) CA Input Specs apply to CA[1:0], CA_CLK, CA_CE# signals and also to SCA signal when the SCA signal is driven and not floated.
- 2) CA Output Specs apply to CA[1:0] signals. The NAND CA[1:0] nominal output drive strength is 50 ohms and does not support ZQ calibration.
- 3) CA[1:0], CA_CLK, CA_CE# will operate unterminated
- 4) All AC Timing measurements are with respect to 0.5*VccQ signal crossing

10.17 SCA Protocol AC Timings

Table 10.17-1 — SCA Protocol AC Timings

Symbol	Description	Min	Max	Unit	Notes
tCELCLK	CA_CE# setup to CA_CLK edge	20	-	ns	
tCLKLCE	CA_CLK# hold to CA_CE# edge	20	-	ns	
tCACI	CA_CLK input cycle time	4	-	ns	
tCAHPI	CA_CLK input cycle high time	0.45	-	tCACI	
tCALPI	CA_CLK input cycle low time	0.45	-	tCACI	
tCACS	CA setup time to CA_CLK @1 V/ns slew rate	0.6	-	ns	
tCACH	CA hold time from CA_CLK @ 1 V/ns slew rate	0.6	-	ns	
tCEH2	Minimum CA_CE# high pulse width	30	-	ns	
tDIPW_CA	CA minimum input pulse width	0.33	-	tCACI	
tCACO	CA_CLK output cycle time	10	-	ns	
tCAHPO	CA_CLK output high time	0.45	-	tCACO	
tCALPO	CA_CLK output low time	0.45	-	tCACO	
tCLKCA	CA_CLK to CA output	-	30	ns	
tCACOPST	CA_CLK post-amble time	tCLKCA+0.5*tCACO	-	ns	
tCDL	CA_CLK final edge for 12h command packet to start of write pre-amble	400	-	ns	1
tCECAZ	CA_CE# high to CA Hi-Z time	0	30	ns	
tCASQ	CA to CA strobe skew	-	0.15*tCACO	ns	
tCAQH	CA hold time	Min(tCAHPO, tCALPO) – 0.15*tCACO	-	ns	
tCASH	CA strobe high time	tCAHPO – 0.15*tCACO	-	ns	
tCASL	CA strobe low time	tCALPO – 0.15*tCACO	-	ns	
tSCPSCE1	SCP to SCE restriction	VSP	-	ns	
tSCRES	RE_n valid before SCE command final CA_CLK low	10	-	ns	
tSCR	CA_CLK final edge to RE_n low	50	-	ns	

Table 10.17-1 — SCA Protocol AC Timings (cont'd)

Symbol	Description	Min	Max	Unit	Notes
tRPRE2	RE_n pre-amble time	30	-	ns	
tRPST_CA	RE_n post-amble setup with respect to final CA_CLK edge	tDQSRE+0.5*tRC	-	ns	
tRPSTH_CA	RE_n post-amble hold with respect to final CA_CLK edge	50	-	ns	
tCLKCAD	CA output header last CA_CLK edge to CA output drive	-	20	ns	
tCLKCAZ	CA output header last CA_CLK edge to host Hi-Z (Note: Bus conflict impact is minimized when tCLKCAZ is shorter than tCLKCAD)	-	5	ns	
tW2R_CA	CA output header last CA_CLK edge to first CA_CLK for CA output (does not include tWHR)	20	-	ns	
tSCDQSS	DQS high before SCE command final CA_CLK low	10	-	ns	
tSCD	SCE command final CA_CLK low to DQS low	50	-	ns	
tWLCEL_CA	CA_CLK low setup to first CE# low after SCA protocol has been enabled	100	-	ns	
tWPRE2	DQS pre-amble time during write operation	25	-	ns	
tWPST_CA	DQS post-amble setup time with respect to final CA_CLK edge	6.5	-	ns	
tWPSTH_CA	DQS post-amble hold time with respect to final CA_CLK edge	50	-	ns	
tR2W_CA	Last CA output CA_CLK falling edge to the CA_CLK rising edge which starts the next header	tCACOPST + tCEH2 + tCELCLK	-	ns	
tDQSRE	Data output RE_n to DQS latency	-	25	ns	
tNTODT_ON	NTO packet last CA_CLK falling edge to when non-target ODT is enabled	-	60	ns	
tNTODT_OFF	NTO packet last CA_CLK falling edge to when non-target ODT is disabled	-	60	ns	
tSCZ	SCT/SCP packet last CA_CLK falling edge to when DQ/DQS/DBI signals are Hi-Z	-	50	ns	
tLUNSEL_CA	LUNSel packet last CA_CLK falling edge to next packet first CA_CLK rising edge	20	-	ns	
NOTE 1 tCDL = tADL – 3*tCACI					

10.18 SCA Reset Restrictions

10.18.1 SCA Reset (FFh) Restrictions

- a) If a data output burst is on-going from a LUN on a CA_CE# (RE is being toggled for data output), the host is required to hold the RE signals static ($RE_t = 0$, $RE_c = 1$) prior to issuing the Reset (FFh) command to the CA_CE#. Issuance of SCT or SCP are not required prior the Reset (FFh) command to the CA_CE#.
- b) If a data input burst is on-going to a LUN on a CA_CE# (DQS is being toggled for data input), the host is required to hold the DQS signals static ($DQS_t = 0$, $DQS_c = 1$) prior to issuing the Reset (FF) command to the CA_CE#. Issuance of SCT or SCP are not required prior the Reset (FFh) command to the CA_CE#.
- c) To ensure that the NAND devices on the CA_CE# accept the Reset (FFh) command, a Command Pointer Reset sequence is required to be issued by the host prior to the issuance of the Reset (FFh) command.

10.18.2 SCA Reset by LUN (FAh) Restrictions

- a) If a data output burst is on-going from a LUN on a CA_CE# (RE is being toggled for data output), the host is required to hold the RE signals static ($RE_t = 0$, $RE_c = 1$) prior to issuing the Reset by LUN (FAh) sequence to that LUN. Issuance of SCT or SCP are not required prior to the issuance of a Reset by LUN (FAh) sequence to that LUN.
- b) If a data input burst is on-going to a LUN on a CA_CE# (DQS is being toggled for data input), the host is required to hold the DQS signals static ($DQS_t = 0$, $DQS_c = 1$) prior to issuing the Reset by LUN (FAh) sequence to that LUN. Issuance of SCT or SCP are not required prior to the issuance of a Reset by LUN (FAh) sequence to that LUN.
- c) If a data input burst is on-going to a LUN or a data output burst is on-going from a LUN on a CA_CE#, a Reset by LUN (FAh) sequence may be issued to a different LUN on the CA_CE# without holding the data input burst or data output burst static, provided that either:
 - i. The LUN to which the Reset by LUN (FAh) is issued is not providing non-target ODT for the LUN which has an on-going data burst, or
 - ii. The LUN to which the Reset by LUN (FAh) is issued is providing non-target ODT, and the non-target ODT is unaffected by the Reset by LUN (FAh) sequence.
- d) To ensure that the Reset by LUN (FAh) command is accepted by the LUN address by the Reset by LUN (FAh) command, a Command Pointer Reset sequence is required to be issued by the host prior to the issuance of the Reset by LUN (FAh) command.

10.18.3 Reset Timing Diagrams

Figure 10.18-1 shows the required reset sequence and timings when a data output burst is interrupted by a Reset (FFh) command:

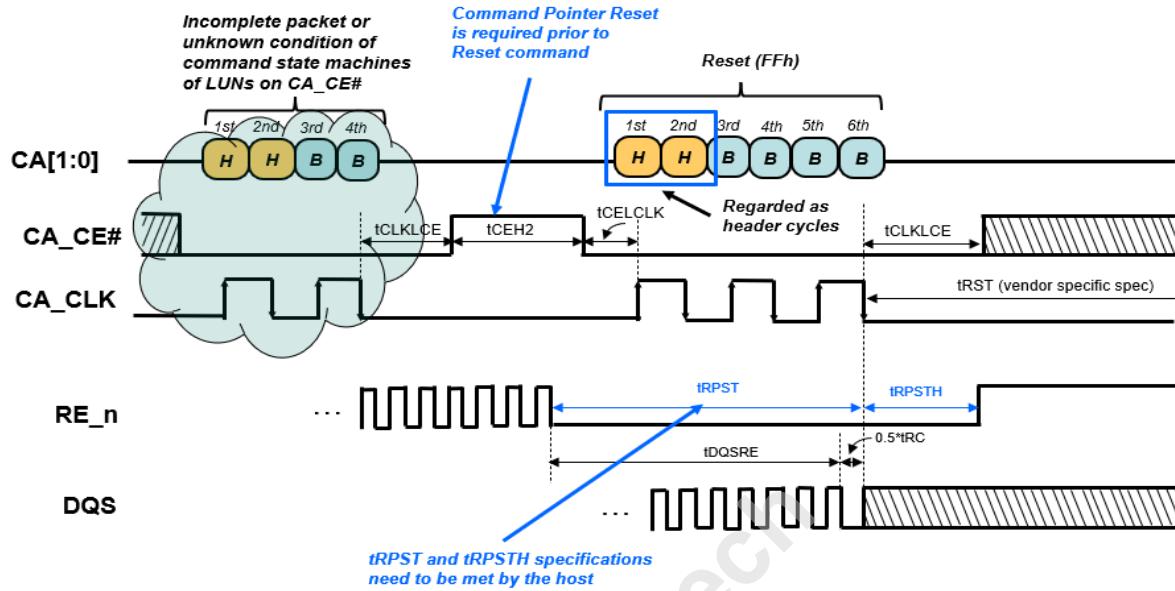


Figure 10.18-1 — Data Output Burst Interrupted by Reset (FFh) Sequence

The timings in **Figure 10.18-1** are applicable to the Reset by LUN (FAh) sequence as well, except that for Reset by LUN (FAh), the tRPST and tRPSTH specs are referenced to the last CA_CLK falling edge of the last address cycle in the Reset by LUN (FAh) sequence.

10.18.3 Reset Timing Diagrams (cont'd)

Figure 10.18-2 shows the required reset sequence and timings when a data input burst is interrupted by a Reset (FFh) command.

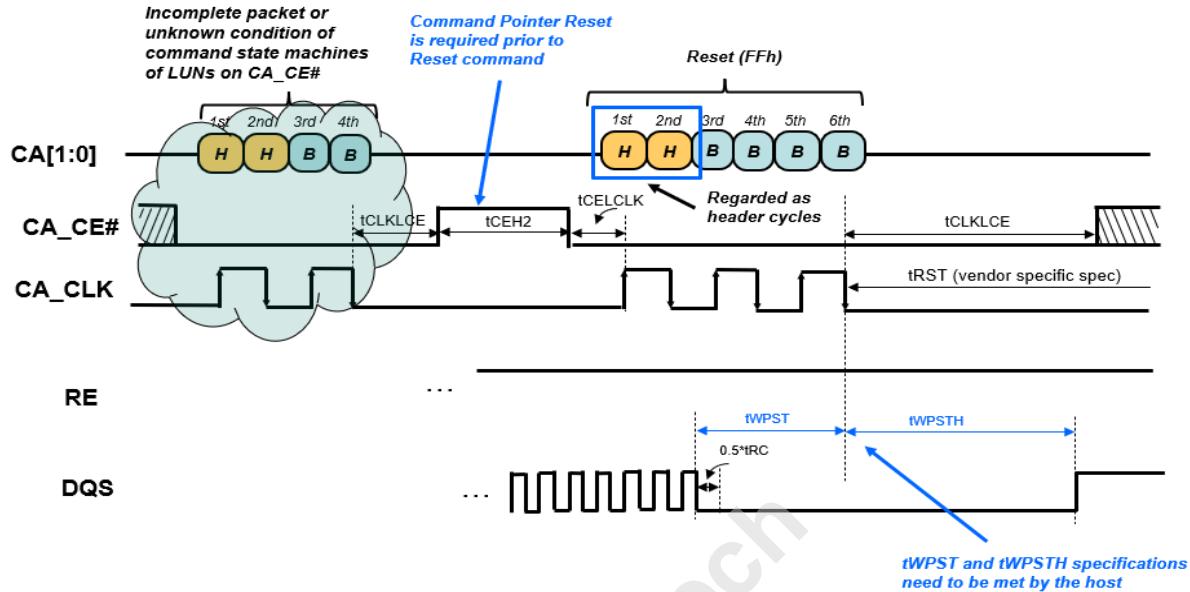


Figure 10.18-2 — Data Input Burst Interrupted by Reset (FFh) Sequence

The timings in **Figure 10.18-2** are applicable to the Reset by LUN (FAh) sequence as well, except that for Reset by LUN (FAh), the tWPST and tWPSTH specs are referenced to the last CA_CLK falling edge of the last address cycle in the Reset by LUN (FAh) sequence.

10.19 SCA CA Slew Rate Derating

When the slew rate of CA_CLK or CA[1:0] signals are < 1 V/ns, the tCACS and tCACH specs shall each be derated according to values in **Table 10.19-1**.

Table 10.19-1 — SCA Protocol CA Slew Rate Derating

		CA_CLK Input Slew Rate (V/ns)							
		1.0	0.9	0.8	0.7	0.6	0.5	0.4	0.3
CA[1] or CA[0] Input Slew Rate (V/ns)	1.0	0	28	63					
	0.9	28	56	91	136				
	0.8	63	91	126	171	231			
	0.7		136	171	216	276	360		
	0.6			231	276	336	420	546	
	0.5				360	420	504	630	840
	0.4					546	630	756	966
	0.3						840	966	1176

NOTE 1 Derating values are in picoseconds

10.20 SCA Output Driver Strength

The pull-up and pull-down impedance mismatch requirements for the SCA output driver are defined in **Table 10.20-1**. The typical pull-up and pull-down impedance of the SCA output driver is 50 ohms. Impedance mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage. The testing conditions that shall be used to verify the impedance mismatch requirements are: $V_{ccQ} = V_{ccQ}(typ)$, $SCA\ Out = V_{ccQ} \times 0.5$.

Table 10.20-1 — Pull-up and Pull-down Impedance Mismatch for SCA Output Driver

SCA Output Driver Strength	Ron = 50Ohms				Unit
	SCA Out	Max	Nom	Min	
R_SCA_CApulldown	0.5*VccQ	90.0	50.0	26.0	Ohms
R_SCA_CApullup	0.5*VccQ	90.0	50.0	26.0	Ohms
R_SCA_CApupd_mismatch	0.5*VccQ	25.0	-	-25.0	Ohms

Annex A — (Informative) Differences between Document Revisions

This table briefly describes the changes from JESD230 to JESD230G.01. If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

A.1 Differences between JESD230G.01 and JESD230G (Oct 2024)

Clause	Term and Description of Change
3.1	Under Table 3.1-1 Added "/ JESD230G.01" label to JESD230G column title. Changed JESD230G/JESD230G.01 VccQL entry from "0.6 V" to "1.2 V or 0.6 V". Changed JESD230G/JESD230G.01 "CMD/ADDR IO" entry to mention SCA protocol first.
5.4	Under BGA-316: updated ballmap, swap SCA_0, SCA_1, update typo. Updated the following labels: R/B0 to R/B0_n, R/B1 to R/B1_n, R/B2 to R/B2_n and R/B3 to R/B3_n. In Figure 5.4.2, V3 typo was fixed to CE7_3_n (from CE7_1_n).
7.7	Table 7.7-2~7.7-9 updated units and descriptions to VccQ/VccQLcondition
7.11	Typo corrected Table 7.11 'FA 27h' →'28h'
8.1.1	Minimum input slew rate is proposed for only DQS_x_t/c and RE_x_n/c.
8.6	Added as new chapter 8.6. VccQ/VccQL at Power on/off.
8.7~8.9	Previous Chapter 8.6 -8 including figures and tables renumbered to 8.7 through 8.9.
8.7.12	Added paragraph description prior to Output Pre DQ to Figure 8.7-20
8.10	Added new chapter 8.10. Progressive warmup cycle.
10.9.1	Define b[7]bit as VSP for SCE packet – Update Figure 10.9-1
10.9.2	Define b[7]bit as VSP for SCP packet – Update Figure 10.9-2
10.9.2	SCE packet issuance without SCP packet - Newly added with Figure 10.9-3
10.9.4	Define b[7]bit as VSP for SCT packet – Update Figure 10.9-4
10.9.5	Updated Figure 10.9-7,10.9-8, removed tDQSD.
10.10	Define b[7]bit as VSP for LUNSel packet – Update Figure 10.10-1, 10.10-2
10.12	Figure 10.12-2 is revised with tCDL definition. tCDL added to Table 10.17-1.
10.17	Multiple edits to Table 10.17-1: Notes column added, tCDL and tSCPSCE1 added, tCDL note added
10.20	SCA output driver pull-up and pull-down mismatch session is newly added.

A.2 Differences between JESD230G and JESD230F.01 (May 2023)

Clause	Term and Description of Change
2.6	Re-labeled clause to “Pin description (Conventional Protocol)”, removed references to Asynchronous and SDR interfaces, added VccQL. renamed VREFQ to VREFQ_DNU.
2.7	Added new clause: “Pin description (SCA Protocol)”
3.1	In NAND Interface Comparison table: removed Toggle 4.0 and ONFI 4.2 from the table and added JESD230G column, added new row for ESD.
3.2	In Supported Features and Operating Conditions Versus Data Transfer Rate table: added new column covering 3600Mbps~4800Mbps, added new row entries for PI-LTT, RDCA, Equalization (DFE), DQS Oscillator, Pausing Data Input/Output, Warm-up

A.2 Differences between JESD230G and JESD230F.01 (May 2023) (cont'd)

- cycle, Conventional protocol, SCA protocol. Updated table to show CTT and Single-Ended Signaling for DQS and RE as Not Supported. Updated table to show updated Training (Write) requirements for Host for Matched and Unmatched DQS. Added Notes to table to clarify what is meant by Optional, Supported and Required. Updated table Notes for JESD230G devices.
- 4.1.1 Removed CTT Interface AC/DC levels from clause, added PI-LTT interface AC/DC levels. Updated AC/DC levels for 3600Mbps and added AC/DC levels for 4000Mbps~4800Mbps.
- 4.1.2 Added new clause: "Input Waveform Definition"
- 4.1.3 Under NAND DQ Rx Mask Specification clause: added guidance for DQ Rx mask usage with DFE, removed CTT specifications, added PI-LTT, added 4000Mbps~4800Mbps, added diagram showing tDIHL definition.
- 4.1.4 Under Controller DQ Rx Mask Specifications clause: removed CTT, added PI-LTT, added 4000Mbps~4800Mbps requirements, updated table notes guiding usage of Controller DQ Rx Mask specifications.
- 4.1.5 Removed CTT Interface VIHL_AC requirements, updated LTT 3600Mbps VIHL_AC requirements, added LTT 4000Mbps~4800Mbps VIHL_AC requirements, added PI-LTT VIHL_AC requirements.
- 4.1.6 Under NAND Minimum Internal VrefQ Allowable Range clause: removed CTT requirements from tables, added PI-LTT requirements to tables in the clause.
- 4.2.1 Under Output Drive and ODT Strengths clause: removed CTT, updated LTT Interface Pull-Up table note that VOH,nom accuracy after ZQ calibration shall be with an RZQ of $300\text{ohm}\pm1\%$, added PI-LTT Interface drive strengths and ODT information.
- 4.2.2 Under Output Levels for Unterminated Signals clause: added PI-LTT requirements.
- 4.2.3 Under Output Timing Reference Loads clause: removed CTT requirements, broke-up Reference loads to Output Timing Reference Loads for Timing and added new Output Reference Loads for Slew Rate. Under Output Timing Reference Loads for Timing, removed 2pF capacitor from the load and updated resistor to "50ohm or Less (VSP)". Updated notes for figures
- 4.2.4 Under Single-Ended Output Slew Rate clause: added PI-LTT VOH/VOL requirements.
- 4.3 Under AC Overshoot/Uundershoot Requirements clause: added ~2000Mhz, ~2200Mhz, ~2400Mhz.
- 4.4.1 Under DC Supply Voltage clause: removed entries for 3.3v Vcc, 3.3 VccQ, 1.8v Vcc, 1.8v VccQ, updated Ipp requirement to 15mA per LUN, added VccQL requirements, updated AC Noise requirements, added new supply impedance Z(f) requirements.
- 4.4.2 Under DC Output leakage current requirements: updated clause to remove 1.8v VccQ, added VccQL, added signals to list (DBI, R/B_n, CA[1:0], RZQ), updated ILOpd and ILOpu
- 4.5 Under Absolute Maximum DC Ratings clause: removed $V_{cc} = 3.3\text{v}$ and $V_{ccQ} = 3.3\text{v}$ nominal, $V_{cc} = 3.3\text{v}$ and $V_{ccQ} = 1.8\text{v}$ nominal, $V_{cc} = 2.5\text{v}$ and $V_{ccQ} = 1.8\text{v}$ nominal, $V_{cc} = 1.8\text{v}$ and $V_{ccQ} = 1.8\text{v}$ nominal, flavors, added VccQL to table.
- 4.6 Added new clause: "Electrostatic Discharge Sensitivity Characteristics"
- 5.1 Under BGA-63: removed Asynchronous SDR ball map
- 5.2 Under BGA-100: removed Asynchronous SDR ball map
- 5.3 Removed LGA-52 ball map.
- 5.3 Under BGA-152/132/136: added SCA_0 and SCA_1
- 5.4 Under BGA-316: added SCA_0, SCA_1, VccQL

A.2 Differences between JESD230G and JESD230F.01 (May 2023) (cont'd)

- 5.5 Under BGA-272/252: added SCA_0, SCA_1, VccQL
5.6 Under BGA-178/154/146: added SCA_0, SCA_1, VccQL
6.1 Under Basic Command Definition clause: updated Change Write Column from mandatory to optional, added table notes for SCA.
6.2 Under Primary & Secondary Command Definition clause: removed ONFI or Toggle-mode heritage column, removed Primary or Secondary column, removed "Refer to Note1" from O/M column and updated O/M entries in table
7.1 Under Feature Address 02h: changed VEN (B0[0]) to Reserved, updated Interface Type B2[1:0] to remove CTT and added PI-LTT, updated description for VOH for LTT B2[6] to include PI-LTT, changed B2[7] from Reserved to VSP, added SCA_OUT(B3[0]) and SCA_DQMIRR (B3[1]).
7.3 Under Feature Address 10h: removed CTT, added note
7.5 Under Feature Address 21h: removed CTT, added PI-LTT to B0[2] description
7.6 Under Feature Address 22h: Added PI-LTT in bit descriptions, added Note 2 for bits used for SCA Non-Target ODT
7.7 Feature Address 23h: added LTT/PI-LTT description to Internal VrefQ bits, added Internal VrefQ tables for PI-LTT
7.9 Added new clause: "Feature Address 26h (DQS Oscillator)"
7.10 Added new clause: "Feature Address 27h (DFE)"
7.11 Added new clause: "Feature Address 28h (RDCA)"
7.12 Under Feature Address 40h, 41h and 42h: removed Per-Pin VrefQ VrefQ Adjustment via Absolute Setting
8.1 Under Test Conditions clause: removed CTT and added PI-LTT requirements, changed minimum input slew rate for LTT to TBD, changed output reference load to 50ohms or Less (VSP), added note to Driver strength, added table for Testing Conditions for Output Slew Rate (LTT), added table for Testing Conditions for Output Slew Rate (PI-LTT)
8.3 Under Package Electrical Specifications clause: added VccQL to introductory paragraph, added package electrical specifications for 1333MT/s to 3600MT/s and 3600MT/s to 4800MT/s, added pad capacitance specifications for 1200MT/s to 2400MT/s, 2400MT/s to 3600MT/s and 3600MT/s to 4800MT/s.
8.6.1 Under ODT Disable and Re-Enable clause: added PI-LTT, added SCA restriction on use of pin-based ODT and 1Bh/1Ch command.
8.6.2 Under Interface Initialization and Training Flows clause: update flow to remove CTT and include PI-LTT.
8.6.5 Added new clause: "Read Duty Cycle Adjustment (RDCA, Optional)"
8.6.6 Under Write DQ Training (Tx Side): removed mention of CTT optionality, updated figures in Timing De-skew of Each DQ Versus DQS sub-clause, added timing specifications for unmatched DQ-DQS receiver.
8.6.7 Under Write DQ Training (Rx Side): added PI-LTT to Write DQ Training (Rx) with Internal VrefQ Training.
8.6.11 Under Fast Set/Get Feature clause: added more registers to list of feature registers which may support Fast Set/Get Feature
8.6.12 Added new clause: "Decision Feedback Equalization (DFE)"
8.6.13 Added new clause: "DQS Oscillator"
9 Removed Parameter Page feature clause
10 Added new clause: "SCA Protocol"

A.3 Differences between JESD230F.01 and JESD230F (October 2022)

Clause	Term and Description of Change
7.8	Corrected typographical error in Table 7.8-1 — Feature Table for Write Duty Cycle Adjustment [24h]" as follows: (1) The note below Table 7.8-1 changed from B0[3:0] for WDCA Step Control to B0[4:0] for WDCA Step Control (2) I/O 4 is now part of WDCA Step Control

A.4 Differences between JESD230F and JESD230E (February 2022)

Clause	Term and Description of Change
3.1	Added JESD230F information to the NAND Interface Spec Overview
3.2	Added 2800Mbps, 3200Mbps, and 3600Mbps details to Supporting Features and Operating Conditions Versus Data Transfer Rate
4.1.1	Added 2800Mbps, 3200Mbps, and 3600Mbps details to CTT and LTT Interface AC/DC Levels
4.1.2	Added 2800Mbps, 3200Mbps, and 3600Mbps details to CTT and LTT Interface DQ Rx Mask Specification
4.1.3	Included Controller CTT and LTT Interface DQ Rx Mask Specification details
4.1.5	Added 2800Mbps, 3200Mbps, and 3600Mbps details to CTT and LTT Interface (1.2V VccQ) VIHL_AC Definition
4.1.6	Separated out a second table for the different VrefQ Value 3 setting in the Minimum Internal VrefQ Allowable Range
4.3	Updated the table for Max. overshoot and undershoot values for 1400Mhz, 1600Mhz and 1800Mhz to the CTT and LTT Interface AC Overshoot and Undershoot Specification
7.1	Updated the Feature Address 02h Register to include the option to support the Value 3 Range/Step Size
7.7.2	Updated the Feature Address 23h to include options for supporting the Value 3 Settings
7.7.2	Added an additional table to NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Value 3 Settings (1.2V VccQ)
7.8	Added a Feature Address 24h (WDCA) clause and table for Write Duty Cycle Adjustment
7.9	Added a Feature Address 40h, 41h and 42h clause with details on Per-Pin VrefQ Adjustment via Offset/Absolute Settings and accompanying tables
8.6.2	Updated the Initial Configurations Interface Training Flow diagram: Specifically details for LTT2 and LTT3 in the Low Power Interface boxes.
8.6.3	New clause and information for DCC (RE_t/c) Training Using Set Feature
8.6.7	New clause and information for Write Duty Cycle Adjustment (WDCA)
8.6.8	New clause and information for Write Training Monitor
8.6.9	New clause and information for Per-Pin VrefQ Adjustment that includes options via Offset and via Absolute Setting
8.6.10	New clause and information for Fast Set/Get Feature
9.1	Updated the Parameter Page Data Structure Definition for bytes 172-175 and 176-179 to include details for all speed grade options for both NV-DDR3 and NV-LPDDR4 speed grades
9.1	Removed bytes 178 and 179 from Reserved (updated Reserved bytes are 180-207)

A.5 Differences between JESD230E and JESD230D (June 2019)

Clause	Term and Description of Change
2.6	Added VPP and DBI pin descriptions
3	Added new NAND Interface General Information clause
4	Added new Input, Output, AC Overshoot/Uundershoot specifications for Como CTT+LTT Interface and for higher data rates up to 2.4Gbps
5	Added 178b/154b/146b Dual Channel packages. Updated 152b/132b, 252b/272b and 316b package ball maps with locations of DBI balls. Updated CE_n changes to Synchronous 132b/152b package ball maps.
7	Added Feature Address Registers 02h, 22h, 23h. Updated information for Feature Address Registers 10h and 21h.
8.6	Under Data Training clause: added ODT Disable and Re-enable sub- clause, added Interface Training Flows sub- clause, added VrefQ Training verbiage in Read DQ Training and Write DQ Training (Tx Side) sub-sections, added Write DQ Training (Rx Side) with Internal VrefQ Training sub- clause
8.7	Under Pausing Data Input/Output: added data pause requirements for >800MT/s, updated language for data burst pause versus data burst exit, updated figures
8.8	Added DBI clause
9	Parameter Page Changes for CTT (Bytes 172-175) and LTT (Bytes 176-179)
10	Added Section 10 Low Latency NAND

A.6 Differences between JESD230D and JESD230C (October 2016)

Clause	Term and Description of Change
2.6	Added ODT_x_n pin and related notes to pin description table
3.2	Added 533Mhz and 600Mhz AC Overshoot/Uundershoot Specs
3.3.1	Added 2.5 V Vcc DC Supply Voltage
3.3.2	Added 15 μ A ILOpd and ILOpu max spec for devices which support >800 MT/s
3.4	Added Absolute Maximum DC Ratings clause
4.4	Added ODT_x_n to BGA-152/132/136 ball maps
4.5	Added ODT_x_n to BGA-316 ball maps
4.6	Added ODT_x_n to BGA-272 ball maps
4.6	Added BGA-252 ball package and MO-210 reference
4.7	Corrected CE_n to RB_n mapping pin labelling error
6	Section 6 Get/Set Feature for each LUN changed to Feature Address Registers section
6.1	Moved clause 6.1 Get Feature for each LUN to clause 5.3
6.1	Added Feature Address 05h
6.2	Moved clause 6.2 Set Feature for each LUN clause to clause 5.4
6.2	Added Feature Address 20h
6.3	Added Feature Address 21h
7.1	Added 37.5 Ohms as Default Value
7.3	Added 37.5 Ohms to Nominal Driver Strength Setting
7.5	Added 533Mhz and 600Mhz tCD specs
7.7	Added Data Training clause
7.8	Added Data Input/Output Pause clause

A.6 Differences between JESD230D and JESD230C (October 2016) (cont'd)

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|------|--|
| 8.1 | Changes to Parameter Page Data Structure Bytes 6-7, 146-147, 169, 172-173
for 37.5 Ohm output driver strength and higher speed grades |
| 8.4 | Changes to Parameter Page Byte 6-7 description for WP/ODT switch functionality |
| 8.26 | Changes to Parameter Page Byte 146-147 descriptions for Toggle-mode DDR2 and
NV-DDR2 higher speed grades |
| 8.39 | Changes to Parameter Page Byte 169 description for 37.5 Ohms |
| 8.41 | Changes to Parameter Page Byte 172-173 description for Toggle-mode DDR3/4 and
NV-DDR3 higher speed grades |

A.7 Differences between JESD230C and JESD230B (July 2014)

Clause	Term and Description of Change
2.6	Pin Description
3	Physical Interface
3.3	Recommended DC Operating Conditions
4.7	CE_n to R/B_n Mapping
7	Data Interface and Timing (New Chapter)
7.1	Test Condition
7.4	Package Electrical Specifications and Pad Capacitance
7.5	tCD Parameter
7.6	Additional Timing Parameter for I/O Speed Greater than 400 MT/s

A.8 Differences between JESD230B and JESD230A (August 2013)

Clause	Description of change
2	VccQ added
6	ZQ calibration added
7	Driver strength added
8.1.38	Driver strength support description changes in Byte 169 of the parameter page

A.9 Differences between JESD230A and JESD230 (October 2012)

Clause	Description of change
2.5	New BGA-316 (Quad x8) package added
2.6	New BGA-272 (Quad x8) package added
5	Parameter page, revision 1 added

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Standard Improvement Form

JEDEC Standard No. JESD230G.01

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

Requirement, clause number _____

Test method number _____ Clause number _____

The referenced clause number has proven to be:

Unclear Too Rigid In Error

Other _____

2. Recommendations for correction:

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