Homework 3
Design for Testability with DFT Compiler and TetraMAX

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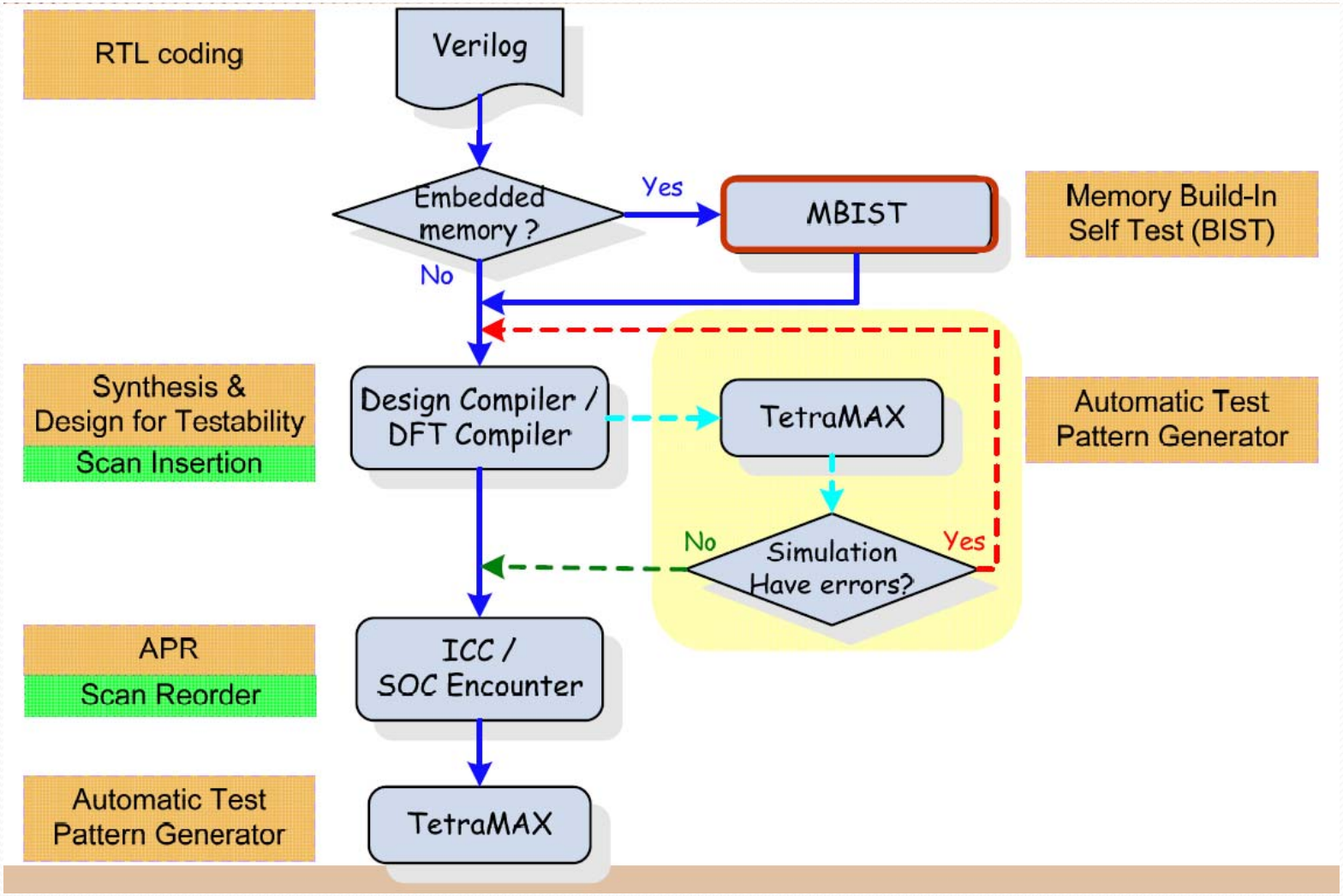
Outline

- DFT Concept
- TetraMAX Overview

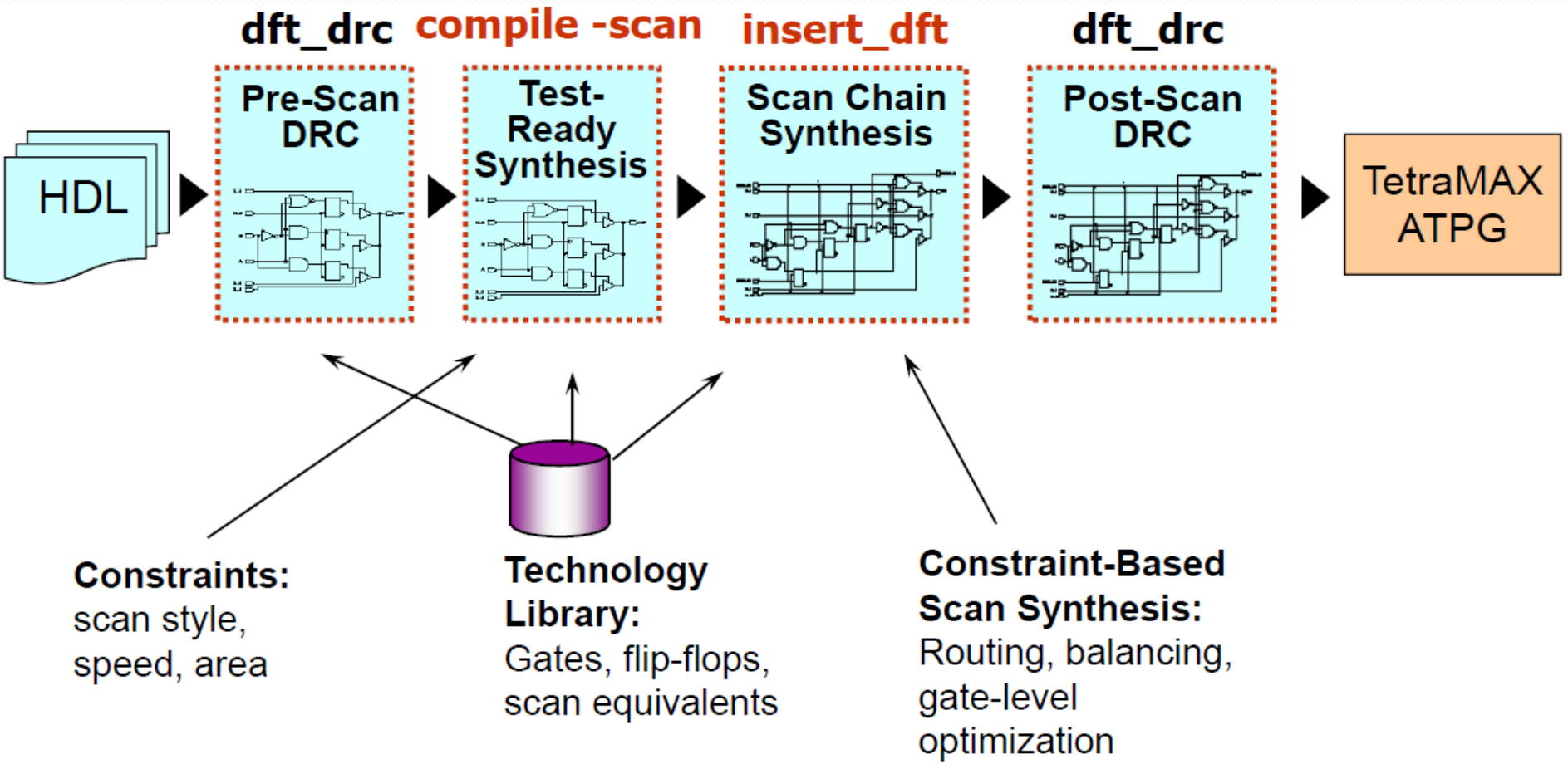
DFT Concept

- Design For Testability
- What is Testing
  - Testing is a process of determining whether a device is good (function correctly) or not.
  - Testing includes test pattern generation, application and output evaluation.
- Why testing?
  - In order to guarantee the product quality, reliability, performances, etc.
  - Cost is the most important.

Test Circuit Design Flow



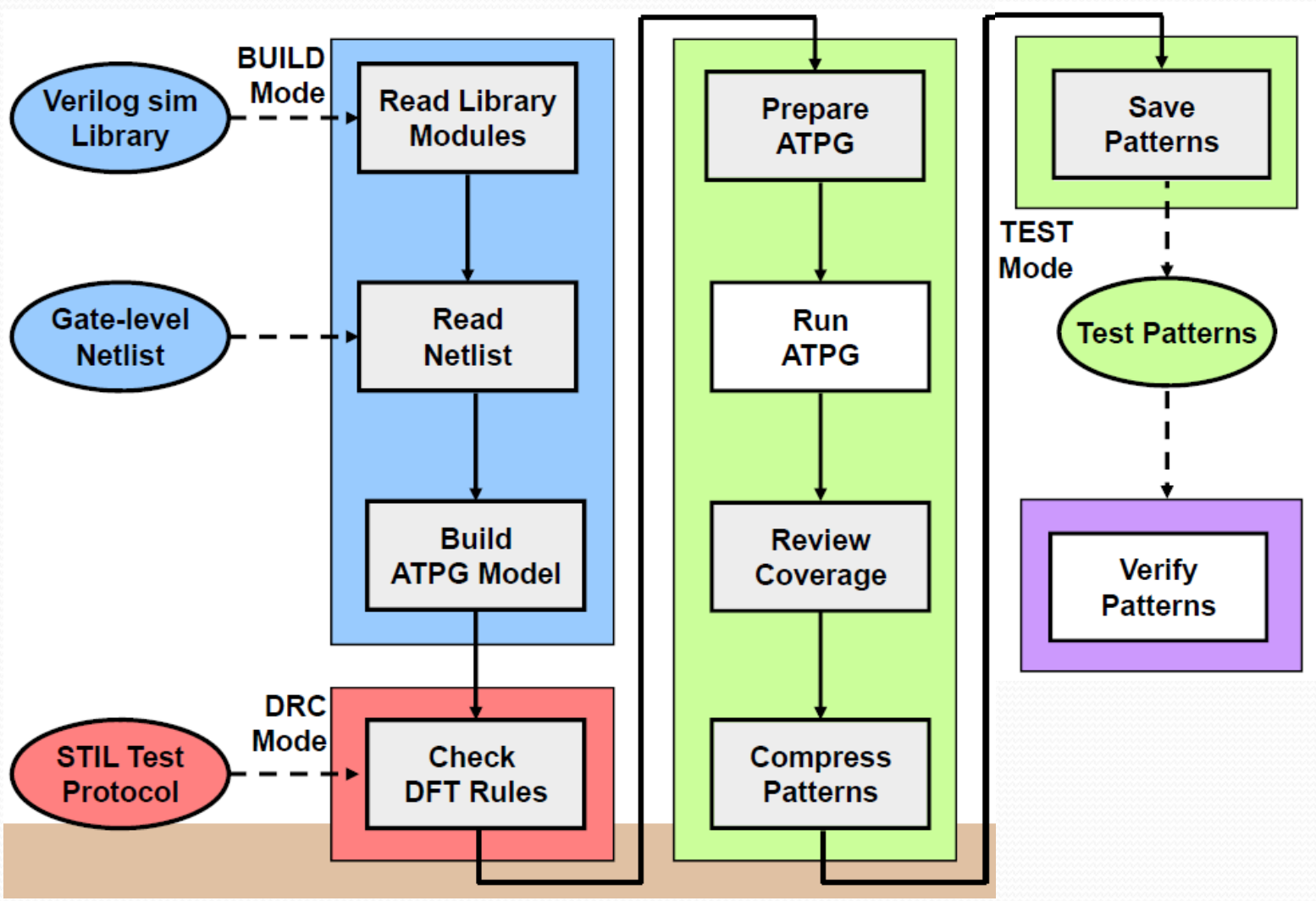
Overview of DFT Compiler Flow



Automatic Test Pattern Generator(ATPG)

- Generate the test patterns for target fault model and keep the number of test pattern as small as possible.
- We will use Synopsys **Tetramax** EDA tool to automatically generate test pattern.
- Besides, “fault coverage” of the testing circuits can also be estimated.

ATPG Flow in TetraMAX

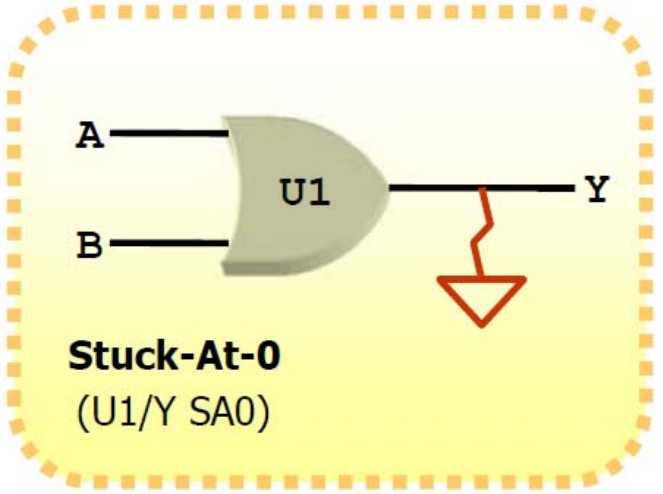


TetraMAX ATPG Command Modes

- BUILD mode:
  - Initial mode
  - Read in design, libraries, models
  - Construct ATPG simulation model in preparation for DRCs
- DRC mode:
  - Testability Design Rule Checks (DRCs) are performed
  - Successful conclusion of DRCs sets mode to “TEST”
- TEST mode:
  - ATPG, Fault Simulation, Fault Diagnosis are performed
  - Test program files, simulation testbenches, etc. written out

Test Pattern Generation

- $T_{A/0}$={10}, $T_{A/1}$={00}
- $T_{B/0}$={01}, $T_{B/1}$={00}
- $T_{Y/0}$={01}or{10}or{11},$T_{Y/1}$={00}
- T= {00,01,10}

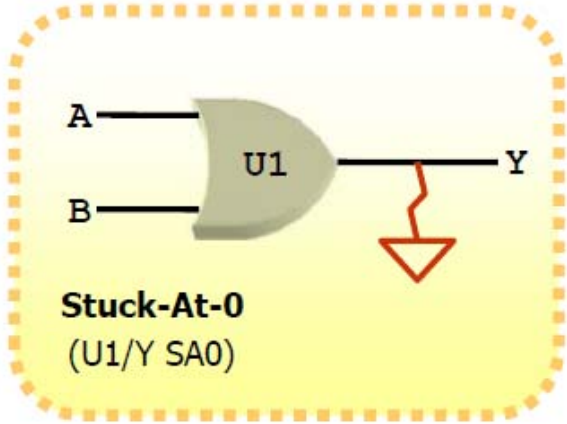


A	B	Y	Y(A/0)	Y(A/1)	Y(B/0)	Y(B/1)	Y(Y/0)	Y(Y/1)
0	0	0	0	**1**	0	**1**	0	**1**
0	1	1	1	1	**0**	1	**0**	1
1	0	1	**0**	1	1	1	**0**	1
1	1	1	1	1	1	1	**0**	1

Fault Coverage

- **Fault coverage** (FC) is the measure of the ability of a test set to detect a given class of faults that may occur on the device under test (DUT).

$$FC = \frac{\text{\# faults detected}}{\text{\# faults in fault list}}$$



Test Pattern (A,B)	Faults Detected	Fault Coverage
{(0,0)}	A/1, B/1, Y/1	3/6= 50%
{(0,1)}	B/0, Y/0	2/6=33.33%
{(1,1)}	Y/0	1/6=16.67%
{(0,0),(0,1),(1,1)}	all	6/6= 100%

Lab

- Objective
  - Understand the baseline DFT Compiler flow.
  - Learn how to use TrtraMAX after we generated the STIL procedure file and synthesized netlist from DFT Compiler.

Getting Start

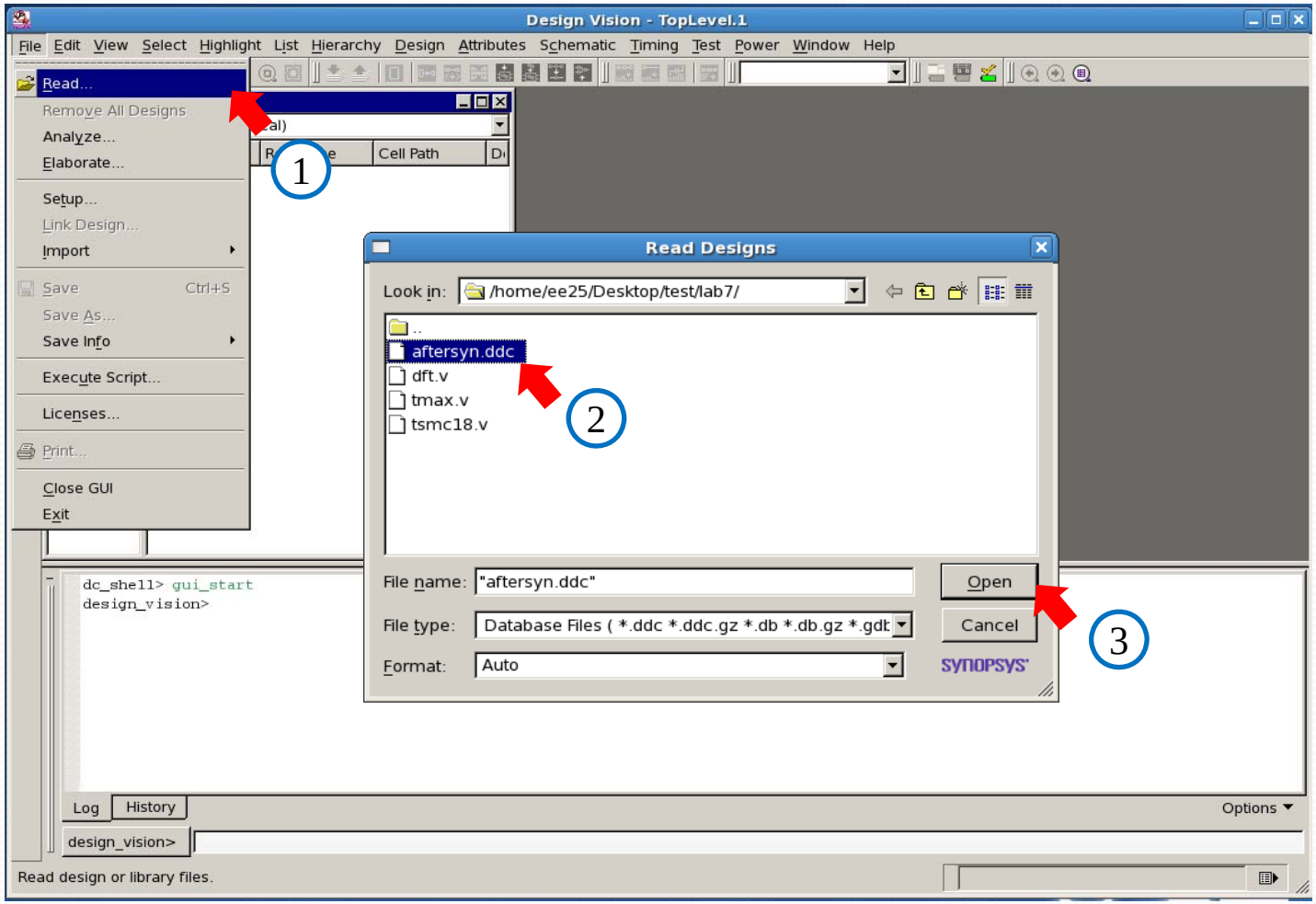
- Enter the directory (open terminal)
  - cd electronic_circuit_102

```
[t101418095@islabx6 ~]$ cd electronic_circuit_102
```

- Copy files
  - cp -r /home/standard/electronic_circuit_102/lab7 .
- Enter the directory
  - cd lab7
- Invoke the Design Vision XG mode
  - dv

Read Design

- Read files



DFT Compiler Flow(1/5)

- Create test protocol and Perform pre-DFT DRC

```
design_vision> create_port -dir in SCAN_IN
```

  - create_port -dir in SCAN_IN
  - create_port -dir out SCAN_OUT
  - create_port -dir in SCAN_EN
  - set_dft_signal -view exist -type ScanClock -timing {45 55} -port clock
  - set_dft_signal -view exist -type Reset -active_state 1 -port reset
  - create_test_protocol
  - dft_drc

DFT Compiler Flow(2/5)

- Perform Test-Ready Compile
  - compile -scan -map_effort high -area_effort high -boundary_optimization

DFT Compiler Flow(3/5)

- Specify test components
  - set_scan_configuration -chain_count 1 -clock_mixing mix_clocks_not_edges -internal_clocks single -add_lockup false
  - set_dft_signal -view spec -port SCAN_IN -type ScanDataIn
  - set_dft_signal -view spec -port SCAN_OUT -type ScanDataOut
  - set_dft_signal -view spec -port SCAN_EN -type ScanEnable -active_state 1
  - set_scan_path chain1 -scan_data_in SCAN_IN -scan_data_out SCAN_OUT

DFT Compiler Flow(4/5)

- Preview the scan synthesis, if it is ok, then insert scan.
  - preview_dft -show all
  - insert_dft

DFT Compiler Flow(5/5)

- Check scan rules after scan inserting and report the result.
  - dft_drc -coverage_estimate

  What was the test coverage reported? _____ %
- How many scan chains did you get? _____
  - report_scan_path -view existing_dft -chain all
- How many flip-flops are in each chain? _____
  - report_scan_path -view existing_dft -cell all

Save File For TrtraMAX

- Save synthesized netlist & STIL procedure file
  - write -format verilog -hier -out chip_scan.vg
  - write_test_protocol -out chip_scan.spf
- Now you can close Design Vision

Open TetraMAX

- Invoke TetraMAX
  - tmax &
- Set messages
  - set_messages -log chip.log -replace

```
BUILD-T> set_messages -log chip.log -replace
```

TetraMAX(1/3)

- Read in library and netlist file
  - read_netlist tsmc18.v
  - read_netlist chip_scan.vg
- Build the fault simulation model
  - run_build_model alu

TetraMAX(2/3)

- Run design rule checking using STIL procedure file
  - set_rules C4 ignore
  - run_drc chip_scan.spf
- Add fault list
  - add_faults -all

TetraMAX(3/3)

- Run ATPG
  - set_pat -internal
  - run_atpg –auto
  - set_faults -fault_coverage
  - set_faults -summary verbose
  - report_summaries
- How many patterns needed? _____
- What is the total fault count? _____
- What is the test coverage? _____ %
- What is the fault coverage?_____ %

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT       1130
  detected_by_simulation         DS      (1060)
  detected_by_implication        DI        (70)
Possibly detected                PT          0
Undetectable                     UD          7
  undetectable-redundant         UR        (7)
ATPG untestable                  AU          5
  atpg_untestable-not_detected   AN        (5)
Not detected                     ND          0
-----------------------------------------------
total faults
test coverage
fault coverage
-----------------------------------------------
          Pattern Summary Report
-----------------------------------------------
#internal patterns
    #basic_scan patterns
-----------------------------------------------
```

Answer

Thanks for your attention.

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