呂彥旻

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一、 實驗名稱

Auto Placement Routing with Innovus (APR)

二、 模擬解果與分析 (附圖)

pre-CTS Timing Analysis 圖

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Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.010  |  4.204  |  0.010  |  0.043  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   36    |    8    |   19    |    9    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-----------------------------+------------------+
|                |             Real            |       Total      |
|    DRVs        +-----------------+-----------+------------------|
|                |  Nr nets(terms) | Worst Vio |  Nr nets(terms)  |
+----------------+-----------------+-----------+------------------+
|   max_cap      |      0 (0)      |   0.000   |      0 (0)       |
|   max_tran     |      0 (0)      |   0.000   |     21 (21)      |
|   max_fanout   |      0 (0)      |     0     |     21 (21)      |
|   max_length   |      0 (0)      |     0     |      0 (0)       |
+----------------+-----------------+-----------+------------------+
```

post-CTS Timing Analysis 圖

```
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+--------
-+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default
 |
+--------------------+---------+---------+---------+---------+---------+--------
-+
|           WNS (ns):|  0.011  |  4.204  |  0.011  |  0.043  |   N/A   |  0.000
 |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000
 |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0
 |
|          All Paths:|   36    |    8    |   19    |    9    |   N/A   |    0
 |
+--------------------+---------+---------+---------+---------+---------+--------
-+

+----------------+-------------------------------+------------------+
```

post-route Timing Analysis 圖

```
vlsi_54@islabx6:~
檔案(F)  編輯(E)  檢視(V)  搜尋(S)  終端機(T)  求助(H)
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          timeDesign Summary
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Hold  views included:
 av_func_mode_min

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.003  |  0.184  |  0.003  |  1.594  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   36    |    8    |   19    |    9    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density:  4.463%
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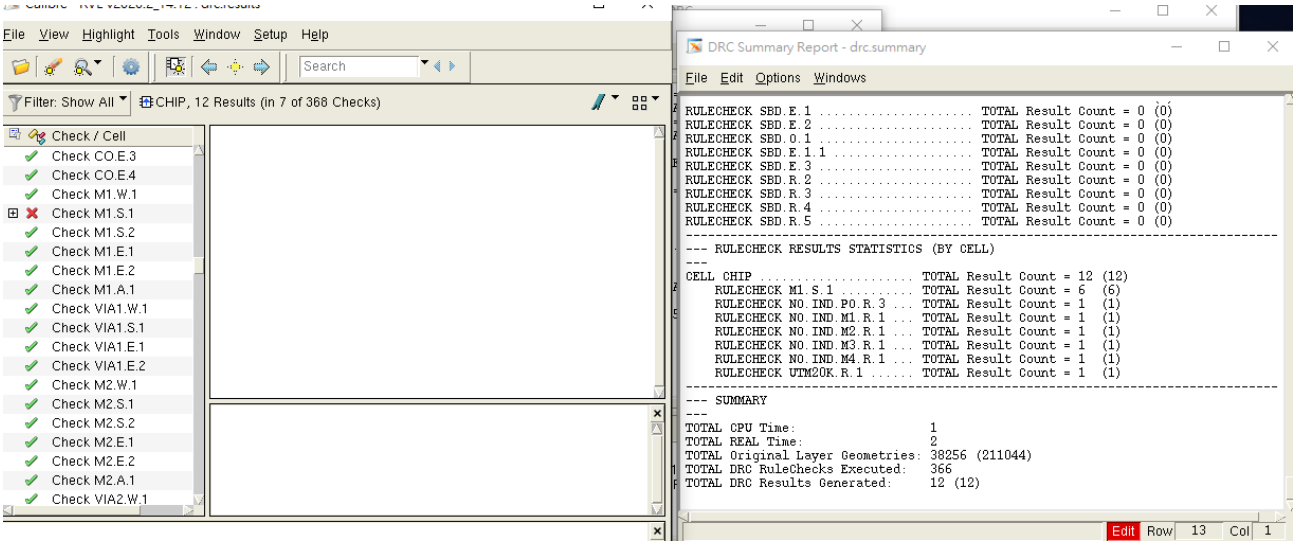
Reported timing to dir timingReports
Total CPU time:  1.88 sec
Total Real time:  2.0 sec
Total Memory Usage:  1283.75 Mbytes
Reset AAE Options
```

DRC 結果圖:



LVS 結果圖: