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一、實驗名稱

Logic Synthesis with Design Compiler

二、實驗目的

使用 Design Vision compiler

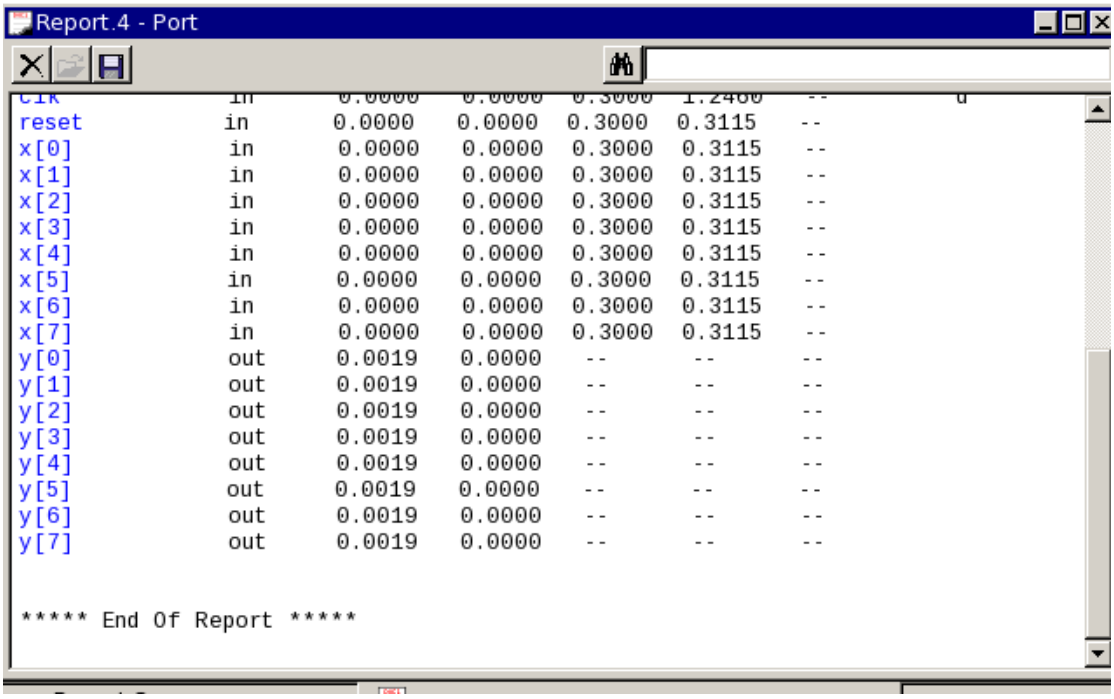
三、實驗過程

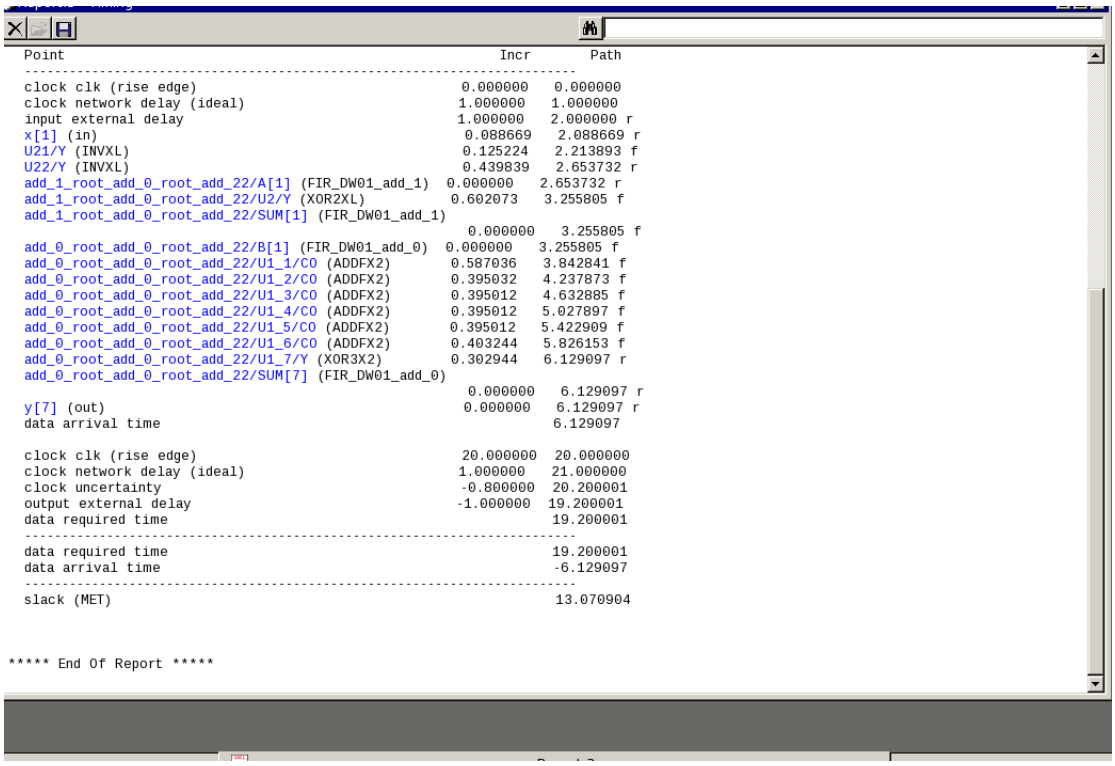
依照講義的操作步驟

四、程式撰寫

依照講義的程式碼

五、模擬解果與分析 (附圖)

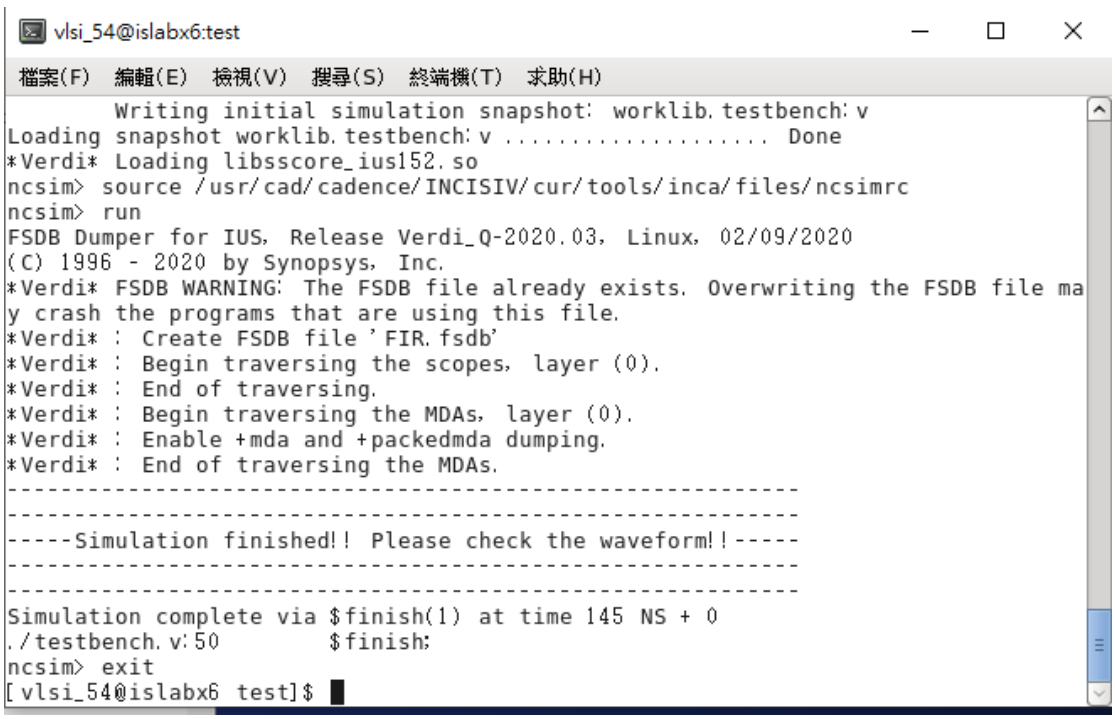




```
  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock clk (rise edge)                                 0.000000   0.000000
  clock network delay (ideal)                           1.000000   1.000000
  input external delay                                  1.000000   2.000000 r
  x[1] (in)                                             0.088669   2.088669 r
  U21/Y (INVXL)                                         0.125224   2.213893 f
  U22/Y (INVXL)                                         0.439839   2.653732 r
  add_1_root_add_0_root_add_22/A[1] (FIR_DW01_add_1)  0.000000   2.653732 r
  add_1_root_add_0_root_add_22/U2/Y (XOR2XL)            0.602073   3.255805 f
  add_1_root_add_0_root_add_22/SUM[1] (FIR_DW01_add_1)
                                                        0.000000   3.255805 f
  add_0_root_add_0_root_add_22/B[1] (FIR_DW01_add_0)  0.000000   3.255805 f
  add_0_root_add_0_root_add_22/U1_1/CO (ADDFX2)         0.587036   3.842841 f
  add_0_root_add_0_root_add_22/U1_2/CO (ADDFX2)         0.395032   4.237873 f
  add_0_root_add_0_root_add_22/U1_3/CO (ADDFX2)         0.395012   4.632885 f
  add_0_root_add_0_root_add_22/U1_4/CO (ADDFX2)         0.395012   5.027897 f
  add_0_root_add_0_root_add_22/U1_5/CO (ADDFX2)         0.395012   5.422909 f
  add_0_root_add_0_root_add_22/U1_6/CO (ADDFX2)         0.403244   5.826153 f
  add_0_root_add_0_root_add_22/U1_7/Y (XOR3X2)          0.302944   6.129097 r
  add_0_root_add_0_root_add_22/SUM[7] (FIR_DW01_add_0)
                                                        0.000000   6.129097 r
  y[7] (out)                                            0.000000   6.129097 r
  data arrival time                                                6.129097

  clock clk (rise edge)                                20.000000  20.000000
  clock network delay (ideal)                           1.000000   21.000000
  clock uncertainty                                    -0.800000  20.200001
  output external delay                                -1.000000  19.200001
  data required time                                               19.200001
  ------------------------------------------------------------------------
  data required time                                               19.200001
  data arrival time                                                -6.129097
  ------------------------------------------------------------------------
  slack (MET)                                                      13.070904


***** End Of Report *****
```



```
vlsi_54@islabx6:test
檔案(F)  編輯(E)  檢視(V)  搜尋(S)  終端機(T)  求助(H)
        Writing initial simulation snapshot: worklib.testbench:v
Loading snapshot worklib.testbench:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi_Q-2020.03, Linux, 02/09/2020
(C) 1996 - 2020 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file ma
y crash the programs that are using this file.
*Verdi* : Create FSDB file 'FIR.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
*Verdi* : Begin traversing the MDAs, layer (0).
*Verdi* : Enable +mda and +packedmda dumping.
*Verdi* : End of traversing the MDAs.
----------------------------------------------------------
----------------------------------------------------------
-----Simulation finished!! Please check the waveform!!-----
----------------------------------------------------------
----------------------------------------------------------
Simulation complete via $finish(1) at time 145 NS + 0
./testbench.v:50        $finish;
ncsim> exit
[vlsi_54@islabx6 test]$
```

六、心得

這次的作業比較簡單，只需要跟著步驟做就會成功。但是其中有很多需要去理解的東西，比如頻率設定或是線路寬度等，都需要仔細摸索才會有更深入的了解。整個過程雖然簡單，是因為這是較小的設計，如果遇到較大的設計模式就需要了解全部的過程。