

呂彥旻

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一、 實驗名稱

Auto Placement Routing with Innovus (APR)

二、 模擬解果與分析 (附圖)

pre-CTS Timing Analysis 圖

Setup views included: av_func_mode_max						
Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.010	4.204	0.010	0.043	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	36	8	19	9	N/A	0

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	21 (21)
max_fanout	0 (0)	0	21 (21)
max_length	0 (0)	0	0 (0)

post-CTS Timing Analysis 圖

timeDesign Summary

Setup views included:
av_func_mode_max

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.011	4.204	0.011	0.043	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	36	8	19	9	N/A	0

post-route Timing Analysis 圖

vlsi_54@islabx6:~

檔案(F) 編輯(E) 檢視(V) 搜尋(S) 終端機(T) 求助(H)

timeDesign Summary

Hold views included:
av_func_mode_min

Hold mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.003	0.184	0.003	1.594	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	36	8	19	9	N/A	0

Density: 4.463%

Reported timing to dir timingReports
Total CPU time: 1.88 sec
Total Real time: 2.0 sec
Total Memory Usage: 1283.75 Mbytes
Reset AAE Options

DRC 結果圖:

The screenshot displays the Calibre DRC interface. On the left, a list of checks is shown under the 'Filter: Show All' tab, with 'CHIP, 12 Results (in 7 of 368 Checks)' selected. The checks include CO.E.3, CO.E.4, M1.W.1, M1.S.1, M1.S.2, M1.E.1, M1.E.2, M1.A.1, VIA1.W.1, VIA1.S.1, VIA1.E.1, VIA1.E.2, M2.W.1, M2.S.1, M2.S.2, M2.E.1, M2.E.2, M2.A.1, and VIA2.W.1. On the right, the 'DRC Summary Report - drc.summary' window is open, showing a table of rule check results and a summary section.

Rule Check	TOTAL Result Count
RULECHECK SED.E.1	0 (0)
RULECHECK SED.E.2	0 (0)
RULECHECK SED.O.1	0 (0)
RULECHECK SED.E.1.1	0 (0)
RULECHECK SED.E.3	0 (0)
RULECHECK SED.R.2	0 (0)
RULECHECK SED.R.3	0 (0)
RULECHECK SED.R.4	0 (0)
RULECHECK SED.R.5	0 (0)

--- RULECHECK RESULTS STATISTICS (BY CELL) ---

Cell	TOTAL Result Count
CHIP	12 (12)

--- SUMMARY ---

TOTAL CPU Time:	1
TOTAL REAL Time:	2
TOTAL Original Layer Geometries:	38256 (211044)
TOTAL DRC RuleChecks Executed:	366
TOTAL DRC Results Generated:	12 (12)

LVS 結果圖:

```
SOURCE NAME:      source.spi ('CHIP')
RULE FILE:         Calibre.lvs
HCELL FILE:        (-automatch)
CREATION TIME:     Mon Dec 13 18:29:37 2021
CURRENT DIRECTORY: /home/vlsi_54/APR/LVS
USER NAME:         vlsi_54
CALIBRE VERSION:   v2020.2_14.12   Thu Apr 2 15:39:27 PDT 2020
```

OVERALL COMPARISON RESULTS

```

#          #####
#          #          #          *  *
#          #          #          CORRECT
##         #          #          \_/_
#          #####
```

Warning: Ambiguity points were found and resolved arbitrarily.
Warning: Source and layout refer to the same data.