

Sequential circuit is broadly classified into two types

- 1) Synchronous sequential circuit
- 2) Asynchronous sequential circuit.

Synchronous Sequential Circuit:-

A Synchronous Sequential Circuit is a system whose behaviour can be defined from the knowledge of its signal at discrete instants of time.

The behaviour of an asynchronous sequential circuit depends upon the order in which its input signals change and can be affected at any instant of time.

Synchronization is achieved by a timing device called a 'master clock generator' which generates a periodic train of clock pulses.

The memory elements used in clock sequential circuit are called flip-flops.

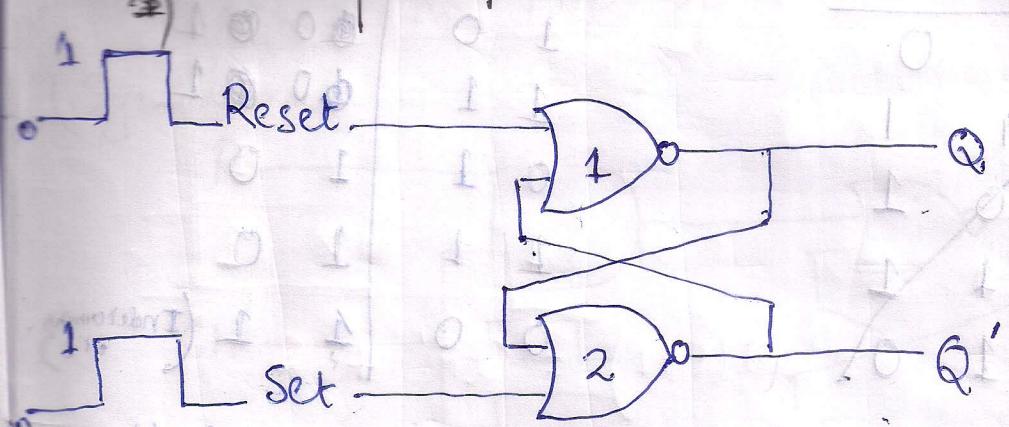
\* Flip-flop:-

The Flip flops are binary cells capable of storing only one-bit of information.

A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the bits stored in it.

A flip-flop can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

## Basic flip-flop circuit :-



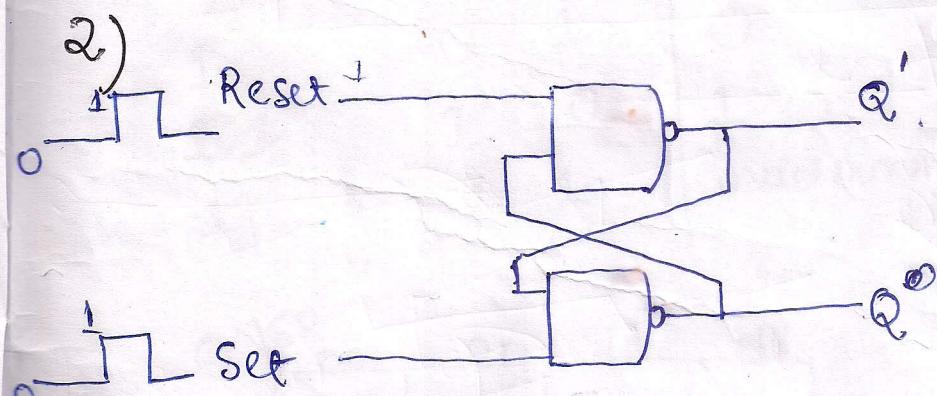
Ques: Difference between Latch and flip flop

This flip flop is known as direct couple RS flip-flop or SR Latch.

S	R	Q	$Q'$
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
0	0	0	1
1	1	0	0 (Indeterministic)

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table  
of NOR  
GATE



S	R	Q	$Q'$
1	0	1	0
0	0	1	1
0	1	0	1
1	1	0	1

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

S	R	Q	$Q'$
1	0	1	0
0	0	1	1
0	1	0	1
0	0	1	1
1	1	1	0

S	R	Q	$Q'$
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

A The NAND basic flip flop circuit operates with both inputs normally at 1 unless the state of the flip flop has to be changed. The application of a momentary 0 to the set input causes output  $Q$  to go to 1 and  $Q'$  to go to 0 thus putting the flip flop into the set state. After the set input returns to 1, a momentary 0 to the reset input causes a transition to the clear state. When both inputs go to 0, both outputs go to 1, a condition to be avoided in normal flip-flop operation.

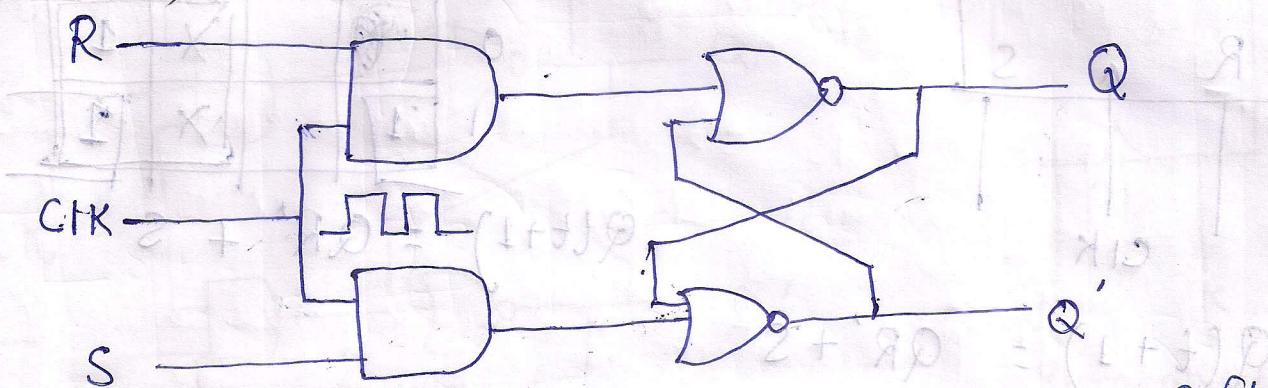
S	R	Q	$Q'$
1	0	0	1
1	1	0	1
1	0	1	0
0	1	1	0

S	R	Q	$Q'$	2
0	1	0	1	
1	1	0	0	
1	0	0	1	
0	0	1	1	

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## Clocked RS - Flipflop :-

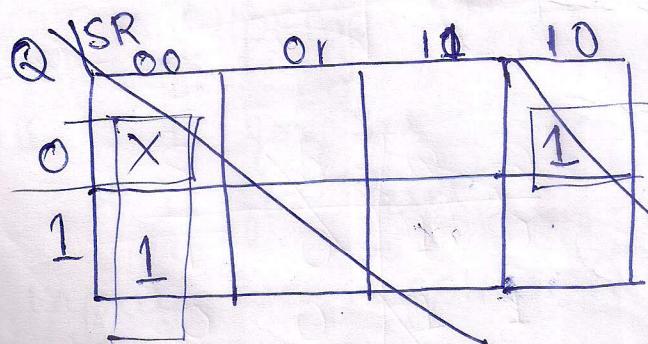
(Synchronous)



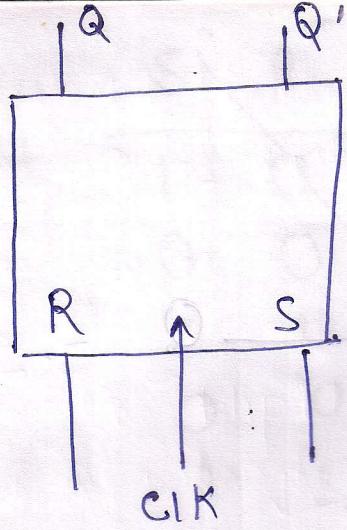
The clocked RS-Flipflop consists of a basic NOR flipflop and two AND gates. The outputs of the AND gates remain at 0 as long as the clock pulse is 0, regardless of S and R input values.

S and R input values

Present state $Q$	S	R	Next state $Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterministic
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate



$$Q(t+1) = \overline{S}\overline{R} + \overline{Q}\overline{R} + Q\overline{S}$$

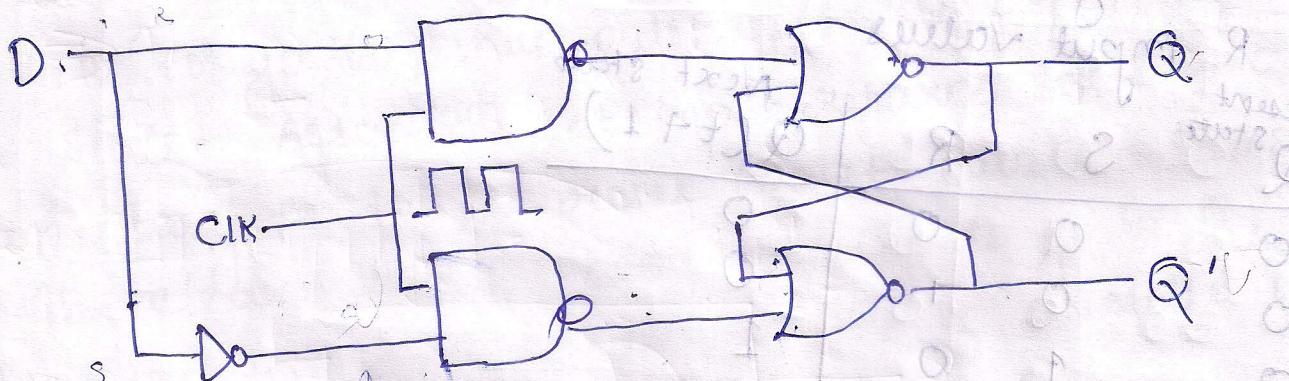


Q	S	R	Q'	10
0	0	0	1	1
1	1	1	0	0

$$Q(t+1) = QR' + S$$

$$Q(t+1) = QR' + S$$

## D Flip-flop:



characteristic table

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1
1	1	1

Q	R	S
0	0	1
0	1	0
1	0	0
1	1	0

Q	R	S	Q(t+1)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	1

$$= A'B + B'A \quad 0B0 + B0 = (1-t)B$$