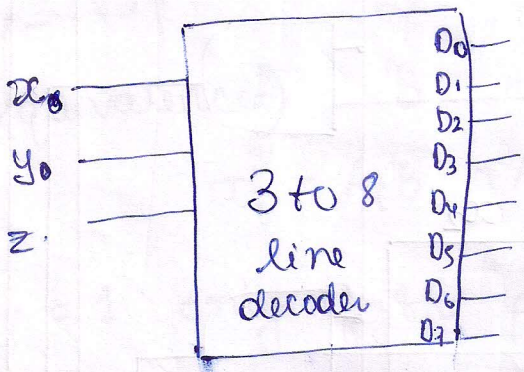
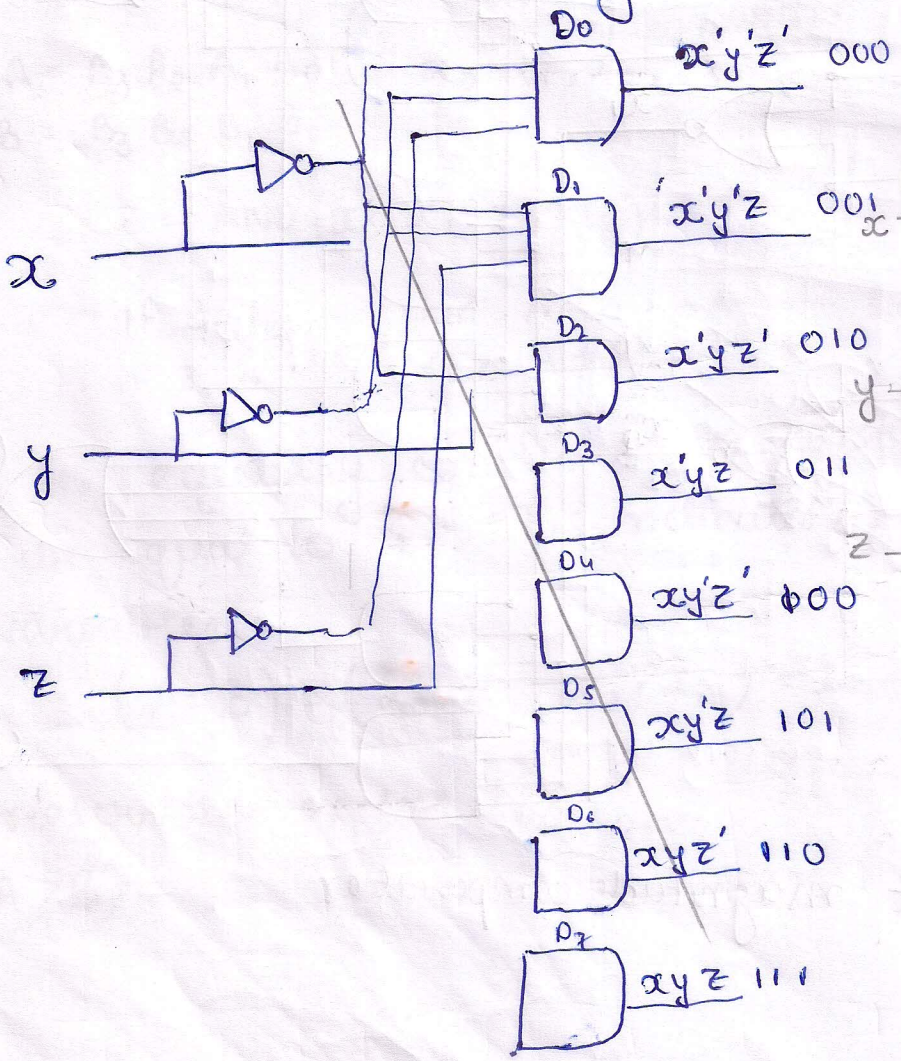
Decoders :-

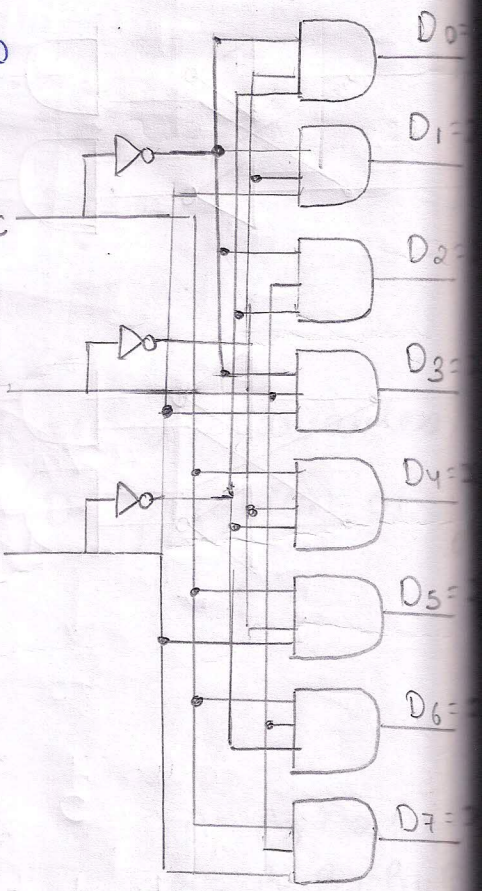
The decoder is a combinational circuit that conver binary information from n input lines to a maxim of 2^n unique output lines. The decoders here are called n-to-m line decoders where $m \leq 2^n$

3 to 8 line decoder —



Block Diagram





A 3-to-8 line decoder

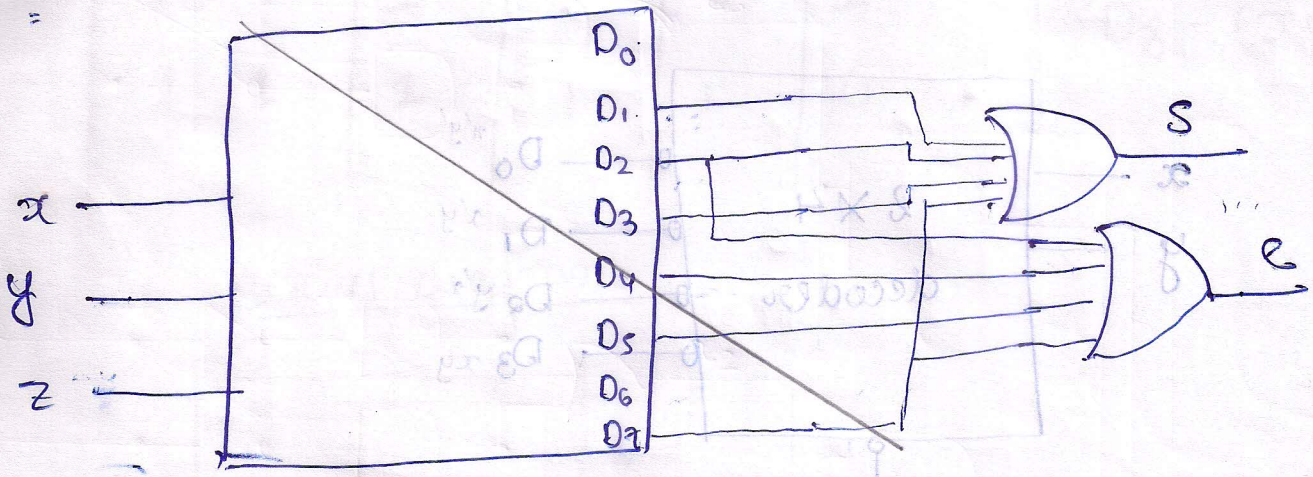
Que:- Implement a full adder circuit with a decoder and two OR gates

$S = x \oplus y \oplus z$

$= x'y'z + x'yz' + xy'z' + xyz$

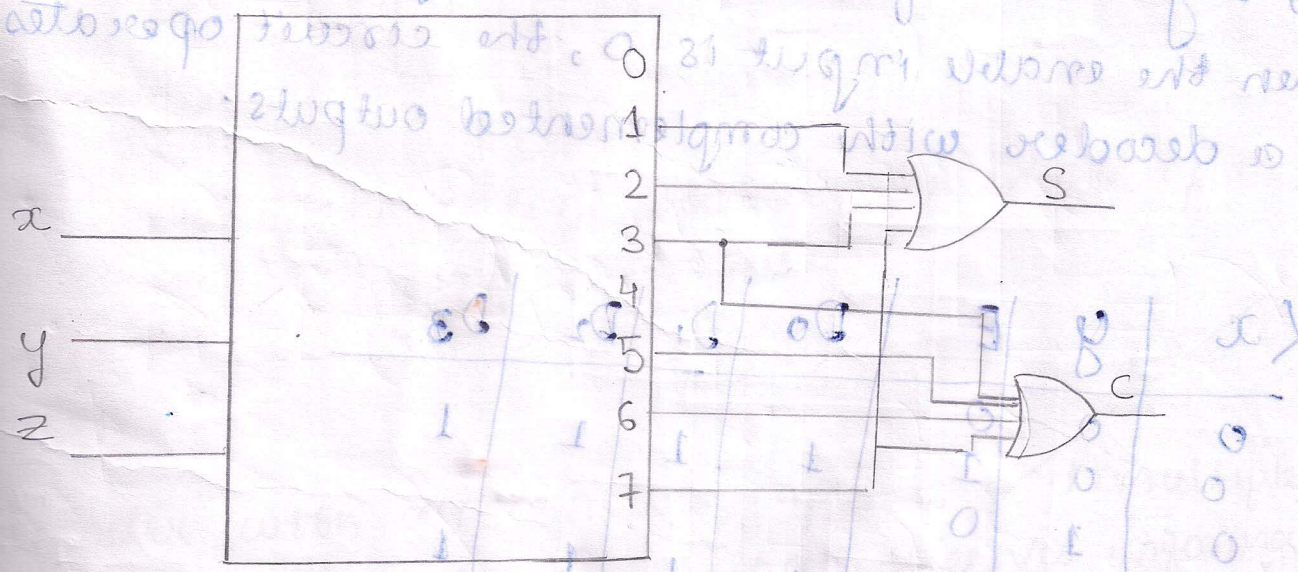
$C = xy + yz + xz$

$= x'yz + xy'z + xyz' + xyz$



$S = x \oplus y \oplus z = \Sigma(1, 2, 3, 7)$

$C = xy + yz + xz = \Sigma(3, 5, 6, 7)$

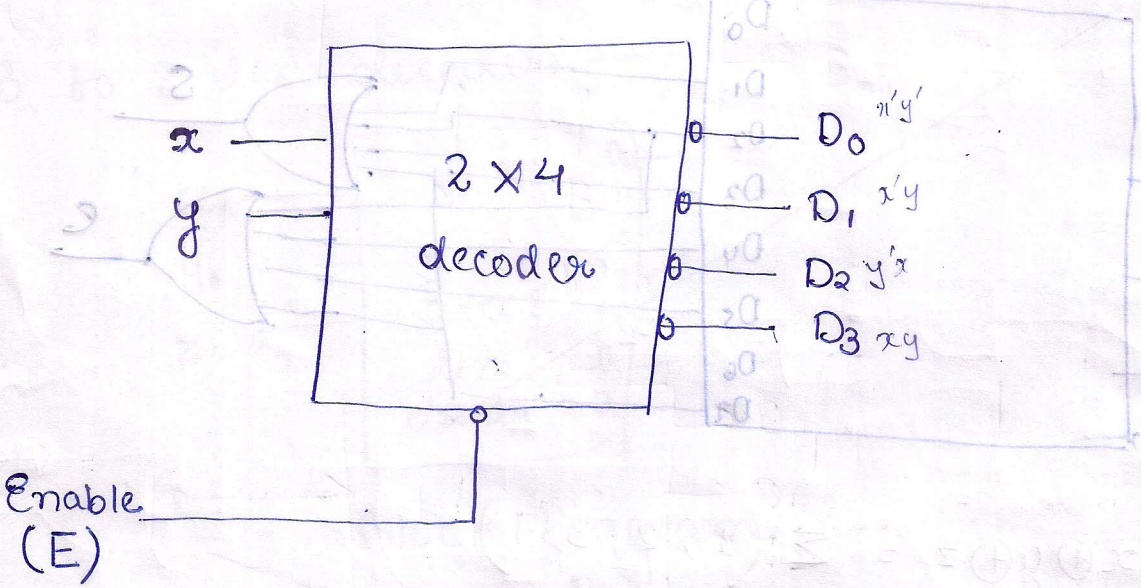


Implementation of a full-adder with a decoder

De-Multiplexer (demux) :-

Decoders include one or more enable inputs to control the circuit operation.

2 to 4 decoder with enable input.



Here all the outputs are equal to 1 if enable input is 1, regardless of the values of inputs x and y. When the enable input is 0, the circuit operates as a decoder with complemented outputs.

x	y	E	D0	D1	D2	D3
0	0	0				
0	0	1	1	1	1	1
0	1	0				
0	1	1	1	1	1	1
1	0	0				
1	0	1	1	1	1	1
1	1	0				
1	1	1	1	1	1	1

E	X	Y	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

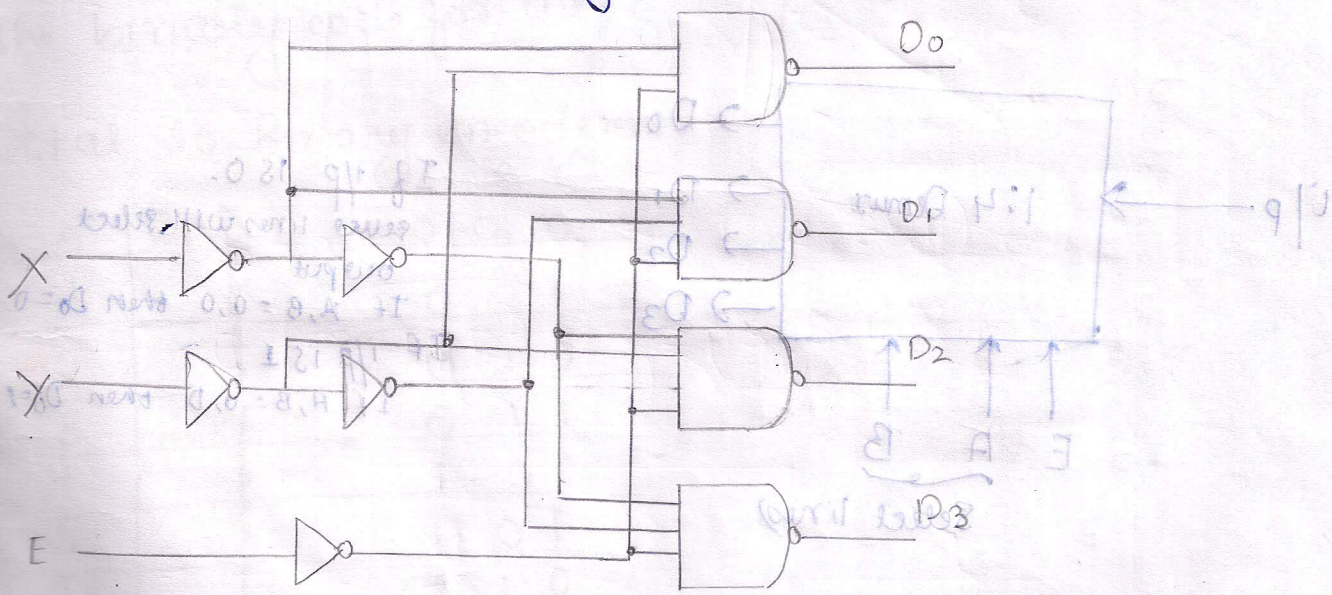
$D_0 = (x'y')'$

$D_1 = (x'y)'$

$D_2 = (xy')'$

$D_3 = (xy)'$

Circuit diagram



A 2-to-4 line decoder with enable input

A decoder with an enable input is a demultiplexer. A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of a specific output line is controlled by the bit values of n selection lines.