

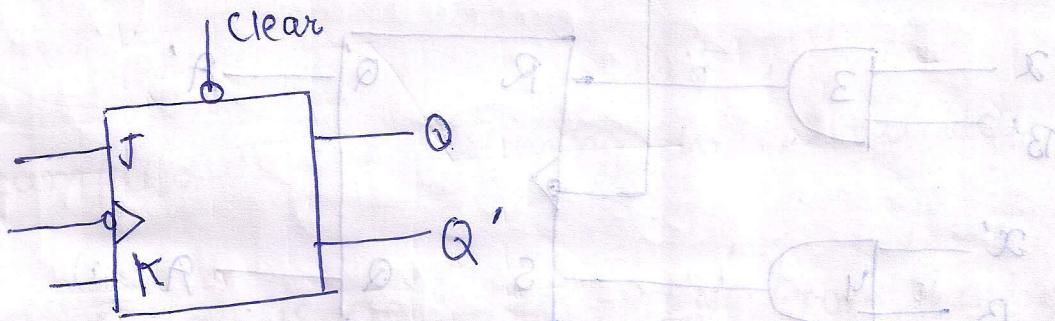
23/04/2015

To set or clear flip flop asynchronously  
Some flip flops have direct inputs usually called direct set or direct clear.

This inputs are needed to bring the flip flops to a known initial state before the normal clock operation.

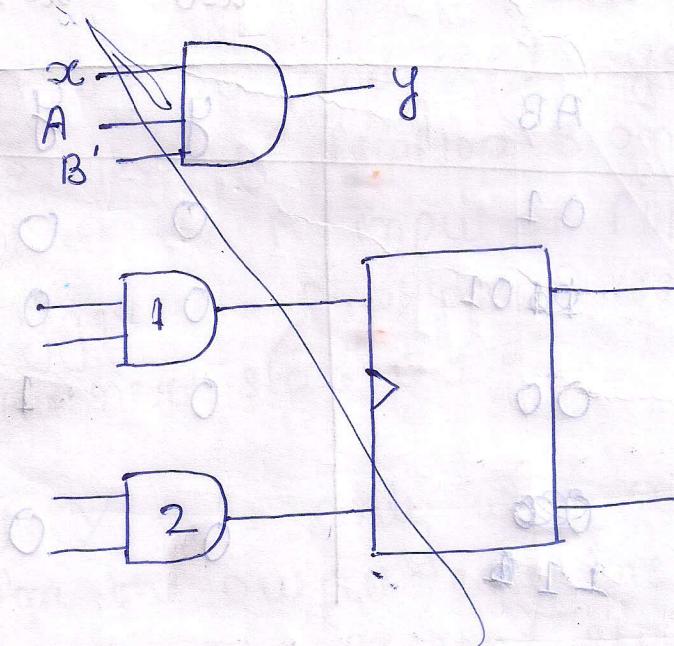
A direct reset input sets the output of a flip flop to some known value asynchronously.

A direct clear switch clears or resets all the flip flops to 0

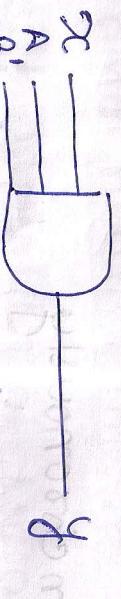


negative edge triggered clocked JK flip flop with direct clear

## ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS



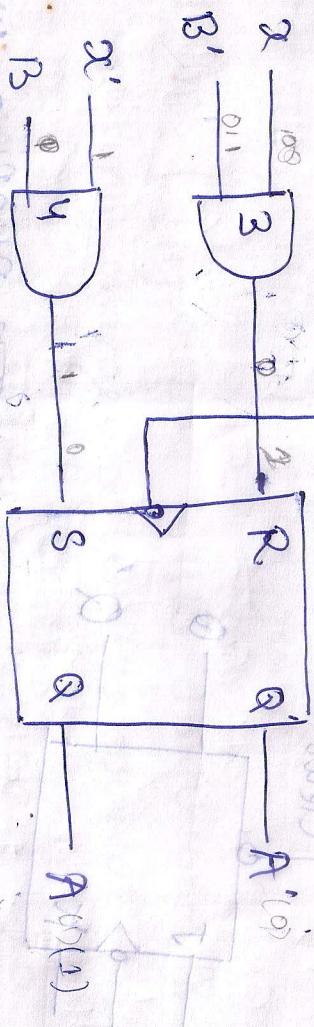
AB	Q	Q'
00	0	1
01	1	0
10	1	0
11	0	1



CIR



SMOS of digital logic  
using D flip-flop  
 $X = 0$  or 1  
 $A = 0$  or 1  
 $B = 0$  or 1  
 $A' = 1$  or 0  
 $B' = 1$  or 0



### State Table:-

Present State	Next state		Output
	$x=0$	$x=1$	
AB	AB	AB	Y
00	00	01	0
01	10	01	0
10	00	00	1
11	10	01	0
	21	05	0

\* A state table consists of present state, next state and output.

\* The present state denotes the state of flipflops before the occurrence of a clock pulse.

\* The next state shows the state of flipflops after the application of a clock pulse.

\* The output list the values of the output variables during the present state.

\* The derivation of the state table starts from initial state.

In this example, we are assuming the initial state at

00,  $A=0, B=0$ . From the logic diagram, with both the flipflops clear and  $x=0$ , none of the AND gates produce a logic 1 signal. Therefore the next state remain unchanged.

With  $AB = 00$  and  $x=1$ , gate 2 produces a logic 1 at the S input of flipflop B and gate 3 produces a logic 1 signal at the R input of flipflop A. When a clock pulse triggers the flipflop A is cleared and B is set making the next state 01.

Output  $Y = 1$  only when  $x=1, A=1$  and  $B=0$ . Therefore the output columns are marked with 0 except when the present state is 1,0 and input  $x=1$ , for which Y is marked with a 1.

## State Diagram

- \* It is a graphical representation of the information available in a state table.
- \* The state is represented by a circle and the transition between states is indicated by directed lines connecting the circles.
- \* The binary number inside each circle identifies the state it represents.
- \* The directed lines are labeled with two binary numbers separated by backward slash ('/')
- \* The input value that causes the state transition is labelled first.
- \* The number after the backward slash gives the value of the output during the present state.
- \* A directed line connecting a circle with itself indicates no change of state occurs.

