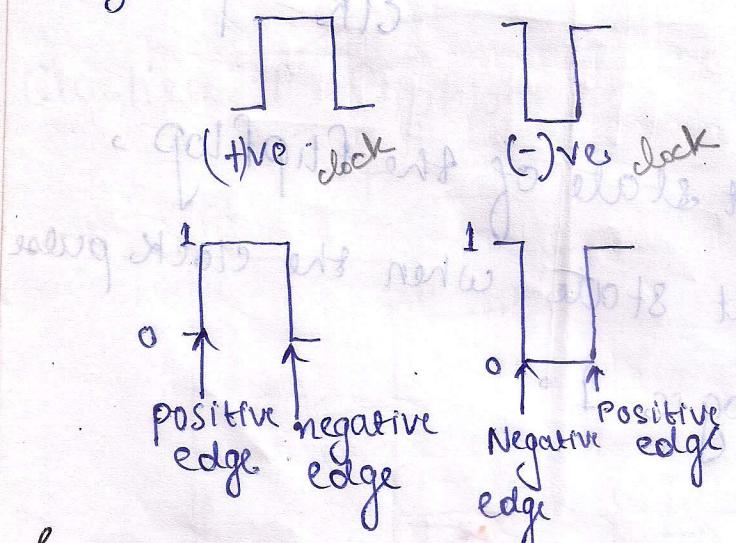


# Triggering of a FlipFlop:-

- The state of a flipflop is switched by a momentary change in the input signal. This momentary change called trigger and the transition it causes is said to trigger the flipflop.

Asynchronous Flipflop require an input trigger define a change of signal level. This level must be returned to its initial value before a second trigger is applied.

Clocked flipflops are triggered by pulses. A pulse starts from 0 and goes to 1 and remain for sometime and then goes to zero.



## Latches :-

- A Latch is a level sensitive device.
- Because of this, the state of the latch may keep changing in circuits with feedback as long as the clock pulse remains active.
- Thus instead of having output change once in a clock cycle, the output may change a number of times resulting in latching of unwanted input to the

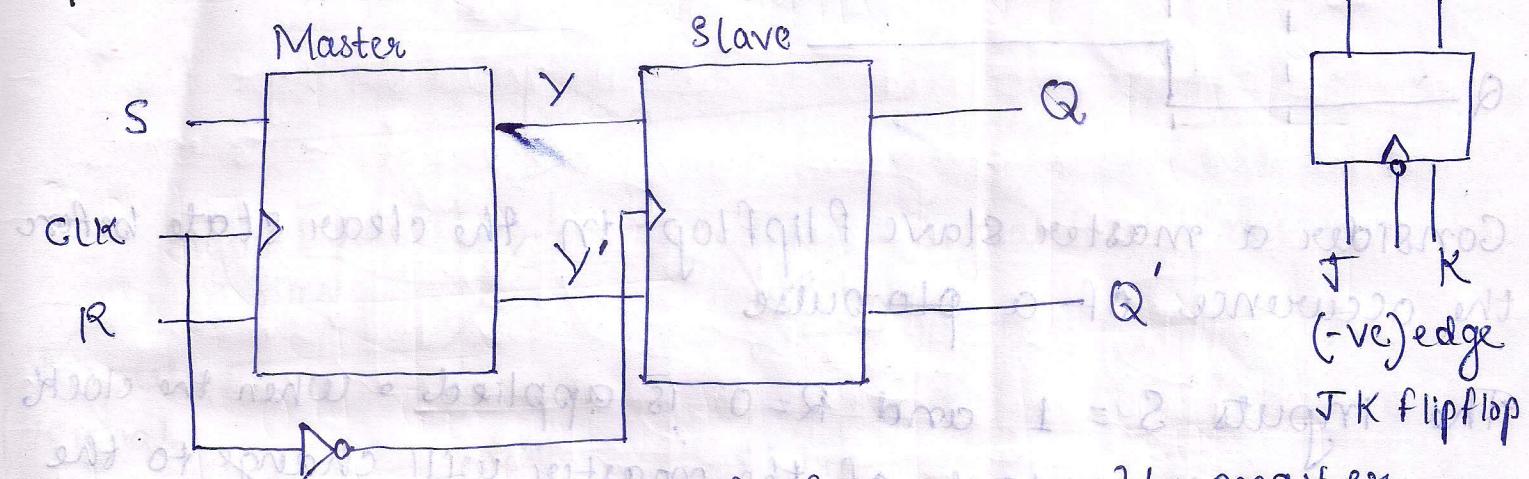
output.

4) Due to this uncertainty, latches cannot be used reliably used as storage elements.

Flipflops

These are edge triggered devices (edge sensitive).

### MASTER SLAVE FLIPFLOP :-

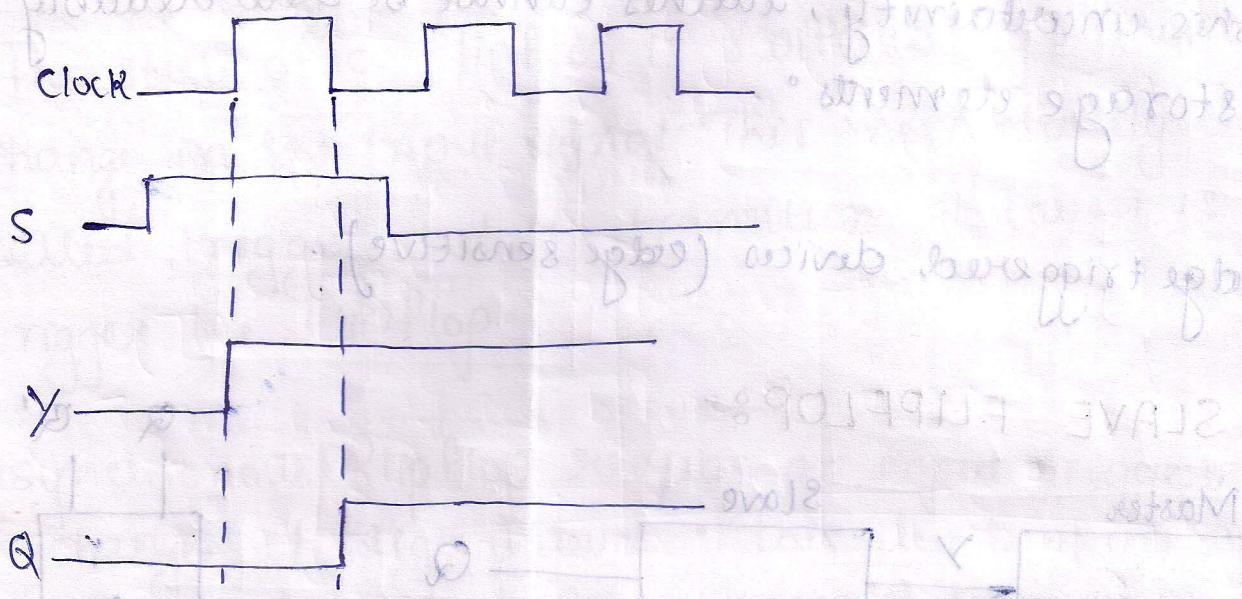


In this configuration, one flipflop serves as the master receiving the external inputs and other as a slave which takes its input from the master. When the clock pulse goes High, information at S and R inputs is transmitted to master.

The slave flipflop however remains inactive since its clock is zero.

When the clock pulse returns to zero, master will be disabled and blocks external input while slave will be enable and pass the output of master. Output will be given

# Timing waveform of Master Slave flipflop:-



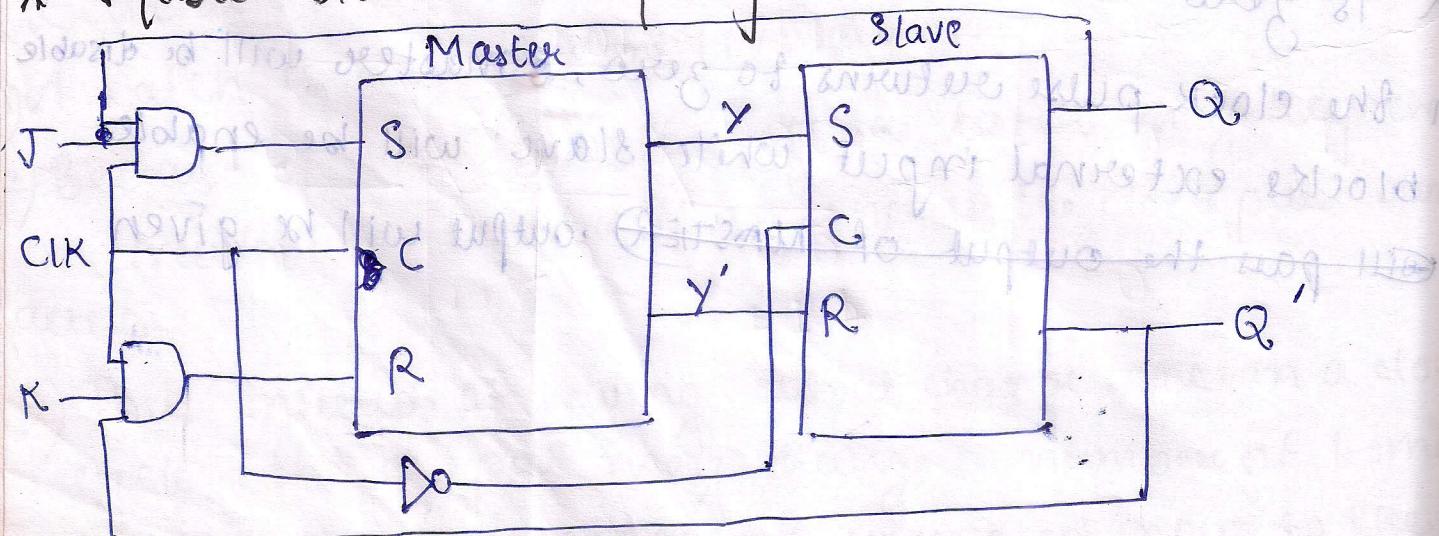
Consider a master slave Flipflop in the clear state before the occurrence of a  $\phi_0$  pulse.

The inputs  $S = 1$  and  $R = 0$  is applied. When the clock goes high, the output of the master will change to the set state while the slave remains disable.

When the clock returns to 0, the master is disable and slave is enable.

Thus the data at the slave's input when the clock was high gets latched at the slave's output.

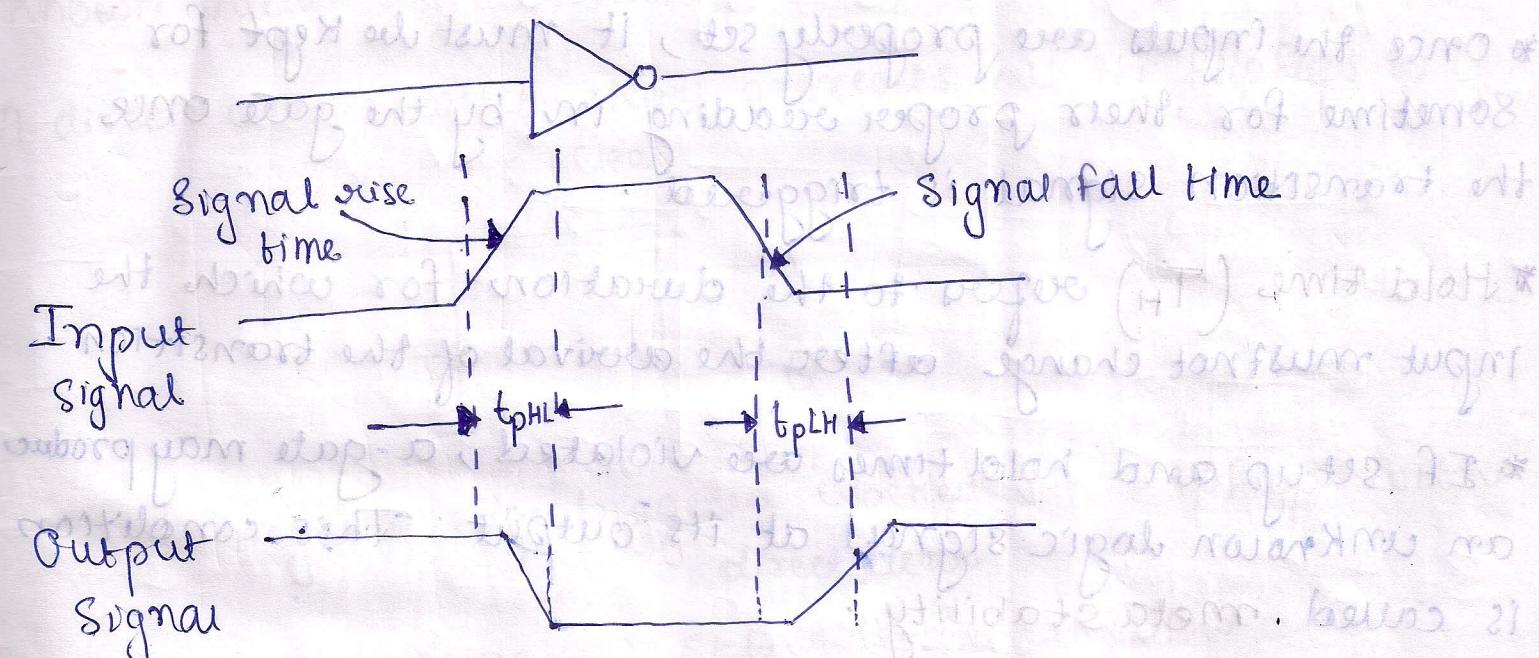
## \* Master Slave JK Flipflop:-



## Propagation Delay :-

In digital logic, every gate has got some finite amount of delay because of which the change in the output is not as instantaneous to the change in the input.

The time it takes for an input to appear at the output is called the propagation delay.



In Figure,  $t_{pHL}$  describes the time it takes for an input to cause the output to change from logic level High to logic level Low.

Similarly,  $t_{plH}$  refers to the delay associated when an input change causes the output to change from logic level Low to logic level High.

The overall delay is the average of these two delays.

## Setup and Hold Time :-

- For correct operation of Logic gates we need to satisfy some timing constraints regarding application of inputs and collecting the outputs.
- Setup time refers to a constant duration for which the inputs must be held before the arrival of the clock transition signal ( $T_s$ )
- Once the inputs are properly set, it must be kept for sometime for their proper reading in by the gate once the transition signal is triggered.
- Hold time ( $T_h$ ) refers to the duration for which the input must not change after the arrival of the transition signal.
- If setup and hold times are violated, a gate may produce an unknown logic signal at its output. This condition is called metastability.

