

15/04/2015

# Programmable Logic Array (PLA)

When the number of don't care conditions is excessive, it is economical to use PLA. In PLA, the decoder is replaced by a group of 'AND' GATES each of which can be programmed to generate a product term of the input variables.

Truth Table

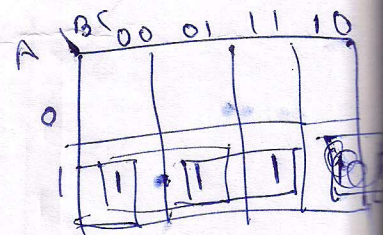
A	B	C	F <sub>1</sub>	F <sub>2</sub>
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

$$F_1 = AB'C' + AB'C + ABC$$

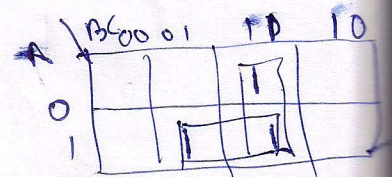
$$F_2 = A'BC + AB'C + ABC$$

$$= AB' + ABC = AB' + A$$

$$= A'BC + AC = AC + BC$$



$$= AB' + AC$$

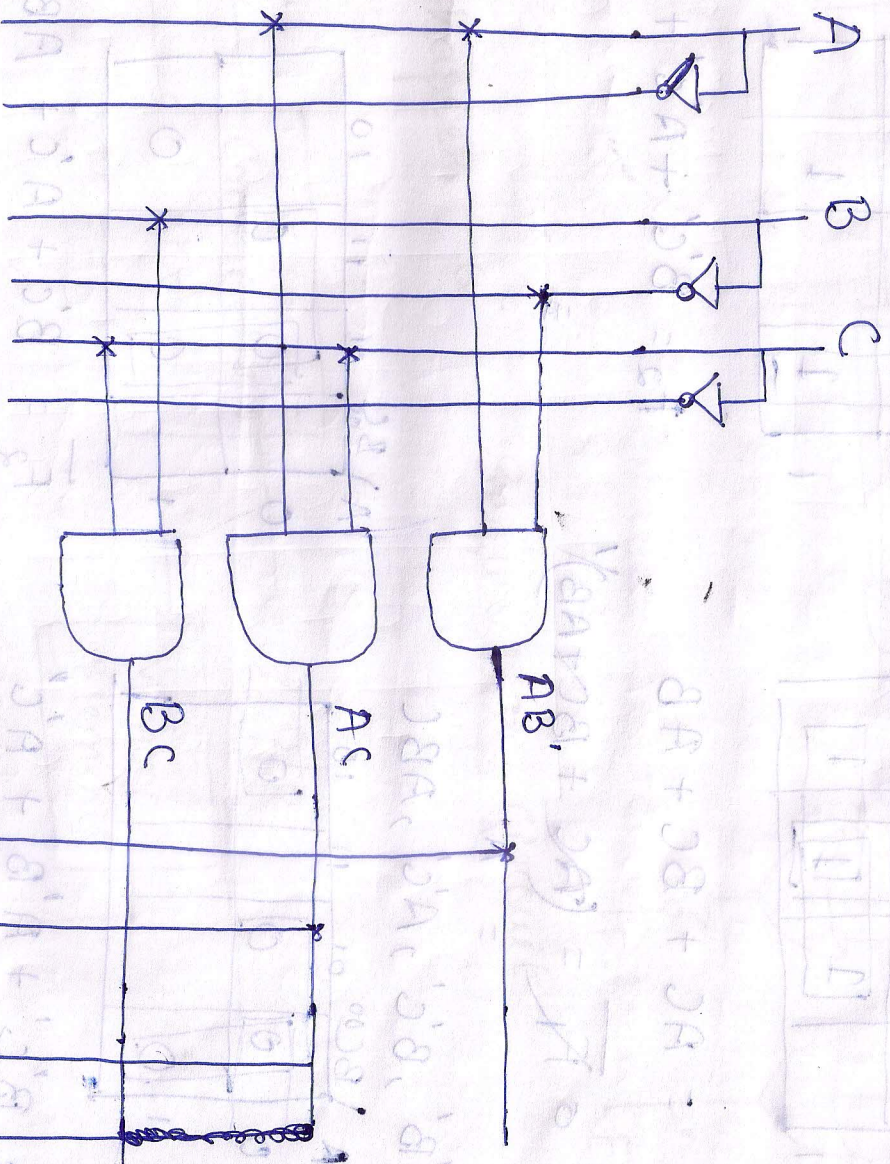


$$= AC + BC$$



# PLD Program - Table

Product Terms	Inputs				Outputs	
	A	B	C		F <sub>1</sub>	F <sub>2</sub>
1	1	0	—		1	—
2	1	1	—		1	1
3	—	—	1	1	—	1



Inputs	A	B	C	F <sub>1</sub>	F <sub>2</sub>
1	1	0	—	1	—
2	1	1	—	1	1
3	—	—	1	—	1



A combination circuit is defined by a function  
 $F_1(A, B, C) = \Sigma(3, 5, 6, 7)$

$$F_2(A, B, C) = \Sigma(0, 2, 4, 7)$$

Implement this circuit with a PLA, 4 product terms and 2 out

having 3 input

A \ BC	00	01	11	10
0			1	
1		1	1	1

A \ BC	00	01	11	10
0	1			1
1	1		1	

$$F_1 = AC + BC + AB$$

$$F_2 = B'C' + A'C' + ABC$$

$$\bar{F}_1 = (AC + BC + AB)'$$

$$= A$$

$$A'B', B'C', A'C', ABC$$

A \ BC	00	01	11	10
0	0	0		0
1	0			

A \ BC	00	01	11	10
0		0	0	
1		0		0

$$\bar{F}_1 = B'C' + A'B' + A'C'$$

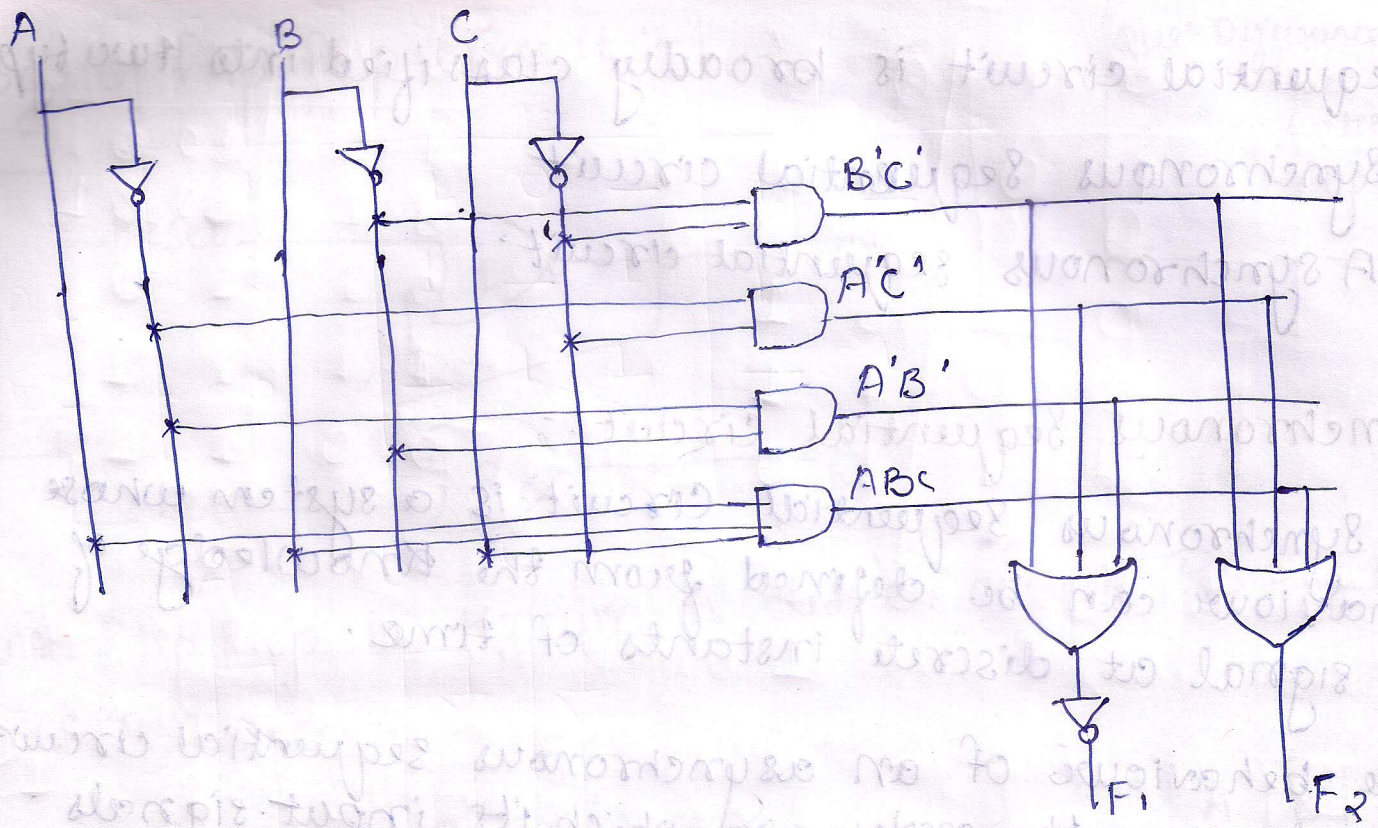
$$\bar{F}_2 = B'C + A'C + ABC'$$

$$\therefore F_1 = (B'C' + A'C' + A'B')'$$

$$F_2 = B'C' + A'C' + ABC$$

	Product Terms	Inputs			Outputs	
		A	B	C	F <sub>1</sub>	F <sub>2</sub>
B'C'	1	—	0	0	1	1
A'C'	2	0	—	0	1	1
A'B'	3	0	0	—	1	0
ABC	4	1	1	1	—	1

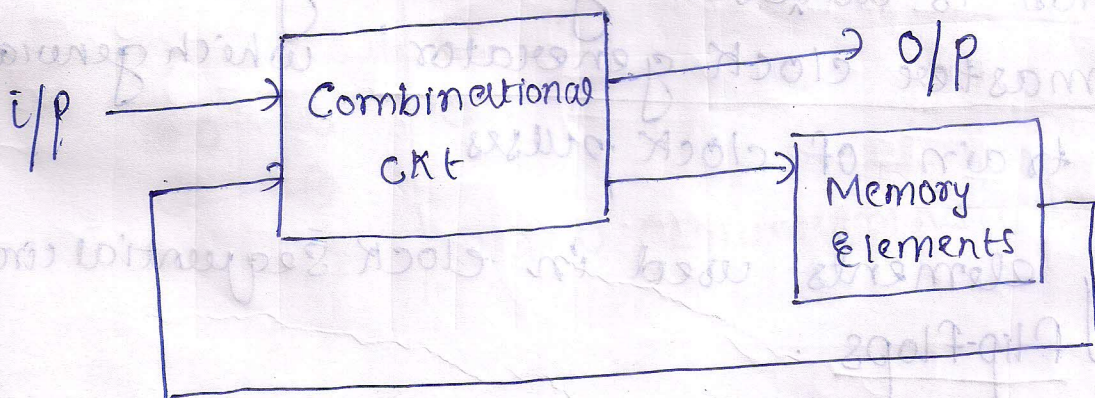




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Chapter - 6

Sequential circuit



Sequential circuit

Memory elements

A sequential circuit consists of a combinational circuit to which memory elements are connected to form a feedback path. The memory elements are devices capable of storing binary information within them. The binary information stored in the memory elements at any given time defines the state of the sequential circuit.