Note on components:

- All 0603 resistors are ±1%, 0.1W
- All 0805 resistors are ±1%, 0.25W
- All electrolytic capacitors are at least 10V= (if otherwise not noted)
- All ceramic capacitors are C0G (NP0) if possible, otherwise X7R by default, at least 16V=

Power Supply

Power Supply.Sch

DSP PS

DSP PS.Sch

DSP Time Base

CLK[0..7]

DSP Time Base.Sch

ETX

(X1)

HBIL
HCNTL0
HCNTL1
HR/W
HDS
HCS[0..3]
HRST[0..3]
HINT[0..3]
HRDY[0..3]
HD[0..7]

(X3)

TDO
TDI
TCK
TMS

ETX.Sch

DSP HPI Bus

HBIL
HCNTL0
HCNTL1
HR/W
HDS
HCS[0..3]
HRST[0..3]
HINT[0..3]
HRDY[0..3]
HD[0..7]

CLK[0..7]

TDO
TDI
TCK
TMS

DSP Core 1

CLK2
CLK3
HRST0
HCS0
HDS
HBIL
HCNTL0
HCNTL1
HR/W
HD[0..7]
HINT0
HRDY0

CLKIN
CLKIN2
RESET
HCS
HDS
HBIL
HCNTL0
HCNTL1
HR/W
HD[0..7]
HINT
HRDY

DSP Core 1.Sch

DSP Core 2

CLK1
CLK7
HRST1
HCS1
HDS
HBIL
HCNTL0
HCNTL1
HR/W
HD[0..7]
HINT1
HRDY1

CLKIN
CLKIN2
RESET
HCS
HDS
HBIL
HCNTL0
HCNTL1
HR/W
HD[0..7]
HINT
HRDY

DSP Core 2.Sch

DSP Core 3

CLK6
CLK4
HRST2
HCS2
HDS
HBIL
HCNTL0
HCNTL1
HR/W
HD[0..7]
HINT2
HRDY2

CLKIN
CLKIN2
RESET
HCS
HDS
HBIL
HCNTL0
HCNTL1
HR/W
HD[0..7]
HINT
HRDY

DSP Core 3.Sch

Internal JTAG Control

Connected to LPT1 (ETX X3)
Compatible to XILINX Parallel III Interface

Board JTAG

VCC VCC VCC VCC

R100 10k
R101 10k
R102 10k
R103 10k

JTAG

VCC 1
GND 2
TCK 3
TDO 4
TDI 5
TMS 6

HDR1X6

External JTAG Control

53 30 29 28

TDO TCK TMS TDI

U1700B XC9572XL-10VQ64C
U1600B XC9572XL-10VQ64C
U1500B XC9572XL-10VQ64C

Pull-up resistors (replacement for DSP Core 4)

VCC R104 10k HINT3
VCC R105 10k HRDY3

Global Nets

GND
FGND
+5V
VCC
+3.3V.ETX
V_DSP

Protel Note:
All nets associated to power symbols are global.

Note on System Reset:

System reset is provided by the ETX module.

ETX module resets system when:
a) +5V is bellow the threshold, or
b) PWGIN is pulled down (used for manual reset)

All external logic to ETX is powered by the LDOs whose input voltage is +5V. LDOs have stable output voltages when their inputs are above 3.5V, which is bellow the threshold for the system reset provided by the ETX module.

BATT1
CR2032

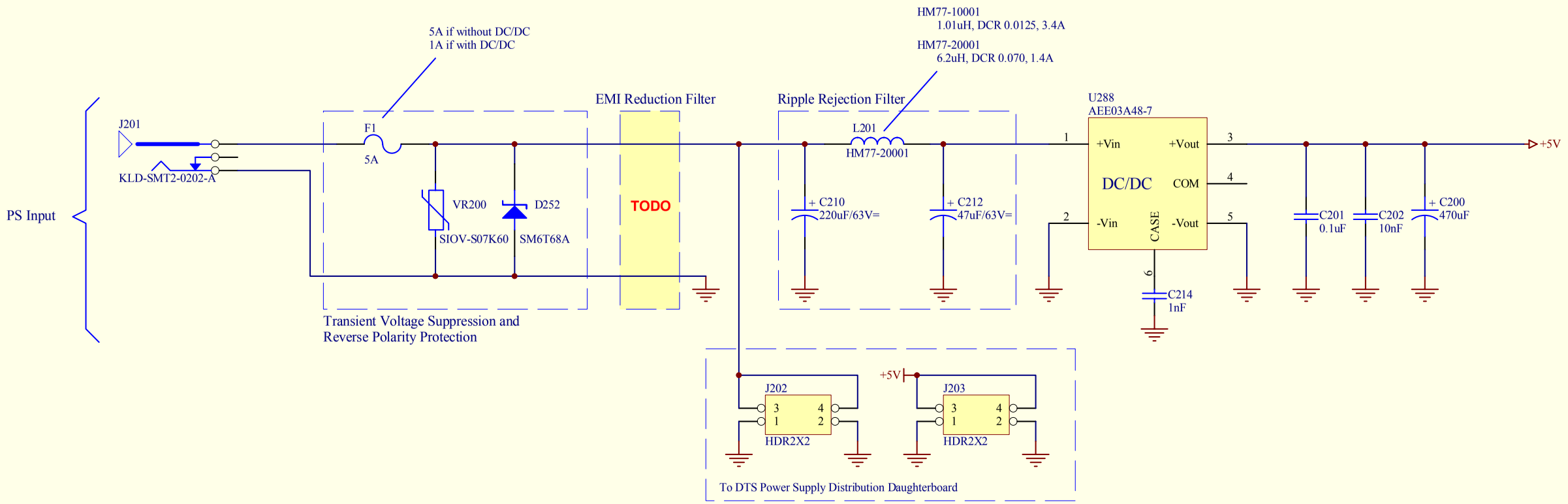
M100
Layer Stackup

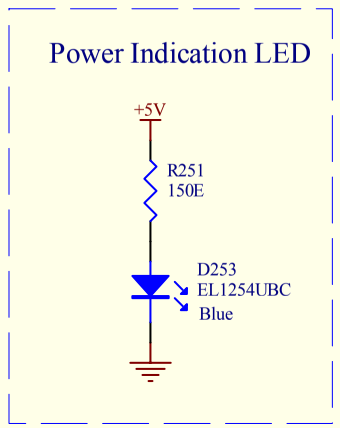
GE6P R2A

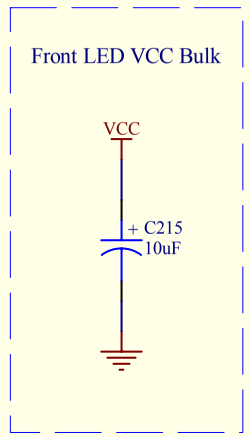
Project Hierarchy
(15 Sheets Total)

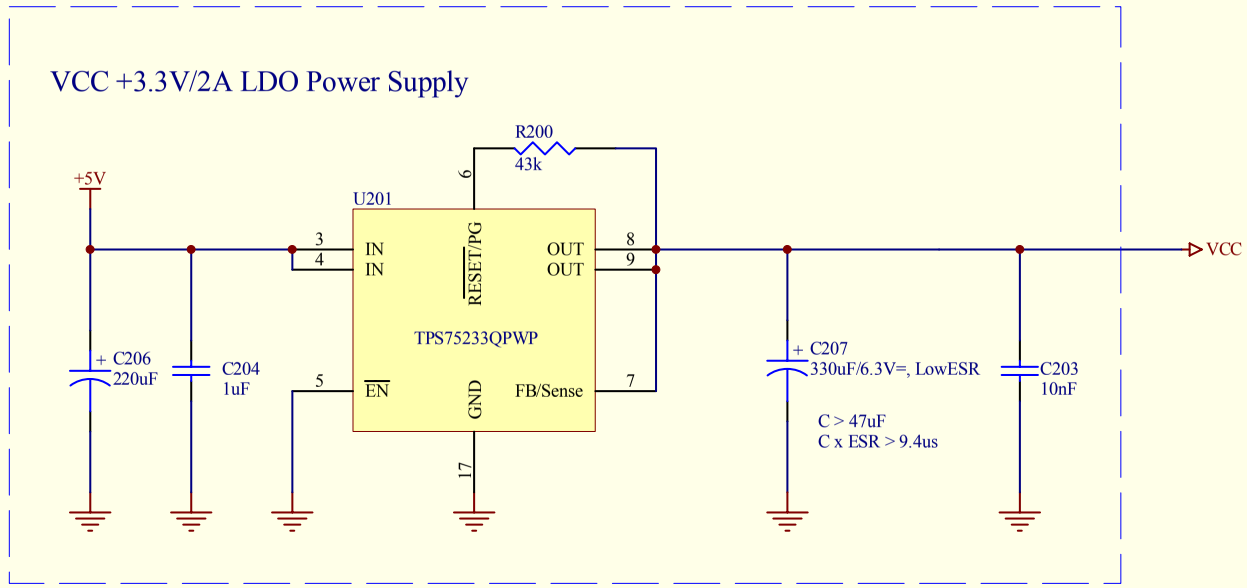
1. This sheet
   - 2. Power Supply
   - 3. ETX Module
     - 4. ETX-X1: PCI, USB
     - 5. ETX-X2: ISA (DSP HPI)
     - 6. ETX-X3: VGA, COM, KBD
     - 7. ETX-C4: Ethernet, CF, SPK, BAT, MRST
   - 8. DSP Core Power Supply
   - 9. DSP Time Base
   - 10. DSP Core 1
     - 11. DASL Pair 1
   - 12. DSP Core 2
     - 13. DASL Pair 2
   - 14. DSP Core 3
     - 15. DASL Pair 3

Title: *GE6P - ELU28 VoIP Gateway*			*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:30	Sheet 1 of 15		
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\GE6P R2B.Sch			









Title *XLUi - Power Supply*			*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:30		Sheet 2 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\Power Supply.Sch			

ETX Module

X1
- PCI
- USB
- Audio
- Misc: SERIRQ, 3.3V out

X2
- ISA

X3
- VGA
- Video
- FP LVDS or PAR
- IrDA
- COM1, COM2
- LPT or FD
- PS/2 Keyboard, Mouse

X4
- Primary IDE
- Secondary IDE
- Power Control & Misc.
- I2C
- SMBus
- Ethernet

X1

ETX X1

$\overline{HRST}$[0..3]
HCS[0..3]
HDS
HBIL
HCNTL0
HCNTL1
HR/$\overline{W}$
$\overline{HINT}$[0..3]
HRDY[0..3]
HD[0..7]

ETX X1.Sch

$\overline{HRST}$[0..3] → $\overline{HRST}$[0..3]
HCS[0..3] → HCS[0..3]
HDS → HDS
HBIL → HBIL
HCNTL0 → HCNTL0
HCNTL1 → HCNTL1
HR/$\overline{W}$ → HR/$\overline{W}$
$\overline{HINT}$[0..3] → $\overline{HINT}$[0..3]
HRDY[0..3] → HRDY[0..3]
HD[0..7] → HD[0..7]

DSP HPI/8 Bus

X2

ETX X2

ETX X2.Sch

X3

ETX X3

TDO
TDI
TCK
TMS

ETX X3.Sch

TDO → TDO
TDI → TDI
TCK → TCK
TMS → TMS

JTAG Control

X4

ETX X4

ETX X4.Sch

ETX Module Mounting Holes (Grounded)

ETX-M1 ETX-M2 ETX-M3 ETX-M4

+5V Low Frequency Decoupling and DC Bulk Capacitors for ETX

Note: All Low ESR, 6.3V

+5V

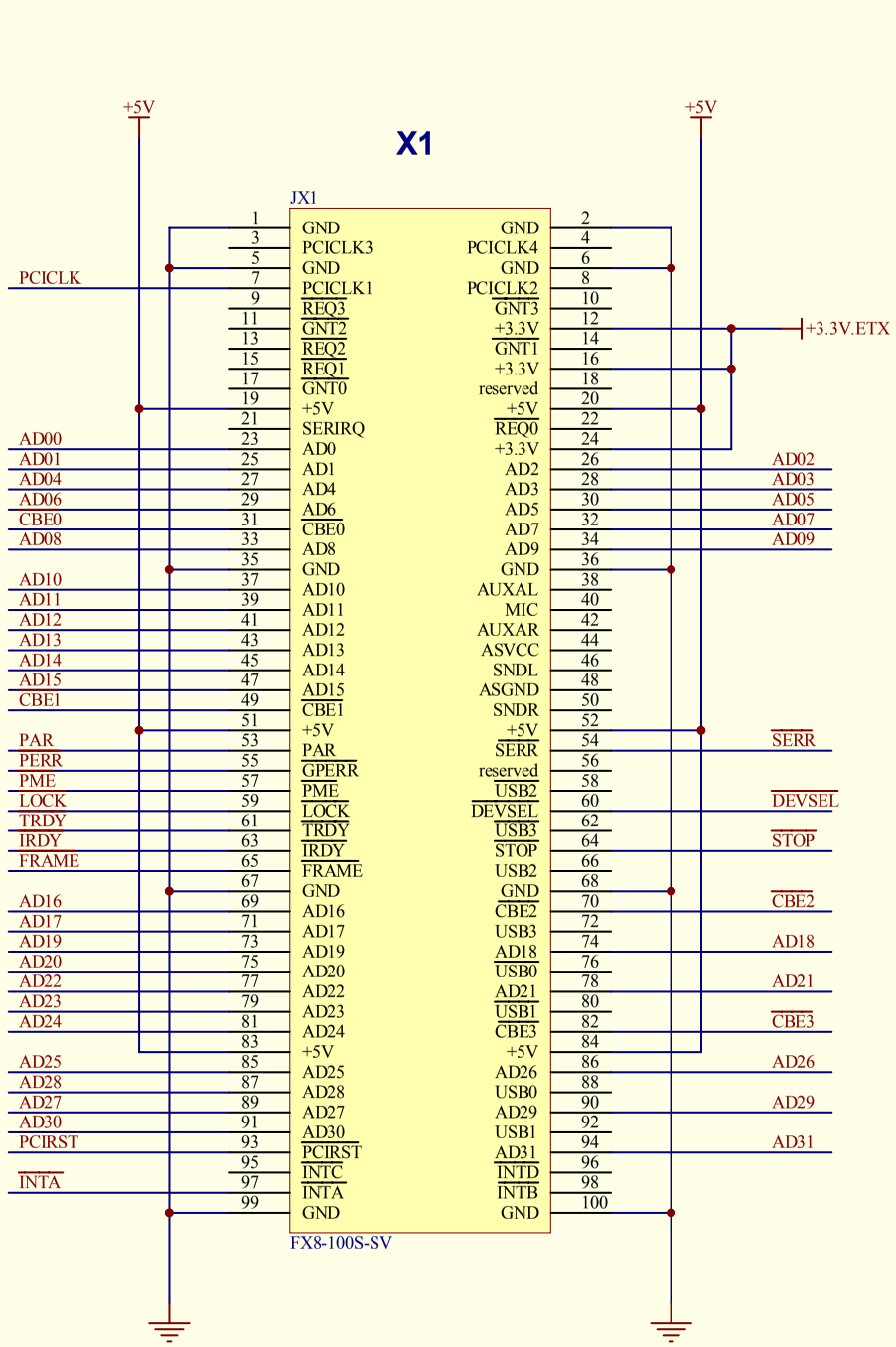
C271 470uF, C272 470uF, C273 470uF, C274 470uF, C275 470uF, C276 470uF, C277 470uF, C278 470uF

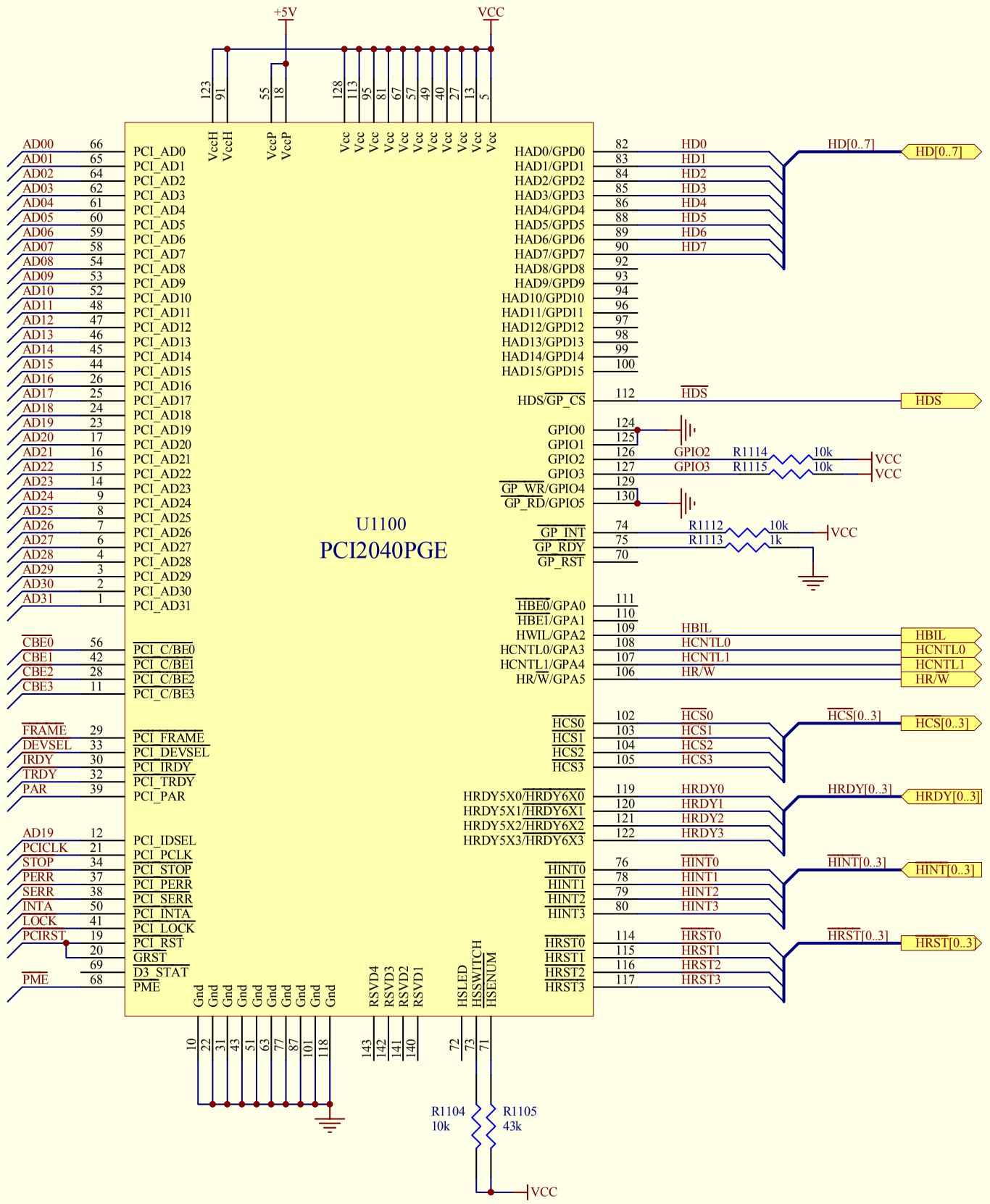
High Frequency Decoupling Capacitors

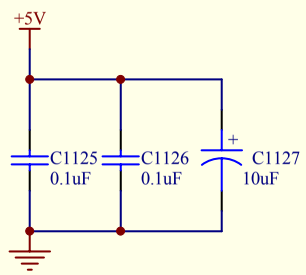
+5V

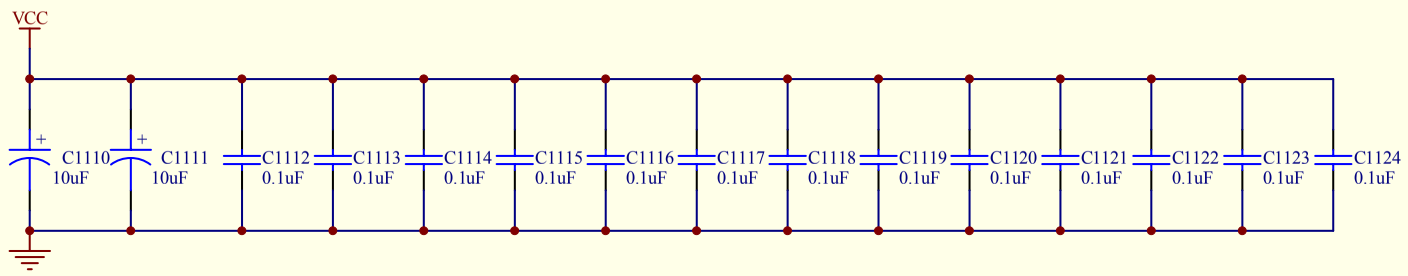
C261 0.1uF, C262 0.1uF, C263 0.1uF, C264 0.1uF, C265 0.1uF, C266 0.1uF, C267 0.1uF, C268 0.1uF

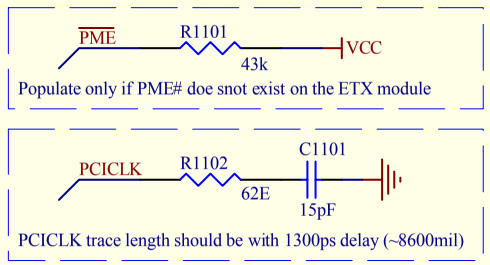
Title *ETX Module*			IPTC Tech. Comm. AB Pyramidbacken 6 141 75 Kungens Kurva Sweden
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:30		Sheet 3 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\ETX.Sch			

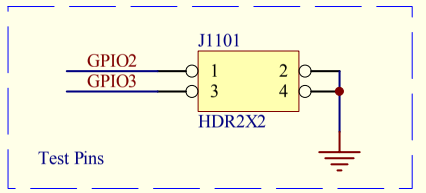








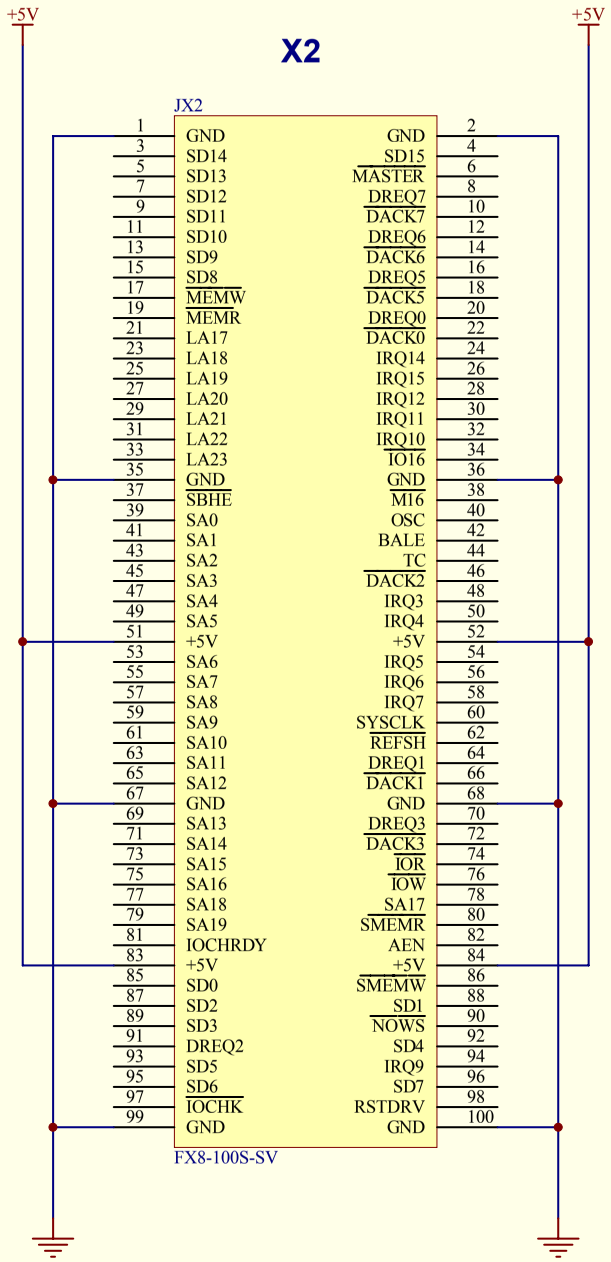




Required Pullups:

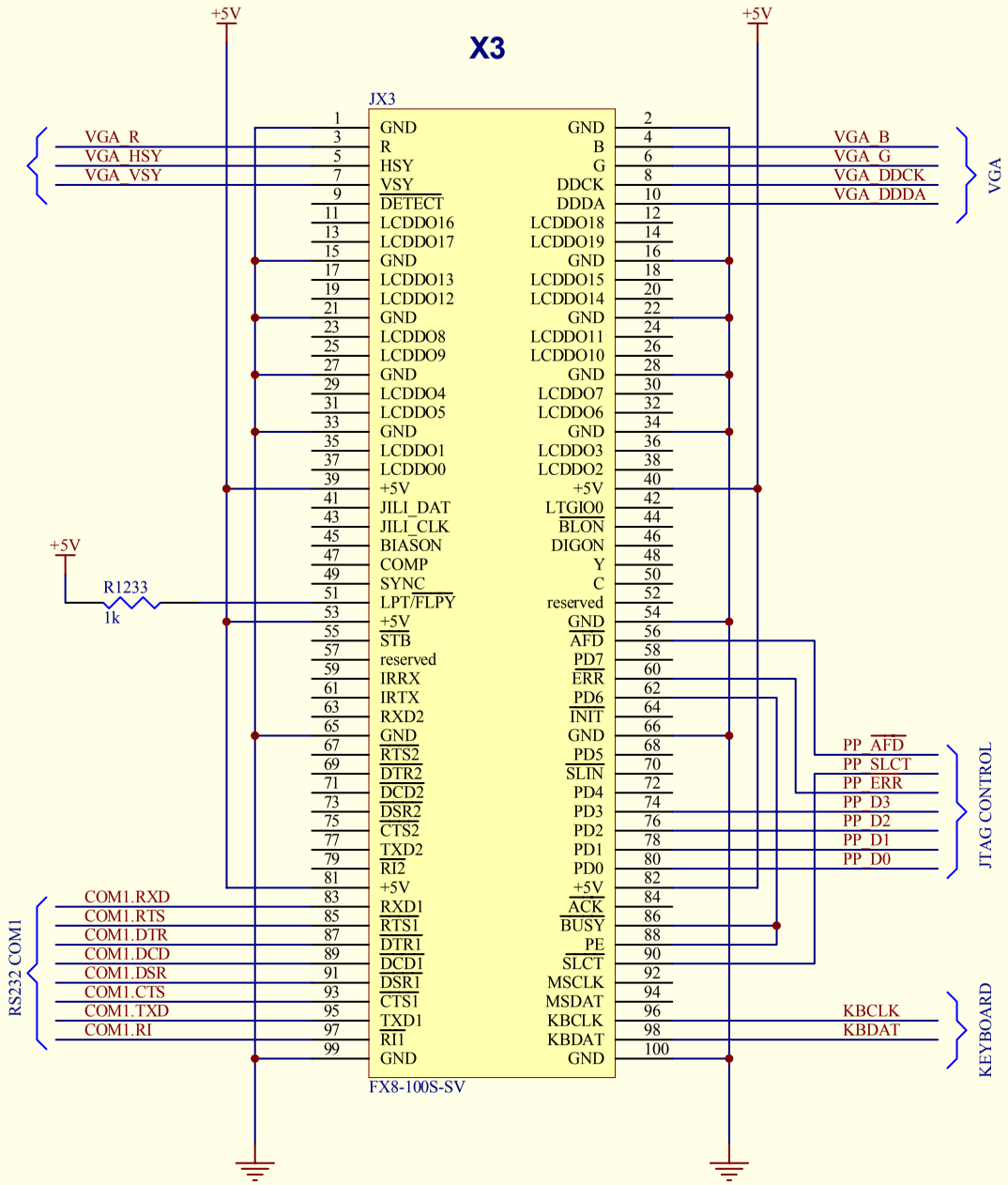
- HINT#: ~10k if not connected
- HRDY: ~10k if not connected
- GPIO: ~10k if not connected or configured as input

Title *ETX (X1) PCI, USB*			*IPTC Tech. Comm. AB Pyramidbacken 6 141 75 Kungens Kurva Sweden*
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:31		Sheet 4 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\ETX X1.Sch			

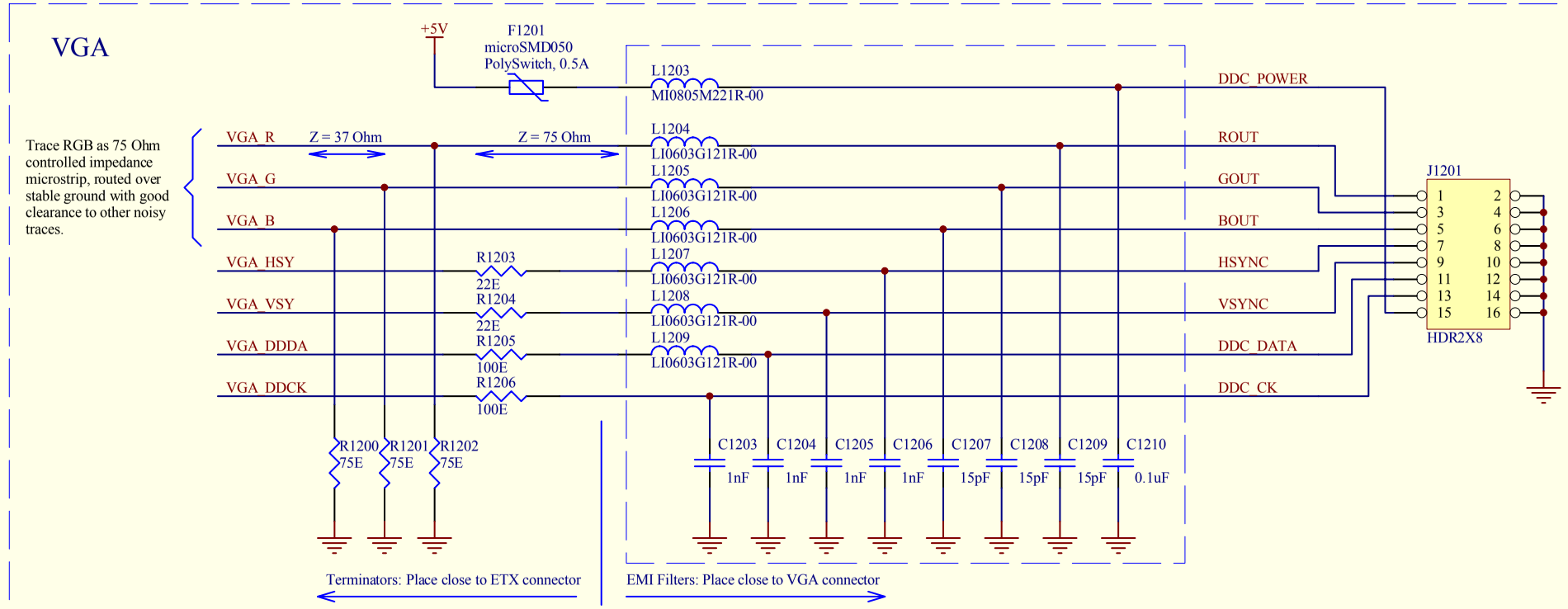


Title	ETX (X2): ISA / DSP HPI8		IPTC Tech. Comm. AB Pyramidbacken 6 141 75 Kungens Kurva Sweden
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006	Time: 22:51:31	Sheet 5 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\ETX X2.Sch			

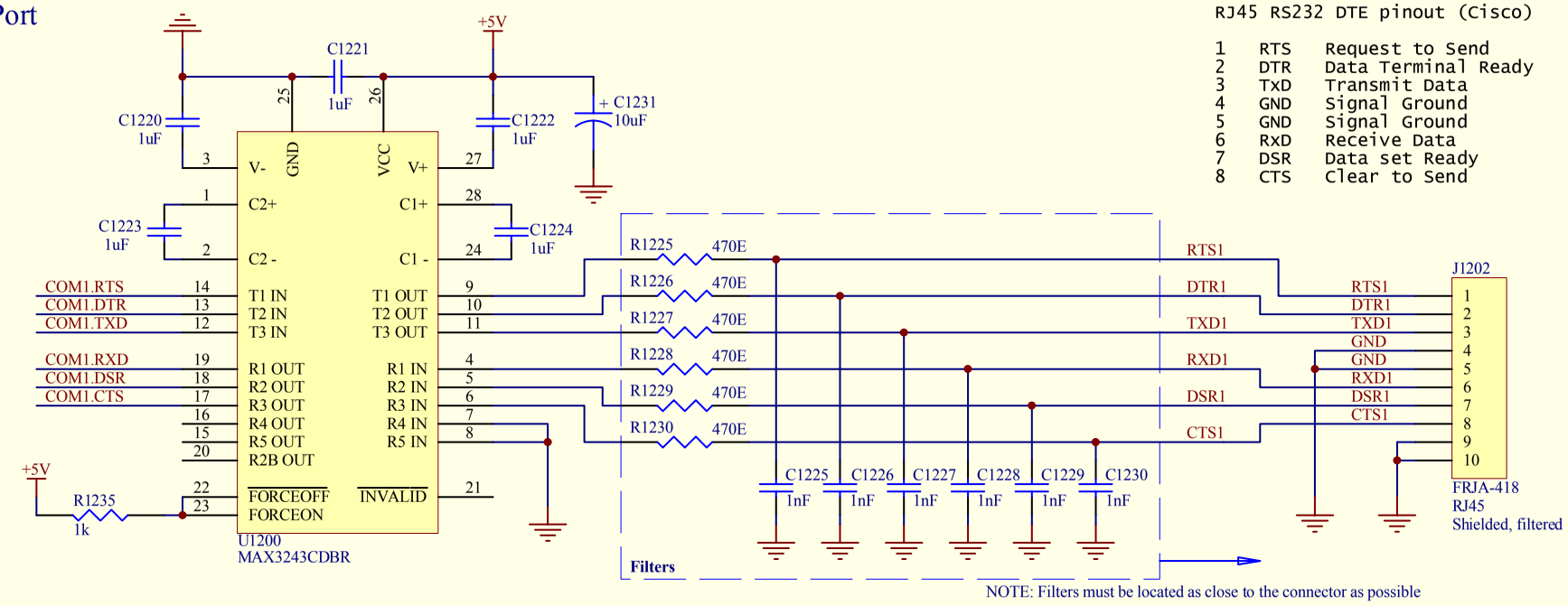
X3



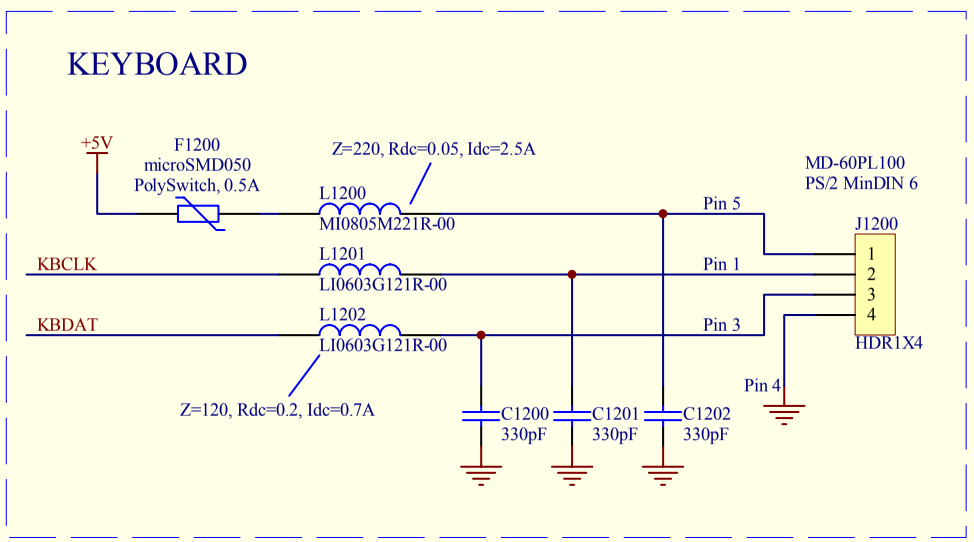
VGA



COM1 Port

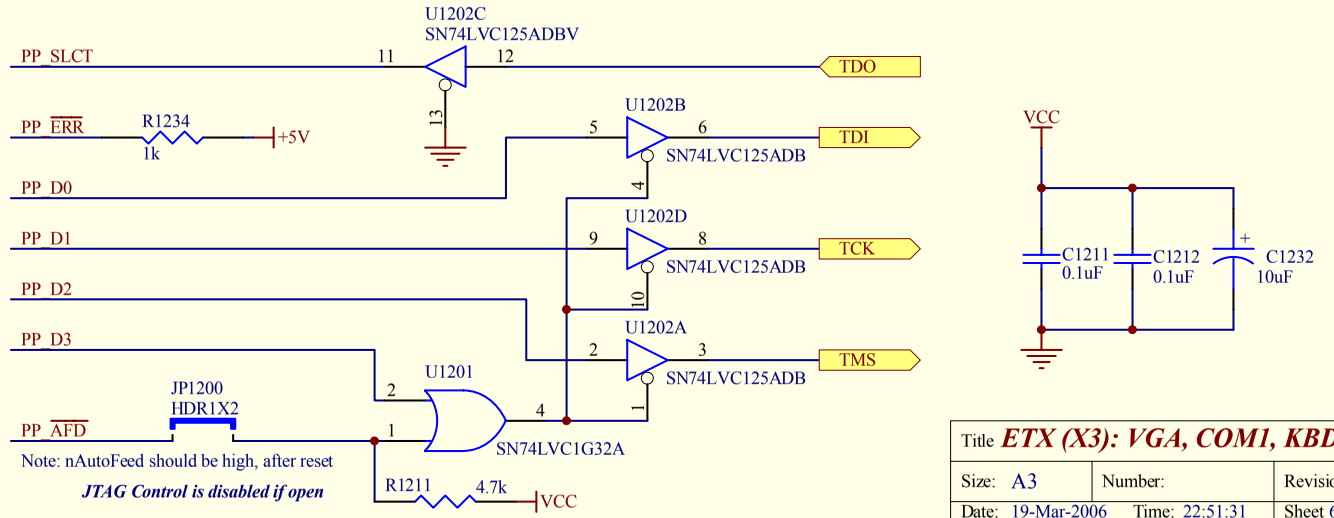


KEYBOARD



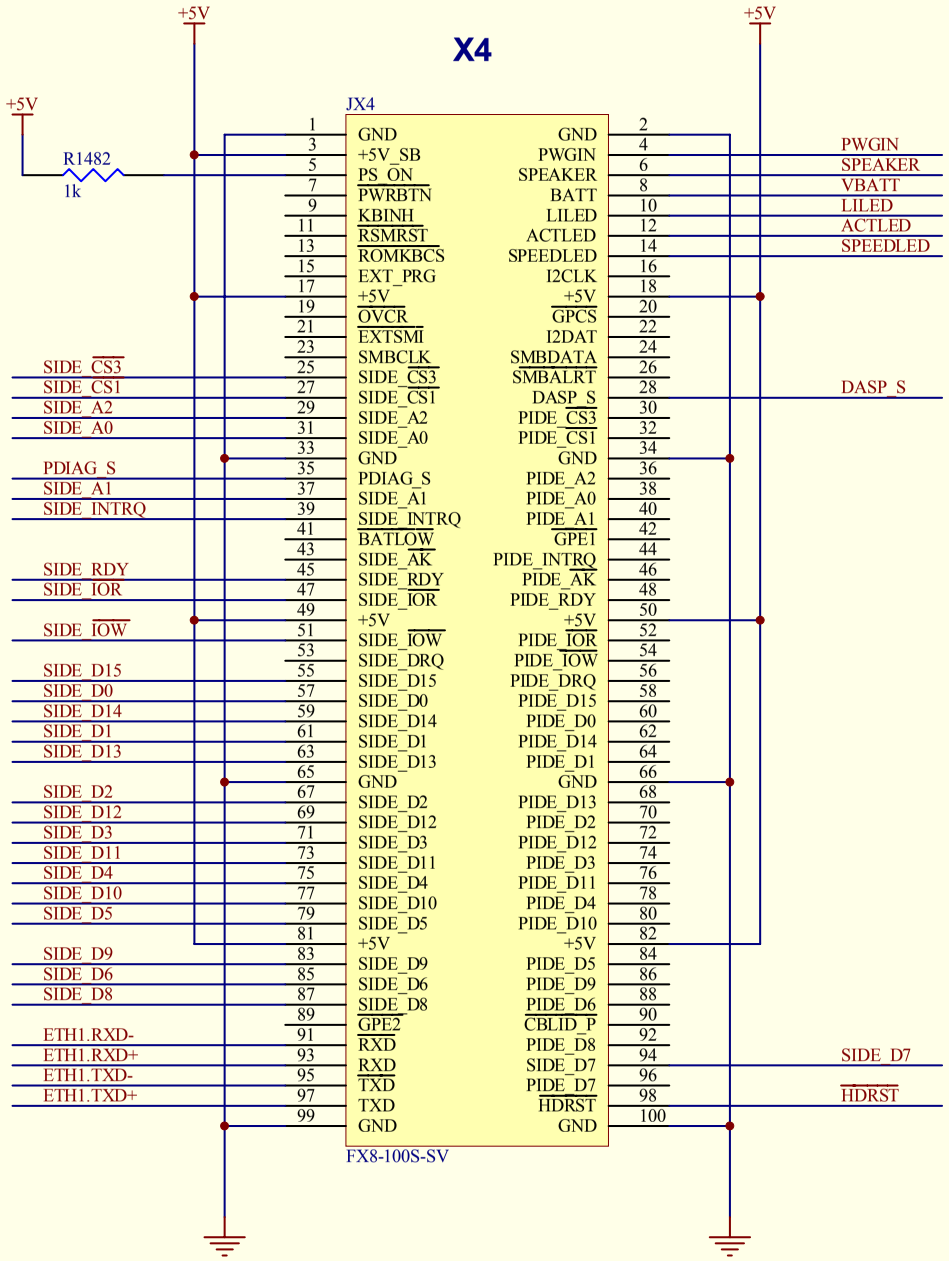
JTAG CONTROL

Compatible with XILINX Parallel III Cable

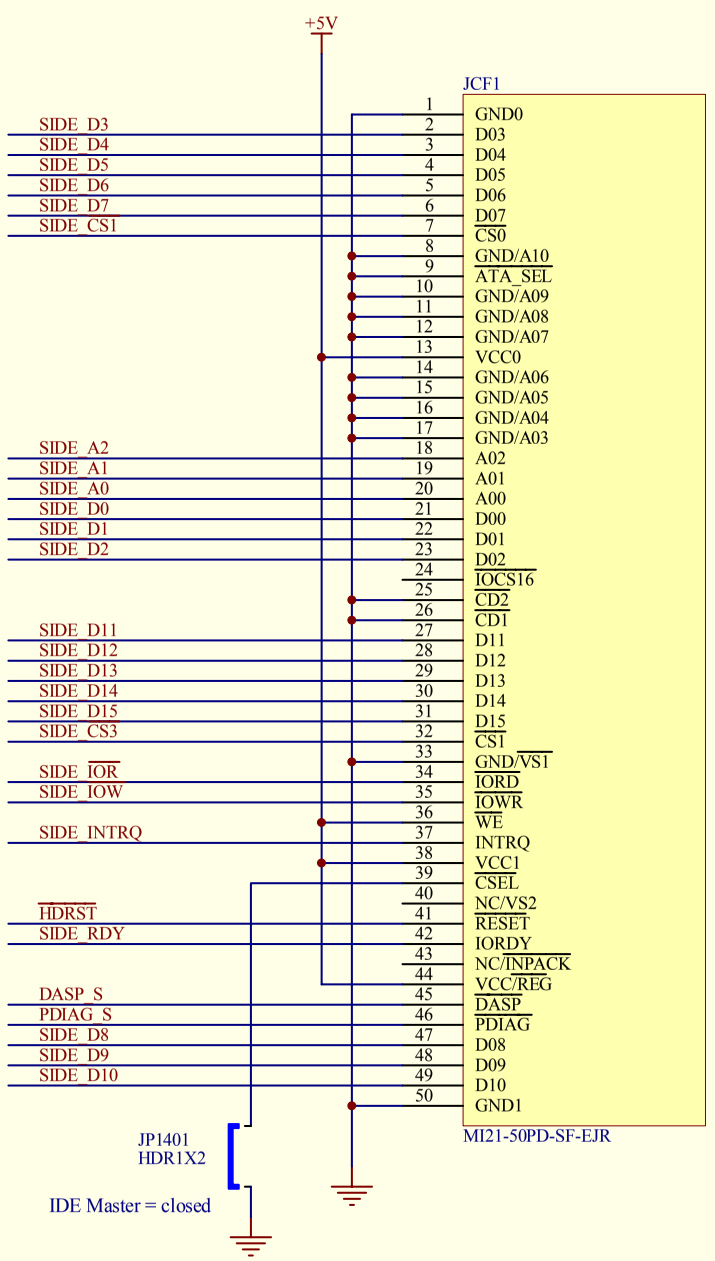


Title	ETX (X3): VGA, COM1, KBD, JTAG Ctrl		IPTC Tech. Comm. AB Pyramidbacken 6 141 75 Kungens Kurva Sweden
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006	Time: 22:51:31	Sheet 6 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\ETX X3.Sch			

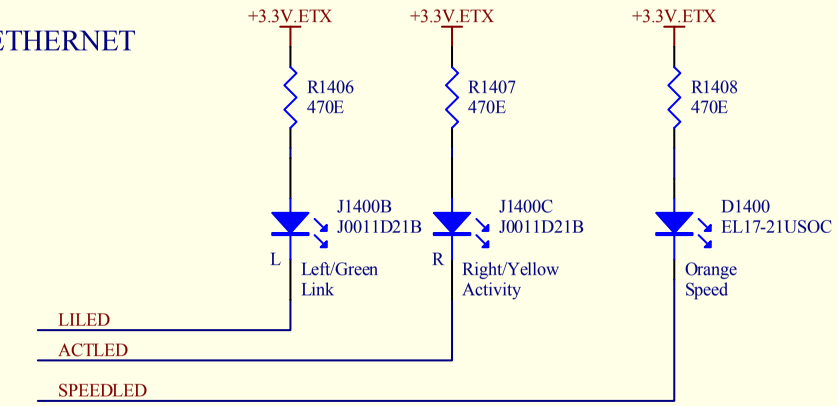
X4

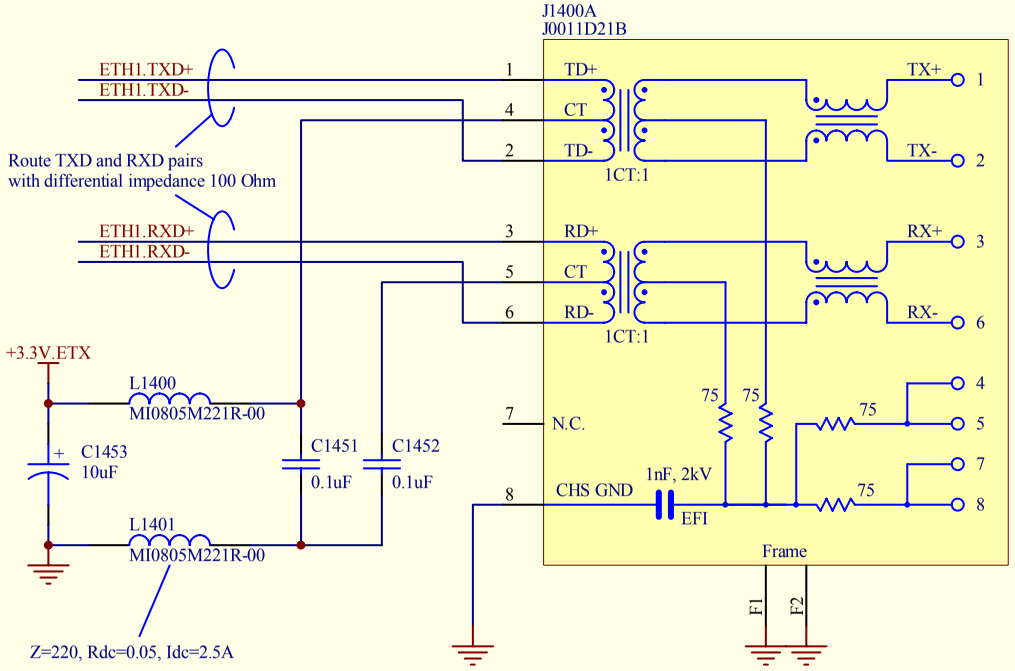


Compact Flash Type I/II Socket



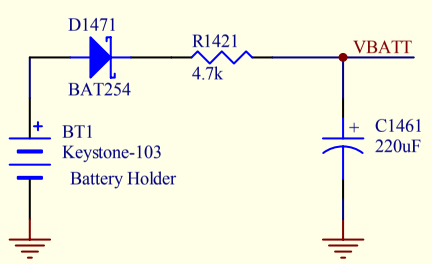
ETHERNET






```
zdiff = 100 Ohm:
    W = 11 mil
    D = 20 mil
    h = 9 mil
    s = D-W = 9 mil
    epsilon_r = 4.3
```

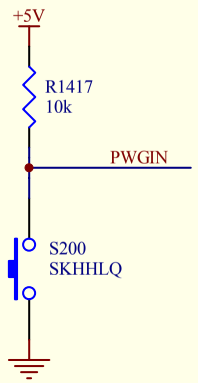
Lithium Battery



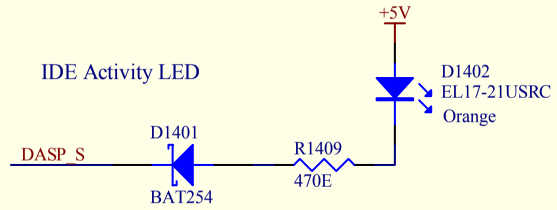
Designed for 1E-6 A Realtimeclock current:
3V-1E-6A*4.7E3 Ohm -0.3V = 2.695V
Imax = 2.7V/4.7E3 OHm = 510E-6A Battery current if shorten

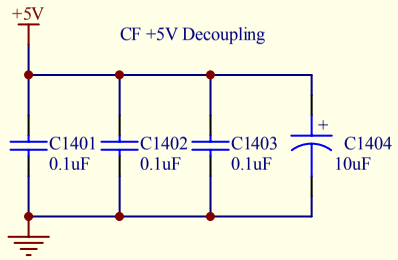
UL 1642: Standard for Safety for Lithium Batteries
UL 2054: Household and Commercial Batteries

Manual Reset

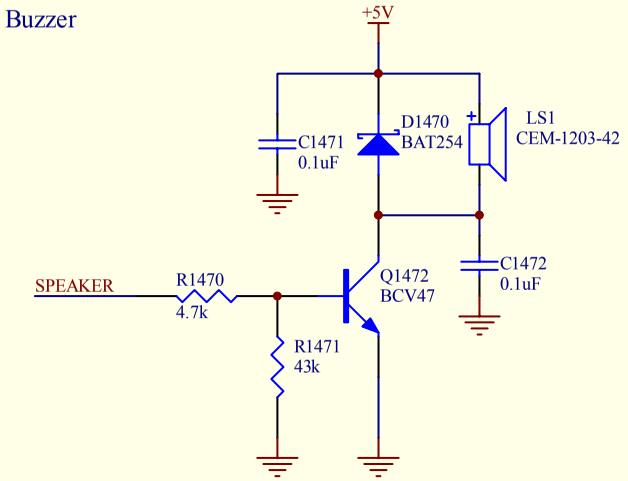


IDE Activity LED





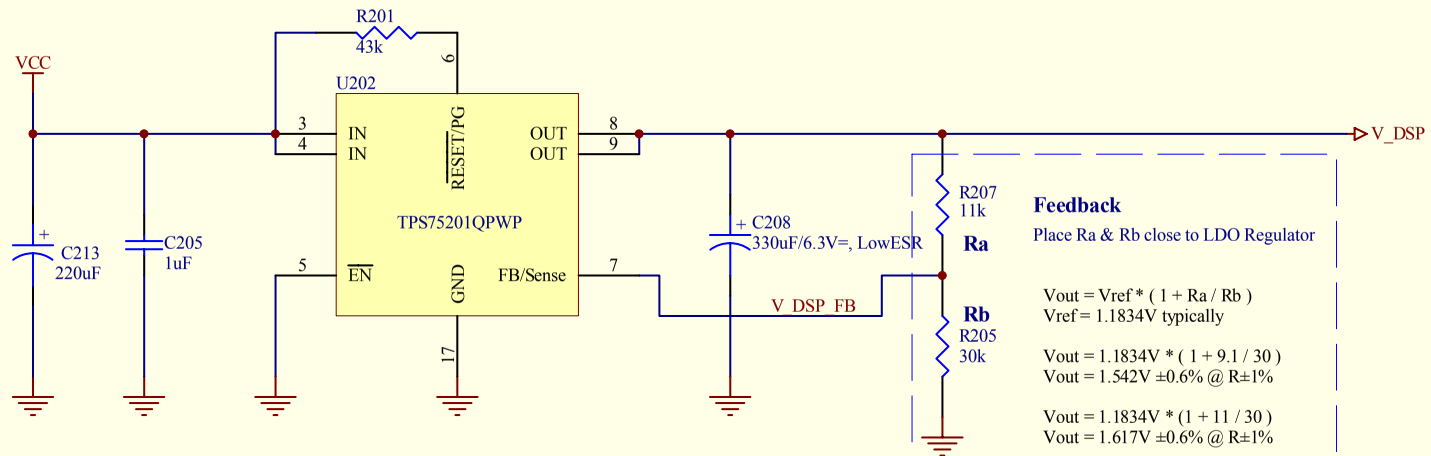
Buzzer



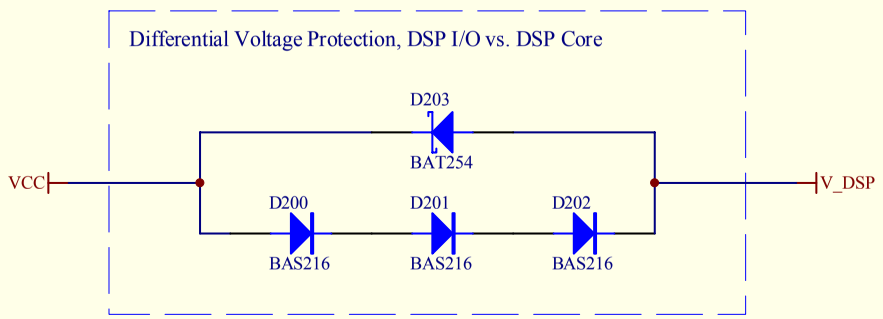
Title: *ETX (X4): CF I/II, SPK, Ethernet*			*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:32		Sheet 7 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\ETX X4.Sch			

DSP Core +1.5-1.6V / 2A LDO Power Supply

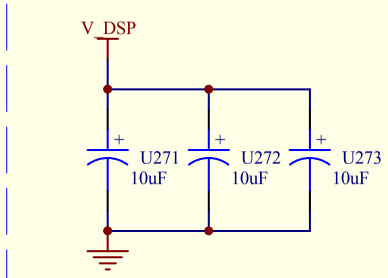
(1.5V for 120 MHz, 1.6V for 160 MHz DSP)



Differential Voltage Protection, DSP I/O vs. DSP Core

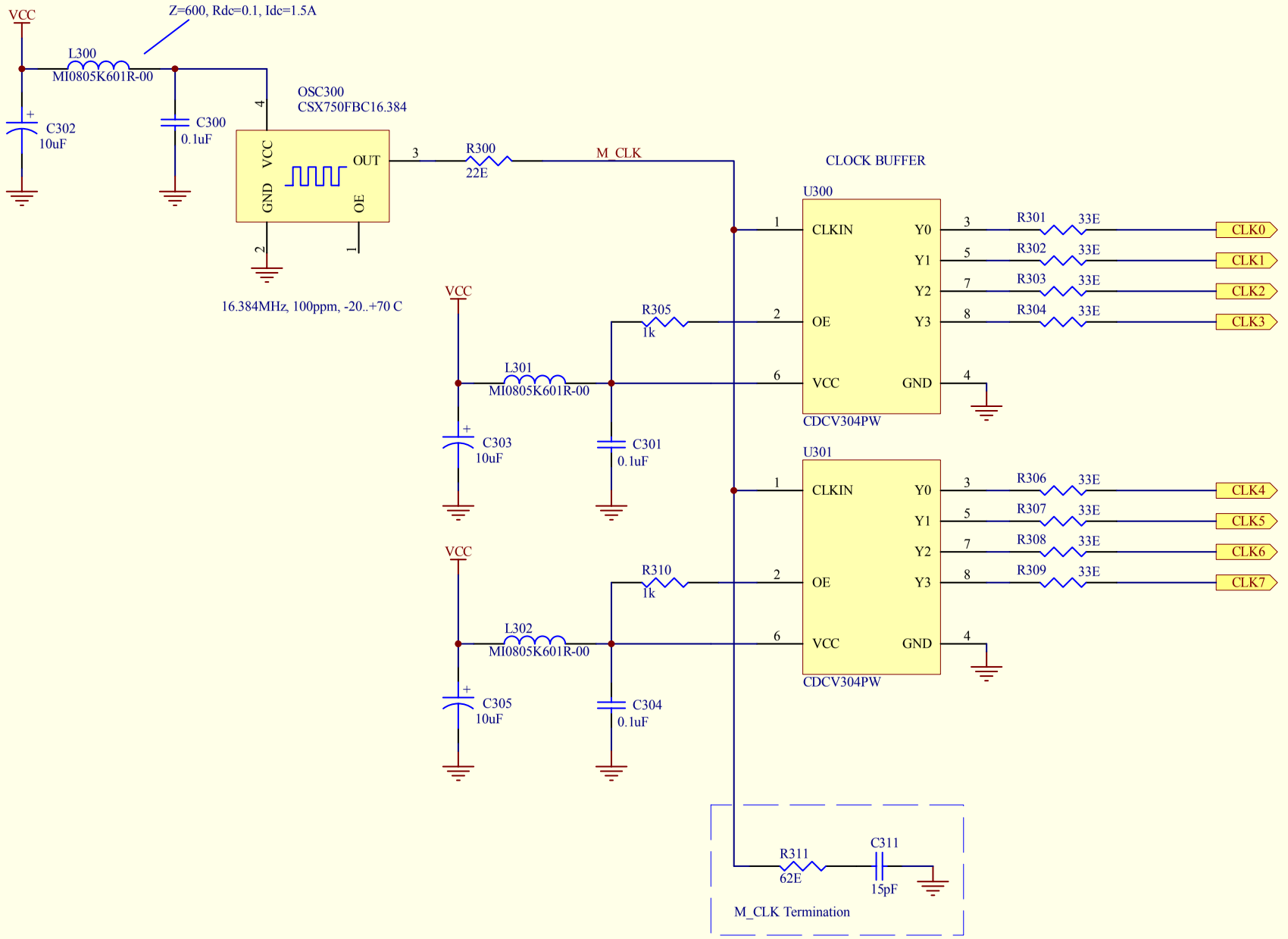


Additional DSP VCORE bulk



Nolte that each DSP has its own VCORE bulk capacitors.

Title **DSP Power Supply**			*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:32		Sheet 8 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DSP PS.Sch			



Suitable Oscillators:

1. Citizen America Corp. (CSX750 SMD oscillator)
   a. CSX750FBC16.384000MTR
   b. CSX750PBC16.384000MTR
   c. CSX750FBC12.000000MTR
   d. CSX750FBC24.000000MTR

2. CTS-Frequency Controls
   a. CB3LV-3C-16.3840-T

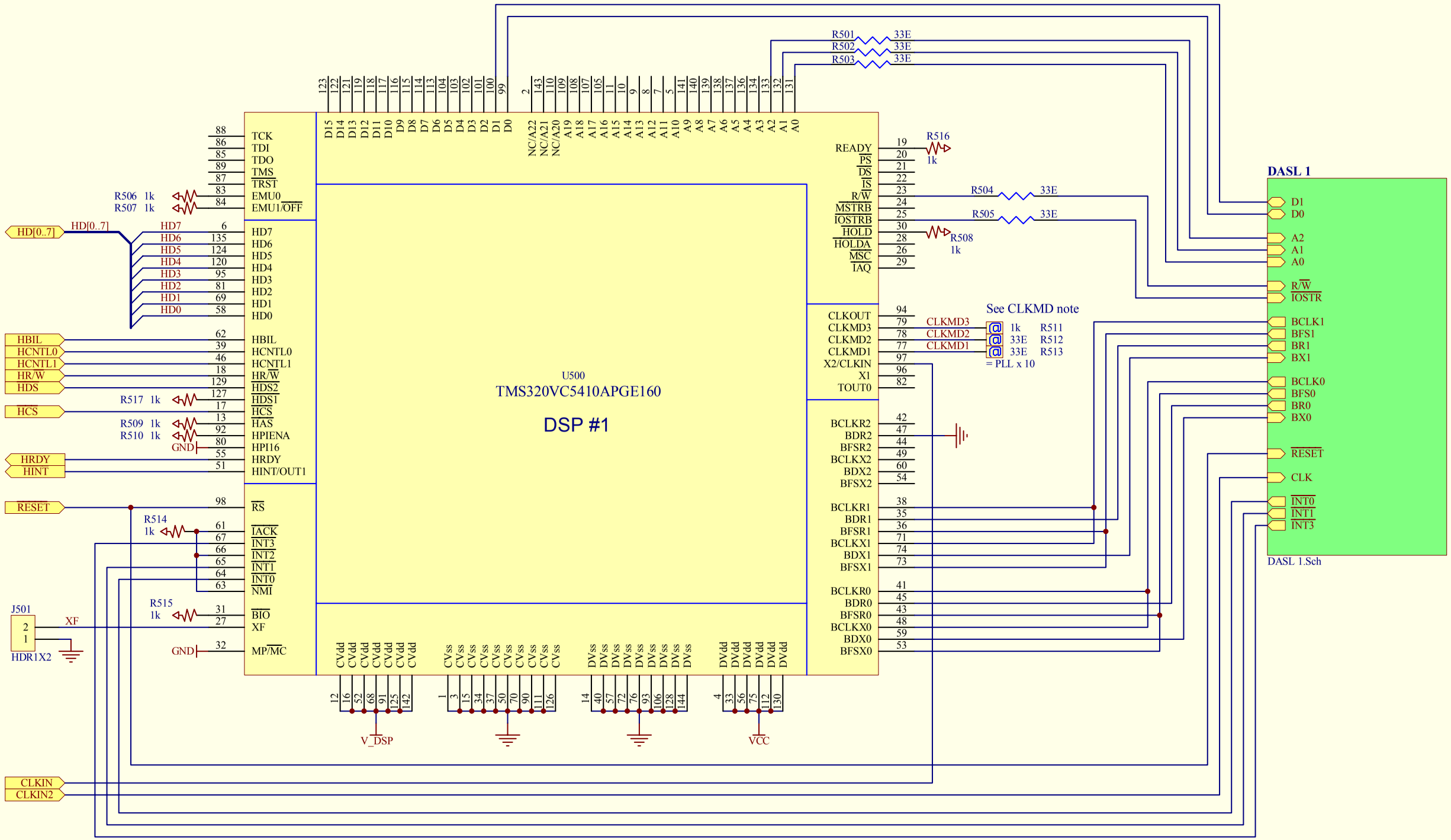
These are 5V, check for 3.3v availability:

-. EPSON
   a. SG-8002CA 16.384 MHz

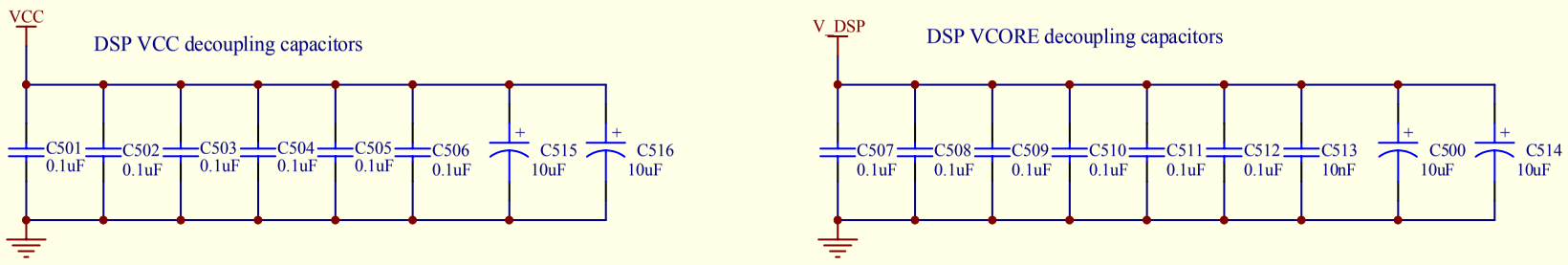
-. C-MAC (CFPS-72 SMD oscillator)
   a. 16.384MHz CFPS-72I C

-. Ratron (CO43 or CO47 SMD oscillator)
   a. CO4310-16.384-EXT-T
   b. CO4710-16.384-EXT-T

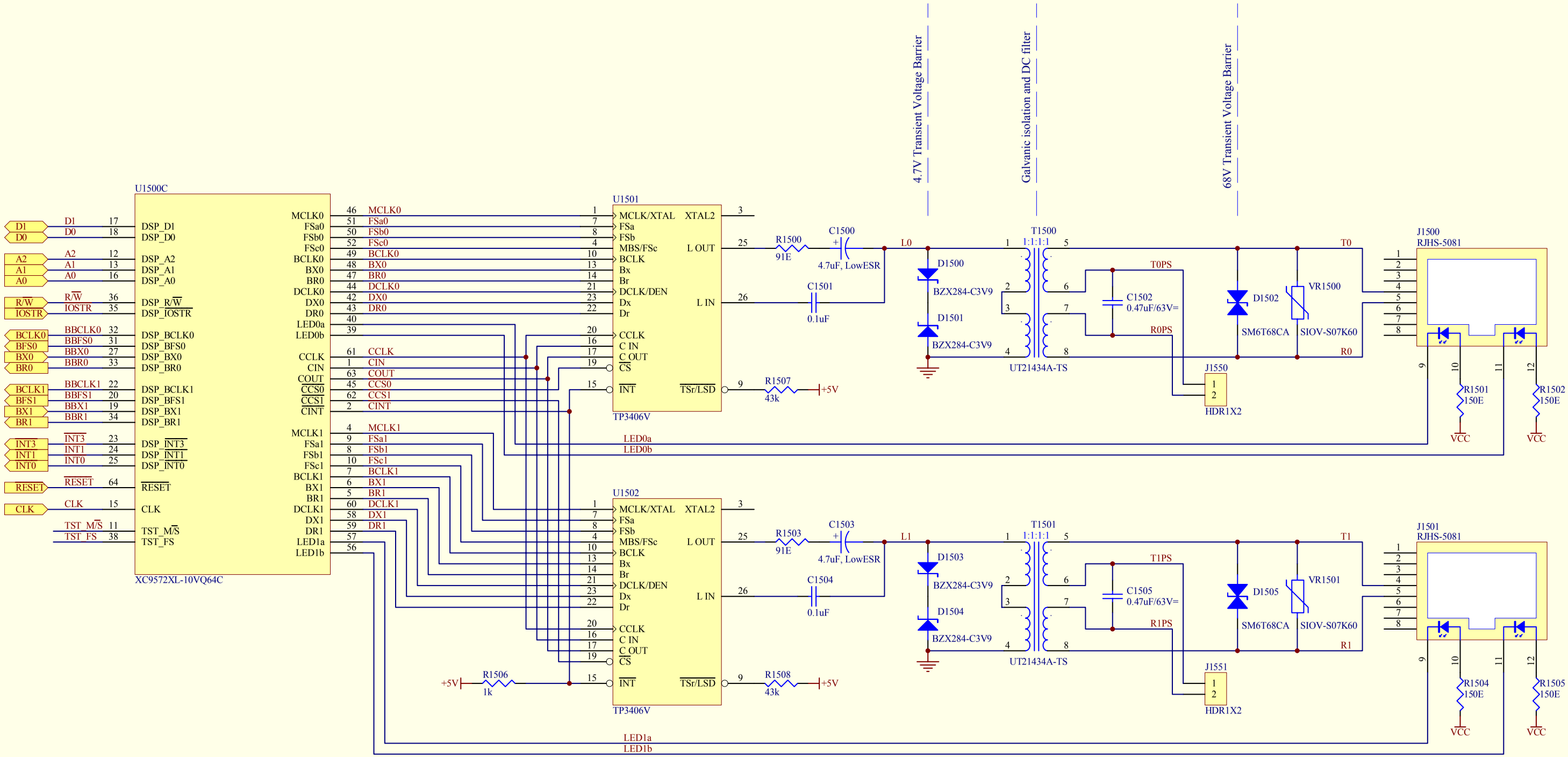
Title **DSP Time Base**		*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A
Date: 19-Mar-2006 Time: 22:51:32	Sheet 9 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DSP Time Base.Sch		

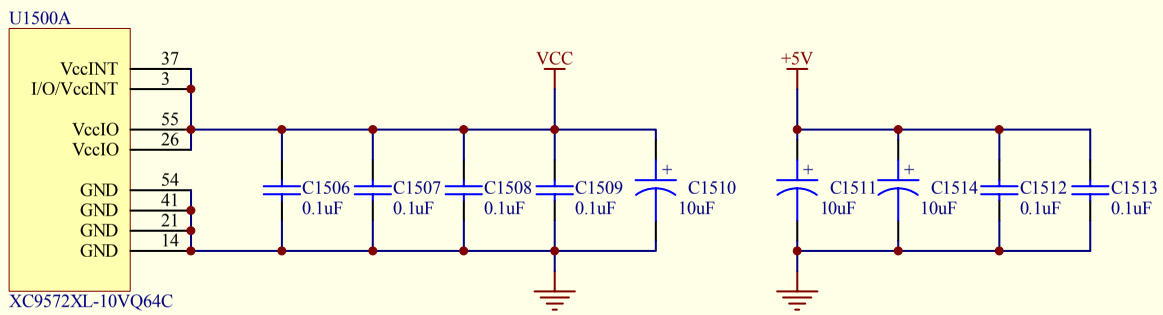


CLKMD 1 2 3	CLKMD VALUE	CLOCK MODE
0 0 0	0000h	1/2 (PLL disabled)
0 0 1	9007h	PLL x 10
0 1 0	4007h	PLL x 5
1 0 0	1007h	PLL x 2
1 1 0	F007h	PLL x 1
1 1 1	0000h	1/2 (PLL disabled)
1 0 1	F000h	1/4 (PLL disabled)
0 1 1	-	Reserved

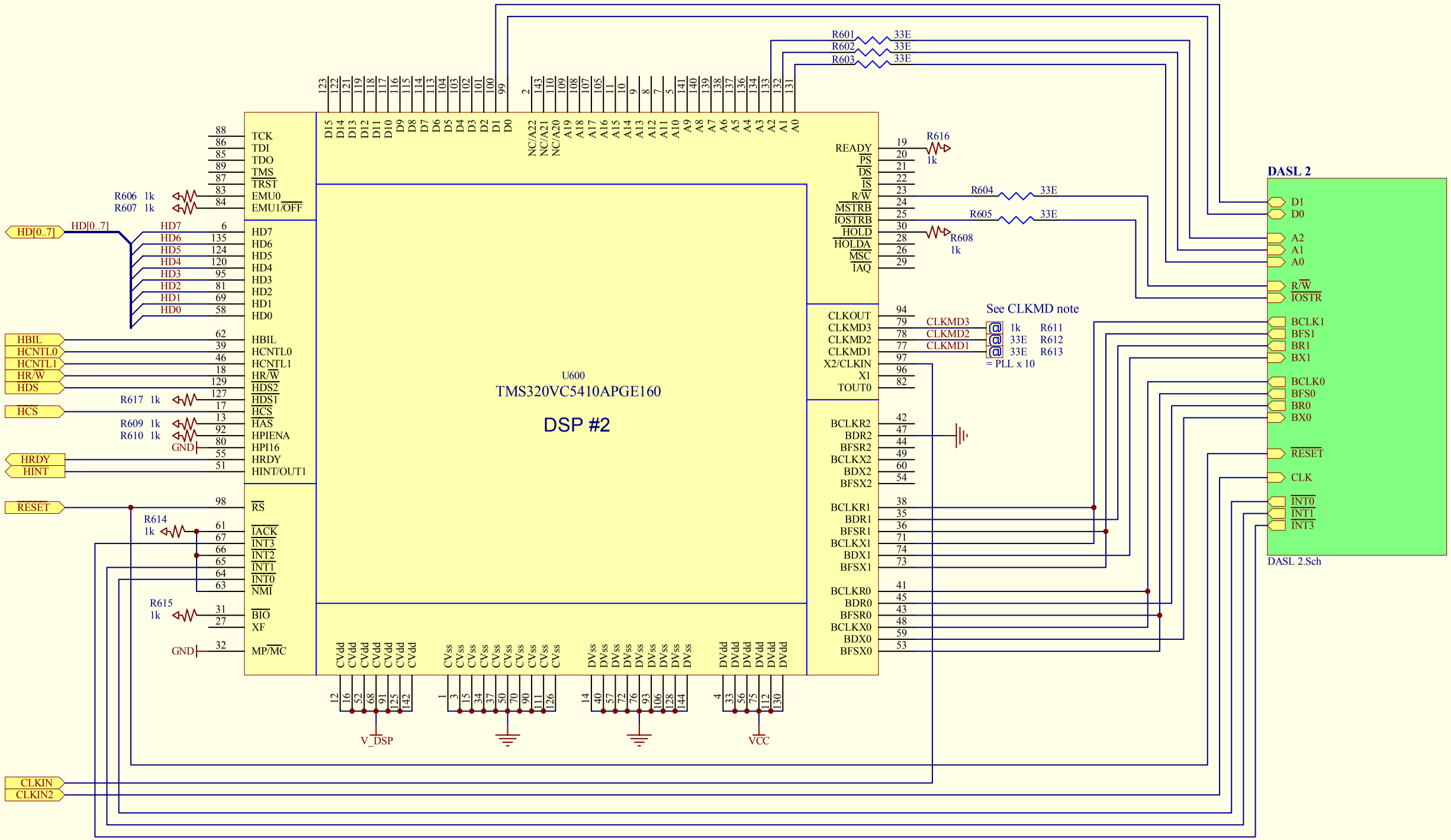


Title: ***DSP Core 1 of 3***		*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A
Date: 19-Mar-2006 Time: 22:51:32	Sheet 10 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DSP Core 1.Sch		

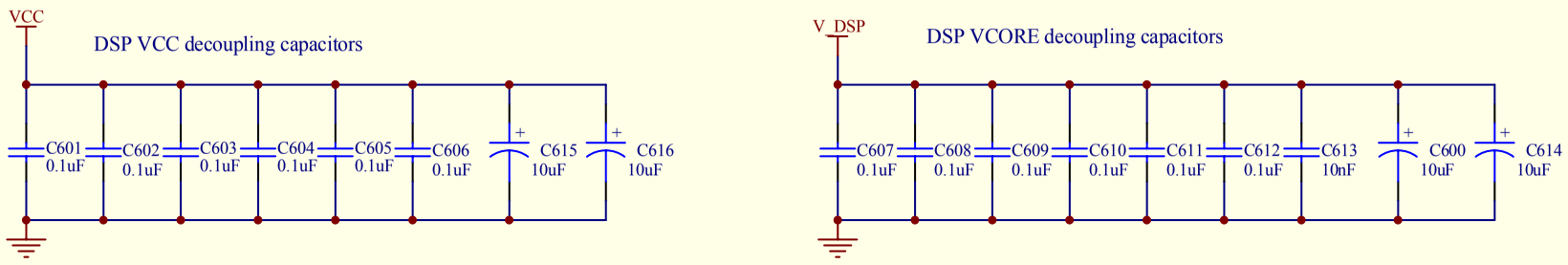




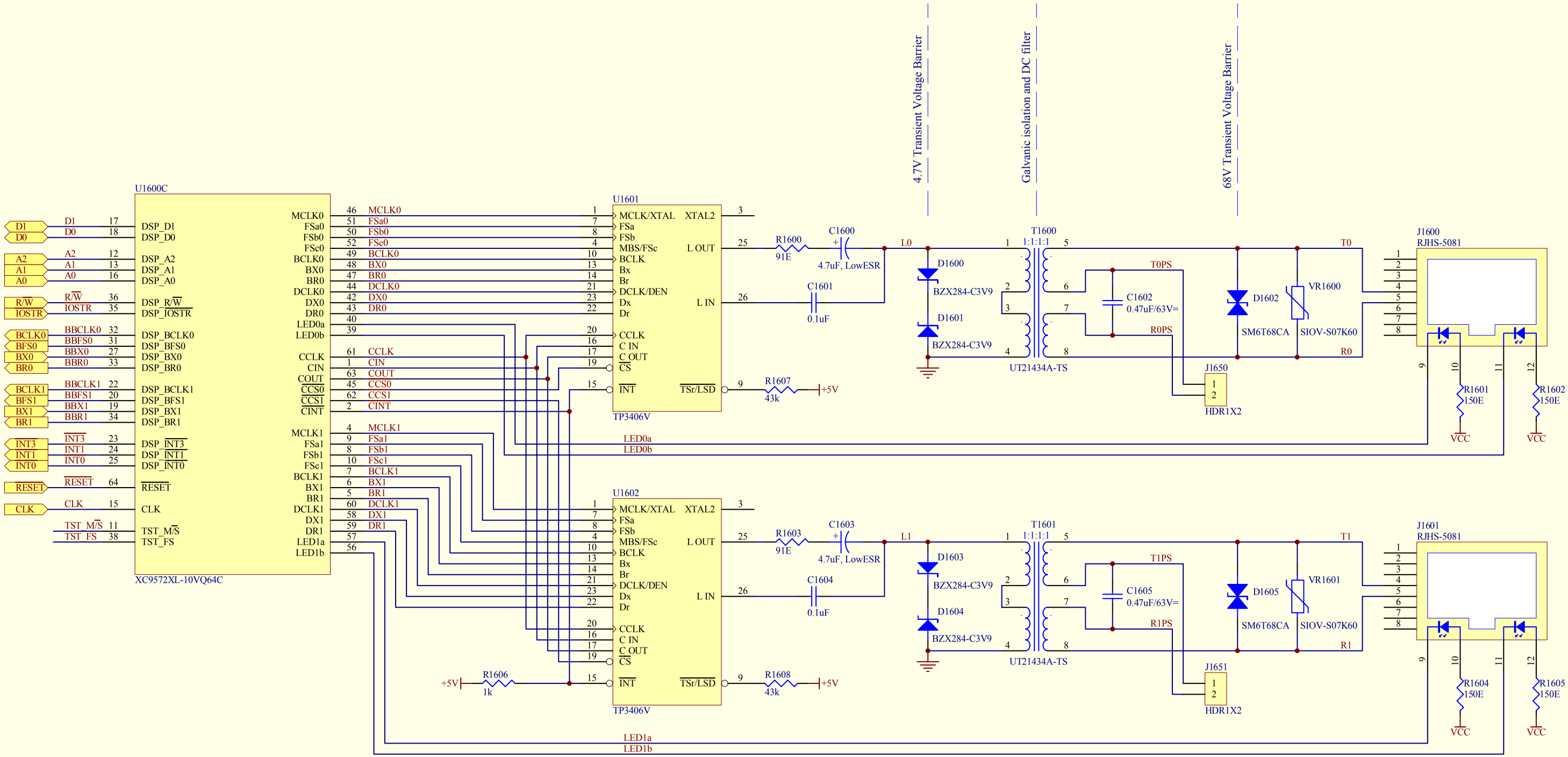
Title: ***DASL Pair: 1 of 3***		*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A
Date: 19-Mar-2006 Time: 22:51:33	Sheet 11 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DASL 1.Sch		

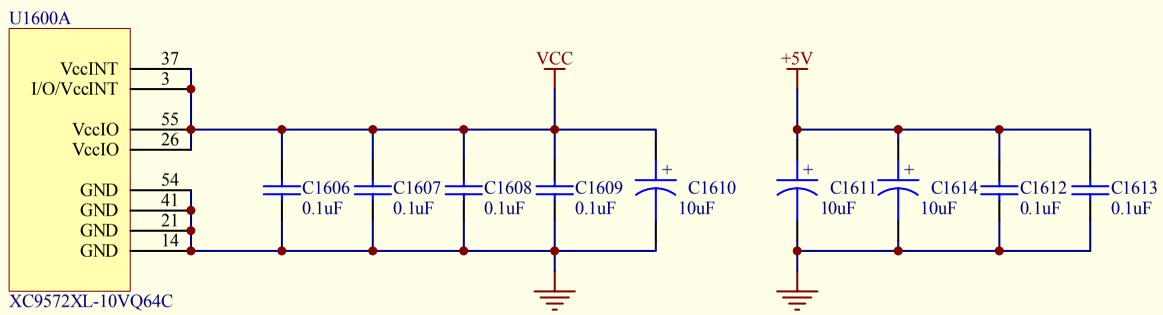


CLKMD 1 2 3	CLKMD VALUE	CLOCK MODE
0 0 0	0000h	1/2 (PLL disabled)
0 0 1	9007h	PLL x 10
0 1 0	4007h	PLL x 5
1 0 0	1007h	PLL x 2
1 1 0	F007h	PLL x 1
1 1 1	0000h	1/2 (PLL disabled)
1 0 1	F000h	1/4 (PLL disabled)
0 1 1	-	Reserved

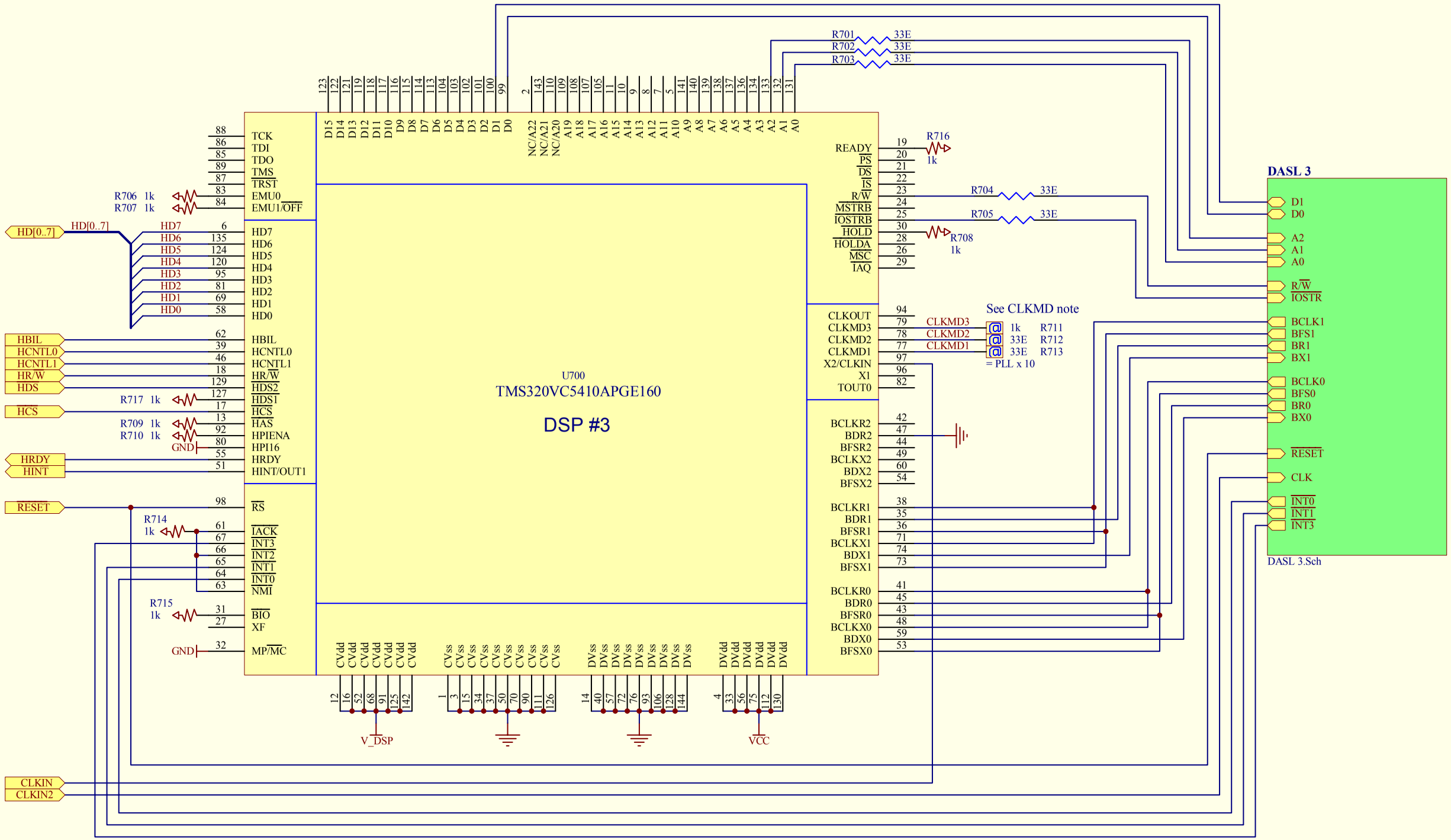


Title: ***DSP Core 2 of 3***		*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A
Date: 19-Mar-2006 Time: 22:51:33		Sheet 12 of 15
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DSP Core 2.Sch		

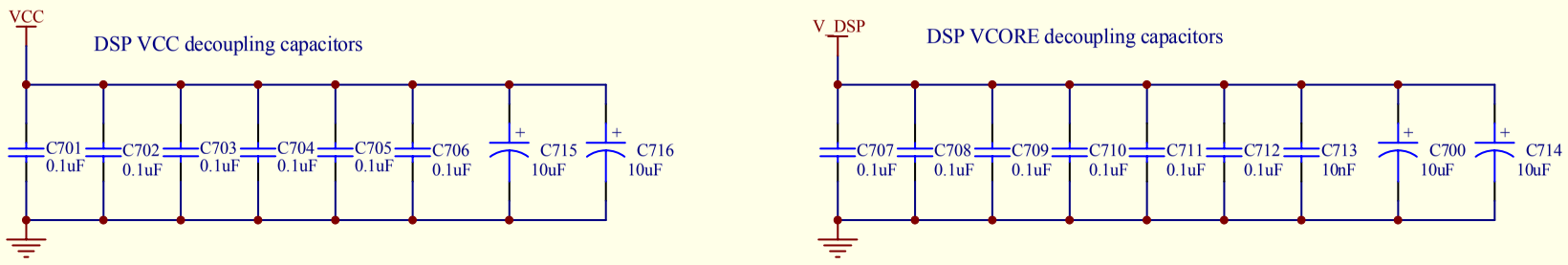




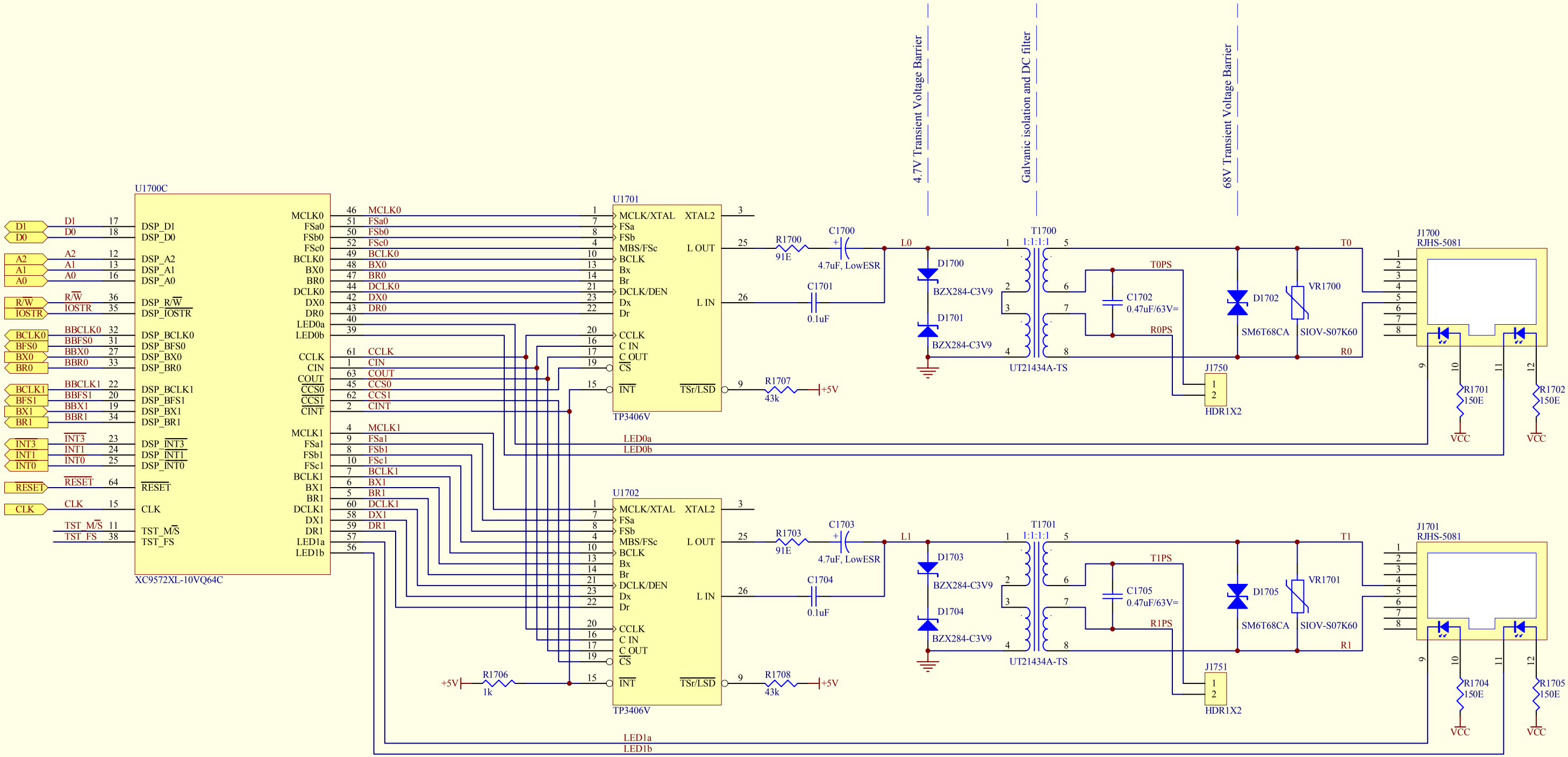
Title: ***DASL Pair: 2 of 3***			*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:33		Sheet 13 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DASL 2.Sch			

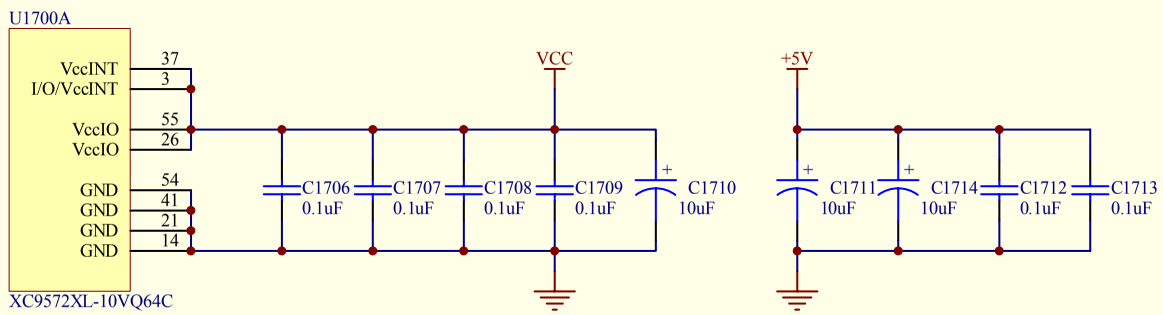


CLKMD 1 2 3	CLKMD VALUE	CLOCK MODE
0 0 0	0000h	1/2 (PLL disabled)
0 0 1	9007h	PLL x 10
0 1 0	4007h	PLL x 5
1 0 0	1007h	PLL x 2
1 1 0	F007h	PLL x 1
1 1 1	0000h	1/2 (PLL disabled)
1 0 1	F000h	1/4 (PLL disabled)
0 1 1	-	Reserved



Title: ***DSP Core 3 of 3***		*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A
Date: 19-Mar-2006 Time: 22:51:33		Sheet 14 of 15
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DSP Core 3.Sch		





Title: ***DASL Pair: 3 of 3***			*IPTC Tech. Comm. AB* *Pyramidbacken 6* *141 75 Kungens Kurva* *Sweden*
Size: A3	Number:	Revision: R2A	
Date: 19-Mar-2006 Time: 22:51:34		Sheet 15 of 15	
File: C:\WORK\DEX28\XLU28\XLU28.ddb - Doc\GE6P R2B\DASL 3.Sch			