Prepared	Subject Responsible	Document Identity		
Mikica B Kocic	Mikica B Kocic	1ad647f3-373d-4e1c-b469-9f32e9401cf8		
Approved / Checked		Date	Rev.	File
-		2006-11-07	R5	-

CONFIDENTIAL

DEX28™ XPU-D™ Architecture

Introduction

XPU-D board is **a wildcard** for Ericsson ASB 150 02 PBX (BusinessPhone™), which means that XPU-D can replace CPU-D_, or any other ASB 150 02 device board like ELU, BTU or VMU-HD, and extend its functionality over VoIP.

Primary usage of the XPU-D board is for upgrading ASB 150 02 to be SIP based, as shown on the Figure 1.

In this case, XPU-D will be used instead of CPU-D_. XPU-D will run multiple *SIP User Agents* on existing analogue and digital extensions, and connect them to new Ericsson SIP based IP-PBX. This should help smooth transition for existing ASB 150 02 users to new Ericsson IMS concept.

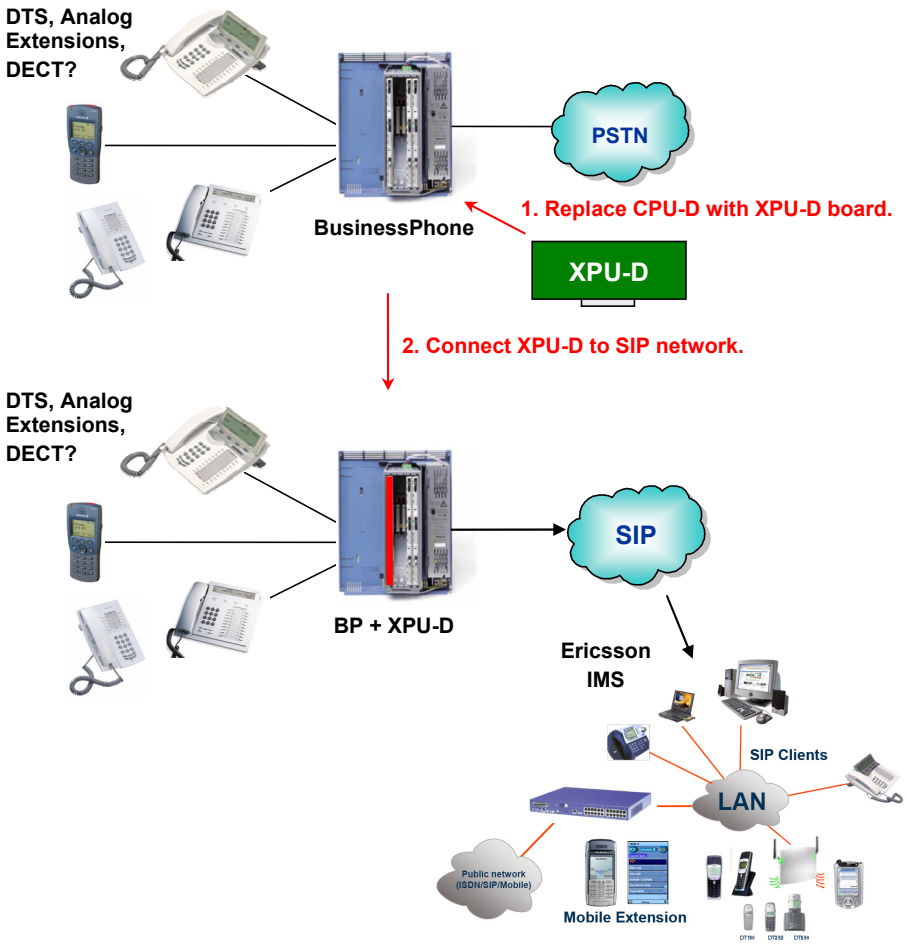


Figure 1: ***XPU-D Instead Of CPU-D in Existing ASB 150 02 Installation***

Advanced Applications

XPU-D is versatile board and it could have other applications like:

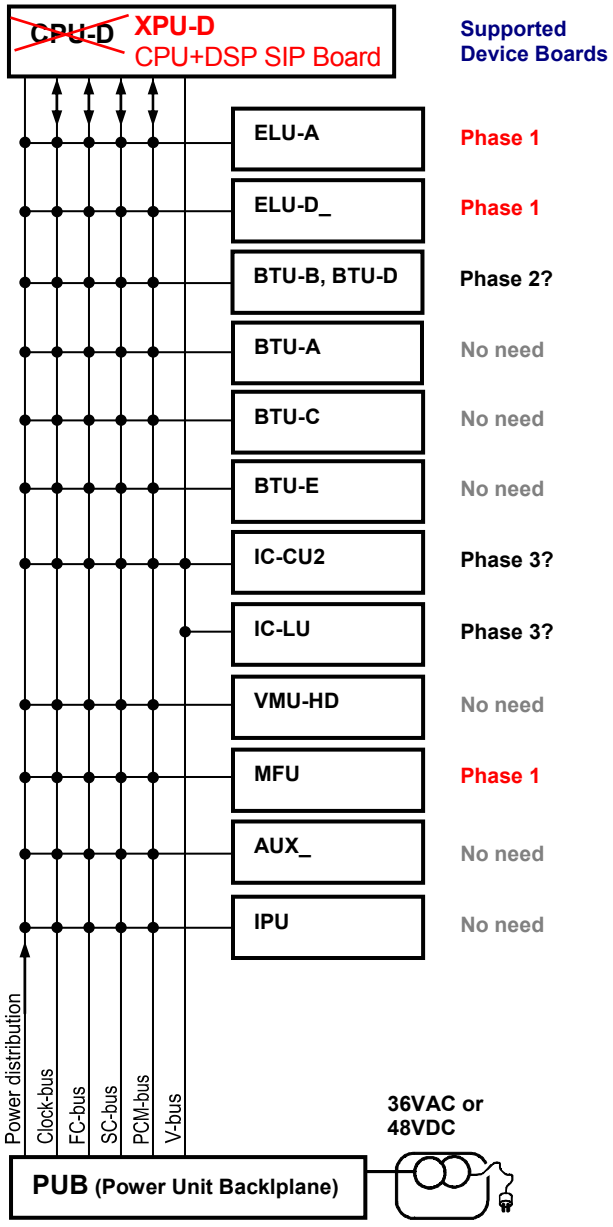
- Voice and backplane signal recording and trace, directly from ASB 150 02 backplane
- VoIP Media gateway to BRI/PRI when using with BTU-B and BTU-D boards
- Replacement of the BTU-D + HAL950 combination
- DECT-IP, etc.

XPU-D as ASB 150 02 CPU-D Development Path

Development of XPU-D, as a CPU-D wildcard, consists of three phases:

- **Phase 1**: XPU-D supports **extension** device boards[1]. *Certain.*
- **Phase 2**: XPU-D supports **both-way trunk** device boards. *Probable.*
- **Phase 3**: XPU-D supports **cordless** device boards. *Possible but not so probable.*

Following diagram shows supported device boards per phase in more detail:



CPU-D_	Board containing the central parts of the PBX's control system.
XPU-D	SIP enabled replacement for the CPU-D_ board.
ELU-A	Board for connecting analogue telephones
ELU-D_	Board for connection of digital telephones
BS	The radio Base Station is connected to the IC-LU and establishes the radio link to the portables
BTU-A	Board for "analogue" connection to the public telephone network or other telephone exchanges
BTU-B	Board for "digital" ISDN connection to the public exchange and terminal equipment in the 2B+D format on up to 8 lines.
BTU-C	Board for "analogue" tie and trunk line with current loop (DC-loop) to connect to other telephone exchanges or public networks incl. DID for some countries
BTU-D	Board for "digital" connection 30B+D to the public exchanges. The board also contains register signaling equipment
BTU-E	Board for "analogue" tie line with E&M signaling for connection to other telephone exchanges.
CM	Call metering board is a daughter board to be installed on a BTU-A or -C for detection of 12/16 kHz and 50 Hz metering pulses
IC-CU2	Controls the DECT cordless system and interfaces to up to 4 base stations (only index2). In the ASB 150 02 system this board acts like an ELU board in the PBX
IC-LU	Provides ADPCM conversion, handling of communication, echo canceling and synchronization of the Base Stations.
IPU	Gateway between the circuit switched and the IP based telephony in conjunction with a corporate LAN/WAN environment.
MFU	Multi function unit comprises 4 analogue extensions with 4 DTMF receivers, 8 digital extensions, 4 ISDN T/S- interfaces and a voice memory function similar to the VMU-HD with 4 registers and 4 voice channels.
REG	Sub-equipped BTU-D, including only the register function
VMU-HD	Board for recording/playback of messages and announcements stored on a PCMCIA flash disk and register function
AUX_	Board providing up to 3 V.24 interfaces to connect devices e.g. PC, printers. The AUX3 provides just 1 V.24 interface
PUB	Back plane with rectifier, voltage converter and five to nine board positions supporting Integrated Cordless functionality.

NOTES:

The boards BTU-A, ELU-A and ELU-D are also available as sub-equipped boards with reduced number of interface lines.

[1] Part of the *Phase 1* is also voice and signal recording and real-time tracing functionality in high-impedance state.

ASB 150 02 Upgrade Overview

Small, single cabinet ASB 150 02 is upgraded by replacing existing CPU-D with XPU-D and configuring XPU-D to connect to SIP network, as shown in Figure 2.

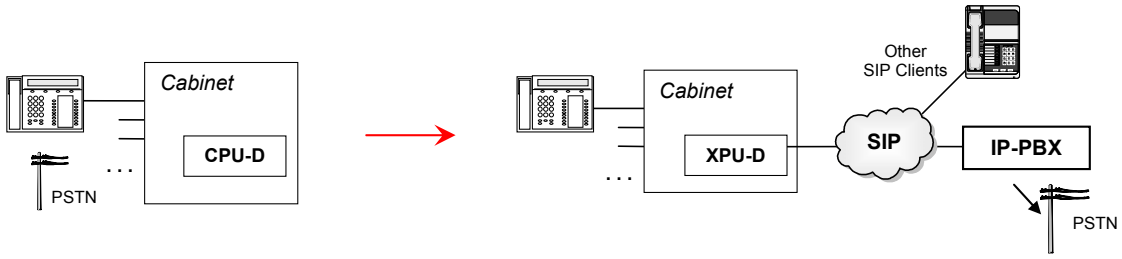


Figure 2: ***Upgrading Small ASB 150 02 with XPU-D***

Large, multi cabinet ASB 150 02 is upgraded by removing existing CPU-D (together with flat-ribbon backplane extension cables between cabinets), and then placing separate XPU-D in each cabinet in empty CPU slot, as shown in Figure 3.

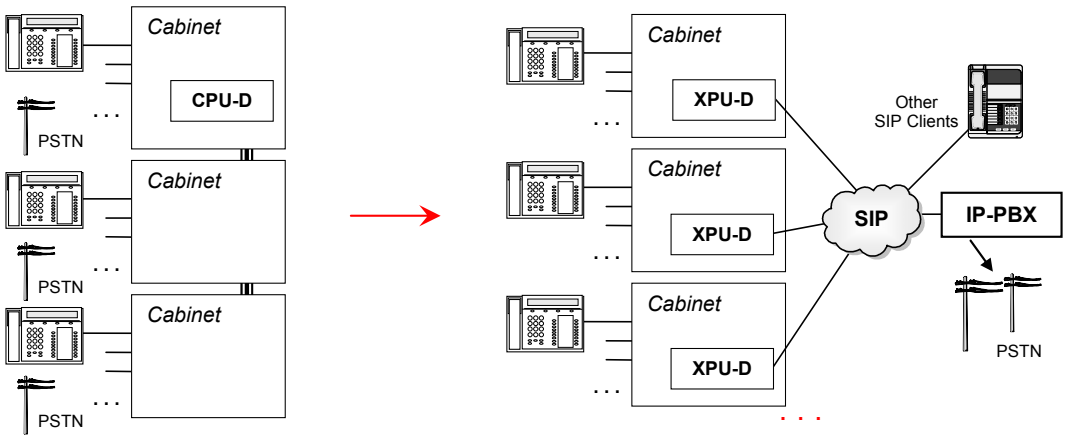


Figure 3: ***Upgrading 3-Cabinet ASB 150 02 with XPU-D***

Note that number of ASB 150 02 is *not limited* in the system based on XPU-D. New cabinets could be joined (from old installations) or added with ease, thus breaking through the limit of 300 extensions per ASB 150 02 system.

SIP Functionality Distribution

ASB 150 02 system equipped with XPU-D is more decentralized and distributed than as it was with CPU-D_.

Directory Numbers database, call setup processing, presence database, call metering and other common functions are transferred to remote IP-PBX, leaving only SIP User Agent[2] functionality on ASB 150 02 locally, as is shown on the Figure 4.

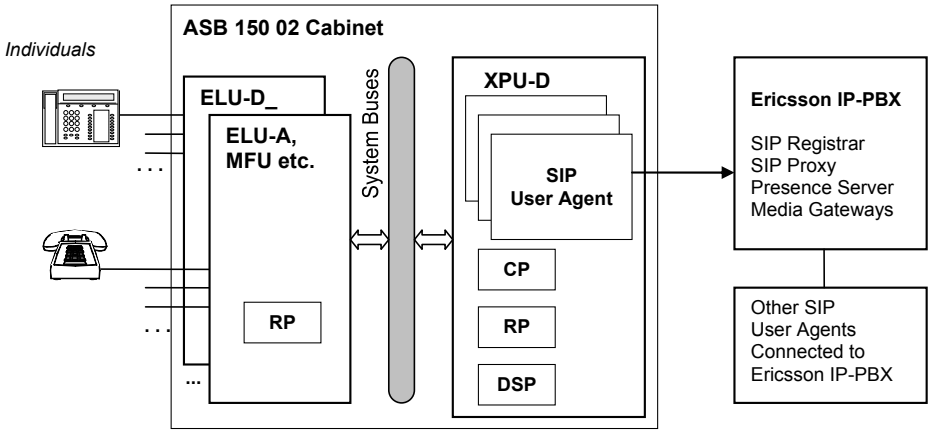


Figure 4: ***XPU-D SIP Functionality Distribution***

Following table summarizes distribution of SIP functionality across XPU-D and Ericsson IP-PBX.

Table: SIP Functionality Distribution

XPU-D Domain	Ericsson IP-PBX Domain
• Runs one User Agent per individual • User Agents are Linux processes • DTS are considered as Linux multimedia terminals with display, keyboard and full duplex audio • User Agents handles individual presence and connection information • PCM-bus time slots are resources. If exhausted, User Agent indicates congestion.	• Directory Numbers Database • Call Setup Handling • Presence Information Database • Call Metering • Media Gateways … Also other SIP User Agents connected to Ericsson IP-PBX.

[2] Also media gateways functionality if it is planned that XPU-D supports BTU cards.

System Capacity and Limitations

Plain ASB 150 02 has all call processing power concentrated in single CPU-D_ board, common for the whole system. Also, all cabinets share the same backplane buses, in particular two PCM buses, each having 64 both-way time-slots connected to single multipoint switching and conferencing unit (MUSAC). In case of the normal traffic a maximum of 120 individuals can be involved in a trunk to trunk connection, trunk to extension connection or extension to extension connection and vice versa. This gives a *maximum of speech 60 channels capacity*, visualized on Figure 5.

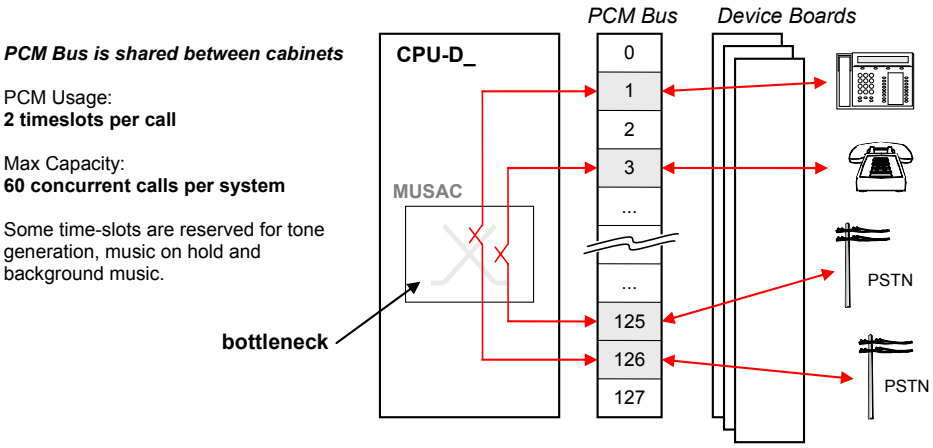


Figure 5: PCM Time-Slots Usage in Plain ASB 150 02

Contrary to this closed cabinet system, XPU-D uses "**divide and conquer**" philosophy to increase system capacity to 384 concurrent calls in 3-cabinet system: *each cabinet* is equipped with XPU-D, and MUSAC functionality is replaced by the switching on LAN.

The XPU-D utilizes one time-slot per call, which can be seen in typical call setup shown on Figure 6.

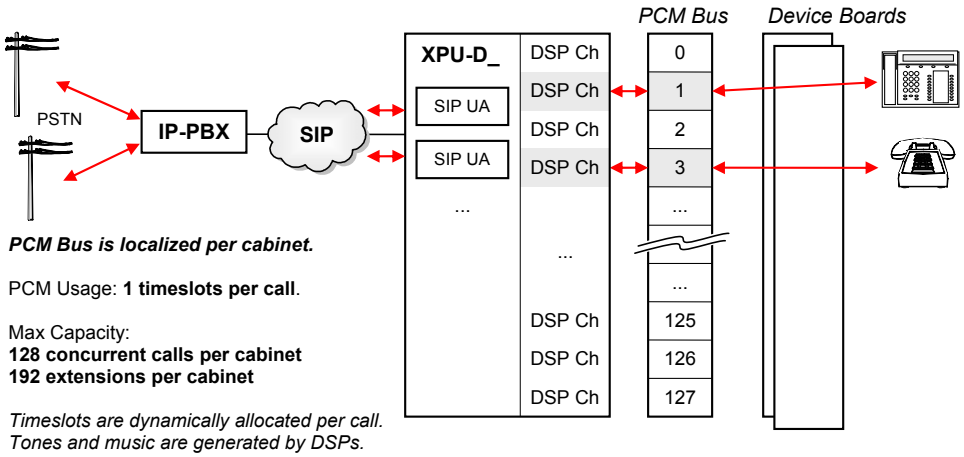


Figure 6: PCM Time-Slots Usage in XPU-D Enabled ASB 150 02

Cabinet connection over LAN eliminates need for flat-ribbon cable connection between cabinets, resulting in increased voice speech capacity and greater maximum traffic, beside with greater modularity and better distribution of processing power and resource handling.

Maximum traffic for 3-cabinet system is now 365 Erlangs at 1.5% grade of service (GOS), because PCM buses are localized per cabinet (not shared between cabinets) and call uses one time-slot only.

Directory number limitations are also removed, because call processing and directory number database are in responsibility of IP-PBX.

Table: SIP-Based and Old ASB 150 02 System Capacity Comparison Summary

XPU-D equipped ASB 150 02	Old ASB 150 02
Maximum number of cabinets: **unlimited** Maximum number of boards: **no limits** per system, 6 boards per cabinet *Cabinets are individually connected to LAN. The system is not limited in size.*	Maximum number of cabinets: **3** (BP250), 2 (BP128i) or 1 (BP50) Maximum number of boards: **total 27** per system, 6 boards per cabinet *Cabinets are connected by flat-ribbon cable and share common backplane bus.*
Maximum number of concurrent calls: **128** per cabinet 3 cabinets with 384 extensions have capacity for maximum **384 concurrent calls**. *Tone generation is DSP task and is individual per channel, meaning that every individual can have different music-on-hold and country specific tone settings. Tones are generated from plain wav files. Music-on-hold and background music from MP3. Number of concurrent calls is, in fact, limited by available DSP processing power, which is scalable.*	Maximum number of concurrent calls: **60** for the whole system 3 cabinets with 250 extensions have capacity for maximum **60 concurrent calls**. *System reserves ca 4 channels for tone generations, music-on-hold and background music.* *Also, the system is limited by maximum number of trunks, which is typically 60 in the largest system.*
Maximum traffic (3 cabinets): **365 Erlang** at GOS 1.5%	Maximum traffic (3 cabinets): **48 Erlang** at GOS 1.5%
Maximum number extensions for the 3-cabinet system: **576** = 3 cabinets x 6 slots x 32 individuals	Maximum number extensions for the 3-cabinet system: 200 (**300** hotel)
Directory Numbers: Not limited as it is IP-PBX task.	Directory Numbers: 1000 external and 400 internal DNs

Operation and Maintenance

Maintenance of the XPU-D is possible both locally and remotely. It can be performed:

- locally over console interface (RS232 or USB)
- remotely or locally over web interface
- remotely or locally using SSH client
- remotely or locally using SNMP

Web interface follows existing DEX28 guidelines and provides a comfortable web browser GUI. No client installation is required as the web browser acts as a client.

All configuration parameters are stored as plain Linux files in single folder. System firmware is remotely upgradeable, either manually or automatically by the system itself. License information is stored on IP-PBX.

Web interface structure corresponds to the following menu tree:

Status: Device & Port, Connections
System Info: General, CPU, Memory, Disk, Users, Network, Kernel
Configuration: Network, SIP User Agents, Users, Date, Advanced, Backup
System Tools: System, Password, Network, Update
Log Files: Messages, Security, Transfer, Logins, Boot, DSP

Installation of the new system

System is preconfigured to get IP parameters using DHCP. When connected to the LAN with IP-PBX, it will retrieve SIP servers' parameters from DHCP server (IP-PBX) and enable user agents on all individuals. Device boards and individuals are auto enumerated. User agents offer free-seating connection menu on the DTS (with DN or user ID, password).

System administrator can also make static SIP identity per individual i.e. disable free-seating.

XPU-D Software Overview

ASB 150 02 Hardware and Software Overview

The ASB 150 02 system comprises a number of printed board assemblies that are interconnected via different common serial busses.

All central control (processing) equipment is located on the CPU-D_ board, together with support functions that are needed in all variants of ASB 150 02.

Several boards with the appropriate interfaces are available to connect equipment (e.g. telephones, other telephone exchanges, computers, printers) to the system.

The functionality of each device board provides the possibility to have several types of interfaces. It is possible for example, to mix telephone connections, and external tie lines on one board.

The regional processors report (on system start) to the central processor what types of boards are installed in the system, their positions and how many individual lines each board is equipped with, so that the central software "knows" the configuration of the installed system.

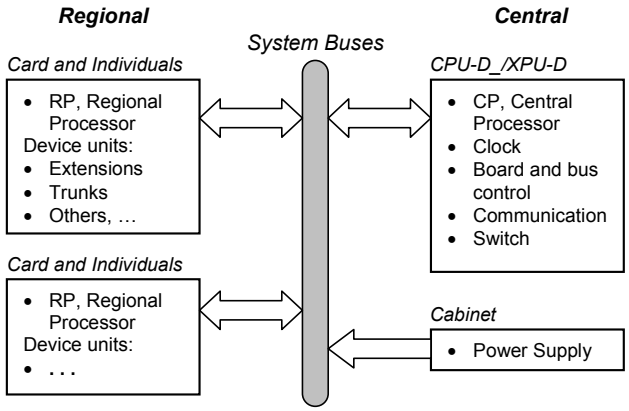


Figure 7: ***ASB 150 02 Hardware Concept***

The ASB 150 02 system software is structured in accordance with the ASB 150 02 hardware architecture:

- A central program controls the telephone traffic's switching logic as well as operation & maintenance functions. Each program block is divided into units with clearly defined functions within the block. Each program block administers its own data.
- A number of regional programs, one for each type of device board. The regional programs also consist of one or more program blocks with separated tasks and local data.

The program units communicate with one another by sending messages (signals). It is the central operating system's main task to distribute messages to the various parts of the system and to queue messages that are waiting to be executed.

XPU-D System Software

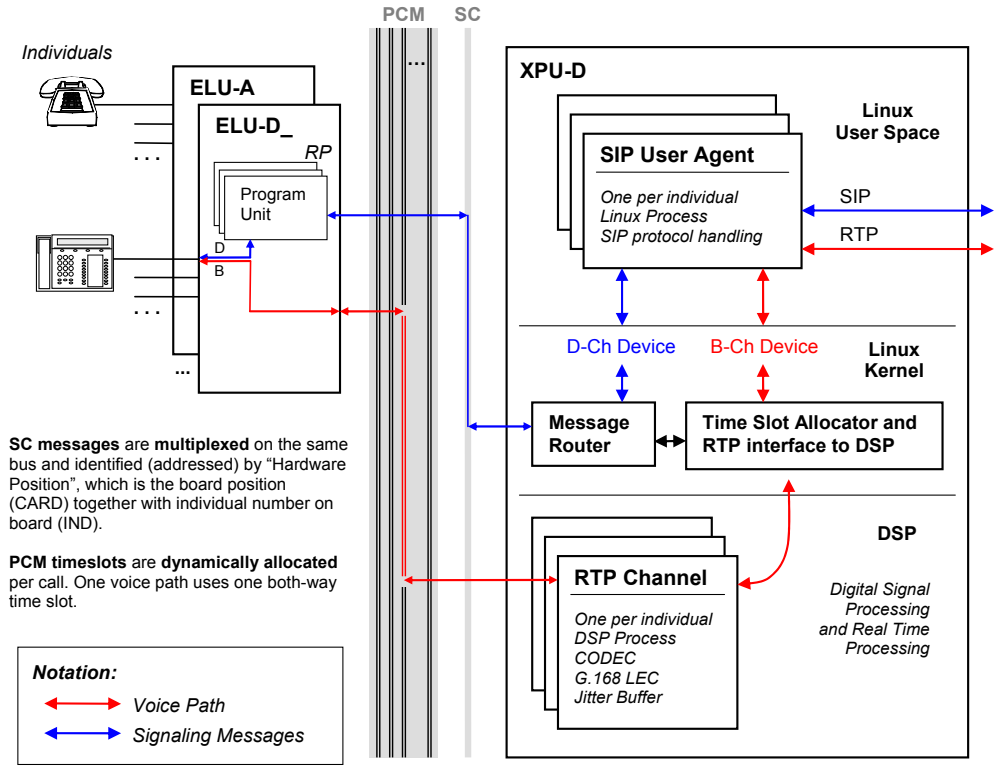


Figure 8: ***XPU-D System Software Block Diagram***

ASB 150 02 system software is divided into a number of regional and central program blocks. A program block administers a well-defined part of the system, certain hardware, a certain type of device, a certain function or a certain type of data.

A program block is usually divided into a number of program units, where each unit has its fixed function within the block. Program blocks communicate with one another by sending/receiving messages. Program units within a block communicate with one another by sending/receiving messages or via local function calls.

Data is administered mainly within a block. When data from a block is needed in another program block, it is requested with the help of messages between the blocks.

A signal input is the place in a program unit where messages (signals) are received.

The operating system in the central software has the task of linking all the parts in the entire system by functioning as distributor of the messages. The operating system in the regional software provides the corresponding features locally on a board. All operating systems have queues for messages waiting to be executed. Each operating system also offers support for local functions on the relevant boards.

Within the system each device board position, each individual device on a board and each signal input in the system has a number to be able to address messages. These numbers are used primarily for messages but are also used as reference for the storage of data and as identity in fault logs.

Regional Software

The regional software on all device boards administers the hardware and line interfaces.

The main task is to read out and verify hardware signals, e.g. key depressions, go off hook or receive incoming ring signals. Furthermore, orders from the central software shall be executed, e.g. flashing LED, start ring signals, generate a tone signal or connect the device's voice channel to the PCM-bus.

It is a system principle (for off-loading the central processor) that all details in the line interfaces shall be administered locally by the regional software. Only functional signals type "call", "digits" or "disconnection" are sent onwards to the central software. All time-critical monitoring is administered by the RP (that is time measurements from milliseconds and upwards).

Data for selection of different settings is stored by the central software and is sent to RP on system start or in conjunction with reprogramming.

Central Software

The central software is running on XPU-D and has master control of all telephony and operation & maintenance functions.

The task of the central software is to receive messages (from RP) concerning verified events, analyze them with regard to the status the device possesses (idle, digit transmission, speech state etc.) and to take appropriate measures as a consequence (interconnect devices, start ringing, etc.).

Central software is divided in two strict parts: real-time critical part and non real-time part.

Real-time part is running on DSP array and is concerned with voice processing. Each DSP has own small real-time operating system and it runs multiple real-time tasks in parallel. Each voice channel has its own set of tasks handling voice compression/decompression, line echo canceling and adaptive play-out buffer (de-jitter buffer).

Non real-time is Linux based and runs on the main CPU. Linux distribution is Fedora Core based.

XPU-D R2A program code is stored in ext3 file system and residing in Compact Flash (CF) card.

XPU-D R1A program code can be stored either in yaffs file system in NAND flash directly connected to CPU, or ext3 file system residing in Secure Digital (SD/MMC) card.

Addressing

For communications between different units in a system a special form of addressing is required. In this system addressing is structured in the following manner:

Identity code (ID-CODE).

Identifies a signal input in a program (a program unit), a program-process and/or an individual device within the entire system.

Complete ID-CODE is used for addressing messages between different program units, and consists of four parameters:

ST Signal type (signal input)
SN Signal number (process number)
CARD Board position
IND Individual number on a board

Central software

Software identifier is called for *Job signal* and comprises two parameters, signal type (ST) and signal number (SN).

ST (8-bit value 64–251, hex 41–FB) is used by the operating system to identify a signal input in a program unit in the central software.

SN is used locally by the program unit, normally in order to be able to differentiate between several concurrent processes (calls) for a specific individual.

Regional software

“Hardware position”, is called for “individual address” and comprises the two parameters, board position (CARD) and individual number (IND).

CARD (6-bit value 0-63) is the number of the board position at which a certain device board is inserted. The number is permanently encoded in the back plane of the cabinet and is read by the board's RP.

IND is the number of a specific individual on a board, such as the individual telephone line or another unit on a device board.

XPU-D Hardware Overview

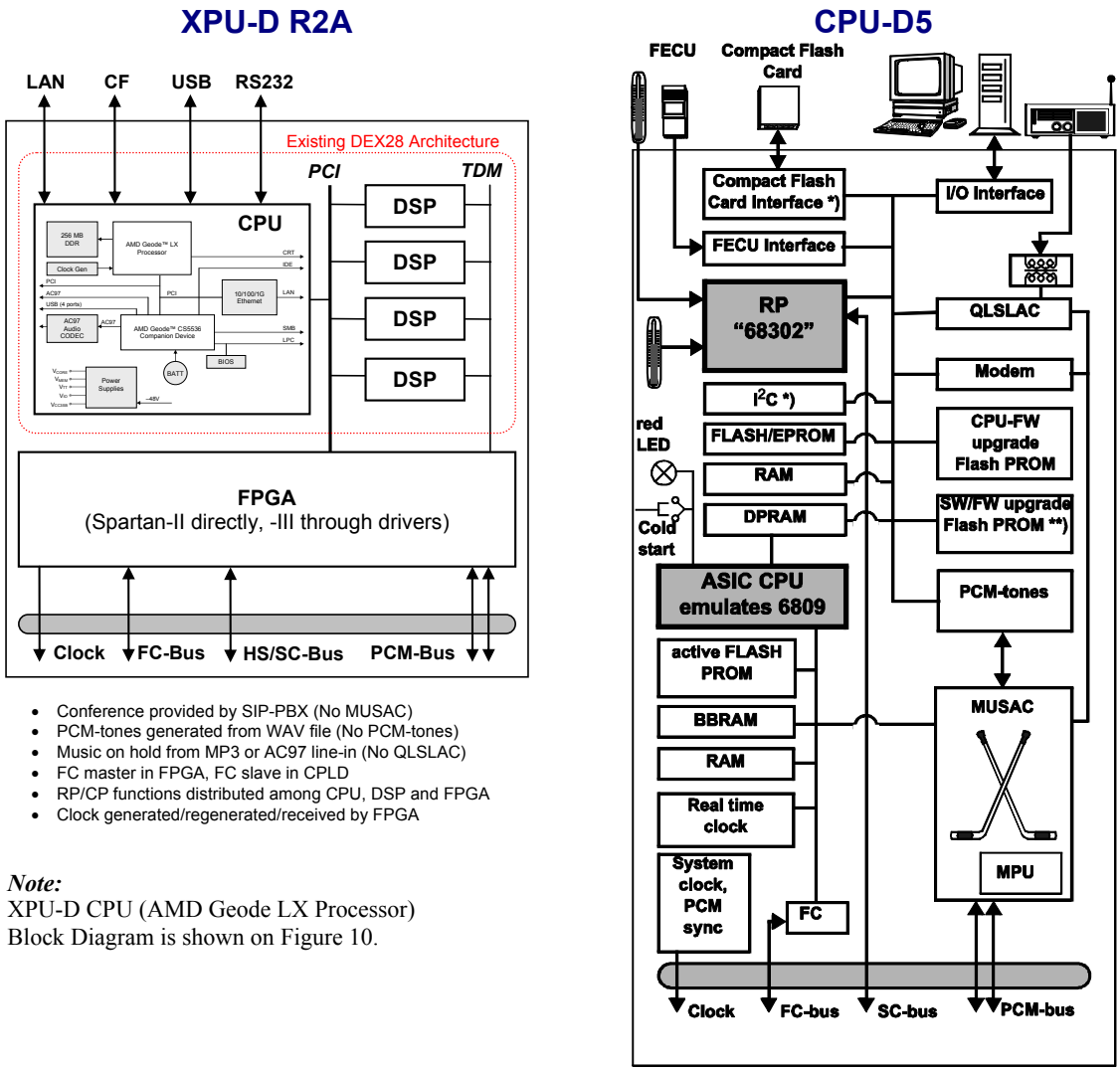
At the present, there are two different XPU-D hardware releases:

R1A Lab board, used *in development* of R2A.
R2A *Under development* and aimed for full production.

Major difference between releases is that R1A is much simpler, and the hardware architecture of both releases will be described more detailed in further text. Software created for R1A should work on R2A without modifications.

XPU-D R2A (Production) Board

This board is under current development, and it is actual board that will be used in full production. Block diagram of the R2A compared to CPU-D5 is shown on the Figure 9.



- Conference provided by SIP-PBX (No MUSAC)
- PCM-tones generated from WAV file (No PCM-tones)
- Music on hold from MP3 or AC97 line-in (No QLSLAC)
- FC master in FPGA, FC slave in CPLD
- RP/CP functions distributed among CPU, DSP and FPGA
- Clock generated/regenerated/received by FPGA

Note:
XPU-D CPU (AMD Geode LX Processor) Block Diagram is shown on Figure 10.

Figure 9: ***XPU-D R2A and CPU-D5 Block Diagrams***

XPU-D R2A Board Characteristics

(Proposed and not final.)

- AMD Geode™ LX 800@0.9W processor (500 MHz, 200 MHz front-side bus)
- PC2100 / PC2700 / PC3200 DDR SODIMM up to 512 MiB
- Processor integrated peripherals
  - TFT/CRT display support
  - PCI 2.2 and 3.0
  - Security Block (AES hidden key storage, random number generator)
- Companion device additional integrated peripherals
  - ATA controller (66 MB/s IDE, supports two UDMA-66 devices)
  - USB Host (four 2.0 480 Mbit High Speed connections, CS5536 companion device only)
  - Flash interface (supports industry standard NAND and/or NOR Flash)
  - LPC (Low Pin Count) port
  - Infrared communication port
- Gigabit Ethernet (Realtek RTL8110SB)
- Xilinx Spartan-III (with 74ACT drivers for PUB) or Spartan-II (directly connected to PUB) (tbd)
- Xilinx XC9500XL for RP slave (optional)
- 2 to 4 Texas Instruments TMS320C6416 Fixed-Point DSPs (tbd)
- PCB: 6 layers

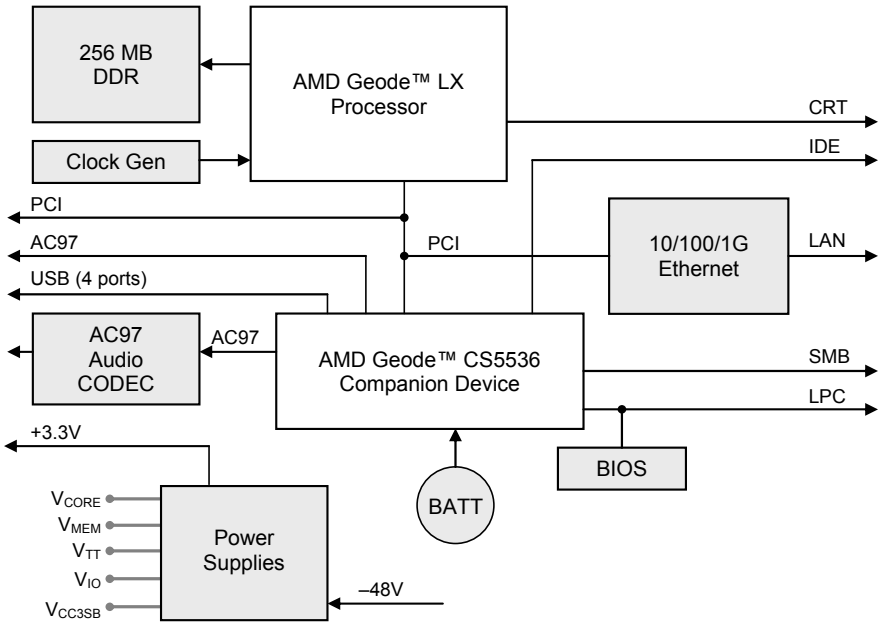


Figure 10: ***AMD Geode LX Processor Block Diagram***

XPU-D R1A (Lab) Board

This board is used for fast prototyping for ASB 150 02. It is used mostly for system buses sniffing, voice recording and wildcard ASB 150 02 device board signaling functional prototypes.

XPU-D R1A does not have DSPs, so it cannot perform complex voice processing functions. However, it is very simple and all communication and FPGA applications that are implemented on it could also run on more advanced R2A, and other similar DEX28 devices.

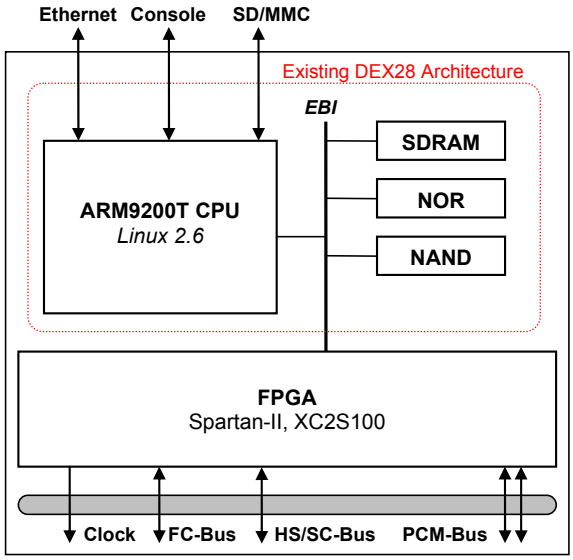


Figure 11: ***XPU-D R1A Block Diagram***

XPU-D R1A Board Characteristics

- Atmel ARM920T™ ARM® Thumb® Processor AT91RM9200
- 200 MIPS at 180 MHz, 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
- 64 MiB 32-bit SDRAM
- 256 MiB NAND Flash for Linux root file system
- 8 MiB NOR Flash for U-Boot, Kernel and Initrd storage
- Processor integrated peripherals
  - Three Synchronous Serial Controllers (SSC)
  - Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Multimedia Card Interface (MCI)
  - USB 2.0 Full Speed Host Double Port
  - USB 2.0 Full Speed Device Port
  - Master/Slave Serial Peripheral Interface (SPI)
  - Two-wire Interface (TWI)
  - Ethernet MAC 10/100 Base-T
- Miscellaneous Devices
  - Spartan-II 100 kGate FPGA in TQFP144 package as interface to ASB 150 02 Backplane
  - AVR (not mounted)
  - SD/MMC card
- PCB: 4 layers

XPU-D Connection to ASB 150 02 Backplane

General

PUB7 (hereafter = backplane) ROA 119 5135 (Power Unit Back plane) included in exchange cabinet BDV 11308.

In principle the backplane consists of a backplane bus connected to nine terminal blocks intended for nine ASB 150 PBAs (Printed Board Assembly, hereafter boards). The power supply for the boards, delivered by a DC/DC converter block with the outputs +5 V, +12 V and –12 V, is also situated on the backplane.

It is possible to replace boards during operation.

On the PUB7 buffers for bus connections to the next backplane are used. All buffer inputs are provided with Schmitt-trigger circuits implemented at buffer-inputs by means of a resistive feedback between the input and the output of each buffer.

All PCM-buses are connected to the next cabinet.

PUB7 is backwards compatible to PUB6.

Backplane Busses

Clock bus Clock signals and synchronization signals for coordination of the system's sub-functions.

FC-bus Function Control bus. Control of the connection of the individual boards to the backplane and restart of individual boards.

SC-bus System Communication bus. Communication link between the system processors.

PCM-bus Bus for voice connection between the individual devices, connected via the system switch.

V-bus Communication bus for the integrated cordless.

Interfaces

- Voltage distribution +5 V exists for each board position on pins C30 and C32
- Voltage distribution +12 V exists on each board position on pin A16
- Voltage distribution –12 V exists on each board position on pin C14
- Voltage distribution –48 V exists on each board position on pin A08, B08 and C08
- Voltage reference 0 V exists for each board position on pins B02, B04, C02, C04, A30,A32, B30 and B32. Pins C02 and A32 are extended.
- Voltage reference 0 V is also distributed via the flat-ribbon cable connector pins A5, B5, A12, A13, A14, A17, B14 and B15.
- The following bus signals have pull-up resistors on the backplane:
  HSSC, CTX, FCC, FCE, TPCM0, TPCM1, TPCM2, TPCM3, SYNC2, SYNC4, 8192kHz, 4096kHz
- The following signals are part of the DCT 1800 bus and have bus terminations near connector 108:
  VR_A, VR_B, VT_A, VT_B, ST

  The bus termination consists of two resistors and one capacitor. Note that the terminations are in the layout but only the pull-up resistors are mounted in PUB7.
- To make it possible to terminate the signals in the ribbon cable, the +5V supply-voltage has been wired to pin B7 of the right ribbon cable connector.

PBX with more than one cabinet

For larger systems the backplanes must be interconnected via a flat-ribbon cable 591 685/2. The backplane possesses block connectors on its right- and left- hand sides for connection of these cables and necessary signal buffers with Schmitt triggers implemented by means of a resistor feedback between the input and the output of each buffer. The output buffer to the next cabinet can be disabled by means of the DIP-switch pos. 70 (pos. OFF) when mounted.

Board Addresses

The number of the board position is permanently encoded in the printed wiring on the back plane board. These numbers are used for the addressing of signals (messages) between CP and RP. On each board a maximum of 128 individuals (individual devices) can be addressed

The address wires (KA0 - KA3) for board positions exist on the contact units (pins A26, B26, C26 and A28). The cabinet address is determined by the address wires KA4 - KA5. The wires exist on:

- Contact units (pins B28, C28).
- Flat-ribbon connector position 21 (pins B16, A16, B17, and A15).
- Flat-ribbon connector position 22 (pins A16, B17, A15, and B16).

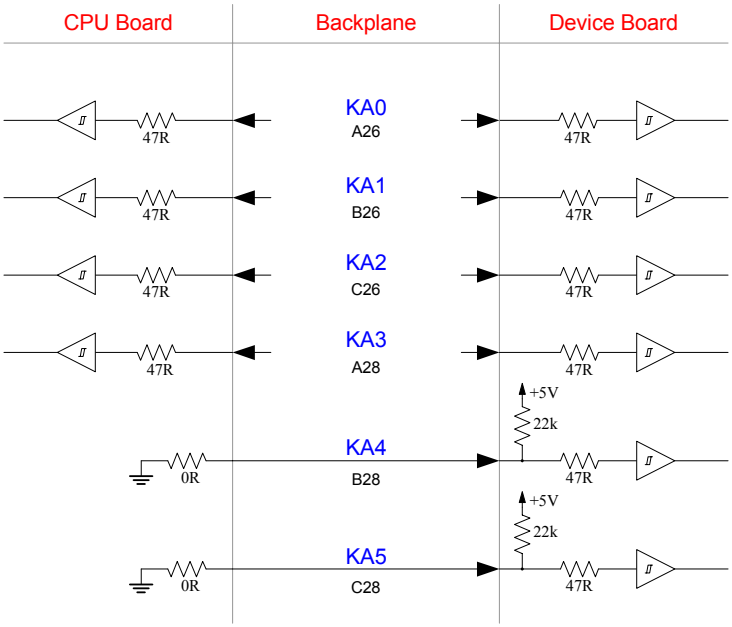


Figure 12: ***Board Address Encoding (KA0 – KA3 different for each position)***

Function Control (FC) Bus

The back plane connection of the device boards is controlled by sending data in serial form (address bit 5 first, FCD 0 last) via the FCD bit and clocking this with a 0→1 change on the FCC bit. After data transmission, the FCE bit is set high (enable) and the selected device board executes the function specified in the issued data. When the FCE bit is high it is also possible to sense the board's status by reading the SENSE-bit.

After reset (watchdog or power up) the FCC- and FCD-signal in the back plane will be low and FCE will be high.

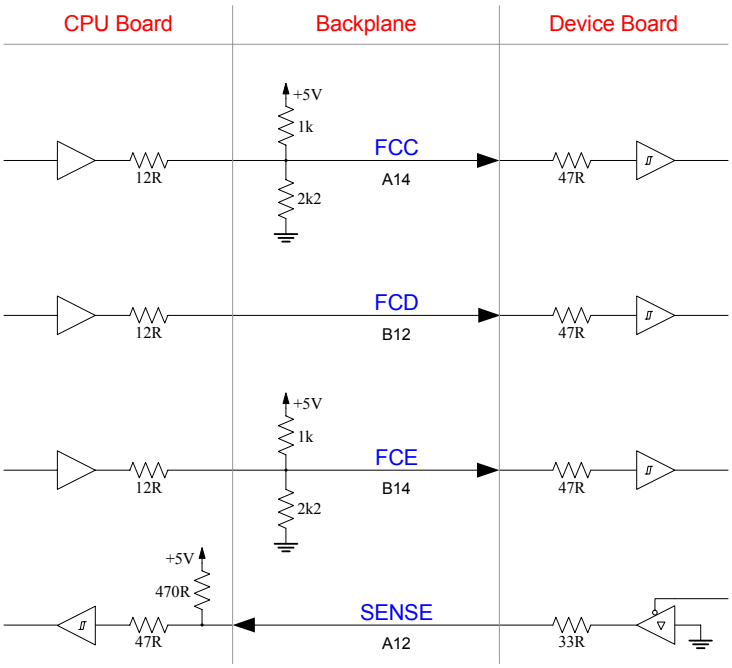


Figure 13: ***FC Bus Circuit Diagram***

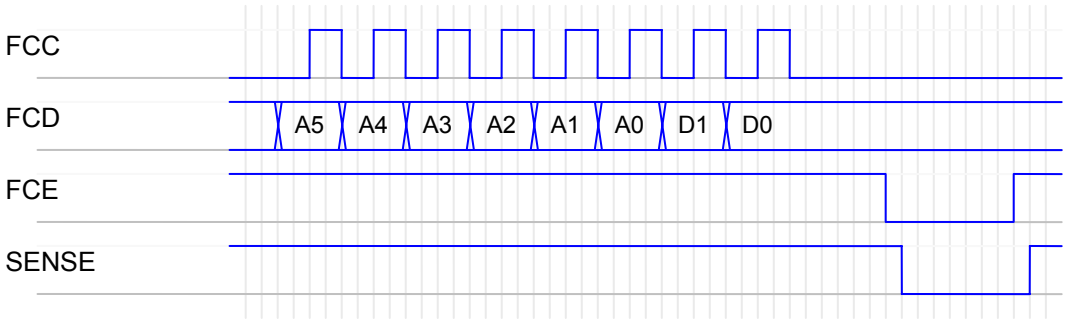


Figure 14: ***FC Bus Signal Diagram***

FC-Bus Commands Table

FCD1	FCD0	SENSE	Device-board status	Function
0	0	1	→ Off	Off and Reset
0	1	0	→ On	On
1	0	1	Off	Check if identified board is On and installed
1	0	0	On	
1	1	0	Off	Check if identified board is installed
1	1	0		

Clock Bus

The system clock is equipped with an oscillator (16,384 MHz) that can be synchronized with a master public telephone exchange via a digital line. The program controls which digital trunk board shall be used as master. Synchronization is continuously monitored and if sync is lost the new sync is extracted from another digital line if available.

Clock bus consists of the following signals:

- MHZ8 or CLK8M: 8,192 MHz clock, which is used to drive device board functions.
- MHZ4 or CLK4M: 4,096 MHz PCM clock.
- SYNC2: Synchronization signal for 2.048 Mbit PCM peripherals on device boards.
- SYNC4: Synchronization signal for 4.096 Mbit PCM peripherals on device boards.
- TSYNC: Synchronization signal recovered from external PSTN signal.

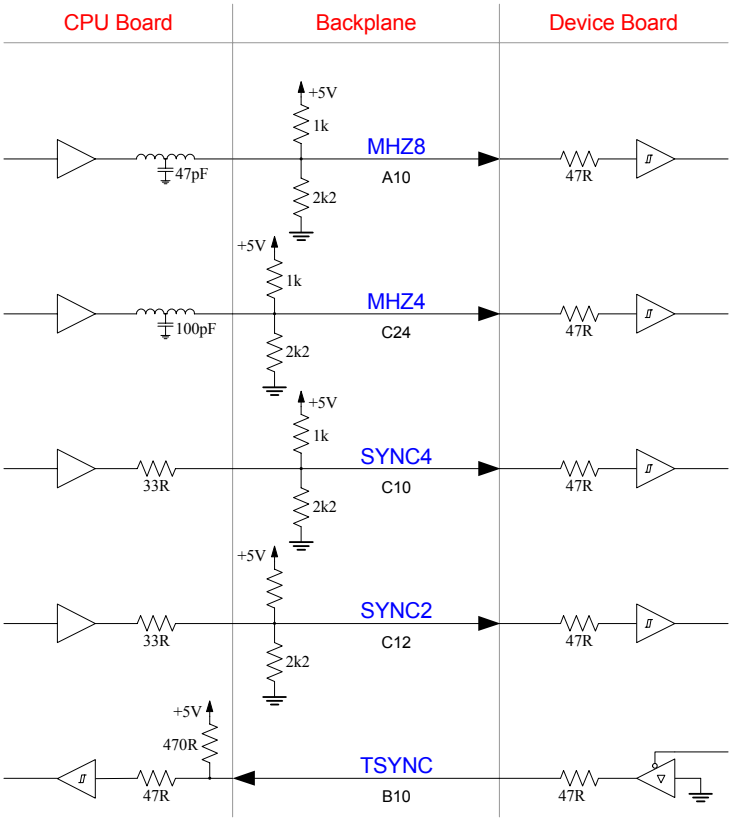


Figure 15: ***Clock Bus Circuit Diagram***

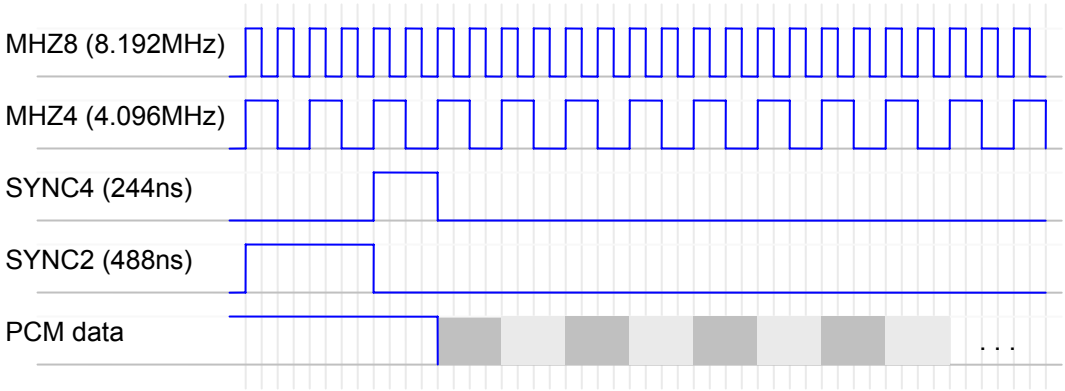


Figure 16: ***Clock Bus Signal Diagram***

PCM Bus

Voice connection between two devices (telephones) is established with the help of a central switch and local switches on the device boards. These switches are connected via two both-way PCM-busses.

Each PCM-bus has 64 time slots (4.096 Mbit/s). These 128 possibilities of interconnecting different devices are administered as a central resource and are “lent” to those devices that are to be interconnected just then. The device boards will be ordered by CPU-D_ to connect an individual device if required, where after CP interconnects two or more devices in the central switch.

The Integrated Cordless has a separate PCM-bus system with 60 time slots linking the control unit and the line unit boards.

Some of the device boards have a local switch for rate adaptation to the PCM bus in the back plane. On all analogue device boards transmission levels to/from the connected devices can be adapted by program-controlled functions.

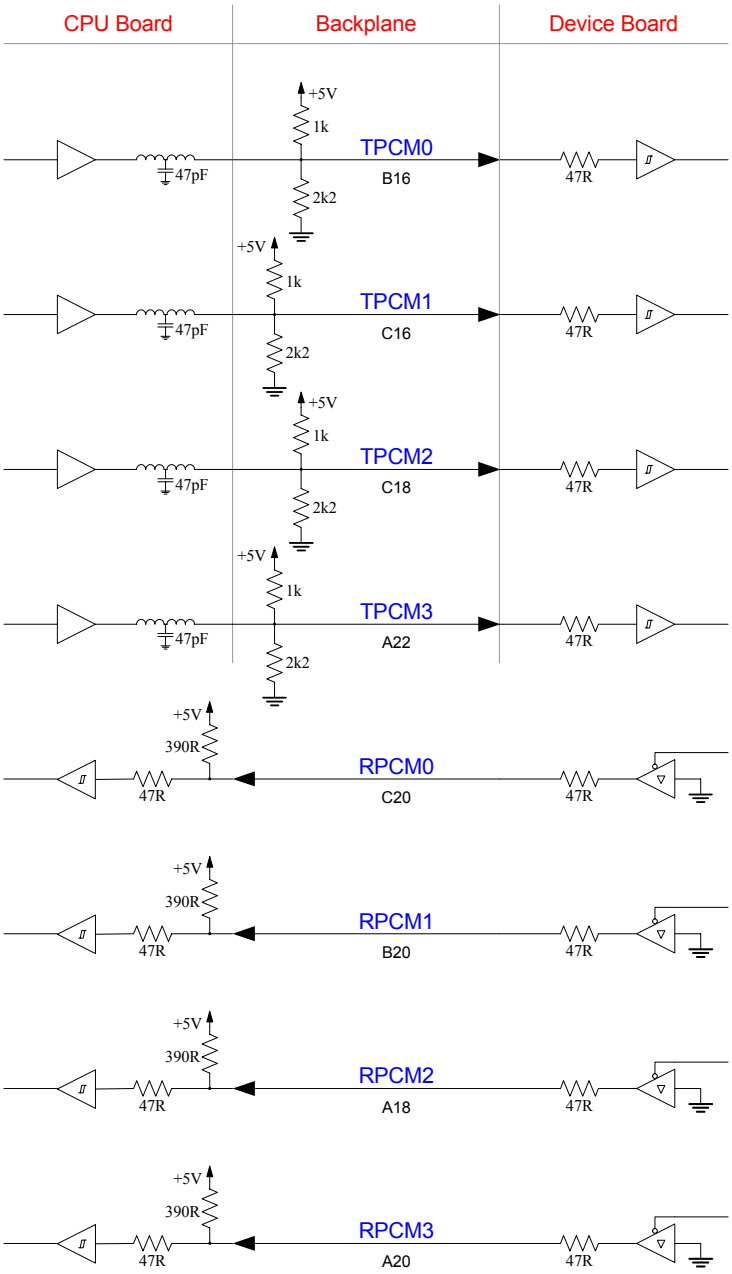


Figure 17: ***PCM Bus Circuit Diagram***

System Communication (SC) Bus

RP communicates with the device boards via the serial communication controllers and two alternative channels:

- **High Speed System Communication (HSSC) Channel**

  1 Mbit/s HDLC single-wire channel with collision detection and two priority levels.
  Spontaneous transfer of data from the device boards is possible.
  The message rate from peripheral boards is programmable via protocol messages. See **1056-ASB 150 02**.

- **System Communication (SC) Channel**

  Standard (old) system communication channel.
  A 64 Kbit/s transmission rate is employed.
  There is no spontaneous transfer of data from the device boards; all communication is initiated by RP.

HSSC-Channel

For fast data communication between the boards, a HSSC channel is used. It works on a single synchronous bi-directional wire at a transmission rate of 1 Mbit/s.[3]

The communication is realized using 5 pins (based on Motorola SCC). The signal HSSCRXD is received directly from the input buffer of RPI. The data can be sent on HSSCTXD only if the output signal HSSCCOLL of the collision detector is low, i.e. there is no other message transmitted on the channel. To avoid a bus conflict when another board is just transmitting, a collision detector is used. It is contained in the FPGA and compares the own transmit signal with the receive signal. If the comparison is successful, no other message is transmitted and the transmission of the own message is continued; if not, a collision information is sent to RP and the transmission is interrupted immediately.

SC-Channel

The transmission rate on SC-Bus is 64 kbit/s. CTX is output for data transmitted to the device boards and CRX is input for data received from the device boards. This is the default communication channel between CPU-D5 and the device boards. EIRQ is the interrupt request signal (active low) to RP.

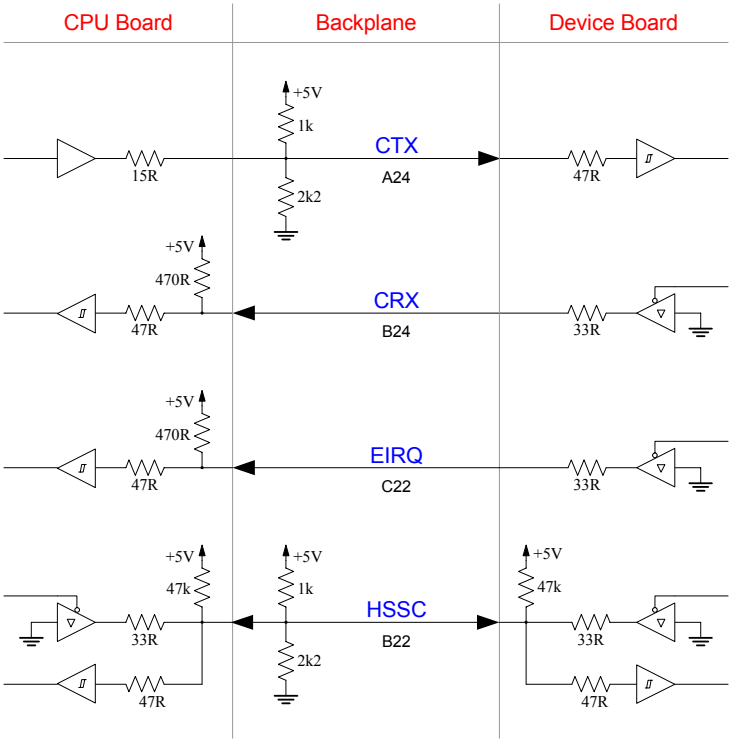


Figure 18: ***SC Bus Circuit Diagram***

[3] It is actually 1.024 Mbit/s, and the HSSC clock is derived from MHZ8

DIN96 Pin-out Table

The pin-out of CPU-D backplane connector adheres to specification **1/1056 ASB 150 02 Uen**, "Back Plane Bus, Appendix". Cordless signals are not used.

Row	a	b	c
1			
2	---	***0V***	***0V***
3		FSYNC	
4	*Test (0V)*	***0V***	***0V***
5			
6	SYP	STROBE	SR
7		ST	
8	***–48V***	***–48V***	***–48V***
9			
10	**MHZ8 (8.096 MHz)**	**TSYNC**	**SYNC4 (244 ns)**
11		VT_A	
12	**SENSE**	**FCD**	**SYNC2 (488 ns)**
13			
14	**FCC**	**FCE**	***–12V***
15		RESET	
16	***+12V***	**TPCM0**	**TPCM1**
17			
18	**RPCM2**	VR_B	**TPCM2**
19		MSYNC	
20	**RPCM3**	**RPCM1**	**RPCM0**
21			
22	**TPCM3**	**HSSC**	**EIRQ**
23		VT_B	
24	**CTX**	**CRX**	**MHZ4 (4.096 MHz)**
25			
26	**KA0**	**KA1**	**KA2**
27		VR_A	
28	**KA3**	**KA4**	**KA5**
29			
30	***0V***	*Test (0V)*	***+5V***
31		INV_4MHZ	
32	***0V***	*Test (0V)*	***+5V***

Notation:

ITALIC	Used for power supply lines
Grey	Used for Cordless-specific signals
Test	Test pins not used in the backplane
---	Unused pins (reserved for future use).
	Grey background: No pin.
	Red background: Longer pins (0V).

DIN96 Pin-out Table (Even Rows Only)

Pin	Backplane	CPU	Device	Signal	Description
a2					Reserved
b2	*0V*	*0V*	*0V*	***GND***	Power Ground
c2	*0V*	*0V*	*0V*	***GND***	Power Ground. Longer pin.
a4	*0V*				Test. Not used.
b4	*0V*	*0V*	*0V*	***GND***	Power Ground
c4	*0V*	*0V*	*0V*	***GND***	Power Ground
a6					Cordless. Not used.
b6					Cordless. Not used.
c6					Cordless. Not used.
a8	*–48V source*	*PS In*	*PS In*	***–48V***	–48V Power Supply
b8	*–48V source*	*PS In*	*PS In*	***–48V***	–48V Power Supply
c8	*–48V source*	*PS In*	*PS In*	***–48V***	–48V Power Supply
a10	Pull-up	Output	Input	**MHZ8**	Clock 8.096 MHz
b10		Input	Output	**TSYNC**	TDM Sync Recover; Def H
c10	Pull-up	Output	Input	**SYNC4**	Clock Sync; 244 ns, 8 kHz
a12		Input	Output	**SENSE**	FC Bus / Sense; Def H
b12		Output	Input	**FCD**	FC Bus / Data; Def L
c12	Pull-up	Output	Input	**SYNC2**	Clock Sync; 488 ns, 8 kHz
a14	Pull-up	Output	Input	**FCC**	FC Bus / Clock; Def L
b14	Pull-up	Output	Input	**FCE**	FC Bus / Enable; Def H
c14	*–12V source*	*PS In*	*PS In*	***–12V***	–12V Power Supply
a16	*+12V source*	*PS In*	*PS In*	***+12V***	+12V Power Supply
b16	Pull-up	I/O	Input	**TPCM0**	PCM TxD, 4.096 Mbit/s
c16	Pull-up	I/O	Input	**TPCM1**	PCM TxD, 4.096 Mbit/s
a18				**RPCM2**	Not used.
b18	Terminated				Cordless. Not used.
c18	Pull-up			**TPCM2**	Not used.
a20				**RPCM3**	Not used.
b20		I/O	Output	**RPCM1**	PCM RxD, 4.096 Mbit/s
c20		I/O	Output	**RPCM0**	PCM RxD, 4.096 Mbit/s
a22	Pull-up			**TPCM3**	Not used.
b22	Pull-up	I/O	I/O	**HSSC**	HSSC Bus / Data, 1 Mbit/s; Def H
c22		Input	Output	**EIRQ**	SC Bus / Event IRQ; Def H
a24	Pull-up	Output	Input	**CTX**	SC Bus / TxD, 64 kbit/s; Def H
b24		Input	Output	**CRX**	SC Bus / RxD, 64 kbit/s; Def H
c24	Pull-up	Output	Input	**MHZ4**	Clock 4.096 MHz
a26	Tied +5V/0V	Input	Input	**KA0**	Card Address / Bit 0
b26	Tied +5V/0V	Input	Input	**KA1**	Card Address / Bit 1
c26	Tied +5V/0V	Input	Input	**KA2**	Card Address / Bit 2
a28	Tied +5V/0V	Input	Input	**KA3**	Card Address / Bit 3
b28		Tied 0V	Input	**KA4**	Card Address / Bit 4
c28		Tied 0V	Input	**KA5**	Card Address / Bit 5
a30	*0V*	*0V*	*0V*	***GND***	Power Ground
b30	*0V*				Test. Not used.
c30	*+5V source*	*PS In*	*PS In*	***+5V***	+5V Power Supply
a32	*0V*	*0V*	*0V*	***GND***	Power Ground. Longer Pin.
b32	*0V*				Test. Not used.
c32	*+5V source*	*PS In*	*PS In*	***+5V***	+5V Power Supply