Digital timing diagram

A **digital timing diagram** is a representation of a set of signals in the time domain. A timing diagram can contain many rows, usually one of them being the clock. It is a tool that is commonly used in digital electronics, hardware debugging, and digital communications. Besides providing an overall description of the timing relationships, the digital timing diagram can help find and diagnose digital logic hazards.
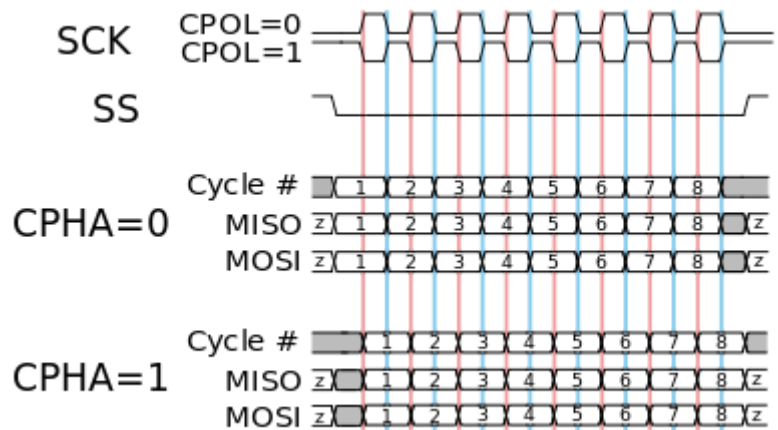
Diagram convention

Most timing diagrams use the following conventions:

- Higher value is a logic one
- Lower value is a logic zero
- A slot showing a high and low is an either or (such as on a data line)
- A Z indicates high impedance
- A greyed out slot is a don't-care or indeterminate.

Example: SPI bus timing

The timing diagram example on the right describes the Serial Peripheral Interface (SPI) Bus. Most SPI master nodes have the ability to set the clock polarity (CPOL) and clock phase (CPHA) with respect to the data. This timing diagram shows the clock for both values of CPOL and the values for the two data lines (MISO & MOSI) for each value of CPHA. Note that when CPHA=1 then the data is delayed by one-half clock cycle.

SPI operates in the following way:

- The master determines an appropriate CPOL & CPHA value
- The master pulls down the slave select (SS) line for a specific slave chip
- The master clocks SCK at a specific frequency
- During each of the 8 clock cycles the transfer is full duplex:
    - The master writes on the MOSI line and reads the MISO line
    - The slave writes on the MISO line and reads the MOSI line
- When finished the master can continue with another byte transfer or pull SS high to end the transfer

A timing diagram for the Serial Peripheral Interface Bus

When a slave's SS line is high then both of its MISO and MOSI line should be high impedance so to avoid disrupting a transfer to a different slave. Prior to SS being pulled low, the MISO & MOSI lines are indicated with a "z" for high impedance. Also, prior to the SS being pulled low the "cycle #" row is meaningless and is shown greyed-out.

Note that for CPHA=1 the MISO & MOSI lines are undefined until after the first clock edge and are also shown greyed-out before that.

A more typical timing diagram has just a single clock and numerous data lines

External links

- Wavedrom [1] is an online timing diagram editor
- Waves [2] has Windows binary