



# VC709 PCIe Design Creation

April 2015

XTP237

# Revision History

Date	Version	Description
04/30/14	12.0	Recompiled for 2015.1.
11/24/14	11.0	Recompiled for 2014.4.
10/08/14	10.0	Recompiled for 2014.3.
06/09/14	9.0	Recompiled for 2014.2.
04/16/14	8.0	Recompiled for 2014.1.
12/18/13	7.0	Recompiled for 2013.4.
10/23/13	6.0	Recompiled for 2013.3. Added AR54939.
06/19/13	5.0	Recompiled for 2013.2
04/03/13	4.0	Recompiled for 2013.1. AR53747 fixed.
01/18/13	3.0	Recompiled for 2012.4. Added AR53747.
10/23/12	2.0	Recompiled for 2012.3.
09/20/12	1.0	Initial version.

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# Overview

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  - Compile Example Design
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# Virtex-7 PCIe x8 Gen3 Capability

## ➤ VC709 Supports PCIe Gen3 Capability

- x8, x4, x2, or x1 Gen3 lane width

## ➤ LogiCORE PIO Example Design

- VC709 PCIe Design Files (2015.1 C) ZIP file
- Available through <http://www.xilinx.com/vc709>

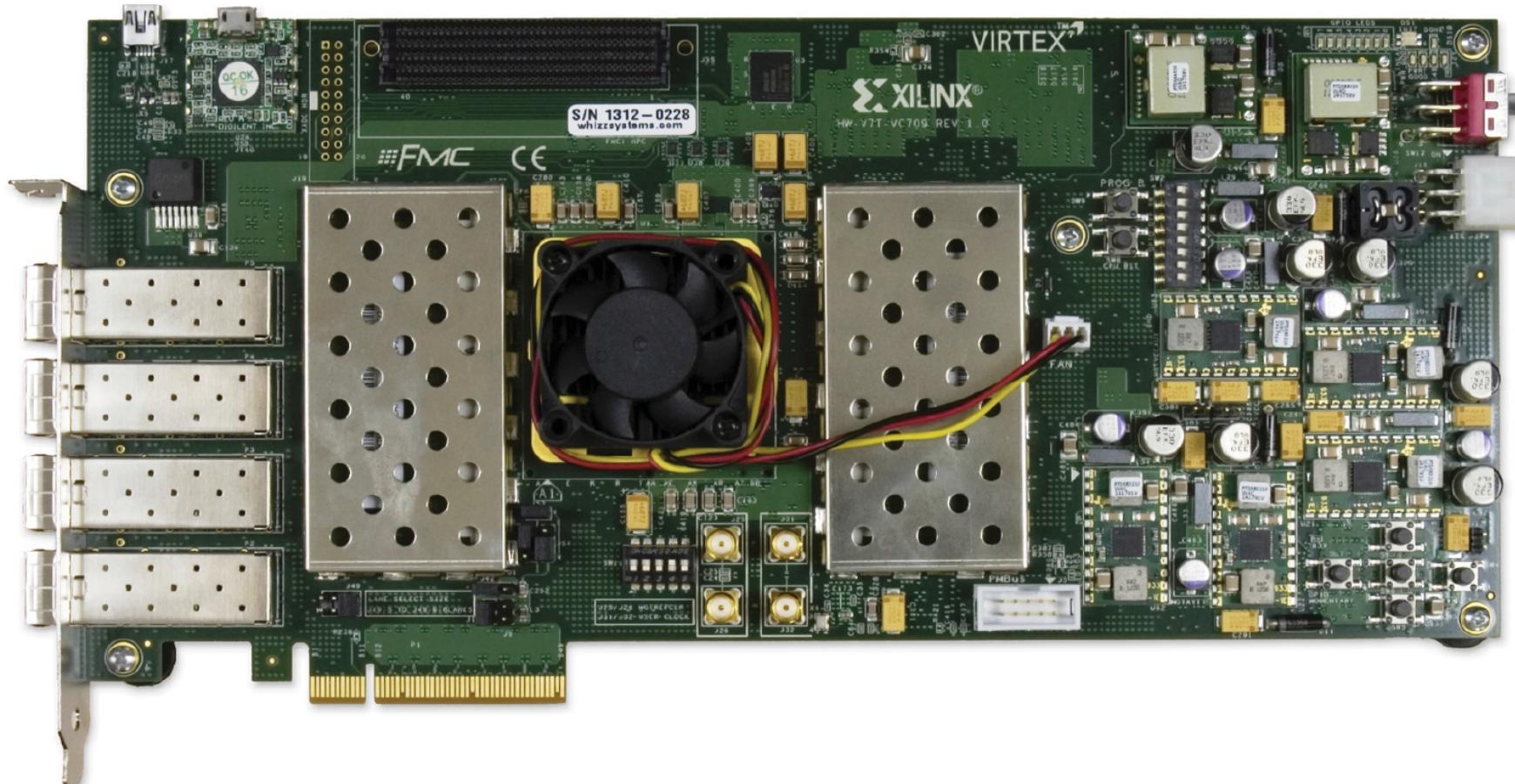
## ➤ Virtex-7 FPGA Gen3 Integrated Block for PCI Express

- See [PG023](#) for details

# Virtex-7 PCIe x8 Gen3 Capability

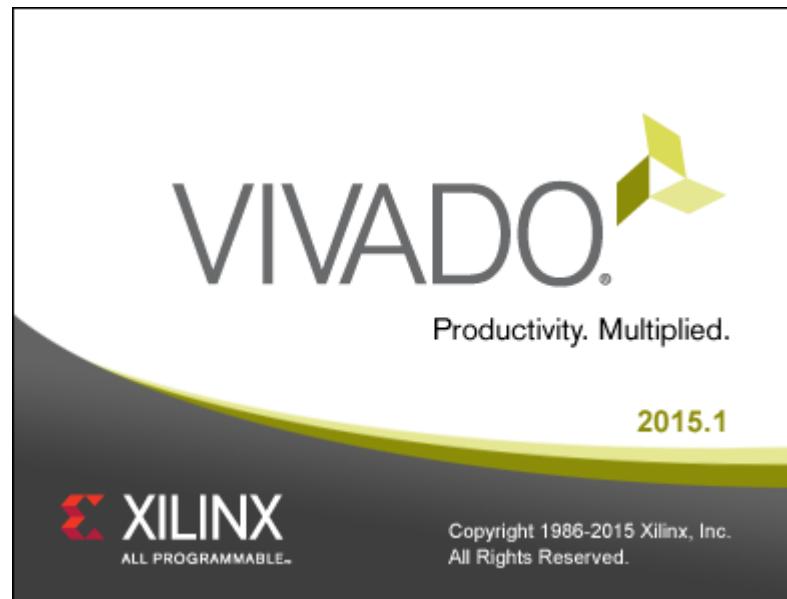
- **Integrated Block for PCI Express**
  - PCI Express Base 2.0 Specification
- **Configurable for Endpoint or Root Port Applications**
  - VC709 configured for Endpoint Applications
- **GTH Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
  - 128 / 256 / 512 / 1024 bytes
- **Configurable BAR spaces**
  - Up to 6 x 32 bit, 3 x 64 bit, or a combination
  - Memory or IO
  - BAR and ID filtering
- **Management and Statistics Interface**

# Xilinx VC709 Board



# Vivado Software Requirements

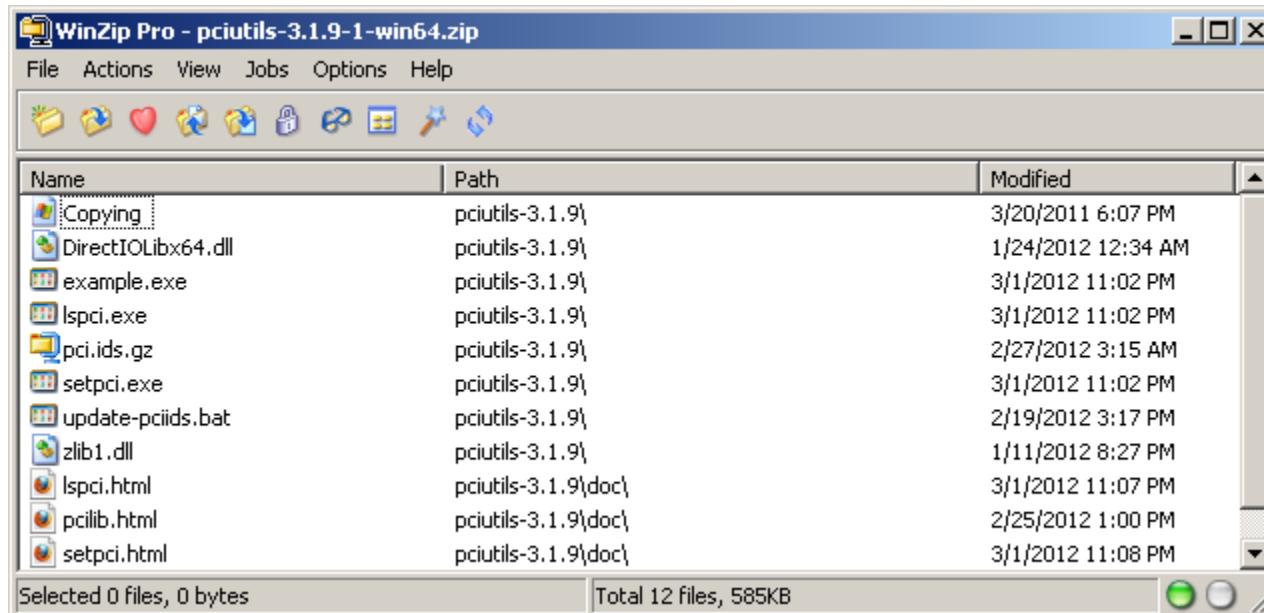
- Xilinx Vivado Design Suite 2015.1, Design Edition



# Ispci Software Requirement

## ► Ispci for Windows

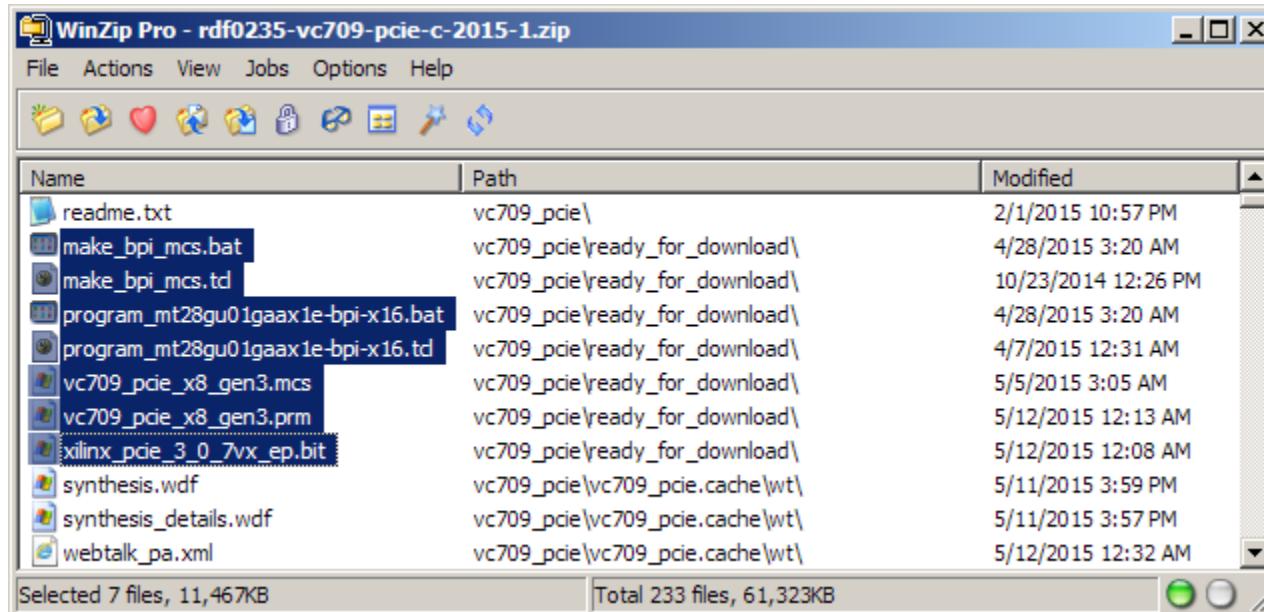
- Free [download](#)
- Unzip to the C:\ drive of the test PC



# Setup for the VC709 PCIe Design

► Open the VC709 PCIe Design Files (2015.1 C) ZIP file, and extract these files to your C:\ drive:

- vc709\_PCIE\ready\_for\_download\\*
- Available through <http://www.xilinx.com/vc709>



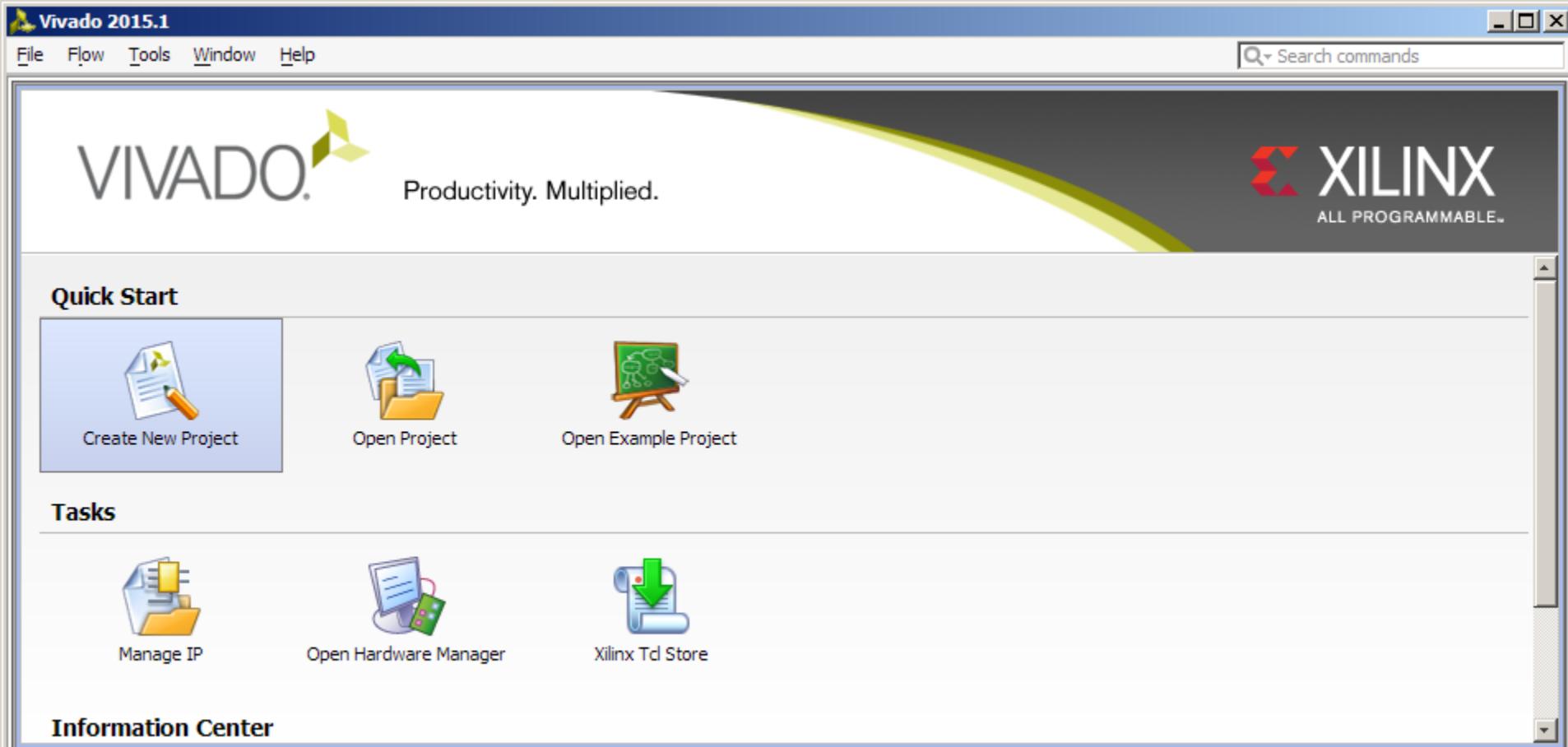
# **Generate x8 Gen 3 PCIe Core**

# Generate x8 Gen 3 PCIe Core

## ► Open Vivado

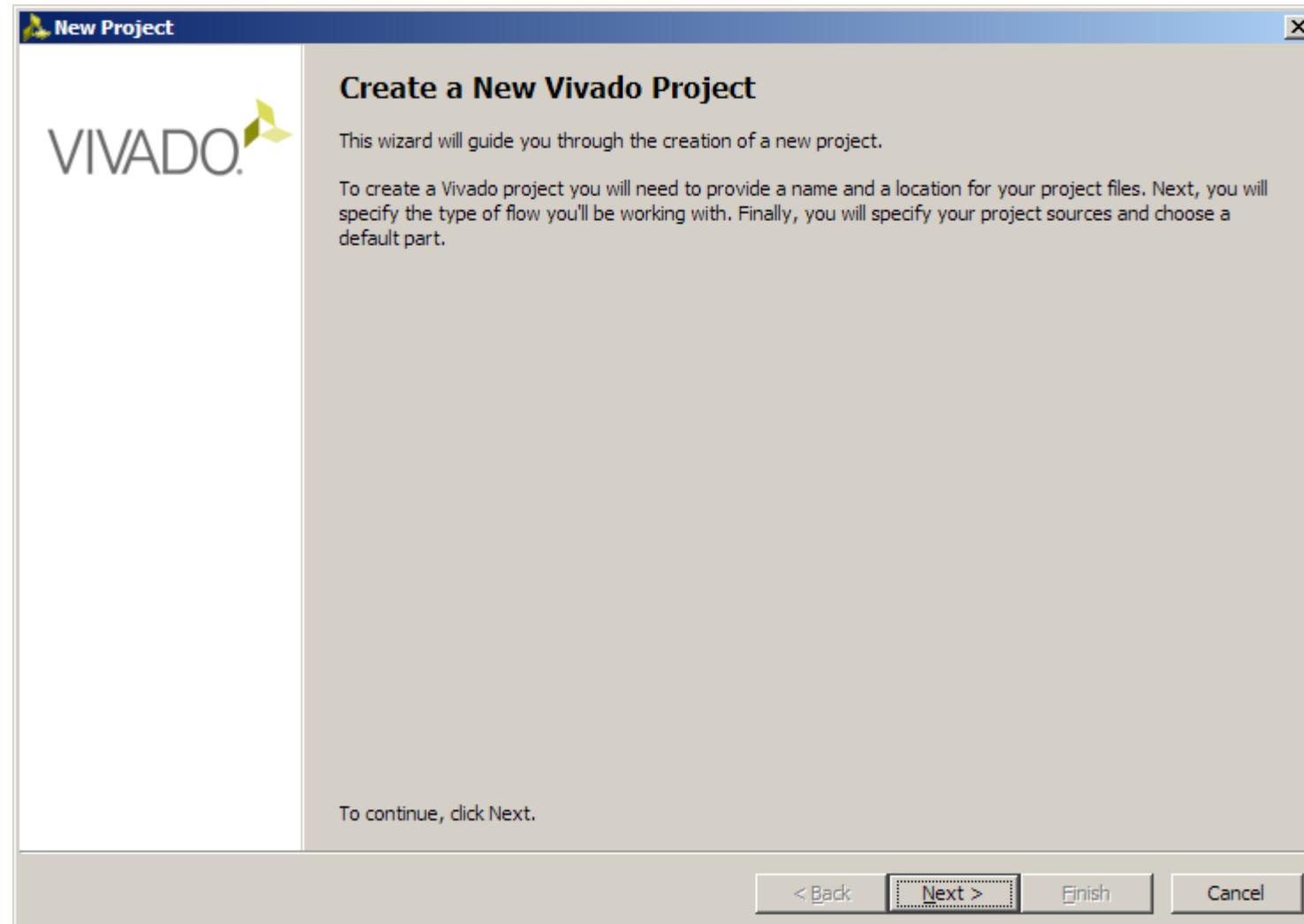
Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

## ► Select Create New Project



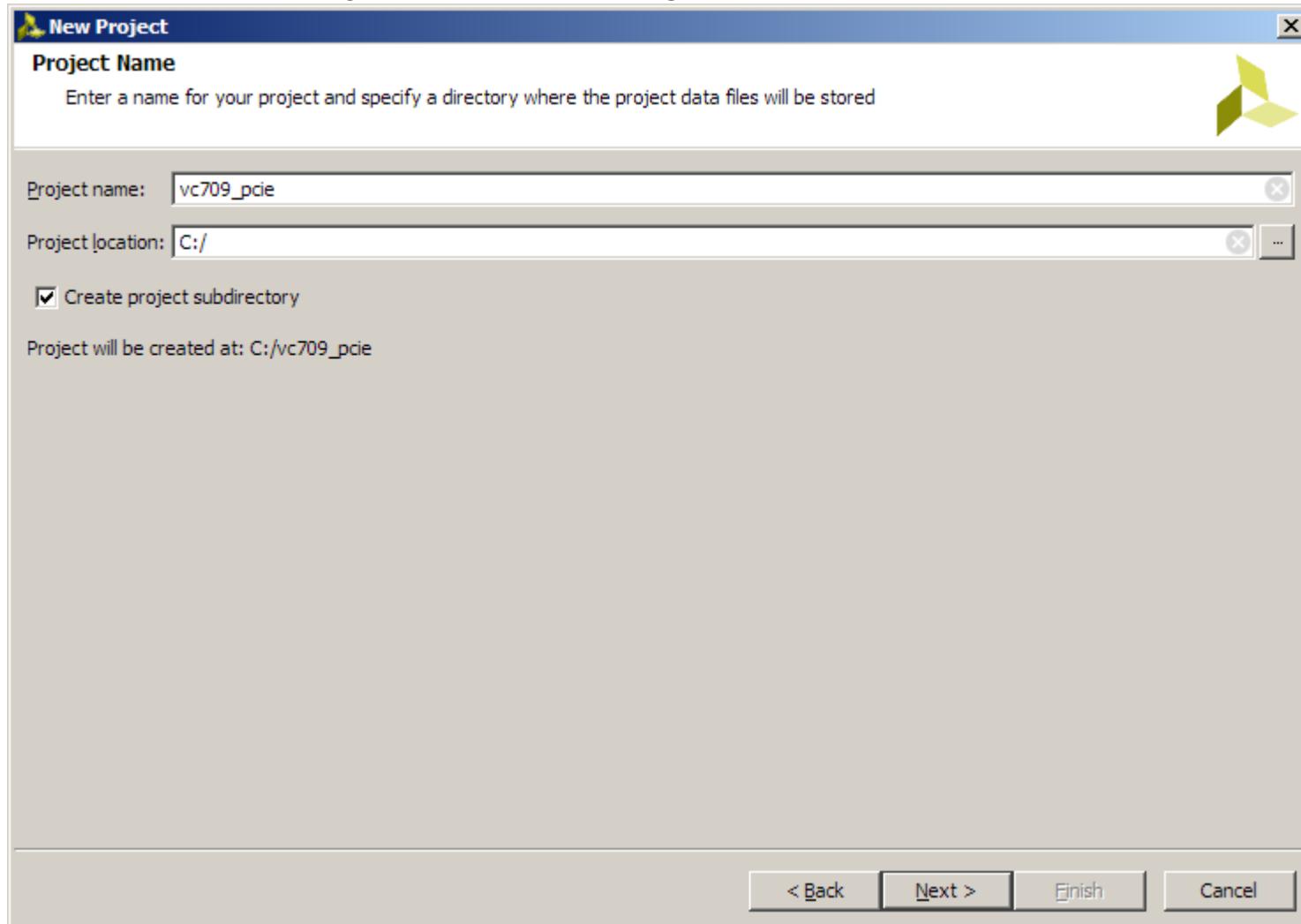
# Generate x8 Gen 3 PCIe Core

► Click Next



# Generate x8 Gen 3 PCIe Core

- Set the Project name and location to vc709\_pcnie and C:\
  - Check Create project subdirectory



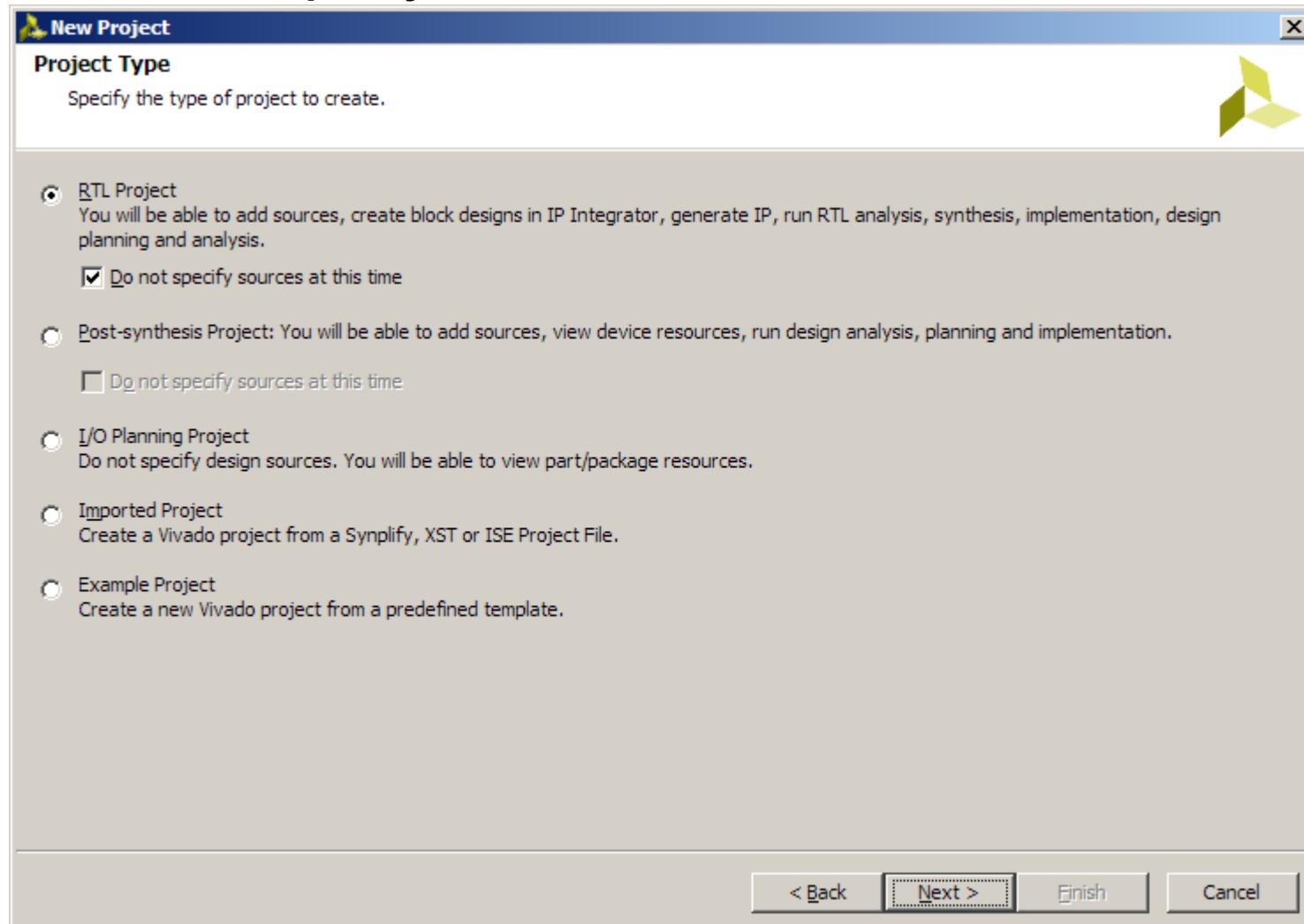
Note: Vivado generally requires forward slashes in paths

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# Generate x8 Gen 3 PCIe Core

## ► Select RTL Project

- Select **Do not specify sources at this time**



# Generate x8 Gen 3 PCIe Core

## ► Select the VC709 board

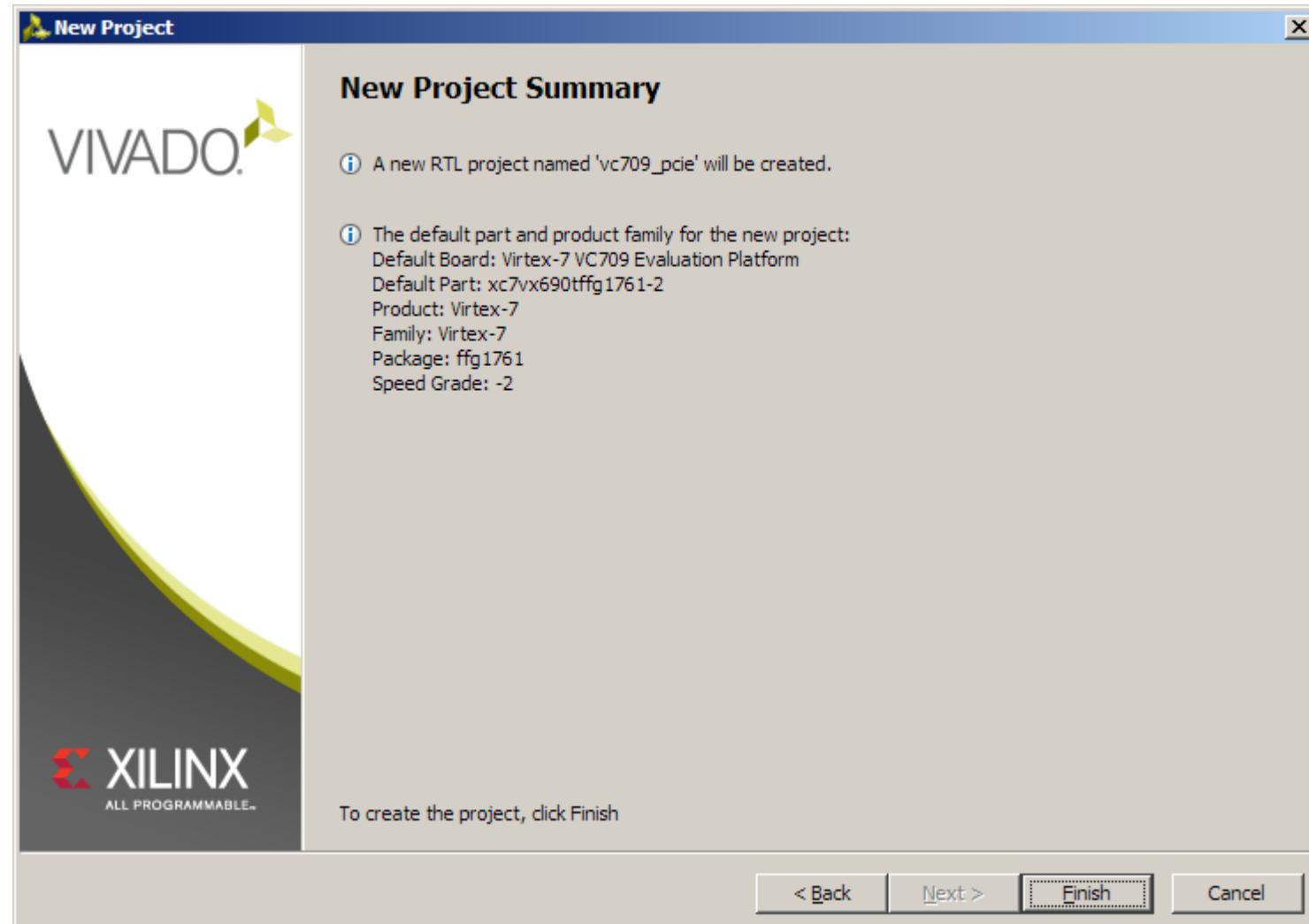
The screenshot shows the 'New Project' dialog with the title 'Default Part'. The instruction 'Choose a default Xilinx part or board for your project. This can be changed later.' is displayed. There are tabs for 'Parts' (selected) and 'Boards'. A 'Filter' section includes dropdowns for 'Vendor' (All), 'Display Name' (All), and 'Board Rev' (Latest), along with a 'Reset All Filters' button. A search bar with a magnifying glass icon is also present. The main area is a table listing various Xilinx boards:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tffg676-2	676	1.2	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcku040-ffa1156-2-e	1,156	1.0	520
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.2	700
<b>Virtex-7 VC709 Evaluation Platform</b>	<b>xilinx.com</b>	<b>1.0</b>	<b>xc7vx690tffg1761-2</b>	<b>1,761</b>	<b>1.6</b>	<b>850</b>
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045tffg900-2	900	1.2	362

At the bottom are navigation buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

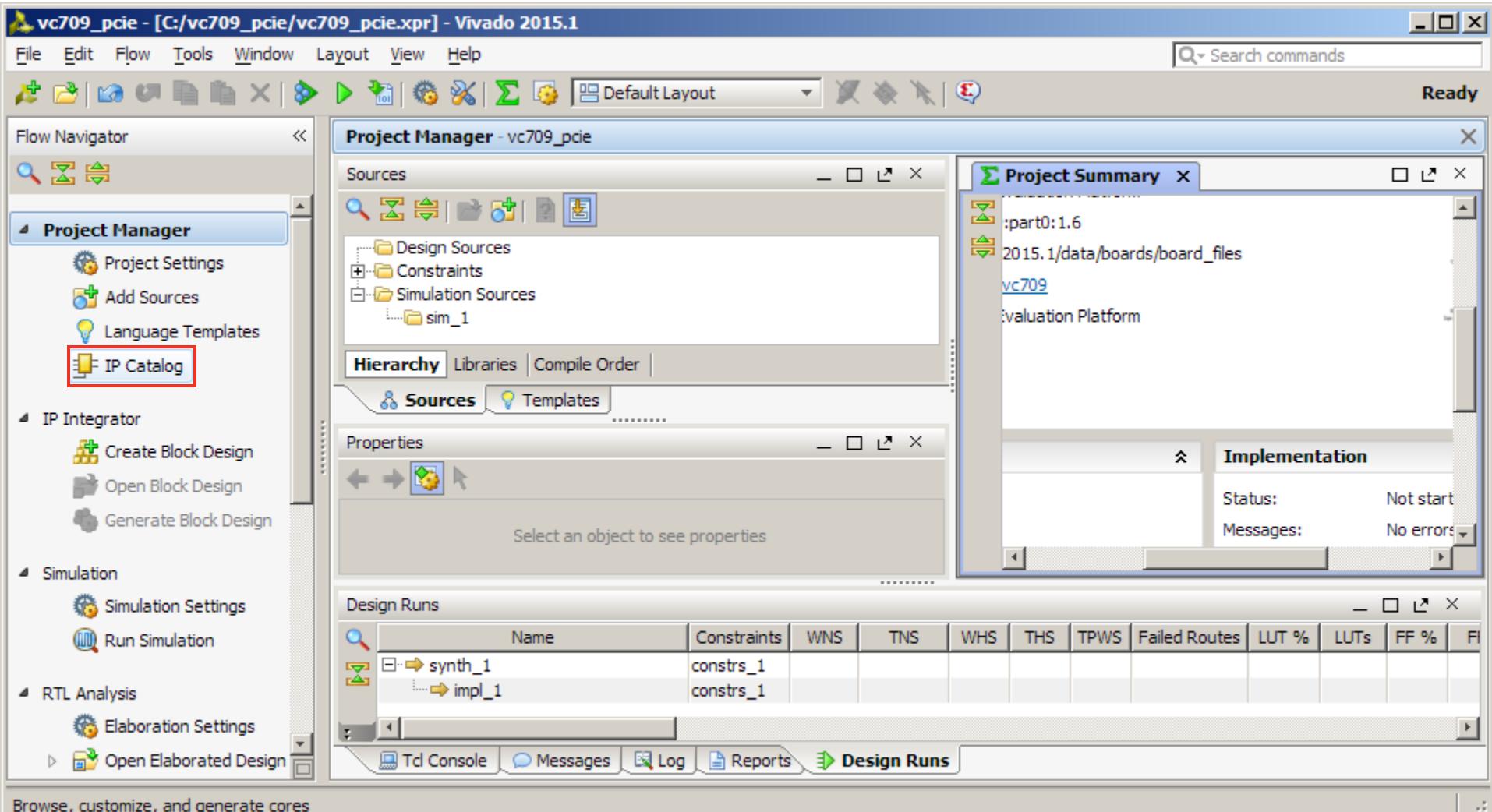
# Generate x8 Gen 3 PCIe Core

► Click Finish



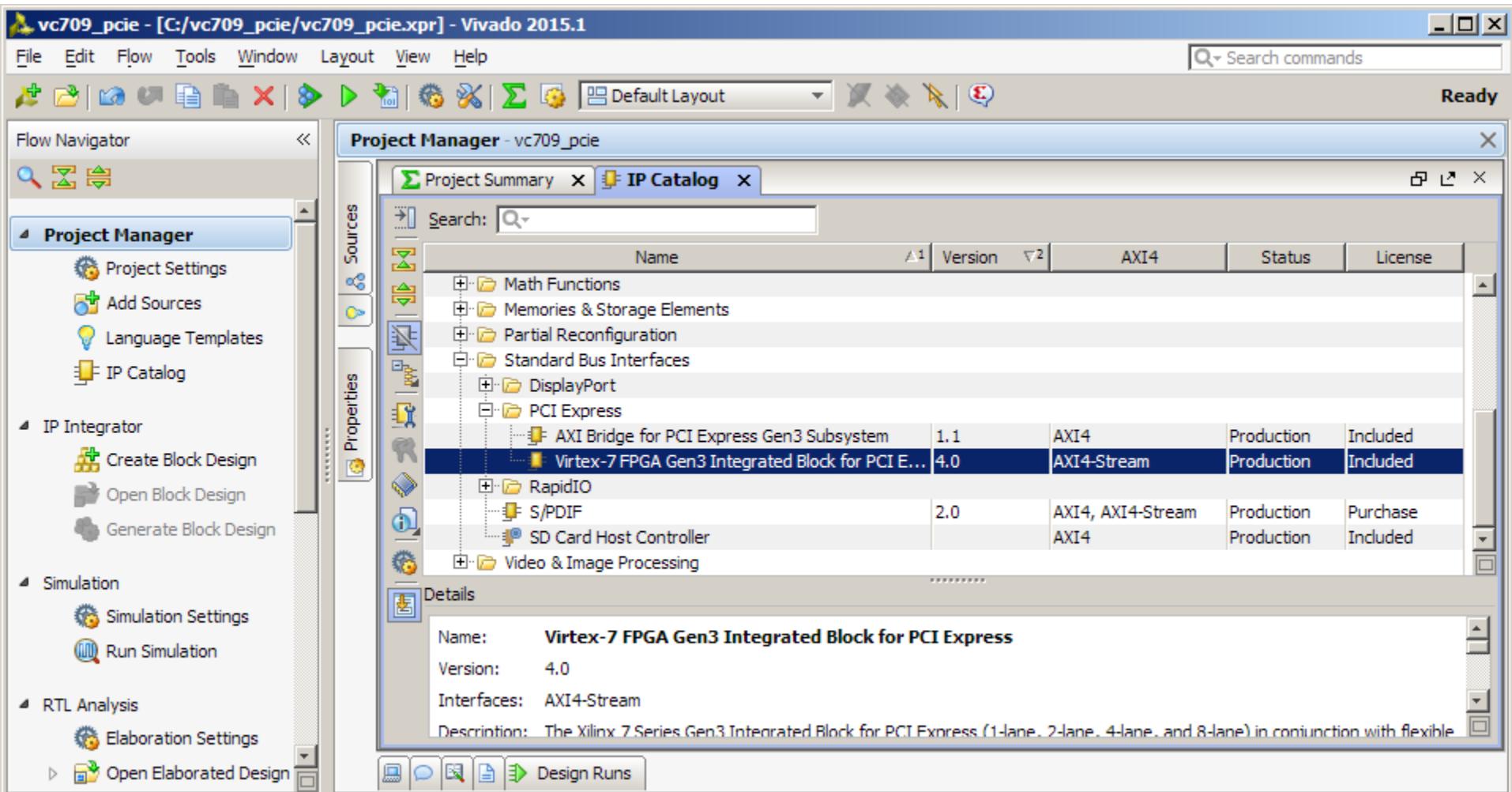
# Generate x8 Gen 3 PCIe Core

► Click on IP Catalog



# Generate x8 Gen 3 PCIe Core

- ▶ Select Virtex-7 FPGA Gen3 Integrated Block for PCI Express, v4.0 under Standard Bus Interfaces



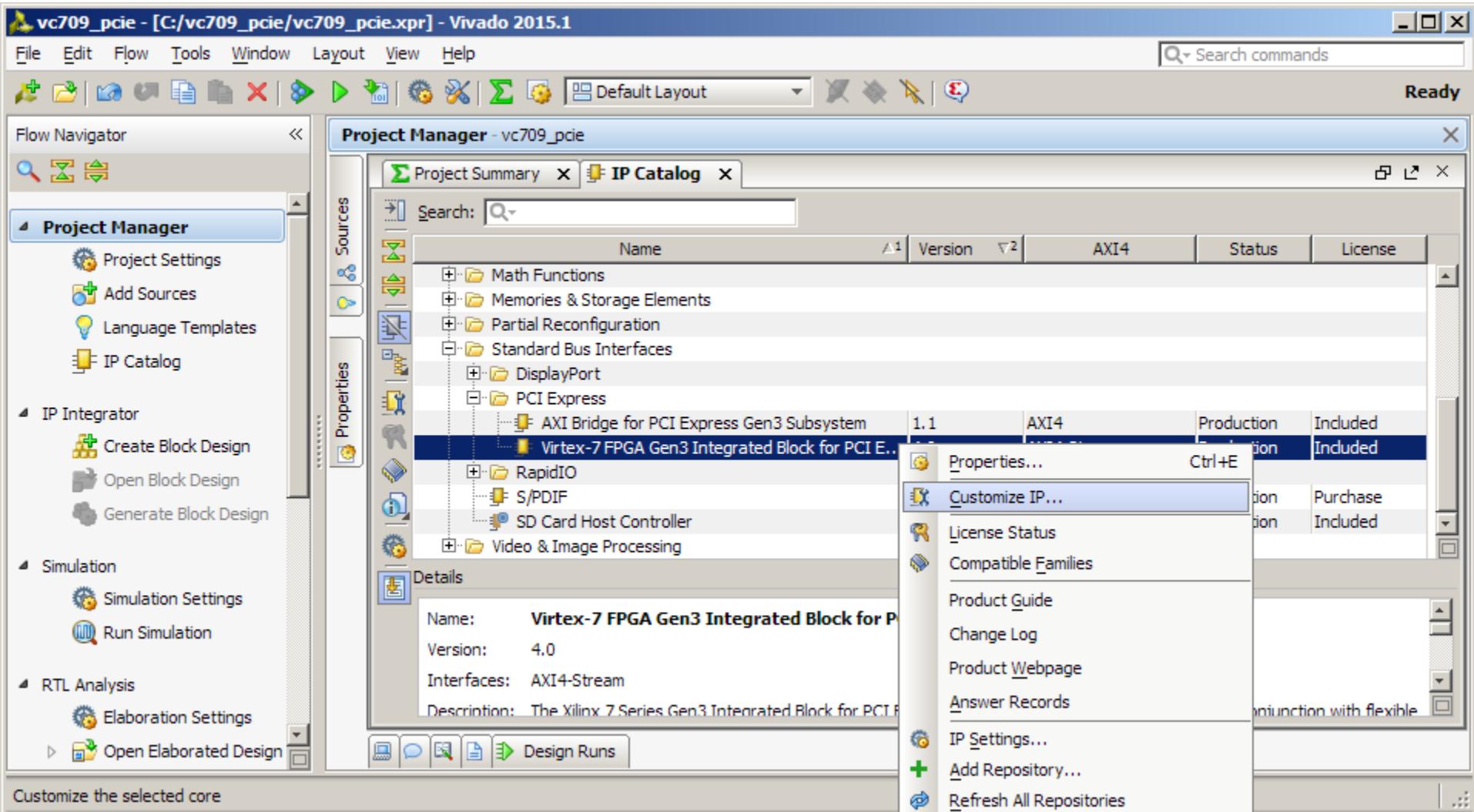
IP: Virtex-7 FPGA Gen3 Integrated Block for PCI Express

Note: Presentation applies to the VC709

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# Generate x8 Gen 3 PCIe Core

- Right click on Virtex-7 FPGA Gen3 Integrated Block for PCI Express
  - Select Customize IP



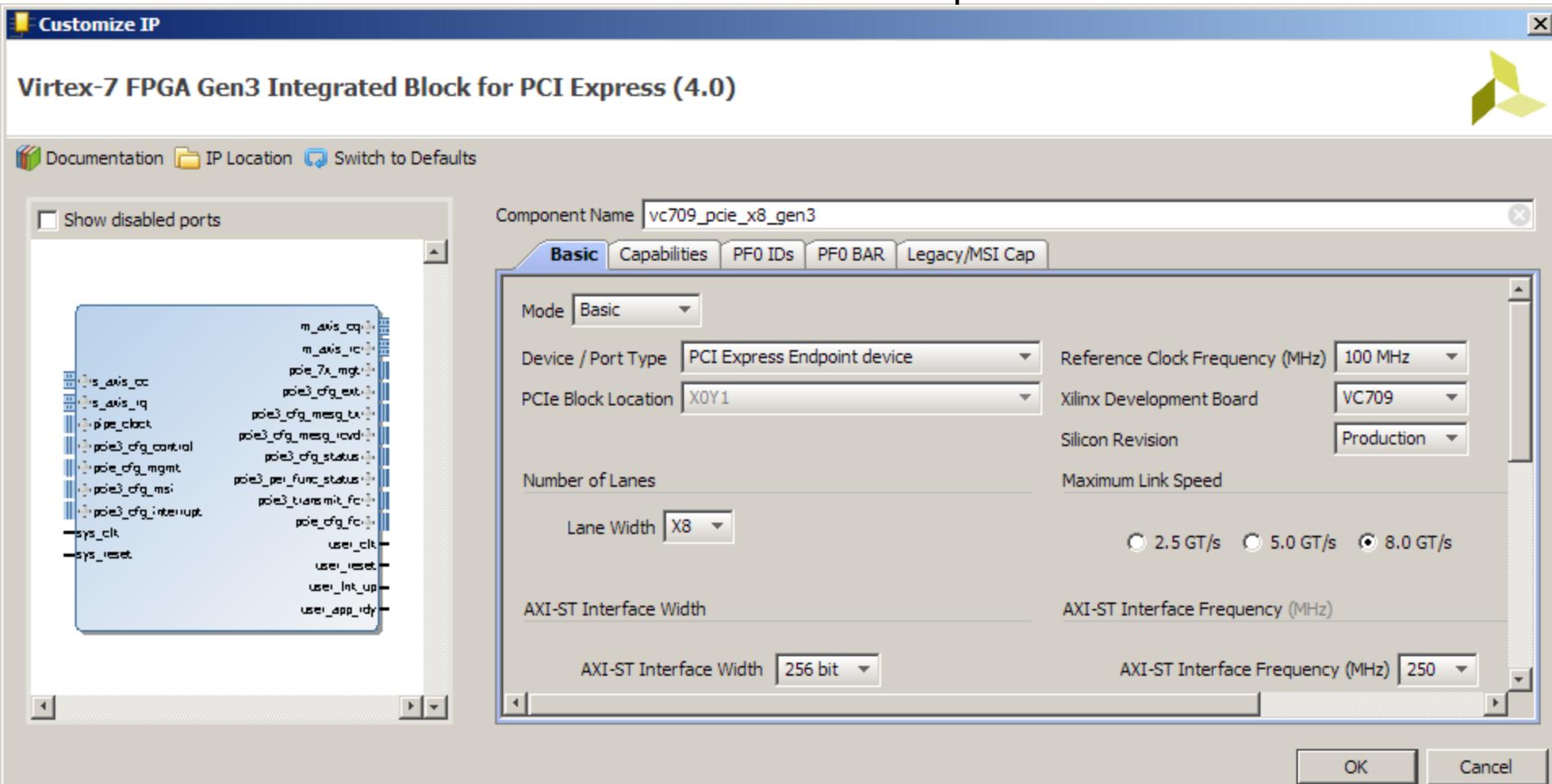
Note: Presentation applies to the VC709

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# Generate x8 Gen 3 PCIe Core

► Under the Basic tab,

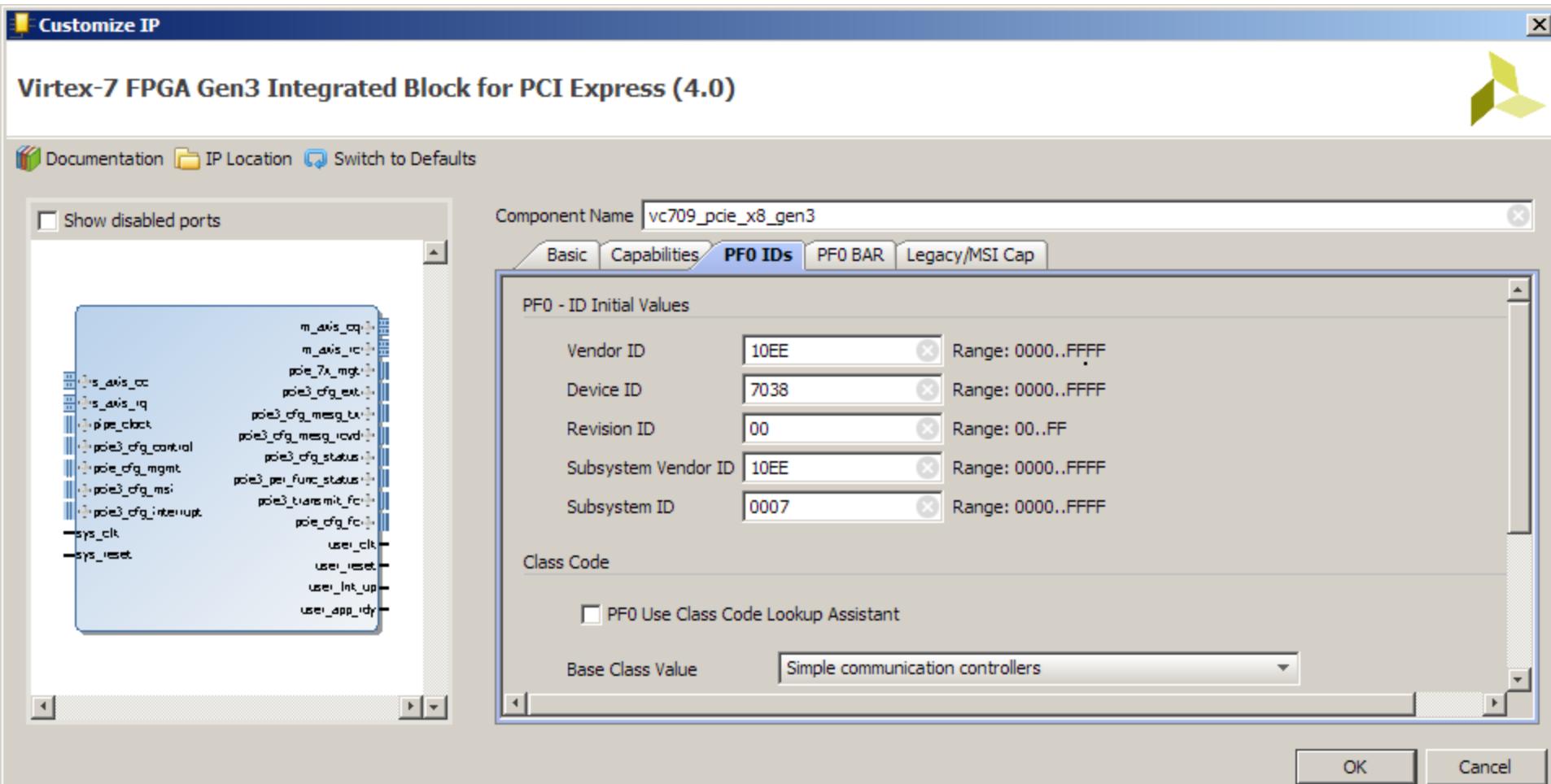
- Set Component name to **vc709\_pcie\_x8\_gen3**
- Set Development Board to **VC709**
- Set Lane Width to **X8** and set the Max Link Speed to **8 GT/s**



# Generate x8 Gen 3 PCIe Core

## ► Under the PF0 IDs tab, note the ID Initial Values

- Vendor ID = **10EE**; Device ID = **7038**; Revision ID = **00**
- Subsystem Vendor ID = **10EE**; Subsystem ID = **0007**

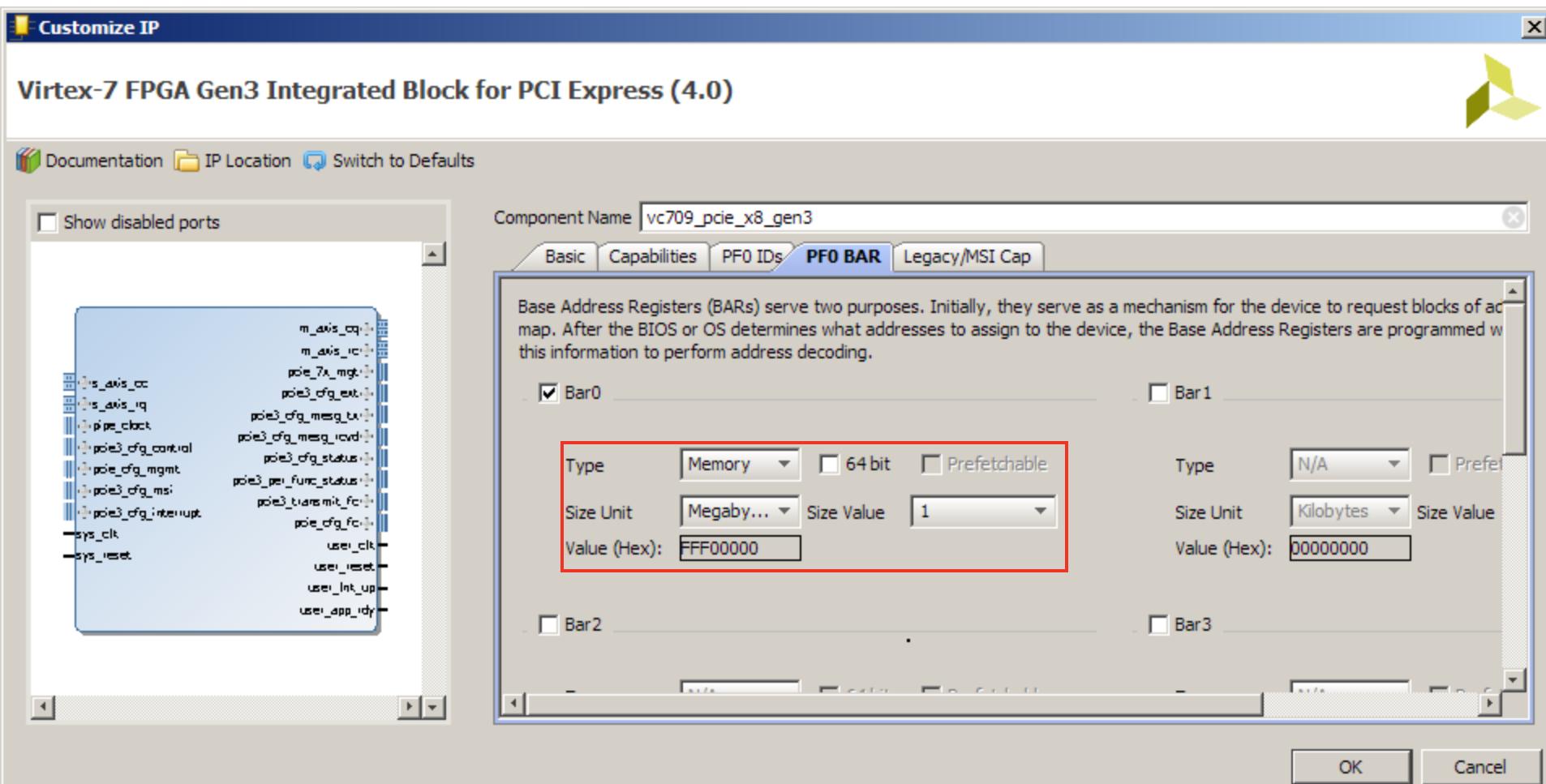


# Generate x8 Gen 3 PCIe Core

► Under the PF0 BAR tab, set BAR 0

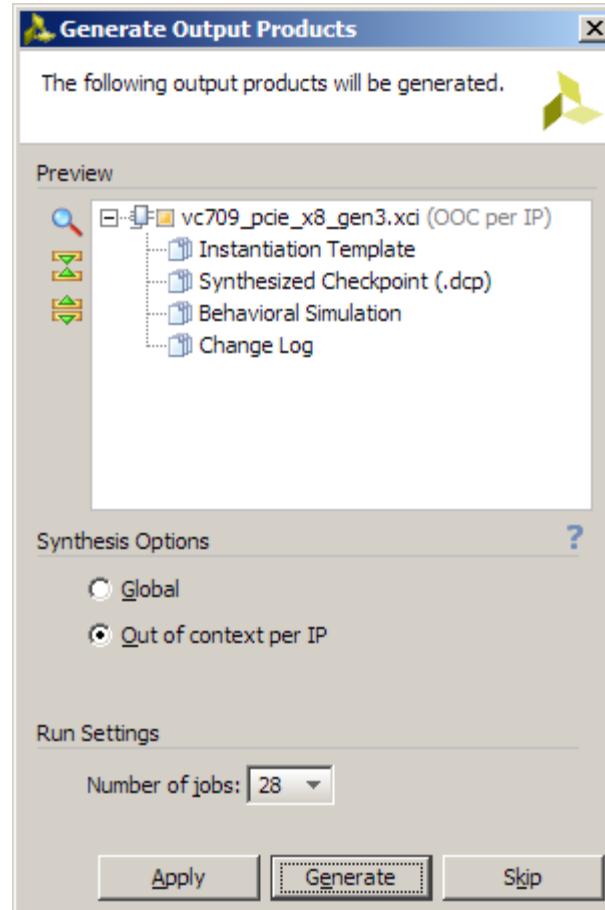
- Set to 1 Megabytes

► Click OK



# Generate x8 Gen 3 PCIe Core

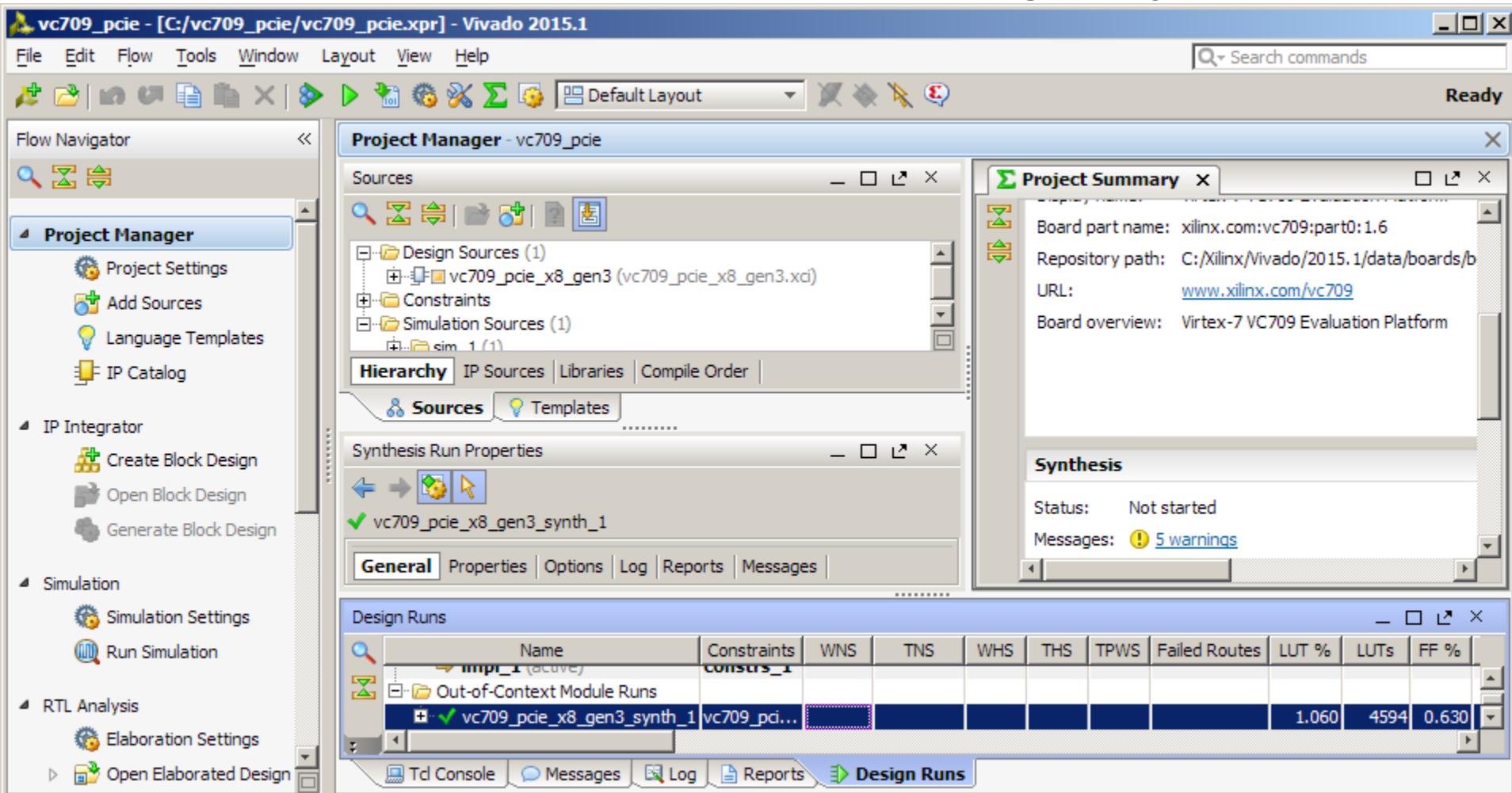
► Click Generate



# Generate x8 Gen 3 PCIe Core

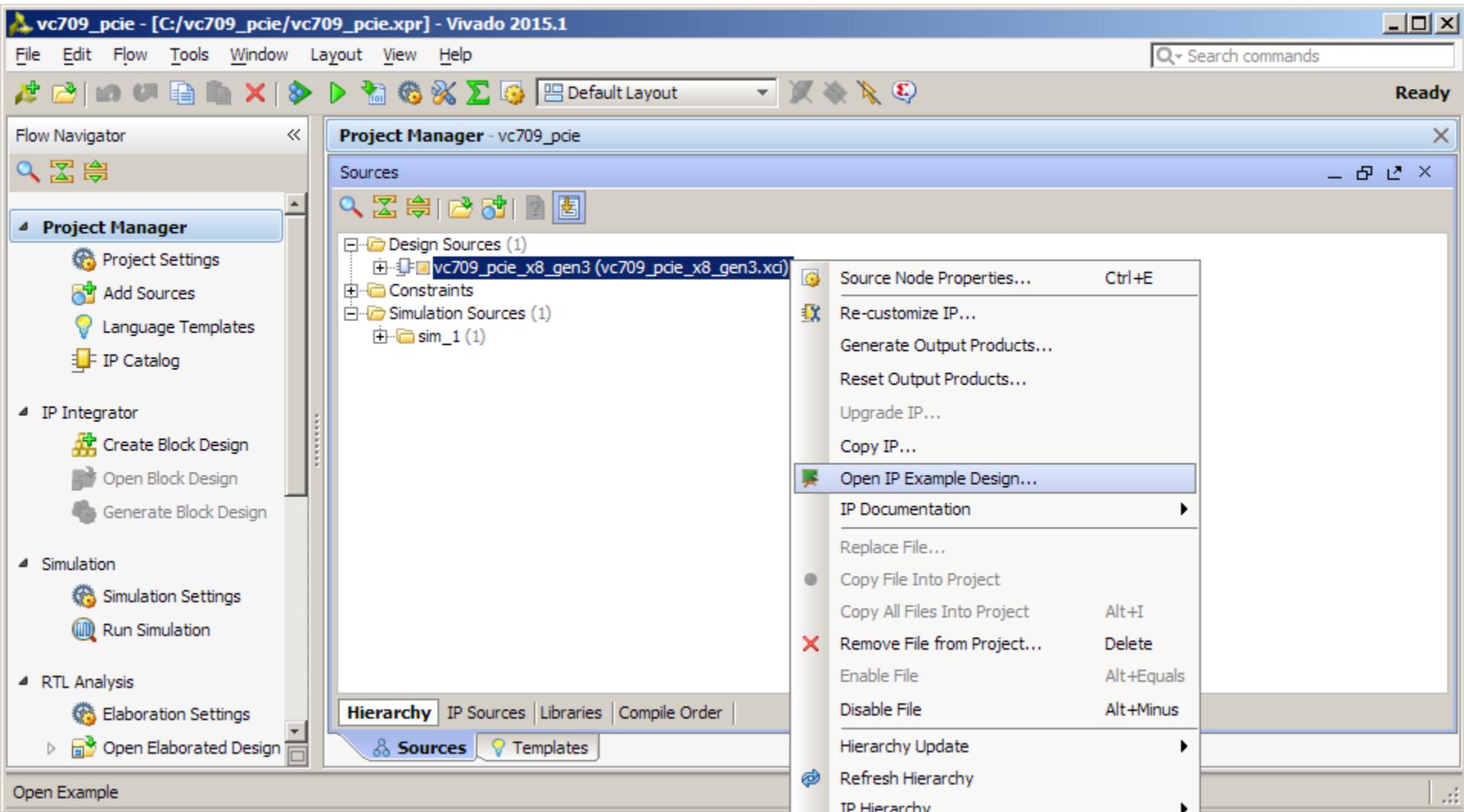
## ► PCIe design appears in Design Sources

- Wait until checkmark appears on vc709\_pcie\_x8\_gen3\_synth\_1



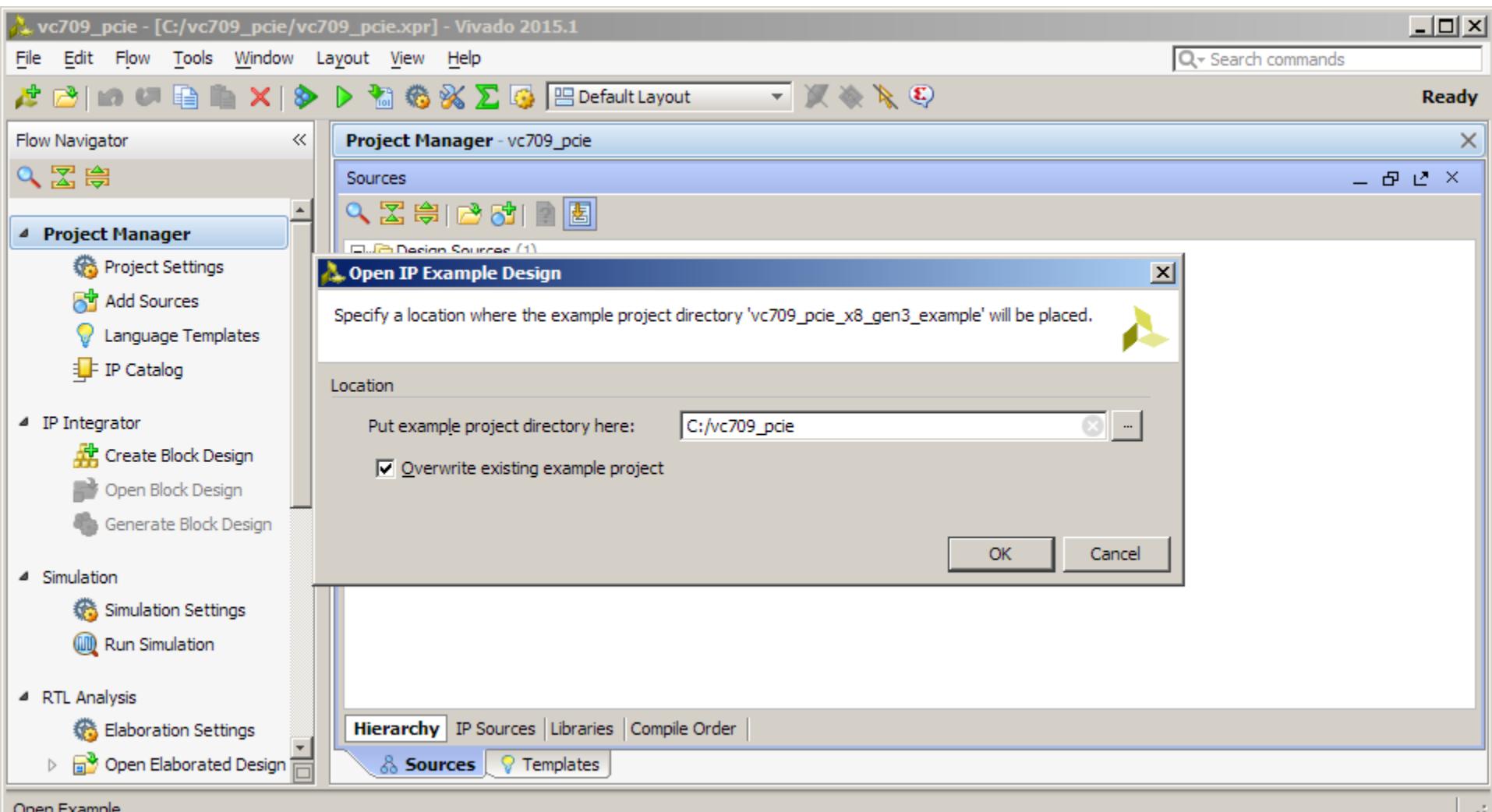
# Generate x8 Gen 3 PCIe Core

- Right-click on vc709\_pcie\_x8\_gen3 and select Open IP Example Design...



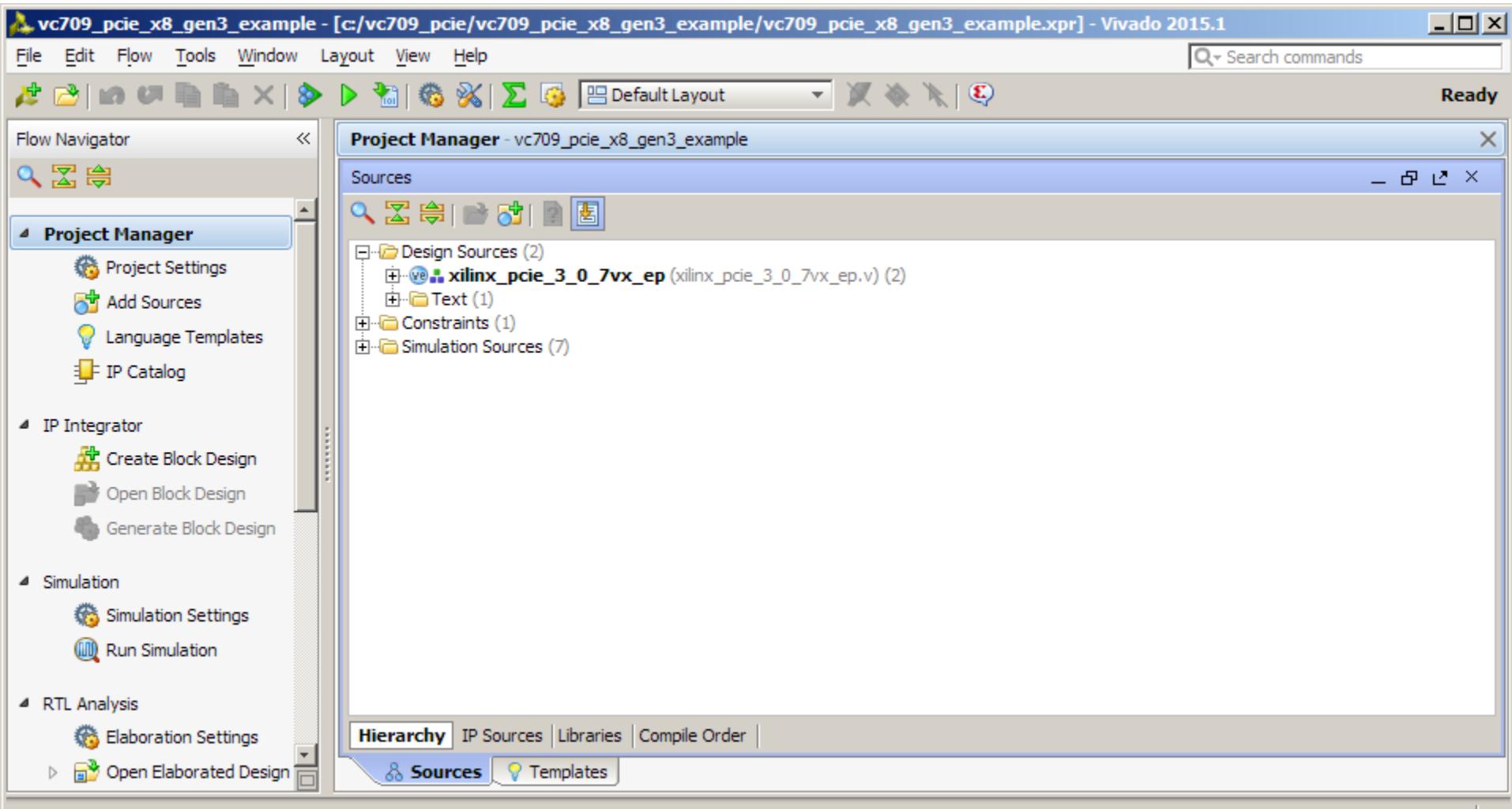
# Generate x8 Gen 3 PCIe Core

► Set the location to C:/vc709\_pcnie and click OK



# Generate x8 Gen 3 PCIe Core

- A new project is created



Note: The original project window can be closed

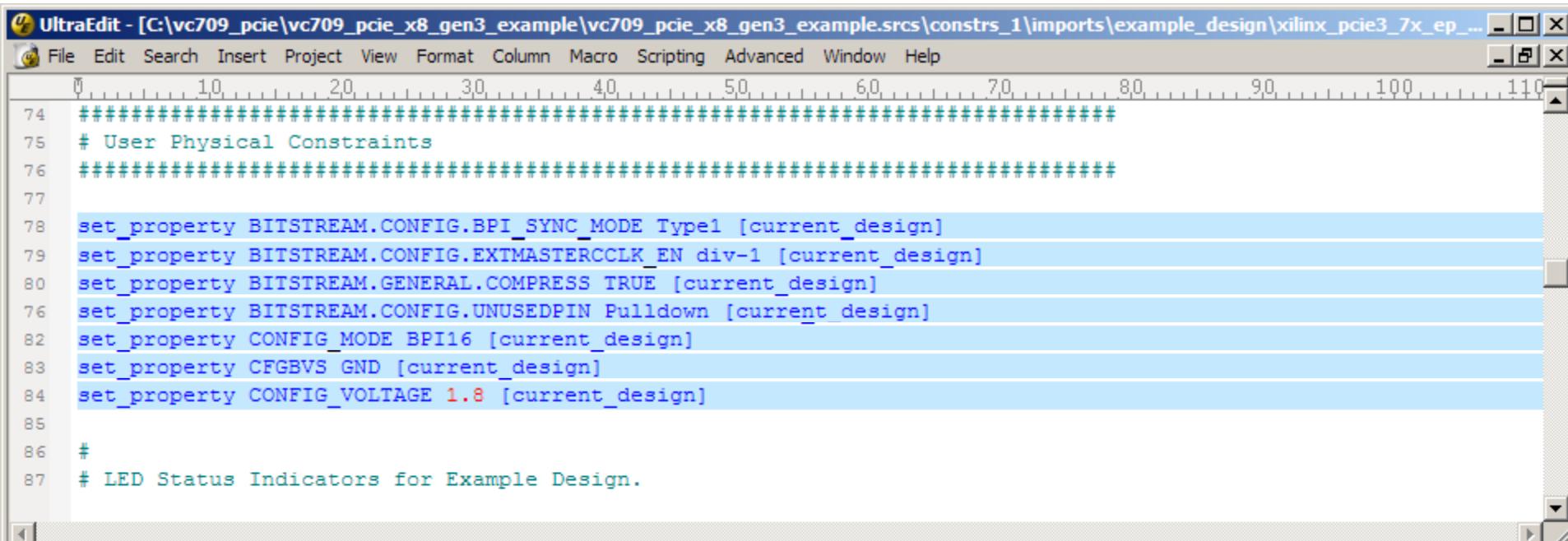
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# Modify PCIe Core

► As per [UG470](#), [UG899](#), [UG908](#), and [G18 Flash](#) specifications

- In the XDC file, `xilinx_pcie3_7x_ep_x8g3_VC709.xdc`, add these lines:

```
set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pulldown [current_design]
set_property CONFIG_MODE BPI16 [current_design]
set_property CFGBVS GND [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
```



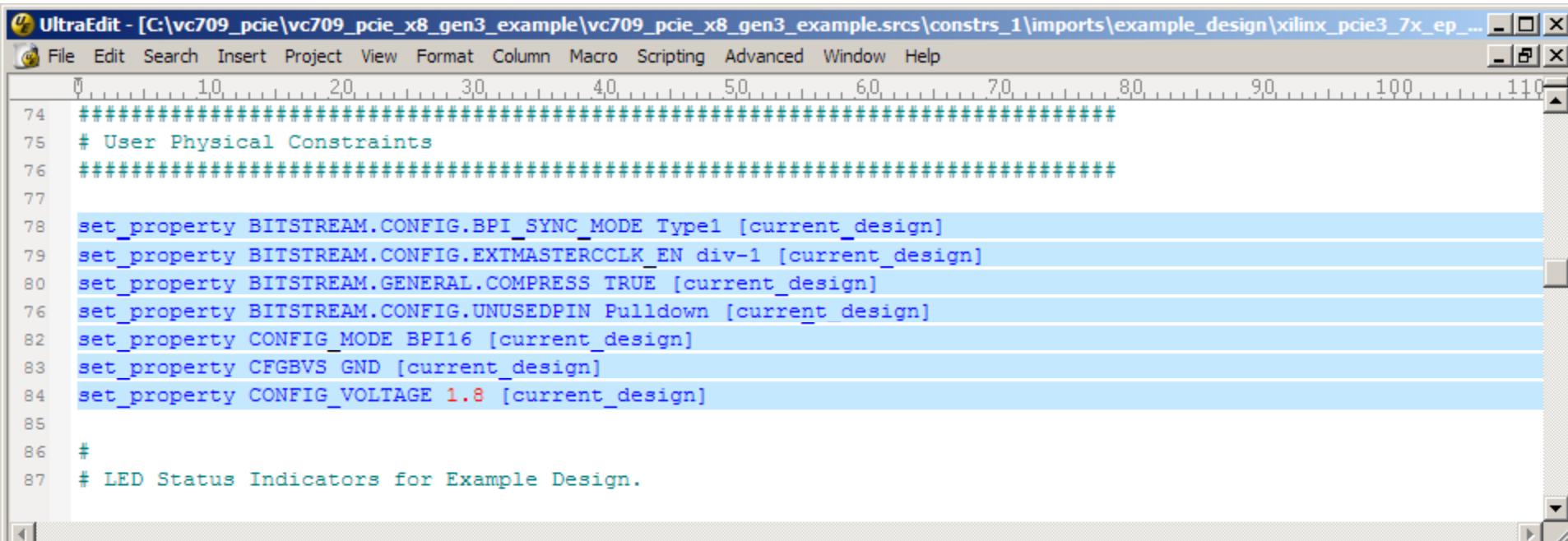
The screenshot shows the UltraEdit text editor displaying an XDC file. The file contains several lines of configuration properties. Lines 74 through 84 are highlighted in blue, indicating they are the new properties added to the file. Line 86 is also highlighted in blue. Line 87 is highlighted in red. The rest of the file is in black text. The file path shown in the title bar is `C:\vc709_pcie\vc709_pcie_x8_gen3_example\vc709_pcie_x8_gen3_example.srcs\constrs_1\imports\example_design\xilinx_pcie3_7x_ep...`.

```
UltraEdit - [C:\vc709_pcie\vc709_pcie_x8_gen3_example\vc709_pcie_x8_gen3_example.srcs\constrs_1\imports\example_design\xilinx_pcie3_7x_ep...]
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
74 #####
75 # User Physical Constraints
76 #####
77
78 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
79 set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
80 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
81 set_property BITSTREAM.CONFIG.UNUSEDPIN Pulldown [current_design]
82 set_property CONFIG_MODE BPI16 [current_design]
83 set_property CFGBVS GND [current_design]
84 set_property CONFIG_VOLTAGE 1.8 [current_design]
85
86 #
87 # LED Status Indicators for Example Design.
```

# Modify PCIe Core

## ► Details on the XDC constraints:

- G18 Maximum Frequency: 108 MHz; VC709 EMCCLK Frequency: 80 MHz
- **BITSTREAM.CONFIG.EXTMMASTERCCLK\_EN div-1**: Sets the EMCCLK in the FPGA to divide by 1, which meets the G18 Maximum Frequency specification
- **BITSTREAM.CONFIG.BPI\_SYNC\_MODE Type1**: For Numonyx G18 Family
- **BITSTREAM.GENERAL.COMPRESS TRUE**: Shrinks the bitstream



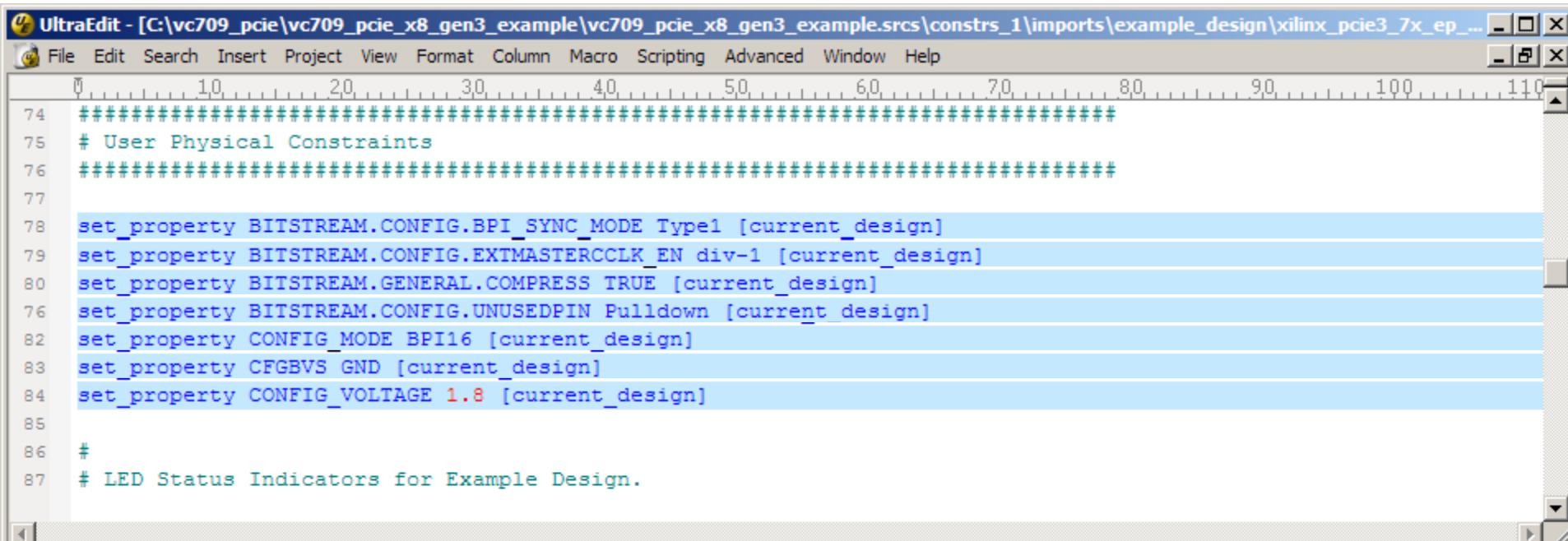
The screenshot shows a code editor window titled "UltraEdit - [C:\vc709\_PCIE\vc709\_PCIE\_x8\_gen3\_example\vc709\_PCIE\_x8\_gen3\_example.srcs\constrs\_1\imports\example\_design\xilinx\_PCIE3\_7x\_ep...]" displaying XDC constraint code. The code defines various properties for the bitstream configuration, including sync mode, master clock division, compression, and power settings. It also includes comments for LED status indicators.

```
UltraEdit - [C:\vc709_PCIE\vc709_PCIE_x8_gen3_example\vc709_PCIE_x8_gen3_example.srcs\constrs_1\imports\example_design\xilinx_PCIE3_7x_ep...
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
74 #####
75 # User Physical Constraints
76 #####
77
78 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
79 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
80 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
81 set_property BITSTREAM.CONFIG.UNUSEDPIN Pulldown [current_design]
82 set_property CONFIG_MODE BPI16 [current_design]
83 set_property CFGBVS GND [current_design]
84 set_property CONFIG_VOLTAGE 1.8 [current_design]
85
86 #
87 # LED Status Indicators for Example Design.
```

# Modify PCIe Core

## ► Details on the XDC constraints:

- **BITSTREAM.CONFIG.UNUSEDPIN Pulldown**: Sets unused pins to be pulled down
- **CONFIG\_MODE BPI16**: The BPI is 16 bits wide
- **CFGVBVS GND**: Set to GND when CONFIG\_VOLTAGE is either 1.5 or 1.8 V
- **CONFIG\_VOLTAGE 1.8**: The KC705 Configuration Bank (Bank 0) voltage is connected to 1.8 V

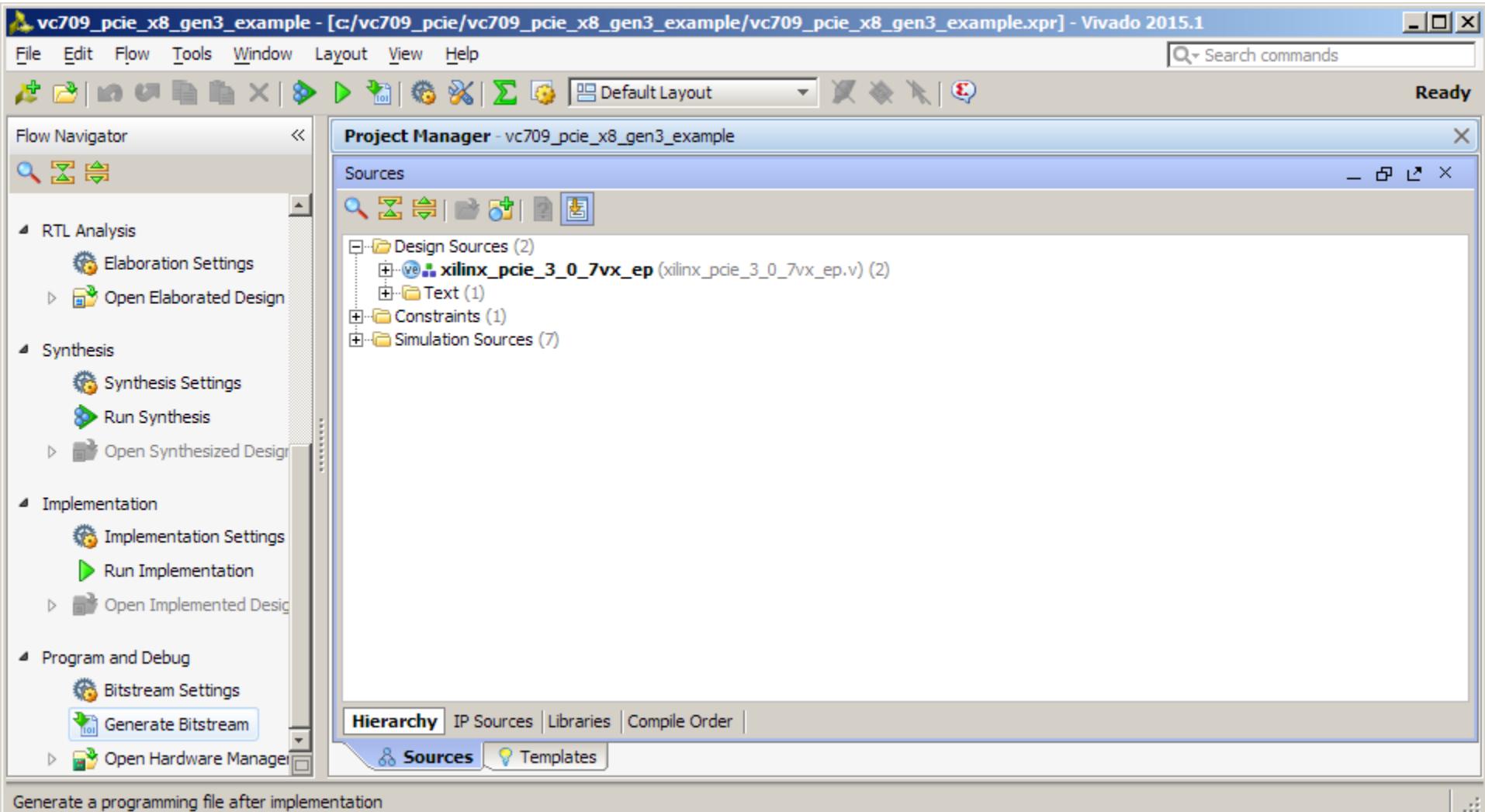


The screenshot shows a code editor window titled "UltraEdit - [C:\vc709\_pcnie\vc709\_pcnie\_x8\_gen3\_example\vc709\_pcnie\_x8\_gen3\_example.srcc\constrs\_1\imports\example\_design\xilinx\_pcnie3\_7x\_ep...]" displaying XDC constraint code. The code defines various properties for a PCIe core, including sync mode, ext master clock enable, compression, unused pin pulldown, configuration mode, configuration voltage, and LED status indicators.

```
UltraEdit - [C:\vc709_pcnie\vc709_pcnie_x8_gen3_example\vc709_pcnie_x8_gen3_example.srcc\constrs_1\imports\example_design\xilinx_pcnie3_7x_ep...
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
0 10 20 30 40 50 60 70 80 90 100 110
74 ######
75 # User Physical Constraints
76 #####
77
78 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
79 set_property BITSTREAM.CONFIG.EXTMASTERCLK_EN div-1 [current_design]
80 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
81 set_property BITSTREAM.CONFIG.UNUSEDPIN Pulldown [current_design]
82 set_property CONFIG_MODE BPI16 [current_design]
83 set_property CFGVBVS GND [current_design]
84 set_property CONFIG_VOLTAGE 1.8 [current_design]
85
86 #
87 # LED Status Indicators for Example Design.
```

# Compile Example Design

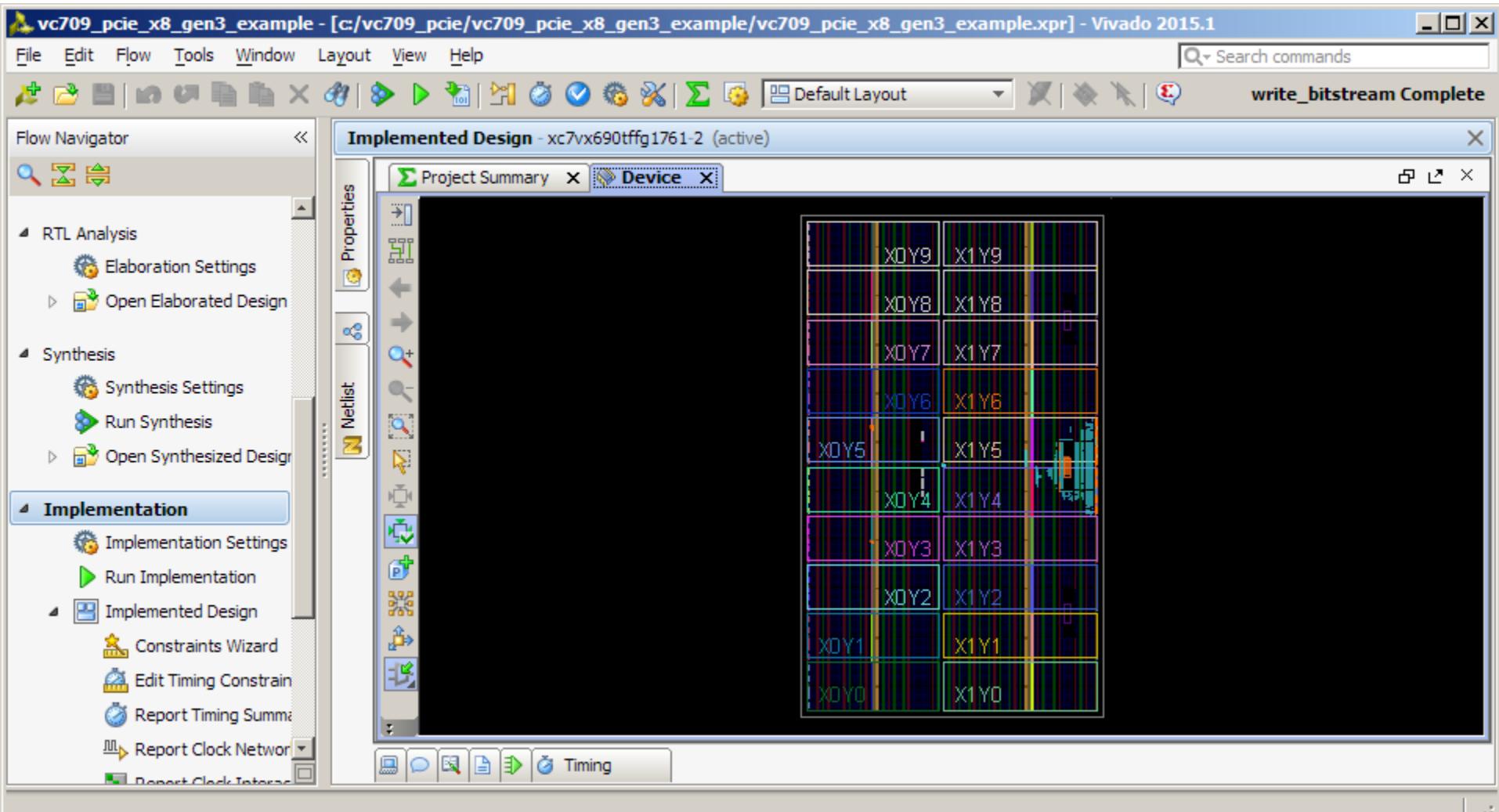
► Click on Generate Bitstream



# Compile Example Design

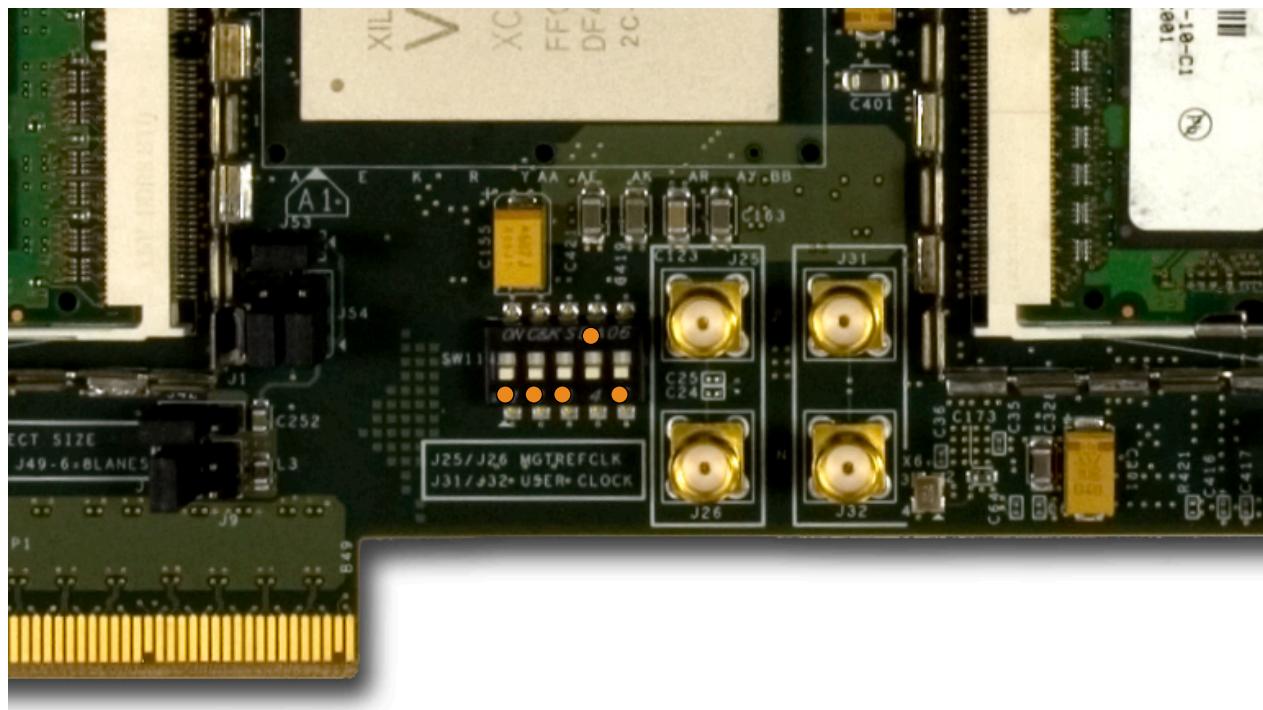
## ► Open and view the Implemented Design

- The PCIe Block can be seen in the middle of the implementation



# Hardware Setup

- Set SW11 to 00010 (1 = on, Position 1 → Position 5, left to right)
    - This enables Master BPI configuration from the Linear Flash
      - Flash A25, A24 = 00
      - FPGA mode pins M[2:0] = 010



**Note:** Presentation applies to the VC709

# Hardware Setup

► Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the VC709 board

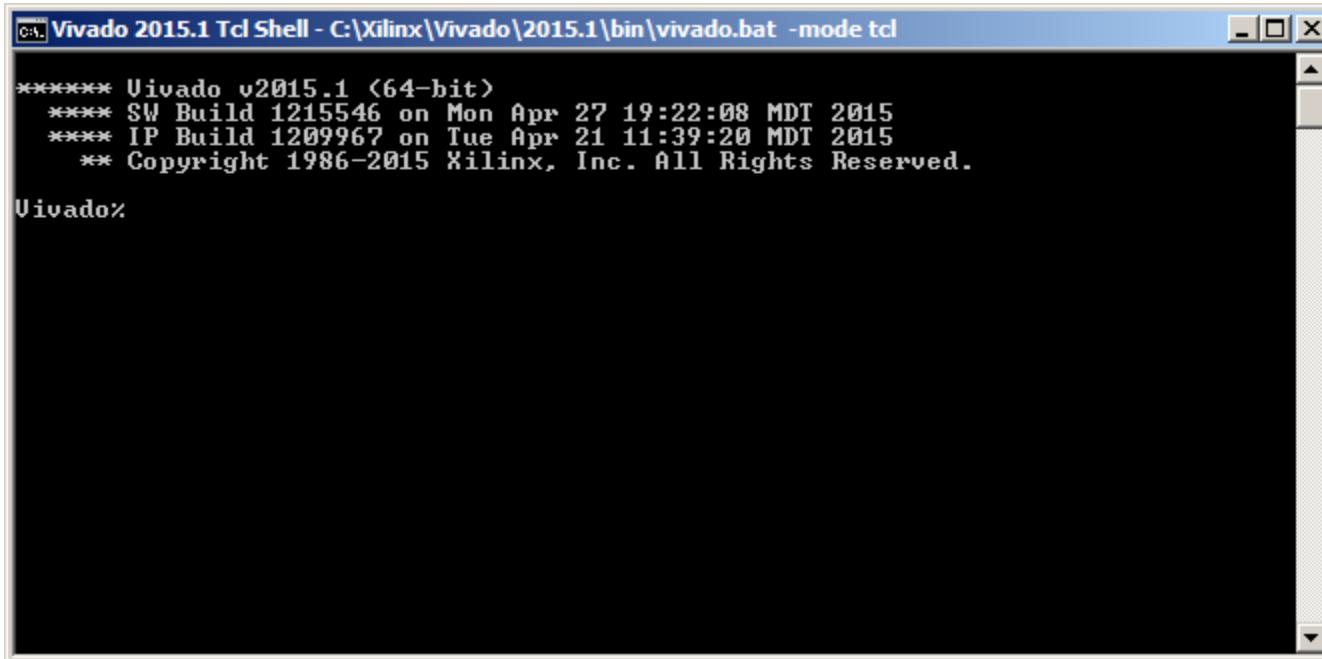
- Connect this cable to your PC
- Power on the VC709 board



# Generate PCIe MCS File

## ► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2015.1 →  
Vivado 2015.1 Tcl Shell**

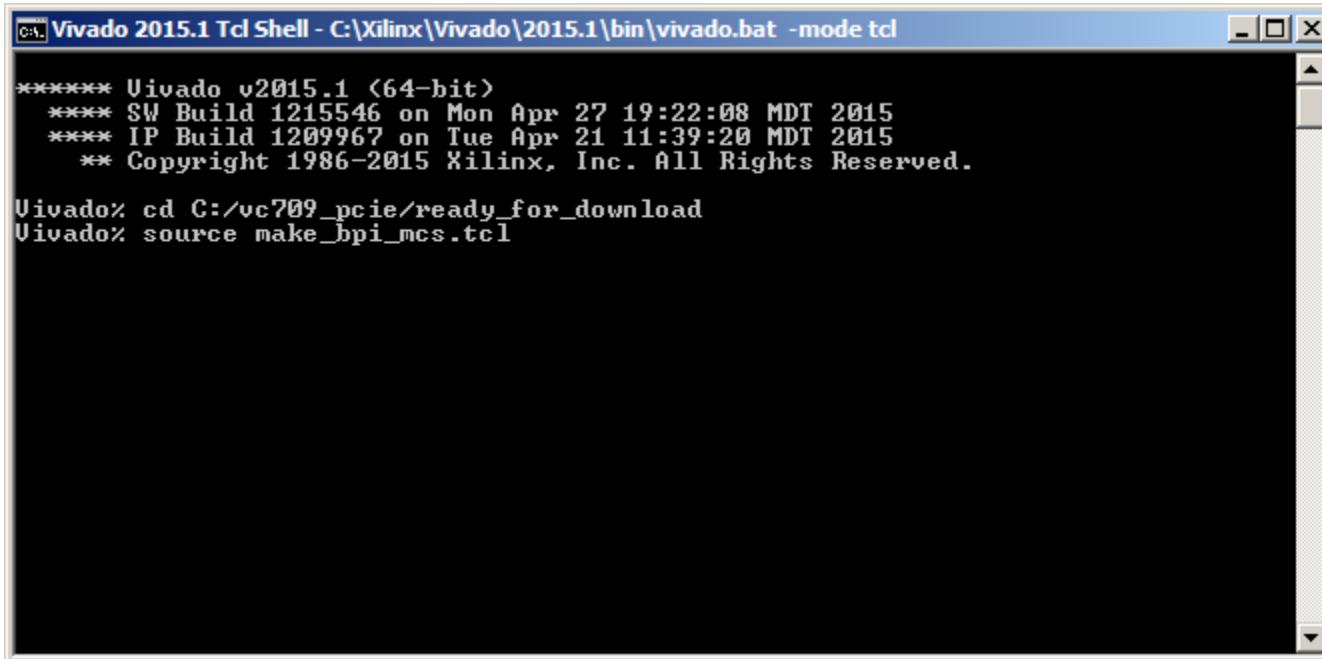


The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:  
\*\*\*\*\* Vivado v2015.1 (64-bit)  
\*\*\*\* SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
\*\*\*\* IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
\*\* Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
Vivado%

# Generate PCIe MCS File

- In the Vivado Tcl Shell type:

```
cd C:/vc709_pcie/ready_for_download  
source make_bpi_mcs.tcl
```



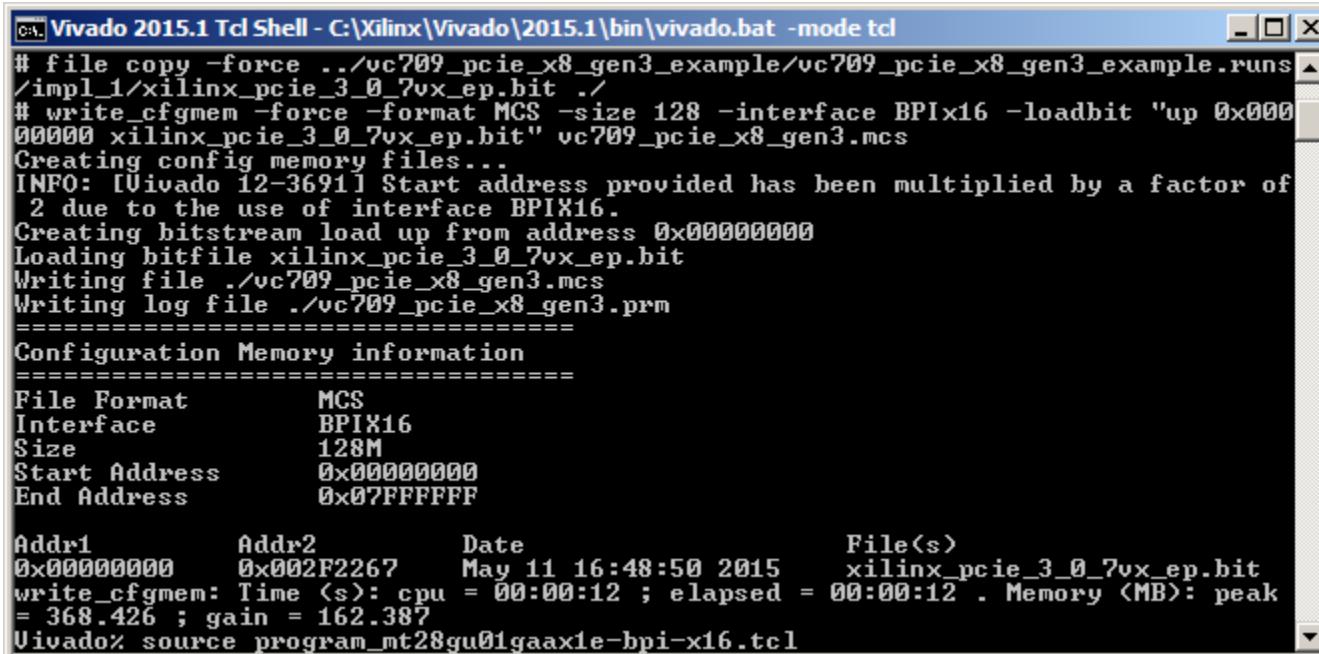
The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2015.1 (64-bit)  
***** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
***** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vc709_pcie/ready_for_download  
Vivado> source make_bpi_mcs.tcl
```

# Program BPI Flash with PCIe Design

- In the Vivado Tcl Shell type:

```
source program_mt28gu01gaax1e-bpi-x16.tcl
```



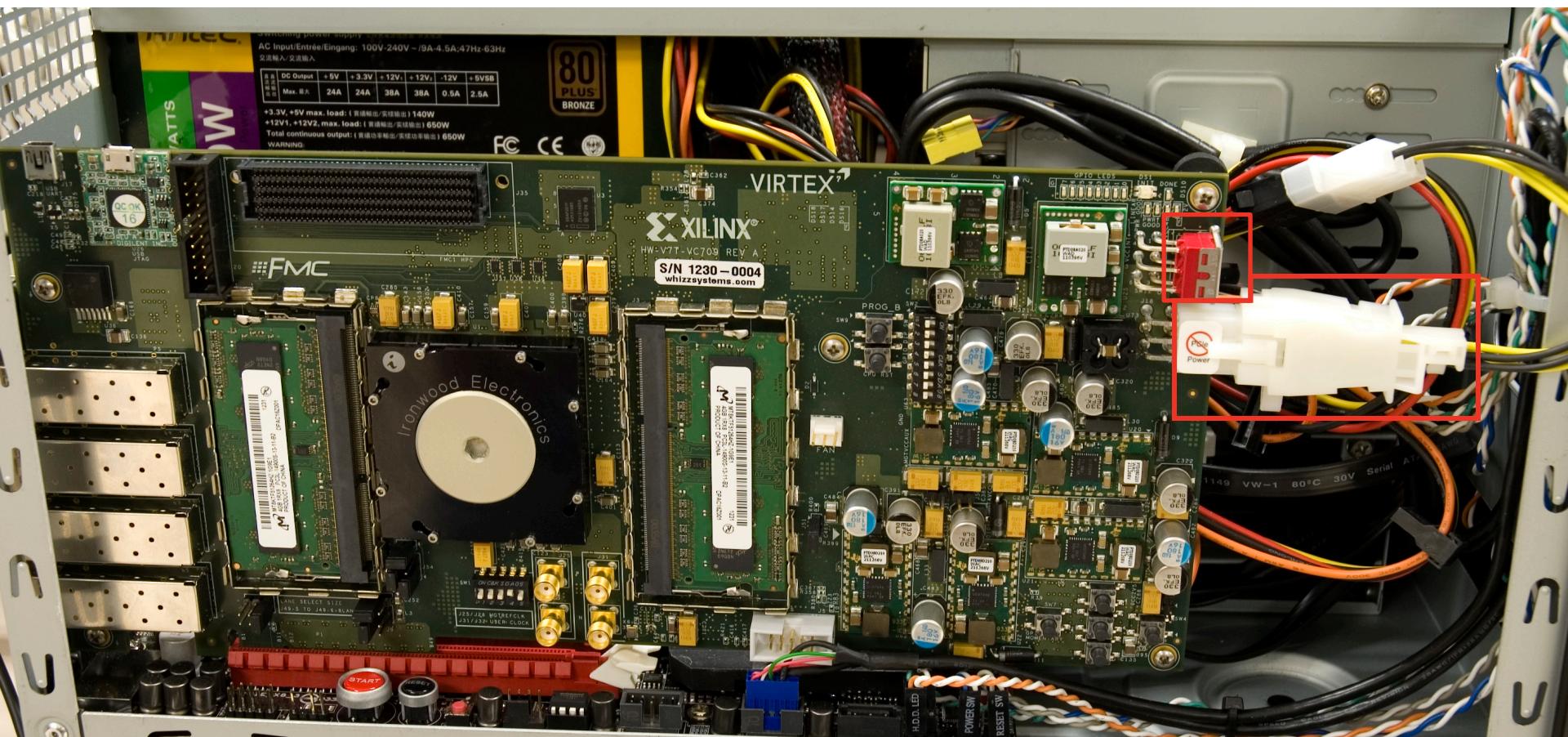
```
# file copy -force ../vc709_pcie_x8_gen3_example/vc709_pcie_x8_gen3_example.runs
# impl_1/xilinx_pcie_3_0_7vx_ep.bit /
# write_cfm -force -format MCS -size 128 -interface BPIx16 -loadbit "up 0x000
00000 xilinx_pcie_3_0_7vx_ep.bit" vc709_pcie_x8_gen3.mcs
Creating config memory files...
INFO: [Vivado 12-3691] Start address provided has been multiplied by a factor of
2 due to the use of interface BPIX16.
Creating bitstream load up from address 0x00000000
Loading bitfile xilinx_pcie_3_0_7vx_ep.bit
Writing file ./vc709_pcie_x8_gen3.mcs
Writing log file ./vc709_pcie_x8_gen3.prm
=====
Configuration Memory information
=====
File Format      MCS
Interface        BPIX16
Size            128M
Start Address   0x00000000
End Address     0x07FFFFFF

Addr1          Addr2          Date           File(s)
0x00000000    0x002F2267    May 11 16:48:50 2015  xilinx_pcie_3_0_7vx_ep.bit
write_cfm: Time <s>: cpu = 00:00:12 ; elapsed = 00:00:12 . Memory <MB>: peak
= 368.426 ; gain = 162.387
Vivado> source program_mt28gu01gaax1e-bpi-x16.tcl
```

# Hardware Setup

## ► Insert the VC709 Board into a Gen3 PCIe slot

- Use the included PC Power adapter; turn on Power Switch

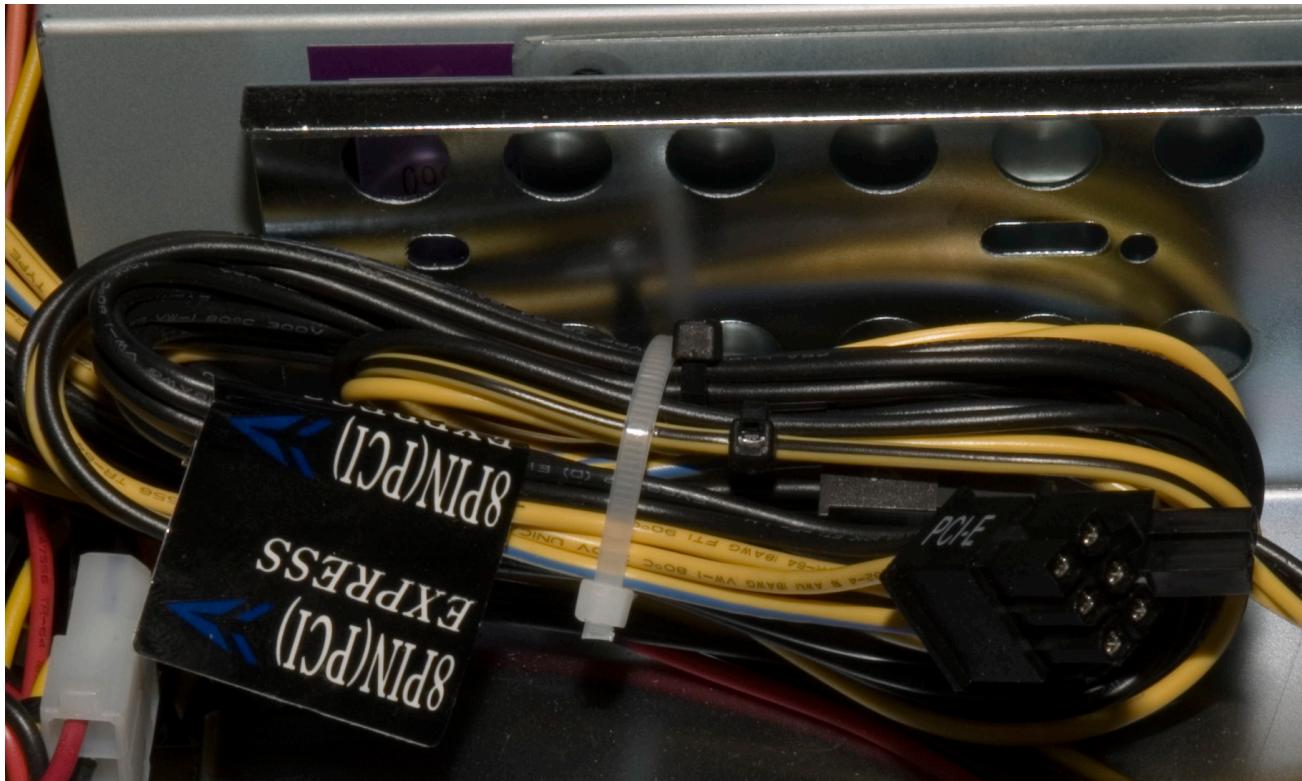


Note: Presentation applies to the VC709

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# Hardware Setup

- Do not use the PCIe connector from the PC power supply

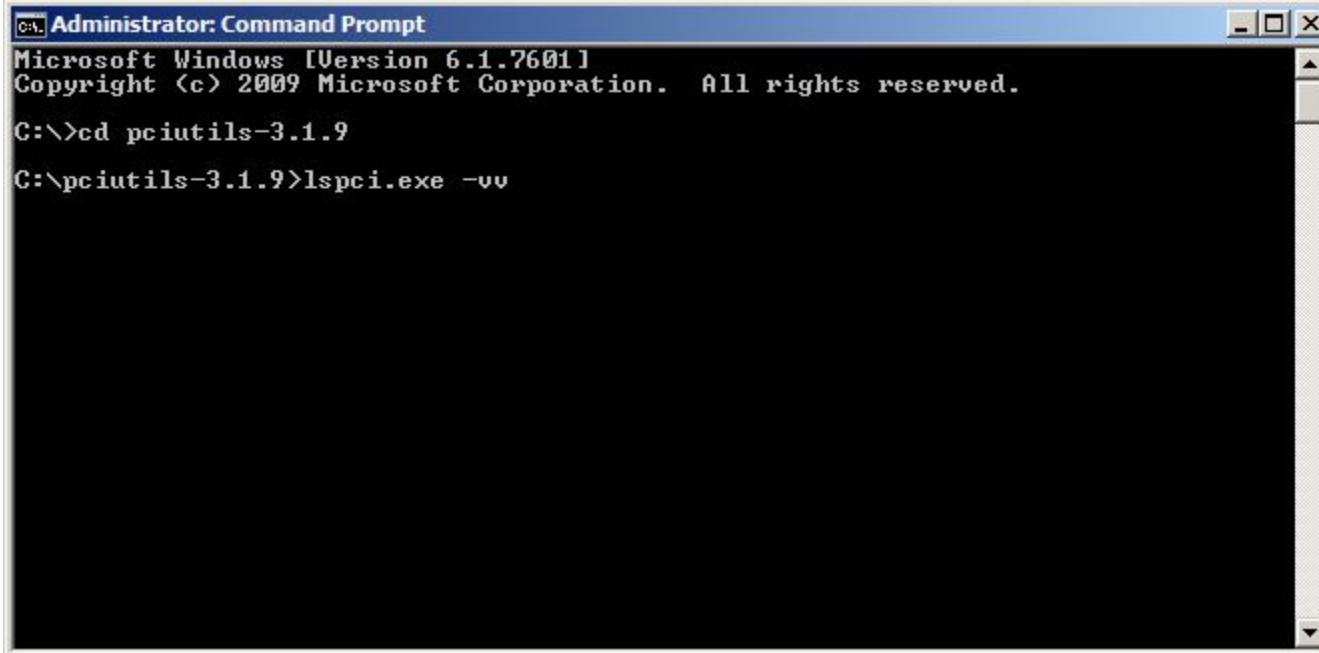


# Running the PCIe x8 Gen3 Design

- Power on the PC
- Open an Administrator command prompt and type:

```
cd pciutils-3.1.9
```

```
lspcie.exe -vv
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window title bar includes the text "Administrator: Command Prompt" and the standard window controls (minimize, maximize, close). The main area of the window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\>cd pciutils-3.1.9
C:\pciutils-3.1.9>lspci.exe -vv
```

The command "lspci.exe -vv" has been entered and is waiting for output.

# Running the PCIe x8 Gen3 Design

- ▶ View the Xilinx item in the results at 8GT/s (Gen3) and Width x8

```
Administrator: Command Prompt
03:00.0 Memory controller: Xilinx Corporation Device 7038
    Subsystem: Xilinx Corporation Device 0007
    Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Step
    ping- SERR- FastB2B- DisINTx-
    Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DESEL=fast >TAbsort- <TAbsort-
    <MAbsort- >SERR- <PERR- INTx-
        Latency: 0, Cache Line Size: 64 bytes
        Interrupt: pin ? routed to IRQ 255
        Region 0: Memory at fb400000 (32-bit, non-prefetchable)
        Capabilities: [80] Power Management version 3
        Flags: PMEClk- DSI- D1- D2- AuxCurrent=0mA PME<D0-,D1-,D2-,D3hot
        -,D3cold->
            Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
            Capabilities: [90] MSI: Enable- Count=1/1 Maskable+ 64bit+
                Address: 0000000000000000 Data: 0000
                Masking: 00000000 Pending: 00000000
            Capabilities: [c0] Express <v2> Endpoint, MSI 00
                DevCap: MaxPayload 512 bytes, PhantFunc 0, Latency L0s <64ns, L1
                <1us
                ExtTag- AttnBtn- AttnInd- PwrInd- RBE+ FLReset-
                DevCtl: Report errors: Correctable- Non-Fatal- Fatal- Unsupported
                RlxdOrd- ExtTag- PhantFunc- AuxPwr- NoSnoop+
                MaxPayload 256 bytes, MaxReadReq 512 bytes
                DevSta: CorrErr- UncorrErr- FatalErr- UnsuppReq- AuxPwr- TransPe
                nd-
                LnkCap: Port #0, Speed 8GT/s, Width x8, ASPM unknown, Latency L0
                unlimited, L1 unlimited
                ClockPM- Surprise- LLActRep- BwNot-
                LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- Retrain- CommClk-
                ExtSynch- ClockPM- 0.4widDis- BWInt- AutBWInt-
                LnkSta: Speed 8GT/s, Width x8, TrErr- Train- SlotClk- DLActive-
                BWMgmt- ABWMgmt-
                DevCap2: Completion Timeout: Range B, TimeoutDis+
                DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-
                LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-, S
                electable De-emphasis: -6dB
                Compliance- ComplianceSOS-
                Transmit Margin: Normal Operating Range, EnterModifiedC
                ompliance- ComplianceSOS-
                LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+, E
                qualizationPhase1+
                EqualizationPhase2+, EqualizationPhase3+, LinkEqualizat
                ionRequest-
```

## References

# References

## ► PCIe Base Specification

- PCI SIG Web Site
  - <http://www.pcisig.com/home>

## ► Xilinx PCI Express

- Xilinx PCI Express Overview
  - <http://www.xilinx.com/products/technology/pci-express.html>
- 7 Series Integrated Block for PCI Express Product Page
  - [http://www.xilinx.com/products/intellectual-property/7\\_series\\_pci\\_express\\_block.html](http://www.xilinx.com/products/intellectual-property/7_series_pci_express_block.html)
- 7 Series Integrated Block for PCI Express Product Guide – PG054
  - [http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_7x/v3\\_1/pg054-7series-pcie.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_7x/v3_1/pg054-7series-pcie.pdf)
- Virtex-7 FPGA Gen3 Integrated Block for PCI Express - Release Notes
  - <http://www.xilinx.com/support/answers/47441.htm>

# References

## ► Micron NOR Flash

- Micron G18 Flash
  - <http://www.micron.com/partsnor-flash/parallel-nor-flash/mt28gu256aaa1egc-0sit>
- Datasheet
  - [http://www.micron.com/~media/documents/products/data-sheet/nor-flash/serial-nor/n25q/n25q\\_256mb\\_3v\\_65nm.pdf](http://www.micron.com/~media/documents/products/data-sheet/nor-flash/serial-nor/n25q/n25q_256mb_3v_65nm.pdf)

## ► Xilinx Generation 7 Configuration with BPI Flash

- 7 Series FPGAs Configuration User Guide – UG470
  - [http://www.xilinx.com/support/documentation/user\\_guides/ug470\\_7Series\\_Config.pdf](http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf)
- Vivado Design Suite Programming and Debugging User Guide – UG908
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2015\\_1/ug908-vivado-programming-debugging.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug908-vivado-programming-debugging.pdf)
- BPI Fast Configuration with 7 Series FPGAs – XAPP587
  - [http://www.xilinx.com/support/documentation/application\\_notes/xapp587-bpi-fast-configuration.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp587-bpi-fast-configuration.pdf)

# Documentation

# Documentation

## ➤ Virtex-7

- Virtex-7 FPGA Family
  - <http://www.xilinx.com/products/silicon-devices/fpga/virtex-7/index.htm>
- Design Advisory Master Answer Record for Virtex-7 FPGAs
  - <http://www.xilinx.com/support/answers/42944.htm>

## ➤ VC709 Documentation

- Virtex-7 FPGA VC709 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html>
- VC709 Getting Started Guide – UG966
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug966-v7-xt-connectivity-getting-started.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug966-v7-xt-connectivity-getting-started.pdf)
- VC709 User Guide – UG887
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug887-vc709-eval-board-v7-fpga.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug887-vc709-eval-board-v7-fpga.pdf)