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A configurable 2-Gbps LVDS transceiver in 150-nm CMOS with pre-emphasis, equalization, and slew rate control

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SUMMARY

A configurable full-duplex low-voltage differential signaling transceiver is presented, which can be configured to operate either for smaller differential channels (a few inches of striplines) or for longer channels (10 m of twisted pair cables). The configurability is embedded in the form of functionalities like pre-emphasis, equalization, and slew rate control within the transceiver. The transmitter employs a hybrid voltage–current-mode driver, which due to replica action, achieves a high-impedance current-mode signal dispatch and at the same time provides a matched impedance at the near end for improved intersymbol interference. The transmitter achieves slew rate control through a band-limited pre-driver, while the pre-emphasis is achieved through a capacitive feed-forward. The receiver employs a large-input common-mode first stage enclosed in a common-mode control loop that enables its first stage to also act like a domain shifter (VDDIO-to-VDDCORE) reducing the overall power consumption. The equalization in the receiver is implemented by using carefully sized active inductive loads inside the receiver. The transceiver is designed and fabricated in 150-nm complementary metal–oxide–semiconductor, sharing the space with a larger die, occupying an area of $400 \times 400\mu$m. The measurement results demonstrate that the transceiver is operating at 2 Gbps both for a 4-in microstrip and a 10-m twisted pair CAT6 cable with 30 and 180 ps of total jitter, respectively. The built-in impedance calibrator minimizes the spread in the on-die termination at the near end provided by the transmitter-minimizing bit error rate across process, voltage, and temperature corners. The transmitter consumes a total power of 17 mW operating at 2 Gbps, that is, 8.5 pJ/bit of energy consumption; the receiver consumes a total power of 3.5 mW while driving a load of 5 pF at 2 Gbps.

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KEY WORDS: LVDS transceiver; voltage-mode driver; low-power receiver; pre-emphasis; equalization; slew rate control; 150-nm CMOS; domain shifter

1. INTRODUCTION

Technology scaling has enabled remarkable increase in operational frequencies of the integrated circuits (ICs). However, the speed gap between on-chip and off-chip data rates has widened because parallelism in the interconnects, that is, simply increasing the bus widths, cannot effectively cater for data rates above Gbps/pin, especially when interconnects are behaving like transmission lines and are necessitating for impedance-matched electrical signaling with the need to address power consumption, increased complexity, and cost of packaging together. Therefore, there is a constant push to replace legacy parallel buses with Gbps/pin point-to-point serial input–output (IO) interfaces operating in conjunction with high-speed serializers and deserializers [1–6].

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In order to achieve high off-chip data rate while keeping power dissipation low, low-voltage differential signaling (LVDS) technique was proposed and widely accepted [7] in prevalent applications. LVDS works by transmitting a low-swing differential voltage signal across the channel with common-mode noise immunity due to its differential signaling scheme. Furthermore, due to the low swing and differential signaling, electromagnetic interference immunity and compliance are improved compared with the single-ended signaling. This enables higher off-chip data rate with fewer IOs and ultimately results in a reduced cost of packaging and thermal management.

The LVDS transceiver conventionally consists of a switching current-mode driver, which typically pumps 3.5 to 4.5-mA current to a 100-Ω termination resistor at the far end. This current-mode signal transmission takes advantage of the fact that the dispatched current is immune to voltage drops across the channel, and the signal integrity at the far end remains unaffected [1–6, 8]. However, an LVDS IO is mostly operating at higher data rates with longer interconnects, taking the communication in transmission line regime. Therefore, a current-mode transmitter, dispatching the signal at a high impedance, creates impedance mismatch at the near end, and in this scenario, an additional termination resistor is needed at the near end for high-speed applications to reduce intersymbol interference (ISI) [9], also known as the class II termination scheme. The easiest way to achieve this is by using a passive termination; however, it doubles the signal current requirement for a targeted output voltage swing, thus doubling the power consumption and generating thermal noise at the near end [10].

Several LVDS transceiver topologies have been proposed in the literature [1–6, 10–13]. Reference [11] demonstrates replacing the near-end termination by a passive resistor–capacitor combination with a current-mode transmitter. This scheme minimizes the reflections at the near end by off-chip band-limited termination matching instead of a resistive termination and therefore it does not consume static power. However, this approach requires a strict control on the induced notch by the off-chip passive network. This strict dependency is reduced by introducing slew control in the driver, which low-pass shapes the dispatched signal and therefore reduces the high-frequency contents which are the main reason behind reflections due to impedance discontinuities. However, slew rate control reduces the bandwidth of the system, making it unsuitable for longer channel at higher data rates [10–12].

A voltage-mode driver does not need the near-end termination because the driver itself provides a matched impedance as its rout [7]. Metal–oxide–semiconductor field-effect transistors (MOSFETs) switching in their triode region are sometimes employed in the impedance-matched transmitter. However, the transition of a MOSFET from off-to-on state incurs going from cut-off region to the saturation region and then ultimately to triode region. As a result, these switches demonstrate a variable impedance, especially during the transition, and this effect manifests in the form of reflections at the near end. Reference [6] employs passive poly or n-well resistors to provide matched 50-Ω impedance in each branch. These approaches suffer from process, voltage, and temperature (PVT) variations and therefore a configurable resistor bank is employed to trim the termination impedance post silicon. At the same time, implementing a complete 50-Ω resistance by using a passive resistor puts stringent requirements on the current steering switches of the transmitter as now, they are expected to have very low impedances ($<5\,\Omega$), dictating very large devices operated in deep triode region. Such large sizes increase capacitive loading right at the output nodes and therefore decrease the data rate of the transmitter [14]. Reference [14] therefore proposes using MOSFET switches in series with passive resistors where 70% of the impedance comes from the linear passive resistors while 30% nonlinear part comes from the MOSFETs. A similar approach in Ref. [15] uses passive resistors in series with source-follower output stages, that is, series combination of 1/gm from the source follower and the passive resistors. However, to achieve the required matched differential termination, it also ends up consuming twice the amount of power consumption; that is, it becomes almost equivalent to using a passive class II termination. Another voltage-mode driver [6] utilizes Bipolar Junction Transistor–CMOS devices, in which the Bipolar Junction Transistor devices' higher transconductance (gm) is used to achieve the match impedance, but it puts up a costly requirement on the process.

To exploit the advantages of both current-mode and voltage-mode transmissions together, Ref. [16] proposes an asymmetric active source termination, which allows reducing the current consumption and

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impedance matching similar to a voltage-mode configuration while still dispatching the signal in current mode. The demonstrated driver in this work derives its core from Ref. [16]. As demonstrated by Ref. [11], slew rate control can help dampen the high-frequency contents in the signal and ultimately reduce ISI. On similar lines, the transmitter in this design embeds digitally controllable slew rate control. Additionally, slew rate control can help reduce simultaneous switching noise (SSN). On the other extreme, for very long channels which act as low-pass filters for the dispatched signals, the received signal at the far end suffers from reduced edge rate and therefore fails to reach the minimum voltage swing within the switching period. This necessitates for pre-emphasis functionality such as proposed in Refs [17, 18] to pre-boost the high-frequency components of the dispatched signal at the near end, compensating for the low pass-natured channel. The presented driver embeds digitally controllable passive pre-emphasis.

On the receiving side, one of the most critical issues is to handle a large input common-mode variation to accommodate the ground offset so that the transmitting and receiving devices can have the freedom of using different grounds [7]. The required ground offset is ±1 V, with 1.2 V as nominal common mode; that is, the common-mode range is from 0.2 to 2.2 V. The literature contains four categories of rail-to-rail receiver stages [19]: (1) consisting of complementary p-type MOS (PMOS) and n-type MOS (NMOS) input stages such as proposed in Ref. [20], (2) consisting of the level-shifted receiver pairs as shown in Ref. [21], (3) consisting of charge-pump principle, and (4) consisting of PMOS input pair mostly in folded cascode configuration such as proposed in Ref. [2]. The charge pumps require a larger area for capacitors and create switching noise and are therefore not preferred for IO applications. Because the folded cascode structure requires two current sources, achieving a high bandwidth requires a high value of transconductance and therefore high bias currents, that is, a power-hungry receiver [2,22]. To further restore the high-frequency contents of the received signal, even in the presence of pre-emphasis in the transmitter from which the signal was dispatched, a relatively low-Q active equalization is required in the receiver, which results in improved eyes and reduced jitter [22, 23]. The presented receiver in this design employs a PMOS input pair with active PMOS load demonstrating an inductive behavior at higher frequency, therefore achieving equalization with a very large input common-mode range.

This paper is organized four sections. Section 2 presents the design details of the LVDS transceiver. Section 3 presents the measurement results and pertinent discussions. Section 4 concludes the paper.

2. DESIGN DESCRIPTION

2.1. Transmitter design

The transmitter employs a hybrid-mode operation. It takes advantage of both current and voltage-mode operations. The schematic of the transmitter is shown in Figure 1. The main components of the transmitter are single-ended-to-differential converter, the pre-driver (PD), and the output driver (OD). Supporting circuitry such as the calibration block and common-mode feedback is also a part of the transmitter. The transmitter embeds multiple configurable performance-enhancing functionalities such as pre-emphasis and slew control.

The OD of the transmitter is responsible for LVDS signaling over the physical media. The OD's main core consists of NMOS transconductors (M1 and M2) connected to active NMOS source-follower loads (M3 and M4). The rout of the driver is relatively low due to the active loads and therefore, from this perspective, the OD can be considered a voltage-mode transmitter. However, this voltage-mode core is operated in current mode by using the tail current source (M6), while the transistor M5 is operated in triode to properly define the common-mode voltage at the drains of M3 and M4. M5 is dimensioned such that its R_{ON} is around 200 Ω.

At the same time, the voltage-mode core is operated by the PD through replica action [15]. The PD is a scaled-down replica of the OD, generating the same v_{DS} across its transconductors (M1PD and M2PD) as that of the OD's transconductors. The outputs of the PD are connected to the gates of the active source-follower loads of the OD. As a result, during a transition, the small-signal v_{gs} of M3 and M4 are significantly reduced. Therefore, the gm of these loads becomes considerably reduced,

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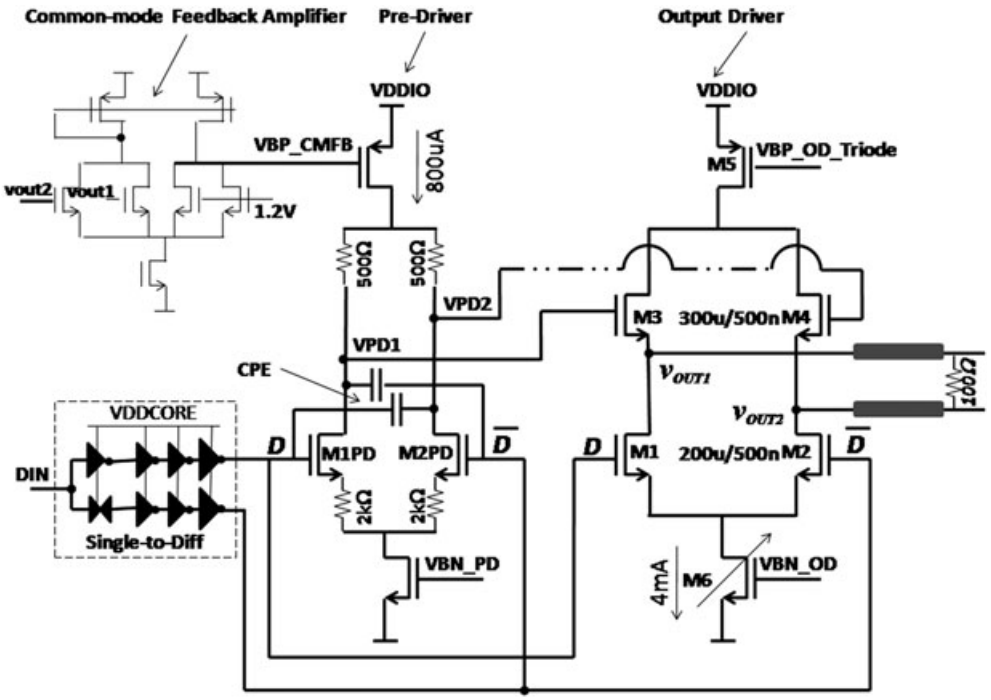

Figure 1. Main functional components of the transmitter, single-ended to differential converter, pre-driver, output driver, and the common-mode feedback amplifier.

and their rout = 1/gm becomes very large, that is, a behavior close to a current source. Therefore, while transmitting the data, due to the replica action, the OD's core behaves like a current-mode transmitter where the transconductors are steering current from current sources from one branch to the other.

Because the transmission is performed at a high impedance (>50 Ω), both near-end and far-end reflections are expected to arrive back at the transmitter. A typical current-mode transmitter is unable to terminate these reflections and therefore it mostly requires an external near-end termination, and this requirement in a current-mode transmitter doubles the current requirements and proves to be power hungry. The under-consideration OD, however, provides an accurate termination for the reflections by using the small-signal rout of the active source-follower loads. Because the reflected signal does not trigger replica action and the active loads experience a finite small-signal change in v_{gs}, their incremental resistance becomes defined by their gm, which is made equal to the impedance of the transmission line under typical PVT conditions.

Therefore, a high-impedance current dispatch on the physical channel is achieved along with the advantage of termination impedance at the near end. It should be noted that this transmitter does not minimize reflections by impedance matching while transmitting data; instead, it provides matched impedance for the reflecting signals so they do not cause ISI by further bouncing back on to the channel. The impedances for both scenarios are expressed in Eqns (1) and (2).

$$R_{OUT\_TRANSMISSION} = \frac{1}{(\delta)gm} \text{where } \delta = \frac{v_{\text{OUT1}} - v_{\text{PD1}}}{v_{\text{OUT1}}} \tag{1}$$

$$R_{OUT\_REFLECTION\_DIFF} = \frac{1}{gm1} + \frac{1}{gm2} \sim 100\Omega \tag{2}$$

Figure 2 depicts the current flow during one of the operating scenarios of the OD. It should be noted that M2 from the transconductors is on, while M1 is off; M3 and M4 from the loads are both on. Therefore, I_{LOAD}, which is the current through the far-end termination resistor R_L, initiates from the current source M5, flows through M3, traverses through the channel and the far-end termination and

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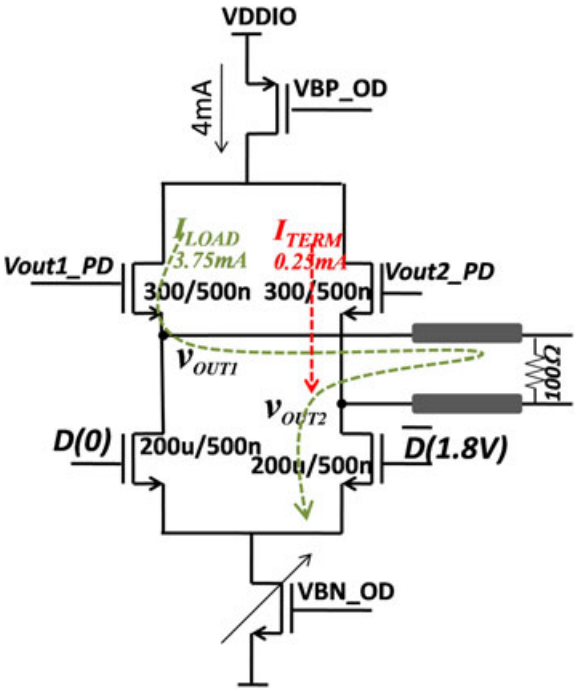

Figure 2. Current distribution within output driver during one of the configurations.

comes back to flow through M2, and finally ends up flowing through current source M6. The typical value of this current is set 4 mA, therefore producing a 400-mV signal across R_L. However, there is an extra component of the current flowing through M4, I_{TERM}, which is configured to be $I_{LOAD}/16 = 250\,\mu A$ (approximately). The reason of keeping M4 biased at a nonzero current even when it is not participating in driving the far-end load is based on the fact that both M3 and M4 are also responsible for providing termination for the signals being reflected to the transmitter due to high-impedance current-mode dispatch. The effective gm of M4 in this scenario is reduced by a factor of $2\sqrt{2}$, as both M3 and M4 are sized to provide gm = 20 mA/V when biased at 2 mA. At the same time, due to the diversion of most of the current toward M3, its gm becomes boosted by a factor of $\sqrt{2}$. The differential termination resistance still falls around 90 Ω, which is a reasonable trade-off as due to the differential nature, LVDS can tolerate a certain degree of impedance mismatch.

The PD differential amplifier is a scaled-down version of the OD. Because VPD1 and VPD2 are used to drive the gates of active source-follower loads and because the output common mode is 1.2 V, the common-mode voltage required is $V_{TH\text{-}SF} + V_{OD\text{-}SF} + 1.2\,V = 2.2\,V$ (approximately). To achieve this common mode and to bring the input devices (M1PD and M2PD) into saturation region for their large overdrives because digital signal is directly applied to them, degeneration resistors of 2 kΩ are used. This is carried out to make sure that the drain resistors and the bias current are used only to generate the required small-signal voltage change to drive the OD, which results in a faster and power-efficient PD at the cost of reducing the gm of the input devices. The output of the PD is capacitively loaded by the active loads of the OD, and because the gm of the PD's input devices is relatively low due to the reduced bias current, the resulting bandwidth is not high enough to produce a square wave output in response to the differential digital square wave input; instead, PD produces a slewed output, which is utilized for slew rate control and SSN minimization as discussed in detail in the following text.

The slewed output of the PD results in a low pass-shaped OD's output. The high-frequency contents of the signal are the main source of reflections on the channel in the presence of impedance discontinuities. The low-pass shaping of the transmitted signal attenuates the high-frequency components, and as a result, the reflections are minimized. At the same time, OD is the main current drawing component from the power supply line. If multiple IOs in an IO slice switch at the same time and draw a large amount of high edge-rate impulsive current, then the system can suffer from

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SSN where the power line's inductive behavior resists in catering the increased current requirements. Therefore, a slewed output which implies a slewed current drawn from the power supply can minimize the possibility of SSN.

However, the inherent low-pass nature of the transmitter would not be able to fulfill the minimum swing requirements of the LVDS standard at the far end for a relatively longer channel at the required data rate (e.g., a 10-m twisted pair cable operating above 1 Gbps). It is a standard practice to employ pre-emphasis in the transmitter to boost the high-frequency contents of the signal to pre-compensate for the low-pass filtering which would be incurred during traversal through the dissipative channel.

The designed transmitter has an inherent resonance at higher frequencies due to the reasons explained in the following text; if this resonance is configured to lie around second to fifth harmonic of the transmitted fundamental tone (2 GHz in this case), then an inherent pre-emphasis can be achieved. The transmitter can be considered as a common-source amplifier with active source-follower loads. The low-frequency small-signal rout of this amplifier is the reciprocal of the load transconductance. However, the Gate-to-Source-Capacitance (CGS) of the loads exhibits a shunting behavior at higher frequencies, reducing the small-signal v_{gs} and therefore, reducing the transconductance and increasing the rout. This is the reason why source followers are considered to display an inductive behavior from the rout perspective. The frequency of this resonance or the placement of the zero depends on the resistance that is driving the source-follower loads and their Connected Grid Switch. However, the overall behavior of the transmitter is large signal and therefore small-signal perspective defines only a portion during the transition where the behavior in the preceding texts manifests itself to achieve a higher edge rate at the output of the transmitter. It can be safely assumed that after 60% of the transition, the transconductor devices (M1 and M2) have already left saturation region, and now application of small-signal approximation is not valid. The other reason for the transmitter to exhibit resonance at higher frequencies is replica action, which again reduces the gm of the loads by reducing their v_{gs}, resulting in a relatively higher rout at the output. However, the argument in the preceding texts of this effect being valid only for a part of transition holds true again. Therefore, to achieve a properly controlled pre-emphasis, this transmitter embeds a capacitive feed-forward structure from the digital input to the OD's input to by-pass the low-pass PD, which responds in a slewed manner. This capacitive feed-forward triggers OD as soon as the digital input arrives and through a capactively coupled glitch pre-charges the output nodes of OD, as shown in Figure 1.

Because the termination provided by the transmitter for the reflecting signal depends on the gm of the active source-follower load, this makes the termination heavily process dependent and temperature dependent and therefore a calibration mechanism is needed. Similar calibration mechanisms are employed in DDR3, DDR4 SSTL/POD signaling in memory's physical layer. One calibrator IO is placed in the vicinity of a cluster of several active IO pads. This calibrator IO is used only for calibration purposes and does not participate in transceiver operation. Once calibration is carried out, the impedance code is copied to all the IOs in the cluster, assuming that the process and temperature gradient has affected the calibrator and the other IOs in the same manner due to vicinity.

The designed calibration logic, as shown in Figure 3, comprises a voltage reference generation by using resistance ladder, modulating the reference voltages at a relatively low-frequency carrier (MHz range), a difference-difference amplifier (DDA), a comparator, and a counter. The designed calibrator requires an external precision termination at the near end because it does not connect to a channel. The calibrator modulates the fixed and known reference voltages and applied it to the OD's input directly to transmit through the calibrator's transmitter starting from lowest gm value. There is no PD in the calibrator cell because replication action is not required, and a complete small-signal voltage division is required to be observed at the output. The gm value is configured by the current sources at the top and bottom of this transmitter core. The resulting output pulses are received at the near end and are compared with the pre-defined pulses that were used to excite the transmitter. Until the required voltage division is achieved, this process continues and counter is incremented to increase the tail currents. The DDA in the calibration loop is being used as a regenerative comparator; the output of the DDA is connected to a cross-coupled NAND-based latch to hold the output, while DDA intermediate nodes are being pre-charged.

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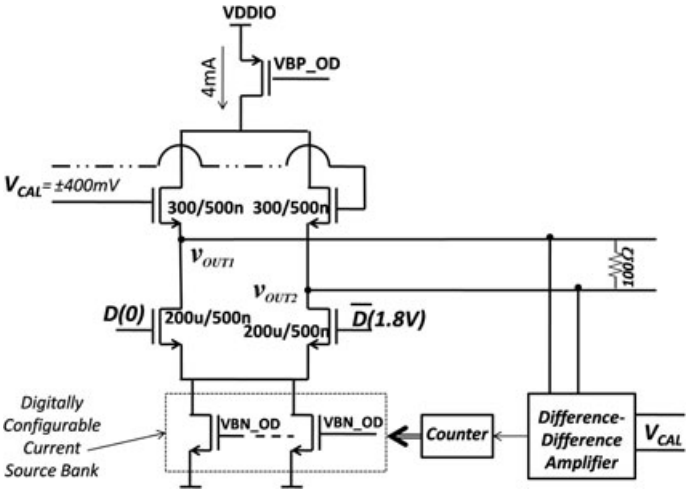

Figure 3. Calibration mechanism for the output impedance of output driver.

2.2. Receiver design

As shown in Figure 4, the receiver is a two-stage amplifier. The first stage caters for the large input common-mode requirements (0.2–2.0 V) and provides a limited gain with a configurable equalization. The first stage has embedded domain-shifting capability (from VDDIO to VDDCORE) which removes the need for a separate contention domain shifter, thus saving a considerable power. The second stage is a progressively sized cascade of inverter buffer.

The first stage is common-source configuration with active source-follower loads. The source-follower loads are employed to utilize the inductive nature of source-follower rout to achieve a resonance at higher frequencies to perform equalization for the sake of boosting high-frequency contents in the received signal. Equalization can be very beneficial when signal is received after traveling through long channels, which act as low-pass filters and result in a slewed reception at the receiver. This slow edge rate can affect the triggering of receiver, and data combinations in which a minimal state change is embedded within another dominant state can be missed by the receiver. The resistors (R1 and R2) at the gate of the source-follower loads can be configured to control the resonance peak and to employ equalization or to bypass it at all. These resistors are also used to

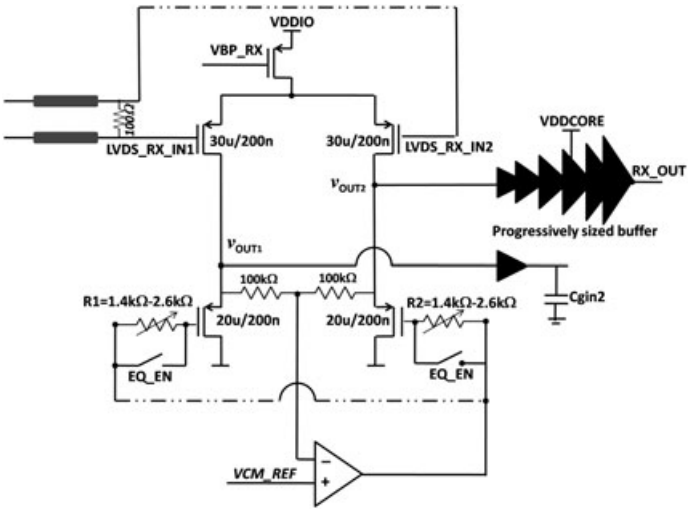

Figure 4. Receiver with active source-follower loads and progressively sized buffers.

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control the output common mode of the first stage of the receiver through the source-follower loads. The common mode is configured around 1 V by using a low-bandwidth common-mode feedback control circuit. Because the second stage consists of cascade of inverters operating at VDDCORE (1.8 V), the 1 V common mode from the first stage falls very close to the switching threshold of the first inverter; therefore, domain shifting is achieved without a domain shifter. The resonance due to the active inductive load also enables power reduction in the first stage because now, bias current reduction can be afforded as the required unity gain bandwidth is enhanced by the resonance.

The complex impedance of the source followers can be expressed, as shown in Eqns (3) and (4) along with pole and zero frequencies. To achieve a reasonable boost due to the resonance, the zero must lie exactly at the targeted frequency while the pole must be 5–6 times farther away from the zero. This necessitates for the fact that the gm of the loads are 5–6 greater than 1/R. To cater for variations in ω_Z with process, R1 and R2 are kept configurable between 1.4 and 2.6 kΩ in eight steps with a step resolution of 150 W; this caters for a ±30% error in the resonance. The calibration mechanism for R1 and R2 is based on an offline manual method by incrementally loading different values in the respective digital configuration flags through external field-programmable gate array (FPGA), which in turn tweaks an internal resistor bank.

$$Z(s) = \frac{1 + sRC_{GS}}{1 + \frac{sC_{GS}}{gm}} \tag{3}$$

$$\omega_P = \frac{gm}{C_{GS}} \& \omega_Z = \frac{1}{RC_{GS}}, \text{where } R1 = R2 = R \tag{4}$$

The progressive sizing in the six-inverter cascade buffer uses a factor of 1.5X based on the fact that it is designed to drive a load of 5 pF (assuming minimal loading from the driver itself), and its input capacitance is 0.5 pF ($F = \sqrt[6]{5p/0.5p - 1.5}$) [24]. The final output inverter exhibits an $R_{ON} < 50\,\Omega$, providing a time of 2τ for the settling of the buffered output for a load of 5 pF ($\tau_{OUT} = R_{ON6} * 5\,pF = 50 * 5\,pF = 250\,ps$).

2.3. *Built-in self-test*

The main functional blocks of the built-in self-test (BIST) are shown in Figure 5. The ring oscillator is implemented by using current-starved inverters, and the delay-locked loop delay line is composed of unit-sized inverters as delay elements. The ring oscillator inverter starvations can be controlled to control the clock frequency from 2 GHz down to 2 MHz. The ring oscillator also provides a

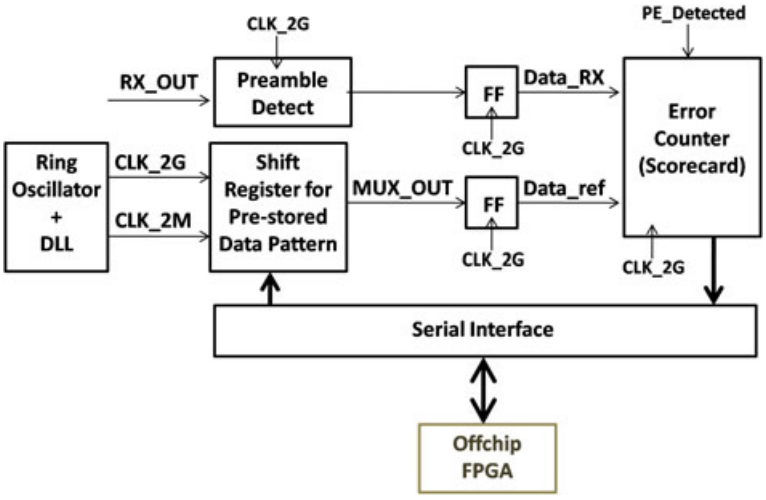

Figure 5. Built-in self-test logic along with the scorecard.

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divided-by-1024 clock CLK_2M used for interfacing with the external FPGA and running slower operations such as impedance calibration. The configuration register is loaded with a pre-determined data pattern along with a preamble by using the off-chip FPGA. Once the reset is de-asserted, if the chip is configured in TX mode, then it starts dispatching the data pattern at 2 GHz, embedding the preamble only at the start of the first packet. The loaded pattern is 24 bit, which can be cycled indefinitely. If the chip is configured in RX mode, then its BIST sits idle and pools for a preamble detection on the received data. If a preamble is detected, then the 24-bit error counter becomes enabled and compares received data with the corresponding prestored data bit. If any mismatch is detected, then error counter is incremented. Once the transmission and reception are carried out, the error counter value is readout by the external FPGA by using the 2-MHz clock at the serial interface.

3. MEASUREMENT RESULTS AND DISCUSSION

The LVDS transceiver was designed and fabricated by using 150-nm CMOS technology, occupying a small shared portion of a larger IC to save cost. The occupied area including the transmitter, receiver, and calibrator is $400 \times 400\,\mu m$ and is packaged in a QFN24 package. Figure 6 shows the measurement setup. Two packaged ICs are mounted on the test printed circuit board (PCB); one of the ICs assumes the role of a transmitter, while the other is enabled only as a receiver. The two devices under test can either be connected together through on-PCB 50W 4-in transmission line or through a 10-m CAT6 twisted pair cable to test under both short and long channel scenarios. The PCB is designed by using FR4 material, and the characteristic impedance of transmission lines is achieved by using predefined lengths and widths as striplines. The PCB is powered by two rechargeable batteries with on-board regulators for both 3.3 and 1.8 V supplies. Figure 7 shows the instrumentation setup. A random pattern, along with the required preamble, is loaded to the internal serial configuration register through Xilinx FPGA Virtex-5 at 10 MHz in both ICs along with their corresponding internal flags.

Figure 8 shows eye diagrams and jitter at zero crossing when a pseudorandom pattern is transmitted by DUT1 at 2 Gbps for three different scenarios: (1) 4-in short transmission line, no pre-emphasis, no equalization, and slew rate control active; 2) 10-m long transmission line, no pre-emphasis, no equalization, and no slew rate control; and 3) 10-m long transmission line, pre-emphasis active, no equalization, and no slew rate control. The transmitted stream is received at the far end by Rohde and Schwarz spectrum analyzer triggered by the deskewed clock of DUT2. The vertical and horizontal openings of the eye diagram are highlighted on the eye diagrams in Figure 8.

The effectiveness of pre-emphasis and equalization for longer channels can be seen from the eye diagrams in the preceding texts. Without the pre-emphasis and equalization, the received signal at the far end does not satisfy the minimum swing requirements (250 mV) for the targeted data rate and therefore the eye opening is smaller than the required qualifications. Pre-emphasis by boosting high-frequency components at the transmitter does draw a certain amount of impulsive current from the supply. At the same time, pre-emphasis also risks exciting the impedance discontinuities across the channel to reflect the boosted high-frequency contents of the signal.

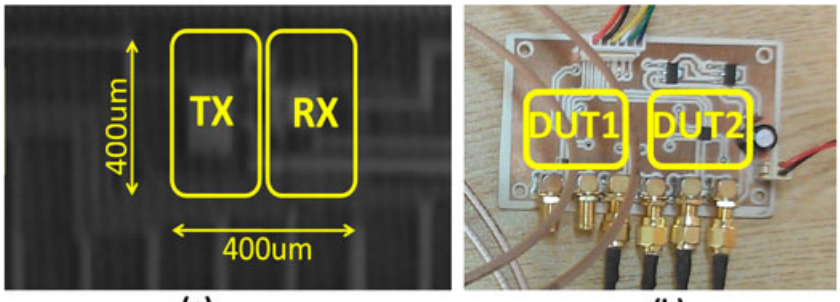

Figure 6. Microphotograph of the transceiver and test printed circuit board.

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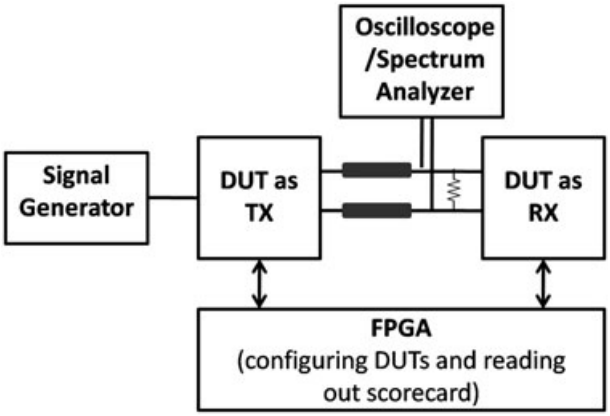

Figure 7. Measurement setup.

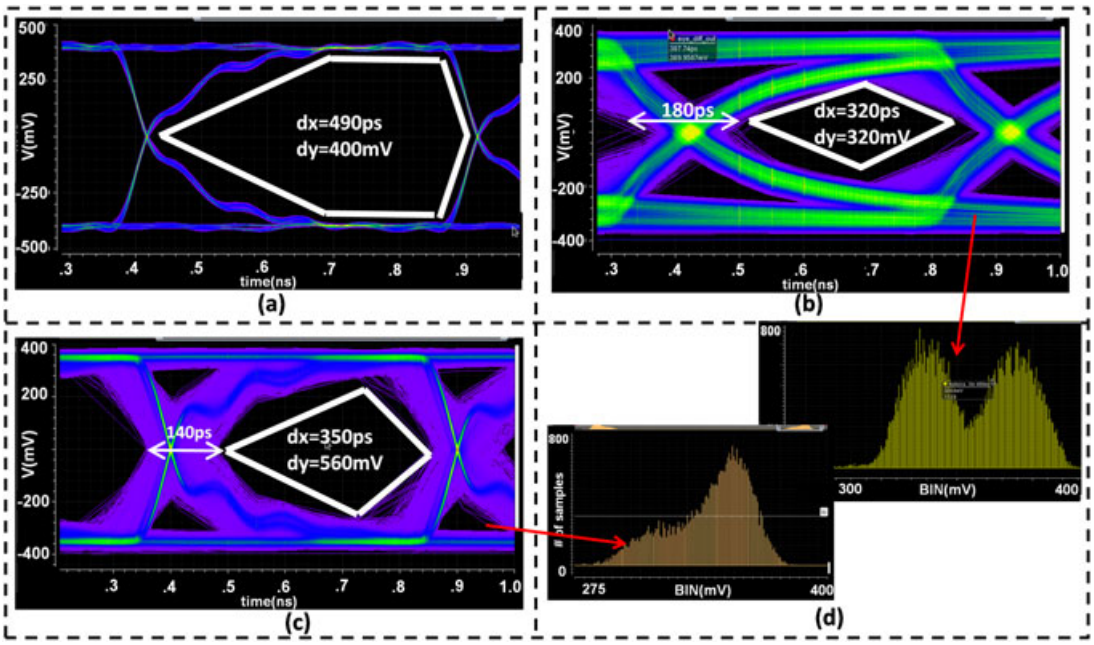

Figure 8. Eye diagram at the far end; (a) 4-in microstrip at 2 GHz with slew rate control, (b) 10-m twisted pair CAT6 cable without pre-emphasis, (c) 10-m twisted pair CAT6 cable with pre-emphasis, (d) histogram of the voltage levels in the eye diagrams. It can be seen in Figure 8c's histogram that many voltage values fall below the minimum required differential voltage swing of 250 mV.

The receiver in standalone configuration is tested by applying a periodic 2-GHz, 400-mV differential signal at 1.2-V common mode with different edge rates, with and without equalization. Figure 9 shows the final digital output of the receiver, which fails to regenerate the signal in case II where edge rate is slow, not letting differential signal exceed 250 mV, and the receiver is operating without equalization. For the same type of input applied with equalization active, we can see in case III that the data are properly received. The effect of equalization, when compared with pre-emphasis from the power consumption perspective, is confined within the receiver, and it does not draw considerable current from the power supply as well. Case IV shows the effect of the receiver's first-stage common-mode output voltage on duty cycle distortion. It can be seen that for 10 different samples, the duty cycle distortion is less than 5%, therefore implying that the common-mode reference generation employed in receiver design is tracking the process variations effectively.

When the BIST is employed for testing, a pseudo random pattern is loaded in DUT1 and DUT2. The ring oscillators for both DUTs are deskewed so that their phase difference is minimized by using

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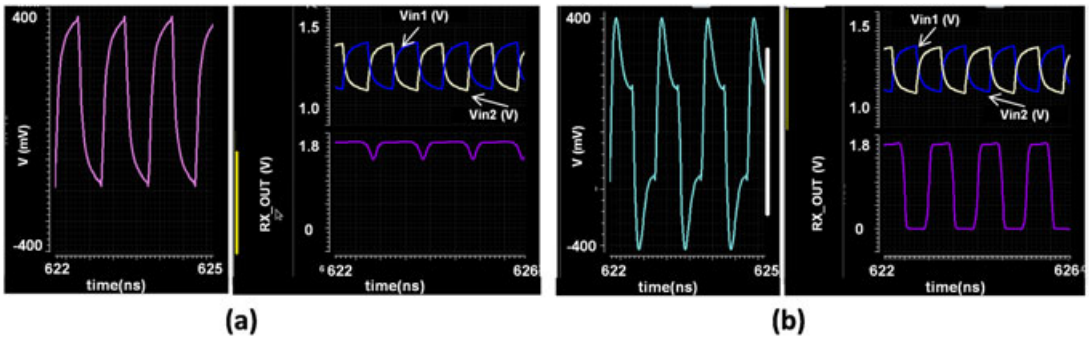

Figure 9. Receiver's first-stage buffered output when its input is arriving through a 10-m twisted pair cable, which is low-pass shaping the input. (a) Without equalization, the receiver is unable to toggle. (b) Due to the high-frequency boost because of equalization, the receiver toggles with minimum duty cycle distortion.

internal delay lines. Figure 10 shows modified bathtub curves with termination impedance at the near end on the x-axis while bit error rate (BER) on the y-axis. The termination impedance is tweaked manually by loading a particular impedance code to the configuration register to induce a ±80% error. To achieve impedance matching with minimum error, calibration is performed before dispatching the data. Same data pattern is dispatched multiple times for different impedance settings, and the scorecard readings are updated if an error is detected. At the end of the test, the error counter is readout through the serial interface. It can be seen in Figure 10 that after a ±60% impedance mismatch, the ISI for a 1-m transmission line at 2 GHz suffers from critically high BER, making the received data undecipherable. A ±60% impedance mismatch is possible due to a ±60%

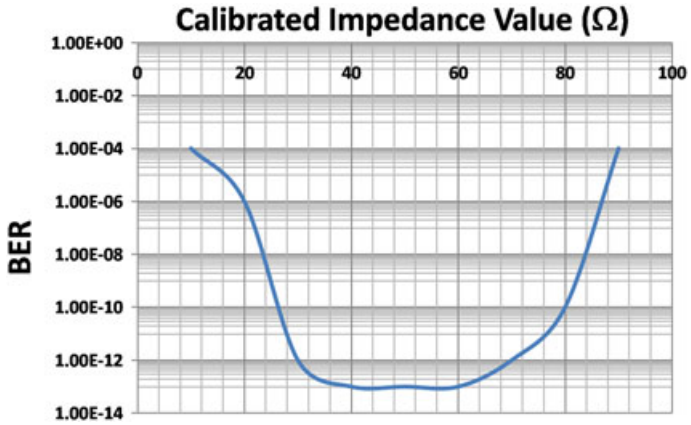

Figure 10. Bit error rate versus the mismatch in termination impedance at the near end for 1-m transmission line at 2 GHz.

Table I. Comparison with state-of-the-art.

Design/year	Technology	Type	Supply voltage (V)	Area (mm^2)	Data rate (DR)	Power (P) (mW)	FoM = P/DR J/bit
[1] 2005	350-nm CMOS	TX	3.3	–	1.4 Gbps	23	16.4×10^{-12}
[2] 2001	350-nm CMOS	TX + RX	3.3	0.256	600 Mbps	100	167×10^{-12}
[3] 2012	350-µm CMOS	TX + RX	3.3	0.15	1.4 Gbps	25	17.8×10^{-12}
[4] 2014	130-nm CMOS	RX	–	7.24	11.2 Gbps	78	6.9×10^{-12}
[5] 2006	SiGe BiCMOS	TX	3.3	–	1 Gbps	21	21×10^{-12}
[6] 2010	SiGe BiCMOS	TX	2.5	–	10 Gbps	15.6	1.56×10^{-12}
[7] 2009	180-nm CMOS	TX	1.8	0.067	2.5 Gbps	8.5	3.4×10^{-12}
This work	150-nm CMOS	TX + RX	3.3	0.16	2 Gbps	20	10×10^{-12}

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spread in the gm of the source-follower load of the transmitter due to PVT variations, therefore establishing the necessity of calibration.

The presented design is compared with state-of-the-art LVDS transceivers available in the literature in Table I. It can be observed that this particular design achieves a reasonable reduction in overall power consumption for the targeted data rate owing to two facts: (1) Transmitter employs a hybrid topology, combining advantages of current-mode and voltage-mode operations, and (2) combining amplification and domain-shifting within the first stage of the receiver removes the need of an extra stage.

4. CONCLUSION

A highly configurable LVDS transceiver is presented. The configurability is embedded in the form of functionalities like pre-emphasis, equalization, and slew rate control, which can help the transceiver to operate either for smaller differential channels (a few inches of striplines) or for longer channels (10 m of twisted pair cables) at the same data rate of 2 Gbps. The measurement results of the hybrid-mode transmitter, achieving a high-impedance current-mode signal dispatch with impedance matching, demonstrated a feasible operation both for shorter and longer channels with 30 and 180 ps of total jitter, respectively. The pre-emphasis in the transmitter improved the eye opening and jitter for a 10-m twisted pair CAT6 cable. The slew rate control becomes useful for shorter channels, where it pre-attenuates the high-frequency contents of the transmitted signal, minimizing the possibility of reflection. The compact low-power receiver demonstrated a 5-dB boost at the center frequency of resonance due to equalization along with a low-power profile due to removal of a separate domain shifter. The built-in impedance calibrator minimized the spread in the on-die termination at the near end provided by the transmitter. The transceiver is designed and fabricated in 150-nm CMOS, sharing the space with a larger die, occupying an area of $400 \times 400\,\mu m$. The transceiver consumes a total power of 20.5 mW at 2 Gbps, that is, ~10 pJ/bit of energy consumption.

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