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Equalization and pre-emphasis based LVDS transceiver

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Abstract This work presents an area-efficient, low-power, high data rate low voltage differential signal (LVDS) transmitter and receiver with signal quality enhancing techniques. The proposed common mode feedback scheme significantly reduces the size of the LVDS transmitter by eliminating the use of area consuming passive resistor and capacitor used for close loop stability compensation. A preemphasis technique has been introduced to enhance the transmitter output's signal quality without significantly increasing the power draw. On the receiver part, an equalization technique has also been introduced to further enhance signal quality, increases data rate and improved jitter with relatively low power consumption. The LVDS transmitter consumes 5.4 mA of current while driving an external 100 ohm resistor with an output voltage swing of 440 mV. The chip consumes an area of 0.044 mm^2. This LVDS receiver has an input common mode range from 0.1 to 1.6 V. It consumes 34 mW of power with a maximum data rate of 2 Gbps. It consumes an area of 0.147 mm^2 a jitter of 11.74 ps rms. A test chip is implemented using 0.18 μm CMOS process.

Keywords Equalization · Pre-emphasis · LVDS · Transmitter · Receiver

1 Introduction

LVDS has been widely used in the industry. However, as demand for data rate continues to increase, new problems start to come out such as degradation of signal quality. This problem is primarily caused by frequency-dependent losses in a transmission line: skin effect and dielectric loss. As frequency increases, current density in the transmission line tends to concentrate near the surface, increasing the effective resistance. As a results, the frequency -dependent losses greatly limit the bandwidth of the transmission path.

Several research papers pertaining to expanding the limitations of LVDS have been published. The efforts for these researches are focused on improving the performance of the LVDS transmitter and receiver in terms of higher data rate, decreasing power consumption, and improving the signal integrity. Literature [1] designed a transmitter and receiver pair that is compatible with the LVDS standard and can reach at Gb/s per pin data rate. However, it consumes large power and requires an area consuming resistor and capacitor for close loop compensation. In order to alleviate this issue, literature [2] focused on low power LVDS drivers that can operate in lower voltage supply relative on other work with the same process though jitter performance is poor especially at higher data rate. Another design was introduced in literature [3] which focused on enhancing signal quality by controlling the slew rate at the output. However an area consuming resistor and capacitor compensation is still needed for [3]. A pre emphasis scheme for an LVDS transmitter is presented in [5] presenting a scheme that boost the LVDS driver strength at every first transiting bit but significantly increasing the dynamic power consumption of the LVDS driver.

This work focuses on enhancing signal integrity while operating at higher data rate and lower power consumption. The preemphasis scheme improves signal quality without significantly increasing the dynamic power consumption. A method of reducing the area consumption of the LVDS driver by eliminating the passive compensations is also introduced. The proposed LVDS receiver is implemented

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with an enhanced signal quality and a lower power consumption. This paper is organized as follows: The architecture of the proposed LVDS transmitter and receiver are discussed in Sect. 2. Circuit implementation is addressed in Sect. 3. Section 4 presents experimental results. Finally, conclusions are given in Sect. 5.

2 Architecture description

Figure 1 presents the complete system block diagram of the proposed LVDS transmitter and receiver. The transmitter is composed of two-stage LVDS transmitter block, pre-emphasis control block with pre-driver and transmitter strength control block. The receiver is constituted by a rail to rail pre receiver block, a two-stage equalizer and the LVDS receiver.

Signals $P_{ctl}[3:0]$, $E_{ctl1}[2:0]$ and $E_{ctl2}[2:0]$ are control signals coming from a digital control block. These are the controls used for pre-emphasis and equalization for the transmitter and receiver respectively. A digital control block sets the appropriate pre-emphasis and equalizer setting depending on the bit error rate (BER) values the controller was able to calculate during calibration scheme. This work is only focused on the analog front end.

2.1 Pre-emphasis

The proposed pre-emphasis scheme is shown in Fig. 2. The pre-emphasis scheme of this work operates like a two tapped finite response filter (FIR). Instead of boosting the first bit of a data, the proposed preemphasis concept only boost the slew_rate of every transitioning signal. The proposed preemphasis works by delaying the data by a fixed small interval and comparing the delayed data to the original data and an XOR function combines them to produce a finite pulse.

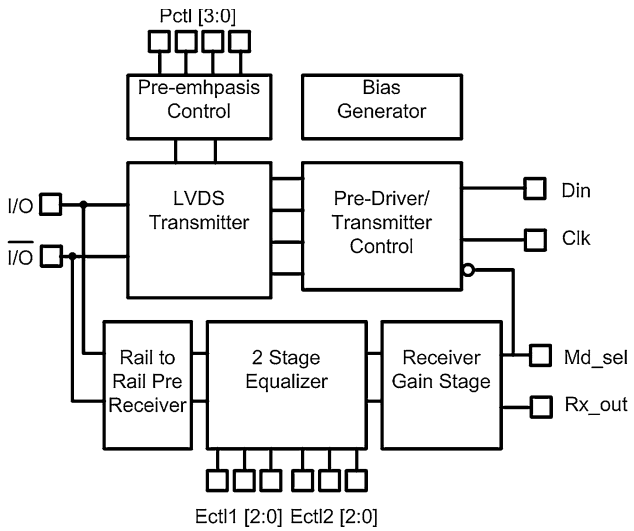

Fig. 1 Proposed transmitter and receiver chip

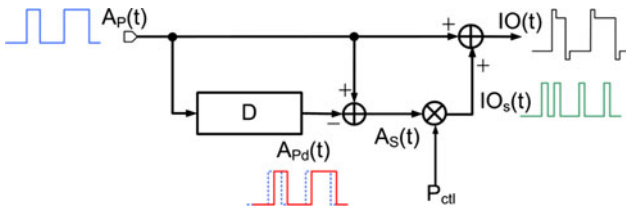

Fig. 2 Proposed pre-emphasis operation

Data $A_p(t)$ is delayed by a duration equal to "D" producing a signal A(t) where:

$$A_{pd}(t) = A_p(t - D) \tag{1}$$

Signal $A_{pd}(t)$ is then subtracted from signal $A_p(t)$ to produce the signal $A_s(t)$ or equal to:

$$A_s(t) = A_p(t) - A_p(t - D) \tag{2}$$

Signal P_{ctl} represents a digitally programmable pre-emphasis drive strength. The value for P_{ctl} depends on the demand needed for the system to equalize a particular transmission line frequency response. Signal P_{ctl} is multiplied to signal $A_s(t)$ producing signal $IO_s(t)$ where:

$$IO_s(t) = P_{ctl}[A_p(t) - A_p(t - D)] \tag{3}$$

$IO_s(t)$ is then added to $A_p(t)$ producing an edge boosted signal represented by IO(t) where:

$$IO(t) = A_p(t) + P_{ctl}[A_p(t) - A_p(t - D)] \tag{4}$$

The above expression shows that when $A_p(t)$ is equal to $A_p(t - D)$, then IO(t) will just be equal to $A_p(t)$. Otherwise, IO(t) will become a boosted signal from $A_p(t)$. $[A_p(t)–A_p(t - D)]$ will only be non-zero during when $A_p(t)$ make transitions. Thus, the expression illustrates that IO(t) will be boosted by a factor "P_{ctl}" during transitions of $A_p(t)$.

2.2 Active peaking

Active peaking is a method of extending the bandwidth of a circuit using active devices such as CMOS transistors instead of using passive inductive peaking through inductors. Bandwidth extension was done by adding zero to the system.

An addition of a stage in a circuit topology will limit the bandwidth capability of such system since additional pole is infused. For the proposed receiver topology, in order to counteract the undesired effect of an additional stage, active peaking is employed. The impedance of an active inductor shown in Fig. 3 can generally be represented mathematically as in [4]:

$$Z_n(s) = \frac{S\frac{L_s}{R_s} + 1}{S^2(L_s C_{out}) + S(\mathrm{K}+1)(L_s R_s) + 1} \quad (5)$$

where:

$$R_s = \frac{G + g_{m2}}{g_{m1} g_{m2}}$$

$$L_s = \frac{C_{gtotal}}{g_{m1} g_{m2}}$$

$$\mathrm{K} = \frac{G + g_{m1}}{G + g_{m2}} \frac{C_{m2gs}}{C_{out}}$$

C_{out} is the total parasitic capacitance at the drain node of M1 or at the gate of M2 in Fig. 3. Rs expression is the equivalent inductor resistance which is inversely proportional to the product of the two devices transconductances namely g_{m1} and g_{m2}. It is directly proportional to the sum of the total second order transconductances denoted as G. Ls on the other hand is the equivalent inductance of the active inductor which is inversely proportional to the product of the two transconductances and directly proportional to the total parasitic capacitance of the active inductor circuitry. Given the parameters Rs and Ls in Eq. (5), the positions of the pole and zero can be controlled by adjusting the aspect ratios of the two devices in an active inductor. However, to realize adaptive equalization, changing the ratios of transistors is difficult. Instead, zero position can be changed by adding a significantly larger capacitor at the M1 gate to control the C_{gtotal} value.

2.3 Zero equalization scheme

Due to the low pass properties of the transmission line, higher frequency components of a signal are degraded. The proposed equalization scheme uses two-tap equalization in order to effectively equalize a lossy line. The proposed equalization scheme on this work provides more flexibility in equalizing transmission lines of different frequency response characteristics as compared to a one tap equalizer.

It is shown in Fig. 4 a simplified explanation of the equalization scheme this work proposes. The upper portion of the figure is the frequency response for the equalizer stage while the bottom portion is the response for the transmission path. For example, if a given transmission path has a loss such as the shaded area labeled as "Loss A", the equalizer can move the zero to a lower frequency until it can produce a peaking having an area almost equal to the area of "Loss A". Thus for such cases, one tap equalization can easily compensate for such loss. However, if a given transmission path has a loss such as "Loss A + Loss B", single tap equalization may not be enough to compensate for the loss. For this work, a second zero is introduced to the system in order to achieve a higher amount of peaking that can compensate for a loss such as "Loss A + Loss B" as given above. A combination of the zero's location in the frequency domain can provide more equalization options for different transmission path frequency response characteristics. Accordingly, the more zeros introduced and being controlled in a transmission path, the more efficient and flexible the equalization scheme will be. However, adding more stages translate to having more power consumption and more area. Thus it is a trade-off that has to be well balanced.

Adjusting the zeroes also counters the phase shift effect. As a zero increase back the magnitude at 20 dB per decade, it also shifts the phase at positive 45° at the zero frequency location until it reaches 90° at frequency 10 times the zero frequency. It should be noted that these effects are the complete opposite of what a pole does to a signal in terms of magnitude and phase. Thus, this scheme also equalizes not only amplitude or signal transition time, but also the timing jitter caused by the phase shift of the high frequency components of a signal.

2.4 Quality factor

The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. For spiral inductors, the quality factor of these inductors is independent of the voltage/current of the inductors. This property, however,

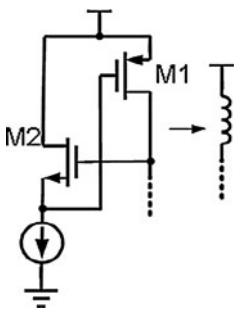

Fig. 3 Active inductor circuit

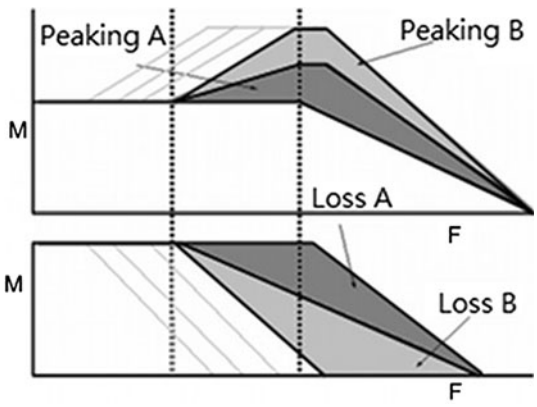

Fig. 4 Receiver equalization concept

does not hold for active inductors as the inductance of these inductors depends upon the transconductances of the devices constituting the active inductors and the load capacitance.

The quality factor of the active inductor affects the amount of peaking of the frequency response. Thus it directly affects the equalization performance of the LVDS receiver. The higher the Q factor, the higher is the peaking. For the given active inductor, the Q factor can be boosted by lowering "Rs" parameter in Eq. (5). To do this, the short channel trans- conductance or g_{ds} of M2 in Fig. 4 can be lowered by applying longer lengths or the body trans-conductance can be reduced by special process technique. However in this work, Q factor was improved by directly increasing g_{m1} and g_{m2}.

3 Circuit implementation

3.1 Proposed LVDS transmitter with pre-emphasis

Figure 5(a) depicts a second stage transmitter that is used in order to boost the driver strength during which the signal is transitioning. The period of the second-stage input pulse is just enough to cover the duration wherein the signal is transitioning as shown in Fig. 5(b). Unlike in the pre-emphasis transmitter in [5] wherein it boost the driver strength at every first bit after transition, this work only boost the signal at every transitioning period, thus the time

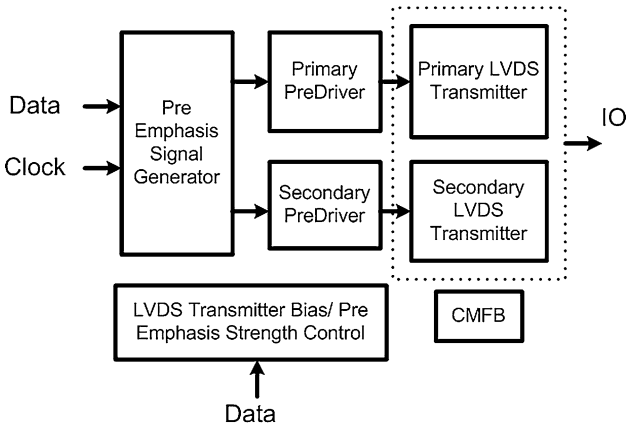

Fig. 6 Proposed LVDS transmitter system block

duration at which the secondary transmitter is providing extra current in this work is lesser than in [5]. Such scheme reduces the dynamic power consumption of the transmitter of this work relative to [5].

The simplified block diagram of the proposed LVDS transmitter is shown on Fig. 6. It consists 7 blocks: two LVDS drivers, two pre-drivers, pre-emphasis signal generator, CMFB and the bias and current control. Aside from the main driver, the proposed LVDS transmitter consists of a secondary driver that provides additional drive strength to the primary driver in order to counter act the losses of a signal during high frequency occurrence. The device sizes on both primary and secondary drivers are large since they need to carry as much as 4 mA of static current when

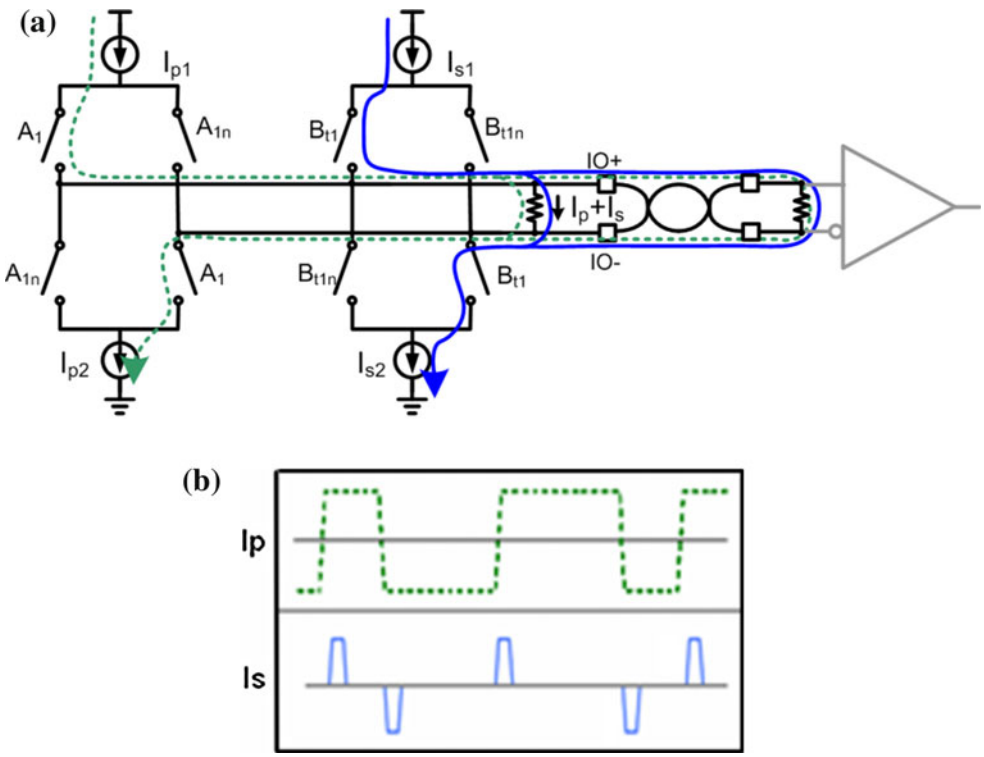

Fig. 5 **a** Simplified schematic of the proposed LVDS driver circuitry, **b** ideal current waveforms for the proposed LVDS driver

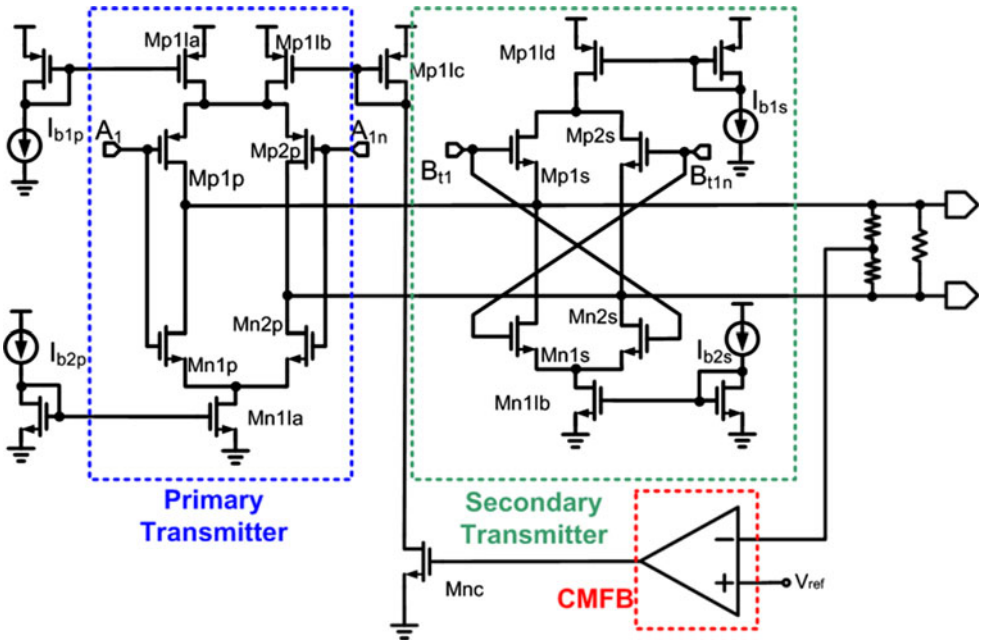

Fig. 7 Primary and secondary LVDS transmitter with CMFB

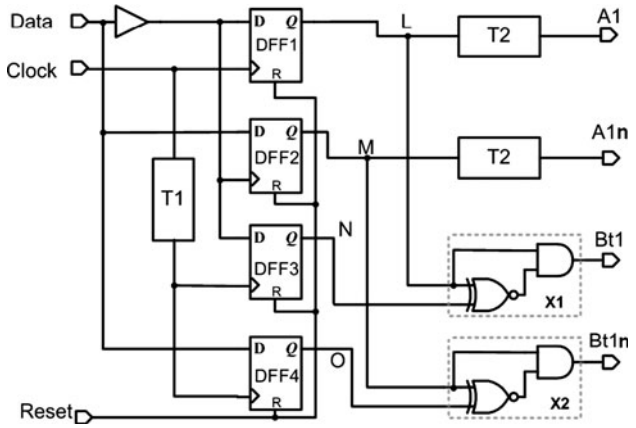

Fig. 8 Pre-emphasis signal generator

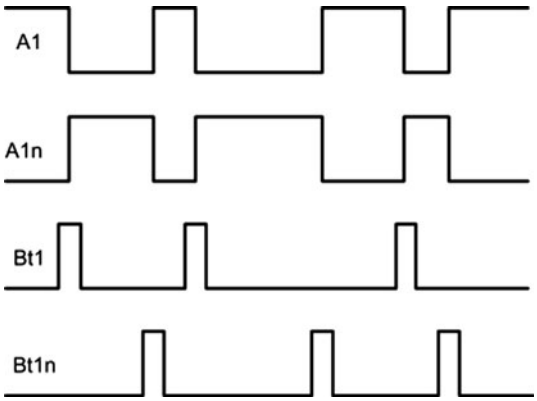

Fig. 9 Signal waveform signal generator

Table 1 Truth Table for Pre-Emphasis

A1	A1n	Bt1	Bt1n
↑	↓	0	1
↓	↑	1	0

driving on these devices that may lead to poor signal driving. Thus the primary and secondary pre-drivers are needed to enable the pre-emphasis signal generator and single ended to differential converter block to effectively drive the highly capacitive primary and secondary driver devices.

The proposed LVDS transmitter driver schematic including the CMFB is shown in Fig. 7. Transistors Mp1p, Mp2p, Mn1p, Mn2p, Mp1Ia. Mp1Ib and Mn1Ia constitute the primary LVDS transmitter while Mp1Id, Mp1 s,

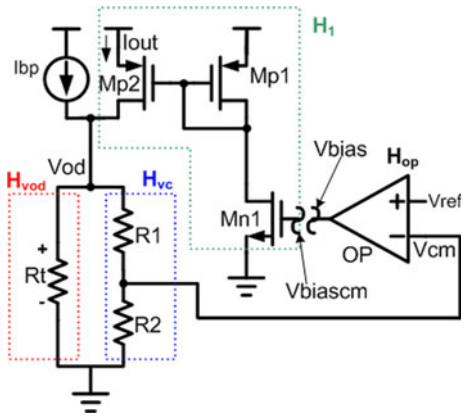

Fig. 10 CMFB loop

Mp2 s, Mn1 s, Mn2 s and Mn1Ib constitute the secondary transmitter for pre-emphasis. Input signals A_1 and A_{n1} are differential, full swing, large signal data while inputs B_{t1} and B_{t1n} are pre-emphasis pulses that drives the secondary transmitter. Transistors Mp1p, Mp2p, Mn1p, Mn2p in the primary driver as well as transistors Mp1 s, Mp2 s, Mn1 s and Mn2 s in the secondary driver act as switches that stirs the current direction along the transmission line depending on the data being transmitted. Transistors Mp1Ia, Mp1Ib, Mn1Ia, Mp1Id and Mn1Ib are current sources and sinks for the primary and secondary drivers.

3.2 Pre-emphasis signal generator and single-ended to differential converter

In order to generate the correct pre-emphasis control signal for the secondary LVDS driver, the pre-emphasis signal generator is required. The schematic of such block is shown in Fig. 8. Aside from providing appropriate pre-emphasis signal, the signal generator block is also responsible for the conversion of a digital single ended data into a digital differential data. The data is being sampled by the clock through two sets of D flip-flop pairs. The first pair which consist of DFF1 and DFF2 produce the differential signals A_1 and A_{1n} for the primary LVDS transmitter while the second set consisting of DFF3 and DFF4 together with the X1 and X2 blocks, generate the pre-emphasis signals for the secondary LVDS transmitter. Signals N and O are delayed from signals L and M through the delay element T1. The XNOR gate in blocks X1 and X2 produce a pulse corresponding to the delays of signals L to N and M to O, respectively. The AND gates of blocks X1 and X2 passes the pulse to the output depending on which signal is transitioning. T1 and T2 delay elements are implemented by simple inverter delays.

Table 1 lists the truth table and Fig. 9 shows the signal waveform, respectively. Signals B_{t1} and B_{t1n} are narrow signals around 250 ps which is just enough to fit the transition time of A_1 and A_{1n}. Additionally, the pre-emphasis signals must also fall exactly at the point of transition of the primary signals. Thus timing between A_1 and A_{1n}, B_{t1} and B_{t1n}, as well as A_1–A_{1n} and B_{t1}–B_{t1n} is very critical especially since the circuit operates at a high frequency. The structure operates such that the two signals in one pair are triggered at the same time by one clock through the D flip-flop. Thus the crossing point of the two signals is typically at half of V_{DD}. The structure also makes the variation in the pulse duration of the B_{t1} and B_{t1n} pulses dependent only on the variation of T1 and not on the other gates. Thus such structure provides proper synchronization for the pre-driver signals.

3.3 Common mode feedback

Figure 10 illustrates the simplified structure of CMFB circuitry shown in Fig. 8. Resistors R_1 and R_2 obtain the average of the two differential signals and feed it to the CMFB error amplifier wherein the latter compares it with a voltage reference signal. Depending on the amount of change in the signal average, the error amplifier adjusts the voltage bias on the gate terminal of NMOS device at its output that supplies a portion of the current to the primary LVDS transmitter. The CMFB amplifier is allowed to control only a portion of the primary driver's current instead of the whole current in order to reduce the feedback gain. As discussed earlier, on this work, the RC stability compensation is eliminated by reducing the feedback gain just well enough to stabilize the close loop system. Doing such method also decreases the loop bandwidth in order to make the loop unaffected by the LVDS signal that has a higher operating frequency.

The loop is composed of stages $H_1(s)$, $H_{vod}(s)$, $H_{vc}(s)$ and $H_{op}(s)$. $H_1(s)$ is the transfer function for the current mirror that is constituted by Mn1, Mp1 and Mp2. $H_1(s)$ has V_{biascm} as the input and I_{out} as the output. $H_{vod}(s)$ is the transfer function for the resistor R_t where its output is V_{cm} signal with input as $I_{out} + I_{bp}$ since R_t is much lesser than $R_1 + R_2$. $H_{vod}(s)$ is simply the resistance R_t. $H_{vc}(s)$ is the transfer function for the resistors R_1 and

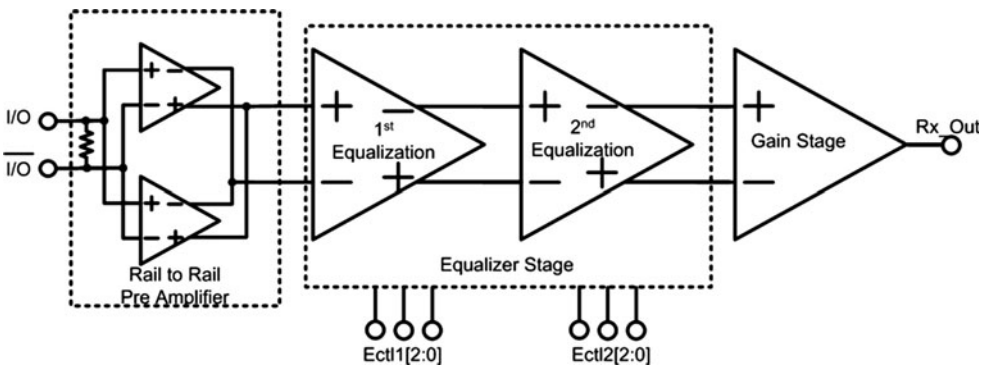

Fig. 11 LVDS receiver system block

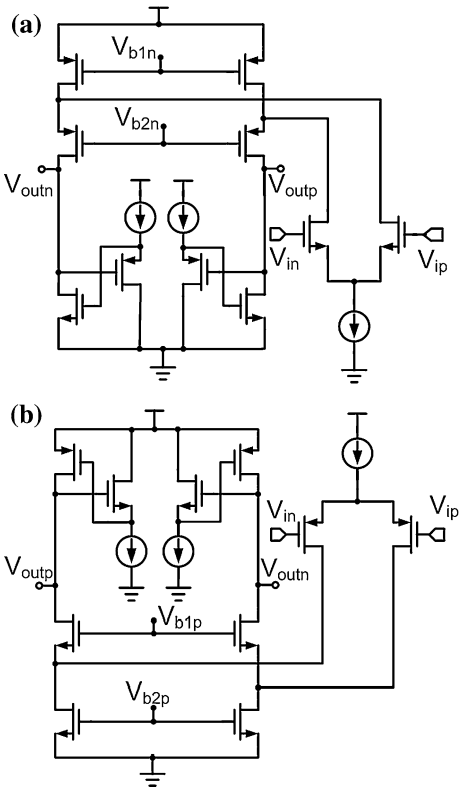

Fig. 12 Pre-amplifier composed of **a** NMOS input and **b** PMOS input

R_2. Input of $H_{vc}(s)$ is signal V_{od} while the output is the signal V_{cm}. $H_{op}(s)$ is the transfer function of the OP Amp.

In order to derive the loop transfer function of the CMFB system, the loop must be cut into two nodes namely Vbias and Vbiascm. Transfer function must then be derived in terms of output over the input. Firstly, HA_O is the DC gain of the operation$_{op}$ is given as:

$$H_{op} = \frac{A_o}{\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)} = \frac{V_{bias}}{\Delta V_{ref}} \tag{6}$$

al amplifier while ω_{p1} and ω_{p2} are the poles located at the output and the input of the OP Amp, respectively. ΔVref is the small signal difference between Vcm and Vref.

H_1 is the transfer function for the current mirror and source being controlled by the CMFB amplifier. It is simplified as:

$$H_1 = \frac{I_{out}}{V_{biascm}} = G_{mH1} \tag{7}$$

H_{vc} is the transfer function for the common mode detector block that is made up by R_1 and R_2. The transfer function is given as:

$$H_{vc} = \frac{\Delta V_{ref}}{V_{od}} = \frac{R_2}{R_1+R_2} = \frac{1}{2} \tag{8}$$

ΔV_{ref} is the small signal V_{ref} or the small signal average derived by the voltage divider resistors. R_1 and R_2 are

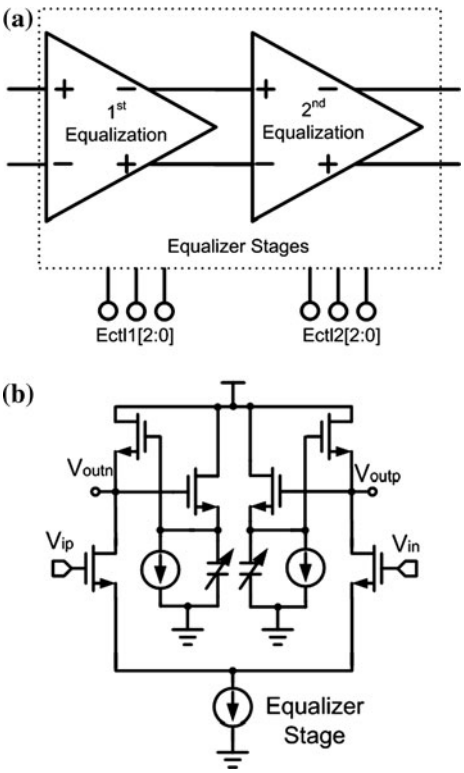

Fig. 13 **a** Double tapped equalizer stage, **b** equalizer circuit

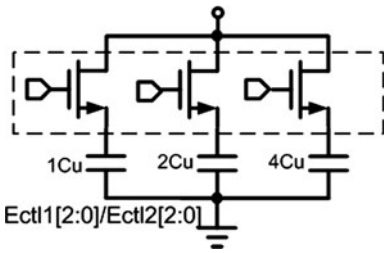

Fig. 14 Binary weighted capacitor array

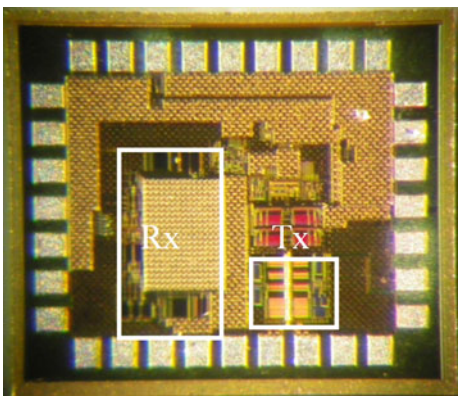

Fig. 15 Chip microphotograph

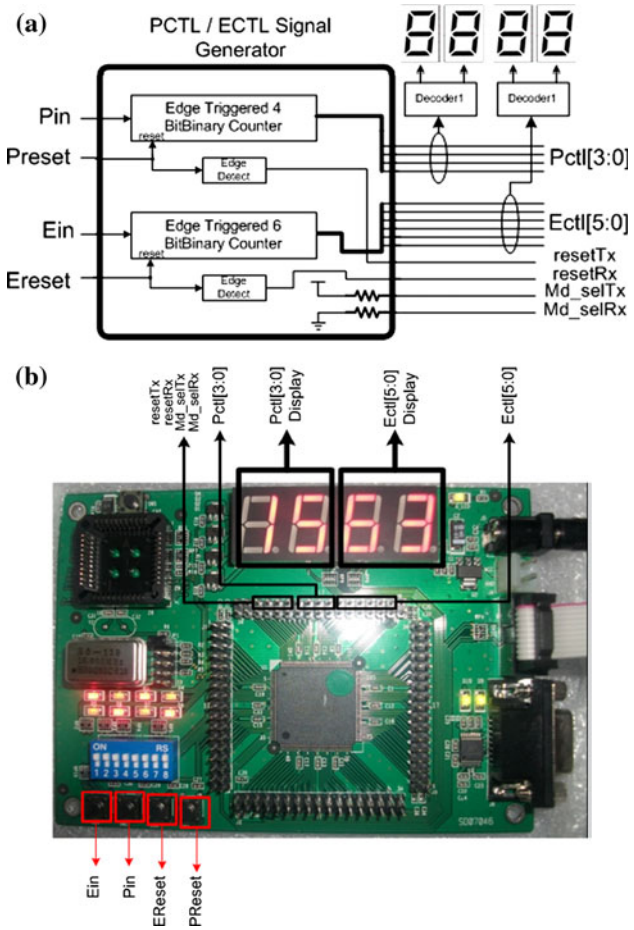

Fig. 16 FPGA for producing Pctl and Ectl signal **a** functional block, **b** actual set up

equal thus the transfer function can further be simplified as half.

H_{vod} is the transfer function for the current to differential voltage converter or simply resistor R_t. It is given as:

$$H_{vod} = \frac{V_{od}}{I_{Total}} = \frac{V_{od}}{I_{bp} + I_{out}} = R_t \tag{9}$$

I_{Total} is the total current that passes through R_t which is equal to $I_{bp} + I_{out}$. The stability in the loop is achieved by the ratio of I_{out} to I_{bp}. The parameter is introduced as:

$$A_r = \frac{I_{out}}{I_{bp}} \tag{10}$$

Thus;

$$H_{vod} = \frac{V_{od}}{I_{out}} = R_t\left(1 + \frac{1}{A_r}\right) \tag{11}$$

In order to express the loop transfer function, expression. V_{bias}/V_{biascm} must be derived where:

$$\frac{V_{bias}}{V_{biascm}} = \frac{A_o}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)} \times (G_{mH1}) \times \frac{1}{2} \times R_t \times \left(1 + \frac{1}{A_r}\right) \tag{12}$$

To simplify the equation, parameter G_v is introduced as:

$$G_v = A_0 \times (G_{mH1}) \times \frac{1}{2} \times R_t \tag{13}$$

Thus the loop transfer function is derived as:

$$\frac{V_{bias}}{V_{biascm}} = \frac{G_v}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)} \times \left(1 + \frac{1}{A_r}\right) \tag{14}$$

As can be seen on the equation, the loop transfer function is given as a second order function. For simplicity in the analysis, let the function be a first order expression by assuming ω_{p2} to be much greater than ω_{p1}. Thus, the loop transfer function can further be simplified as:

$$\frac{V_{bias}}{V_{biascm}}(s) = \frac{G_v}{\left(1 + \frac{s}{w_{p1}}\right)} \times \left(1 + \frac{1}{A_r}\right) \tag{15}$$

From the simplified loop expression, the loop gain can be seen to be dependent directly on the DC gain G_v and at the same time on the term $(1 + 1/A_r)$. The expression can still be further simplified thus deriving:

$$\frac{V_{bias}}{V_{biascm}}(s) = \frac{G_v \cdot w_{p1}}{(w_{p1} + s)} \times \left(1 + \frac{1}{A_r}\right) \tag{16}$$

$G_v \cdot \omega_{p1}$ is the gain-bandwidth product of the feedback system. Thus from the above equation, the gain-bandwidth product can now be derived by equating V_{bias}/V_{biascm} to 1 and substituting $G_v \cdot \omega_{p1}$ to s. Thus the gain-bandwidth product is expressed as:

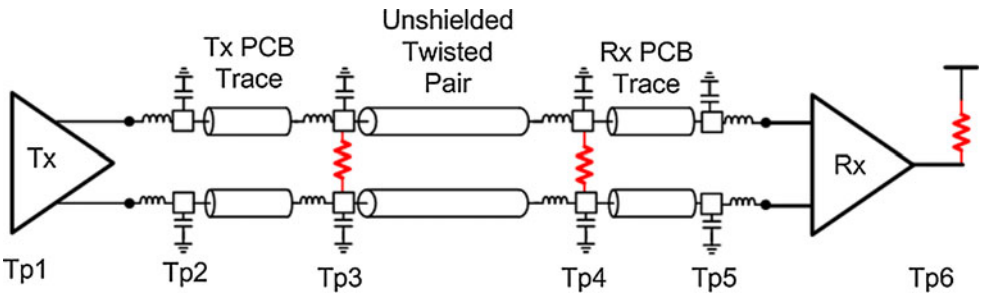

Fig. 17 Actual chip measurement set up

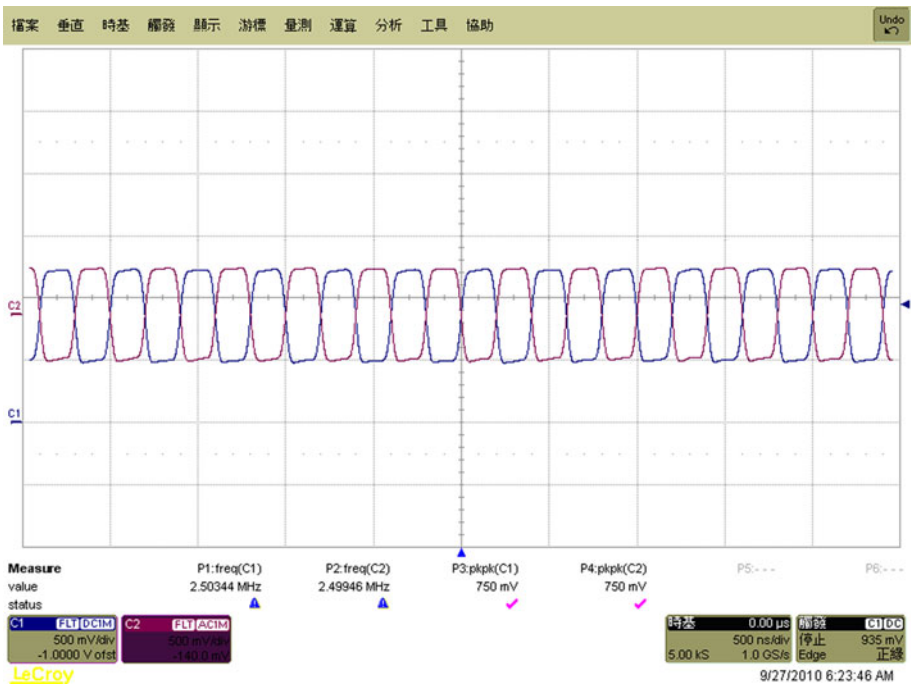

Fig. 18 LVDS signal with stable common mode level

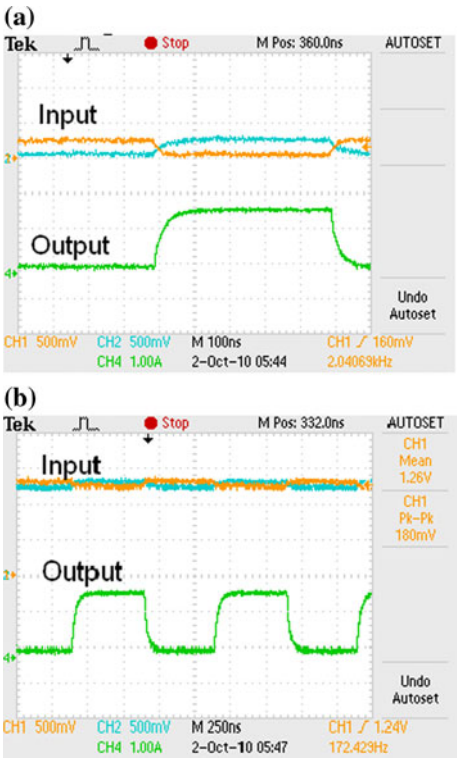

Fig. 19 LVDS receiver rail to rail test. **a** $V_{cm} = 0.1$ V and **b** $V_{cm} = 1.6$ V

$$1 = \frac{G_v \cdot w_{p1}}{(w_{p1} + G_v \cdot w_{p1})} \times \left(1 + \frac{1}{A_r}\right) \tag{17}$$

Then it can be simplified that

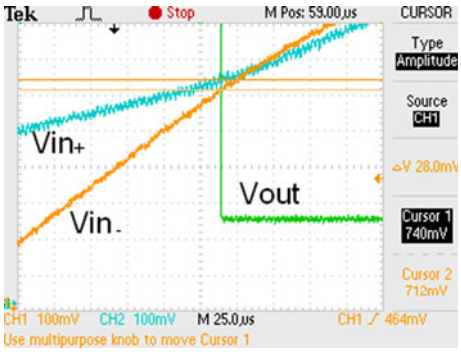

Fig. 20 LVDS receiver offset test

$$G_v \cdot w_{p1} = A_r \times w_{p1} \tag{18}$$

From the above expression, the gain-bandwidth product is derived to be directly proportional to the current ratio A_r. Thus this shows that the current ratio is equal to the dc loop gain of the CMFB system. Increasing I_{out} will increase the gain and moving the gain-bandwidth frequency further from the origin. Otherwise, decreasing I_{out} will decrease the current ratio which eventually decreases the gain thus moving the gain-bandwidth frequency towards the origin. This relationship is utilized by this work in order to properly stabilize the close loop system without using passive resistor and capacitor compensation. By properly selecting the current ratio, a stabilized close loop system was achieved.

3.4 Proposed LVDS receiver

The receiver can accept low voltage differential signal as low as 100 mVp signal (LVDS standard) with an input common range of 0–1.65 V and amplify it to a rail to rail digital signal that is eventually fed to a SerDes block of a digital core.

For this work, the LVDS receiver is composed of 3 stages as can be seen on Fig. 11. The pre-amplifier stage enables the whole receiver to accept LVDS signals with common modes from 0.1 to 1.6 V as specified in the LVDS electrical specs [6]. It is composed of a rail-to-rail amplifier. However, adding additional stages translates to additional poles which eventually degrade the over-all bandwidth of the whole receiver system. To balance this condition, active peaking is used as a load for the two preamplifiers. For this work, active inductors are used for active peaking.

The LVDS standard requires the receiver to receive signals with a very wide common mode range. Thus for this work, a rail-to-rail pre-receiver is utilized in order to accept signals from 0.1 to 1.6 V. Figure 12 depicts the schematic for the rail-to- rail pre-amplifier circuit that is composed an NMOS-input pair and a PMOS-input pair folded cascaded amplifier.

The pre-amplifier outputs a differential signal equal to the sum of the outputs of the NMOS and PMOS input pre-amplifier stages in parallel. The output differential signal of the pre- amplifier will be equal to twice the input differential voltage multiplied by the gain. In logarithmic terms, the gain is equal to the gain in dB for 1 pre-amplifier plus 6 dB.

For input common mode equal to 0.1 V, the NMOS pre receiver goes to cut-off while the PMOS pre-amplifier still stays in saturation to provide sufficient gain for the LVDS receiver 2nd stage. While for input common mode equal to 1.6 V, the PMOS pre-amplifier cuts-off and the NMOS will remain in saturation.

Figure 12(a) is the pre-amplifier circuit designed by the NMOS input folded cascade amplifier. The input common mode range of the NMOS input folded cascade topology is expected to have an input common mode range from the threshold level of the NMOS up to V_{DD}. Thus this pre-amplifier will be active whenever the input common mode level is at this range. The compliment of the NMOS input folded cascode amplifier is the PMOS input as shown in Fig. 12(b). This pre-amplifier will accept an LVDS signal with a DC level from 0 V up to V_{DD} minus the threshold level of the PMOS.

Folded cascode structure is used in order to achieve an almost input DC independent gain-bandwidth product for the first stage. The common gate devices set a low DC voltage at the drain terminals of the input devices in order to keep the voltage gain almost independent to the input DC. Each fully differential stage corresponds to one zero, thus one stage introduce one zero into the system and control it depending on the proper equalization setting being dictated by a logical control block. Moreover, the active inductor loads are designed to cancel the dominant pole at the output thus still being able to achieve a higher bandwidth. The pre-amp stage sets the proper input bias for the equalizer stage.

The equalizer stage consists of a two stage differential amplifiers shown in Fig. 13 with digitally programmable active inductor load. The active inductors are adjusted digitally through a binary weighted set of capacitor array for each load as shown in Fig. 14. Upon adjusting the capacitor array with 8 possible values, the zero produced by one equalizer stage is adjusted along the frequency domain with 8 possible steps creating a variable amount of peaking. Utilizing two stages of the equalizer enables the receiver to have a wider dynamic range or 8 × 8 possible zero combinations that can be used in equalizing the lossy transmission line.

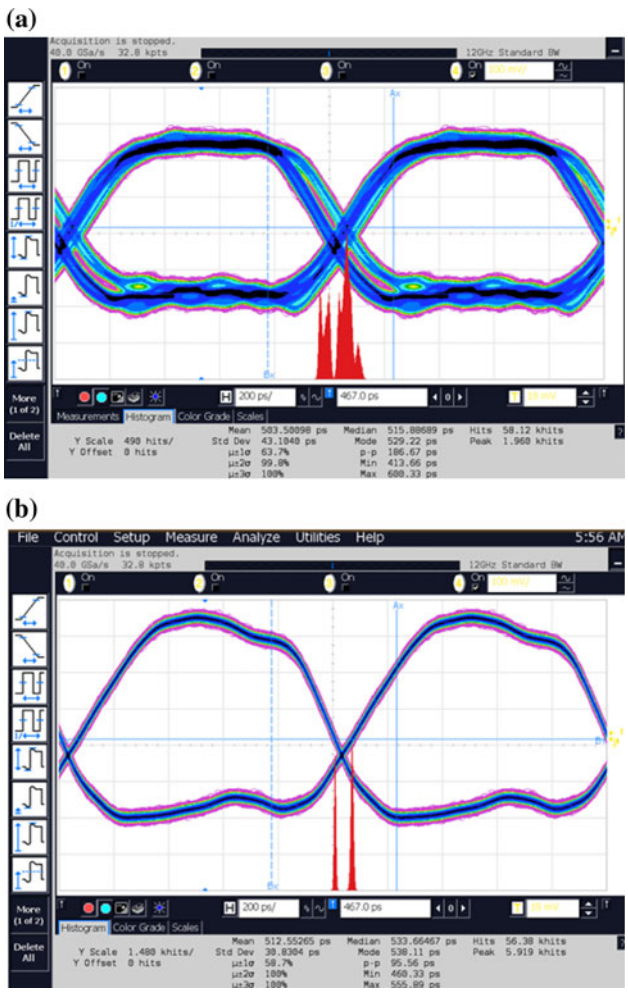

Fig. 21 LVDS transmitter pre-emphasis test at 200 ps per division time scale and 100 mV per division on magnitude scale. **a** Before pre-emphasis and **b** after pre-emphasis

4 Experimental results

Figure 15 displays the chip micrograph. The test chip is implemented in a 0.18 μm CMOS process that takes a total chip area 1,062 × 877 μm^2. Figure 16(a) shows the pre-emphasis and equalization control signal generator block. It is implemented using Altera's Max II FPGA. A Max II kit was used as seen in Fig. 16(b). It consists of 4 inputs. Every toggle of the P_{in} signal increments the P_{ctl}[3:0] from zero to its maximum by one. Preset simply resets the P_{ctl} signal back to zero. E_{in} signal increments the E_{ctl}[5:0] from zero to its maximum by one at every toggle. E_{reset} resets the E_{ctl} signal back to zero. Edge triggered 4-bit and 6-bit binary up counter were used for the P_{ctl} and E_{ctl} functions. The edge detect block monitors the toggling for P_{reset} or E_{reset} where it eventually gives a reset signal to the

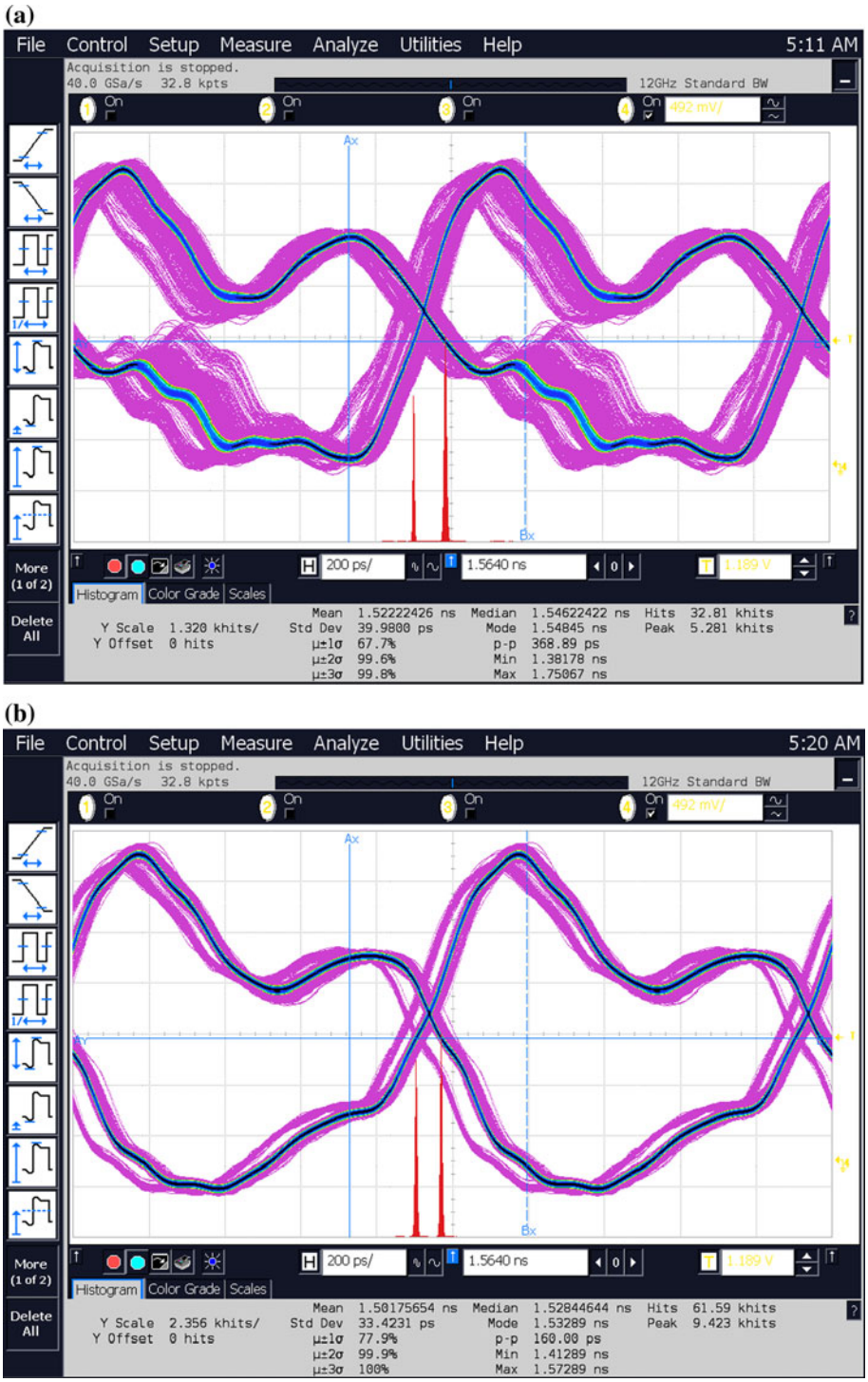

Fig. 22 LVDS receiver equalization test at 200 ps per division time scale and 492 mV per divisionon magnitude scale. **a** Before equalization and **b** after equalization

transmitter or receiver at every toggle edge. To visually check the pre-emphasis and equalization setting, a two-digit seven segment display is used show the current settings for each. This signal generator block is implemented in FPGA and was coded in behavioral Verilog.

Figure 17 shows the actual test set-up for the experiment. Two chips are configured as a transmitter and a receiver mounted on an FR4 PCB. The boards are then connected via an unshielded twisted wire pair with 0.5 m length. Data is inputted into the transmitter and eventually transmitting it via the transmission path given in Fig. 17 and received by the receiver. Figure 18 shows the LVDS signal measured at TP4. It can be seen that the common mode level of the LVDS signal is constant thus it confirms the functionality of the proposed common mode feedback scheme of this work.

Figure 19(a), (b) shows the LVDS receiver rail-to-rail test. Figure 19(a) shows an LVDS signal with common mode equal to 0.1 V being received by the receiver. It shows that the receiver was still able to convert it to full swing digital signal at its output. Figure 19(b) shows a receiver receiving an LVDS signal with common mode level equal to 1.6 V. It shows that the receiver still was able to convert it to full swing digital signal at a very high common mode level.

Figure 20 shows the receiver offset test. Two inputs were swept through a signal generator and the output is observed. The offset is measured from the point of intersection of the inputs to the transition point of the output. It was measured to be 28 mV.

With the same set up as Fig. 17, preemphasis and equalization function were then tested separately. The preemphasis test is done by disabling the equalization feature making the receiver function as a normal receiver. Data is then transmitted from the transmitter to the receiver along the lossy transmission line starting with a turned off preemphasis. Through the FPGA controller, the preemphasis settings are then gradually increased until the signal quality is achieved. Figure 21(a), (b) shows the results in the LVDS transmitter pre-emphasis test measured at TP4. Figure 21(a) shows the LVDS signal without pre-emphasis having an eye height = 320 mV and an eye peak to peak jitter = 186.67 ps. Figure 21(b) shows the LVDS signal at TP4 after pre-emphasis. It is observed that an improved eye height of 440 mV and an improved eye jitter of 95.56 ps. The signals were measured at a speed of 1 Gbps.

For the equalization verification, the preemphasis feature is disabled thus the transmitter simply functions as a normal transmitter. Same as the preemphasis test, the equalization test starts at a turned off equalization feature, then gradually increase the equalization setting until the best signal quality is achieved. Figure 22(a), (b) shows the signal at TP6. Figure 22(a), (b) shows the signals before and after equalization respectively. Figure 22(a) shows a measured peak to peak jitter equal to 369 ps. Figure 22(b) shows an improved measured peak to peak jitter of 160 ps. Figure 23 shows the signal verification at the receiver output or TP6. A k28.5 signal pattern in inputted into the transmitter and the output is checked at the receiver. It can be seen from the waveform that the signal transmitted is still the same signal being received. Figure 24(a) depicts the eye signal eye at the receiver output when the pair is ran at 1.7 Gbps. It can be seen that the

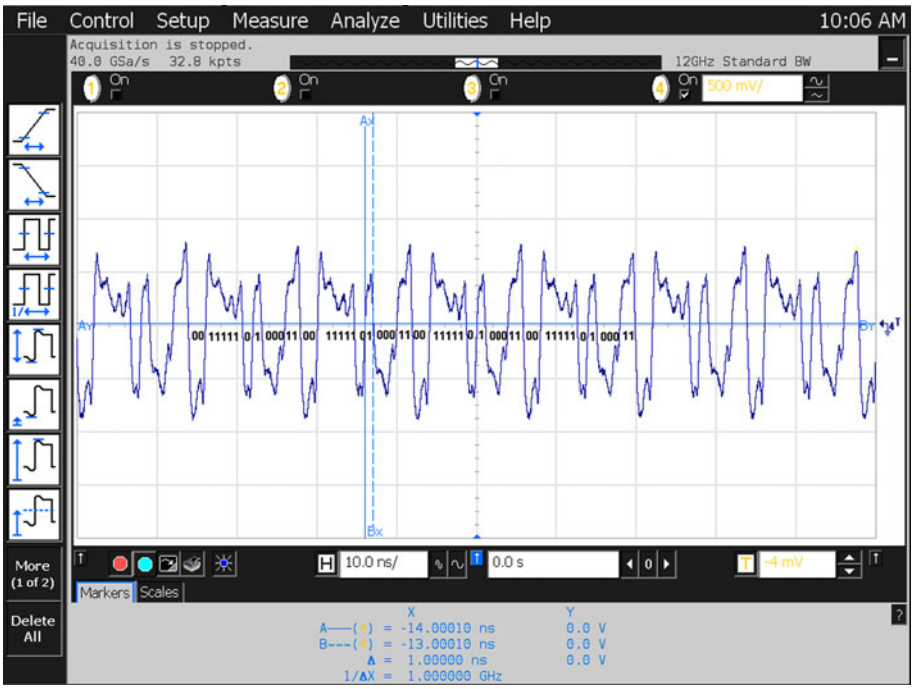

Fig. 23 Output at TP6 using k28.5 signal pattern

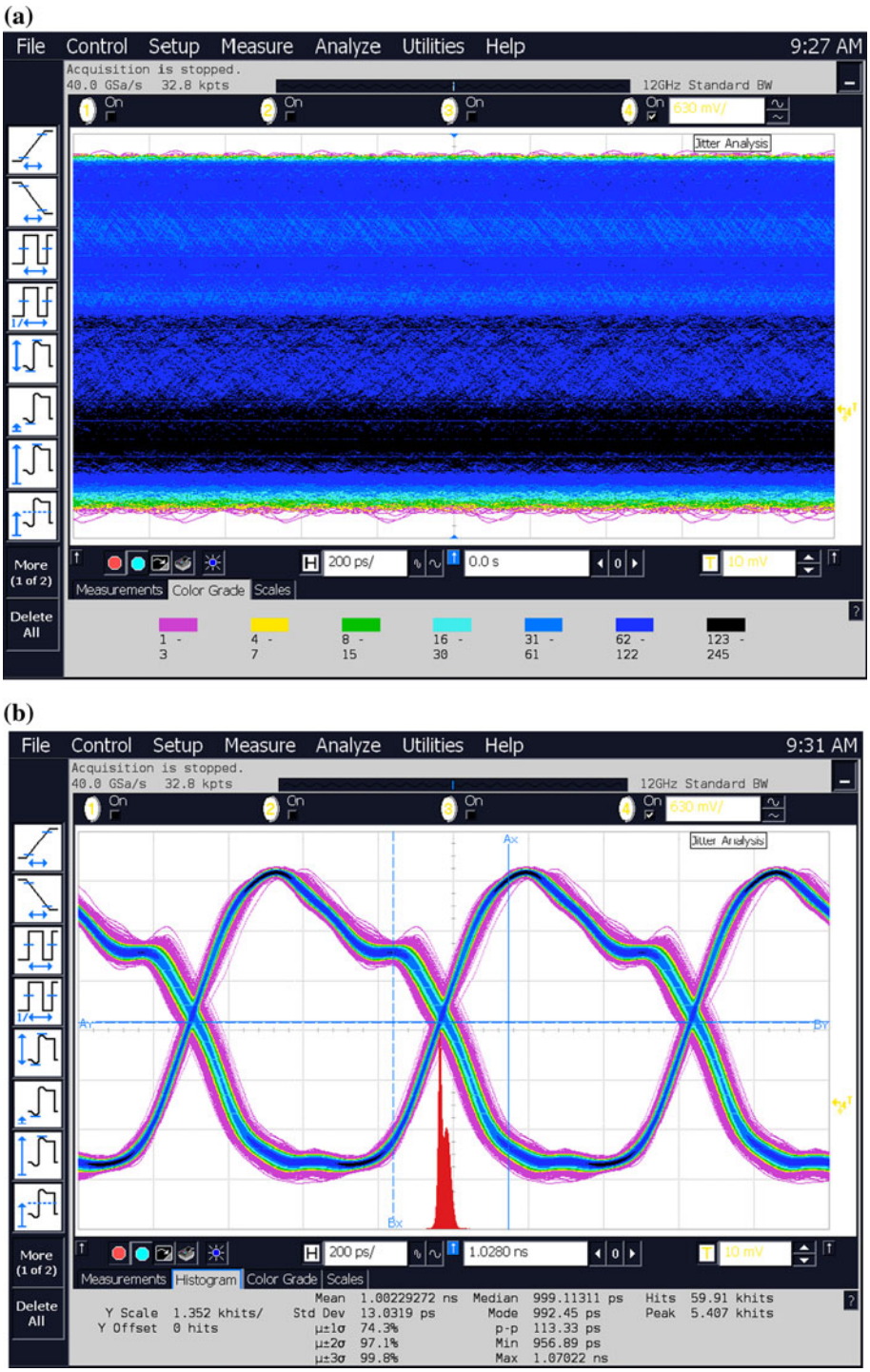

Fig. 24 Equalization plus pre-emphasis verification at 1.7 Gbps. **a** Failed transmission before pre-emphasis and equalization and **b** successful transmission after pre-emphasis and equalization

signal eye is total closed. Thus failure of transmission occurs. Figure 24(b) shows the signal eye quality at the transmitter plus receiver output at Tp6. It can be seen that the eye significantly improved from a failed transmission. Jitter for this waveform was measured to be 13 ps rms. Thus pre emphasis plus equalization effectively improves signal integrity even at worst bandwidth or transmission line.

Table 2 summarizes that this work has one of the lowest amounts of jitter at same test condition, one of the lowest power dissipation, one of the fastest operating frequency, one of the smallest area, but the only one that does not use passive RC compensation. Literatures [1, 7] and [4] specified that they use passive RC compensation thus consuming a significant percentage of area for the resistor and capacitor. Literatures [3, 8] and [9] did not specify if they use passive

Table 2 Transmitter comparison table

Transmitter	This work	JSSC'09 [3]	TCSI'05 [10]	MWCAS'01 [8]	JSSC'05 [2]	JSSC'01 [1]	JSSC'01 [7]
Technology	0.18 μm CMOS	0.18 μmm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.35 μm CMOS
V_{dd}	1.8	1.9	1.7–3.5	1.8	1.8	3.3	3.3
V_{OD} (mV)	442	430	265–300	152–212	340	400–425	320
I_{DD} (mA)	5.4	4.8 mA	6–7 mA	12.8 mA	12.8 mA	13 mA	5.5 mA
Max data rate (Gbps)	2.5	2.5	1.2	1.24	1.4	2	1
Jitter (prms)	5.1 ps @ 1 Gbps	4.5 ps @ 1 Gbps	14.2 ps @ 1.56 Gbps	N/A	50 ps @ 1 Gbps	N/A	N/A
Area (mm^2)	0.044	0.067	0.068	0.022	0.11	0.175	0.039
Passive compensation	None	Yes	N/A	N/A	N/A	Yes	Yes
F.O.M ($mW * mm^2$/ Gbps)	0.17	0.24	0.83	0.403	1.8	3.75	0.71

Table 3 Receiver comparison table

Receiver	This work	JSSC'01 [1]	ISCAS'05 [11]	ISCAS' [12]	ISSCC'06 [13]
Technology	0.18 μm	0.35 μm	0.25 μm	0.13 μm	0.25 μm
V_{dd}	1.8 V	3.3 V	2.5 V	3.3 V	3.3 V
Power Consumption	34 mW	33 mW	51 mW	11 mW	153 mW
Maximum data rate	2 Gbps	1.2 Gbps	1.3 Gbps	1.3 Gbps	1.4 Gbps
Normalized power dissipation (mW/Gbps)	17	27.5	39.73	8.46	109.28
Cell size	0.147	0.081	N/A	0.066	1.3
Jitter	30 ps p-p	N/A	N/A	60 ps	312 ps p-p

RC compensation, however, when they discussed about their CMFB, they refer to [1] that uses RC compensation on its CMFB. The jitter in [4] is much smaller than this work since its novelty is focused on minimizing the skew of the LVDS signal thus it is expected that it will yield a better jitter results. Although this works transmitter is also focused on improving signal integrity at the transmitter, the advantage of this work compared to [4] is that, this work does not utilize area consuming RC compensation.

For the overall performance comparison of this works transmitter relative to other published work, a figure of merit (F.O.M) is defined as:

$$F.O.M = \frac{Power \cdot Area}{DataRate} \tag{19}$$

It is proved that this work has the lowest FOM as compared to the closest published work. Accordingly, it concludes that the transmitter has the lowest power consumption with the highest operating frequency while having one of the smallest chip area.

Table 3 shows that this works receiver has the smallest amount of jitter and having the highest operating frequency at a comparable amount of power dissipation. The area is bigger than the other published work because of the addition of the equalizer block. Nonetheless, power consumption is still comparable to the other published work despite the addition of the equalization feature that enables the receiver to have the lowest amount of jitter. The improvements shown from the transmitter and receiver are very critical since it espouse the improvement of the most important parameters in any transceiver system. In the transmitter, it has eliminated the use of resistor and capacitors for compensation, thus it reduce the chip area for normal transmitters. It also has one of the smallest amounts of power even though it has the additional pre-emphasis feature. In the case of the receiver, the data rate improvement is significant since it signify higher speed capability with lower increase in power even if it has the additional equalization feature. The equalization feature of the receiver is the most important part of this work since it espouses the enhancement in signal integrity. As can be seen,

this works jitter is significantly lower than other published work, thus making it suitable for high speed and sophisticated clock and data recovery (CDR) system.

5 Conclusion

A pre-emphasis and equalization scheme for an LVDS transmitter and receiver has been presented. Both proposed pre-emphasis and equalization scheme effectively compensates for the high frequency losses due to the non-idealities of the transmission line. As demonstrated in the actual experiment, a very lossy transmission line with a degraded signal quality was greatly compensated. From a failed transmission, through pre-emphasis and equalization, transmission becomes successful. On the other hand, the use of area consuming resistor and capacitor for loop stability compensation for the LVDS transmitter were also eliminated. This is done by using the common mode feedback scheme presented by this work. As shown in the actual measurement results, the common mode level of the LVDS signal is seen to be stable, thus implying that the proposed CMFB scheme effectively stabilized the LVDS transmitter without using the area consuming resistor and capacitor compensations. The proposed LVDS transmitter turned out to have one of the highest operating frequencies with one of the lowest power dissipation while having the lowest chip size. In the proposed LVDS receiver, it achieves the lowest amount of jitter and also has the highest operating frequency at almost the same amount of power as compared to the references.

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