SPI Finite State Machine

CPOL = 0
CPHA = 0
} SPI mode 0

↳ **CPOL**: Sets the polarity of the clock signal during the Idle state. } Since CPOL = 0, the first edge is a rising edge.

CPHA: Selects the clock phase, depending on CPHA the rising or falling edge will be used to sample/shift data. } Since CPHA = 0, data is captured on the first clock edge, which if CPOL = 0 will be the rising edge.

* ↳ IF CPHA = 1, then data would be sampled on the second clock edge ie the falling edge if CPOL = 0.

Just for understand.

FSM inputs & outputs

↳ Inputs:
- t_start: Start Transaction
- reset: Syncronous Reset
- count: number of bytes to shift remaining

↳ Outputs:
- cs: Control Slave
- Load/unload status
- state

FSM States

↳ State 0 (reset/error): Initial State of FSM, but also default state.

↳ State 1 (idle): When a transaction hasn't started, or when a transaction just finished

↳ State 2 (load): When a transaction just starts (t_start = 1), from idle, "loading" transaction data, including count (the # of bits of data needed to be shifted).

↳ State 3 (Transact): Either coming from load state or itself if count (!= 0), meaning there is data remaining needing to be shifted, then we come to the transact state.

Data Shifting ← Here we do the data shifting.

There are a few things needed to be done for data shifting.

1. We assign MOSI line to the most significant digit of our mosiR shift register.
   ↳ Only is the slave is selected (CS = 0), else set to 1'bz undefined.
2. We assign spi_clk to the sys_clk if we're in transact state else pull to 1b'0.
3. On the rising edge of the spi_clk and we are in trasact state, shift the misoR register left by one bit and in the new space put the miso line's current state/data.
4. On the Falling edge of spi_clk and in transact mode, we shift mosiR register left by one, (because that left most bit was sent down the MOSI line in step 1.) and in the new space fill it with a 0, 1'b0.
5. Also on the falling edge of spi_clk and in trasact decrement the count register.

↳ State 4 (unload): This is where we "latch" the content of the miso shift register to the dout register.

FSM Diagram : Rudra D.

R : Register
"/": Output State