Homework 1

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ECE/CS 5510 Multiprocessor Programming

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1.
(a) *Safety*: both processes are never in the critical section at a same time.
(b) *Liveness*: clients may retain resources eventually.
(c) *Safety*: a situation where it is not cloudy before it rains should never happen.
(d) *Safety*: more than one person never sits on the drivers seat.
(e) *Liveness*: the green light will eventually be turned on.
(f) *Safety*: the car never enters the roundabout when there is a car in the roundabout.
(g) *Liveness*: the car will leave the roundabout eventually.
(h) *Safety*: more than one direction/side is never green at a same time.

2.
Time for single instruction on the first machine:

$$\frac{1}{N * x}$$

Time for single instruction on the second machine:

$$\{(1-p) + \frac{p}{2N}\} * \frac{1}{x} \; (where\ p\ is\ fraction\ of\ parallelizable)$$

So that the second system is advantageous,

$$\frac{\frac{1}{N*x}}{\{(1-p)+\frac{p}{2N}\}*\frac{1}{x}} > 1$$

$$\frac{1}{N*x} > \{(1-p)+\frac{p}{2N}\}*\frac{1}{x}$$

$$\frac{1}{N} > \{(1-p)+\frac{p}{2N}\}$$

$$2 > 2N - 2NP + P$$

$$2 - 2N > (1-2N)P$$

$$\therefore \frac{2-2N}{1-2N} < P$$

$$(\because N >= 1 \; and \; 2*N \text{ is the number of cores})$$

3.
Without the optimization, we get

$$\frac{T_s}{T_p} = P + \frac{1-P}{N}$$

With optimization, we can get a new equation with a new fraction of sequential P':

$$4*\frac{T_s}{T_p} = P' + \frac{1-P'}{N} \text{ where } P'=\frac{P}{10}$$

Now we have two equations.

$$\frac{T_s}{T_p} = P + \frac{1-P}{N} \tag{1}$$

$$4*\frac{T_s}{T_p} = \frac{P}{10} + \frac{1-\frac{P}{10}}{N} \tag{2}$$

$$where \; T_s \; is \; time \; of \; sequential \; part,$$

$$T_p \; is \; time \; of \; parallel \; part, and \; P \; is \; fraction \; of \; sequential$$

$$\therefore P = \frac{5}{N-1}$$

The invariant is

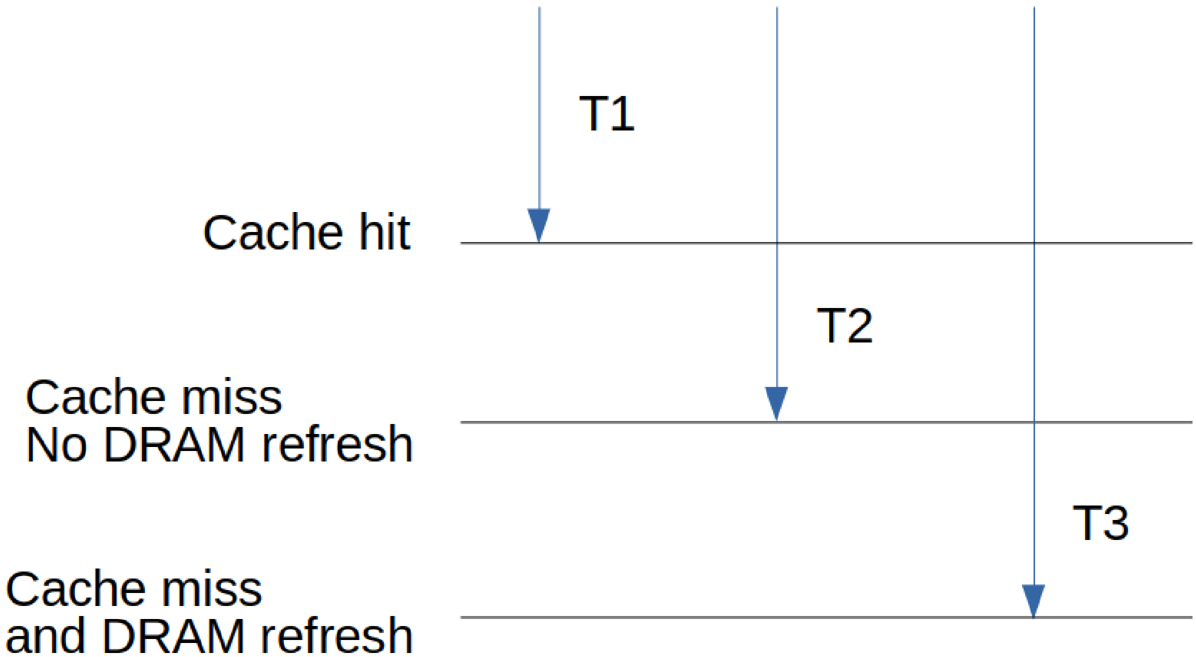
$$0 < P < 1$$

Therefore,

$$0 < \frac{5}{N-1} < 1$$

$$\therefore N > 6$$

4.



Let N is the number of accesses, T_1 is access time of cache hit for a single instruction, T_2 is access time of cache miss with no DRAM refresh for a single instruction, and T_3 is access time of cache miss with DRAM refresh for a single instruction.

Elapsed time is

$$E_1 = 0.5NT_1 + 0.35NT_2 + 0.15NT_3$$

If the penalty incurred by DRAM refresh is eliminated, then

$$T_3 = T_2$$

So, elapsed time in those case is

$$\begin{aligned} E_2 &= 0.5NT_1 + 0.35NT_2 + 0.15NT_2 \\ &= 0.5NT_1 + 0.5NT_2 \end{aligned}$$

Performance benefit (speed up) is

$$\frac{E_2}{E_1} = \frac{0.5NT_1 + 0.5NT_2}{0.5NT_1 + 0.35NT_2 + 0.15NT_3}$$

5.
Let's assume $n = 10$.
Then, we can divide the loop into 10 parallel blocks like below. The blocks can be executed parallelly.

block 0

$$\begin{bmatrix} CPU0 : A[0][1] += A[0][2] - A[0][0] \\ CPU1 : A[1][1] += A[1][2] - A[1][0] \\ CPU2 : A[2][1] += A[2][2] - A[2][0] \\ \vdots \\ CPU9 : A[9][1] += A[9][2] - A[9][0] \end{bmatrix}$$

block 1

$$\begin{bmatrix} CPU0 : A[0][2] += A[0][3] - A[0][1] \\ CPU1 : A[1][2] += A[1][3] - A[1][1] \\ CPU2 : A[2][2] += A[2][3] - A[2][1] \\ \vdots \\ CPU9 : A[9][2] += A[9][3] - A[9][1] \end{bmatrix}$$

$$\vdots$$

block 9

$$\begin{bmatrix} CPU0 : A[0][9] += A[0][10] - A[0][8] \\ CPU1 : A[1][9] += A[1][10] - A[1][8] \\ CPU2 : A[2][9] += A[2][10] - A[2][8] \\ \vdots \\ CPU9 : A[9][9] += A[9][10] - A[9][8] \end{bmatrix}$$

As you can see above, there is dependency among columns, but no dependency among rows.
For example, $A[0][1]$ on the block 0 should be executed before the second block 1.
In conclusion, the inner loop (j) can be parallelized because the inner loop determines row.
The outer loop (i) can NOT be parallelized because the outer loop determines column.

6.
The state of lamps can only be either "both on (on,on)" or "both off (off, off)". One student is assigned to a captain. The captain only turns the lamps off when they are on. He does nothing when the lamps are off. He can turns off as much as he wants. Other students can only turn on the lamps twice when they are off. If the lamps are on or they have already turned on the lamps twice, they do nothing.
The captain increases his count when the lamps are on and he turns them off. When his counter reaches 22, he can state that all students have entered the common room at least once. Other students do not answer.