De-Yu Lian

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Education

National Taiwan University Sept 2022 – May 2024
Master of Science in Electronics Engineering *Taipei City, Taiwan*

- **Thesis Research:** VLSI Power Delivery Network Optimization | *C++, Python, Matlab, CUDA*
  * Supervisor: Charlie Chung-Ping Chen, Florin Dartu
  * Cooperated TSMC Joint Developed Project (JDP) with Design Flow Signoff Deportment (DFSD).
  * Proposed a power grid optimization method to improve chip reliability on voltage drop issues.
  * Developed a tool that achieves a 223x speed improvement while maintaining zero error compared to the commercial golden tool Synopsys HSPICE.
  * Experimental results from the test case in the IBM and 2023 The CAD Contest at ICCAD Problem C show that, compared to before adjustment, our optimization method has significantly improved the voltage drop issue and saved up to 0.3 % of the area.
  * **Technical Skills:** SPICE Simulation & Optimization, Linear Programming, Numerical Analysis, Reinforcement learning

Yuan-Ze University Sept 2016 – Aug 2021
Bachelor of Science in Electrical Engineering *Taoyuan City, Taiwan*

Experience

Taiwan Semiconductor Manufacturing Co., Ltd (TSMC) July 2023 – Aug 2023
Intern Digital Designer at Design Technology Platform / Design Flow Signoff Department *Hsinchu City, Taiwan*

- Developed a spice tool that achieves a 39x speed improvement while maintaining zero error compared to the commercial golden tool.
- Won fourth place in TSMC Internship competition.

Electronic Design Automation Camp Aug 2022
Vice Chairman *Taipei City, Taiwan*

- Organized the Electronic Design Automation Camp, co-hosted by National Taiwan University and the IEEE Council on Electronic Design Automation (CEDA), to foster discussions in the Electronic Design Automation field among students from various universities.

Cadence Design Systems, Inc July 2022 – Sept 2022
Software Engineer Intern *Hsinchu City, Taiwan*

- Research Relationship between heat effect and metal layer density.
- Study how to connect power and thermal models between Cadence's Voltus & Celsius.

Foxconn Technology Group July 2019 – Aug 2019
Software Engineer Intern *Taoyuan City, Taiwan*

- Developed a fire risk assessment and early warning expert system, employing computer vision to detect potential hazards accurately.
- Integrated advanced sensor technology to monitor environmental conditions, significantly enhancing the system's predictive capabilities and reliability.

Honors & Awards

TSMC Internship Competition Aug 2023
Taiwan Semiconductor Manufacturing Company *Hsinchu City, Taiwan*

- Won fourth place(Honorable Mention) in TSMC internship competition.

Undergraduate Graduation Project Competition Mar 2019
Yuan Ze University Department of Electrical Engineering *Taoyuan City, Taiwan*

- Led the team and got third place in the graduation thematic competition.

ActInSpace: Largest Worldwide Space Application Hackathon Mar 2018
French Space Agency (CNES) & National Space Program Office (NSPO) *Taipei City, Taiwan*

- Led the team and got Third place in the Taiwan regional competition.

Student Engineering Thesis Competition Dec 2017
College of Electrical and Communication Engineering & College of Engineering, Yuan Ze University *Taoyuan City, Taiwan*

- Got the best paper award in a student engineering thesis competition.

Projects

Image Recognition on STM32 Microcontrollers | *Python, TensorFlow Lite, TinyML*

- In this project, we have designed a neural network based on MobileNetV2 that can perform an image recognition task (CIFAR-10) and deploy it on STM32 MCU.
- In our MobileNetV2-based model, we can keep the accuracy to 0.881667 and the average latency at 578ms.
- We also can achieve an accuracy of 0.9 in EfficientNet and successfully use the pruning and quantized method to reduce the model size by 4x.
- **Technical Skills:** Edge Computing, Neural Networks, Computer Vision

Fault Effect Mitigation on Deep Neural Network | *Python, Verilog, Pytorch, TinyML*

- In this work, we proposed a method combining two fault-tolerant techniques from previous research: range restriction (Ranger) and weight pruning.
- We have successfully fitted Ranger into the TinyML platform and optimized unaligned pruning for memory boundaries into one DNN model.
- **Technical Skills:** Circuit Design, Neural Networks, Computer Vision, Fault-Tolerant Computing

2023 CAD Contest Problem D @ IEEE/ACM ICCAD: Fixed-Outline Floorplanning with Rectilinear Soft Blocks | *C++*

- In the design flow of the silicon chip, floorplanning plays an essential role in providing specific analysis of the chip area and wirelength between modules in the earlier stage before the placement and routing.
- In this project, we use the 'scan' technology to find vacant space and put soft blocks in the fixed region. Finally, we successfully finished the floorplanning process of the three cases and significantly optimized the total half-perimeter wirelength (HPWL).
- **Technical Skills:** Physical Design

Gauss-Seidel Iteration Machine (GSIM) for Solving Linear Equations | *Verilog*

- Led a project team in developing a circuit, a MediaTek collaboration, as part of the NTU CVSD final project.
- Uses the Gauss-Seidel method to efficiently and accurately solve multiple linear equations, demonstrating a deep understanding of numerical methods and hardware.
- Incorporated features like integer asymmetric saturation for overflow management and fractional truncation for bit-width reduction enhance GSIM's reliability and precision.
- Completed a chip design from RTL architecture design to synthesis, verification, placing, routing, and DRC checking.
- **Technical Skills:** Circuit Design, Numerical Analysis

Simple Image Processing and Display Controller | *Verilog*

- Designed and implemented a 16x16 image display controller with advanced processing capabilities for enhanced visual representation in consumer electronics.
- Implemented core functions for dynamic image processing, including origin shifting (right, left, up, down), scaling (up and down), and applying a median filter operation. These functions allow for versatile image adjustments and enhancements directly on the hardware level.
- Developed sophisticated algorithms for image quality improvement and format conversion, including YCbCr display for color space manipulation and Census transform for texture analysis. These features enable the display controller to support various image types and quality enhancement techniques.
- **Technical Skills:** Circuit Design, Computer Vision

Publications

Ocean Climate CubeSat Constellation (OCCC) Mission Oct 2022

Conference: Preliminary Workshop for Mission Idea Contest 8th Istanbul Technical Universit, Ayazaga Campus, Istanbul, Turkey

Technical Skills

Programming Languages: C/C++, MATLAB, Verilog, Python
Library: Eigen, Gurobi, CPLEX, PyTorch, Tensorflow, CVXPY, OpenCV, Scipy, Numpy
Concepts: SPICE simulation & optimization, RC reduction, Physical Design, Computer Vision, Computer Architecture, Fault-Tolerant Computing, Edge Computing, Artificial Intelligence, Neural Networks, API