De-Yu Lian

+886 989-869-198 dj7061214@gmail.com linkedin.com/in/deyulian/ github.com/deyulian

Education

National Taiwan University Sept 2022 – May 2024
Master of Science in Electronics Engineering *Taipei City, Taiwan*

- **Relevant Coursework:** Advanced Digital Signal Processing(Python), Computer Vision(Python), Fault-Tolerant Computing(C++), Digital Signal Processing in VLSI Design(C++), Advanced Integrated Circuit Design(Verilog, Python), Computer Aided Analysis & Optimization of Integrated Circuit(C++), Computer-aided VLSI System Design(Verilog)
- **Thesis Research:** VLSI Power Delivery Network Optimization (TSMC Joint Developed Project)

Yuan-Ze University Sept 2016 – Aug 2021
Bachelor of Science in Electrical Engineering *Taoyuan City, Taiwan*

- **Relevant Coursework:** Machine Learning and Its Applications(Python)

Experience

Taiwan Semiconductor Manufacturing Co., Ltd (TSMC) July 2023 – Aug 2023
Intern Digital Designer at Design Technology Platform / Design Flow Signoff Department *Hsinchu City, Taiwan*

- Developed a spice tool that achieves a 39x speed improvement while maintaining zero error compared to the commercial golden tool.
- Won fourth place in TSMC Internship competition.

EDA Camp Aug 2022
Vice Chairman *Taipei City, Taiwan*

- Organized the EDA Camp, co-hosted by National Taiwan University and the IEEE Council on Electronic Design Automation (CEDA), aimed at fostering discussions in the EDA field among students from various universities.

Cadence Design Systems, Inc July 2022 – Sept 2022
Software Engineer Intern *Hsinchu City, Taiwan*

- Research Relationship between heat effect and metal layer density
- Study how to connect power and thermal models between Cadence's Voltus & Celsius

Foxconn Technology Group July 2019 – Aug 2019
Software Engineer Intern *Taoyuan City, Taiwan*

- Developed a fire risk assessment and early warning expert system, employing computer vision to detect potential hazards accurately.
- Integrated advanced sensor technology to monitor environmental conditions, significantly enhancing the system's predictive capabilities and reliability.

Honors & Awards

TSMC Internship Competition Aug 2023
Taiwan Semiconductor Manufacturing Company *Hsinchu City, Taiwan*

- Won fourth place(Honorable Mention) in TSMC internship competition.

Graduation Theme Competition Mar 2019
Yuan Ze University Department of Electrical Engineering *Taoyuan City, Taiwan*

- Led the team and got the Third place in graduation thematic competition.

ActInSpace: Largest Worldwide Space Application Hackathon Mar 2018
French Space Agency (CNES) & National Space Program Office (NSPO) *Taipei City, Taiwan*

- Led the team and got Third place in the Taiwan regional competition

Student Engineering Thesis Competition Dec 2017
College of Electrical and Communication Engineering & College of Engineering, Yuan Ze University *Taoyuan City, Taiwan*

- Got the first prize award in student engineering thesis competition.

Thesis

VLSI Power Delivery Network Optimization | *C++, Python, Matlab, CUDA*

- Cooperated TSMC Joint Developed Project (JDP) with Design Flow Signoff Deportment (DFSD)
- Proposed a power grid optimization method to improve chip reliability on voltage drop issues
- Developed a tool that achieves a 223x speed improvement while maintaining zero error compared to the commercial golden tool Hspice.
- Experimental results from the testcase in the IBM and 2023 The CAD Contest at ICCAD show that, compared to before adjustment, our optimization method has significantly improved the issue of voltage drop and also saved up to 0.3% of the area.

Projects

Image Recognition on STM32 Microcontrollers | *Python, TensorFlow Lite, TinyML*

- In this project, we haved design a neural network based on MobileNetV2 that can perform image recognition task (CIFAR-10) and deploy it on STM32 MCU.
- In our MobileNetV2 based model, we can keep the accuracy to 0.881667 and average latency at 578ms.
- We also can achieve an accuracy of 0.9 in EfficientNet, and successfully use the pruning and quantized method to reduce the model size by 4x.

Fault Effect Mitigation on Deep Neural Network | *Python, Verilog, Pytorch, TinyML*

- In this work, we proposed a method combining two fault-tolerant techniques from previous research: range restriction (Ranger) and weight pruning.
- We have successfully fitted Ranger into the TinyML platform and optimized unaligned pruning for memory boundaries into one DNN model.

2023 CAD Contest Problem D @ IEEE/ACM ICCAD: Fixed-Outline Floorplanning with Rectilinear Soft Blocks | *C++*

- In the design flow of the silicon chip, floorplanning plays an essential role in providing specific analysis of the chip area and wirelength between modules in the earlier stage before the placement and routing.
- In this project, we use the 'scan' technology to find vacant space and put soft blocks in the fixed region. Finally, we finished the floorplanning process of the three cases successfully and optimize the total half-perimeter wirelength (HPWL) to the significant extent.

Gauss-Seidel Iteration Machine | *Verilog*

- Led the team to solve the Gauss-Seidel Iteration Machine circuit developed by MediaTek in the NTU CVSD final project.
- Completed a chip design from RTL architecture design to synthesis, verification, placing, routing and DRC checking.

Publications

Ocean Climate CubeSat Constellation (OCCC) Mission Oct 2022

Conference: Preliminary Workshop for Mission Idea Contest 8th Istanbul Technical Universit, Ayazaga Campus, Istanbul, Turkey

Technical Skills

Programming Languages: C/C++, MATLAB, Verilog, Python
Concepts: Computer Vision, Computer Architecture, Fault tolerance, RC reduction, Edge Computing, Artificial Intelligence, Neural Networks, API