

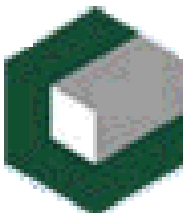
Plataforma HW/SW de sistemas de procesamiento

Maestría en Sistemas Digitales

Alejandro J. Cabrera Sarmiento

Dpto. de Automática y Computación
Universidad Tecnológica de La Habana “José Antonio Echeverría”
CUJAE

alex@automatica.cujae.edu.cu



Sumario

- Creación de proyectos con BSB
- Definición de especificaciones HW con XPS
 - **Fichero MHS** (*Microprocessor Hardware Specification*)
- Platgen: *Platform Generator*
- Configuración de la plataforma SW con XPS
 - **Fichero MSS** (*Microprocessor Software Specification*)
- LibGen: *Library Generator*



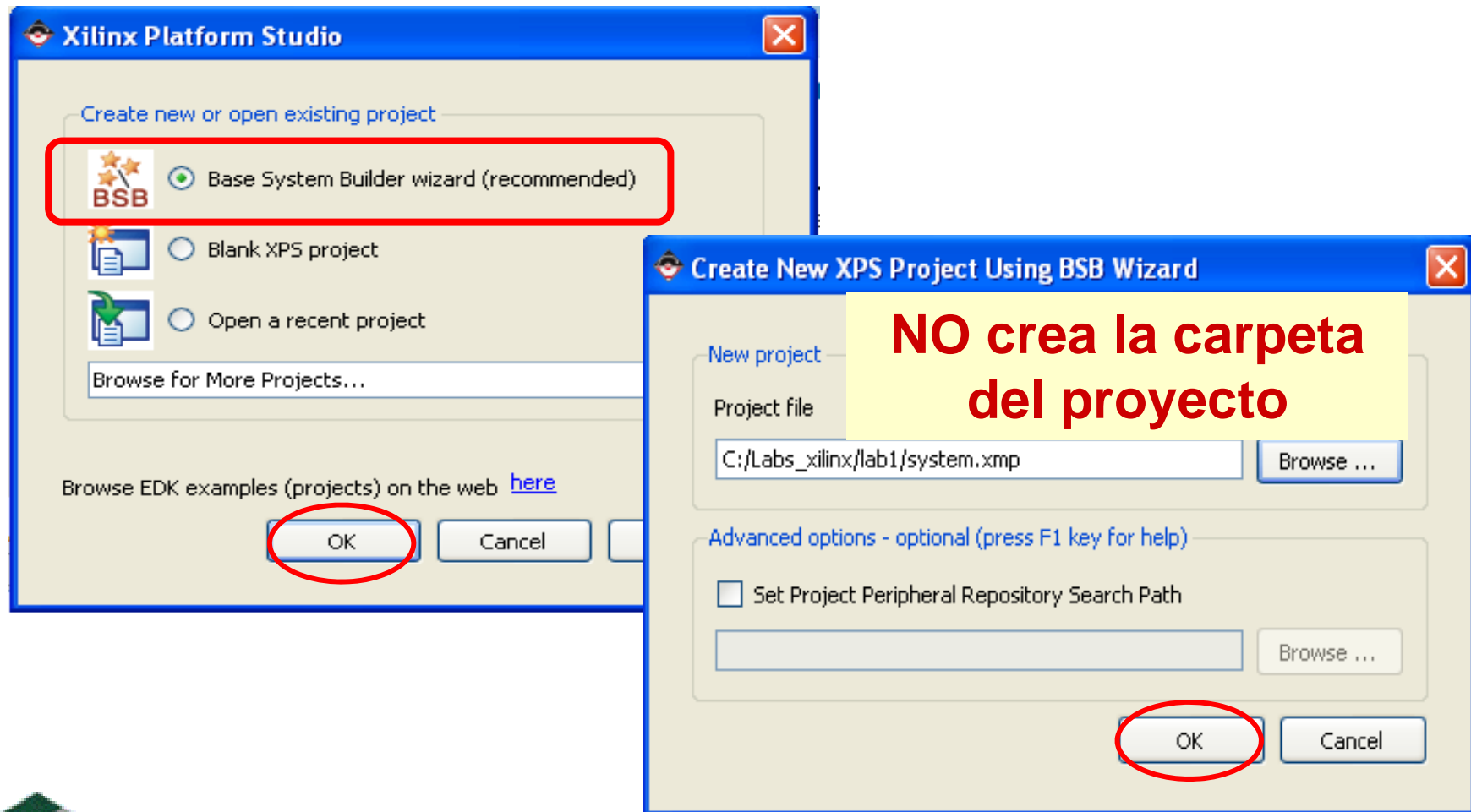
Inicio de proyectos en XPS

- ❑ La creación de un proyecto de un sistema de procesamiento empotrado basado en MicroBlaze (o Power PC) requiere la definición de los ficheros de especificación de hardware (**MHS**) y software (**MSS**)
- ❑ Existen tres procedimientos para crear una plataforma en XPS:
 - Mediante el asistente *Base System Builder* (**BSB**)
 - Si la placa que se utiliza es una de las soportadas
 - Mediante Xilinx Platform Studio (**XPS**):
 - IP Catalog: especificación hardware ... **MHS**
 - Software Platform Settings: configuración software ... **MSS**
 - Combinación de ambos

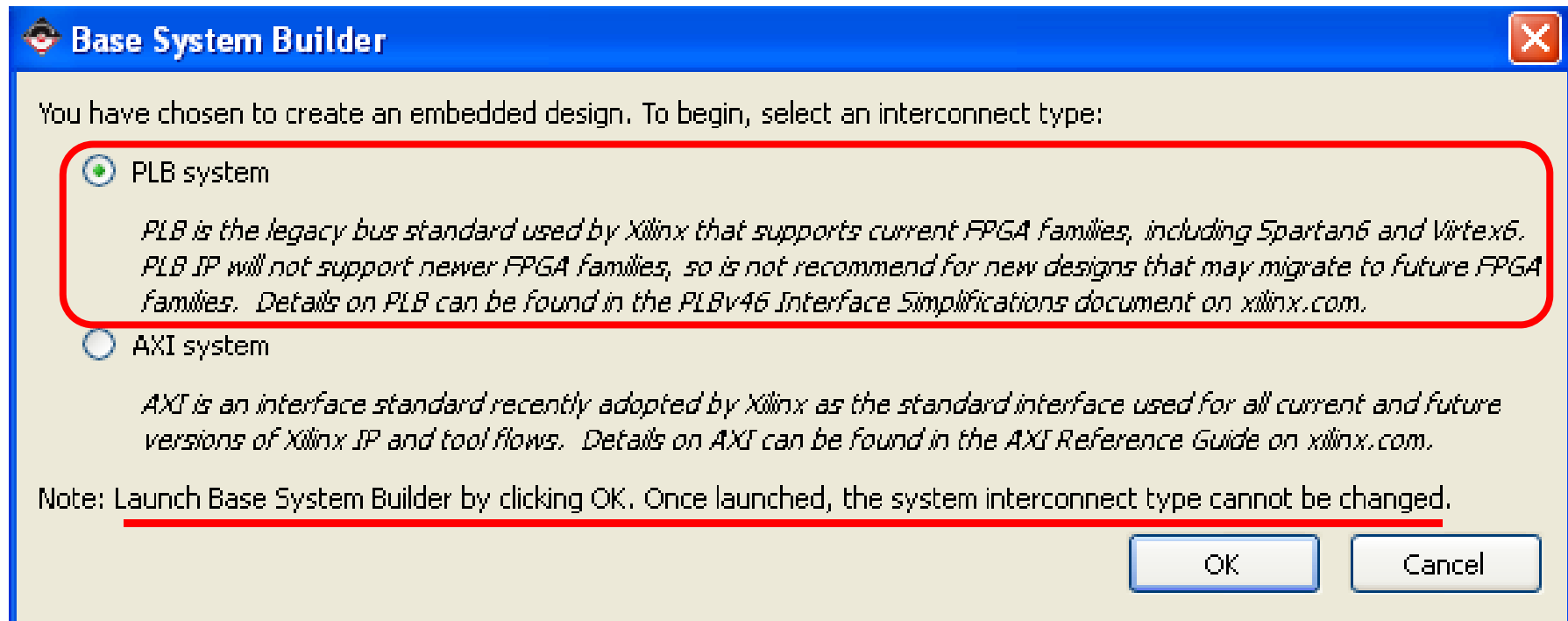


Creación de Proyectos con *BSB*

Al iniciar XPS...



Bus de expansión en BSB



AXI sólo con Spartan-6+, Virtex-6+ y Zynq



1.- Selección de placa de desarrollo

Fabricante
Placa

Base System Builder

Welcome **Board** System Processor Peripheral Cache Application Summary

Board Selection
Select a target development board.

Board

☒ I would like to create a system for the following development board

Board Vendor: Xilinx
Board Name: **Spartan-3A Starter Kit**
Board Revision: D

☐ I would like to create a system for a custom board

Board Information

Architecture: spartan3a Device: xc3s700a Package: fg484 Speed Grade: -4

☐ Use Stepping

Reset Polarity: Active High

Related Information

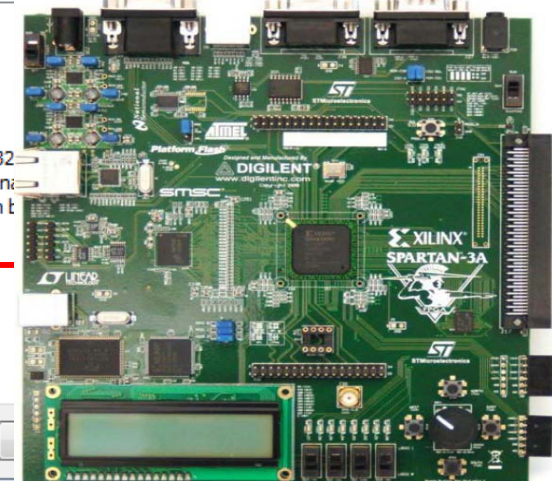
[Vendor's Website](#)
[Vendor's Contact Information](#)
[Third Party Board Definition Files Download Website](#)

The MicroBlaze Spartan-A Embedded Development Board utilizes Xilinx Spartan-3A XC3S700A-FG484 device. The board includes two RS232, four DIP switches, four push buttons, eight LEDs, VGA port, 16 character 2 line LCD display, PS/2 port, push button rotary encoder, SPI analog-to-digital converter, SPI digital to analog converter, 10/100 Ethernet port, 2-16 Mbit SPI flash, 4MB of parallel flash and 512 MB DDR2 SDRAM. Push button South(RESET) is used as system reset. The design to be created also works on revision C board.

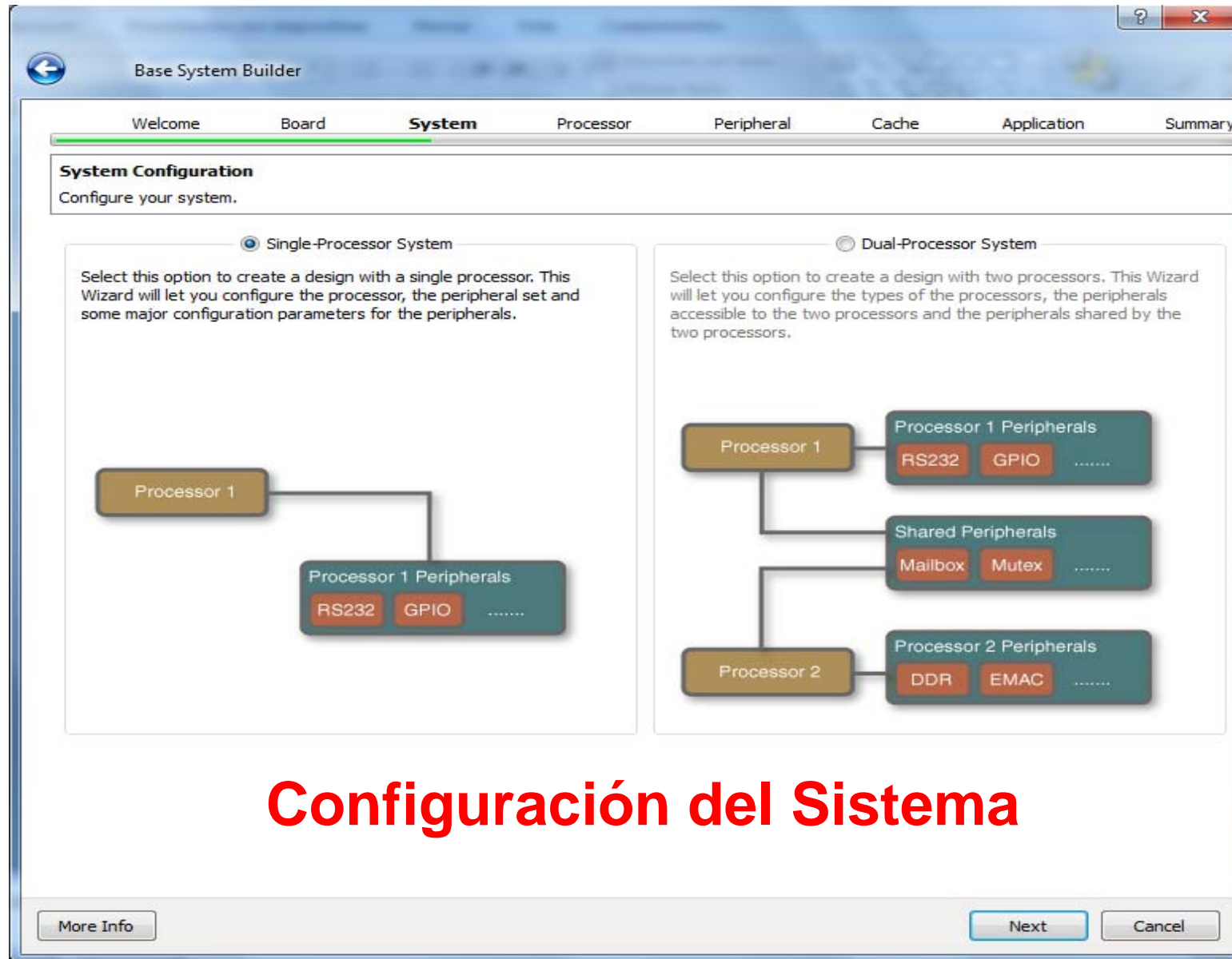
[More Info](#) [Next](#)

Placa personalizada

Spartan-3 Starter Board
Spartan-3A DSP 1800A Starter Board
Spartan-3A DSP 3400A Development Board
Spartan-3A Starter Kit
Spartan-3AN Starter Kit
Spartan-3E 1600E MicroBlaze Dev Board
Spartan-3E Starter Board
Spartan-6 SP601 Evaluation Platform
Spartan-6 SP605 Evaluation Platform
Virtex 4 ML403 Evaluation Platform
Virtex 4 ML405 Evaluation Platform



2.- Sistema (single o dual processor)



Configuración del Sistema

3.- Configuración del procesador

Base System Builder

Welcome Board System **Processor** Peripheral Cache Application Summary

Processor Configuration
Configure the processor(s).

Reference Clock Frequency 50.00 MHz

Processor 1 Configuration

Processor Type MicroBlaze

System Clock Frequency 50.00 MHz

Local Memory 8 KB

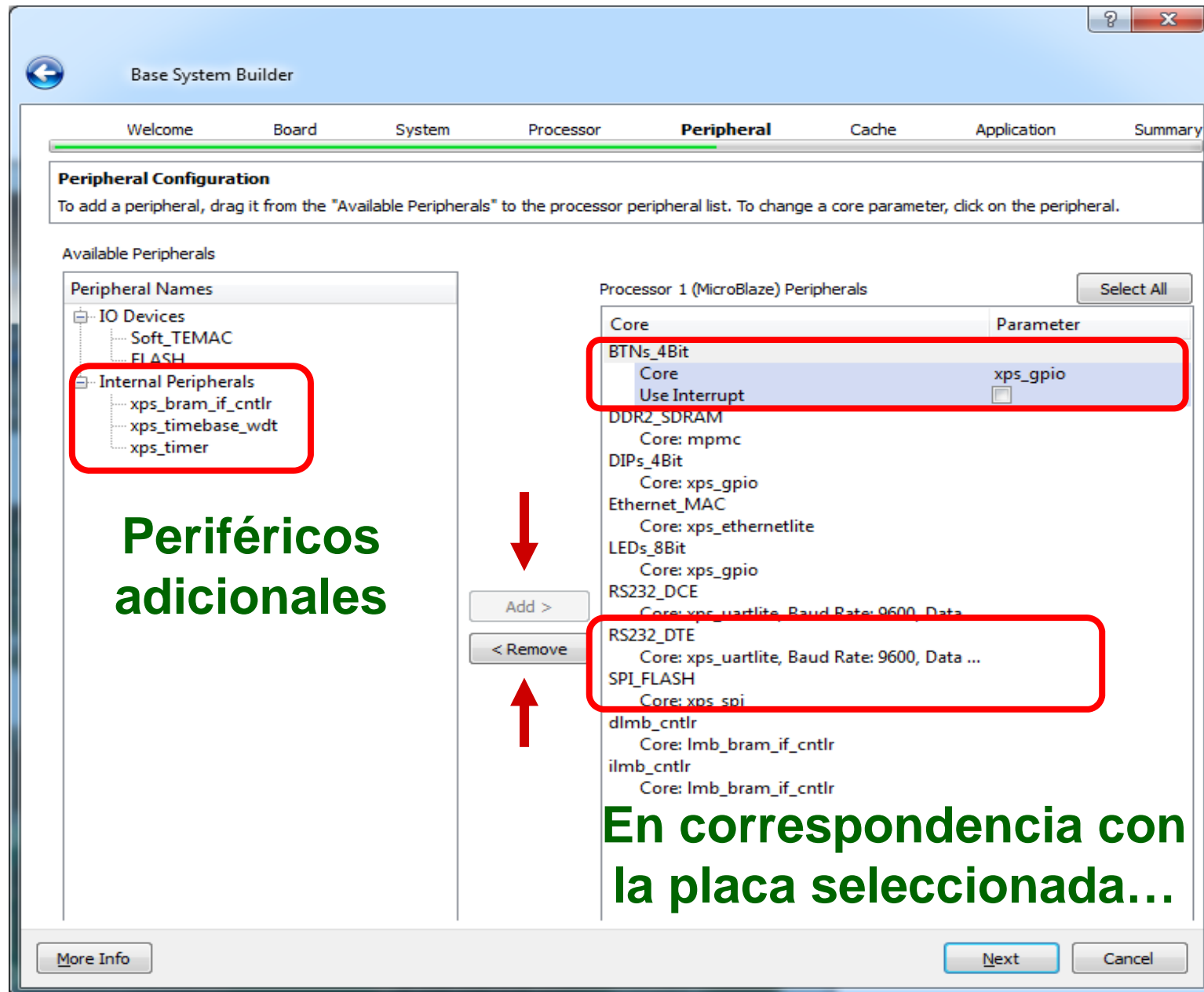
Debug Interface On-Chip HW Debug Module

☐ Enable Floating Point Unit

- Frecuencia de reloj de referencia
- Procesador (MicroBlaze o PPC)
- Frecuencia de reloj del procesador
- Tamaño de Memoria Local
- Interfaz de depuración (implícita)
- Habilitación de FPU (opcional)

More Info Next Cancel

4.- Selección de periféricos



5.- [Configuración de Cache]

Base System Builder

Welcome Board System Processor Peripheral **Cache** Application Summary

Cache Configuration
Select cache size and cache memory for processor(s).

Processor 1 (MicroBlaze) Cache
In MicroBlaze, caches are optional and configurable. Caches are implemented using FPGA LUTs for small caches or Block RAMs for large sized caches.

☒ Instruction Cache
Instruction Cache Size: 2 KB

☒ Data Cache
Data Cache Size: 4 KB

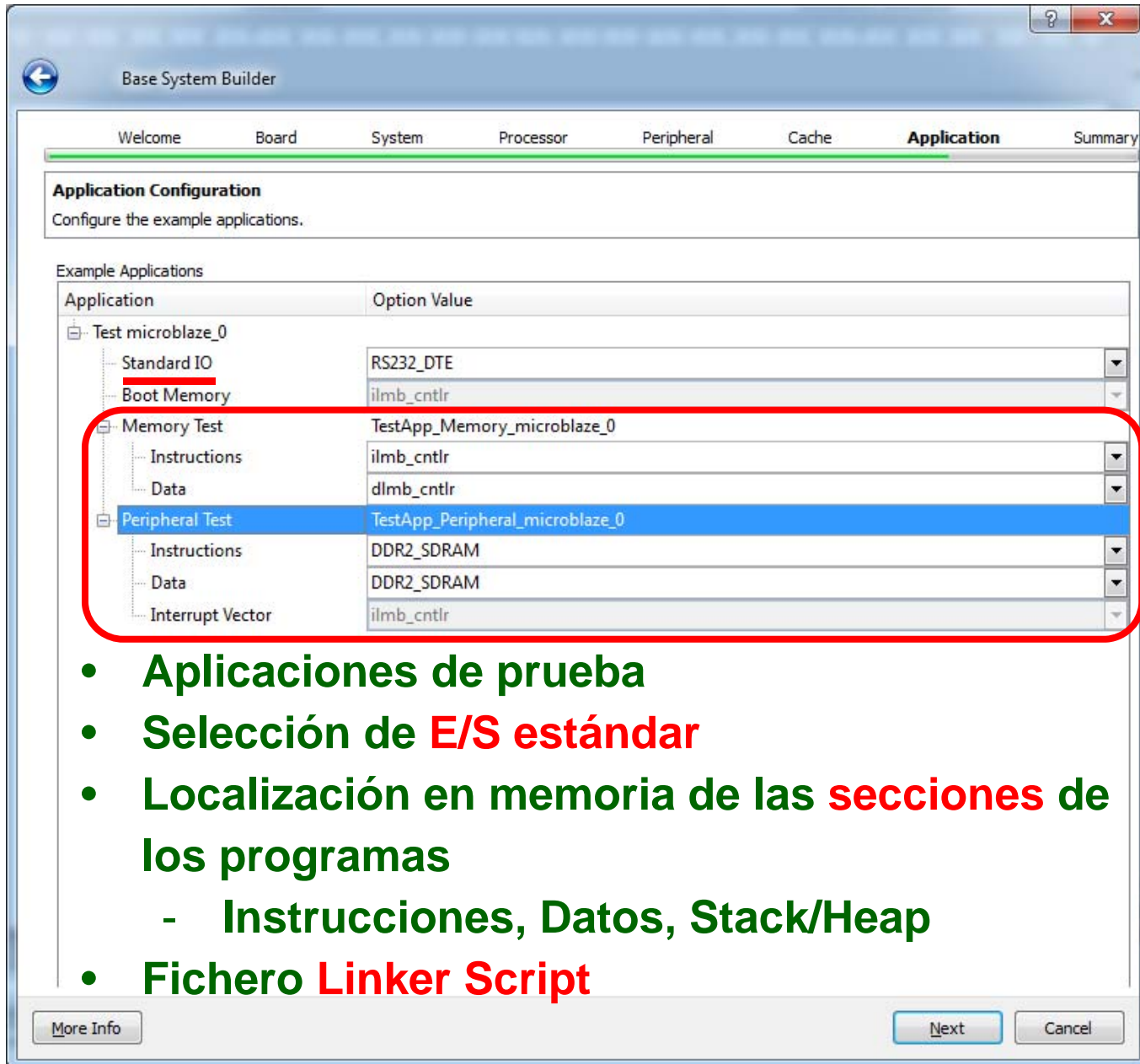
Instruction Cache Memory
☒ DDR2_SDRAM

Data Cache Memory
☒ DDR2_SDRAM

More Info Next Cancel

- Sólo si existe memoria externa
- Caches separadas e independientes
- Correspondencia directa

6.- Configuración software



Base System Builder

Welcome Board System Processor Peripheral Cache **Application** Summary

Application Configuration
Configure the example applications.

Example Applications

Application	Option Value
Test microblaze_0	
Standard IO	RS232_DTE
Boot Memory	ilmb_cntlr
Memory Test	TestApp_Memory_microblaze_0
Instructions	ilmb_cntlr
Data	dlmb_cntlr
Peripheral Test	TestApp_Peripheral_microblaze_0
Instructions	DDR2_SDRAM
Data	DDR2_SDRAM
Interrupt Vector	ilmb_cntlr

- Aplicaciones de prueba
- Selección de **E/S estándar**
- Localización en memoria de las **secciones** de los programas
 - Instrucciones, Datos, Stack/Heap
- Fichero **Linker Script**

More Info Next Cancel

7.- Resumen del sistema

Base System Builder

Welcome Board System Processor Peripheral Cache Application **Summary**

Summary

Below is the summary of the system you are creating.

System Summary

Core Name	Instance Name	Base Address	High Address
Processor1	microblaze_0		
xps_gpio	BTN5_4Bit	0x81440000	0x8144FFFF
mpmc	DDR2_SDRAM	0x44000000	0x47FFFFFF
xps_gpio	DIPs_4Bit	0x81420000	0x8142FFFF
xps_gpio	LEDs_8Bit	0x81400000	0x8140FFFF
xps_uartlite	RS232_DCE	0x84020000	0x8402FFFF
xps_uartlite	RS232_DTE	0x84000000	0x8400FFFF
lmb_bram_if_cntlr	dlmb_cntlr	0x00000000	0x00003FFF
lmb_bram_if_cntlr	ilmb_cntlr	0x00000000	0x00003FFF

File Location

- Overall
 - D:\kkkk\system.xmp
 - D:\kkkk\system.mhs
 - D:\kkkk\system.mss
 - D:\kkkk\data\system.ucf
 - D:\kkkk\etc\fast_runtime.opt
 - D:\kkkk\etc\download.cmd
 - D:\kkkk\etc\bitgen.ut
 - TestApp_Memory_microblaze_0
 - TestApp_Peripheral_microblaze_0

Resumen del HW del sistema de procesamiento

Localización de ficheros relevantes

Ficheros de opciones y comandos

More Info Finish Cancel

Xilinx Platform Studio (XPS)

The screenshot displays the Xilinx Platform Studio (XPS) interface in the System Assembly View. The main window is titled "Xilinx Platform Studio - D:\kkkk\system.xmp - [System Assembly View]". The interface includes a menu bar (File, Edit, View, Project, Hardware, Software, Device Configuration, Debug, Simulation, Window, Help) and a toolbar with various icons.

On the left, the "Project" panel shows the "Platform" section with "Project Files" (MHS File: system.mhs, MSS File: system.mss, UCF File: data/system.ucf, iMPACT Command File: etc/download, Implementation Options File: etc/fast, Bitgen Options File: etc/bitgen.ut) and "Project Options" (Device: xc3s700afg484-4, Netlist: TopLevel, Implementation: XPS (Xflow), HDL: VHDL, Sim Model: BEHAVIORAL). Below this is the "Design Summary" section.

The central area shows a block diagram with components connected by lines. A legend at the bottom of this area defines symbols: Master (blue square), Slave (blue circle), Master/Slave (blue diamond), Target (purple triangle), Initiator (pink triangle), Connected (blue circle), Unconnected (light blue circle), Monitor (green square), Production (yellow star), License (paid) (orange star), License (eval) (light orange star), Local (blue star), Pre Production (light blue star), Beta (light blue star), and Development (light blue star). Below the legend are tabs for "Start Up Page", "Design Summary", "Block Diagram", and "System Assembly View".

On the right, the "Bus Interfaces" panel is active, showing a table of components:

Name	Bus Name	IP Type	IP Version
dmb		lmb_v10	1.00.a
ilmb		lmb_v10	1.00.a
mb_plb		plb_v46	1.05.a
microblaze_0		microblaze	8.00.b
lmb_bram		bram_block	1.00.a
dmb_cntlr		lmb_bram_i...	2.10.b
ilmb_cntlr		lmb_bram_i...	2.10.b
DDR2_SDRAM		mpmc	6.02.a
mdm_0		mdm	2.00.a
BTNs_4Bit		xps_gpio	2.00.a
DIPs_4Bit		xps_gpio	2.00.a
LEDs_8Bit		xps_gpio	2.00.a
RS232_DCE		xps_uartlite	1.01.a
RS232_DTE		xps_uartlite	1.01.a
clock_gener...		clock_gene...	4.01.a
proc_sys_re...		proc_sys_re...	3.00.a

Below the table is the "Bus Interface Filters" panel, which allows filtering components by connection (Connected, Unconnected), bus standard (LMB, PLBV46), Xilinx Point To Point (XIL_BRAM, XIL_BSCAN, XIL_MBDEBUG3, XIL_MBTRACE2, XIL_MEMORY_CH...), and interface type (Slaves, Masters, Master Slaves, Monitors, Targets, Initiators).

At the bottom, the "Console" panel shows the following messages:

```
Copied C:/Xilinx/12.4/ISE_DS/EDK/data/xflow/bitgen_spartan3a.ut to etc directory
Generated Block Diagram.
Diagram Controls
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
```

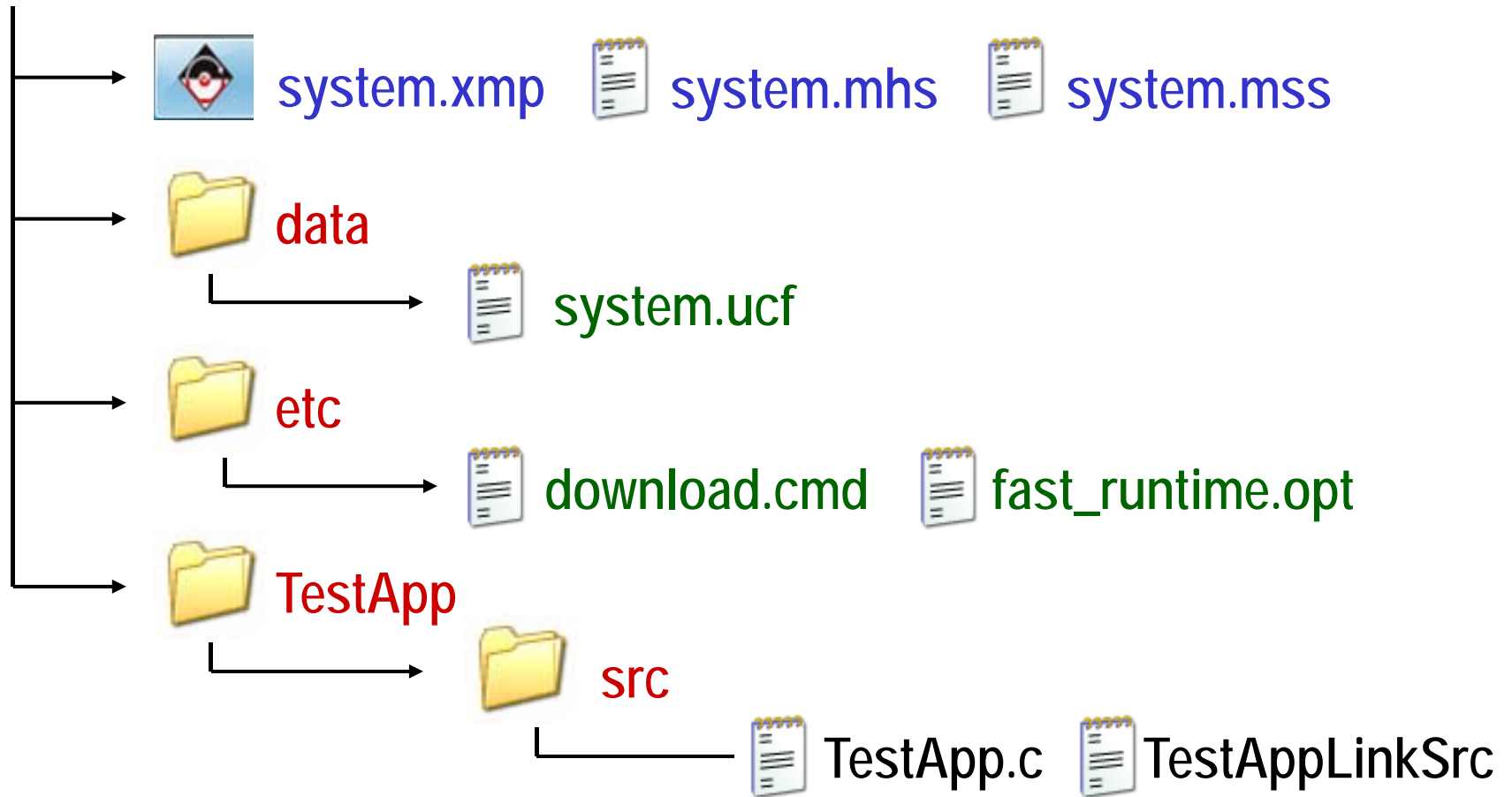
The bottom of the console panel has tabs for "Console", "Warnings", and "Errors".

Overlaid text labels identify key areas: "Proyecto, Aplicaciones SW, Módulos IP" (Project, SW Applications, IP Modules) points to the Project panel; "Conexiones" (Connections) points to the block diagram; "HW del sistema MB" (MB system HW) points to the Bus Interfaces table; "Panel de Filtro" (Filter Panel) points to the Bus Interface Filters panel; and "Consola de Mensajes" (Message Console) points to the Console panel.

Estructura del proyecto

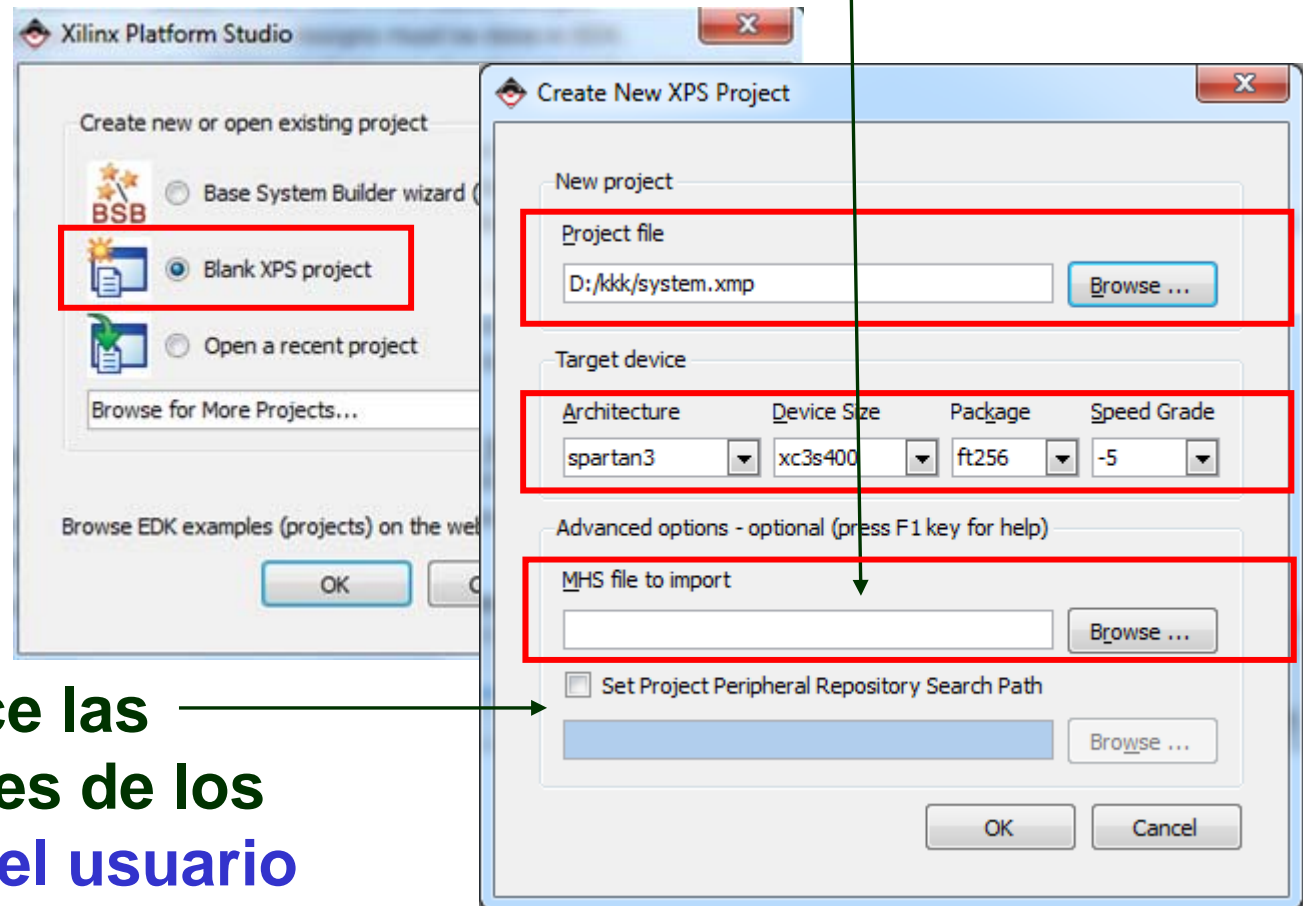
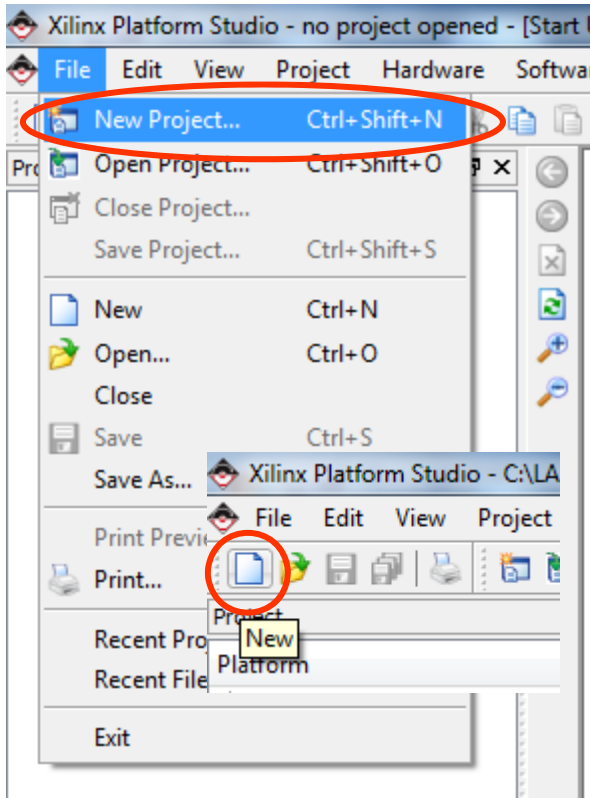


Directorio_del_proyecto



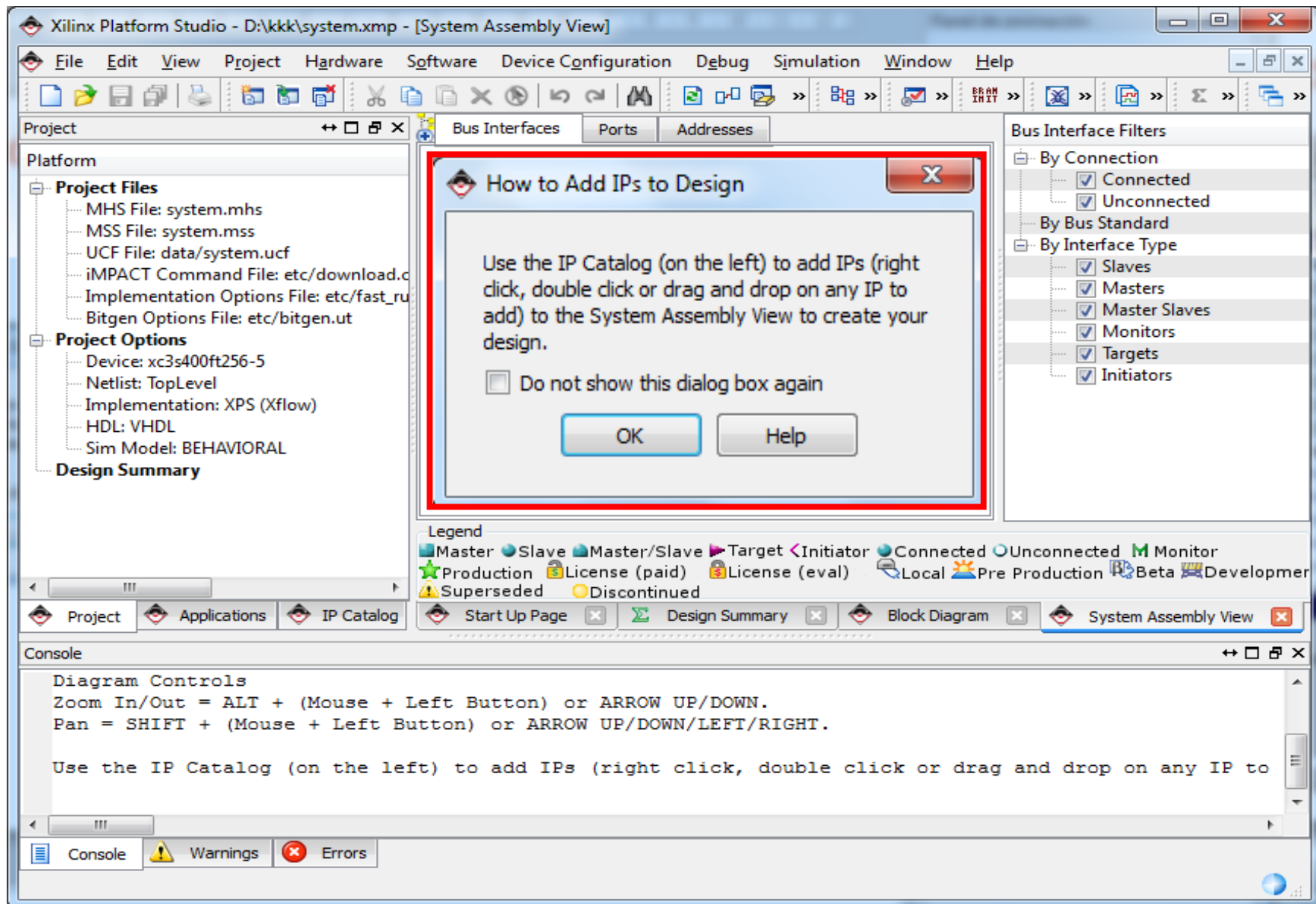
Creación de proyectos con *Platform Studio*

Puede **importarse** un **fichero** de especificación de hardware MHS



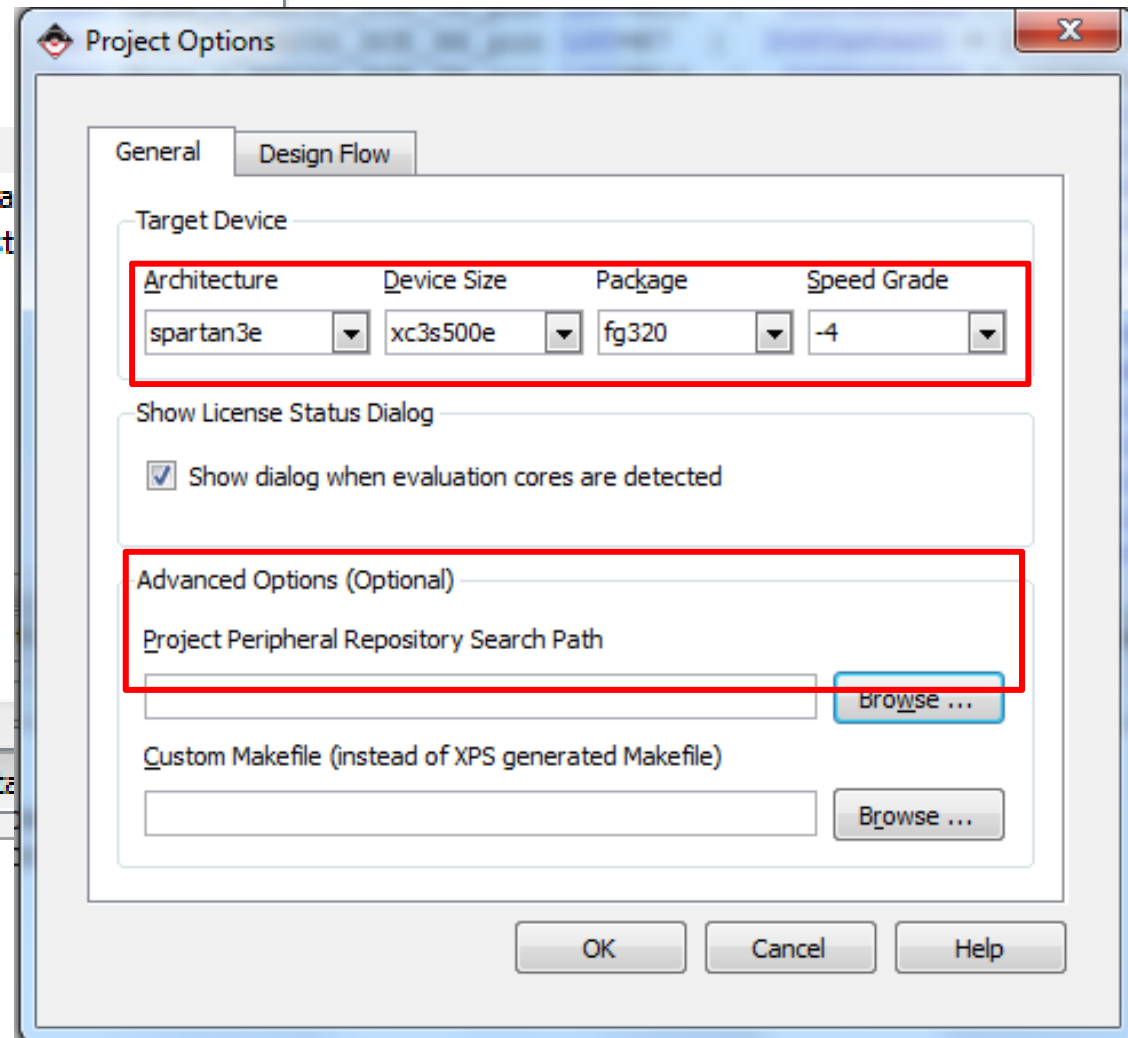
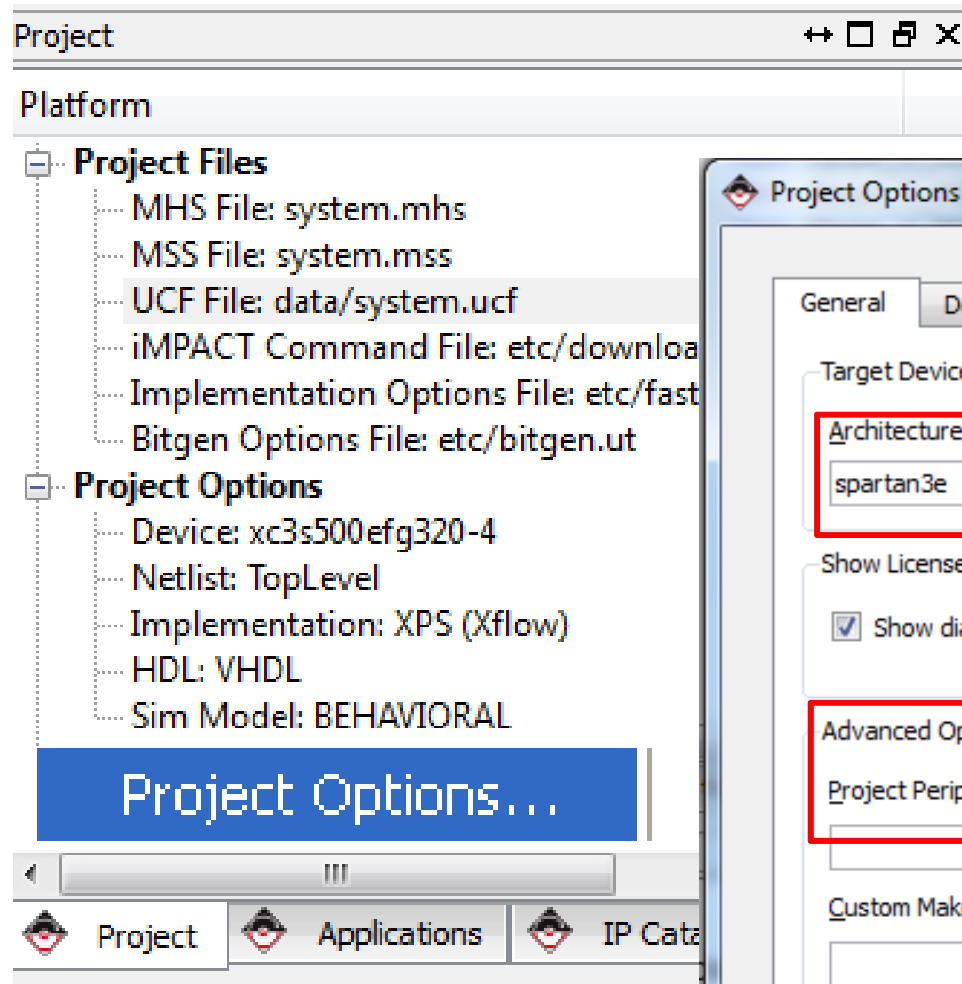
Establece las localizaciones de los módulos IP del usuario

Creación de un proyecto desde cero

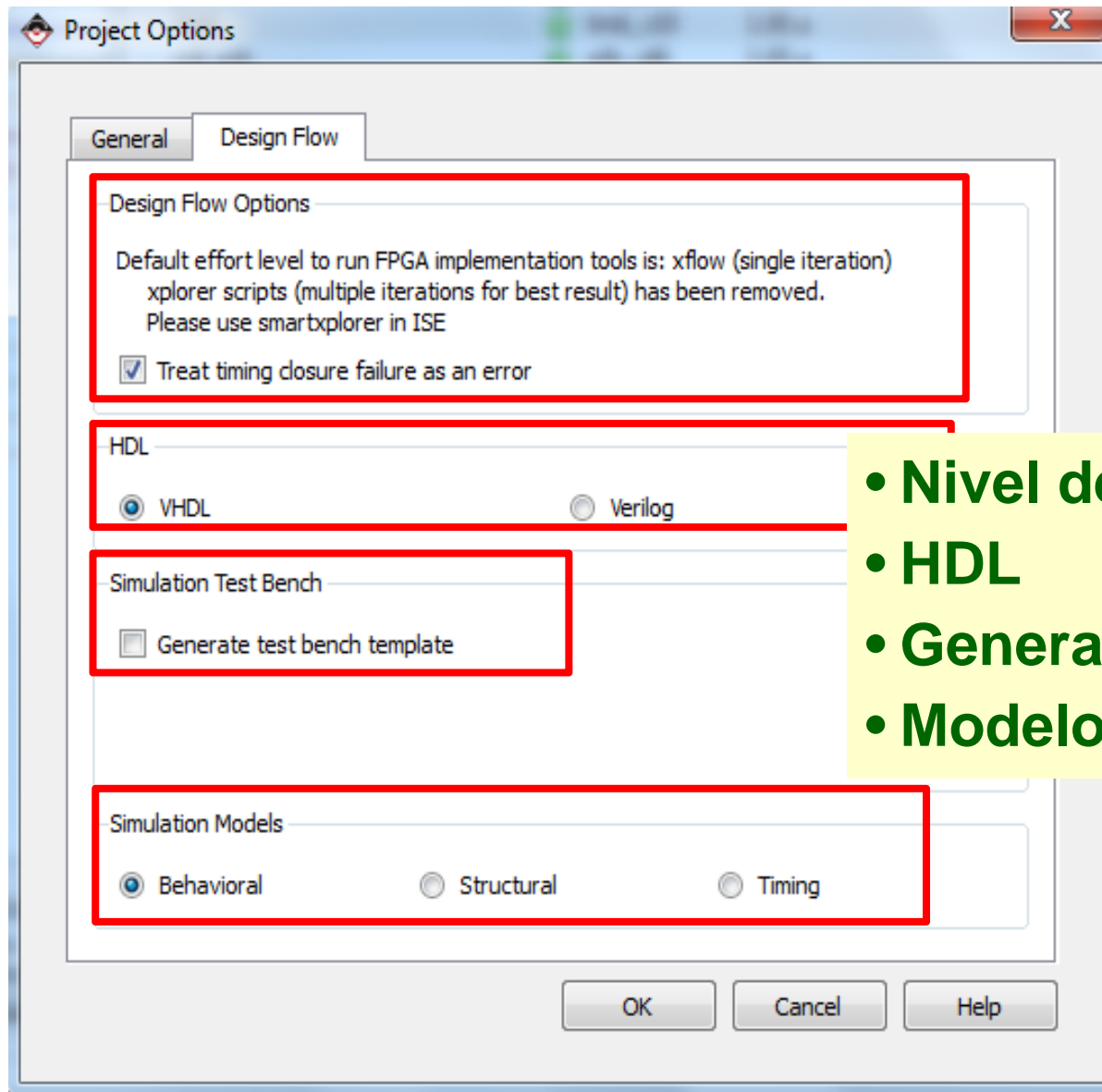


Proyecto (Project Tab)

Opciones generales

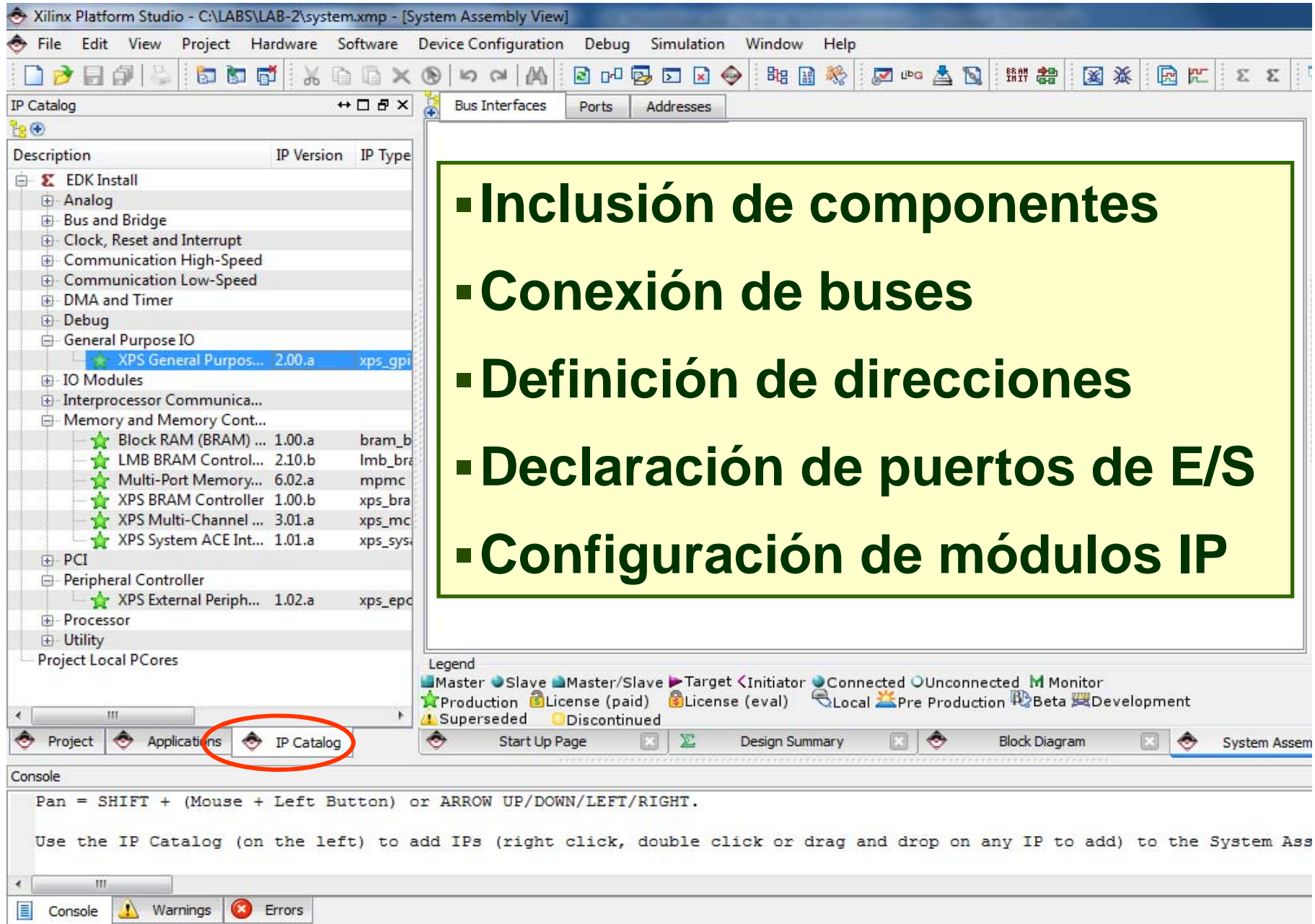


Opciones del flujo de diseño



- Nivel de esfuerzo de xflow
- HDL
- Generación de testbench
- Modelo de simulación

Especificación hardware de la plataforma



The screenshot displays the Xilinx Platform Studio interface. The 'IP Catalog' pane on the left lists various IP components under the 'EDK Install' tree. The 'XPS General Purpos...' component is highlighted. The 'Console' pane at the bottom shows instructions for using the IP Catalog.

IP Catalog

Description	IP Version	IP Type
EDK Install		
Analog		
Bus and Bridge		
Clock, Reset and Interrupt		
Communication High-Speed		
Communication Low-Speed		
DMA and Timer		
Debug		
General Purpose IO		
XPS General Purpos...	2.00.a	xps_gpi
IO Modules		
Interprocessor Communica...		
Memory and Memory Cont...		
Block RAM (BRAM) ...	1.00.a	bram_b
LMB BRAM Control...	2.10.b	lmb_br
Multi-Port Memory...	6.02.a	mpmc
XPS BRAM Controller	1.00.b	xps_bra
XPS Multi-Channel ...	3.01.a	xps_mc
XPS System ACE Int...	1.01.a	xps_sys
PCI		
Peripheral Controller		
XPS External Periph...	1.02.a	xps_epc
Processor		
Utility		
Project Local PCores		

Legend

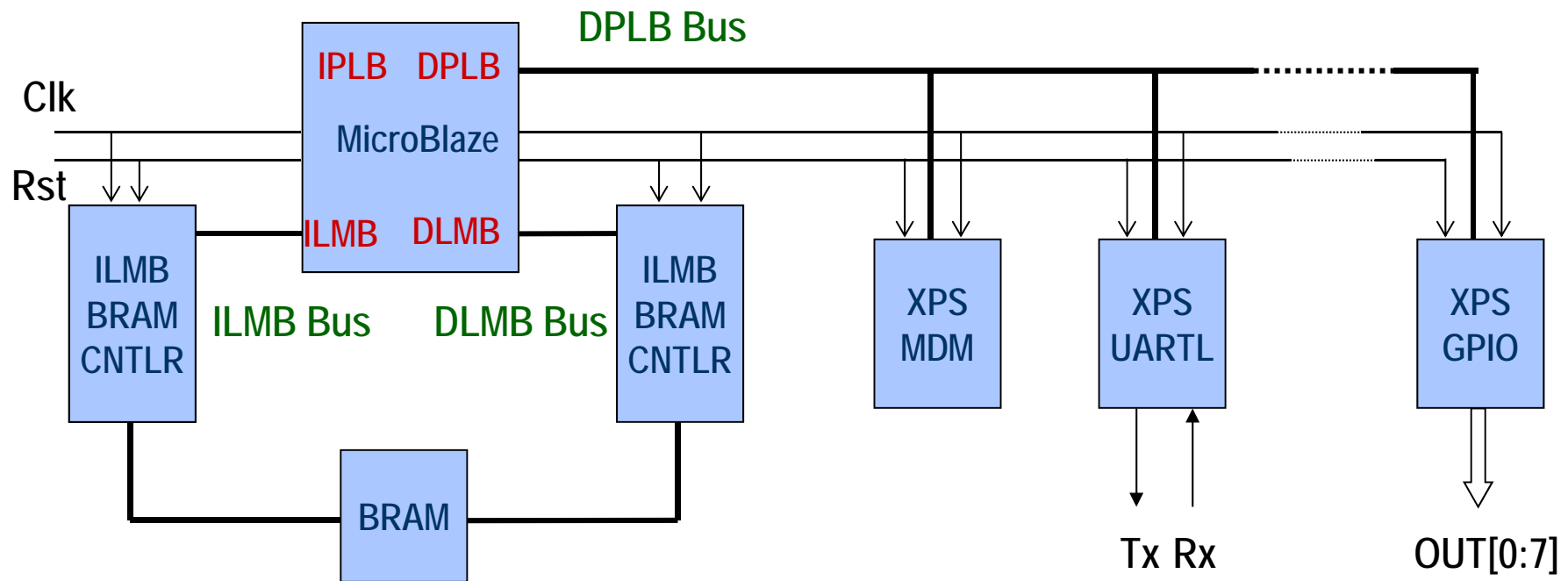
- Master (blue circle)
- Slave (blue circle)
- Master/Slave (blue circle)
- Target (purple circle)
- Initiator (pink circle)
- Connected (blue circle)
- Unconnected (blue circle)
- Monitor (green circle)
- Production (green star)
- License (paid) (yellow star)
- License (eval) (yellow star)
- Local (blue star)
- Pre Production (blue star)
- Beta (blue star)
- Development (blue star)
- Superseded (yellow star)
- Discontinued (yellow star)

Console

```
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
```

Use the IP Catalog (on the left) to add IPs (right click, double click or drag and drop on any IP to add) to the System Ass

Especificación hardware de la plataforma



1.- Inclusión de componentes (IP Catalog)

The image shows the Xilinx Platform Studio interface with the IP Catalog and the MicroBlaze Configuration Wizard open.

IP Catalog: The IP Catalog window displays a list of IP blocks. The "MicroBlaze" entry is highlighted with a red box, and a red arrow points to it. A red circle highlights the "Add IP" button in the context menu.

MicroBlaze Configuration Wizard: The wizard is titled "MicroBlaze Configuration Wizard" and shows the "Select configuration:" section. The "Current Settings" option is selected. The "Welcome to MicroBlaze Configuration Wizard" message is displayed. The "Advanced" tab is selected, showing various configuration options like "Frequency", "Area", and "Performance".

Annotations:

- Selección de módulos IP** (Selection of IP modules) - Green text with a red arrow pointing to the MicroBlaze entry in the IP Catalog.
- Configuración del módulo IP** (IP module configuration) - Red text at the bottom of the wizard window.

1.- Inclusión de componentes (IP Catalog)

Asignación de nombres

Name	Bus Na	IP Type	IP Version
microblaze_0		microblaze	8.00.b
lmb_v10_0		lmb_v10	1.00.a
plb_v46_0		plb_v46	1.05.a
lmb_v10_1		lmb_v10	1.00.a
debug_mod		mdm	2.00.a
LEDS_8bit		xps_gpio	2.00.a
RS232		xps_uartlite	1.01.a

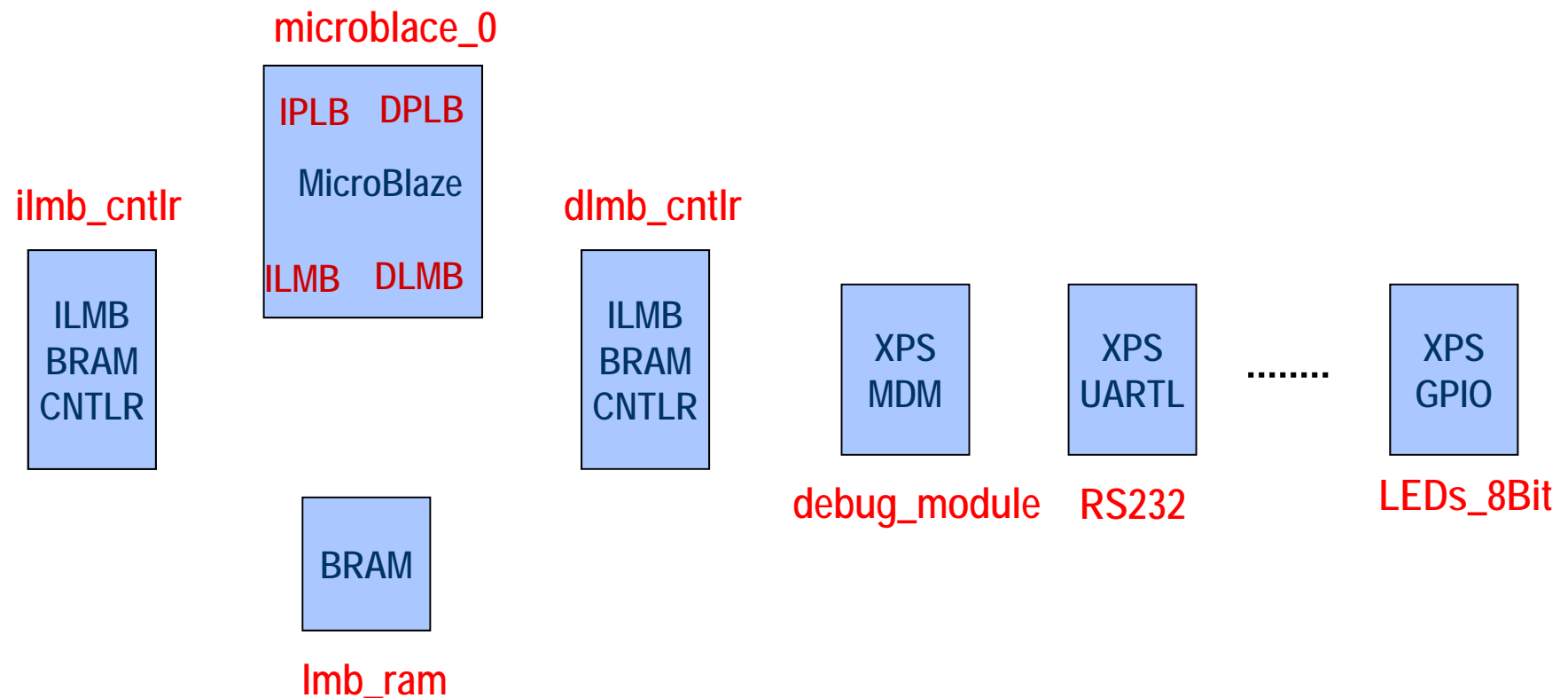
Legend

- Master
- Slave
- Master/Slave
- Target
- Initiator
- Connected
- Unconnected
- Monitor
- Production
- License (paid)
- License (eval)
- Local
- Pre Production
- Beta
- Development
- Superseded
- Discontinued

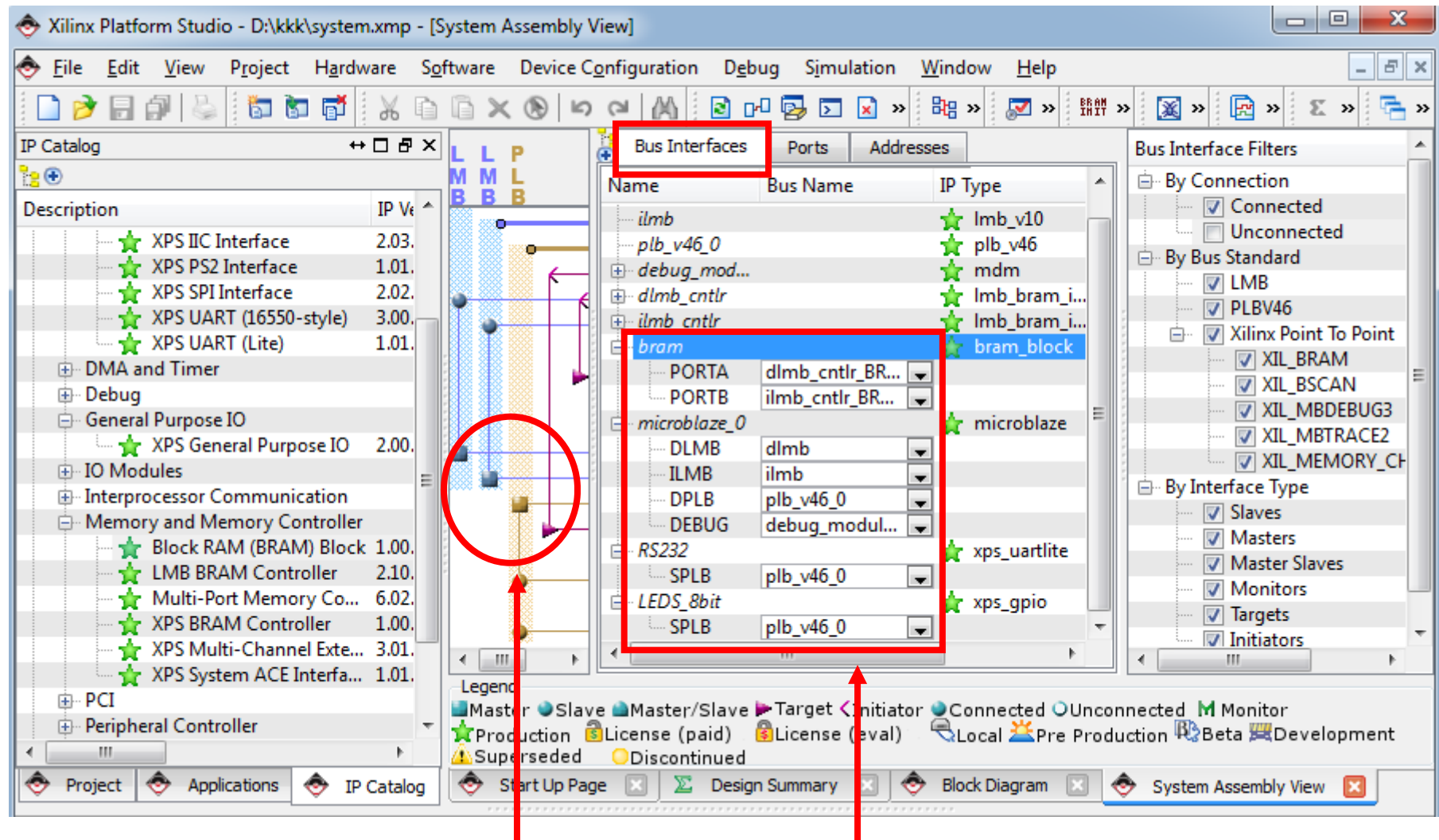
Console

```
WARNING:EDK:2137 - Peripheral LEDS_8bit is not accessible from any processor in the system. Check Bus Int
WARNING:EDK:2137 - Peripheral RS232 is not accessible from any processor in the system. Check Bus Interfa
WARNING:EDK:2137 - Peripheral debug_module_0 is not accessible from any processor in the system. Check Bu
```

1.- Inclusión de componentes



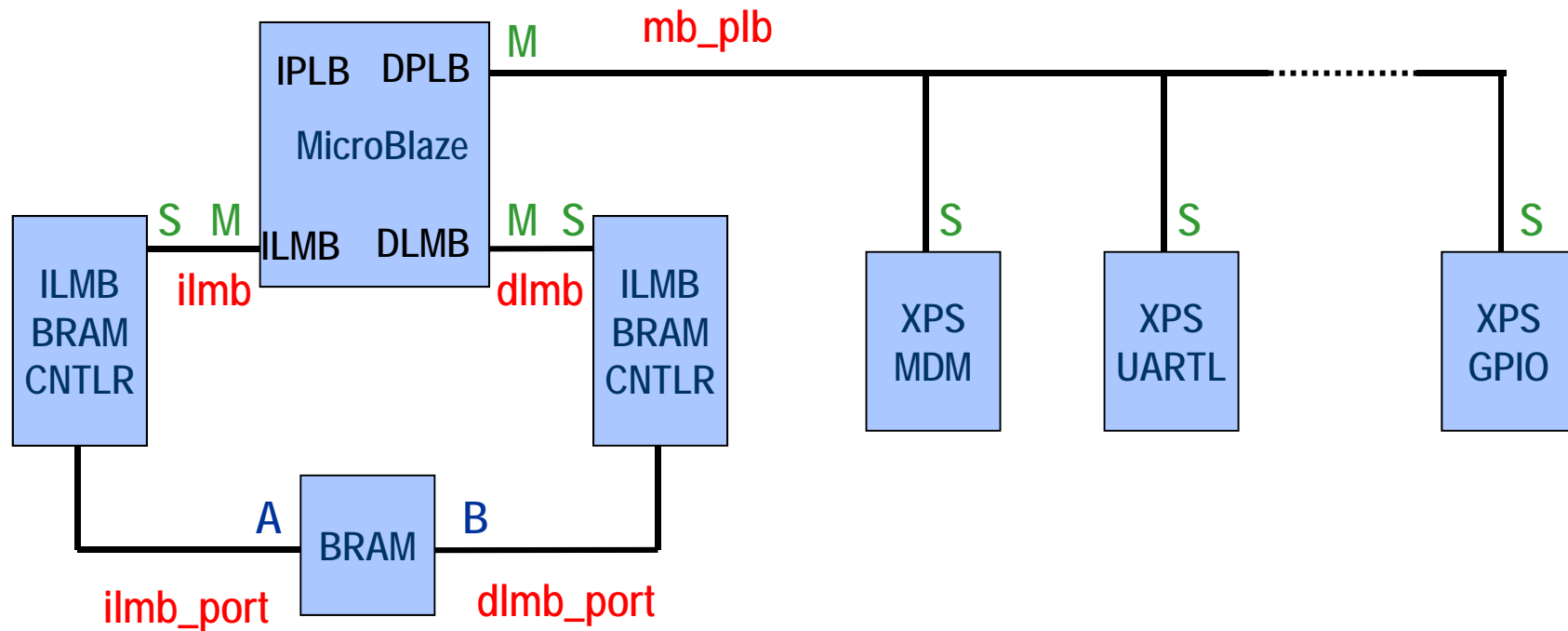
2.- Conexión de buses (*Bus Interfaces*)



Conexión de buses

Conexiones de
módulos IP

2.- Conexión de buses



3.- Definición de direcciones (*Addresses*)

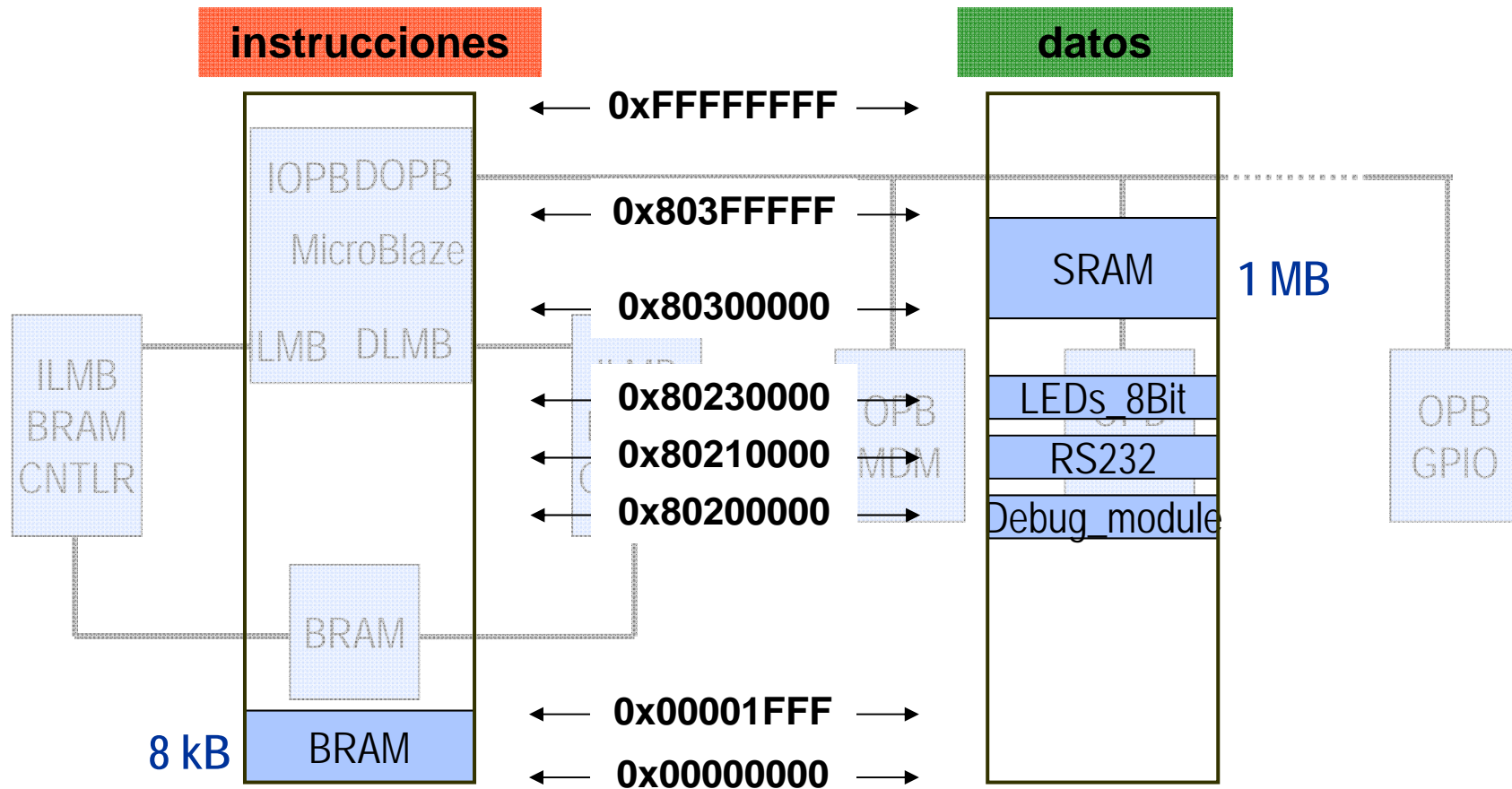
The screenshot shows the Xilinx Platform Studio interface with the 'Addresses' tab selected. The table below lists the addresses for various components in the 'microblaze_0's Address Map'.

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address Map							
dmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	dmb	<input type="checkbox"/>
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	ilmb	<input type="checkbox"/>
Ethernet_MAC	C_BASEADDR	0x81000000	0x8100FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
LEDs_8Bit	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
DIPs_4Bit	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
BTNs_4Bit	C_BASEADDR	0x81440000	0x8144FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
SPL_FLASH	C_BASEADDR	0x83400000	0x8340FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
RS232_DTE	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
RS232_DCE	C_BASEADDR	0x84020000	0x8402FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
DDR2_SDRAM	C_MPMC_BASE	0x8C000000	0x8FFFFFFF	64M	SPLB0		<input type="checkbox"/>

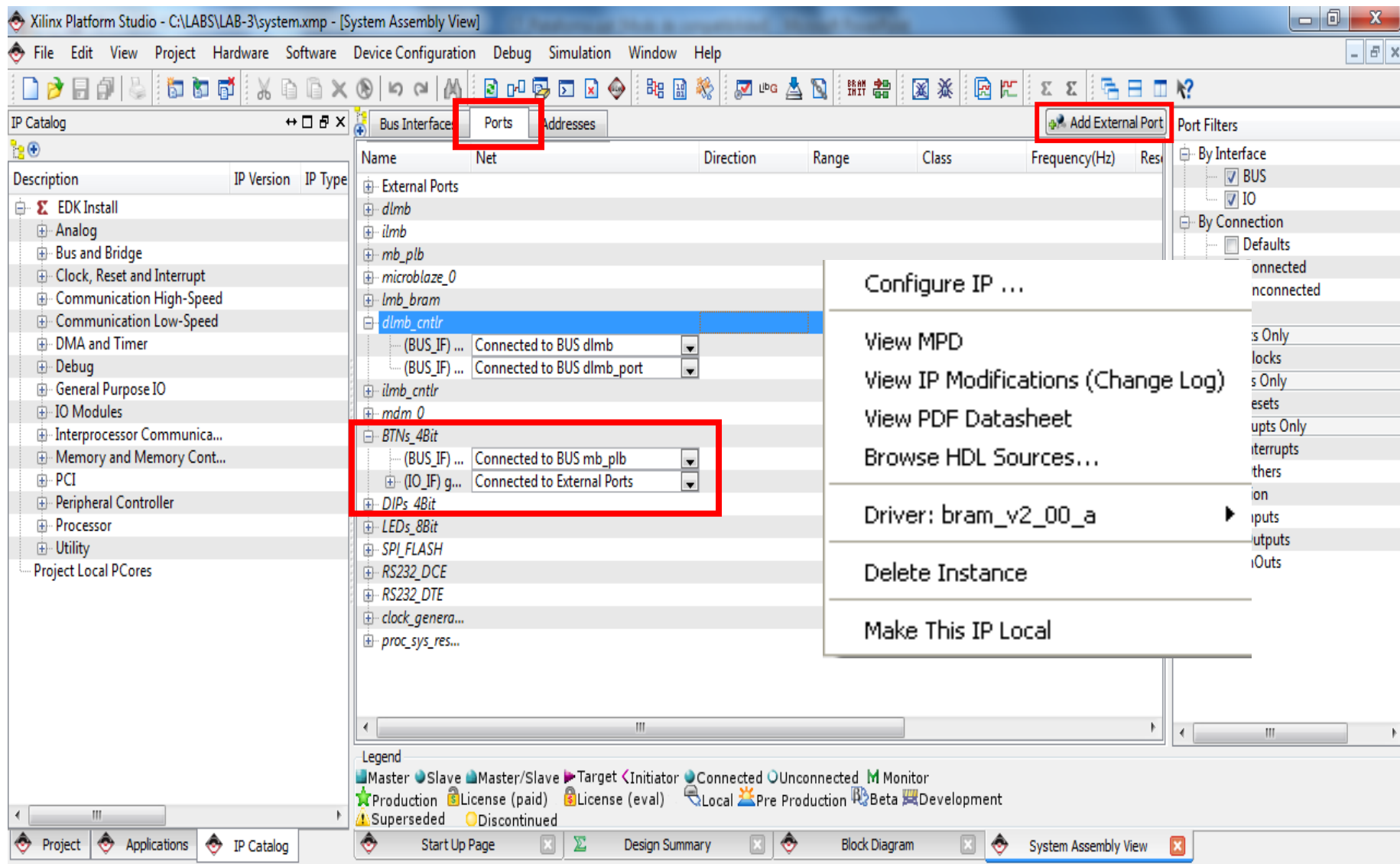
Definición manual del espacio de direcciones

Generación automática

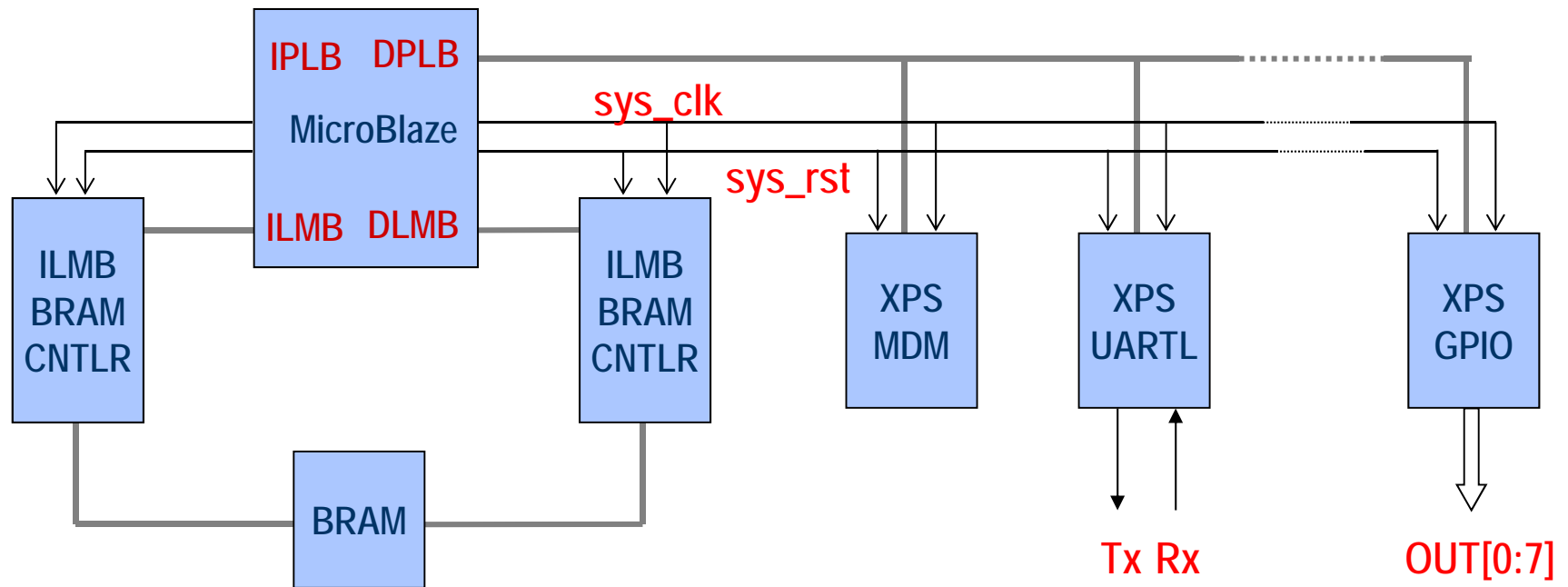
3.- Definición de direcciones



4.- Declaración de puertos de E/S (*Ports*)



4.- Declaración de puertos de E/S



5.- Configuración de módulos (*Parámetros*)

The screenshot displays the Xilinx Platform Studio interface. On the left, the IP Catalog is visible, showing a tree of IP blocks. The central pane shows a system assembly diagram with various IP blocks connected. On the right, a table lists the IP blocks and their properties.

Name	Bus Name	IP Type	IP Version
dLmb		lmb_v10	1.00.a
ilmb		lmb_v10	1.00.a
mb_plb		plb_v46	1.05.a
microblaze_0		microblaze	8.00.b
lmb_bram		bram_block	1.00.a
dLmb_cntlr		lmb_bram_i...	2.10.b
ilmb_cntlr		lmb_bram_i...	2.10.b
mdm_0			
BTNs_4Bit			
DIPs_4Bit			
LEDs_8Bit			
SPI_FLASH			
RS232_DCE			
RS232_DTE			
clock_gener...			
proc_sys_re...			

A context menu is open over the 'LEDs_8Bit' block, showing the following options:

- Configure IP ...
- View MPD
- View IP Modifications (Change Log)
- View PDF Datasheet
- Browse HDL Sources...
- Driver: gpio_v3_00_a
- Delete Instance
- Make This IP Local

Parámetros de configuración de módulos IP

system.mhs

Microprocessor Hardware
Specification

Processor IP
MPD Files

Microprocessor Peripheral
Definitions

```
BEGIN opb_uartlite
  PARAMETER INSTANCE = myuart
  PARAMETER HW_VER = 1.00.b
  PARAMETER C_DATA_BITS = 8
  PARAMETER C_CLK_FREQ = 100000000
  PARAMETER C_BAUDRATE = 9600
  PARAMETER C_USE_PARITY = 0
  PARAMETER C_ODD_PARITY = 1
  PARAMETER C_BASEADDR = 0x00010000
  PARAMETER C_HIGHADDR = 0x000100FF
  PORT OPB_Clk = sys_clk
  PORT OPB_Rst = peripheral_rst
  PORT RX = rx
  PORT TX = tx
  BUS_INTERFACE SOPB = myopb
END
```

Sobrescribe los valores
definidos en el fichero MPD

```
OPTION SIM_MODELS = BEHAVIORAL : STRUCTURAL

BUS_INTERFACE BUS=SOPB, BUS_STD=OPB, BUS_TYPE=SLAVE

# Generics for vhdl or parameters for verilog
PARAMETER C_BASEADDR = 0xFFFF8000, DT=std_logic_vector
PARAMETER C_HIGHADDR = 0xFFFF80FF, DT=std_logic_vector
PARAMETER C_OPB_DWIDTH = 32, DT=integer
PARAMETER C_OPB_AWIDTH = 32, DT=integer
PARAMETER C_DATA_BITS = 8, DT="integer range 5 to 8"
PARAMETER C_CLK_FREQ = 125_000_000, DT=integer
PARAMETER C_BAUDRATE = 9600, DT=integer
PARAMETER C_USE_PARITY = 1, DT=integer
PARAMETER C_ODD_PARITY = 1, DT=integer
```

Contiene los valores por defecto
de todos los parámetros



Fichero MHS (Project Tab)

The screenshot displays the 'Project' tab in a software interface. On the left, the 'Project Files' list includes:

- MHS File: system.mhs
- MSS File: system.mss
- UCF File: data/system.ucf
- iMPACT Command File: etc/downl...
- Implementation Options File: etc/fa...
- Bitgen Op...

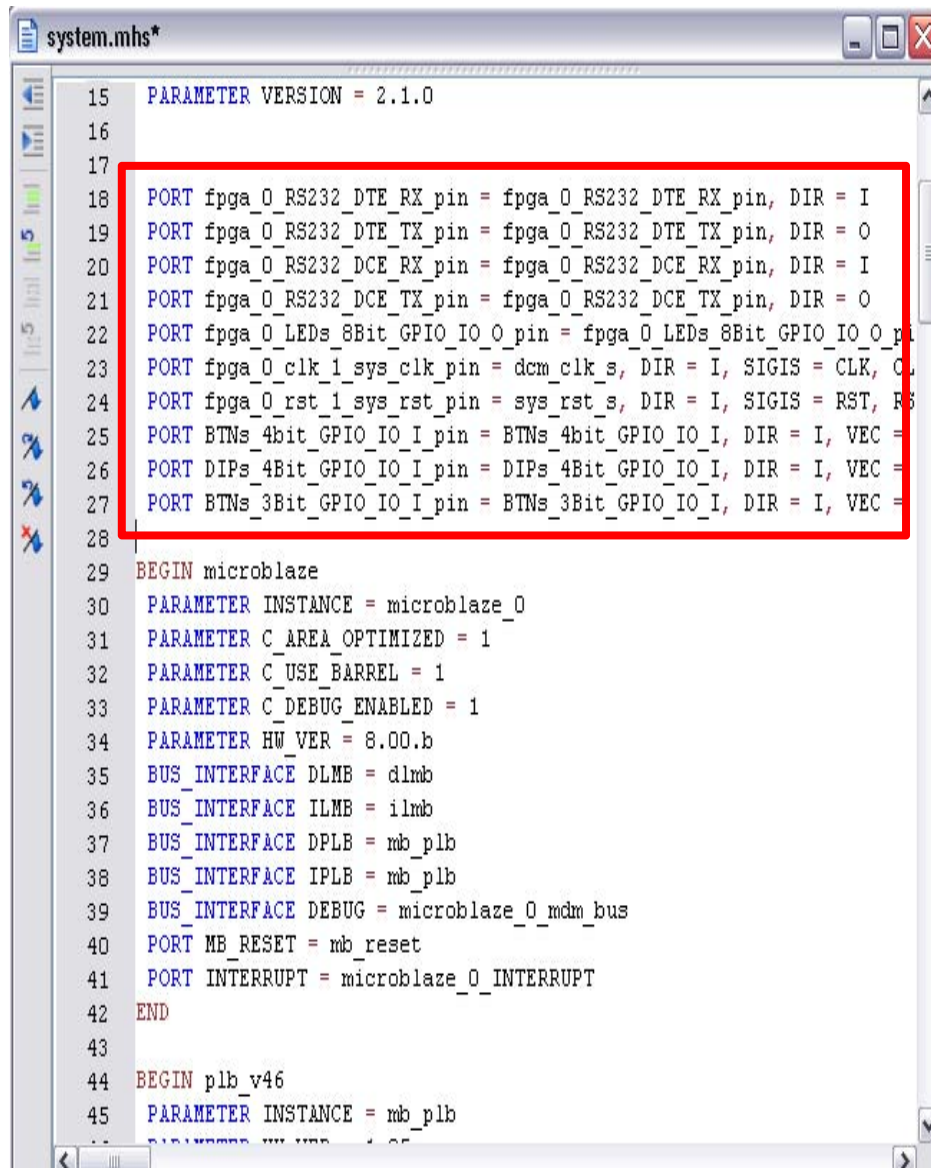
Below this list, the 'Project Options' section is visible, with a blue 'Open' button highlighted over the 'Device: xc...' entry. Other options include 'Netlist: TopLevel', 'Implementation: XPS (Xflow)', 'HDL: VHDL', and 'Sim Model: BEHAVIORAL'. The 'Design Summary' section is also present.

At the bottom of the interface, there are three tabs: 'Project', 'Applications', and 'IP Ca...'. The 'Project' tab is currently selected.

The main window displays the content of the 'system.mhs' file, which is a VHDL configuration file. The code is as follows:

```
114
115 BEGIN xps_uartlite
116     PARAMETER INSTANCE = RS232_DCE
117     PARAMETER C_BAUDRATE = 9600
118     PARAMETER C_DATA_BITS = 8
119     PARAMETER C_USE_PARITY = 0
120     PARAMETER C_ODD_PARITY = 0
121     PARAMETER HW_VER = 1.01.a
122     PARAMETER C_BASEADDR = 0x84020000
123     PARAMETER C_HIGHADDR = 0x8402ffff
124     BUS_INTERFACE SPLB = mb_plb
125     PORT RX = fpga_0_RS232_DCE_RX_pin
126     PORT TX = fpga_0_RS232_DCE_TX_pin
127 END
128
129 BEGIN xps_gpio
130     PARAMETER INSTANCE = LEDs_8Bit
131     PARAMETER C_ALL_INPUTS = 0
132     PARAMETER C_GPIO_WIDTH = 8
133     PARAMETER C_INTERRUPT_PRESENT = 0
134     PARAMETER C_IS_DUAL = 0
135     PARAMETER HW_VER = 2.00.a
136     PARAMETER C_BASEADDR = 0x81400000
137     PARAMETER C_HIGHADDR = 0x8140ffff
138     BUS_INTERFACE SPLB = mb_plb
139     PORT GPIO_IO_O = fpga_0_LEDs_8Bit_GPIO_IO_O
140 END
```


Fichero de especificaciones de hardware



```
15  PARAMETER VERSION = 2.1.0
16
17
18  PORT fpga_0_RS232_DTE_RX_pin = fpga_0_RS232_DTE_RX_pin, DIR = I
19  PORT fpga_0_RS232_DTE_TX_pin = fpga_0_RS232_DTE_TX_pin, DIR = O
20  PORT fpga_0_RS232_DCE_RX_pin = fpga_0_RS232_DCE_RX_pin, DIR = I
21  PORT fpga_0_RS232_DCE_TX_pin = fpga_0_RS232_DCE_TX_pin, DIR = O
22  PORT fpga_0_LEDs_8Bit_GPIO_IO_0_pin = fpga_0_LEDs_8Bit_GPIO_IO_0_pin
23  PORT fpga_0_clk_1_sys_clk_pin = dcm_clk_s, DIR = I, SIGIS = CLK, CL
24  PORT fpga_0_rst_1_sys_rst_pin = sys_rst_s, DIR = I, SIGIS = RST, R
25  PORT BTNs_4bit_GPIO_IO_I_pin = BTNs_4bit_GPIO_IO_I, DIR = I, VEC =
26  PORT DIPS_4Bit_GPIO_IO_I_pin = DIPS_4Bit_GPIO_IO_I, DIR = I, VEC =
27  PORT BTNs_3Bit_GPIO_IO_I_pin = BTNs_3Bit_GPIO_IO_I, DIR = I, VEC =
28
29  BEGIN microblaze
30  PARAMETER INSTANCE = microblaze_0
31  PARAMETER C_AREA_OPTIMIZED = 1
32  PARAMETER C_USE_BARREL = 1
33  PARAMETER C_DEBUG_ENABLED = 1
34  PARAMETER HW_VER = 8.00.b
35  BUS_INTERFACE DLMB = dlmb
36  BUS_INTERFACE ILMB = ilmb
37  BUS_INTERFACE DPLB = mb_plb
38  BUS_INTERFACE IPLB = mb_plb
39  BUS_INTERFACE DEBUG = microblaze_0_mdm_bus
40  PORT MB_RESET = mb_reset
41  PORT INTERRUPT = microblaze_0_INTERRUPT
42  END
43
44  BEGIN plb_v46
45  PARAMETER INSTANCE = mb_plb
```

- **PORT**

- Fuera de un componente: **señales externas**
- Dentro del componente: **interconexiones**

- **Componentes entre BEGIN y END**

- **PARAMETER:** **parámetros locales del componente**

- **BUS_INTERFACE:**

- Conexión a **buses**

Fichero de especificaciones de hardware

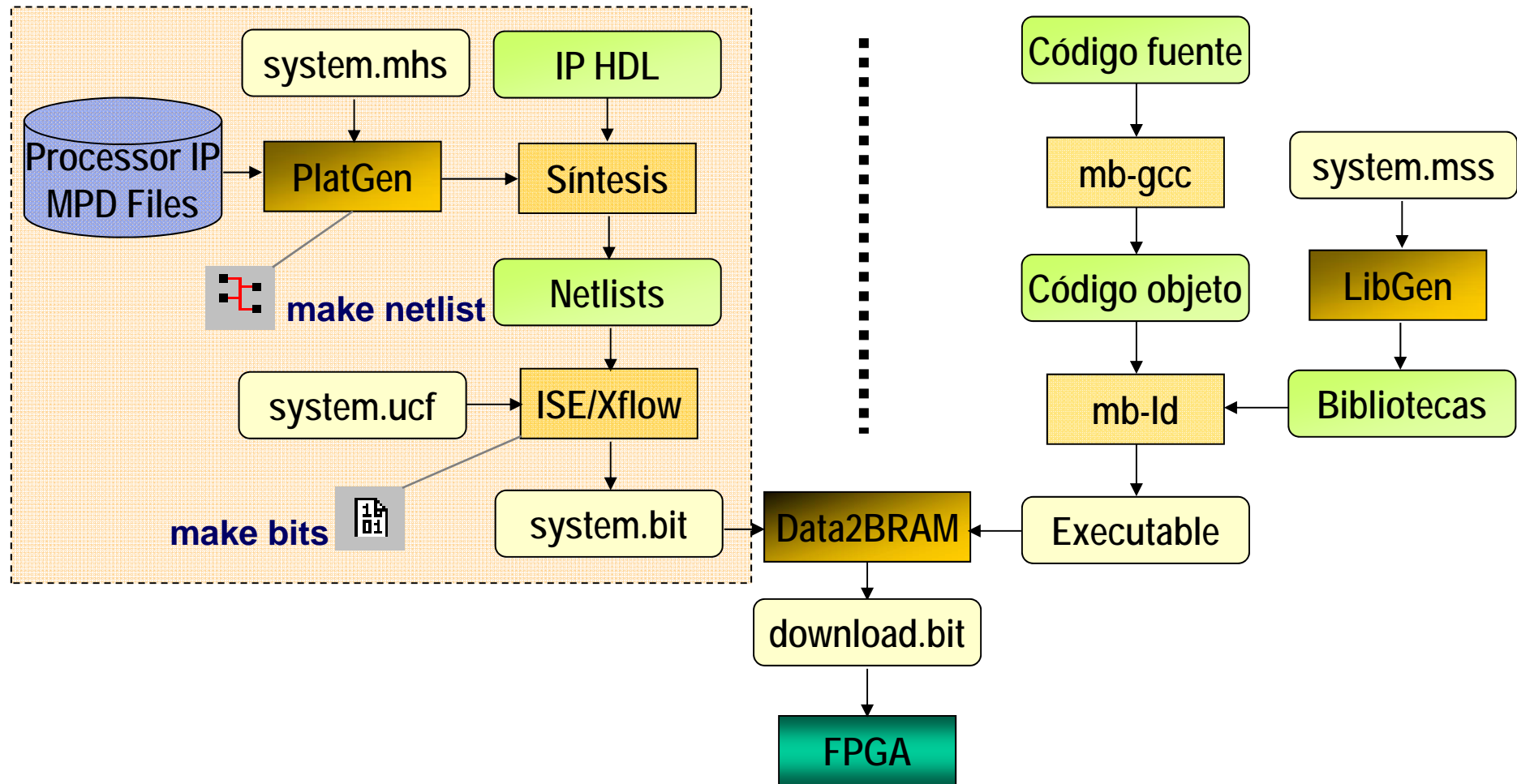
```
75  
76 BEGIN lmb_bram_if_cntlr  
77     PARAMETER INSTANCE = ilmb_cntlr  
78     PARAMETER HW_VER = 2.10.b  
79     PARAMETER C_BASEADDR = 0x00000000  
80     PARAMETER C_HIGHADDR = 0x00001fff  
81     BUS_INTERFACE SLMB = ilmb  
82     BUS_INTERFACE BRAM_PORT = ilmb_port  
83 END  
84  
85 BEGIN bram_block  
86     PARAMETER INSTANCE = lmb_bram  
87     PARAMETER HW_VER = 1.00.a  
88     BUS_INTERFACE PORTA = ilmb_port  
89     BUS_INTERFACE PORTB = dlmb_port  
90 END  
91  
92 BEGIN xps_uartlite  
93     PARAMETER INSTANCE = RS232_DTE  
94     PARAMETER C_BAUDRATE = 9600  
95     PARAMETER C_DATA_BITS = 8  
96     PARAMETER C_USE_PARITY = 0  
97     PARAMETER C_ODD_PARITY = 0  
98     PARAMETER HW_VER = 1.01.a  
99     PARAMETER C_BASEADDR = 0x84000000  
100    PARAMETER C_HIGHADDR = 0x8400ffff  
101    BUS_INTERFACE SPLB = mb_plb  
102    PORT RX = fpga_0_RS232_DTE_RX_pin  
103    PORT TX = fpga_0_RS232_DTE_TX_pin  
104 END
```

→ Direcciones de memoria

→ Versión del IP (HW)

→ Configuración periférico

Creación de la plataforma hardware



Platform Generator (*PlatGen*)

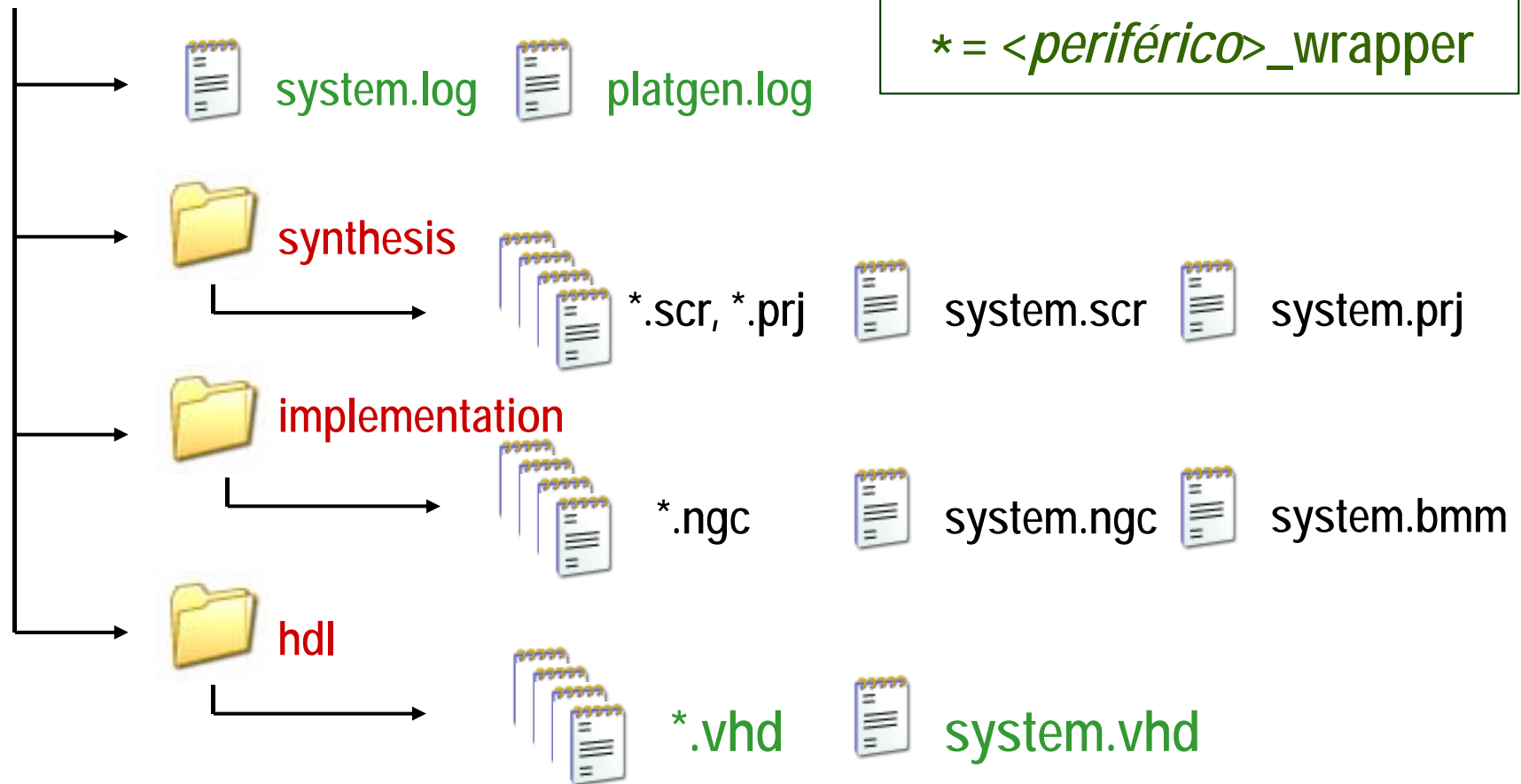
- *PlatGen* crea el hardware de la plataforma a partir de:
 - **Fichero MHS** (*Microprocessor Hardware Specification*)
 - **Ficheros MPD** (*Microprocessor Peripheral Definition*)
- *PlatGen* construye el sistema de procesamiento empujado como un conjunto de listas de conexión de hardware (**ficheros HDL y netlists de implementación**)
- Las salidas de *PlatGen* se organizan en los directorios:
 - **HDL**
 - **synthesis**
 - **implementation**



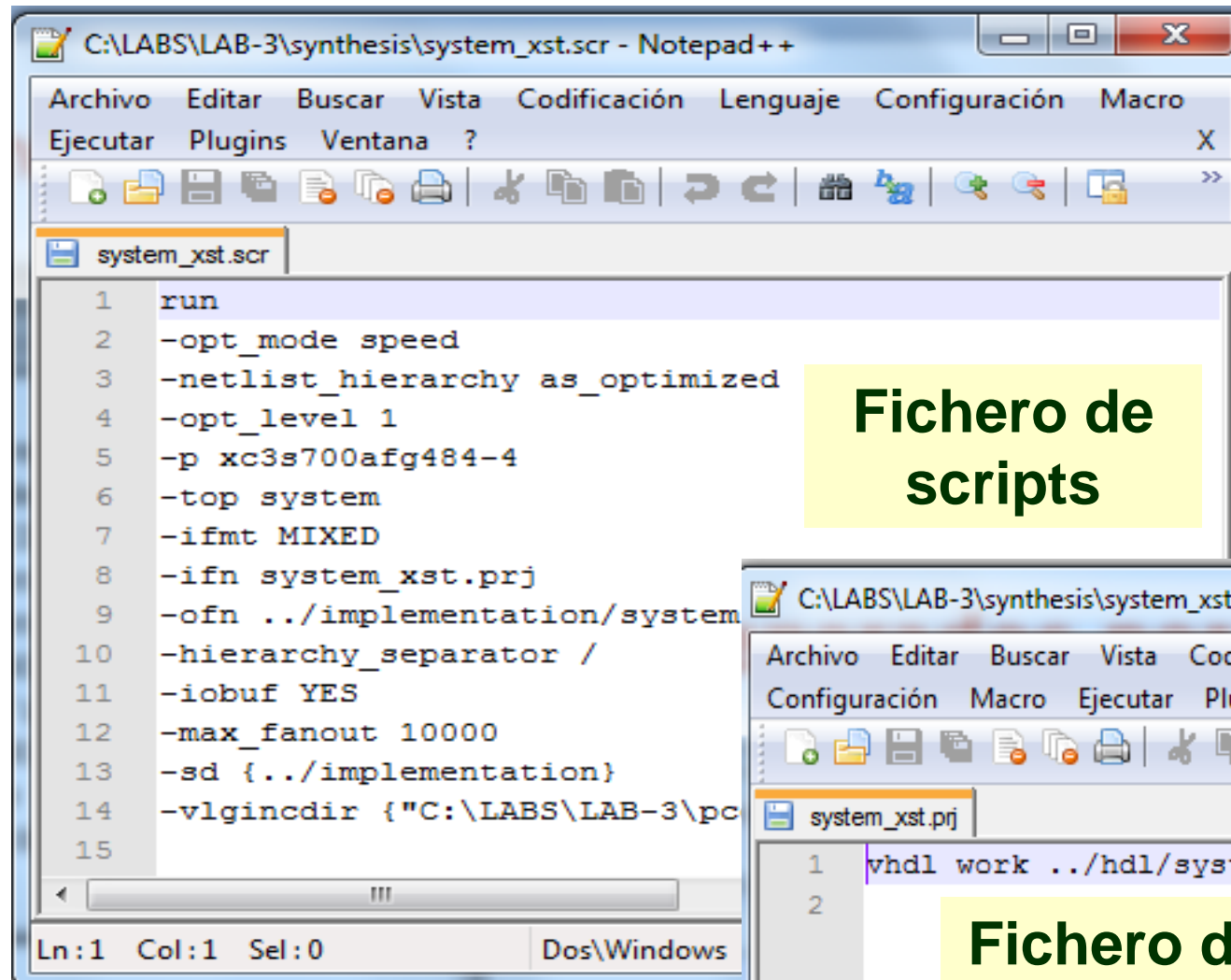
Ficheros generados por *PlatGen*



Directorio_del_proyecto

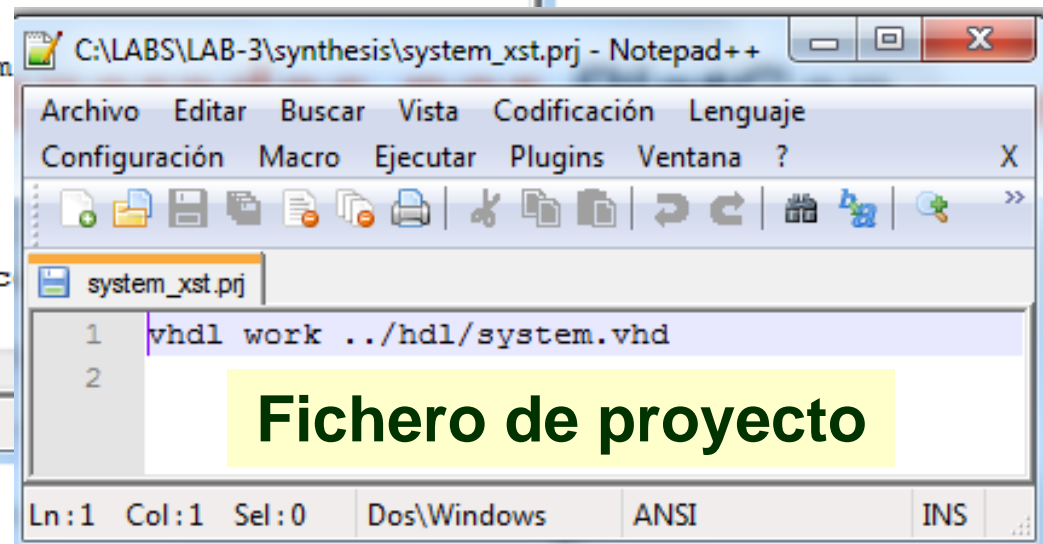


Ficheros generados por *PlatGen* (cont.)



```
1 run
2 -opt_mode speed
3 -netlist_hierarchy as_optimized
4 -opt_level 1
5 -p xc3s700afg484-4
6 -top system
7 -ifmt MIXED
8 -ifn system_xst.prj
9 -ofn ../implementation/system
10 -hierarchy_separator /
11 -iobuf YES
12 -max_fanout 10000
13 -sd {../implementation}
14 -vlgincdir {"C:\LABS\LAB-3\pc
15
```

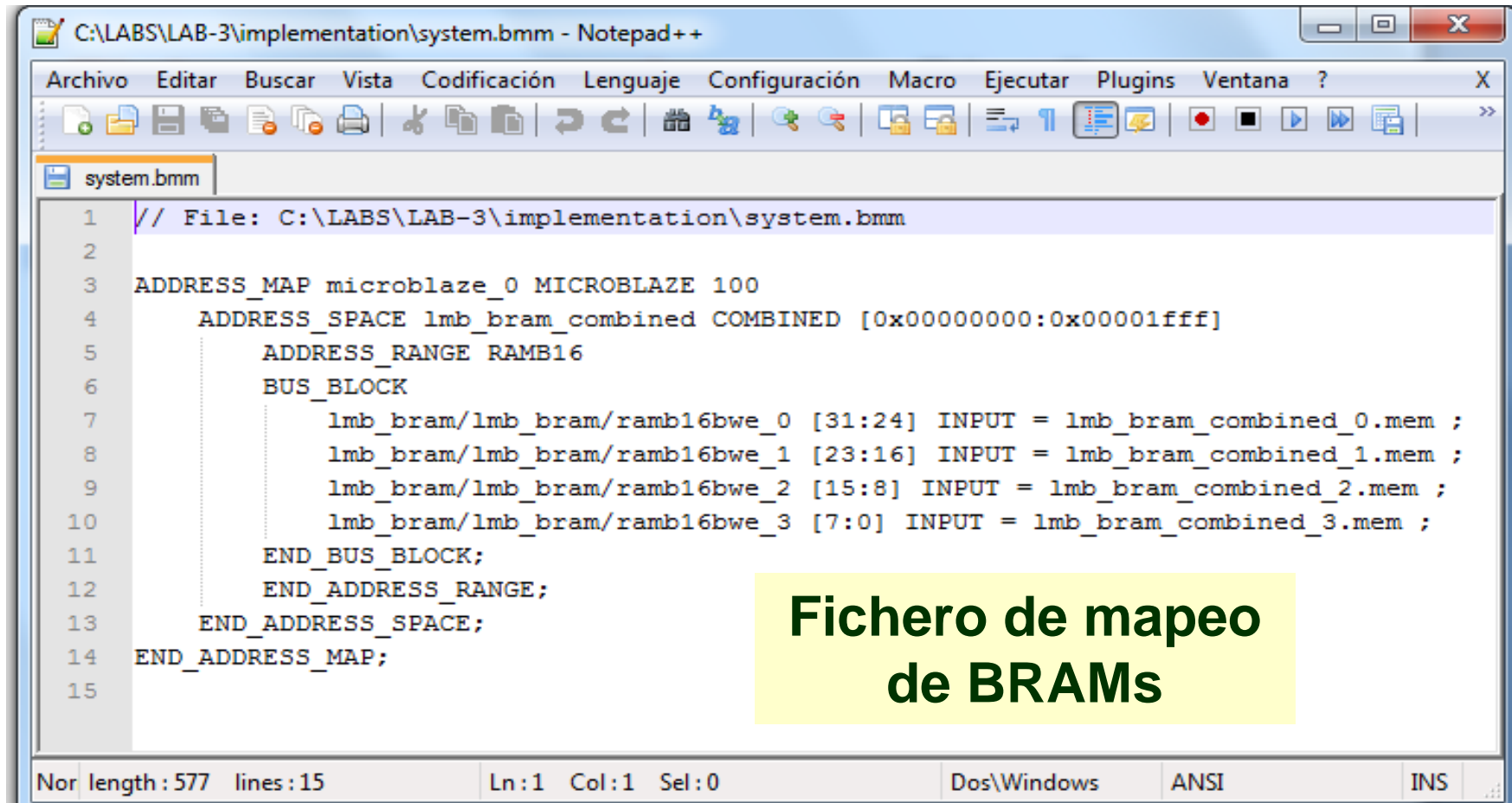
Fichero de scripts



```
1 vhdl work ../hdl/system.vhd
2
```

Fichero de proyecto

Ficheros generados por *PlatGen* (cont.)

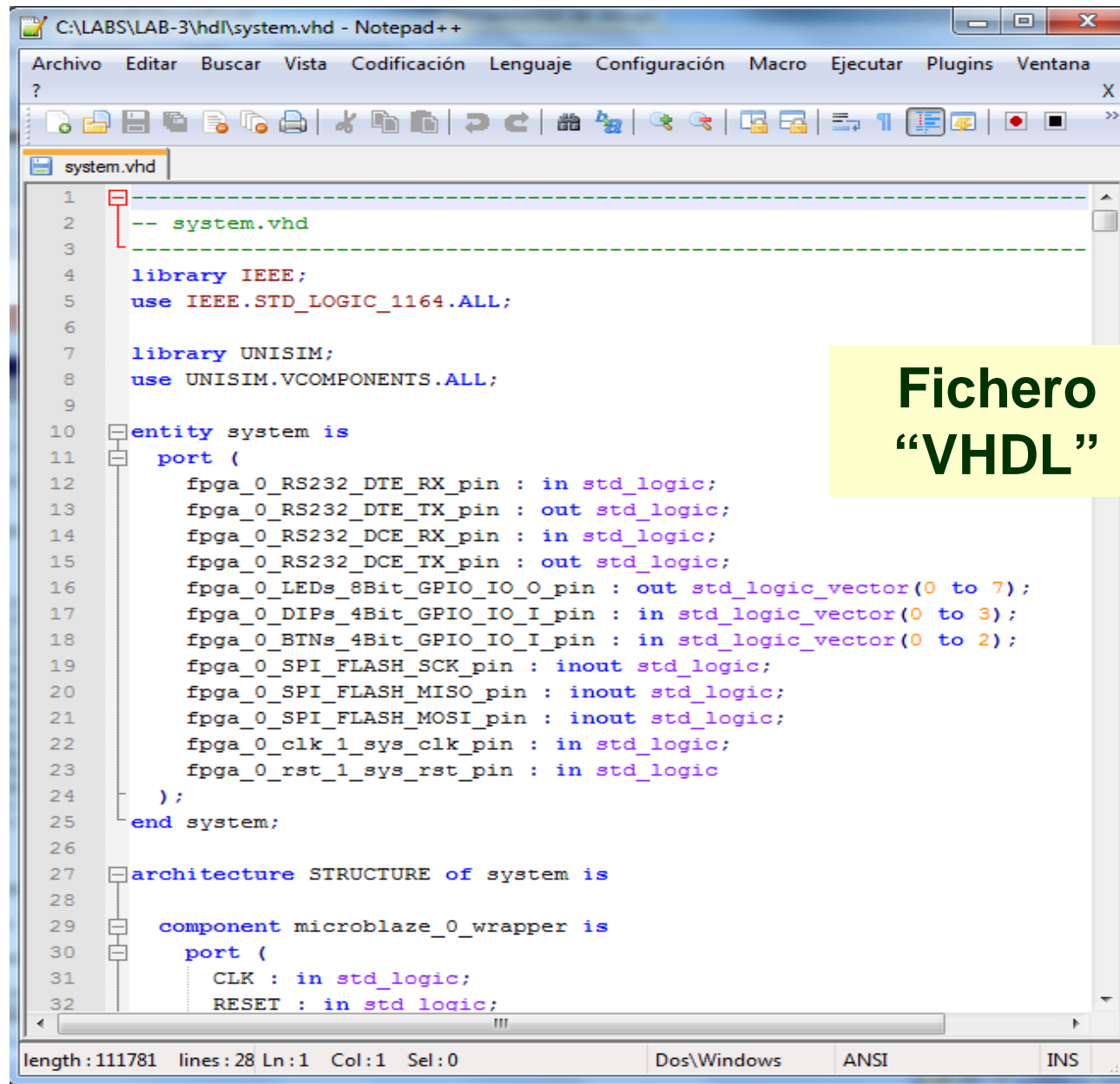


```
1 // File: C:\LABS\LAB-3\implementation\system.bmm
2
3 ADDRESS_MAP microblaze_0 MICROBLAZE 100
4     ADDRESS_SPACE lmb_bram_combined COMBINED [0x00000000:0x00001fff]
5         ADDRESS_RANGE RAMB16
6             BUS_BLOCK
7                 lmb_bram/lmb_bram/ramb16bwe_0 [31:24] INPUT = lmb_bram_combined_0.mem ;
8                 lmb_bram/lmb_bram/ramb16bwe_1 [23:16] INPUT = lmb_bram_combined_1.mem ;
9                 lmb_bram/lmb_bram/ramb16bwe_2 [15:8] INPUT = lmb_bram_combined_2.mem ;
10                lmb_bram/lmb_bram/ramb16bwe_3 [7:0] INPUT = lmb_bram_combined_3.mem ;
11            END_BUS_BLOCK;
12        END_ADDRESS_RANGE;
13    END_ADDRESS_SPACE;
14 END_ADDRESS_MAP;
15
```

Fichero de mapeo de BRAMs

Nor length : 577 lines : 15 Ln: 1 Col: 1 Sel: 0 Dos\Windows ANSI INS

Ficheros generados por *PlatGen* (cont.)




```
1  -- system.vhd
2
3
4  library IEEE;
5  use IEEE.STD_LOGIC_1164.ALL;
6
7  library UNISIM;
8  use UNISIM.VCOMPONENTS.ALL;
9
10 entity system is
11     port (
12         fpga_0_RS232_DTE_RX_pin : in std_logic;
13         fpga_0_RS232_DTE_TX_pin : out std_logic;
14         fpga_0_RS232_DCE_RX_pin : in std_logic;
15         fpga_0_RS232_DCE_TX_pin : out std_logic;
16         fpga_0_LEDs_8Bit_GPIO_IO_0_pin : out std_logic_vector(0 to 7);
17         fpga_0_DIPs_4Bit_GPIO_IO_I_pin : in std_logic_vector(0 to 3);
18         fpga_0_BTNs_4Bit_GPIO_IO_I_pin : in std_logic_vector(0 to 2);
19         fpga_0_SPI_FLASH_SCK_pin : inout std_logic;
20         fpga_0_SPI_FLASH_MISO_pin : inout std_logic;
21         fpga_0_SPI_FLASH_MOSI_pin : inout std_logic;
22         fpga_0_clk_1_sys_clk_pin : in std_logic;
23         fpga_0_rst_1_sys_rst_pin : in std_logic;
24     );
25 end system;
26
27 architecture STRUCTURE of system is
28
29     component microblaze_0_wrapper is
30     port (
31         CLK : in std_logic;
32         RESET : in std_logic;
```

length : 111781 lines : 28 Ln : 1 Col : 1 Sel : 0

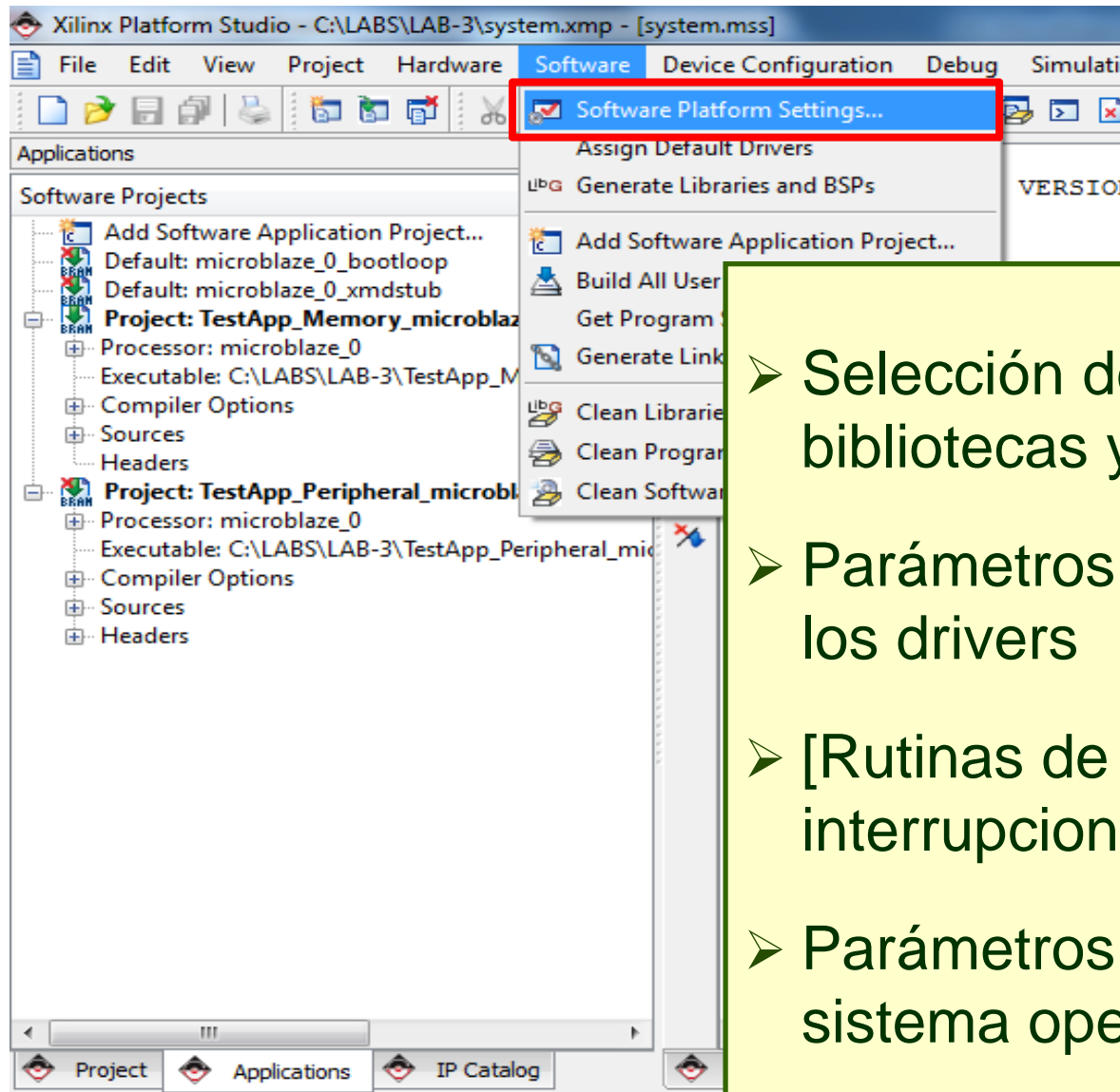
Dos\Windows ANSI INS

Fichero
“VHDL”

Implementación del sistema con *Xflow*

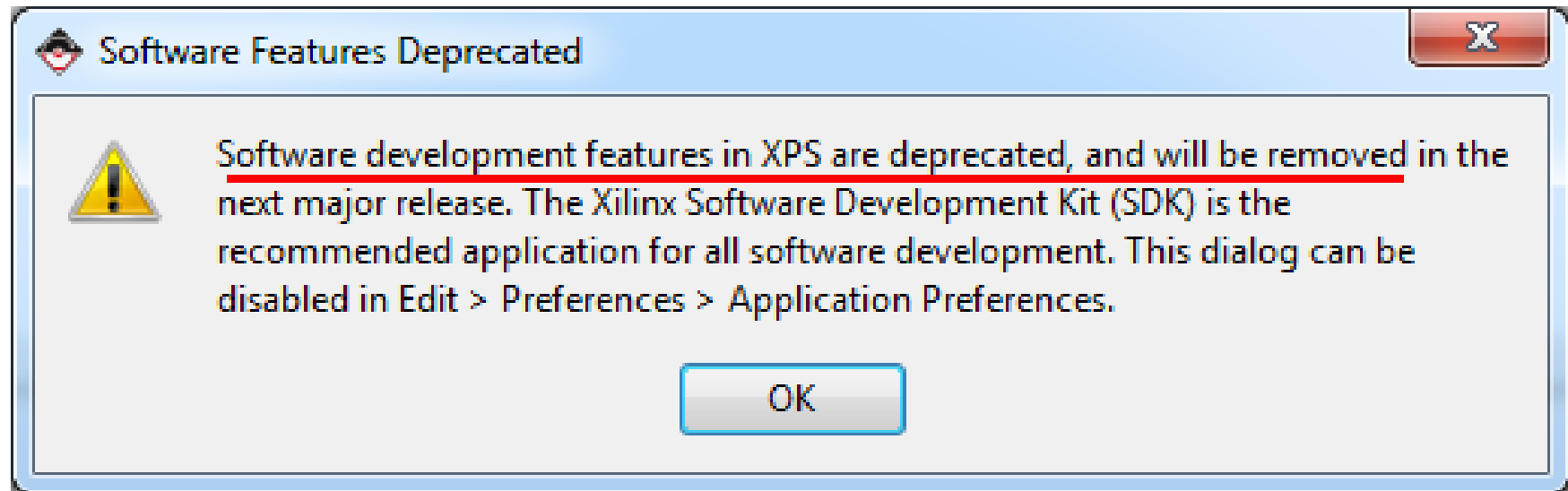
- La opción “**Generate Bitstream**”  permite generar el fichero de configuración de la FPGA a través de *Xflow*
- *Xflow* ejecuta las distintas herramientas de implementación del entorno ISE:
 - Traducción (*ngdbuild*)
 - Mapeo tecnológico (*map*)
 - Place & Route (*par*)
 - Generación del bitstream (*bitgen*)
- El proceso de implementación puede controlarse mediante los ficheros: **etc/fast_runtime.opt** y **etc/bitgen_spartan3.ut**
- Es necesario definir el **fichero de restricciones** con la localización de los pines I/O de la FPGA: **data/system.ucf**
- Tras realizar el proceso se obtiene las **conexiones** del sistema de procesamiento en: **implementation / system.bit**

Configuración software de la plataforma



- Selección de drivers, bibliotecas y sistema operativo
- Parámetros del procesador y los drivers
- [Rutinas de manejo de interrupciones]
- Parámetros de bibliotecas y sistema operativo

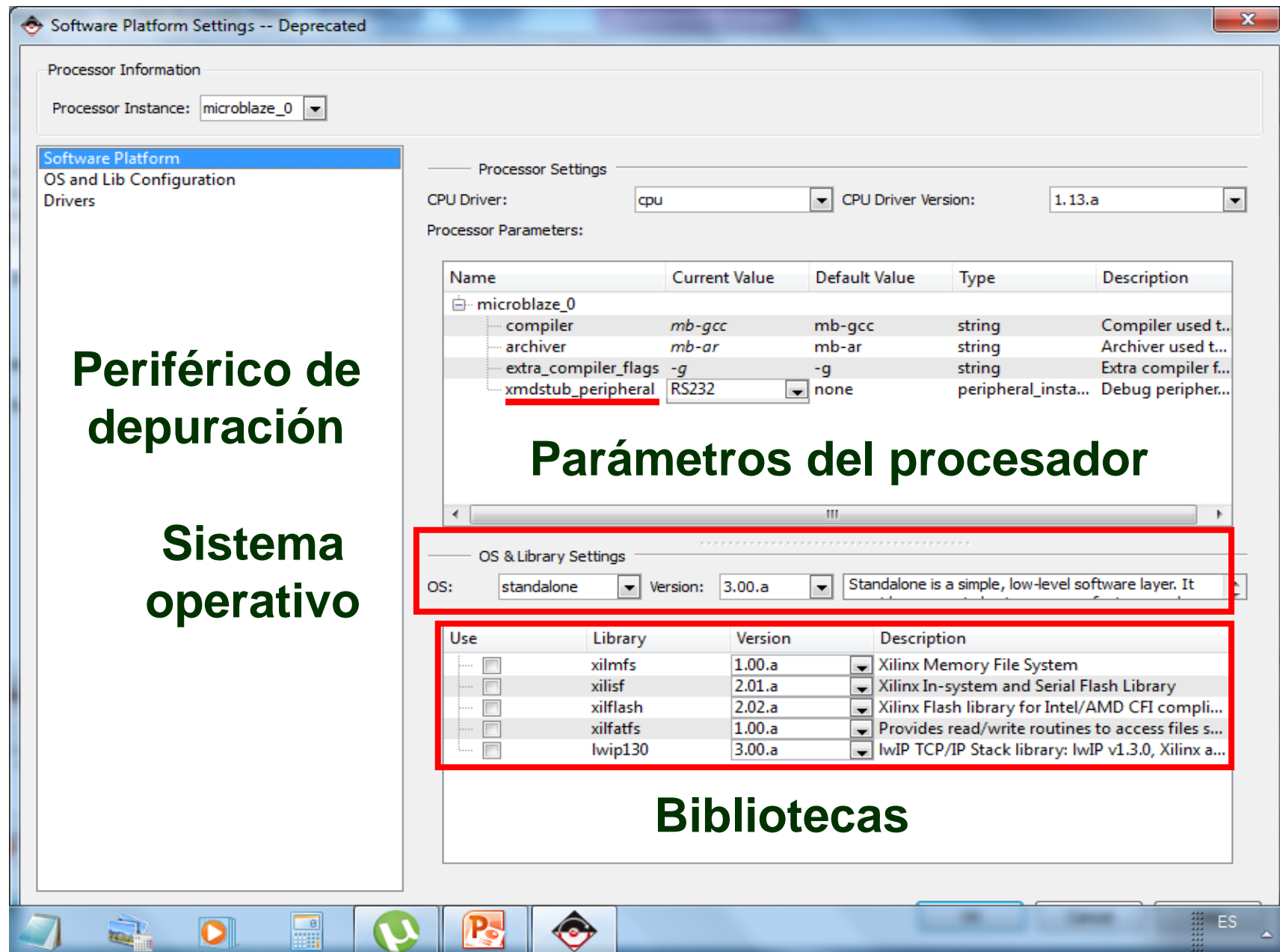
Software platform settings



- **Se elimina a partir de ISE-DS v13**
- **Reemplazado por SDK (Eclipse)**



1.- Software Platform



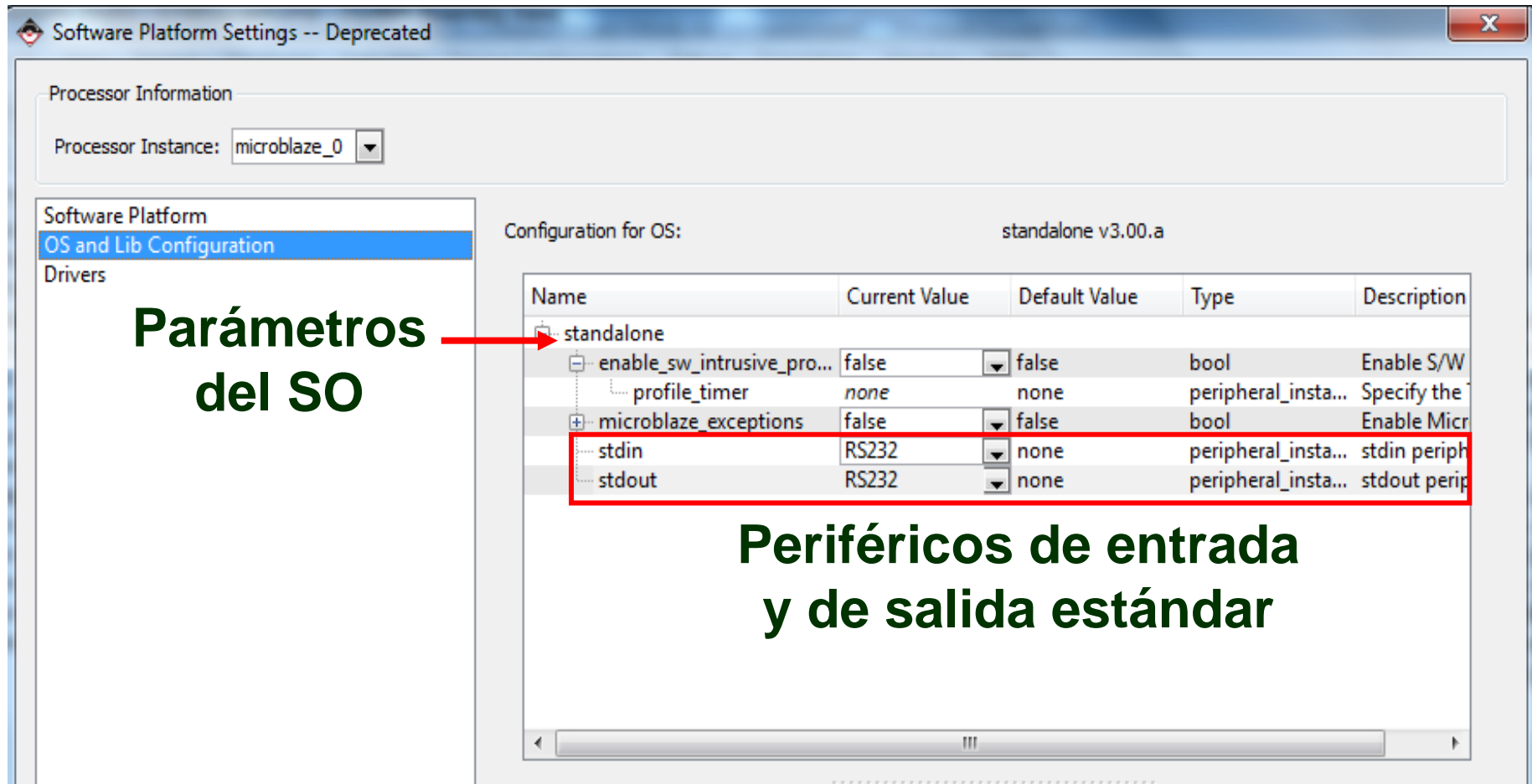
SO Standalone

Lo que apenas se ve...

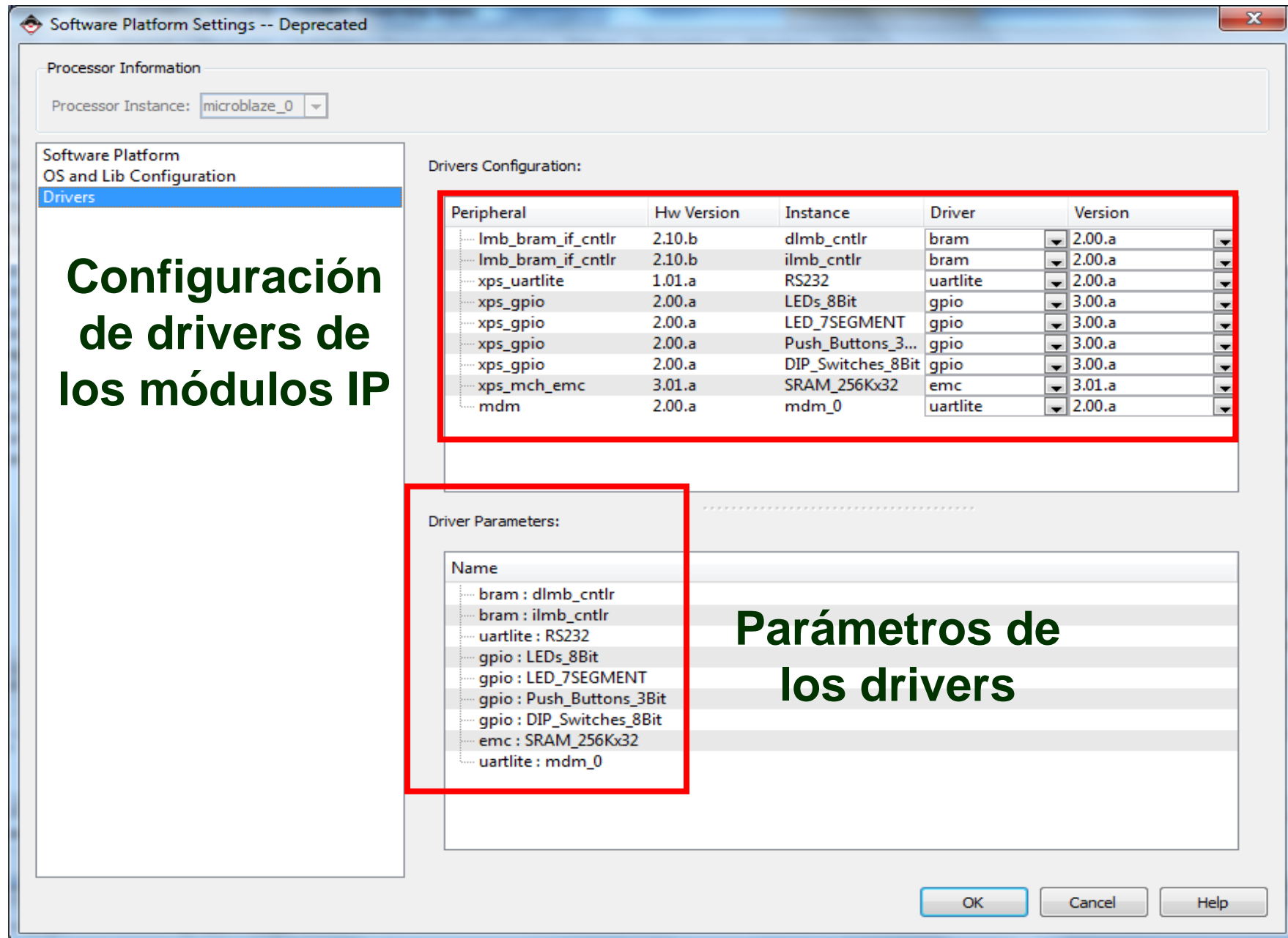
“Standalone is a simple, **low-level software layer**. It provides access to basic processor features such as **caches**, **interrupts** and **exceptions** as well as the basic features of a hosted environment, such as **standard input and output**, **profiling**, **abort** and **exit**.”



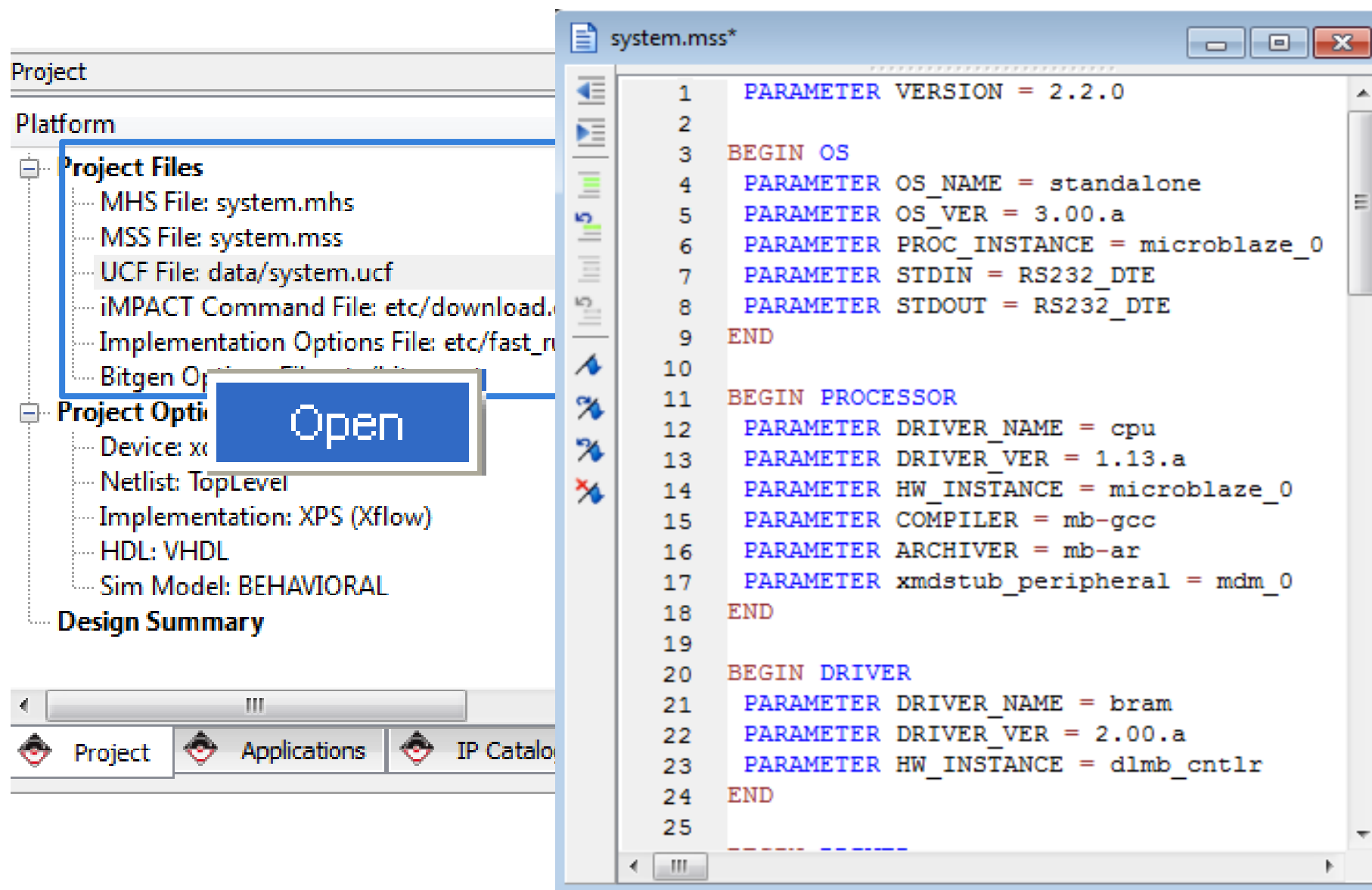
2.- OS and Library Configuration



3.- Drivers



Fichero MSS (Project Tab)



Fichero de Especificaciones de Software

```
1
2  PARAMETER VERSION = 2.2.0
3
4  BEGIN OS
5    PARAMETER OS_NAME = standalone
6    PARAMETER OS_VER = 3.00.a
7    PARAMETER PROC_INSTANCE = microblaze_0
8    PARAMETER stdin = RS232
9    PARAMETER stdout = RS232
10 END
11
12 BEGIN PROCESSOR
13   PARAMETER DRIVER_NAME = cpu
14   PARAMETER DRIVER_VER = 1.13.a
15   PARAMETER HW_INSTANCE = microblaze_0
16   PARAMETER COMPILER = mb-gcc
17   PARAMETER ARCHIVER = mb-ar
18   PARAMETER xmdstub_peripheral = RS232
19 END
20
21 BEGIN DRIVER
22   PARAMETER DRIVER_NAME = uartlite
23   PARAMETER DRIVER_VER = 2.00.a
24   PARAMETER HW_INSTANCE = RS232
25 END
26
```

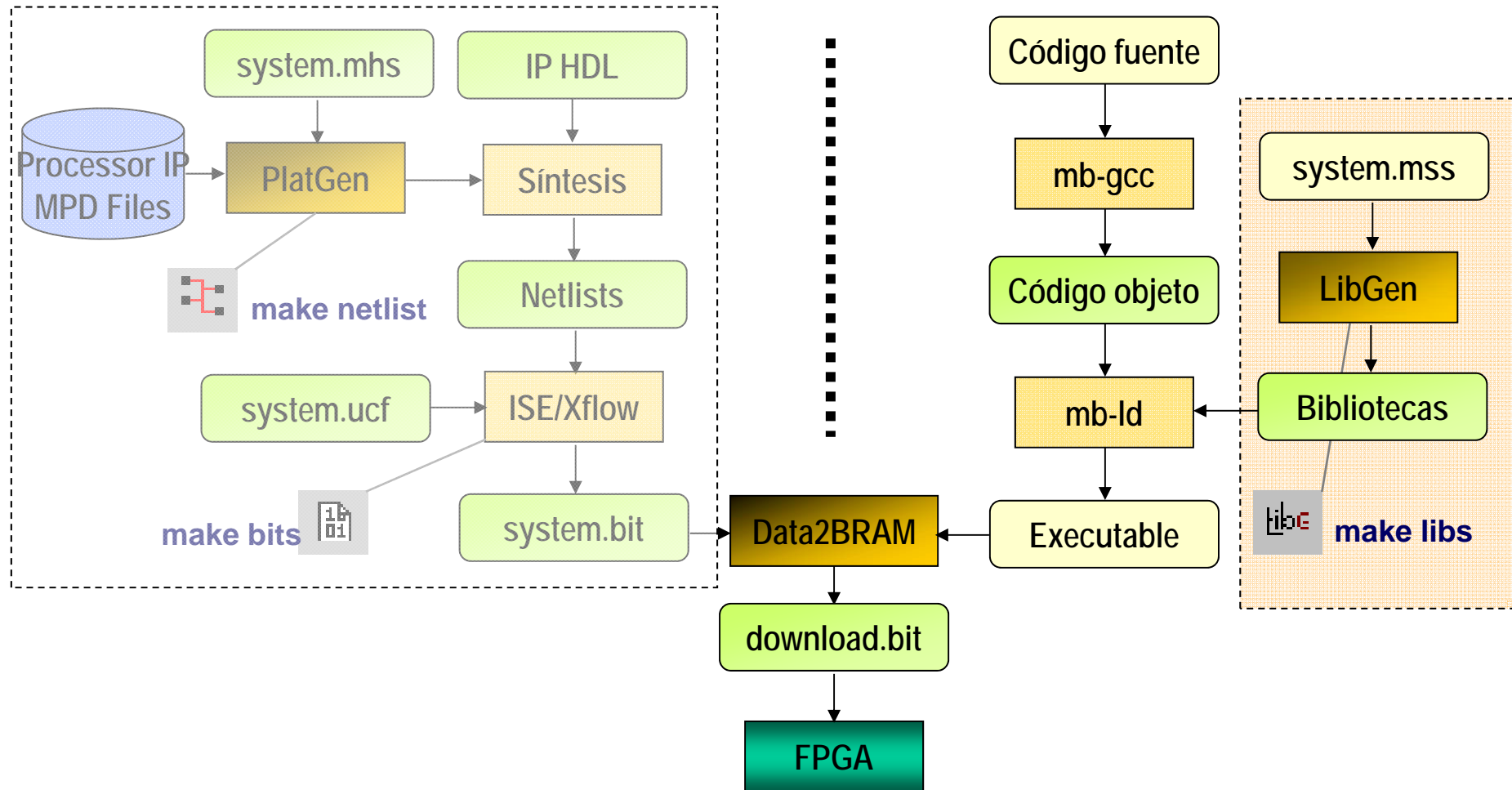
→ **Parámetro global**

→ **OS:** Sistema operativo,
Versión, Identificador,
E/S estándar

→ **PROCESSOR:** Nombre,
Versión, Identificador,
Compilador, Periférico de
depuración

→ **DRIVER:** Nombre, Versión,
Identificador

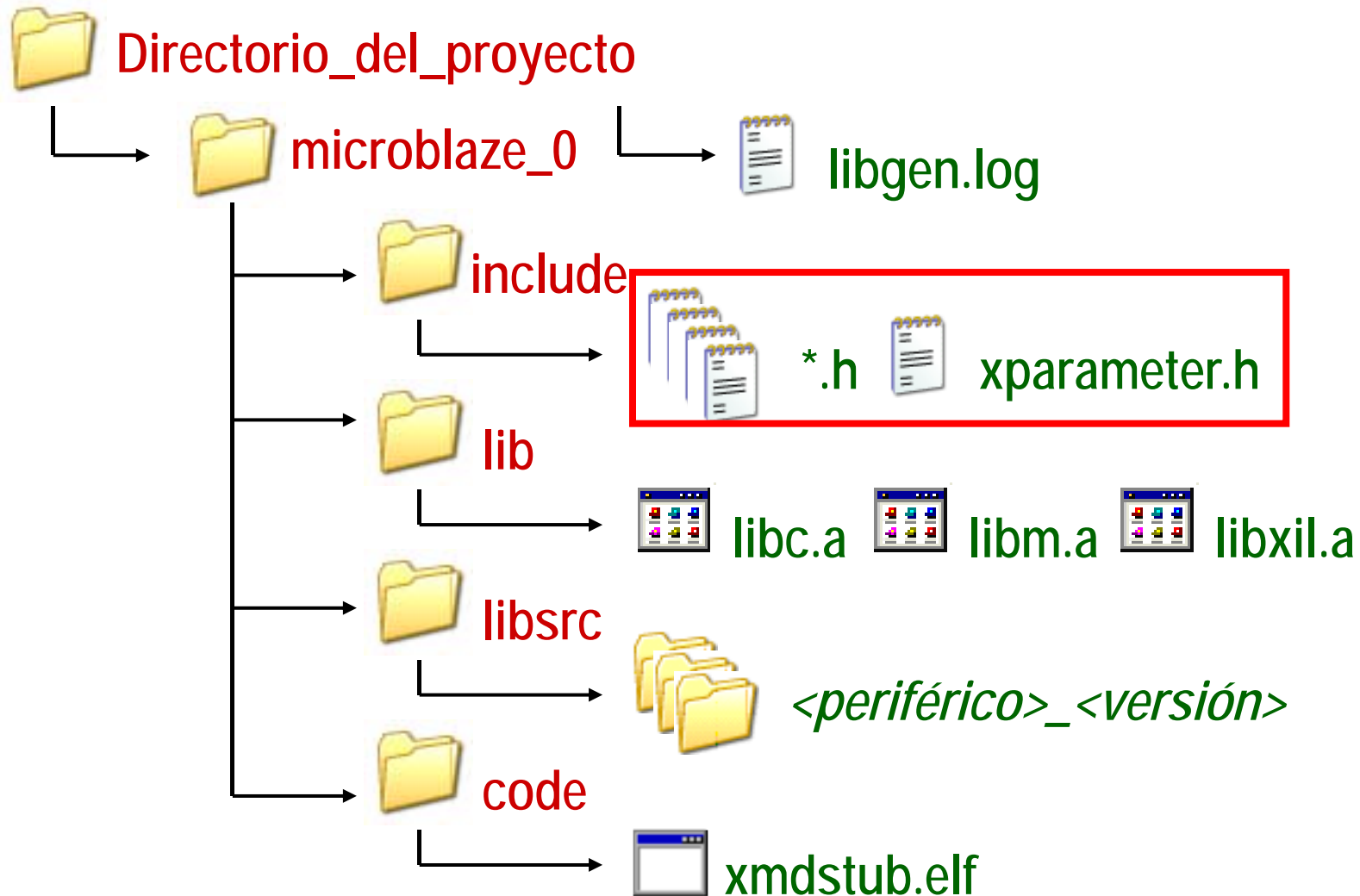
Generación del software de la plataforma



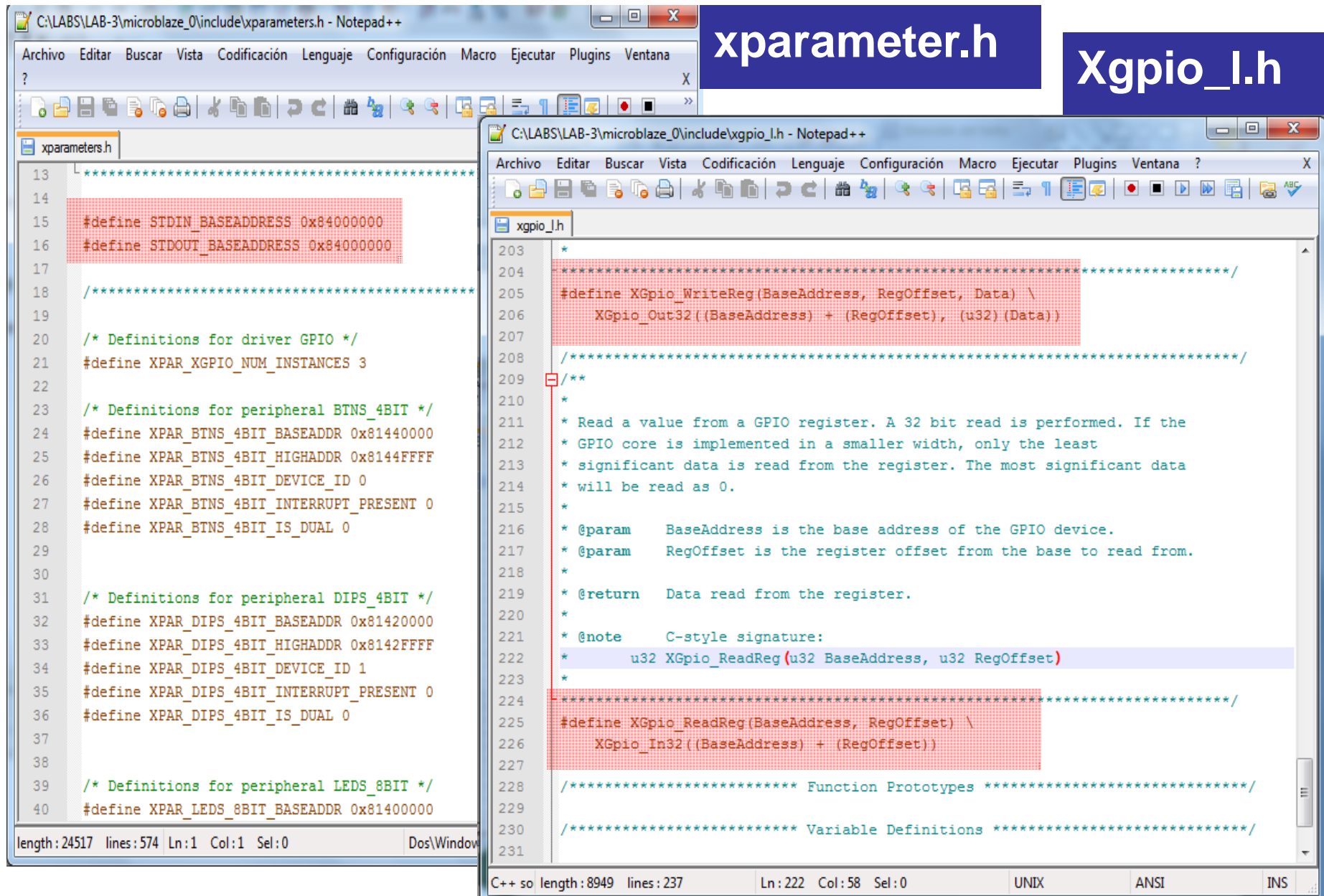
Library Generator (*LibGen*)

- **LibGen** configura, a partir del fichero de especificación de software (**MSS**), las bibliotecas y drivers que utilizarán las aplicaciones del sistema empotrado
- Para cada procesador presente en el sistema, **LibGen** genera la siguiente **estructura de directorios**:
 - **include**
 - Ficheros de cabecera (**.h**) de los drivers
 - Fichero **xparameters.h** (direcciones base, #defines, funciones prototipo)
 - **lib**
 - Bibliotecas compiladas **libc.a**, **libm.a**, **libxil.a**
 - **libsrc**
 - Ficheros intermedios y makefiles necesarios para compilar SO, drivers y bibliotecas
 - **code**
 - Repositorio para ejecutables (**xmdstub.elf**)

Ficheros generados por *LibGen*



Ficheros generados por *LibGen* (cont.)



The image displays two Notepad++ windows side-by-side, showing header files generated by LibGen. The left window, titled 'C:\LABS\LAB-3\microblaze_0\include\xparameters.h - Notepad++', shows the 'xparameter.h' file. The right window, titled 'C:\LABS\LAB-3\microblaze_0\include\xgpio_I.h - Notepad++', shows the 'Xgpio_I.h' file. Both windows have a menu bar with options like Archivo, Editar, Buscar, Vista, Codificación, Lenguaje, Configuración, Macro, Ejecutar, Plugins, and Ventana. The status bar at the bottom of the left window shows 'length: 24517 lines: 574 Ln: 1 Col: 1 Sel: 0 Dos\Windows'. The status bar at the bottom of the right window shows 'C++ so length: 8949 lines: 237 Ln: 222 Col: 58 Sel: 0 UNIX ANSI INS'.

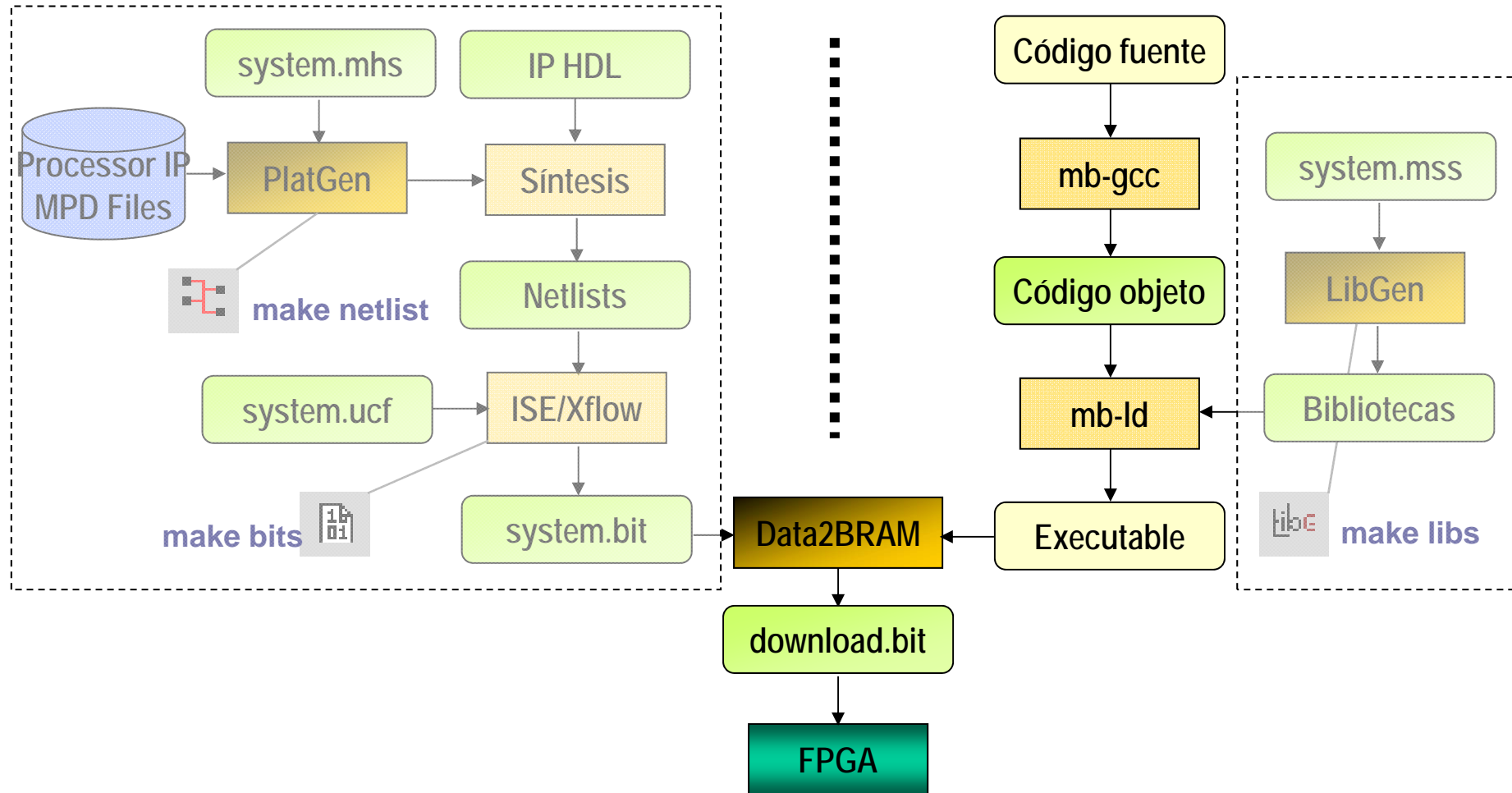
xparameter.h

```
13  *****
14
15  #define STDIN_BASEADDRESS 0x84000000
16  #define STDOUT_BASEADDRESS 0x84000000
17
18  /*****
19
20  /* Definitions for driver GPIO */
21  #define XPAR_XGPIO_NUM_INSTANCES 3
22
23  /* Definitions for peripheral BTNS_4BIT */
24  #define XPAR_BTNS_4BIT_BASEADDR 0x81440000
25  #define XPAR_BTNS_4BIT_HIGHADDR 0x8144FFFF
26  #define XPAR_BTNS_4BIT_DEVICE_ID 0
27  #define XPAR_BTNS_4BIT_INTERRUPT_PRESENT 0
28  #define XPAR_BTNS_4BIT_IS_DUAL 0
29
30
31  /* Definitions for peripheral DIPS_4BIT */
32  #define XPAR_DIPS_4BIT_BASEADDR 0x81420000
33  #define XPAR_DIPS_4BIT_HIGHADDR 0x8142FFFF
34  #define XPAR_DIPS_4BIT_DEVICE_ID 1
35  #define XPAR_DIPS_4BIT_INTERRUPT_PRESENT 0
36  #define XPAR_DIPS_4BIT_IS_DUAL 0
37
38
39  /* Definitions for peripheral LEDS_8BIT */
40  #define XPAR_LEDS_8BIT_BASEADDR 0x81400000
```

Xgpio_I.h

```
203  *
204  *****/
205  #define XGpio_WriteReg(BaseAddress, RegOffset, Data) \
206  XGpio_Out32((BaseAddress) + (RegOffset), (u32)(Data))
207
208  /*****
209  /**
210  *
211  * Read a value from a GPIO register. A 32 bit read is performed. If the
212  * GPIO core is implemented in a smaller width, only the least
213  * significant data is read from the register. The most significant data
214  * will be read as 0.
215  *
216  * @param BaseAddress is the base address of the GPIO device.
217  * @param RegOffset is the register offset from the base to read from.
218  *
219  * @return Data read from the register.
220  *
221  * @note C-style signature:
222  * u32 XGpio_ReadReg(u32 BaseAddress, u32 RegOffset)
223  *
224  *****/
225  #define XGpio_ReadReg(BaseAddress, RegOffset) \
226  XGpio_In32((BaseAddress) + (RegOffset))
227
228  /***** Function Prototypes *****/
229
230  /***** Variable Definitions *****/
231
```

Creación de la plataforma HW/SW



Documentación

➤ Manuales

- *Platform Studio User Guide*
- *Embedded System Tools Ref. Manual → Basic System Builder*
- *Embedded System Tools Ref. Manual → Platform Generator*
- *Embedded System Tools Ref. Manual → Library Generator*

➤ Soporte Web

- EDK
 - <http://www.xilinx.com/edk>
- Ejemplos
 - http://www.xilinx.com/ise/embedded/edk_examples.htm
- Tutoriales
 - <http://support.xilinx.com/support/techsup/tutorials/index.htm>

