Sistemas empotrados y módulos IP

Maestría en Sistemas Digitales

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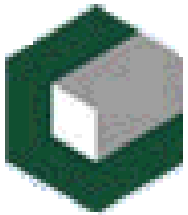


Técnicas avanzadas de diseño de sistemas digitales

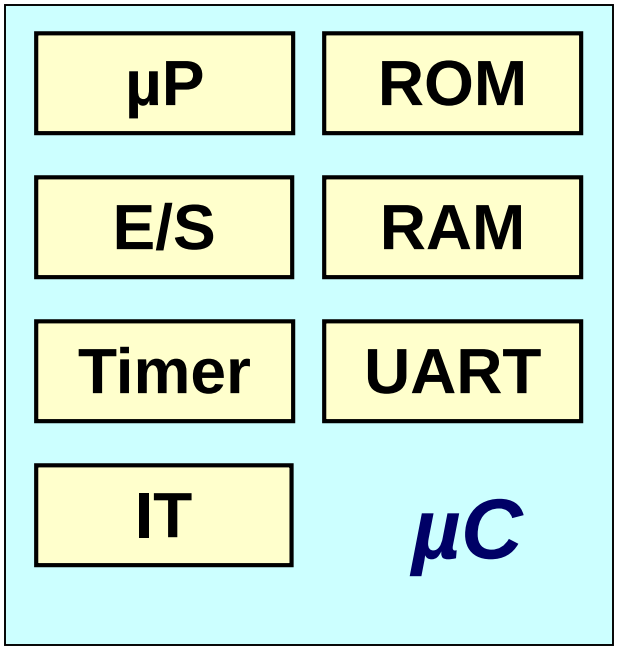
- Lenguajes de descripción de hardware
- Dispositivos programables
- Sistemas empotrados (SoC, SoPC)
- Reusabilidad
  - Módulos de Propiedad Intelectual (IP)
- Codiseño HW/SW

Paquete tecnológico

Objetivo de los sistemas empotrados

- **Integrar funcionalidad diversa en *un solo chip***
- **Ventajas significativas**
- **Origen:**
  - **Microcontroladores**

(single chip microcomputer)



Sistemas empotrados

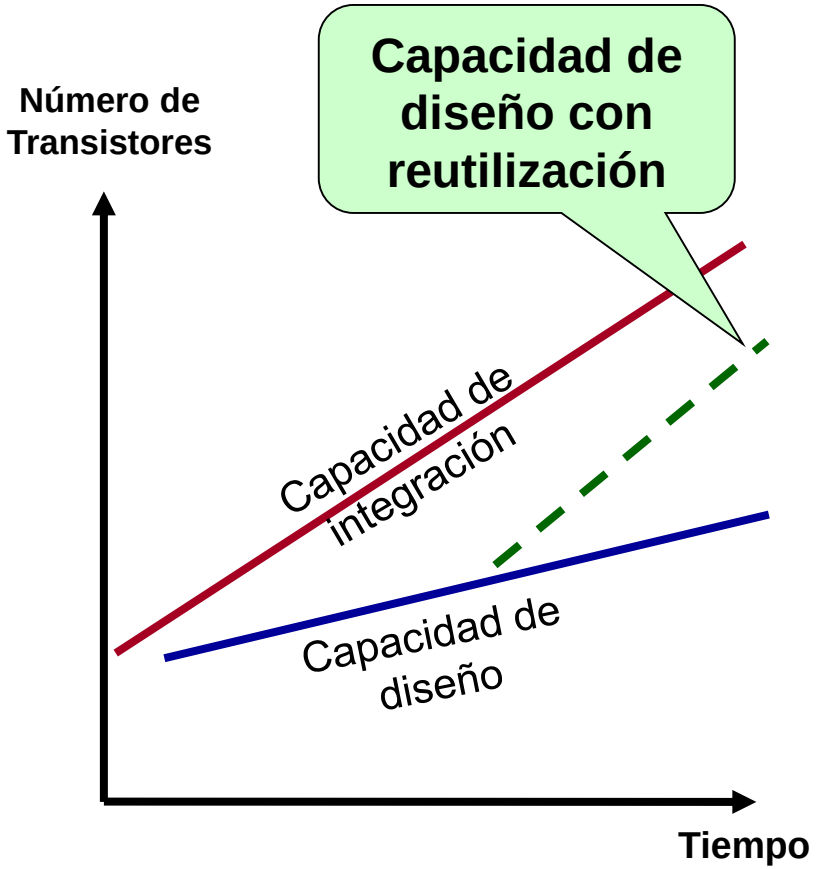
Integración de 2 ó mas macrocomponentes utilizadas previamente como CI independientes

- **Realización *System on Programmable Chip* (SoPC)**
- **El *µC* sólo realiza una *funcionalidad SW***
- **Necesidad de añadir *HW específico* on chip**
- **Usualmente, implementaciones *híbridas HW/SW***
- **Basados en *técnicas de reusabilidad***

Pero… *¿cómo integrar un µC en un FPGA?*

Reusabilidad

- **No se puede *perder tiempo* en diseñar componentes ya utilizados y verificados previamente**
- **Necesidad de *reutilización* de componentes**
- **Necesidad de *descripciones SW* de *componentes HW complejas***



Módulos de Propiedad Intelectual

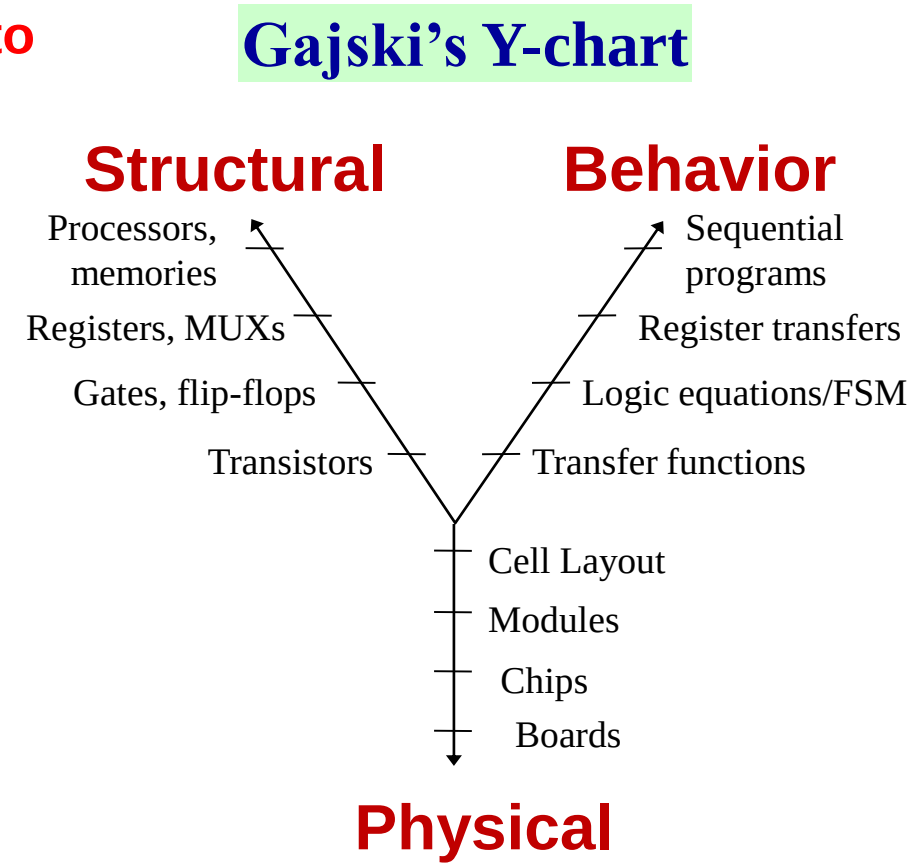
Módulos de Propiedad Intelectual

- **Descripción *software* de componentes *hardware* complejas**
  - **Ficheros: código fuente, netlist, …**
- **Bloques funcionales *pre diseñados* y *pre verificados***
- **Hardware *configurable***
- **Base de la *reusabilidad***

***Espina dorsal* de las técnicas avanzadas de diseño digital**

Tipos de IP

- ***Soft CORE***
  - **Descripción de comportamiento**
  - **Tipicamente en HDL**
  - **Independiente de la tecnología**
- ***Firm CORE***
  - **Descripción estructural**
  - **Optimizados para una arquitectura**
  - **Tipicamente en HDL o netlist**
- ***Hard CORE***
  - **Descripción física**
  - **Suministrada mediante ficheros de layout (o ya implementados)**
  - **Dependiente de la tecnología**



Ejemplos de IP

CA

Cores are availabl
vendors (FPGA co
models and refere

Processors and

8051-Compatible r
C8051 legacy r
D80530 fast (2
R8051 high-spe
R80515 high-sp
R8051X-C high
Infineon peri

Other 8-bit control
PIC® – C165X,
CZ80CPU, CZ8
C6805, C6811

C68000 16-bit pro

DSPs (Digital Sign
16-bit – C3202
24-bit – C5600

Bus and Network Interfaces

CAN – bus controller, dual CAN controller

Ethernet MAC – 10/100, 10/100 Lite, 10/100/1000

FireWire – 1394a link layer controller

I2C serial bus – master/slave, slave, high-speed

LIN bus controller

Parallel ports – ECP slave, EPP slave

PCI – 32-bit, 33 /66 MHz target, master/target, multifunction
64-bit, 66 MHz target, master/target
32-bit, 33/66 MHz host bridge

SPI Serial Protocol Interface – master/slave, slave

USB – versions 1.1, 2.0, On-The-Go (OTG)

Multimedia Functions

JPEG encoder, decoder, codec
Lossless (LJPEG) encoder, decoder

JPEG 2000 – encoder, decoder

MPEG-4 encoder, multi-channel

I2S inter-IC sound bus

SPDIF digital audio interface

CSC color space converter

Huffman encoder and decoder

Image Conversion – block-to-raster, raster-to-block, combination

DCT (Discrete Cosine Transform) – forward, inverse, forward/inverse

DWT (Discrete Wavelet Transform) – forward/inverse, line-based forward, block-based forward

Serial Communications

UARTs
H16450S synchronous interface,
H16550S with FIFOs and synchronous interface,
H16750S with FIFOs, IrDA, and synch. interface,

SDLC global serial channel controller

Basic Functions

Standard parts and devices cores

Simulation models – logic devices, memories

Replacement Series

cores specially designed for replacing obsolete and unavailable parts

Bit-slice processors: 4-bit – C2901
16-bit – C29101, C29116A, C49402, C59016

16-bit processors – C80186TX

Microprogram controllers – C2910A, C3910, C49410

DMA controllers – C8237, C82380 32-bit

Peripherals
C6845 CRT controller
C8279 programmable keyboard/display interface
C8255A programmable peripheral interface
C8259A programmable interrupt controllers
C8254 programmable timer/counter

UARTs – H16450, H16550 with FIFOs,
H16750 with FIFOs and IrDA , H8250

Z80 processor support
CZ80CTC programmable counter/timer
CZ80DMA direct memory access controller
CZ80PIO programmable parallel I/O controller
CZ80SIO serial I/O controller

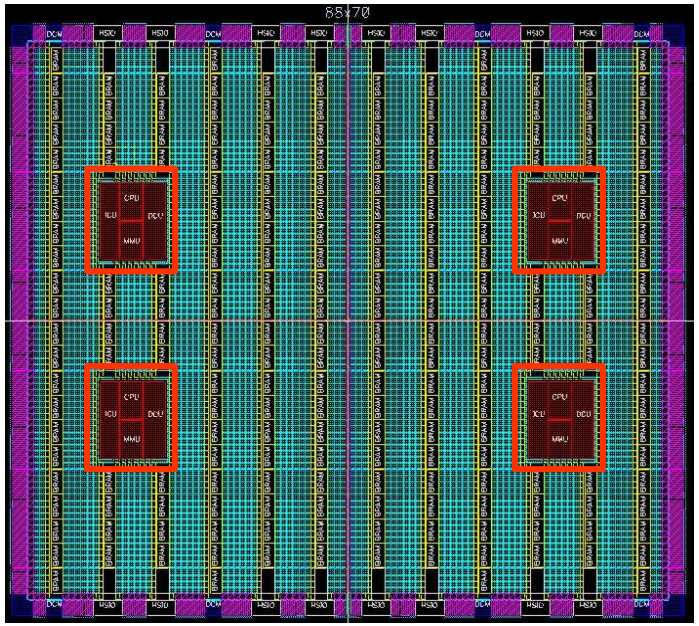
IPs de procesadores para FPGAs

❑ Soft/firm Cores

- MicroBlaze (Xilinx) → MicroBlaze
- NIOS (Intel - Altera) → Nios II
- LEON (http://www.gaisler.com/)
- Microcontroladores (8051, …)

❑ Hard Cores

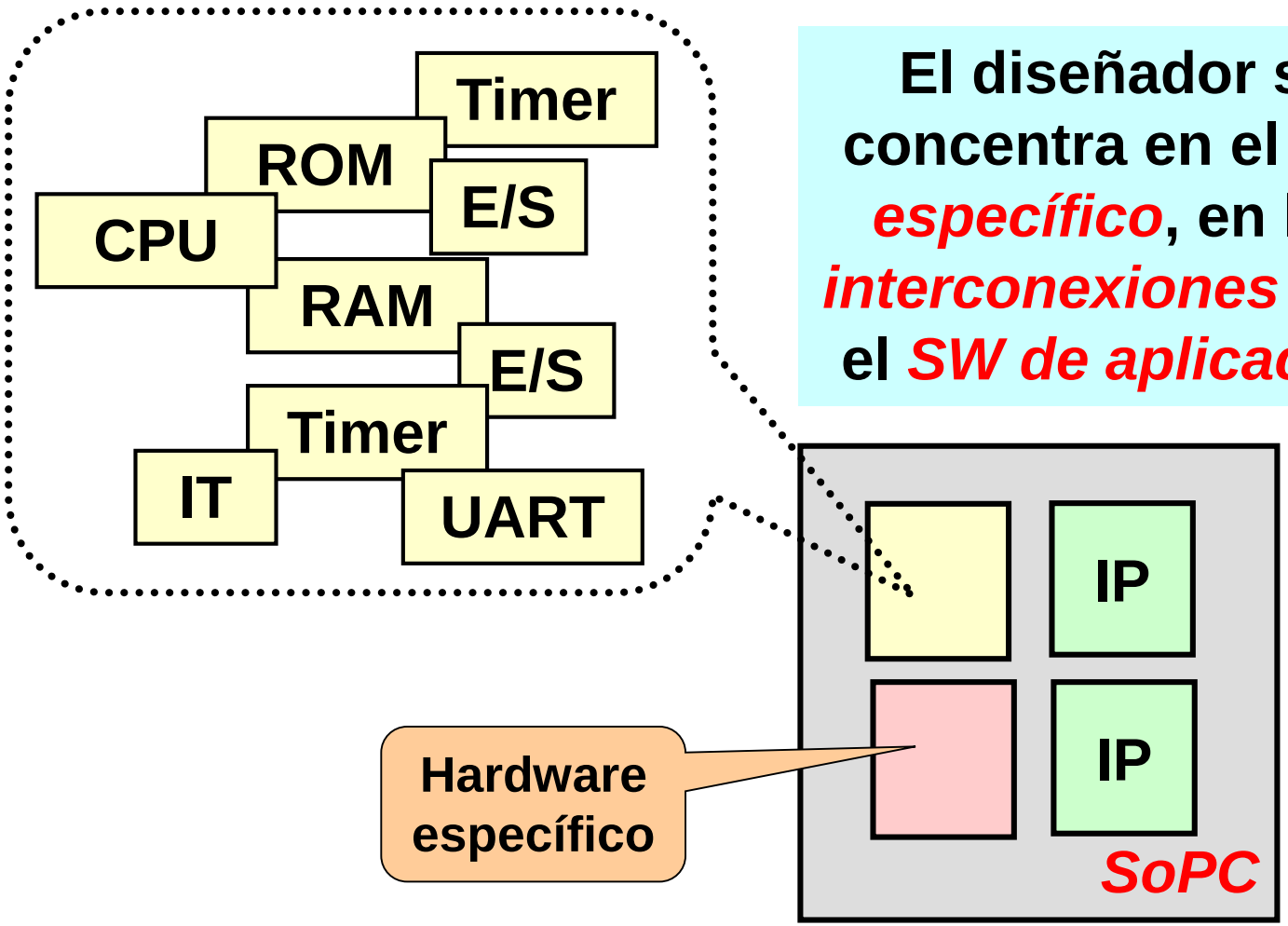
- ARM922T
  (Altera Excalibur, APEX 20K)
- PowerPC
  (Xilinx, Virtex-II Pro y Virtex-4)



Reemplazados por hardcore de
sistemas de procesamiento

Tecnología de IP y desarrollos empotrados

Desarrollo SoPC basado en IPs



Integrantes de un módulo IP

- **Componentes descritas mediante *ficheros***
- ***Documentación***
- **Con frecuencia, con *herramientas de CAD específicas***
- ***Soporte técnico***
- **Parte *jurídica* (para los de pago)**

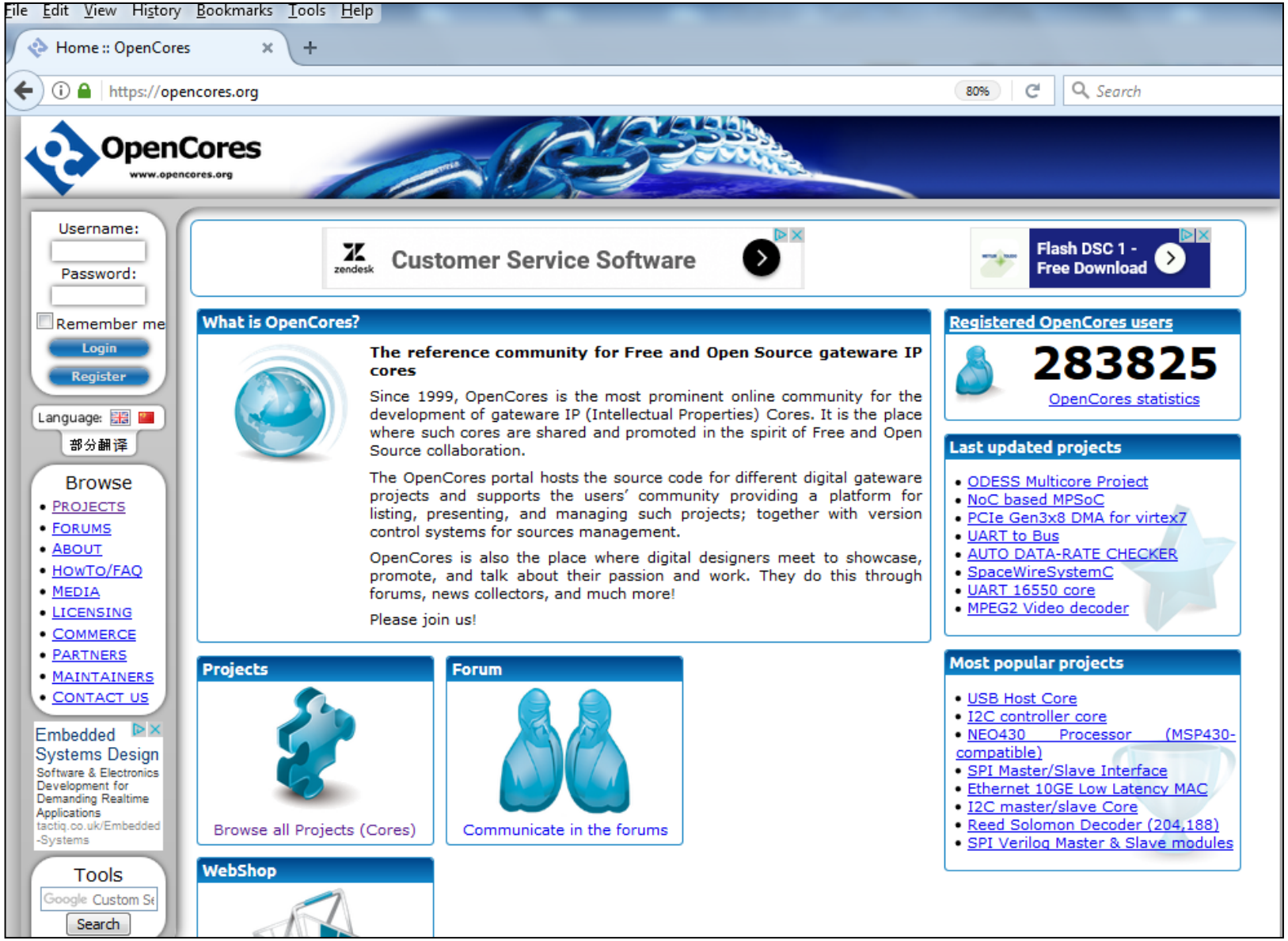
Elementos a considerar al seleccionar un IP

- **Funcionalidad**
- **Consumo de recursos**
- **Configurabilidad**
- **Herramientas de desarrollo**
- **Soporte técnico**
- **Costo**

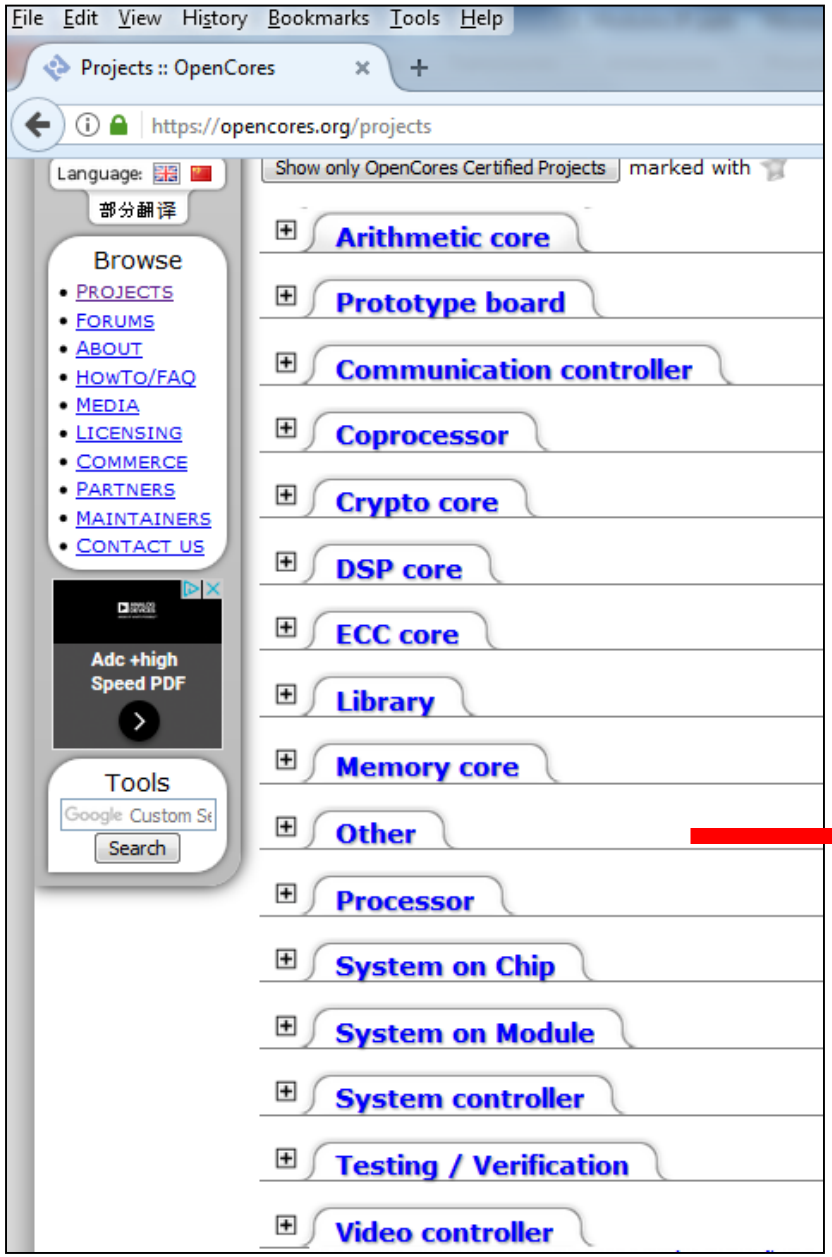
- **8051 simple**
- **Presintetizado**
- **Limitado a 1000 ciclos**
- **Sin soporte técnico**

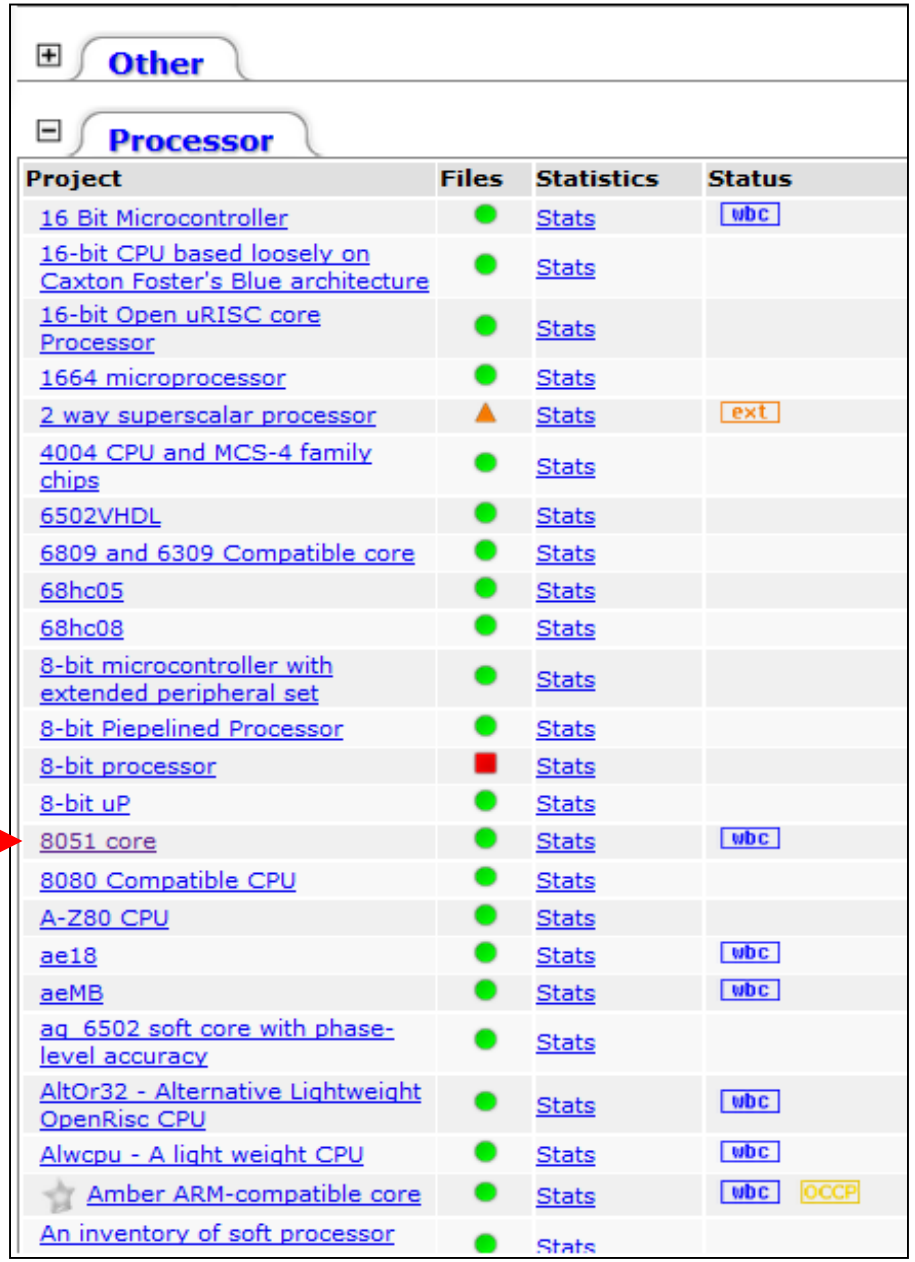
…por *“sólo”* 1000 €

Sitio de IP: opencores.org



Proyectos en opencores.org





8051 en opencores.org

8051 core :: Overview

Details

Name: 8051
Created: Sep 25, 2001
Updated: Nov 13, 2016
SVN Updated: May 5, 2009
SVN: Browse
Latest version: download
Statistics: View

Other project properties

Category: Processor
Language:
Development status: Alpha
Additional info: *none*
WishBone compliant: Yes
WishBone version: n/a
License:

Description

The 8051 microcontroller is member of MCS-51 family, originally designed in th
introduction and is estimated it is used in a large percentage of all embedded s
chip peripherals, like timers and counters, additionally there are 128 bytes of o
memory.

Features

- 8-bit CPU optimized for control applications
- Exstensive Boolean processing (single-bit logic) capabilities
- 64K Program Memory address space
- 64K Data Memory address space
- up to 64K bytes of on-chip Program Memory (ROM)
- 128 bytes of on-chip Data RAM
- 4, 8 bit wide, ports outputs (byte or bit addressable)
- 4, 8 bit wide, ports inputs (byte or bit addressable)
- Two 16-bit timer/counters
- 6-source/5-vector interrupt structure with two priority levels priority levels

Status

Basic core is now syntesizable. I test it with XESS XSV board.
It have all pheripherals.

I/O ports

- rst (in) reset
- clk (in) clock
- int0 (in) external interrupt 0
- int1 (in) external interrupt 1
- ea (in) external access
- iadr_o (out) program rom addres
- idat_i (in) input from external rom
- istb_o (out) strobe to program rom
- iack_i (in) acknowledge from external rom
- icyc_o (out) cycle output to external rom
- dat_i (in) exteranal ram input
- dat_o (out) exteranal ram output
- adr_o (out) external address
- we_o (out) write to external ram
- stb_o (out) strobe
- ack_i (in) acknowledge
- cyc_o (out) cycle
- p0_in, p1_in, p2_in, p3_in (in) port inputs
- p0_out, p1_out, p2_out, p3_out (out) port outputs
- rxd (in) receive
- txd (out) transmit
- t0, t1 (in) t/c external inputs

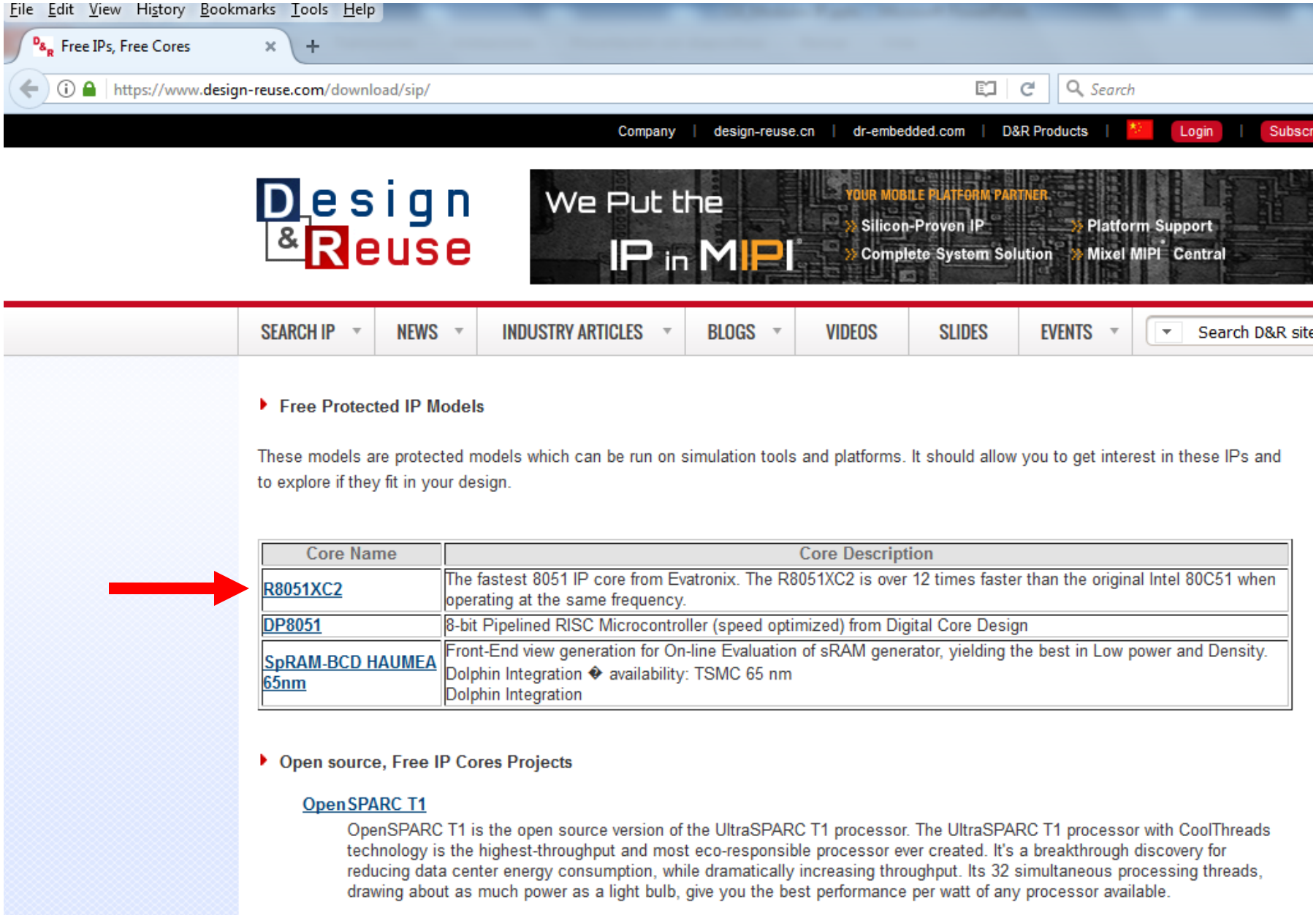
IMAGE: interface.jpg

FILE: interface.jpg
DESCRIPTION: interface

Modules

- oc8051_acc: accumulator
- oc8051_alu: aritmetic logic unit
- oc8051_alu_src1_sel, oc8051_alu_src2_sel, oc8051_alu_src3_sel: alu source
- oc8051_b_register: sfr b register
- oc8051_comp: compare
- oc8051_cy_select: carry select
- oc8051_decoder: main module, decodes instruction and creates control signa
- oc8051_defines

Sitio de IP: www.design-reuse.com



Propuesto

- **Confeccione un programa para un 8051 con reloj de 12 MHz que cada dos segundos, medidos con ayuda de un temporizador atendido por interrupción, lea el estado de ocho interruptores conectados al puerto P1 y lo envíe a ocho LED conectados al puerto P1.**