# 32-Channel RF Signal Amplifier and Attenuator System

## Design and Theory of Operation

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# Introduction

The 32-Channel RF Signal Amplifier and Attenuator System is a modular amplifier and attenuation system designed to provide 2nd stage amplification in close proximity to a 4.7 T MRI scanner (at a Larmor frequency of 200 MHz). With proper choice of components it can readily be adapted to a wide range of other frequencies and applications. Each channel's amplifier and attenuator circuitry is housed on a separate daughterboard for flexibility and easy servicing. These Daughterboards stand perpendicular to a larger Motherboard which contains all the common circuitry such as power distribution and protection circuitry, as well as the interface for attenuation control (Figure 1).

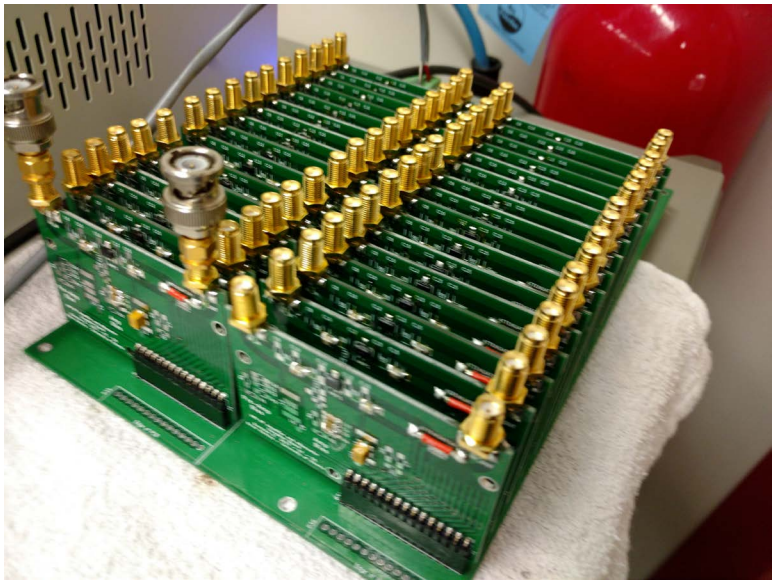

*Figure 1: The 32-Channel RF Signal Amplifier and Attenuator System. Note the daughterboard modules assembled in an array attached to the motherboard.*

# License and Disclaimer



**The static magnetic field of the MRI scanner can cause dangerous forces on ferromagnetic materials.** The instructions contained in this document require familiarity with MRI electronics and with the MRI environment. Standard precautions for working with such equipment must be followed. Specifically, all materials, tools and components used in construction must be non-magnetic if they are to be used within the MRI suite.

# Design

## Principle of Operation

The 32-Channel RF Signal Amplifier and Attenuator System is designed to provide, for each channel, RF amplification using a single device (gain block), followed by an optional programmable attenuator to allow the signal level to be adjusted depending on the requirements of the subsequent stage (in this case the MRI scanner's spectrometer). The design is modular, expandable and readily serviceable by using a separate board for each channel, laid out in an array on a single backplane (motherboard). The use of separate boards also provides high isolation (low crosstalk) between channels. A block diagram of one RF channel is shown in Figure 2.

The Motherboard distributes power and sets the attenuator states of up to 32 Daughterboards. Multiple motherboards can be daisy-chained if more than 32 channels are needed, taking care not to exceed the maximum current limits. Depending on the

application's requirements and component selection, some components (marked "optional" on the schematics) may be omitted. Board design follows IPC standards [1].

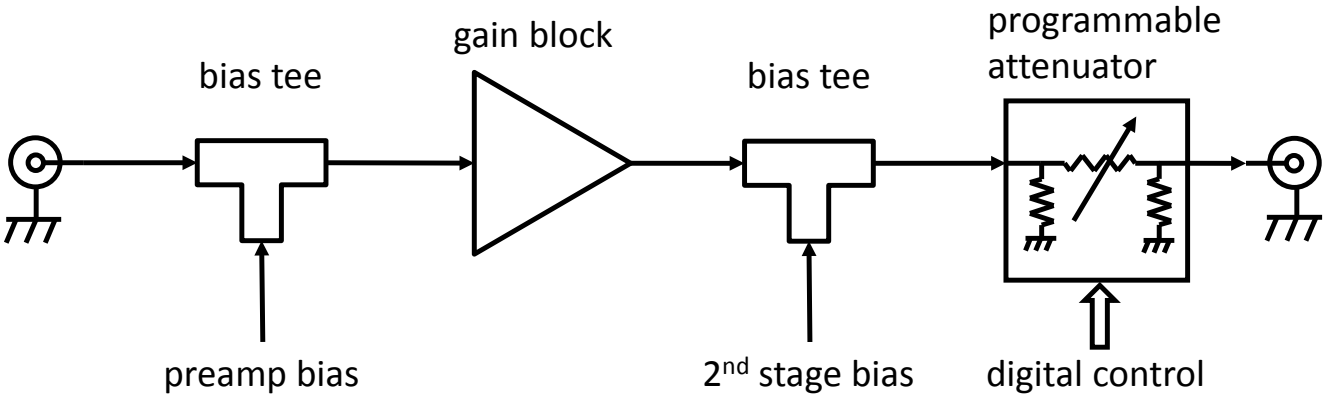


*Figure 2: Block diagram of one channel of the RF amplifier and attenuator system. RF signal flow is left to right.*

## Motherboard

The motherboard contains all the power and control inputs for the amplifiers and attenuators. The daughter boards interface with the motherboard using female 2.54 mm straight pin headers on the motherboard and male 2.54 mm right-angle headers on the daughterboard. The motherboard is a 1.6 mm thick two-layer FR4 printed circuit board (PCB), plated with 2 ounce copper (70 μm) to limit the resistance of the traces. Schematics are shown in Figure 3 and Figure 4. The PCB layout is shown in Figure 5.

### Power

Power for 3 separate DC rails is provided through a 4-pin connector (P1). The rails supply, respectively, the RF amplifiers, attenuators, and optional external 1st stage amplifiers (e.g., for preamps at the RF coil) through a bias voltage at RF input of each DaughterBoard.

In our application the rails are all 5 volts, fed by an external 6.5 volt power supply, which is located outside of the MRI scanner room. Each power input is protected by 1 A resettable fuses (F1–F3), and if desired can be regulated (in our case to 5 volts) using 1084 voltage regulators (U1–U6, dual footprints are provided depending on package choice). The power regulators must be adequately heat-sinked to prevent failure. The design includes holes for bolt-on heat sinks as well as footprints for surface mount heat sinks on both the front and back of the board.

Capacitors (C1–C12) and resistors (R27–R32) for the power regulators must be used according to the regulator's documentation. Additional footprints are provided on the board for optional power filtering components. Redundant footprints for both through-hole and surface-mount components are available on the PCB for flexibility in component choice and implementation.

Protection against overvoltage and electrostatic discharge (ESD) is provided by Zener (Z1–Z3) and transient-voltage-suppression (TVS) diodes (TVS1–TVS3), respectively [2]. Reverse polarity protection can be provided at the input of the voltage regulator by shunting to ground using an appropriately-rated reverse polarity diode. If the polarity is correct the diode will

carry negligible current, but if polarity is reversed it will shunt current to ground, activating the fuse and protecting components downstream.

## Control

The control and interface components for the SKY12347-362LF attenuators are located on the motherboard. Manual control of these 6 bit attenuators is provided by 6 SPST switches (DIP1) and on-board jumpers for the latch enable (LE, JP1) and parallel-serial (P/S, JP2) interface selection. Remote attenuator control is available via a parallel or serial interface through the header (P2) located above the attenuator control switches.

Due to limitations in the P/S selection of the attenuator, parallel operation of the chip requires that the LE pin be switched high (5 V) after the power to the chip is brought high. To accommodate this, the current limiting resistor for the LE pin (R18) should use a large value (e.g., 1 MΩ) to provide a time delay on the LE pin. In this configuration the attenuator bits are set directly by either manual control with the motherboard switches, or – with the switches in the off position – remotely using the attenuator control header (P2) on the motherboard located above the switches.

Alternatively, remote control of the attenuator state can be controlled using a serial interface, by setting the P/S pin high and following the manufacturer's documentation. The serial interface has the additional advantage of providing feedback of the attenuator state to a computer using the Serial Out pin (SO). This remote attenuation is not provided, but would be easily implemented with a separate module connected to the attenuator control header (P2).

## LED Indicators

The status of each power rail and attenuator bit is indicated using low-current LEDs (D1–D9) in series with resistors (R1–R9).

## Expandability

Multiple motherboards may be daisy-chained using the headers at the bottom edge of the PCB (P35 and P36) to expand the design to accommodate additional channels. If this is done, each PCB should be fed its power separately and only the attenuator circuitry should be interconnected. Maximum current on the attenuator traces is 1 A, and may need to be appropriately fused in case an accidental fault should occur.

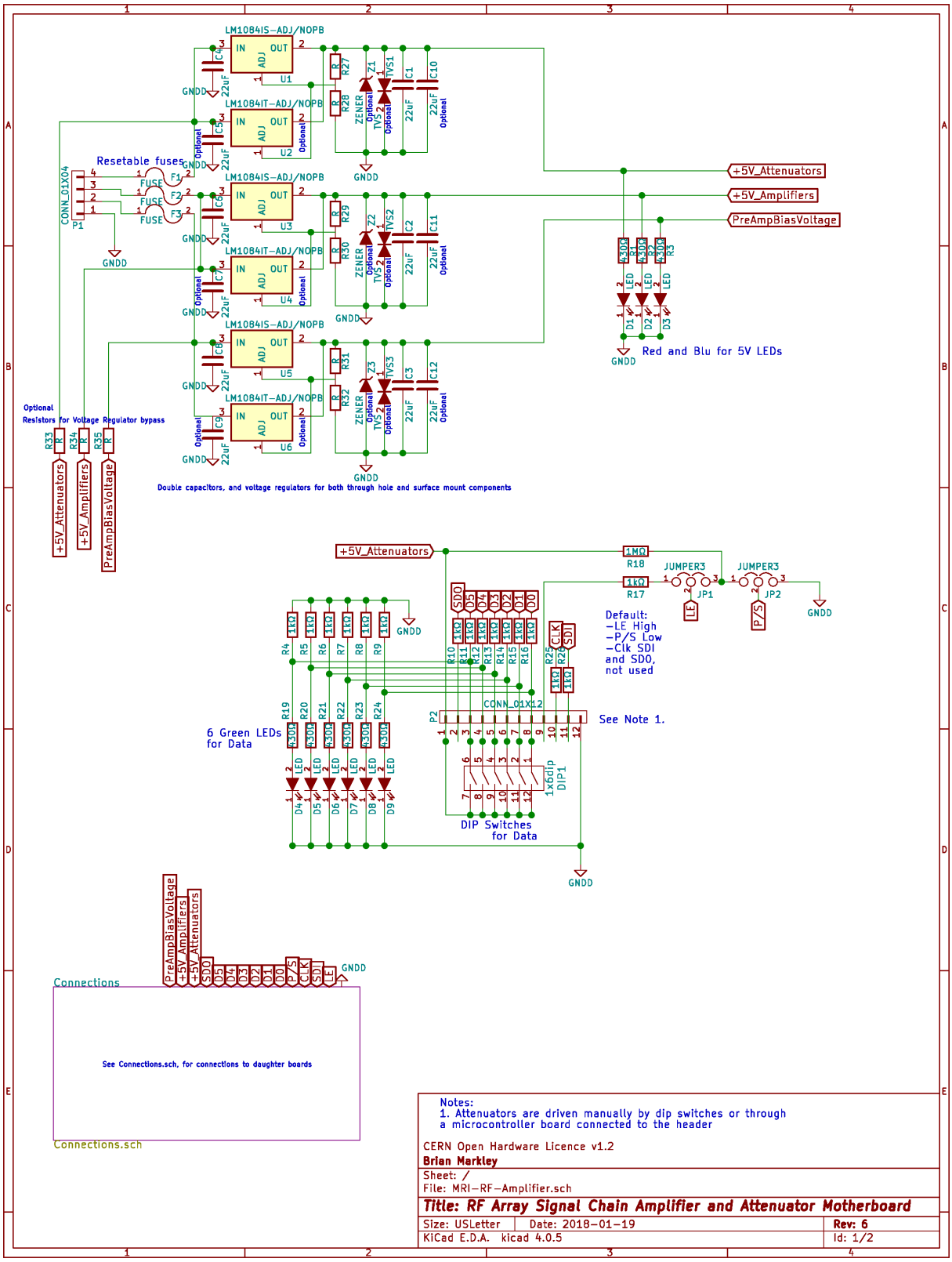


*Figure 3: Schematic of Motherboard power (top) and attenuator control circuitry (middle).*

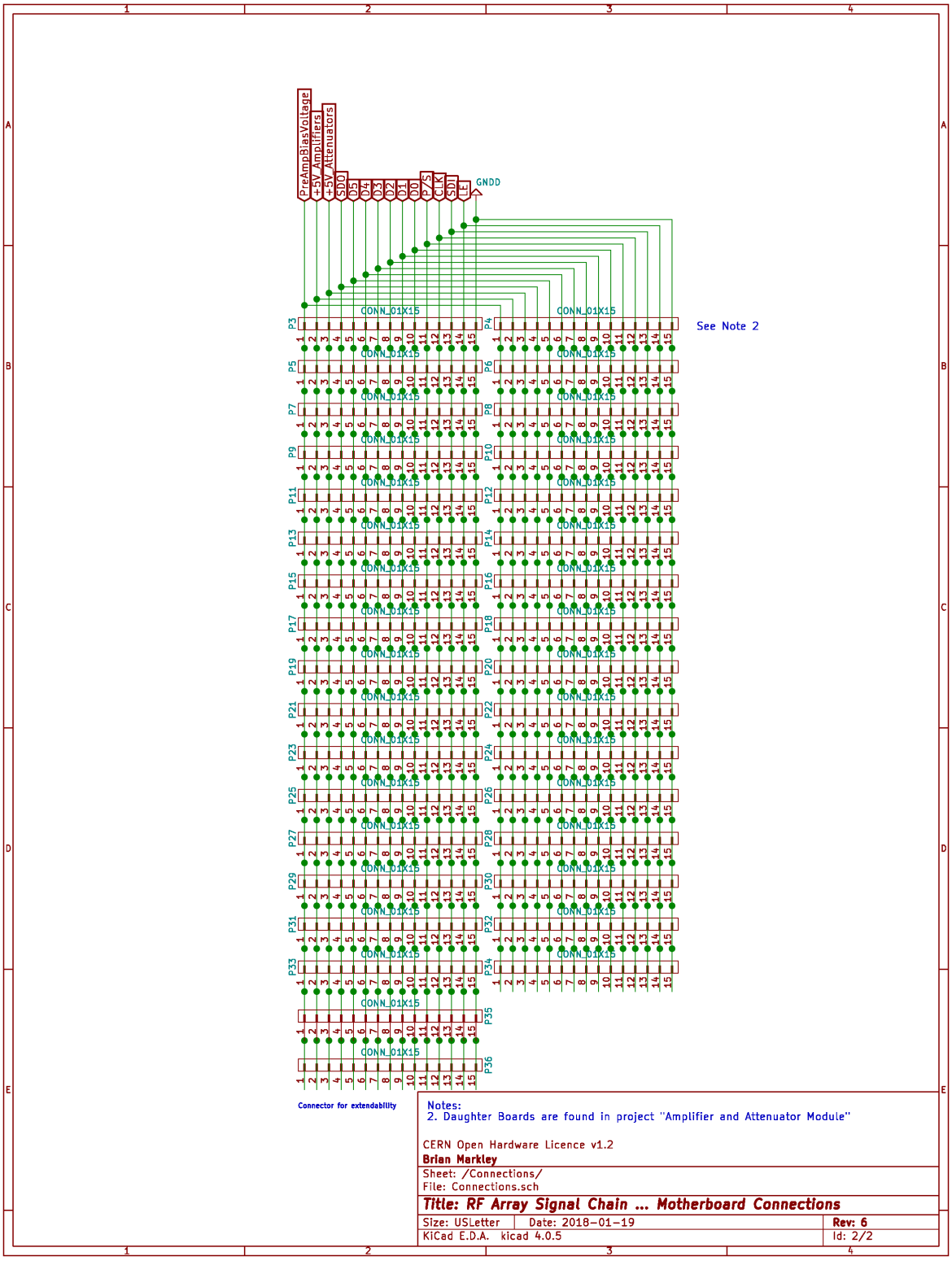


*Figure 4: Schematic of the Motherboard header array.*

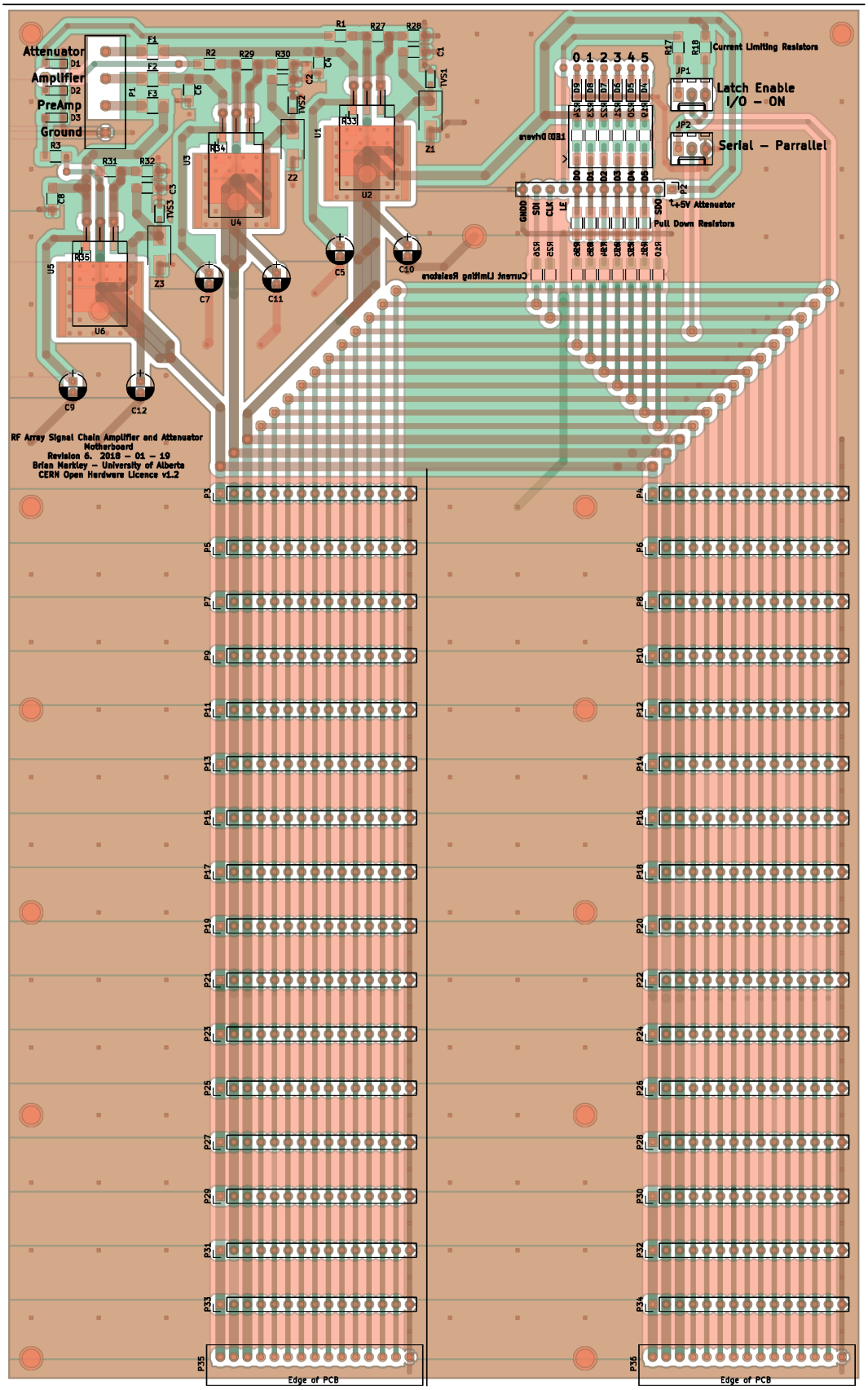


*Figure 5: Motherboard PCB layout.*

## Daughterboards

Each daughterboard contains an amplifier (gain block) and attenuator, as well as a bias tee for providing DC bias to an external 1st stage amplifier (preamp). To minimize PCB cost from our supplier, the design includes two identical boards on a standard half eurocard size (80 mm × 100 mm), with a v-score where they can be separated. The PCB is a two-layer design on a 1.6 mm thick FR4 substrate with 1 ounce copper (35 μm). The schematic and the PCB layout are included in Figure 6 and Figure 7, respectively.

### RF Transmission Line

A coplanar waveguide with ground was used with the grounds designed to act primarily as a shielding element. The gap between the ground and RF line is 3.0 mm, and the RF line is 3.0 mm wide, which produces a transmission line with a characteristic impedance of 50 Ω, at 200 MHz (calculated using the transmission line calculator included with KiCAD). Using a separate board for each channel ensures that the length and shape of the transmission lines, and thus frequency and phase response for each channel, are identical. Input and output RF connections on each board can be made using a variety of end-launch coaxial connectors (RF1 and RF2) for 1.6 mm boards such as SMA.

### Amplification

Broadcom MGA-30889 amplifiers (AMP1) were selected for this design due to their high gain, and stability with a relatively low noise figure [3]. This device is now listed as “end-of-life” and will become obsolete. However, by using a standard SOT89-3 package, a wide variety of alternate amplifiers (gain blocks) is available for replacement. If the system is to be used in a location with significant static magnetic field ($B_0$), the amplifiers’ performance should be measured in such conditions to ensure adequate performance. In many cases it is sufficient to rotate the orientation of the amplifiers relative to $B_0$ to restore performance equivalent to the zero-field case. Footprints for optional components are available to allow for filtering and matching needs of various amplifiers that use the SOT89 footprint. Pads for low-current LEDs (D1–D3) and associated current-limiting resistors (R1, R4, R5) are provided to allow visual confirmation of power states if desired.

### Bias Tees

The amplifiers are powered using a DC bias tee (L3 or L4 and neighboring capacitors) to inject DC into the RF output pin. A pre-amplifier located closer to the MRI RF coil may also be powered through the optional pre-amp DC bias tee (L1 or L2 and neighboring capacitors), upstream from the on-board amplifier. If possible, inductors should be chosen to have a self-resonance frequency (SRF) close to the Larmor frequency of operation. Like all other components in the design, inductors for the DC bias tees must be air-core, phenolic-core, or other non-magnetic types if they are to be exposed to the static magnetic field of the MRI scanner. Those containing ferromagnetic materials will saturate and present a much lower inductance than the nominal value.

### Attenuation

A 6-bit SKY12347-362LF attenuator[1] (ATTENUATOR1) was selected for the design due to its relatively economical cost and 31.5 dB range of operation with 0.5 dB resolution [4]. This robust chip is controllable by either a serial or parallel interface. For parallel use the jumpers

[1] currently listed by the manufacturer as “not recommended for new designs”. A drop-in alternate device has not been found.

on the motherboard need to be set to parallel mode (P/S pin set low) and the latch enable to ON (LE pin set high) as described in Control. The design may also be implemented without attenuators by soldering a short insulated wire across the attenuator's footprint to join input and output RF traces. This was done on the prototype with good results.

## Interfacing and Mounting

The attenuator control and power connections interface with the Motherboard using a right-angle male 2.54 mm header (P1). The RF signal input and output interface to coaxial cables using end-launch connectors such as SMA or others having similar footprints. Note that forces on these connectors can be enough to displace the daughterboards because the header alone is not rigid enough to provide strong mounting. Therefore, it is recommended that additional mechanical supports be provided using the mounting holes or using bulkhead-type RF connectors secured to a plate that is perforated to accommodate all 64 RF connections.

Care should also be taken to ensure that the daughterboards are not mated to the motherboard in the reverse orientation or with only a partial number of pins inserted (e.g., headers shifter by 1). No protection is provided against mating errors and damage may result to the Motherboard and/or Daughterboards.

## Futureproofing

The design is meant to be flexible so that the boards can be easily swapped out for maintenance or modification. Likewise, the daughterboard could be used independently of the motherboard as a single-channel device, although it may require power and protection circuitry external to the board. The amplifier SOT89 package is very common for gain blocks available from a variety of manufacturers, thus providing ample flexibility to the design. However, the QFN footprint of the attenuator is not commonly used – and there appears to be no drop-in replacement for this component. For this reason the daughterboard design may need to be modified for a different attenuator or if the current one becomes obsolete and is replaced with a newer model.

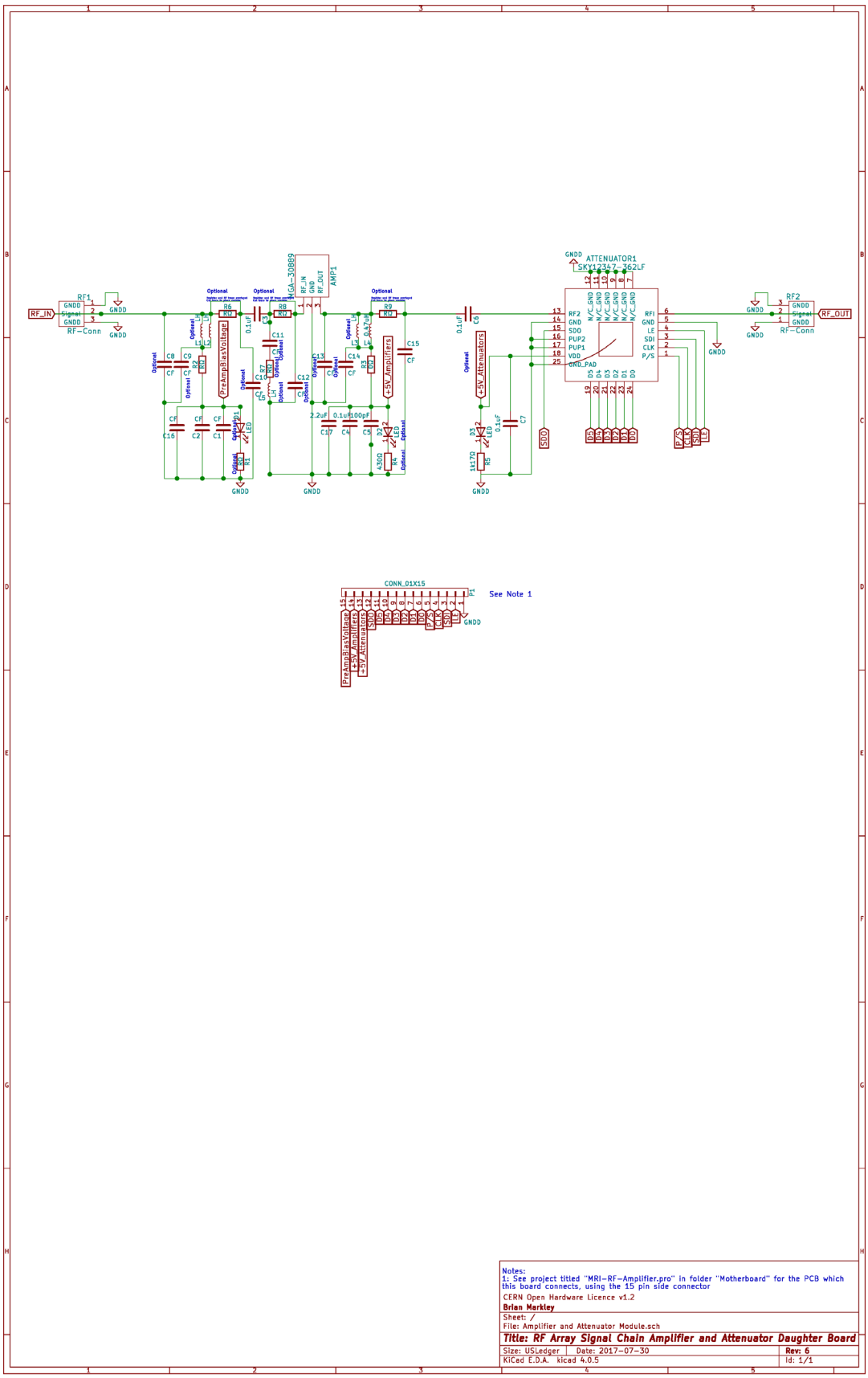


*Figure 6: Schematic of the Daughterboards.*

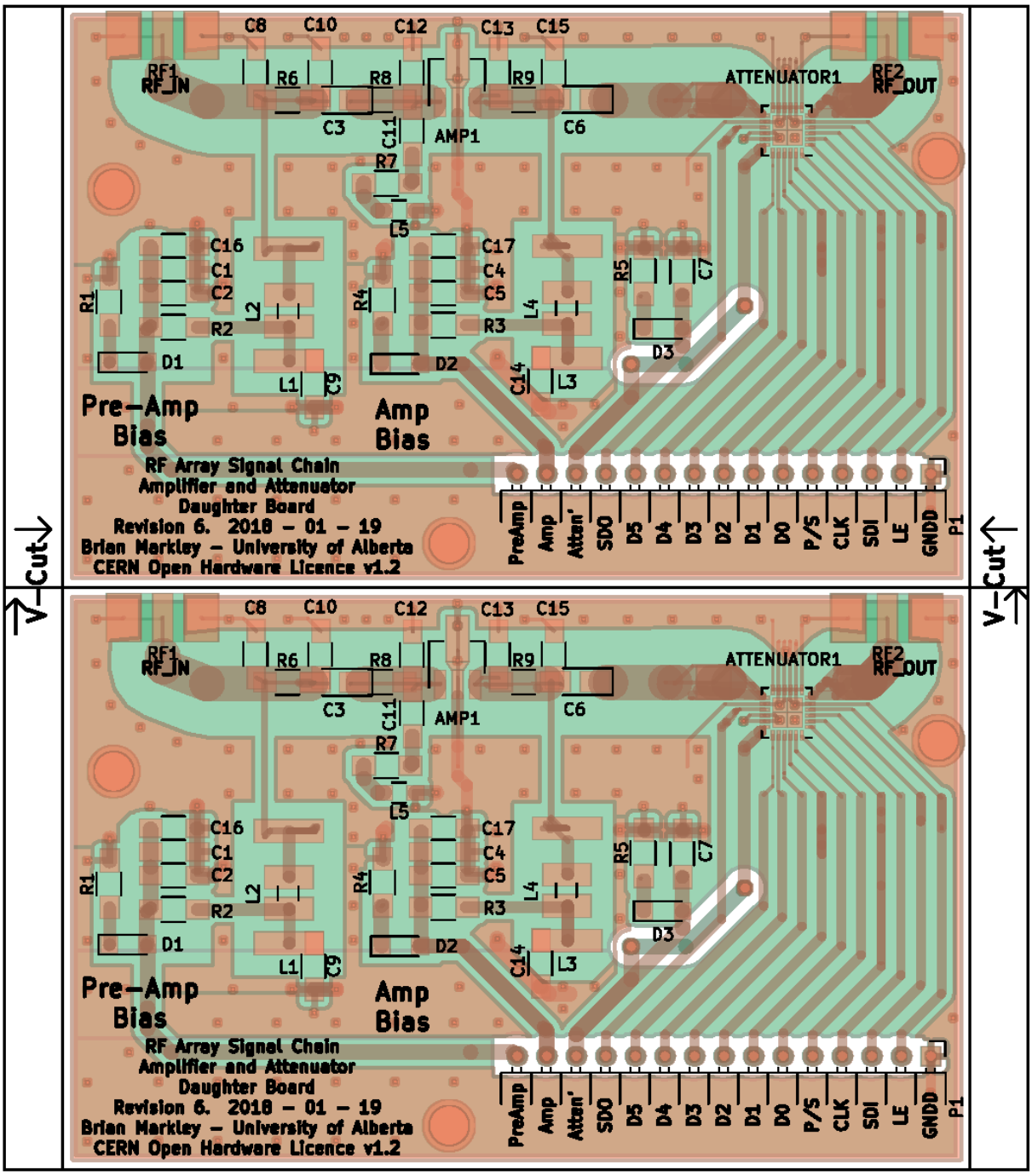


*Figure 7: PCB Layout of Daughterboards.*

# Performance as Built

The following tables summarize the performance of the system as built using the listed components. Performance using different components will vary.

## Absolute Maxima

| | | |
|---|---|---|
| Amplifier and Attenuator Voltage MotherBoard | 7 | volts |
| Amplifier Current MotherBoard | 4 | amps |
| Attenuator Current MotherBoard | 1 | amp |
| RF Input DaughterBoard | 20 | dBm |
| Amplifier Voltage DaughterBoard | 5.5 | volts |
| Attenuator Voltage (Power and Control) | 6.0 | volts |

## Specifications

| | | |
|---|---|---|
| $S_{21}$ (Gain) @ 200 MHz and -15 dBm VNA output | 15.4 | decibels |
| $S_{11}$ @ 200 MHz and -15 dBm VNA output | -19 | decibels |
| $S_{22}$ @ 200 MHz and -15 dBm VNA output | -15 | decibels |
| $S_{12}$ @ 200 MHz and -15 dBm VNA output | -20 | decibels |
| Maximum Attenuation | 31.5 | decibels |
| Attenuation increment | 0.5 | decibels |
| Attenuator Voltage Input | 5 | volts |
| Amplifier Voltage Input | 5 | volts |
| Control Voltage | 5 | volts |

# Design Package Details

The complete package for this design is available for download from https://github.com/dezanche/MRI_RF_hardware. In addition to this document it contains the license, PCB design, parts lists and component files for motherboard and daughterboards.

## License

This hardware design is provided under the terms of the CERN Open Hardware Licence v1.2 (available online at https://www.ohwr.org/licenses/cern-ohl/license_versions/v1.2) and any subsequent updates. Modifications of this design are allowed provided that the Licensee makes the modified documentation publicly available. The original repository is an appropriate location to publish such updated documentation.

According to §4.2 of the license, the authors kindly request “information about the type, quantity and dates of production of Products the Licensee has (had) manufactured” based on this design.

### PCB Files

The “MotherBoard” and “Amplifier and Attenuator Module” Folders contains the PCB design files, PDFs, and PCB production files (Gerber and drill files) – for the motherboard, and daughterboard. The PCB designs were produced using KiCAD (http://kicad-pcb.org/), which is free, open-source software.

### Parts

In the “Parts” folder there are parts lists for both PCBs, lists of compatible amplifiers, and datasheets for both the amplifier and attenuator.

## Acknowledgements

This design is a fork of a “Capstone” engineering team design project that included Luona Zhang, Tae Young Choi, and Joshua Fisher in addition to BDM. We thank Lukas Winter for helpful discussions on the topic of licensing, and acknowledge funding from the Natural Sciences and Engineering Research Council of Canada (grant RGPIN 04844).

## References

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